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Mixed-signal clock-skew calibration in time-interleaved analog-to-digital converters

David Camarero de La Rosa

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École Doctorale
d'Informatique,
Télécommunications
et Électronique de Paris

Thèse

présentée pour obtenir le grade de Docteur
de l'École Nationale Supérieure des Télécommunications

Spécialité : Électronique et Communications

David CAMARERO DE LA ROSA

Calibrage mixte du décalage de l'horloge
dans les convertisseurs analogique
numérique à entrelacement temporel

Soutenue le 1^{er} juin 2007 devant le jury composé de :

Patrick Garda	Président
Philippe Benabes	Rapporteurs
Dominique Dallet	
Yves Jaouen	Examineurs
Dominique Morche	
Patrick Loumeau	Directeur de thèse
Jean-François Naviner	

Mixed-Signal Clock-Skew Calibration in
Time-Interleaved Analog-to-Digital Converters

David Camarero

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Abstract

Clock-skew errors in time-interleaved ADCs importantly degrade the linearity of such converters. These nearly constant but unknown errors, that must not be confused with random jitter, prevent time-interleaved ADCs from performing uniform sampling. There are some different techniques of facing clock-skew errors : two-ranks sample-and-hold, channel randomization, global passive sampling, clock-edge reassignment, all-digital calibration techniques and all-analog calibration techniques. We propose a new kind of mixed-signal clock-skew calibration technique. Compared to the all-digital ones, ours distinguishes itself by the simplicity of its hardware elements. On the other hand, compared to the all-analog ones, ours keeps the inherent robustness of a digital clock-skew detection. A demonstrator shows the feasibility of our technique. This demonstrator consists of two 10-bit commercial ADCs, an FPGA to implement a digital clock-skew detector and an ASIC in a CMOS $0.35\ \mu\text{m}$ technology to implement a digitally trimmable multi-phase sampling clock generator. In this highly hostile environment of interconnected discrete components, our demonstrator can correct an initial clock-skew of thousands of picoseconds with a granularity of 1.8 picoseconds.

French Summary

Introduction

Le décalage de l'horloge dans les convertisseurs analogique numérique à entrelacement temporel (CAN ET) dégrade la linéarité de ces convertisseurs de façon appréciable. Ce décalage, considéré dans la pratique constant, est inconnu et il ne doit pas être confondu avec la gigue d'horloge sur l'instant d'échantillonnage. L'échantillonnage réalisé par des CAN ET subissant ce décalage n'est pas uniforme, mais nonuniforme de façon périodique.

Il y a différentes techniques permettant de contourner ce problème : l'échantillonnage à deux niveaux, brassage aléatoire de l'ordre d'utilisation des CANs, l'échantillonnage global passif, le ré assignement de l'horloge d'échantillonnage, des techniques de calibrage tout en numérique et des techniques de calibrage tout en analogique. Une technique de calibrage mixte, analogique numérique, est proposée dans cette thèse. Elle peut être divisée en deux sous systèmes : un détecteur numérique du décalage de l'horloge et un correcteur du décalage de l'horloge ajustable numériquement. Par rapport aux techniques de calibrage tout en numérique, celle proposée dans cette thèse est moins coûteuse en termes de surface et consommation. Par rapport aux techniques de calibrage tout en analogique, elle garde la robustesse face à la dispersion, propre aux circuits numériques.

Description Générale de la Technique

La fig. 1 montre un diagramme du démonstrateur conçu pendant cette thèse permettant de valider la technique de calibrage mixte du décalage de l'horloge. Il s'agit d'un CAN ET à deux voies, un FPGA où se trouve le détecteur numérique du décalage de l'horloge (DDSS) et un ASIC en technologie CMOS AMS 0.35 μm où est localisé le correcteur du décalage de l'horloge (DCDE). Le DDSS extrait l'information concernant le décalage de l'horloge d'échantillonnage de la voie 1, ϕ_1 , par rapport à l'horloge de la voie 0, ϕ_0 , considérée comme celle de référence et, donc, sans erreur. A partir de ces données, le DDSS indique au 1^{er} DCDE d'avancer ou retarder ϕ_1 pour aboutir à un échantillonnage uniforme (sans considérer la gigue aléatoire sur l'horloge). Le 1^{er} DCDE doit, donc, transformer l'information numérique fournie par le DDSS en un délai ajustable appliqué sur le parcours suivi par ϕ_1 . Les deux sous systèmes forment une boucle à contre réaction négative stable capable de suivre les lentes évolutions du décalage de l'horloge. Ce principe de calibrage, exposé ici pour le cas concret

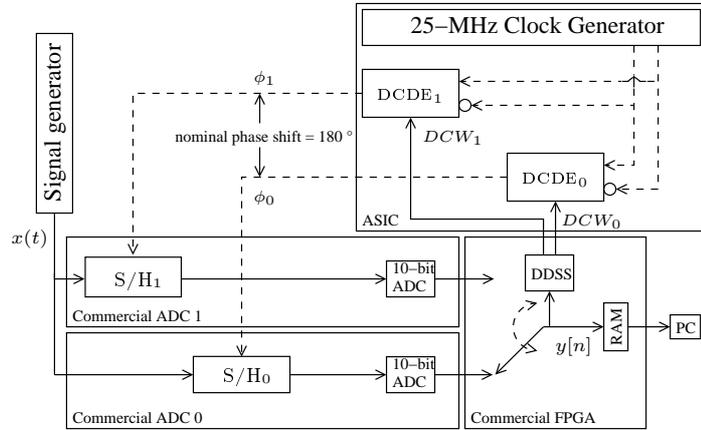


FIG. 1 – Diagramme du démonstrateur mettant en oeuvre la technique de calibrage mixte du décalage de l’horloge.

d’un CAN ET à deux voies, peut être généralisé à un nombre quelconque de voies M . Ceci est montré sur la fig. 2.

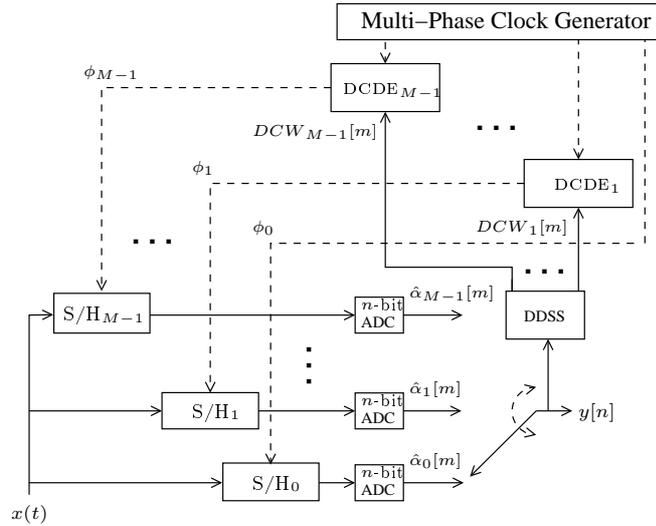


FIG. 2 – Diagramme générale de la technique de calibrage mixte du décalage de l’horloge.

A cause de la nature discrète des composants utilisés dans le démonstrateur, la fréquence d’échantillonnage de chaque CAN mis en parallèle est limitée à 25 MHz. D’ailleurs, le décalage de l’horloge attendu est de l’ordre d’un millier de picosecondes, c’est-à-dire, entre deux et trois ordres de grandeur supérieur au décalage de l’horloge attendu avec un CAN ET et un générateur d’horloge complètement intégrés. Néanmoins, un effort particulier a été réalisé pour parvenir à un décalage d’horloge résiduel, après calibrage, autour d’une picoseconde.

Pour effectuer le calibrage d’un CAN ET à deux voies, comme celui utilisé

dans le démonstrateur, juste un seul DCDE est nécessaire. Pourtant, pour des raisons de flexibilité, deux DCDEs ont été finalement implémentés.

Détecteur Numérique du Décalage de l'Horloge (DDSS)

La fig. 3 montre un diagramme du DDSS. Bien que notre démonstrateur

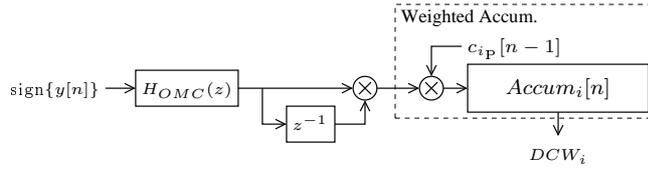


FIG. 3 – Diagramme du détecteur numérique du décalage de l'horloge.

soit conçu pour un CAN ET à deux voies, cette fig. 3 montre les composants nécessaires pour un nombre quelconque de voies M .

Le signal d'entrée du détecteur est physiquement un seul bit, celui qui porte l'information sur le signe du signal numérique. Ceci permet de réduire de façon très importante la complexité (en termes de surface et consommation) des circuits numériques utilisés pour la détection. Par ailleurs, il permet de rendre le DDSS robuste face aux disparités des gains de voies propres aux CANs ET.

La fonction de transfert du filtre numérique $H_{OMC}(z)$ est

$$H_{OMC}(z) = 1 - z^M.$$

Ce filtre est nécessaire pour rendre le DDSS robuste face aux disparités en sortie des voies pour une tension d'entrée nulle, propres aux CANs ET. L'accumulateur pondéré module le signal à son entrée par le signal de modulation $c_{iP}[n]$. Ce signal est un signal périodique, formé par des valeurs entières comprises entre $-(M-1)$ et $M-1$. Les vecteurs horizontaux de la matrice \mathbf{C} montrent une période de ces signaux de modulation, pour i compris entre 1 et M :

$$\mathbf{C} = \begin{pmatrix} M-1 & -1 & \dots & & -1 \\ M-2 & M-2 & -2 & \dots & -2 \\ \vdots & & & & \vdots \\ 1 & 1 & \dots & 1 & -(M-1) \end{pmatrix}.$$

Le choix précis de ces valeurs dépend de l'horloge d'échantillonnage à calibrer. Par exemple, pour le cas des CANs ET à deux voies, une période de $c_{iP}[n]$ est simplement $\{+1, -1\}$.

Correcteur du Décalage de l'Horloge Ajustable Numériquement (DCDE)

Les DCDEs font parti d'un générateur d'horloges d'échantillonnage. La fig. 4 montre un diagramme de ce générateur. Le DCDE est formé par un convertisseur

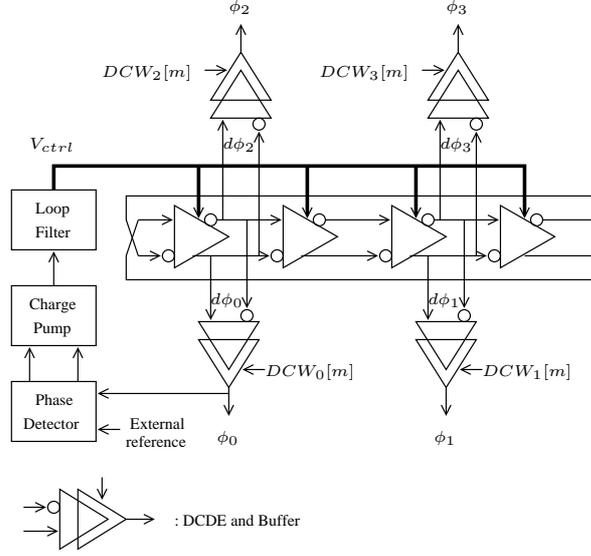


FIG. 4 – Diagramme du générateur d’horloges d’échantillonnage.

de signal d’horloge différentiel à non-différentiel (DTSEC) et un générateur de tension de polarisation ajustable numériquement (DTBG). Ceci est montré dans la fig. 5. Dans le cadre de notre démonstrateur, deux signaux d’horloge différen-

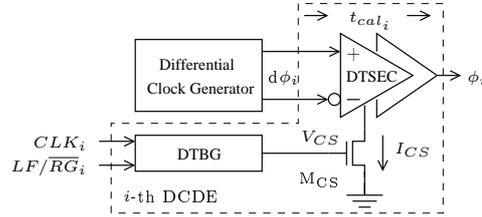


FIG. 5 – Diagramme du correcteur du décalage de l’horloge ajustable numériquement.

tiels, déphasés nominalement de 180° , sont convertis au format non-différentiel par les DTSECs. Le schéma électrique d’un DTSEC est montré dans la fig. 6. Ce circuit a la propriété de fournir à sa sortie un horloge d’échantillonnage dont le rapport cyclique est du 50%. Les sorties sont les horloges d’échantillonnage ϕ_0 et ϕ_1 . Dans cette conversion au format non-différentiel, deux délais supplémentaires, t_{cal_i} où $0 \leq i \leq 1$, sont ajoutés, respectivement, sur ϕ_0 et ϕ_1 . La valeur précise de chacun de ces délais dépend de la valeur d’un mot de contrôle numérique (DCW_i),

$$t_{cal_i} = t_{step} DCW_i,$$

où t_{step} est le pas temporel dans cette conversion numérique temps. Le décalage d’horloge après convergence, t_{res_i} , vérifie

$$|t_{res_i}| \leq t_{step}.$$

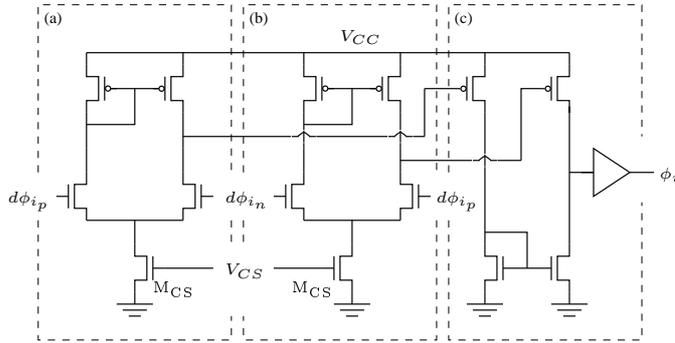


FIG. 6 – Schéma électrique du DTSEC.

Physiquement, la valeur de t_{cal_i} est modifiée par le changement du point de polarisation du DTSEC. Il y a un rapport presque linéaire entre la tension de polarisation V_{CS} et t_{cal_i} . Ceci est montré sur la fig. 7. Pour compléter la

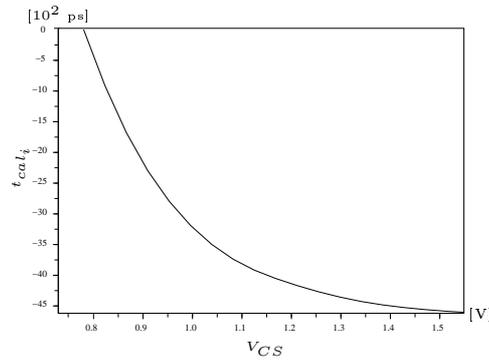


FIG. 7 – Graphique de l'évolution de t_{cal_i} par rapport à V_{CS} dans notre DTSEC.

conversion numérique temps, une conversion numérique tension doit être menée. Cela est fait au moyen du DTBG, dont un diagramme est montré dans la fig. 8. Il est formé par N sources de courant commutables par un bit de contrôle, dont

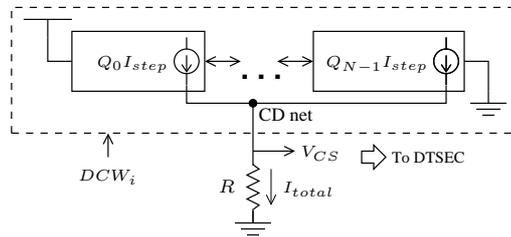


FIG. 8 – Diagramme du générateur de tension de polarisation ajustable numériquement (DTBG).

l'état est indiqué par Q_j , $0 \leq j \leq N - 1$. Ces bits de contrôle représentent, en codage thermométrique, le DCW_i . L'ensemble de ces bits de contrôle forment un registre à décalage bidirectionnel à entrée série, sortie parallèle. Quand un

bit de contrôle est en état logic bas, $Q_j = 0$, sa source de courant associée n'est pas active. Si un bit de contrôle est en état logique haut, $Q_j = 1$, sa source injecte un courant I_{step} dans le noeud CD net. Le courant global I_{global} est

$$I_{global} = \sum_{j=0}^{N-1} Q_j I_{step} = DCW_i I_{step}.$$

Ceci représente une conversion numérique courant. Enfin, une résistance R est chargée de la conversion courant tension.

Résultat des Mesures

La fig. 9 montre la densité spectrale de puissance du signal numérique de

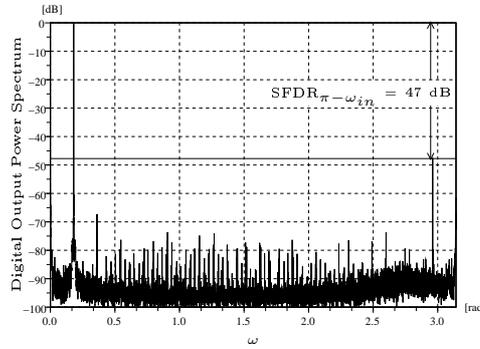


FIG. 9 – Densité spectrale de puissance du signal numérique de sortie avant le calibrage.

sortie de notre démonstrateur, avant le calibrage. La raie à gauche sur la fig. est associée au signal d'entrée, à faible fréquence. Une raie parasite, à haute fréquence, se trouve à droite sur la fig. Cette raie parasite, due uniquement au décalage d'horloge, limite fortement la linéarité du CAN ET. La fig. 10 montre la densité spectrale de puissance du signal numérique de sortie de notre

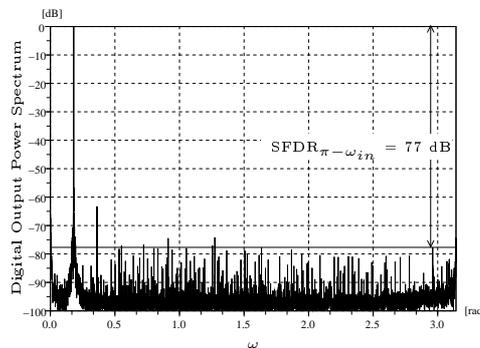


FIG. 10 – Densité spectrale de puissance du signal numérique de sortie après le calibrage.

démonstrateur, après le calibrage. Le signal d'entrée est le même que celui utilisé dans la fig. 9. Après le calibrage, il n'y a plus de raie parasite prépondérante due au décalage d'horloge. La fig. 11 montre la densité spectrale de puissance

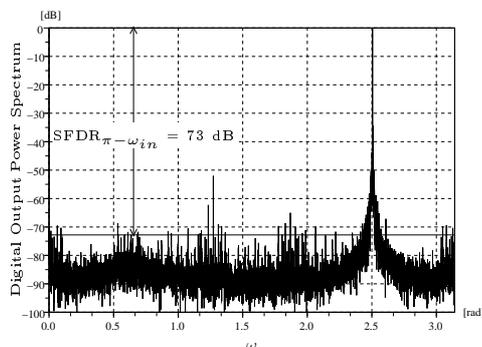


FIG. 11 – Densité spectrale de puissance du signal numérique de sortie après le calibrage pour un signal d'entrée à haut fréquence.

du signal numérique de sortie après le calibrage pour un signal d'entrée à haute fréquence. La raie à droite sur la fig. est associée au signal d'entrée. La raie parasite associée au décalage d'horloge se trouve maintenant à gauche sur la figure. A nouveau, les limitations en linéarité dues au décalage de l'horloge sont négligeables par rapport à d'autres non linéarités observables sur le spectre.

Le paramètre le plus important dans le sous système de correction est t_{step} . Les résultats des mesures de t_{step} sont résumés par l'histogramme montré dans la fig. 12. D'après ce histogramme, une granularité de 1,8 ps pour la correction est atteinte.

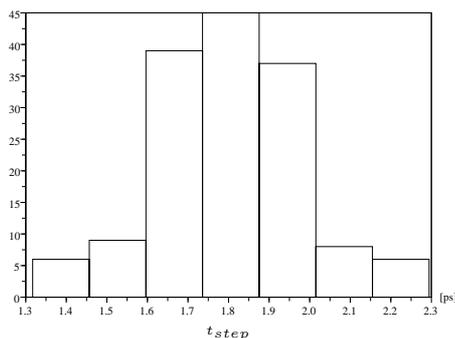


FIG. 12 – Histogramme de mesures de t_{step} .

Conclusions

Une nouvelle technique de calibrage de l'horloge d'échantillonnage est proposée et validée à l'aide d'un démonstrateur.

Le tableau 1 montre une comparaison simplifiée de toutes les techniques de

	Complexité	Robustesse	Rest. d'entrée	N. de voies
Mixte	Faible	Oui	Non	Quelconque
Tout en numérique	Élevée	Oui	Oui	2
Tout en analogique	La plus faible	Non	Non	Quelconque

TAB. 1 – Caractéristiques des techniques de correction.

correction proposées. Le même est fait concernant les techniques de détection dans le tableau 2.

Mixte	La plus faible	Oui	Oui	Quelconque
Tout en numérique	Faible	Oui	Oui	2
Tout en analogique	Élevée	Non	Non	Quelconque

TAB. 2 – Caractéristiques des techniques de détection.

La technique mixte développée dans cette thèse relie un faible coût matériel et une robustesse face aux dispersions pendant le processus de fabrication. Ceci constitue notre apport par rapport à l'état de l'art des techniques de calibrage de l'horloge d'échantillonnage.

Symbols and Abbreviations

f_s	(Global) Sampling frequency
M	Number of time-interleaved channels
i	Channel index
j	$\sqrt{-1}$
ϕ_i	i -th sampling clock
ϕ_{ip}	i -th pre-phase clock signal
T	(Global) Sampling period
m	Time index after downsampling or before upsampling
n	Time index
k	Alias signal index
ω	Normalized frequency
ω_{in}	Normalized sinusoidal input signal frequency
A_{in}	Sinusoidal input signal amplitude
ϕ_{in}	Sinusoidal input signal phase
t	Time
$t_{ideals_i}[m]$	Vector of ideal sampling instants for the i -th sampling clock
$t_{s_i}[m]$	Vector of actual sampling instants for the i -th sampling clock
t_{e_i}	i -th channel related clock-skew
t_{cal_i}	i -th channel related added calibration time
t_{res_i}	i -th channel related residual clock-skew
$t_{j_i}[m]$	Sampling jitter
t_{step}	Time step
$x(t)$	Analog input signal
$X(\omega/T)$	Fourier transform of the analog input signal
$y[n]$	Digital output signal
$Y(e^{j\omega})$	Discrete-time Fourier transform of the digital output signal
$\alpha_i[m]$	Sampled signal on the i -th channel
$\hat{\alpha}_i[m]$	Quantized sampled signal on the i -th channel
$\beta_i[n]$	Upsampled and delayed sampled signal on the i -th channel
\mathbb{Z}	Set of integer numbers
g_i	i -th channel gain
o_i	i -th channel offset
$n_{q_i}[m]$	Quantization noise
q_i	Quantification step size
$\delta(\cdot)$	Dirac's delta function or first derivative of a given function
FS	Quantizer full-scale
L	Length of a finite impulse response filter or transistor channel length

SV	Voltage-to-time conversion factor
VD	Digital-to-voltage conversion factor
DR	Number of static storage cells in a shift-register
μ	Carrier mobility
C_{ox}	Gate oxide capacitance
V_{TH}	Threshold voltage
V_{CC}	Supply voltage
σ	Standard deviation
r_{fg}	Cross-correlation of signals f and g
$\Re\{\cdot\}$	Real part of the argument
ADC	Analog-to-digital converter
BW	Bandwidth of the input signal
CMOS	Complementary metal-oxide-semiconductor
DC	Direct Current
DCDE	Digitally Controlled Delay Element
DCW	Digital Control Word
DDSS	Digital Detection Subsystem
DFT	Discrete Fourier Transform
DSCT	$\Delta\Sigma$ continuous-time
DSDT	$\Delta\Sigma$ discrete-time
DTBG	Digitally trimmable bias generator
DTCG	Digitally trimmable clock generator
DTSEC	Differential-to-single-ended converters
FFT	Fast Fourier Transform
FIR	Finite impulse response
FPGA	Field programmable gate array
LSB	Least significant bit
MUX	Multiplexer
NMOS	N-channel metal-oxide-semiconductor
MSB	Most significant bit
OSR	Oversampling ratio
Opamp	Operational amplifier
PLL	Phase-locked loop
PMOS	P-channel metal-oxide-semiconductor
S/H	Sample-and-hold
SFDR	Spurious free dynamic range
SNDR	Signal to noise and distortion ratio
SoC	System-on-a-chip

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Chapter 1

Introduction

1.1 Motivations

The evolution of telecommunications tends toward an optimization of the radio resources. This can be done by increasing the transmission bit rates as well as by designing adaptive radio devices able of taking advantage of several communication standards. On the other hand, the evolution of integrated circuits tends toward major possibilities of the available digital signal processing in a single chip. The conjunction of both trends makes arise the Software-defined Radio concept. In this context, operations on the received signal traditionally carried out by analog circuits are entrusted to digital ones. Nowadays, the available resolution and speed on the analog-to-digital conversion limits this new conception of a radio receiver. Parallel analog-to-digital converters (ADCs) seem to be the best suited way of increasing analog-to-digital conversion rates while keeping a high resolution in complementary metal-oxide-semiconductor (CMOS) technologies. This thesis prolongs the efforts on this area carried out in the research group where it has been done. The thesis about parallel structures shown in [46] and [44] have been previously accomplished in this same research group.

Among all the possible parallel ADCs, those based on time-interleaved techniques are conceptually the simplest ones. It seems reasonable that before attempting to design more sophisticated structures, the implementation of time-interleaved ADCs should be completely mastered. Three intrinsic problems prevents us from reaching this goal : gain-mismatch, offset-mismatch and clock-skew. Among these problems, clock-skew is the more challenging. There are two reasons for that :

First, clock-skew causes a phase error on the sampled signal. This makes difficult to perform a clock-skew estimation, because it cannot be done with a simple power estimation as in some gain calibrations. Another kind of more sophisticated estimations must be employed.

Second, the clock-skew correction techniques based on purely digital methods are found to be extremely complex. As described later in this work, they consist of a bank of adaptive filters, clocked at the full sampling frequency. Even if they can be easily implemented with today's technologies, from a low-area and low-power point of view, another solution would be preferable.

This thesis attempts to give some answers to both challenges.

1.2 Organization of the Thesis

The organization of the thesis is as follows :

Chapter 2 gives an overview of the different types of parallel ADCs, the aim of such converters, and the position of time-interleaved ADCs among them. Besides, the main effects of mismatches due to fabrication dispersion in time-interleaved ADCs are reviewed, specially those related to clock-skew.

Chapter 3 classifies a wide range of previously proposed techniques to minimize or cancel clock-skew effects. This range includes techniques as different as channel randomization or clock-skew calibration. All along this classification, detailed reviews are carried out. They pointed out some pending research works and mistakes. The conclusion of this chapter focuses on a comparison between the reported clock-skew calibration techniques. This is useful to appreciate the research contributions of the new calibration technique proposed straight afterwards in this work.

Chapter 4 expounds our new calibration technique. From the classification on Chapter 3, it is called Mixed-Signal Clock-Skew Calibration Technique. The exposition is mainly divided into two parts, one dealing with the correction technique (Section 4.3), the other with the detection technique (Section 4.4). The conclusion of this chapter compares as quantitatively as possible the existing calibration techniques and the new one. Some aspects of this comparison depend on the implementation. Since this chapter deals only with the principle of operation, the comparison is completed in Chapter 5, where one possible implementation is detailed.

Chapter 5 presents a demonstrator designed to experimentally verify the Mixed-Signal Clock-Skew Calibration Technique. This demonstrator has a double aim : First, to complete the comparison carried out in the previous chapter. Second, to verify the feasibility of our calibration technique. This last point is fully developed in the next chapter.

Chapter 6 discusses the test and measurements from our demonstrator. Achievements, design failures and second order effects are highlighted. This first experience is globally considered as extremely useful to succeed again in future implementations.

Chapter 7 shows conclusions, highlights the research contributions, and proposes some perspectives.

Among the appendices, let us stand out the following ones selected by their research contributions :

Appendix A, where the analytical expressions of the digital correction filters for the M -channels general case of the Jamal *et al.*'s Calibration Technique (see Subsection 3.4.1) are shown.

Appendix C, where some unnoticed limitations of the measurement technique proposed in Jin and Lee's Calibration (see Subsection 3.4.1) are revealed in.

Chapter 2

Parallel ADCs

2.1 Overview of Parallel ADCs

We define a parallel ADC as a set of low conversion rate single ADCs that provides a higher global conversion rate, denoted f_s . Generally, f_s is M times that of a single ADC, where M is the number of single ADCs, also called channels. This definition allows us to distinguish between this kind of architecture and other ADCs that can be occasionally called parallel ADC. It is the case of, for example, flash converters, where comparators perform a parallel conversion of a single sample, or pipeline converters, where low resolution converters are configured in cascade mode. In both cases, the addition of a new comparator or low resolution converter increases the digital output resolution, while the conversion rate remains the same.

The main motivation to make parallel ADCs is to attain high output resolutions at high conversion rates. Fig. 2.1 shows a selection of published CMOS

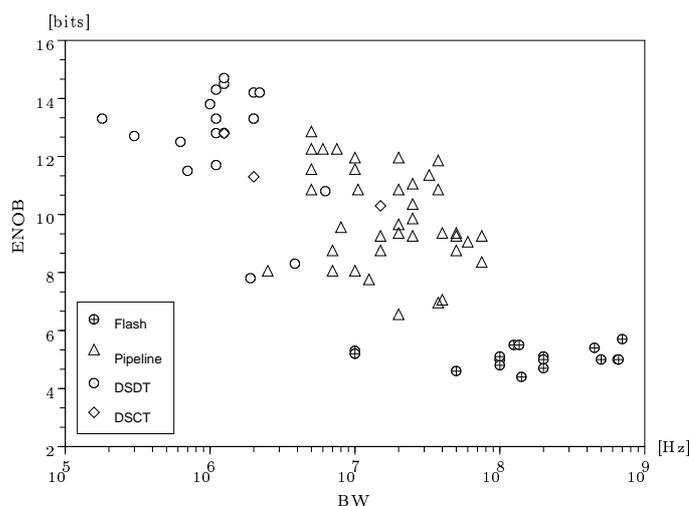


Figure 2.1: Published CMOS ADCs placed in the ENOB versus BW space.

ADCs from 1998 to 2005 [51]. Four types of ADCs are considered : flash, pipeline, $\Delta\Sigma$ discrete-time (DSDT) and $\Delta\Sigma$ continuous-time (DSCT). The vertical axis shows the effective number of bits (ENOB) while the horizontal axis shows the bandwidth (BW) of the input signal, i.e., $f_s/2$ for Nyquist-type ADCs as flash and pipeline and $f_s/(2 \cdot \text{OSR})$ for $\Delta\Sigma$ ADCs, where OSR denotes the oversampling ratio. Parallel ADCs aspire to fill the space of high resolution and conversion rate at the top right of the figure.

Parallelism can also reduce the power consumption at a given sampling rate and resolution. On one hand, for a single ADC, the increase in power is not a linear function of f_s . On the other hand, in parallel ADCs, the number of channels is an extra parameter that can be wisely chosen to minimize power consumption, because of the reduced bias currents used in opamps if low rate switched-capacitors circuits are used. With regard to the area, depending on the architecture, opamps can be shared between the channels [43], so the increase in area is not necessarily a linear function of M .

Parallel ADCs suffer from several fabrication mismatches that deteriorate their performances. The use of quadrature mirror filter banks [64] have been proposed to make robust parallel ADCs. Moreover, as in speech and image applications, the quadrature mirror filters banks allow to use a subband coding, by means of two different filter banks : the analysis and the synthesis filter bank. There are ADC proposals that use a discrete-time analysis filter bank [53] and others that use a a continuous-time one [67]. Fig. 2.2 shows a diagram of the

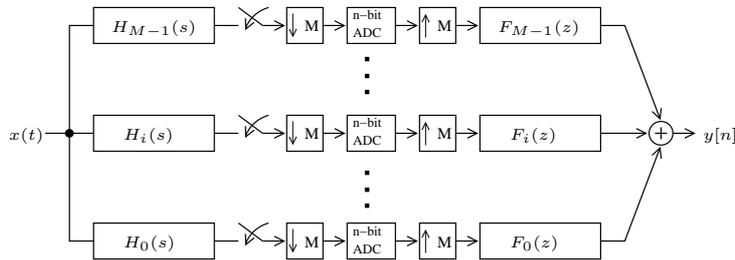


Figure 2.2: Diagram of a hybrid filter bank ADCs.

latter proposals, called hybrid filter bank ADC, where $H_i(s)$ are the transfer functions of the analysis filters in the S-domain and $F_i(z)$ are the transfer functions of the synthesis filters in the Z-domain.

Unfortunately, these architectures also suffer from the fabrication mismatches they are supposed to compensate and demand a higher complexity than other simpler parallel ADCs. Time-interleaved ADCs are a particular case of these architectures.

2.2 Principle of Time-interleaved ADCs

The time-interleaved architecture is conceptually one of the simplest ways among the different options of implementing a parallel ADC [68]. Its aim is to attain high conversion rates by means of just using identical single ADCs synchronized by different clock phases. While the total resolution ideally equals that of a single ADC, the global conversion rate is that of a single ADC times M , the

number of used ADCs. Fig. 2.3 illustrates the parallel operation, where S/H

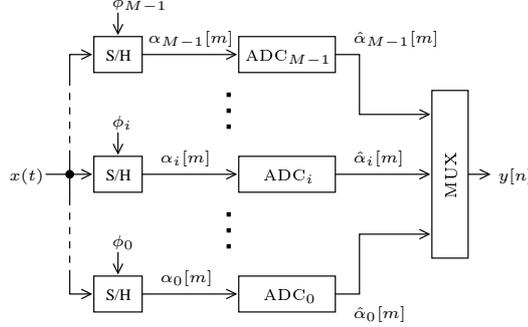


Figure 2.3: Diagram of a general time-interleaved ADC.

stands for sample-and-hold. Fig. 2.4 shows the timing of this time-interleaved

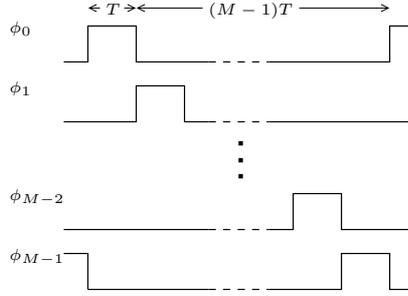


Figure 2.4: Timing for a general time-interleaved ADC.

ADC, necessary to understand the time-interleaved concept. As shown in the figures, there are M channels, $M \geq 2$. The i -th channel receives the sampling clock ϕ_i , nominally delayed T seconds from ϕ_{i-1} , $1 \leq i \leq M-1$, where ϕ_0 is considered the time reference. The ideal sampling instants for the i -th channel are :

$$t_{ideal\ s_i}[m] = MTm - (M-1-i)T, \quad m \in \mathbb{Z}, \quad (2.1)$$

where \mathbb{Z} denotes the set of integer numbers. A multiplexer arranges the ADC outputs $\hat{\alpha}_i[m]$ to form one global digital output $y[n]$, $n \in \mathbb{Z}$, in such a way that

$$y[n] = \sum_{i=0}^{M-1} \hat{\alpha}_i \left[\frac{n-i}{M} \right], \quad (2.2)$$

where

$$\hat{\alpha}_i \left[\frac{n-i}{M} \right] = \begin{cases} \hat{\alpha}_i \left[\frac{n-i}{M} \right], & \text{if } \left[\frac{n-i}{M} \right] \in \mathbb{Z}, \\ 0, & \text{if } \left[\frac{n-i}{M} \right] \notin \mathbb{Z}, \end{cases} \quad (2.3)$$

so

$$y[n] = \{ \dots, \hat{\alpha}_{M-1}[-1], \hat{\alpha}_0[0], \dots, \hat{\alpha}_{M-1}[0], \hat{\alpha}_0[1], \dots \}, \quad (2.4)$$

where $\underline{\cdot}$ denotes the $n=0$ sample.

This structure provides a global sampling rate $f_s = 1/T$, while the individual sampling rate of each single ADCs is f_s/M , i.e., M times lower. It allows to

relax the single ADC constraints and increase the overall sampling rate, two incompatible goals when considering just a single ADC.

The diagram of fig. 2.5 represents a fully discrete-time model for an ideal

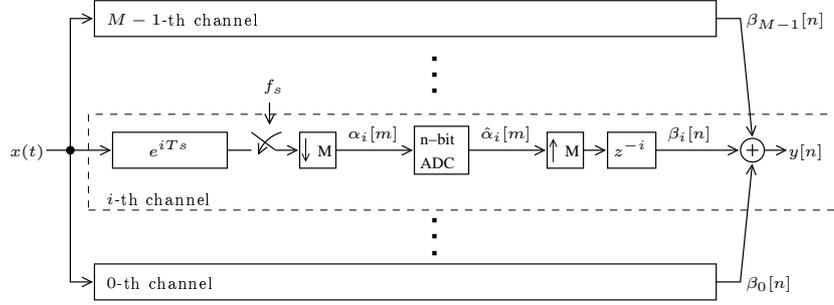


Figure 2.5: Diagram of a discrete-time model of an ideal time-interleaved ADCs.

time-interleaved ADC. It is used to analytically write the frequency domain expression of $y[n]$, denoted $Y(e^{j\omega})$, from the frequency domain expression of the analog input $x(t)$, $X(\omega/T)$, where ω denotes the normalized frequency, t denotes the time, and $j = \sqrt{-1}$. If the quantification is neglected, for an ideal time-interleaved ADC, $Y(e^{j\omega})$ is [23] :

$$Y(e^{j\omega}) = \sum_{i=0}^{M-1} \beta_i(e^{j\omega}), \quad (2.5)$$

where,

$$\beta_i(e^{j\omega}) = \frac{1}{MT} \sum_{k=-\infty}^{\infty} X\left(\frac{\omega}{T} - \frac{2\pi}{MT}k\right) e^{-j\frac{2\pi}{M}ik}, \quad k \in \mathbb{Z}. \quad (2.6)$$

Substituting (2.6) in (2.5) we have :

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{\infty} X\left(\frac{\omega}{T} - \frac{2\pi}{T}k\right), \quad (2.7)$$

i.e., the spectrum of a signal sampled at a rate $1/T$. The alias terms in (2.6) for $k \neq lM$, $l \in \mathbb{Z}$, cancel each others when the signals from all the channels are added. It can be easily understood with a geometric representation of the values of the exponential components of these alias. For a fixed k , $k \neq lM$, these values are uniformly placed on the complex unity circle when they are evaluated considering i . Once added, they cancel each others. On the other hand, for $k = lM$, the result of the addition is M . Fig. 2.6 illustrates, for a $M = 4$ channels example, a set of alias signals where only the alias for $k = 0$ and $k = 4$ are the desired ones.

In the previous paragraph, the single ADCs are assumed to be identical. However, in today's analog technologies, it is not true even for identically designed and fabricated ADCs [49]. Fabrication dispersion modifies the characteristics of every single ADCs in an uncontrolled manner, that often is handled from a probabilistic point of view [38]. These mismatch errors are a serious drawback of time-interleaved ADCs. The three main mismatches are gain mismatch, offset mismatch, and clock-skew, although other mismatch errors also

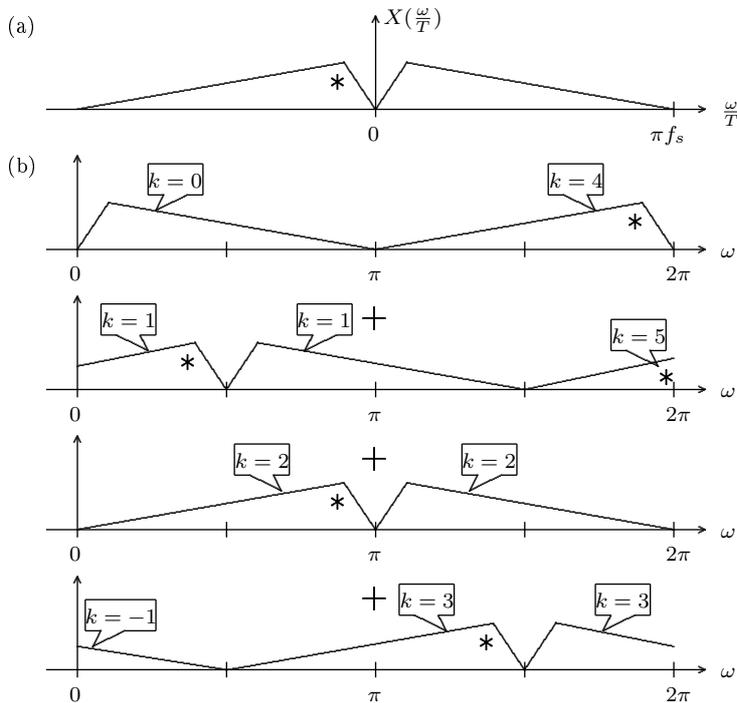


Figure 2.6: (a) Bandlimited analog input signal. (b) Alias decomposition of $\beta_i[n]$ for $0 \leq \omega \leq 2\pi$.

occur [37]. They degrade the dynamic performance of the global converter, reducing the linearity measured in terms of the spurious free dynamic range (SFDR) observed at the spectrum of the digital output. In fact, when characterizing ADCs, it is common to use histogram methods. But mismatch errors in time-interleaved ADC are not well detected in such tests, but rather in fast Fourier transform (FFT) spectrum testing methods [58]. The mismatch effects are discussed in detail in Section 2.3. Of course, besides these errors, the time-interleaved ADCs also suffers from the usual errors of any ADC, e.g., sampling jitter, nonlinearities, gain, offset, *etc.*

2.3 Mismatch in Time-interleaved ADCs

The gain and offset mismatches mainly arise from the single ADCs. Fig 2.7 intuitively shows the extraction of these characteristics from a non-ideal transfer function of a single ADC. Analytically, the discrete-time input of the i -th single ADC, $\alpha_i[m]$, and its output, $\hat{\alpha}_i[m]$, are related by :

$$\hat{\alpha}_i[m] = g_i \alpha_i[m] + o_i + n_{q_i}[m], \quad (2.8)$$

where g_i and o_i are its particular gain and offset, and $n_{q_i}[m]$ is the quantization noise that depends on the quantification step size, q_i . For a given single ADC, g_i and o_i are assumed to be constant, independent of the signal and unknown. On the other hand, they are different for each single ADC. With regard to the

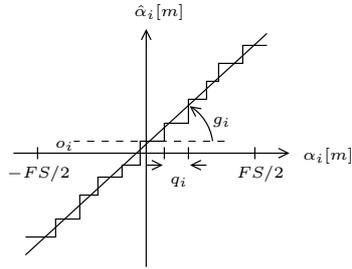


Figure 2.7: Plot of the transfer function of an ADC with gain and offset errors.

quantization noise, the nominal q_i s as well as the quantizer full-scale, FS , of each single ADC are the same for all those in a given time-interleaved ADC. From now on, the quantization noise will be neglected unless otherwise stated.

Clock-skew arises from mismatches in the multi-phase clock generator system and on-chip clock distribution. If clock-skew is present, the actual sampling instants for the i -th channel become :

$$t_{s_i}[m] = MTm - (M - 1 - i)T + t_{e_i} + t_{j_i}[m], \quad (2.9)$$

where t_{e_i} is the clock-skew associated to that channel and $t_{j_i}[m]$ is the sampling jitter. The clock-skew is an unknown constant timing offset added to the ideal sampling instants. It is different for each channel. Clock-skew must not be confused with sampling jitter, generally considered as a Gaussian random variable with zero mean. Sampling jitter will be neglected from now on unless otherwise stated. Fig. 2.8 shows clock-skew effects on the timing for a general

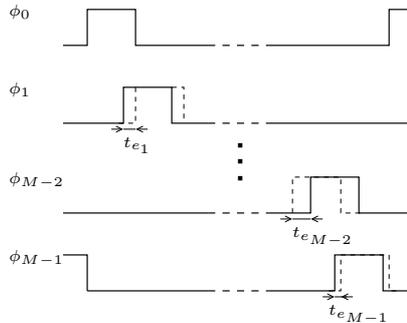


Figure 2.8: Timing with clock-skew for a general time-interleaved ADC.

time-interleaved ADC. The dashed lines represent the ideal sampling clocks. The continuous lines represent the actual sampling clocks, shifted in time in comparison with the ideal ones. As a result of clock-skew in time-interleaved ADCs, we get a periodically nonuniformly sampled signal.

Fig. 2.9 redraws the time-interleaved ADC in fig. 2.3 to incorporate the cited mismatches [52] [38]. The following paragraphs show the effects of the three types of mismatches one by one, assuming that the two others do not exist.

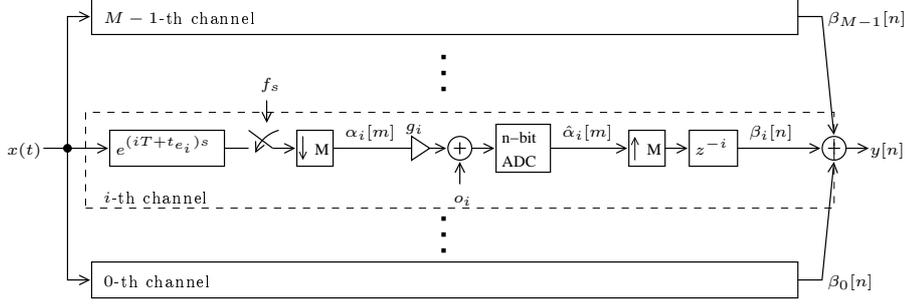


Figure 2.9: Diagram of a discrete-time model of a non-ideal time-interleaved ADC.

2.3.1 Offset Mismatch

Analytical Output Spectrum with Offset Mismatch

If only offset mismatch errors are present, the digital spectrum of $y[n]$ is [23] :

$$\begin{aligned}
 Y(e^{j\omega}) &= \frac{1}{T} \sum_{k=-\infty}^{\infty} X\left(\frac{\omega}{T} - \frac{2\pi}{T}k\right) \\
 &\quad + 2\pi \sum_{k=-\infty}^{\infty} O_k \cdot \delta\left(\omega - \frac{2\pi}{M}k\right),
 \end{aligned} \tag{2.10}$$

where

$$O_k = \frac{1}{M} \sum_{i=0}^{M-1} o_i \cdot e^{-j\frac{2\pi}{M}ik}, \tag{2.11}$$

and $\delta(\cdot)$ denotes the Dirac's delta function. The δ -spikes associated to O_k are independent of the signal and could reduce the signal to noise and distortion ratio (SNDR) and the SFDR of the time-interleaved ADC.

Fig 2.10 illustrates the digital output spectrum for a $M = 4$ channels time-interleaved ADC with offset mismatch for a sinusoidal input and 10-bit quantification. To clearly observe the effects of the offset mismatch, four deliberately high o_i values are chosen : 10 times the quantification step size, q_i , $15q_i$, $-17q_i$ and $22q_i$. The input signal peak-to-peak amplitude is almost FS .

SNDR Loss Due to Offset Mismatch

The SNDR is defined as :

$$\text{SNDR} = 10 \log \left(\frac{P_s}{P_e} \right), \tag{2.12}$$

where P_s is the signal power and P_e is the error power. For a sinusoidal input signal,

$$x(t) = A_{in} \cos\left(\frac{\omega_{in}}{T}t\right), \tag{2.13}$$

$P_s = A_{in}^2/2$. Assuming o_i to be Gaussian random variables with zero mean and variance σ_o^2 , the mean error power is σ_o^2 [23]. The SNDR for the mean

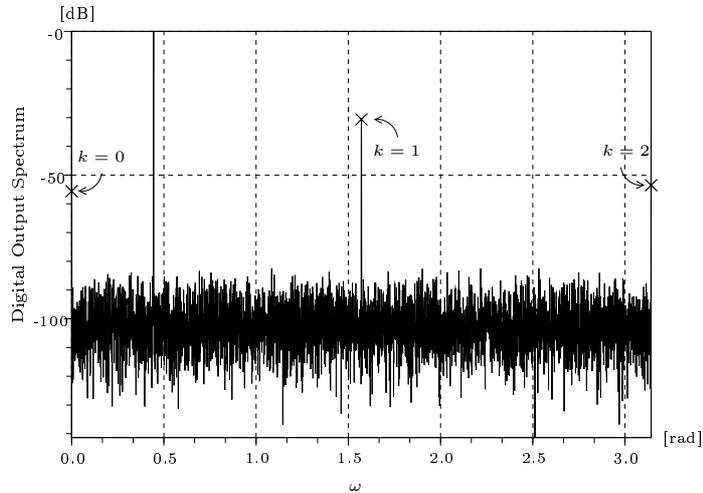


Figure 2.10: Plot of the digital output spectrum of a $M=4$ channels time-interleaved ADC with offset-mismatch for a sinusoidal input and 10-bit quantification.

error power is :

$$\text{SNDR} = 10 \log \left(\frac{A_{in}^2}{2\sigma_o^2} \right). \quad (2.14)$$

Calibration of Offset Mismatch

There are several solutions to correct offset mismatch : [15] [27] [20] [14] [44]. Providing with more insight in these solutions is out of the scope of this work.

2.3.2 Gain Mismatch

Analytical Output Spectrum with Gain Mismatch

If only gain mismatch errors are present, the digital spectrum of $y[n]$ is [23] :

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{\infty} G_k \cdot X \left(\frac{\omega}{T} - \frac{2\pi}{MT} k \right), \quad (2.15)$$

where

$$G_k = \frac{1}{M} \sum_{i=0}^{M-1} g_i \cdot e^{-j \frac{2\pi}{M} ik}. \quad (2.16)$$

For a sinusoidal input signal, the alias terms associated to G_k are placed at frequencies that depend on ω_{in} :

$$\left[\omega_{in} + \frac{2\pi}{M} k \right] \text{ and } \left[2\pi - \left(\omega_{in} + \frac{2\pi}{M} k \right) \right]. \quad (2.17)$$

It is illustrated in fig. 2.11 for a $M=4$ channels time-interleaved ADC, where the gain errors are arbitrarily chosen to be -5% , 3% , 2% , and -3% . Unlike

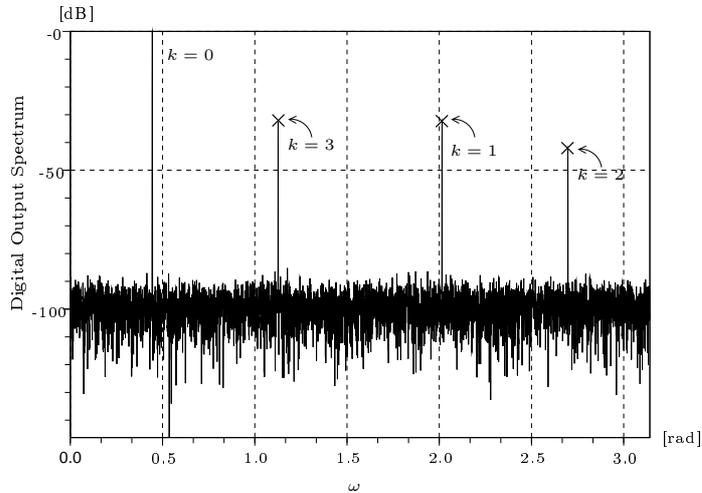


Figure 2.11: Plot of the digital output spectrum of a $M=4$ channels time-interleaved ADC with gain-mismatch for a sinusoidal input and 10-bit quantification.

the frequencies of the alias terms, the values of G_k are independent of the input signal. These alias terms could reduce the SNDR and the SFDR of the time-interleaved ADC.

If there are no errors, i.e., $g_i = g \forall i$, then

$$G_k = \begin{cases} g & \text{for } k = Ml, l \in \mathbb{Z} \\ 0 & \text{for all other } k, \end{cases} \quad (2.18)$$

and the alias terms centered at $\omega = \frac{2\pi}{M}k$, $k \neq Ml$ are cancelled giving the ideal spectrum shown in (2.7) multiplied by G_0 , the overall gain.

SNDR Loss Due to Gain Mismatch

For a sinusoidal input signal, assuming g_i to be Gaussian random variables with g mean and variance σ_g^2 , the SNDR for the mean error power is [23] :

$$\text{SNDR} \approx 10 \log \left(\frac{g}{\sigma_g} \right) - 10 \log \left(1 - \frac{1}{M} \right), \quad (2.19)$$

provided that G_0 can be any value slightly different from the nominal gain.

Calibration of Gain Mismatch

There are several solutions to correct gain mismatch : [27] [20] [14] [44]. Providing with more insight in these solutions is out of the scope of this work.

2.3.3 Clock-Skew

Analytical Output Spectrum with Clock-Skew

From the digital spectrum analysis technique for periodically nonuniformly sampled signals, if only clock-skews are present, the digital spectrum of $y[n]$ is [29] :

$$Y(e^{j\omega}) = \sum_{i=0}^{M-1} \beta_i(e^{j\omega}), \quad (2.20)$$

where,

$$\beta_i(e^{j\omega}) = \frac{1}{MT} \sum_{k=-\infty}^{\infty} e^{j(\omega - \frac{2\pi}{M}k) \frac{t_{e_i}}{T}} e^{-j \frac{2\pi}{M} ik} X\left(\frac{\omega}{T} - \frac{2\pi}{MT}k\right). \quad (2.21)$$

(2.20) can be rewritten as :

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{\infty} S_k(\omega) X\left(\frac{\omega}{T} - \frac{2\pi}{MT}k\right). \quad (2.22)$$

where

$$S_k(\omega) = \frac{1}{M} \sum_{i=0}^{M-1} e^{j(\omega - \frac{2\pi}{M}k) \frac{t_{e_i}}{T}} e^{-j \frac{2\pi}{M} ik}. \quad (2.23)$$

Interestingly, the alias terms associated to $S_k(\omega)$ are centered at the same frequencies that those arising from gain-mismatch. But for clock-skew, the value $S_k(\omega)$ depends on the input signal frequencies, while for gain-mismatch, G_k is independent from them. Intuitively, for a sinusoidal input signal, the higher ω_{in} , the higher the energy error for a given t_{e_i} . It is illustrated in fig. 2.12, where

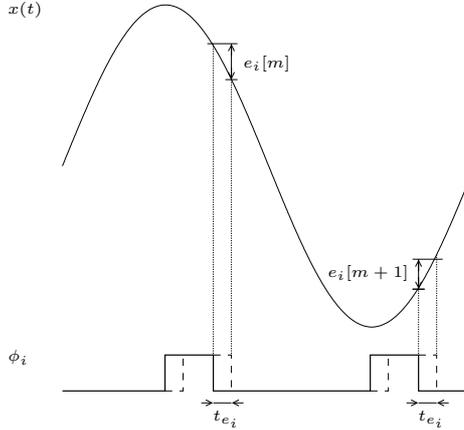


Figure 2.12: Plot of sampling errors in sampled data arising from clock-skew in a time-interleaved channel.

$e_i[m]$ are the sampling errors in the i -th channel arising from clock-skew.

Similarly to G_k , if there are no errors, i.e., $t_{e_i} = 0 \forall i$, we have

$$S_k(\omega) = \begin{cases} 1 & \text{for } k = Ml, l \in \mathbb{Z} \\ 0 & \text{otherwise,} \end{cases} \quad (2.24)$$

SNDR Loss Due to Clock-Skew

For a sinusoidal input signal, assuming t_{e_i} to be Gaussian random variables with zero mean and variance $\sigma_{t_e}^2$, the SNDR for the mean error power can be approximated as [29] :

$$\text{SNDR} \approx 20 \log \left(\frac{1}{2\pi\sigma_{t_e}(\omega_{in}/T)} \right) - 10 \log \left(1 - \frac{1}{M} \right). \quad (2.25)$$

Fig. 2.13 shows the plot of this theoretical SNDR limit versus σ_{t_e} for two si-

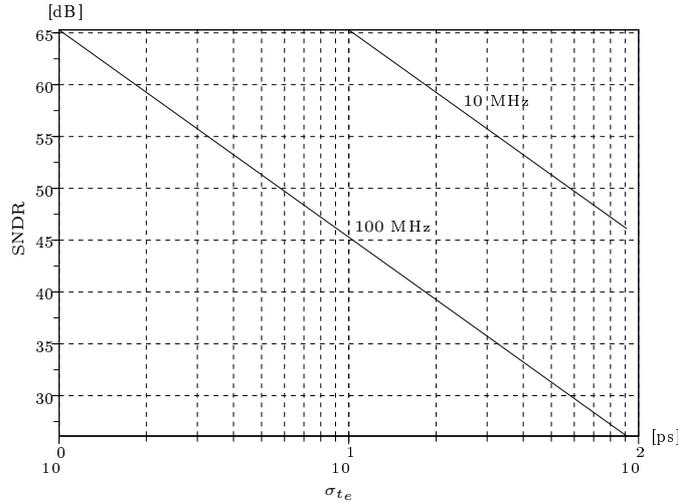


Figure 2.13: Plot of the theoretical SNDR limit versus σ_{t_e} in a $M = 4$ channels time-interleaved ADC.

nusoidal input signals at 10 MHz and 100 MHz, in a $M = 4$ channels time-interleaved ADC.

In a $M = 2$ channels time-interleaved ADC, spectral analysis is a simple way of measuring the actual clock-skew. In order to do that, we must know the associated t_{e_i} to the measured SFDR in absence of gain mismatch. Arranging the equations shown in [37], the theoretical relations between the SFDR and t_{e_1} for a given input signal frequency can be easily derived. The results of these derivations are here :

$$\text{SFDR} = 20 \log \left[\cot \left(|t_{e_1}| \frac{\omega_{in}}{2T} \right) \right], \quad (2.26a)$$

$$|t_{e_1}| = \frac{\arctan \left(\frac{1}{\sqrt{\text{SFDR}_{\text{lin}}}} \right)}{\frac{\omega_{in}}{2T}}, \quad (2.26b)$$

where $\text{SFDR}_{\text{lin}} = 10^{\frac{\text{SFDR}}{10}}$, $|\cdot|$ denotes the absolute value operator and it is assumed, without loss of generality, that the channel 0 is the reference of time, i.e., $t_{e_0} = 0$ and, then, t_{e_1} is the only clock-skew. Fig. 2.14 shows this theoretical SFDR versus $t_{e_1} \cdot (\omega_{in}/T)$. The horizontal axis shows up the relative values of t_{e_1} and ω_{in}/T .

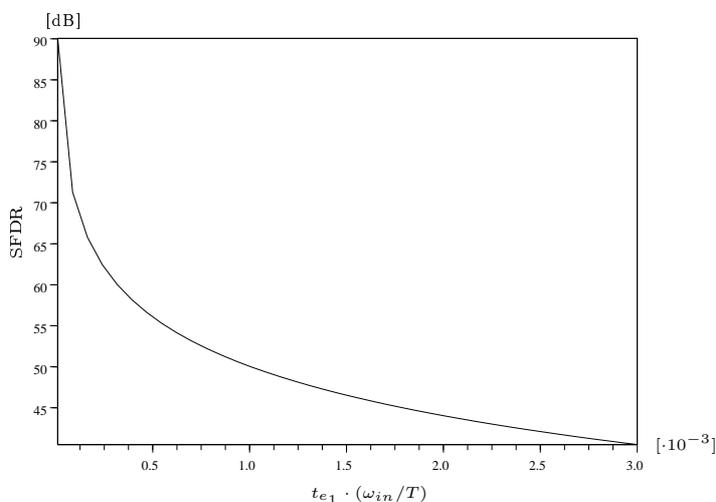


Figure 2.14: Plot of the theoretical SFDR versus $t_{e1} \cdot (\omega_{in}/T)$ in a $M = 2$ channels time-interleaved ADC.

2.4 Conclusion

This chapter presents the concept of parallel analog-to-digital conversion as a manner of obtaining high resolution and high sampling rate converters. Time-interleaved ADCs are identified as the simplest architecture in the parallel ADCs family. Then, the specific errors of time-interleaved ADCs and their impacts on the digital output signal are analyzed from an analytical point of view. These errors are originated in mismatches between the channels of the time-interleaved ADCs. They are mainly three : gain and offset mismatch, and clock-skew.

The rest of this work is devoted to clock-skew in the sampling instants. Clock-skew is a critical error in time-interleaved ADCs because we resort to this kind of architecture to convert very high frequency signals. But precisely the greater the input signal frequency, the greater the effects of clock-skew in the digital output signal.

Let us use an example to give the order of magnitude of clock-skew effects. From fig. 2.13, note that for an input signal at 10 MHz, σ_{t_e} should be less than 10 ps if 65 dB of SNDR is required. At 100 MHz, σ_{t_e} should be less than 1 ps. As shown in Subsection 3.3.1, it is very difficult to achieve with a CMOS technology.

Chapter 3

Techniques to Minimize Clock-Skew Effects

3.1 Two-ranks Sample-and-Hold

The two-ranks sample-and-hold (S/H) front-end is one of the first solutions proposed to avoid clock-skew in time-interleaved ADCs [54]. Fig. 3.1 shows a

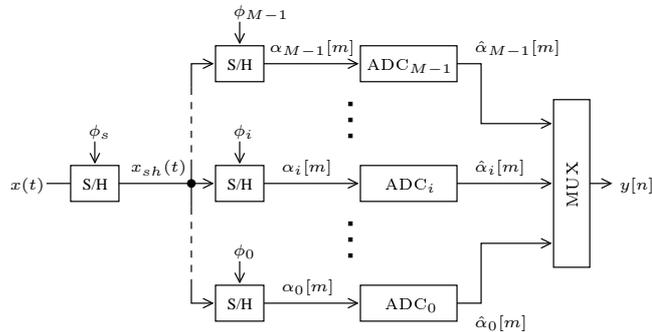


Figure 3.1: Diagram of a two-ranks S/H front-end for a time-interleaved ADC.

diagram of this architecture. A single S/H samples the analog input $x(t)$ at f_s rate. Its output, denoted $x_{sh}(t)$, is again sampled by one of the time-interleaved S/H at the slower rate f_s/M . Clock-skews in ϕ_i clock signals can be neglected because the $x_{sh}(t)$ signal is sampled at the end of the hold phase of the fast S/H. In this moment, $x_{sh}(t)$ is nearly constant, greatly reducing the clock-skew effects on the resampled signal.

The advantage of using only a single S/H is that only one sampling clock (denoted ϕ_s) determines all the sampling instants, fully avoiding any clock-skew during the input signal sampling.

The drawback of this solution is that it is not a fully parallel circuit, as defined in Section 2.1. It means that the fast S/H limits the overall conversion rate of the ADC below a certain technological limit. Note that if an ADC is not to be operated beyond this technological limit, maybe the time-interleaved

architecture is not the more appropriate design choice because of its inherent complexity.

3.2 Channel Randomization

Clock-skew effects have a negative impact on both SNDR and SFDR. For telecommunication applications, the linearity of a receiver, measured in terms of SFDR, is an important parameter because the interference between channels at different frequencies could prevent a correct reception.

Channel randomization is a technique that improves the SFDR of a time-interleaved ADC [61]. This is true for any kind of channel mismatches, not only clock-skew. Fig. 3.2 shows a diagram of a modified time-interleaved ADC to

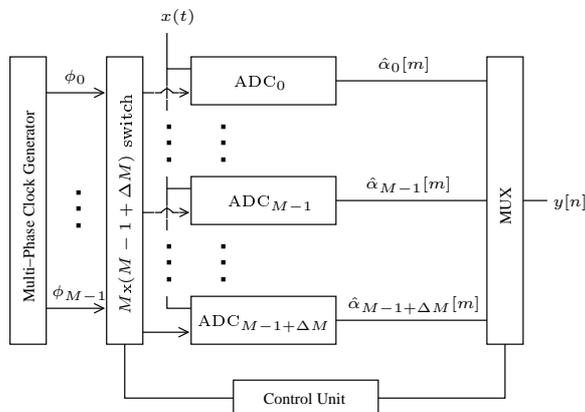


Figure 3.2: Diagram of a randomly interleaved ADC.

allow channel randomization, called randomly interleaved ADC. If a single ADC_i needs $M \cdot T$ s to digitalize a sample, then ΔM extra single ADC_i s, $M \leq i \leq M-1+\Delta M$, must be added for a fixed interleaved ADC to become a randomly interleaved ADC. Moreover, a $M \times (M-1+\Delta M)$ switch¹ is needed between M clock signals from the multi-phase clock generator and all the ADC_i s. This switch can be made by means of a network composed of basic 2×2 switches [32]. Every input can potentially be connected to any output. Finally, a control unit selects the instantaneous interconnections of the $M \times (M-1+\Delta M)$ switch and the multiplexer in a proper way.

For a sinusoidal input, the error spectrum at the output of a randomly interleaved ADC does not contain any spurious δ -spikes, which greatly improves the SFDR [18]. Instead, for a low ΔM , it is shown that the error has an *oscillation-like* spectrum, the peak value of which is reduced when ΔM is increased. In fact, the greater ΔM , the more white becomes the resulting error spectrum. On the other hand, the SNDR is the same for both a randomly interleaved ADC and a fixed interleaved ADC. Intuitively, it can be understandable because no

¹Or, at least, a $1 \times (M-1+\Delta M)$ switch, i.e., a demultiplexer, where only one clock signal, operating at the full sampling rate $1/T$, is present at the input of the demultiplexer. Note that in contrast with the two-rank S/H solution, where using only one clock signal removes any clock-skew, due to inequalities in the delays of the different paths through the demultiplexer, here using one clock signal does not remove clock-skew.

amount of error is removed by randomization. Randomization just reduces the correlation between the channels mismatches and the input signal.

The usefulness of channel randomization must be carefully weighed up. Time-interleaved ADC are generally used to achieve good resolution and high conversion rate at the same time. Channel randomization offers the possibility of increasing the SFDR without improving the lowered SNDR. If good resolution is not needed and the resulting SNDR is at levels comparable with other ADC architectures of less nominal resolution, probably a time-interleaved ADC is not again the most suitable choice because of its complexity.

3.3 Clock Distribution Techniques

Two clock distribution techniques have been proposed to cancel or minimize clock-skew in fully parallel circuits. The former technique is called global passive sampling. It was first conceived for double-sampled circuits [72] and subsequently developed for time-interleaved ADC [22]. It has been also called edge-driven switching [59].

The latter technique was directly conceived for time-interleaved ADCs and is called clock edge reassignment [73]. It has been also called edge-driven clocking [59].

3.3.1 Global Passive Sampling

The global passive sampling technique was for the first time proposed in [72]. This technique was developed to cancel the clock-skew previously found by the same authors in sample-and-hold circuits using double-sampling technique [70] [71].

Global Passive Sampling and Double-Sampling

Fig. 3.3 shows the unity-gain sampler, a basic switched-capacitor S/H circuit.

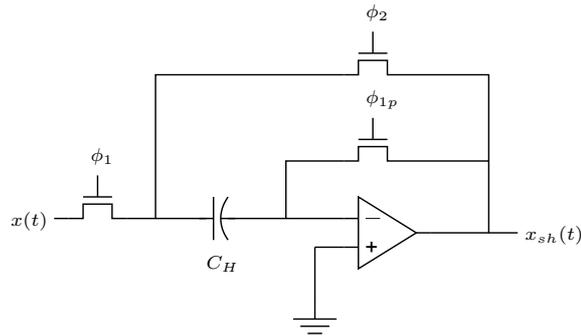


Figure 3.3: A simple switched-capacitor S/H : the unity-gain sampler.

There are two distinguishable phases during its operation : the sampling phase (with ϕ_1 in *high* logic level and ϕ_2 in *low* logic level) and the hold phase (with ϕ_1 in *low* logic level and ϕ_2 in *high* logic level). Traditionally, during the sampling phase the operational amplifier (opamp) is kept idle supplying a virtual ground for the sampling capacitor. It allows to cancel its input offset voltage [35]. But,

in some applications, a constant offset voltage is tolerable or, simply, it will be later removed by means of calibration. For these applications, double-sampling techniques propose to share one opamp between two different sampling channels to avoid the idle phase [6]. Fig. 3.4 shows a double-sampled S/H circuit. It

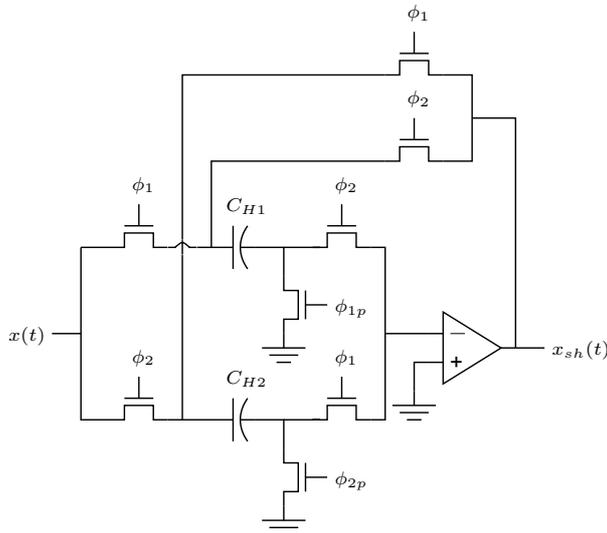


Figure 3.4: Double-sampled S/H circuit.

actually doubles the sampling rate for a given opamp. In our example, the falling edges of phases ϕ_{1p} and ϕ_{2p} determine the sampling instants for the two channels, respectively. They are slightly advanced to ϕ_1 and ϕ_2 respectively, being known consequently as pre-phase signals. This is the so-called bottom plate sampling technique, used to avoid charge injection distortion from the switches [24]. For a correct sampling synchronization, these two phases must have exact 180 degree phase shift.

Clock-skew arises when ϕ_{1p} and ϕ_{2p} do not have exact 180 degree phase shift. Measures from real circuits in a $0.25 \mu\text{m}$ CMOS technology show that clock-skew can be more than 50 ps [74]. A clock-skew of 25 ps has been measured in other work for a $1\text{-}\mu\text{m}$ CMOS technology [7]. In fact, clock-skew depends on the exact multi-phase clock generator structure. Subsection 3.3.2 shows that clock-skew can be minimized if the multi-phase clock generation is carefully conceived.

From a clock-skew point of view, the digital output exhibits the same distortion than that found in two-channels time-interleaved ADCs. From a gain-mismatch point of view, since the same opamp is used for the two channels, there is no distortion. From an offset mismatch point of view, there are two components : the main one is the opamp offset discussed above. It is shared by the two channels, so no offset-mismatch arises from it, just offset. The second one is the charge injection from the two different sampling switches. If it is kept small and/or signal independent by virtue of the bottom plate sampling, its effects could be neglected. Let us now describe the case of a time-interleaved double-sampled front-end S/H, made from $M/2$ circuits as that shown in fig. 3.4. A M -channels type clock-skew distortion and a $M/2$ -channels type gain and offset mismatch distortion will be observed at the discrete-time output. The

M -channels type clock-skew arises from the M different switches and sampling clocks. The $M/2$ -channels type gain and offset mismatches arise from the $M/2$ shared opamps.

Double-sampling can be used to design power-efficient M -channels time-interleaved systems, as e.g. the four-channels pipeline ADC shown in [60]. There, double-sampling is used to design the MDACs. Two MDACs of two different pipeline channels operating with a 180 degrees phase shift are placed in parallel at pipeline stages of equivalent resolution. These two MDACs share one double-sampling opamp.

Following a two-ranks S/H strategy, the sampling operation is done by only one double-sampled S/H, as that shown in fig. 3.4. A modification is carried out to avoid the two-channels type clock-skew. It is discussed just below.

The global passive sampling technique is presented in [72] and is extensively discussed in [69]. Fig. 3.5 shows the modification done on the diagram of fig. 3.4.

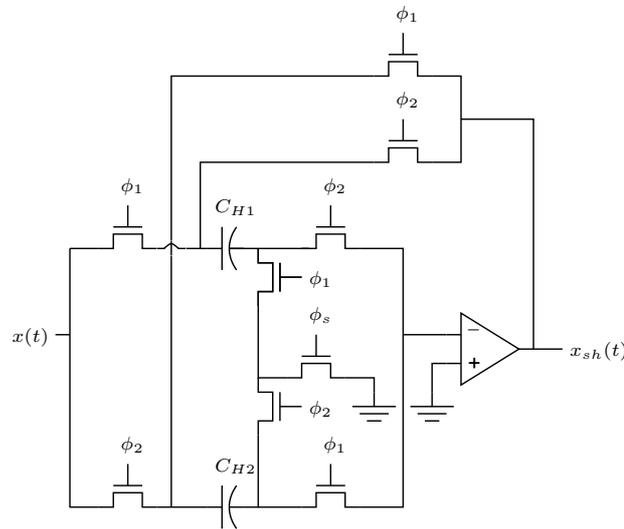


Figure 3.5: Global passive sampling in a double-sampled S/H circuit.

A single sampling clock signal ϕ_s and a sampling switch are shared by two channels. ϕ_s operates at the full sampling rate $1/T$, while the non-overlapping ϕ_1 and ϕ_2 phases operate at half the full sampling rate. ϕ_s determines the sampling instants, turning off the sampling switch slightly before than the level change on the ϕ_1 or ϕ_2 clocks, as shown in fig. 3.6. Note that consequently there is no need of individual pre-phase signals associated to ϕ_1 or ϕ_2 clocks. Finally, since there is only one sampling clock, clock-skew is completely removed in a first order approximation. It is discussed later in this Section.

Global Passive Sampling and Time-interleaved

The global passive sampling technique is presented in a general time-interleaved context in [22] and later in [59]. It is illustrated in fig. 3.7, where the duty cycle of the non-overlapping ϕ_i clock signals is less than $1/M$. On the other hand, the hold phase for the opamps could be up to near $M - 1$ times longer, depending on

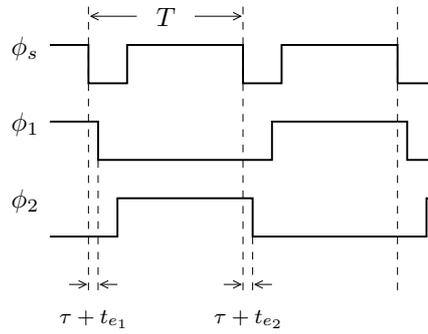


Figure 3.6: Timing of the global passive sampling technique applied to the double-sampled S/H circuit.

what type of ADCs are used in the channels, relaxing opamp power dissipation, speed and resolution tradeoff. The ϕ_s clock determines the sampling instant in a similar way to that shown in fig. 3.6, a particular case where $M = 2$.

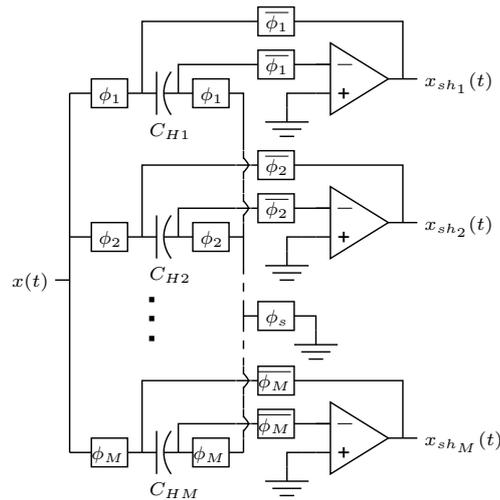


Figure 3.7: Global passive sampling for a time-interleaved S/H circuit.

Global Passive Sampling Drawbacks

An accurate analysis of the parasitic capacitances associated with the added sampling switch is presented in [22], showing some physical limitations of this technique. Fig. 3.8 illustrates the problem. These parasitic capacitances play a role in the output signal distortion when combined with a timing as that shown in fig 3.6. In a well designed clock distribution tree, τ defines the nominal time gap between the *high-to-low* transitions of ϕ_s and the *high-to-low* transitions of ϕ_i for the i -th channel. t_{e_i} defines the dispersion associated with this time gap. In fact, when the sampling switch ϕ_s is turned off, even if the charge in the shorted nodes X and Y is preserved, the voltage changes along with the input

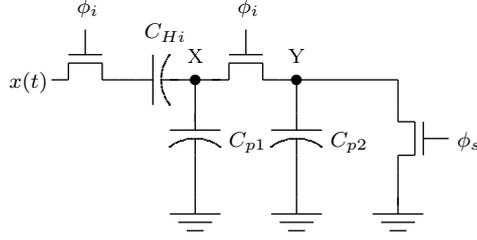


Figure 3.8: Parasitic capacitors in the i -th channel of a time-interleaved global passive sampling circuit.

signal during the actual time gap $\tau + t_{e_i}$. It causes an input depending charge distribution between C_i , C_{p1} and C_{p2} . When ϕ_i is turned off, there is an input depending charge lost on node X, the charge contained in C_{p2} in that badly controlled instant.

From [22], the i -th S/H output for an ideal opamp at the end of the hold phase² is :

$$x_{sh_i}(t_{ideal\ s_i}[m] + t_h) = (1 - a) \cdot x(t_{ideal\ s_i}[m]) + a \cdot x(t_{ideal\ s_i}[m] + \tau + t_{e_i}), \quad (3.1)$$

where

$$a = \frac{C_{p2}}{C_{p1} + C_{p2} + C_i}. \quad (3.2)$$

The mean time gap τ simply introduces a slight linear filtering on the input signal. On the other hand, when multiplexing all the opamp outputs, the random t_{e_i} components introduce a M -channels type clock-skew distortion. Nevertheless, it will be reduced by a factor $1/a$ compared to a time-interleaved ADC not using the global passive sampling technique. Assuming t_{e_i} , $0 \leq i \leq M - 1$ as independent random variables with normal distributions and equal variances σ_t^2 , the SNDR is approximately :

$$\text{SNDR} = 20 \log \left(\frac{1}{\sigma_t 2\pi\omega_{in}/T} \right) - 10 \log \left(1 - \frac{1}{M} \right) - 20 \log(a). \quad (3.3)$$

There is another physical limitation : the impact of the increased resistance due to the additional sampling switch. Unfortunately, there is a lack of a detailed analysis of it. Maybe it is because of the variety of possible switch configurations. However, simulations show for simple n -channel metal-oxide-semiconductor (NMOS) switches that harmonic distortion grows considerably compared to an ordinary two switches sampling [22]. It could limit the overall attainable resolution.

3.3.2 Clock Edge Reassignment

Description

As in the global passive sampling technique, clock edge reassignment uses only one sampling clock operated at full sampling rate. On the other hand, for one

²The time instant at the end of the hold phase for the sample taken at $t_{ideal\ s_i}[m]$ is $t_{ideal\ s_i}[m] + t_h$

channel, the input path is formed only by two switches, instead of three, avoiding the drawbacks of the previous solution.

Fig. 3.9 shows a general M -channels clock distribution tree based on that

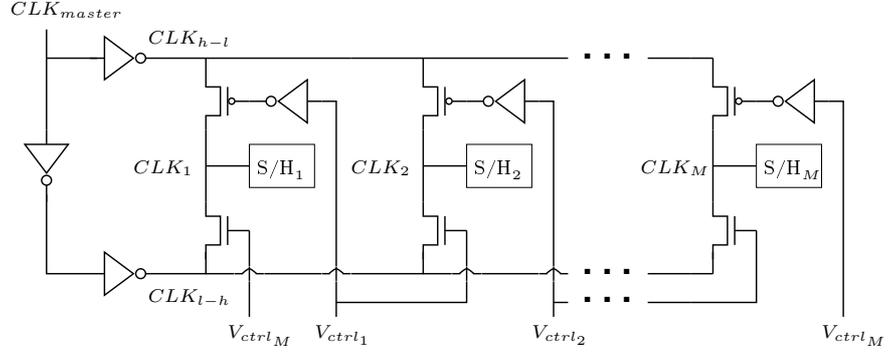


Figure 3.9: M -channels clock edge reassignment circuit.

used in [73] for a two-channels time-interleaved ADC. The timing diagram in fig. 3.10 is useful to understand how it works. Assume that the *low-to-high* tran-

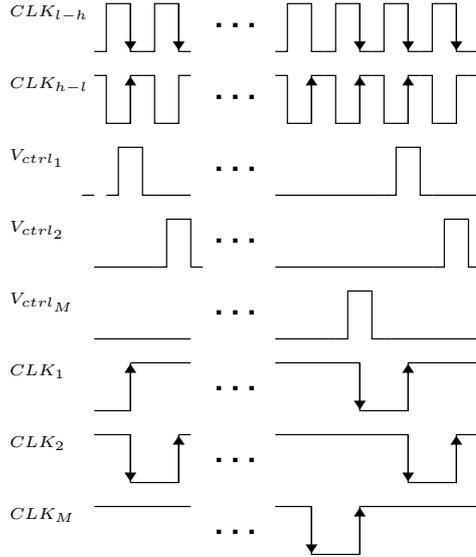


Figure 3.10: Timing for a M -channels clock edge reassignment circuit.

sitions of the CLK_{h-l} signal determine the sampling instants. The p-channel metal-oxide-semiconductor (PMOS) transistors at the top of the fig. 3.9 drive these transitions to the appropriate S/H depending on the state of the specially conceived V_{ctrl_i} signals. On the other hand, the NMOS transistors at the bottom drive the *high-to-low* transitions to the S/Hs. The resulting individual sampling clock signals for each S/H are CLK_i .

Another example of clock edge reassignment circuit can be found in [41]. The starting point is a conventional non-overlapped two-phases clock generator. It generates the clock phases needed for the circuit shown in fig. 3.4. Then, this

clock generator is modified to alternatively drive the *high-to-low* transitions of the same sampling clock to the ϕ_{1p} and ϕ_{2p} clock signals.

Clock Edge Reassignment Drawbacks

Clock dividers are traditional multi-phase clock generation circuits [3]. Compared to these circuits, clock edge reassignment minimizes the clock-skew between channels. But a residual clock-skew unavoidably arises when the path followed by the sampling clock signal differs from one channel to another. Even in carefully designed layout, where all paths are minimized and designed equal, fabrication dispersion can introduce an appreciable clock-skew.

In [73], for a 0.6- μm CMOS technology, it is said that the clock-skew is maintained below 10 ps. It suffices for an 8-bit ADC sampling a 75 MHz signal. For a greater input signal frequency or resolution, it will not be enough. In [41], simulations show a 2.3 ps clock-skew. However it is not clear how the dispersion notion has been introduced in the simulations. In the author's opinion, only measures on real circuits can provide trustworthy results.

3.4 Clock-Skew Calibration Techniques

The calibration techniques can be classified into three categories :

- All-digital calibration techniques.
They benefit from easy of portability through the technology evolution and they are not affected by fabrication dispersion problems. Unfortunately, some digital reconstruction methods can potentially be very complex. It will be discussed later in this Section.
- All-analog calibration techniques.
Depending on the calibration system, analog blocks could be potentially simpler than digital blocs. Their main drawback is that the clock-skew is detected out of the digital domain, so it could be not correctly sensed and, consequently, not completely removed. Moreover, analog calibration systems are sensible to fabrication dispersion.
- Mixed-signal calibration techniques.
These techniques could potentially benefit from portability, simplicity and robustness to fabrication dispersion from the previous two categories.

From another point of view, almost all calibration techniques can be split into two clearly different subsystems : a correction subsystem and a measurement subsystem.

3.4.1 All-Digital Calibration Techniques

Jamal *et al.*'s Calibration [27][28]

Overview This calibration technique applies to a 2-channels time-interleaved ADC. It is based on a digital correction filter and on a clock-skew detector as shown in fig. 3.11. The filter coefficients depend on the precise value of the clock-skew. To correctly set the coefficients, the filter and the clock-skew detector are

embedded in a negative feedback loop. When the measured clock-skew finally converge to the actual clock-skew, the correction filter is supposed to properly eliminate the clock-skew in the digital domain.

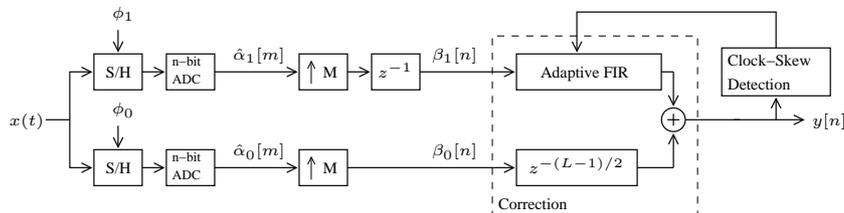


Figure 3.11: General diagram of the Jamal *et al.*'s calibration technique.

Correction Technique This technique applies to a 2-channels time-interleaved ADC and uses one digital filter. In fig. 3.11, the bottom channel, channel 0, is considered as the reference one. The signal in channel 1 is sampled with an unknown clock-skew t_e . The effects of clock-skew on the $\beta_1[n]$ signal can be seen as a phase shift in the frequency domain. This phase-shift can be corrected with an all-pass filter that only modifies the phase. Because of the impulse response coefficients depend on t_e , an adaptive filter is necessary. This adaptive filter follows the evolution of the measured clock-skew until the clock-skew detection block converges. For a well-designed feedback system, the correction filter must be able of removing the clock-skew in the steady state for a given ADC resolution. The Nyquist-Shannon Sampling Theorem is the only condition that the inputs signals must verify for perfect reconstruction to be possible [19]. The ideal impulse response of the correction filter is :

$$h[n] = -\frac{\sin\left(\pi\frac{t_e}{T}\right)}{\pi\left(n - \frac{t_e}{T}\right)}. \quad (3.4)$$

A detailed discussion of (3.4) can be found in Appendix B.1. In practice, a causal finite impulse response (FIR) filter of length L , L odd, is used. Therefore, the $\beta_0[n]$ signal must go through a fixed delay of $(L-1)/2$ samples. The computational cost is L multiplications per sample. Real data results show that a 21-coefficients FIR filter with 10-b coefficients suffices to correct the clock-skew for a 10-b accuracy and input signal frequencies as high as 90% of $f_s/2$, where $f_s=120$ Msamples/s.

We have developed our own technique for the M -channels general case. It has been published in [4] and it is explained in Appendix A. In the context of the existing literature, this work can be classified into the set of techniques that uses multirate filter banks for reconstruction of band-limited signals from their periodic nonuniform samples.

Reconstruction of sampled signals has been a main topic in signal processing literature for many years. An early work that uses multirate filter banks for reconstruction can be found in [65] [66]. The proposed system uses a constant matrix multiplier and M FIR filters. Recently, in a time-interleaved context, a similar work has been published in [55], where only M FIR filters take part in the reconstruction structure.

Measurement Technique This technique applies to a two-channels time-interleaved ADC. It performs a digital clock-skew detection that is followed by an accumulator. The diagram of the clock-skew detector is shown in fig. 3.12. The clock-skew is sensed from the digital signal $y[n]$, that suffers from clock-skew

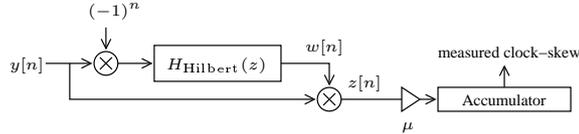


Figure 3.12: Diagram of the clock-skew detector.

when the correction filter is not properly configured. Let t_{res} be the residual clock-skew in $y[n]$ not yet corrected by the correction filter. As shown in Appendix B.2.1, the direct current (DC) component of $z[n]$ is proportional to t_e , or t_{res} in closed-loop configuration. Briefly, the discrete-time Hilbert filter and the multiplication of $w[n]$ and $y[n]$ allow to perform a frequency shifting of the clock-skew related spurious signals. These spurious signals are shifted on the DC component of $z[n]$. If present, the accumulator senses it and its output evolves while it is different from zero. This accumulated value, the measured clock-skew, is used to set the correction filter coefficients. When the measured clock-skew coincides with the actual clock-skew, t_{res} and the DC component of $z[n]$ becomes zero. In this situation, called steady state, the measured clock-skew is stable, i.e., it does not change or changes only by very small amounts around the actual clock-skew.

Finally, there is one condition that the input signal $x(t)$ must meet. As explained in Appendix B.2.2, $x(t)$ for the clock-skew detector to work properly must verify :

$$\left| X\left(\frac{\omega}{T}\right) X\left(\frac{\pi}{T} - \frac{\omega}{T}\right) \right| = 0. \quad (3.5)$$

Conclusion Depending on the application, the adaptive correction filters could require too much area and power. According to [27], just one calibration filter is estimated to require 5 mm^2 and 190 mW in a $0.35\text{-}\mu\text{m}$ CMOS technology at 120 Msamples/s for a 10-b ADC. Of course, this technique could be promising when digital technologies evolve.

With regard to the measurement technique, the negative feedback loop is proved to be an effective way to measure the clock-skew. Moreover, as explained in Appendix B.2.3, this technique can tolerate gain and offset mismatch between the two ADCs. Therefore, from a fabrication dispersion point of view, it is a robust technique. Unfortunately, it can only handle a two-channels systems and restrictions exist on the usable input signals to calibrate. It precludes the use of the measurement technique in background calibration for general bandlimited signals.

Jin and Lee's Calibration [33]

Overview It is a background calibration technique based on the injection of a known test signal to carry out clock-skew measurements. These measurements are used to correctly set the coefficients of a reconstruction filter. The filter is

based on an interpolation method. There is not feedback of any kind, unlike the Jamal *et al.* calibration.

Only theoretical analysis and simulation results show the operation of this technique.

Correction Technique This technique is based on the Neville's iterative algorithm [62]. It is a linear interpolation method that can be implemented as a FIR filter. A different filter is needed for each channel, except for the reference one, considered as clock-skew free. The coefficient formulation is the same for each filter, but their actual values are related to the clock-skew associated with the channels. Therefore they must be adaptive filters. In general, they all can be grouped in only one time varying FIR filter to provide a completely clock-skew free output. It is illustrated in fig. 3.13, where the coefficients of the

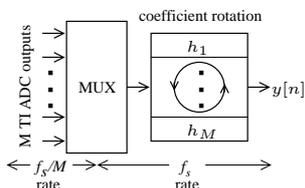


Figure 3.13: Multiplexer and M -channels interpolation filter.

interpolation filter have to be rotated with a period of M samples accordingly with the number of channels. Of course, the coefficient rotation rate is f_s . The filter coefficients must to be updated to follow the measured clock-skew evolution. The coefficient update rate can be low because clock-skew is a constant or nearly constant feature.

The h_i filters from the figure are L -coefficients long for a L -points interpolation. Then, the computational cost is L multiplications per sample, independently of the number of channels. Simulation results show, for a sinusoidal input, a good SFDR (120 dB) for a 32-points interpolation with negligible oversampling. A 20 dB loss is expected for a 18 bits of accuracy in the computation. No results are provided for more complex signals.

Measurement Technique It is not a fully digital technique, but rather a mixed signal one because a known analog test signal must be added to the input signal before the S/H stage. The clock-skew measure, however, is provided by the ADCs in the digital domain. Fig. 3.14 shows a diagram of the measurement circuit, with the added test signal $r(t)$. Fig. 3.15 shows the relation between the clock-skew error t_{e_i} and the digital estimated delays $ED_i[m]$. To better understand the principle, assume for the moment that the input signal $x(t)$ is equal to zero. Let $r(t)$ be a ramp signal of period T . For equally spaced sampling instants, all the $ED_i[m]$ values are the same (zero or a near zero value). In practice, the later the sample is taken, the higher $ED_i[m]$ is. By comparing all the $ED_i[m]$ signals, a quantitative information about the relative clock-skew between channels can be extracted.

For this measurement technique to work properly, the DC component of every sequence of samples $x(t_{s_i}[m])$ must be zero. If this is the case, the digital low pass filter allows to detect the clock-skew related component, the cause of the

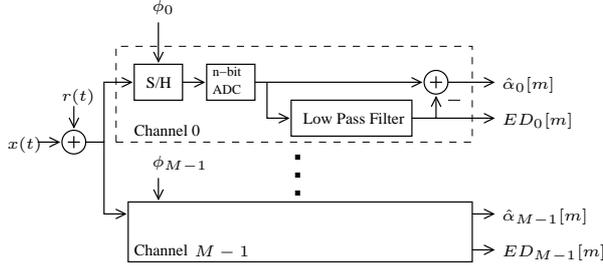


Figure 3.14: Diagram of the Jin and Lee's clock-skew measurement technique.

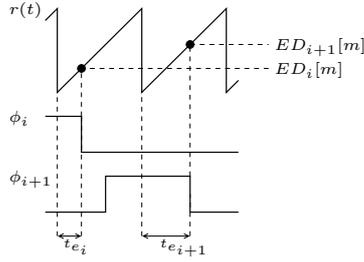


Figure 3.15: Test signal and timing of the Jin and Lee's clock-skew measurement technique.

only DC component in each channel. From this principle, we can derive this input signal restriction :

$$\left| X \left(\frac{2\pi}{MT} k \right) \right| = 0, \quad \forall k \in \mathbb{Z}. \quad (3.6)$$

It is done in Appendix C. This restriction has been neglected by Jin and Lee. If there is sampling jitter, it will be filtered by a sufficiently selective low pass filter. If it is not verified, the input signal contributes a clock-skew independent DC component preventing the actual clock-skew from being measured. The result of the i -th channel measure, $ED_i[m]$, is subtracted from the digital signal, so $\hat{\alpha}_i[m]$ contains only information about the input signal. Next, $ED_i[m]$ and $\hat{\alpha}_i[m]$ are given to the interpolation filter.

The use of an injected test signal could reduce the allowable dynamic range for the input signal. For low clock-skew cases, however, it can be shown that the reduction is negligible.

Conclusion The adaptive correction filter could require a great amount of digital circuitry the area and power of which are not negligible. Unfortunately, there is a lack of more details in this work. For sinusoidal input signals, a slightly oversampling is needed. It is an input signal restriction.

With regard to the measurement technique, although a S/H and adder circuit is proposed, no real implementation has been done. From a hardware point of view, the precise generation of the test signal is a drawback. Moreover, this measurement technique is sensible to any nonideality in the ADCs, as well as

gain mismatch and offset mismatch between channels. For all these reasons, it could be said that it is not a robust measurement technique from a fabrication dispersion point of view.

Finally, there is one severe input signal restriction, shown in (3.6).

Other Similar Works

Correction Techniques For practical reasons, the filter bank structures are preferred in all-digital calibration systems. Nevertheless, it is worth mentioning other works as [31] where, by means of a matrix multiplication and with the knowledge of the clock-skews, the spectral content of a nonuniformly sampled signal is recovered. In [34] a filter bank structure is used, with simpler filters that are not adaptive. Unfortunately, they can only be used to reconstruct a class of heavily oversampled signals.

Measurement Techniques An algorithm for estimating the clock-skew is presented in [30]. An isolated test signal is injected in the time-interleaved ADC and, by means of mainly a Discrete Fourier Transform (DFT), the clock-skews are extracted in the digital domain. Another algorithm uses a wavelet analysis [45]. It obtains a more accurate estimation of the clock-skews from a lower number of samples. But both are by far computationally more complex than the techniques previously presented here.

3.4.2 All-Analog Calibration Technique

Wu and Black's Calibration [74]

Overview This calibration technique acts on the multi-phase clock generation subsystem, independently of the time-interleaved ADC. The chosen multi-phase clock generator is a voltage-controlled ring oscillator, composed of four differential delay cells, embedded in a phase-locked loop (PLL), as shown in fig. 3.16. This kind of ring oscillator naturally provides eight clock signals ϕ_j , $0 \leq j \leq 7$, all at the frequency imposed by the PLL and an external reference. The phases of these clock signals are nominally spaced to drive eight channels of a time-interleaved ADC. However, due to dispersions during the fabrication process and/or systematic mismatches, seven clock-skews between the phases must be adjusted, being ϕ_0 the phase of reference. To correct them, there are seven adjustable delay cells, individually trimmed by means of the V_{ctrl_j} signals. It is done in seven negative feedback loops, composed of the adjustable delay cells and delay comparators. These phase loops are independent of the PLL used to adjust the frequency.

In a general case, a ring oscillator composed of $M/2$ differential delay cells would be used as clock generator for a M -channels time-interleaved ADC. $M - 1$ adjustable delay cells would be used to calibrate $M - 1$ clock signals.

Correction Technique This work proposes a sampling instant correction carried out directly in the clock generation subsystem. The sampling instant calibration for the j -th time-interleaved channel is done by the j -th adjustable delay cell and V_{ctrl_j} . Fig. 3.17 shows the diagram of an adjustable delay cell. In fact, this circuit is the same used in the voltage-controlled ring oscillator and

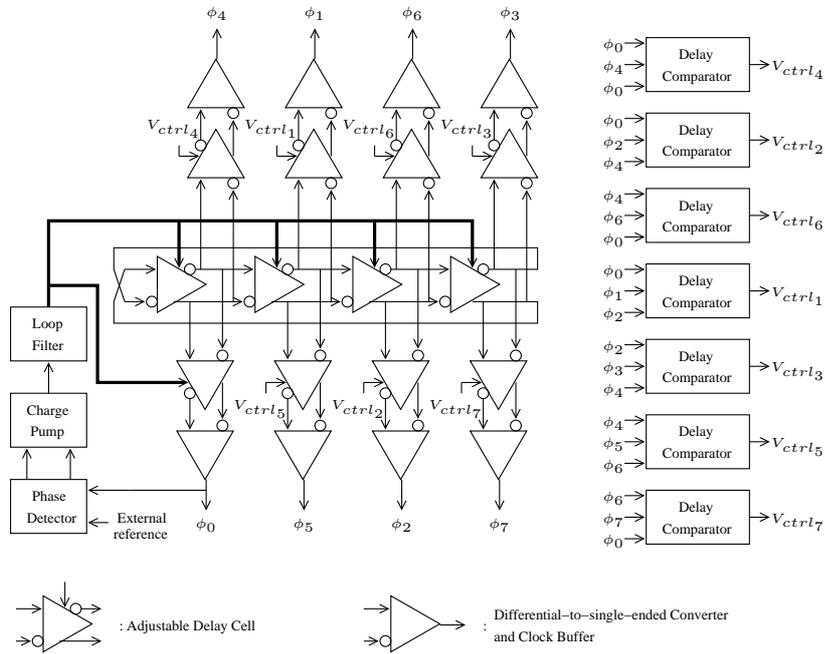


Figure 3.16: General diagram of the Wu's *et al.* calibration technique.

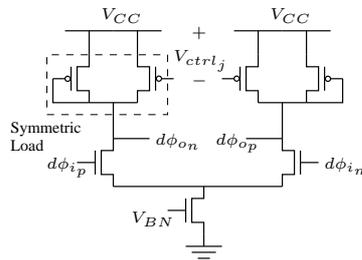


Figure 3.17: Adjustable delay cell.

will be further discussed in Subsection 5.4.2. Now, a brief description of its operation in this context follows.

V_{ctrl_j} is an analog signal that changes the equivalent resistance of the PMOS transistors pairs, called symmetric loads in fig. 3.17. The symmetric loads control the charge transfer speed during the output transitions between opposite states. They actually modify the total time that it takes to a signal to go through the delay cell. The output signals $d\phi_{op}$, $d\phi_{on}$ have a limited excursion between V_{CC} and $V_{CC} - V_{ctrl_j}$. For this reason, the output signals must drive a high slew-rate differential-to-single-ended rail-to-rail clock buffer, not shown in fig. 3.17. It provides a proper sampling clock signal.

Measurement Technique The measure is done based on the clock signals themselves. Two premises allow it : first, there is a clock signal considered as the reference one, ϕ_0 . Second, the phases of the clock signals must be equally

spaced in time because they have to drive an uniform sampling time-interleaved ADC.

Let the sampling instants be determined by the *low-to-high* transitions of the clock signals. A measure of the phase difference between ϕ_i and ϕ_j is obtained by measuring the time passed between two consecutive *low-to-high* transitions of these clock signals. It is denoted as $\Delta t_{i,j}$ for ϕ_i preceding ϕ_j . $\Delta t_{j,i}$ denotes the complementary time, i.e., ϕ_j preceding ϕ_i . Fig. 3.18 illustrates it. For the

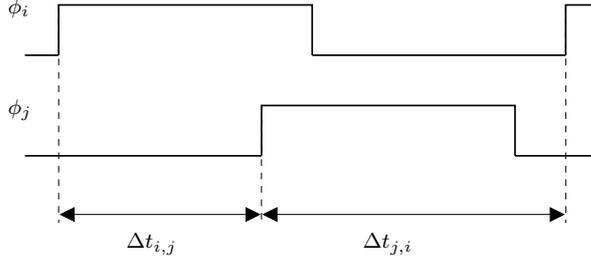


Figure 3.18: Timing of two clock signals and $\Delta t_{i,j}$, $\Delta t_{j,i}$ definition.

eight phases case, the first step in the calibration process is to establish ϕ_4 from ϕ_0 , the reference clock signal. Ideally, ϕ_4 and ϕ_0 are out of phase by 180 degrees. If it is the case, the measured $\Delta t_{0,4}$ and $\Delta t_{4,0}$ must be equal. If not, the fourth adjustable delay cell is trimmed by means of V_{ctrl_4} until $\Delta t_{0,4} = \Delta t_{4,0}$ is verified. When ϕ_4 is correctly established, ϕ_2 can be calibrated by equaling $\Delta t_{0,2}$ and $\Delta t_{2,4}$ and ϕ_6 by equaling $\Delta t_{4,6}$ and $\Delta t_{6,0}$. A similar process is done for the remaining clock signals. All these calibrations can be carried out at the same time. It can be generalizable to any M clock signals case.

Fig. 3.19 shows a delay sensing circuit. There are two input signals, ϕ_i and

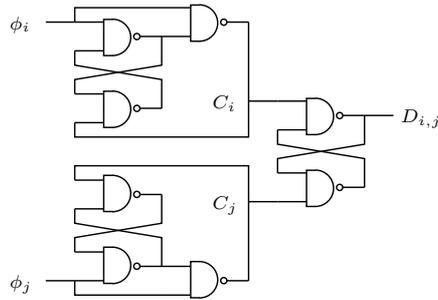


Figure 3.19: Delay sensing circuit.

ϕ_j , and one output signal, $D_{i,j}$. It can be shown that the duty cycle of $D_{i,j}$ is almost proportional to $\Delta t_{i,j}$, and $D_{i,j}$ is almost the complementary signal of $D_{j,i}$. Signals with these characteristics are appropriated to be injected as inputs in a charge pump circuit as that shown in the middle of fig. 3.20. The charge pump together with two delay sensing circuits form a delay comparator. There are $M - 1$ of them. The j -th delay comparator carries out the calibration of ϕ_j . Its inputs are ϕ_i , ϕ_j , ϕ_k . Its output is V_{ctrl_j} and depends on the duty cycles of the internally generated $D_{i,j}$ and $D_{i,k}$. Ideally, a negative feedback loop fixes

Digitally Controlled Current Starved Delay Element

A digitally controlled current starved delay element is a more evolved solution. It has been first proposed in the all-digital PLL context [13]. An example of this type of delay element is shown in fig. 3.21. The bits of a DCW activate

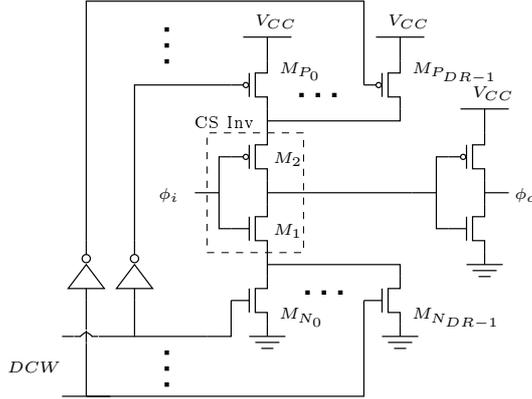


Figure 3.21: Diagram of a digitally controlled current starved delay cell.

or deactivate the transistors M_{N_l} and M_{P_l} , $0 \leq l \leq DR - 1$. They control the charging and discharging currents of the output capacitance of the inverter CS Inv. The greater the current, the shorter the delay. A variable resistor NMOS or PMOS stack can be used instead of M_{N_l} or M_{P_l} [57].

Unfortunately, there is not a straightforward relation between the aspect ratio of the active transistors and the added delay. In fact, the M_{N_l} and M_{P_l} transistors add a parasitic capacitance at the source of M_1 and M_2 respectively. This capacitance depends on which transistors are active [42]. It precludes from using equally sized transistors for the digital-to-time interface. However, because of fabrication dispersion issues as those explained in Subsection 4.3.3, equally designing these transistors is mandatory if a low dispersion in the values of t_{step} is needed.

A simple solution to overcome the drawbacks of the previous current starved delay element is the use of a current mirror [42]. It is illustrated in fig. 3.22. Note that the current-to-voltage conversion performed by the transistor M_{CM} follows a quadratic law.

Shunt Capacitor Delay Element

The use of shunt capacitors is another known technique [36]. It is illustrated in fig. 3.23. The voltage V_{CS} at the gate of the shunt transistor M_1 controls the charge and discharge current to the MOS capacitor M_2 from the inverter.

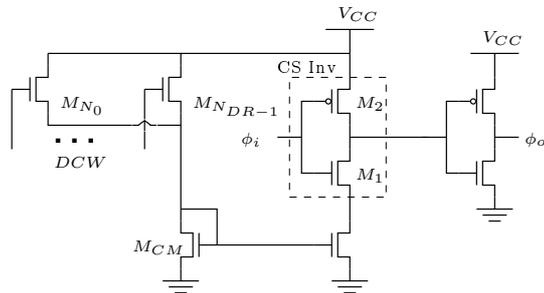


Figure 3.22: Diagram of a digitally controlled current starved delay cell with current mirror.

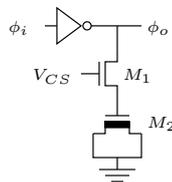


Figure 3.23: Diagram of a shunt capacitor delay cell.

3.5 Conclusion

3.5.1 General Conclusion

Section 3.1 and Section 3.3 show two families of solutions to the clock-skew problem. They are generally simple and greatly reduce clock-skews, but they all have any kind of limitation. They could be well-suited for applications where simplicity is a priority and no extreme performances are required. However, to exploit all the possibilities of time-interleaved architectures, the two-rank S/H solution should be avoided and a calibration system as those described in Section 3.4 should be used instead. They allow to use a fully time-interleaved circuit, at the price of a greater complexity. An extra advantage of using calibration is a simpler layout design : if calibration is being used, some systematic clock-skews (introduced, e.g., by making clock signal paths of different length for layout convenience) could be tolerated and later compensated by calibration.

From a combined solution point of view, calibration is often not incompatible with some clock distribution techniques, specially clock edge reassignment. Moreover, in a hypothetical clock-skew calibrated circuit, channel randomization could spread the residual non-linear distortion all over the digital spectrum, improving the linearity as explained in Section 3.2. So a state-of-the-art solution for clock-skew in time-interleaved ADCs should implement these three solutions at the same time : clock edge reassignment, any clock-skew calibration technique and channel randomization.

3.5.2 Comparison of Clock-Skew Calibration Techniques

Some improvements can be done in the current clock-skew calibration techniques, as explained in Subsection 3.5.3. But to show what is left to be done,

first, let us enumerate the characteristics used to describe the calibration techniques in every partial conclusion of Section 3.4 :

- **Complexity** The complexity is evaluated in terms of extra required hardware to carry out the calibration.
- **Robustness** The robustness refers to the sensibility to fabrication dispersion. The fabrication dispersion can affect the calibration subsystem itself or other elements of the circuit. A calibration technique is said to be robust when it can ensure a proper calibration even in the presence of fabrication dispersion anywhere in the circuit.
- **Input Restrictions** Some calibration techniques need the analog input signal to verify some special restrictions or requirements for the calibration system to work properly.
- **Type of Measurement** Background and foreground calibration is one possible classification for calibration techniques. Foreground calibration interrupts the normal operation to carry out the clock-skew measurements. Although it can be done during the system power-up or standby, it is desirable to run continuously a calibration to track device and environmental variations. This latter kind of calibration is called background calibration.
- **Test Signal** Some calibration systems need an internally generated test signal to perform the calibration.
- **Allowable M** This characteristic is the number of time-interleaved channels that can be handled by the correction or measurement technique.

As in Section 3.4, it can be enlightening to divide the calibration systems in correction subsystems and measurement subsystems when comparing them using the previous characteristics. The comparison will be done in a qualitative fashion. It is out of the scope of this work to determine quantitatively which is the best calibration system nowadays. The aim of this work is to propose another option and outline its advantages and drawbacks compared to previous works.

With regard to the correction techniques, table 3.1 summarizes their characteristics.

With regard to the measurement techniques, table 3.2 summarizes their characteristics.

3.5.3 Author's Mixed-Signal Calibration Technique

As a priority, a desirable calibration technique must be both simple and robust. It can be achieved by mixing two of the reviewed techniques.

From the *analog* domain, the use of an adjustable delay cell as in Wu and Black's work will provide a very simple way of correcting clock-skews, without any input restriction.

With regard to the measurement technique, from the *digital* domain, a Jamal *et al.*'s like technique would be suited. A background calibration technique would be desirable too but, to the best of the author knowledge, once the clock-skews are calibrated, there is no reason to believe that significant clock-skews will

	Complexity ^a	Robustness	Input Restrictions	Allowable M
Jamal <i>et al.</i> 's	High	Yes	Yes	2
Jin and Lee's	High	Yes	Yes	Any
Wu and Black's	Low	No ^b	No	Any

Table 3.1: Comparison of the correction techniques.

^aOnly a qualitative appreciation is given here. For details, see the respective descriptions.

^bInside a negative feedback loop, it could be *Yes*, as explained in Section 4.2.

	Complexity ^a	Robustness	Input Restrictions	Type of Measurement	Test Signal	Allowable M
Jamal <i>et al.</i> 's	Low	Yes	Yes	Foreground ^b	No ^c	2
Jin and Lee's	High	No	Yes	Foreground ^b	Yes	Any
Wu and Black's	High	No	No	Background	No	Any

Table 3.2: Comparison of the measurement techniques.

^aOnly a qualitative appreciation is given here. For details, see the respective descriptions.

^bIt is *Foreground* as long as the input restrictions are not verified.

^cAn input signal is needed, but not necessarily internally and carefully generated.

arise during the normal operation. In fact, the physical conditions will change in the same way for all the clock paths. It makes preferable a robust and simple foreground technique to a non-robust and complex background technique.

A mixed-signal circuit is the nature of the technique proposed by the author in Chapter 4, besides contributing substantial modifications on the previous work :

- In Subsection 4.3.2, a more suitable choice of the delay cell is done.
- In Subsection 4.3.3, a digital-to-analog interface is conceived for the adjustable delay cell.
- In Subsection 4.4.1, a completely new formulation of the digital clock-skew measurement is carried out to allow multiple clock-skews measurements for a general M -channels case.
- In Subsection 4.4.3, new input signal restrictions for a general M -channels

case are shown for the clock-skew measurement technique to work properly.

- In Section 4.4.4, further modifications of the measurement technique that ensure its robustness and reduce the required hardware.

Chapter 4

Mixed-Signal Calibration Technique

4.1 Calibration Technique Overview

Fig. 4.1 shows the proposed calibration technique. It is composed of two sub-

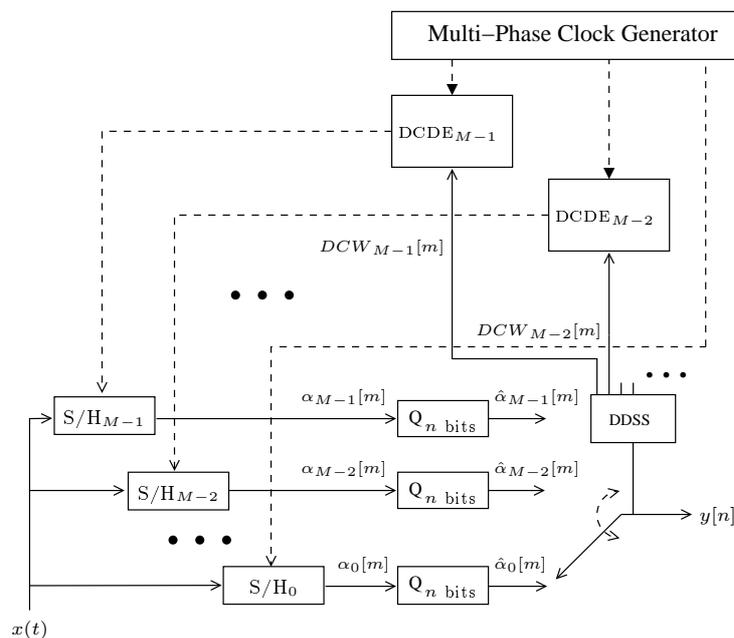


Figure 4.1: General diagram of the mixed-signal calibration technique.

systems. The clock-skew corrections are done by Digitally Controlled Delay Elements (DCDEs). The measurements are performed by a Digital Detection Subsystem (DDSS). The DDSS independently evaluates the clock-skew for each time-interleaved channel from the digital output $y[n]$. It is not done for the

zereth channel, the sampling instants of which are considered as the time reference. The DDSS outputs are the Digital Control Words (*DCWs*), binary values generated in accumulators. Then, these $M - 1$ *DCWs*, adjust $M - 1$ DCDEs respectively, placed in the sampling clock paths. The i -th DCDE modifies the actual sampling instants¹, $t_{s_i}[m]$, adding the necessary $t_{cal_i}[m]$ to compensate the clock-skew t_{e_i} :

$$t_{s_i}[m] = MTm - (M - 1 - i)T + t_{res_i}[m], \quad (4.1)$$

where

$$t_{res_i}[m] = t_{e_i} + t_{cal_i}[m], \quad (4.2)$$

i.e., the residual i -th clock-skew after the correction applied by the i -th DCDE. When $t_{cal_i}[m]$ equals $-t_{e_i}$, $t_{res_i}[m]$ becomes null and stable, i.e., it does not change or changes only by very small amounts around zero. This situation is called steady state and can be attained in a well-designed negative feedback loop.

4.2 Closed-Loop Analysis

Before entering in the details of the DCDE and the DDSS, let us take an overview on how they interact each other. Each DCDE and DDSS pair is embedded in a negative feedback loop that is independent of the other loops. These loops are individually modelled as shown in fig. 4.2. Now, let us analyse it to gain some

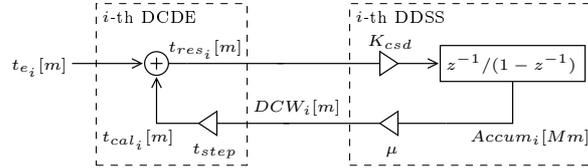


Figure 4.2: Model of the i -th clock-skew calibration loop.

insight into the loop dynamics and to help us to know how to properly set the loop parameters. From fig. 4.2, in the Z-domain, $T_{e_i}(z)$ and $T_{cal_i}(z)$ are related by :

$$T_{cal_i}(z) = H_i(z)T_{e_i}(z). \quad (4.3)$$

$H_i(z)$, the one-channel calibration system transfer function, is :

$$H_i(z) = z^{-1} \frac{\mu t_{step} K_{csd}}{1 - (1 + \mu t_{step} K_{csd})z^{-1}}, \quad (4.4)$$

where K_{csd} is the i -th clock-skew detector gain of physical units [s^{-1}] and μt_{step} is the feedback gain of physical units [s]. This system is stable if

$$|1 + \mu t_{step} K_{csd}| < 1, \text{ i.e., } -2 < \mu t_{step} K_{csd} < 0. \quad (4.5)$$

¹The causality of the DCDE is neglected for the sake of simplicity, but it can be easily taken into account by adding a constant delay in all the sampling instants.

For a given K_{csd} , μt_{step} is set to guarantee the stability and to adjust the rate of convergence and the variance of $t_{cal_i}[m]$ in the steady state. The impulse response associated to $H_i(z)$ is

$$h_i[m] = \mu t_{step} K_{csd} (1 + \mu t_{step} K_{csd})^{m-1} u[m-1], \quad (4.6)$$

where $u[m]$ is the unit step function. So, for a stable loop, the response $t_{cal_i}[m]$ to a step input signal $t_{e_i}[m] = t_{e_i} \cdot u[m]$, is :

$$t_{cal_i}[m] = \mu t_{step} K_{csd} t_{e_i} \sum_{l=1}^m (1 + \mu t_{step} K_{csd})^{l-1} u[m-1]. \quad (4.7)$$

For $m \rightarrow \infty$, $t_{cal_i}[m]$ becomes :

$$\lim_{m \rightarrow \infty} t_{cal_i}[m] = -t_{e_i}, \quad (4.8)$$

the value that cancels $t_{res_i}[m]$.

At this point, some considerations must be done :

- $z^{-1}/(1-z^{-1})$ is the transfer function of an imaginary accumulator. Physically, the output of this accumulator is the downsampled output of a real accumulator $Accum_i[n]$, as shown in Subsection 4.4.1. In practice, the feedback gain μt_{step} is generated by dropping some of the least significant bits (LSBs) of the output of this real accumulator and by applying a positive digital-to-time conversion. Analytically, $t_{cal_i}[m]$ can be written as :

$$t_{cal_i}[m] = t_{step} \cdot DCW_i[m], \quad (4.9)$$

where t_{step} is a digital-to-time conversion factor and $DCW_i[m]$ is

$$DCW_i[m] = \lfloor \mu \cdot Accum_i[Mm] \rfloor, \quad (4.10)$$

where $\lfloor \cdot \rfloor$ denotes the floor function, $Accum_i[Mm]$ is the downsampled i -th accumulator output and μ is some negative power of two. The truncation introduces a nonlinearity not considered in the previous model of the clock-skew calibration loop.

Unavoidably, due to the digital nature of the proposed system, a residual clock-skew $t_{res_i}[m]$ different from zero will persist. Let us assume a constant t_{step} for all the possible values of $DCW_i[m]$. A well-designed negative feedback loop must guarantee that

$$|t_{res_i}[m]| \leq t_{step} \quad (4.11)$$

in the steady state. Fig. 4.3 shows an example of convergence of $t_{cal_i}[m]$, for $t_{step} = 1$ ps, and $t_{e_i} = 4.8$ ps. It can be observed that the final value of $t_{cal_i}[m]$ oscillates around the actual $-t_{e_i}$.

- Note that the detection is done from the digital signal, so all clock-skews from different analog sources are merged in t_{e_i} , including those arising from mismatches between the DCDEs. From a fabrication dispersion point of view, it makes the DCDE a robust element.

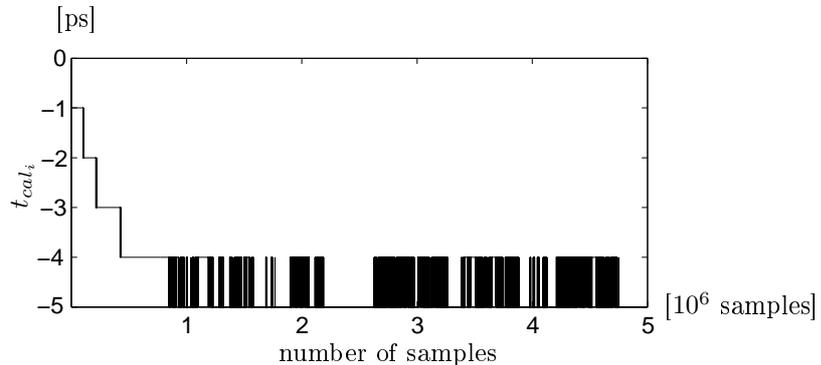


Figure 4.3: Plot of t_{cal_i} versus number of samples during calibration.

- To take into account sampling jitter, $t_{j_i}[m]$ must be added to $t_{e_i}[m]$ and $t_{cal_i}[m]$ in fig. 4.2. The response of the system evaluated at $t_{cal_i}[m]$ to sampling jitter can be seen to be the same as for clock-skew, i.e., a low pass filtering. Since sampling jitter has zero mean and only the most significant bits (MSBs) of $Accum_i[m]$ are used, the system is very robust to these sampling instants errors.

4.3 Digitally Controlled Delay Element

4.3.1 Principle of Operation

The i -th DCDE is placed between the multi-phase clock generator and the i -th time-interleaved S/H, as shown in fig. 4.1. Our DCDEs are merged in the multi-phase clock generator, as shown in fig. 4.4. This clock generator is the same used by Wu and Black, previously described in Subsection 3.4.2. Briefly, let us remind that it consists of a voltage controlled ring oscillator, composed of four differential delay cells, embedded in a PLL. The differential delay cells provide eight differential clock signals nominally shifted to drive up to eight channels of a time-interleaved ADC. In our work and in fig 4.4, only four differential clock signals are used, but it can be generalized to any even number of clock signals. This clock generator, and particularly the differential choice, is justified in Section 5.4.2.

In general, the differential clock signals must be single-ended converted and buffered before using them as sampling clocks. Therefore, differential-to-single-ended converters (denoted DTSECs) are needed. But in our calibration strategy, they perform a differential-to-single-ended conversion as well as sampling instant correction. The aim of this choice is to add as few as possible extra hardware to perform the calibration operations.

Our DCDE can be classified into the category of digitally controlled current starved delay elements. A shunt capacitor technique is not retained because it does not offer any advantage in comparison with using a current starved DTSEC circuit. Fig. 4.5 shows the two subcircuits that compose a DCDE : a DTSEC and a digitally trimmable bias generator (denoted DTBG).

- The DTSEC performs a nearly linear voltage-to-time conversion : for a

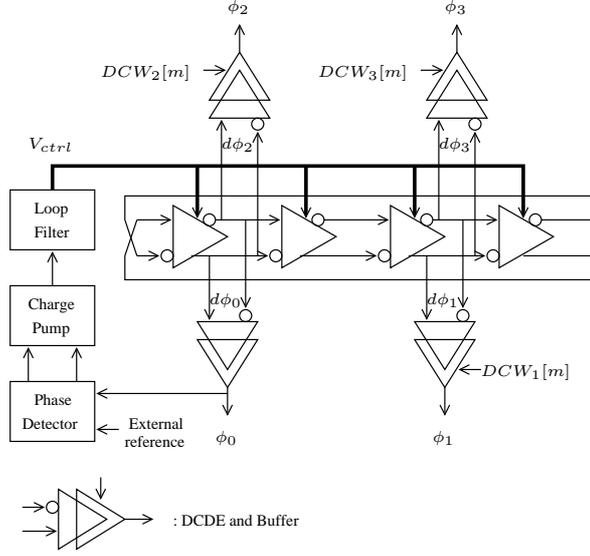


Figure 4.4: Diagram of a multi-phase clock generator and DCDEs.

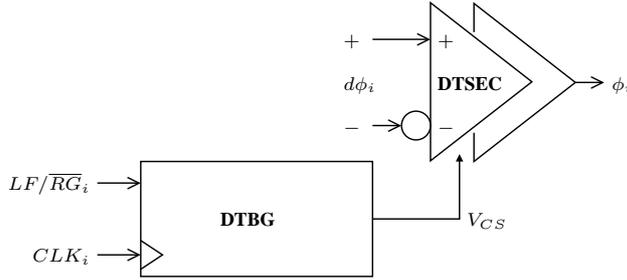


Figure 4.5: Diagram of the DCDE.

given input voltage V_{CS} , there is a proportional *relative delay* as explained in detail in Subsection 4.3.2. Let us define *delay* as the time needed for the differential clock signal $d\phi_i$ to go through the differential-to-single-ended converter and become the sampling clock signal ϕ_i . Fig. 4.7 shows a plot of *relative delay* versus V_{CS} extracted from transient electrical simulations of a differential-to-single-ended converter. Let the slope of this curve be denoted by SV , of physical units [s/V].

- The DTBG performs a linear digital-to-voltage conversion. For a given $DCW_i[m]$, there is an associated voltage V_{CS} . Let the VD parameter of physical units [V] be the conversion factor. Note that there is no $DCW_i[m]$ signal present in fig. 4.5, but CLK_i and LF/\overline{RG}_i signals. These signals transmit information equivalent to the $DCW_i[m]$ in serial fashion. It is explained in Subsections 4.3.3 and 4.4.5.

The global digital-to-time factor $VD \cdot SV$, of physical units [s], is the already

mentioned in Section 4.2 t_{step} parameter :

$$t_{step} = VD \cdot SV. \quad (4.12)$$

4.3.2 Differential-To-Single Ended Converter

The chosen DTSEC is shown in fig. 4.6. It is composed of two identical NMOS

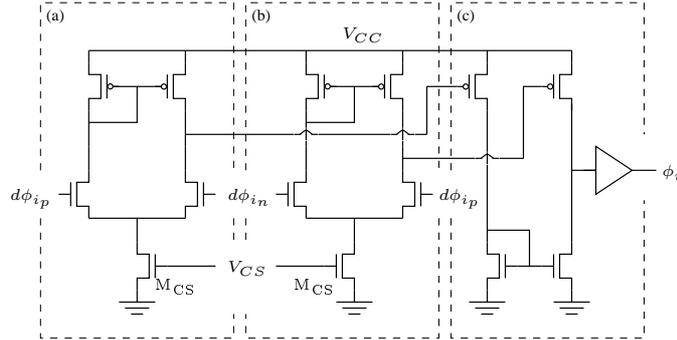


Figure 4.6: DTSEC and clock buffer.

differential amplifiers with active current mirror (inside the dashed boxes labeled (a) and (b)) and two PMOS common-source amplifiers connected by an NMOS current mirror plus a clock buffer (inside the dashed box labeled (c)). This structure provides a single-ended rail-to-rail clock signal with roughly a 50% of duty cycle [39], a desirable feature for a sampling clock signal. There are two inputs signals : the differential clock signal $d\phi_i$, measured between $d\phi_{ip}$ and $d\phi_{ip}$, and V_{CS} . V_{CS} is the bias voltage of the transistors M_{CS} . It controls the bias currents of the differential amplifiers and, hence, the charge transfer speed during output transitions.

As it has been previously mentioned, the DTSEC performs a nearly linear voltage-to-time conversion between the input voltage V_{CS} and a *relative delay* added by itself. Let us define *delay* as the absolute time needed for $d\phi_i$ to go through the DTSEC and become the sampling clock signal ϕ_i . Let us define *relative delay* as the difference between *delay* for a given V_{CS} and *delay* for the minimum applicable V_{CS} , denoted $V_{CS_{min}}$. It is simply modeled by² :

$$relative\ delay = SV \cdot (V_{CS} - V_{CS_{min}}). \quad (4.13)$$

Out of this Subsection, *relative delay* is denoted $t_{cal_i}[m]$. This model holds as long as $V_{CS_{min}} \leq V_{CS} \leq V_{CS_{max}}$. The $V_{CS_{min}}$ and $V_{CS_{max}}$ bounds depend on the desired linearity as well as the operation regions of the transistors M_{CS} . V_{CS} must be high enough to guarantee that the two M_{CS} are active (i.e., $V_{CS_{min}} > V_{TH_n}$) and low enough to guarantee that the two M_{CS} are in the saturation region, even for the minimal values of ϕ_{ip} and ϕ_{in} . The saturation must be guaranteed to preserve a reasonable common mode rejection ratio [56]. If not, the coupled noise in the $d\phi_i$ common mode signal could add a not tolerable extra jitter during the differential-to-single-ended conversion.

Fig. 4.7 shows the plot of *relative delay* versus V_{CS} . The plot also shows the

²delay for $V_{CS_{min}}$ ensures the causality of the circuit even if in the following paragraphs negative values of *relative delay* are shown.

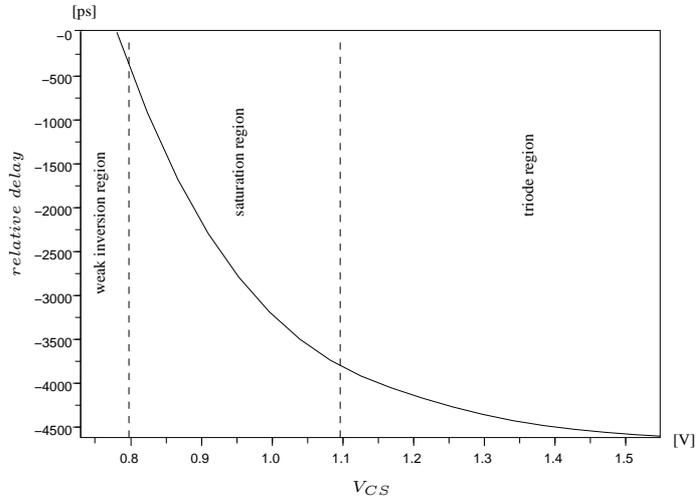


Figure 4.7: Plot of *relative delay* versus V_{CS} of our DTSEC.

limits of the M_{CS} polarization regions. When increasing V_{CS} , once the triode region is reached, *relative delay* is less sensitive to the V_{CS} variations. It is the expected behavior because the bias current of the differential amplifiers is less dependent on V_{CS} when M_{CS} are in triode region.

Fig. 4.7 demonstrates that the model shown in (4.13) is justified, specially for V_{CS} variations limited to some mV, i.e., some tens of ps.

4.3.3 Digitally Trimmable Bias Generator

Principle of Operation

The DTBG performs a linear digital-to-voltage conversion between $DCW_i[m]$ and V_{CS} . Fig. 4.8 shows a simplified diagram of the DTBG. The digital inputs

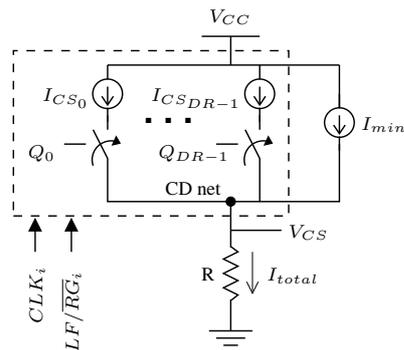


Figure 4.8: Simplified diagram of the DTBG.

signals are CLK_i and LF/\overline{RG}_i . The analog output signal is V_{CS} . CLK_i and LF/\overline{RG}_i are decoded to form $DCW_i[m]$ inside the dashed box. It is stored by DR static storage cells denoted Q_l , $0 \leq l \leq DR - 1$. Q_l activates (for *high*

logic state) or deactivates (for *low* logic state) a l -th current source that injects I_{CS_l} when it is active. The currents from all the active current sources are added at CD net. It performs a digital-to-current conversion that is assumed to be linear. Finally, the resistance R carries out a linear current-to-voltage conversion generating V_{CS} . I_{min} , from a continuously active current source, is also added at CD net to guarantee that $V_{CS} \geq V_{CS_{min}}$, even when all Q_l are in *low* state. V_{CS} is simply :

$$V_{CS} = R \cdot I_{total}, \quad (4.14)$$

where

$$I_{total} = \sum_{l=0}^{DR-1} Q_l I_{CS_l} + I_{min}. \quad (4.15)$$

Thermometrical Code VS Binary Code

An ambiguity in the code used to store $DCW_i[m]$ is deliberately left in the previous paragraph. The binary code minimizes DR . However, as explained in the following paragraphs, it would provide the poorest control over the actual value of t_{step} . On the other hand, the thermometrical code maximizes DR but it provides the greatest control over t_{step} .

The value of t_{step} is intuitively derived in (4.12). However, assumptions in the linearity of all the conversion process have been taken. From now on, the linearity of the digital-to-current conversion is no longer assumed. Let us redefine t_{step} here, considering it rather as a vector than as a scalar. In fact, t_{step_j} is just the delay difference between two consecutive values of $DCW_i[m]$, denoted j and $j + 1$:

$$t_{step_j} = SV \cdot R \cdot (I_{total}(j+1) - I_{total}(j)), \quad 0 \leq j \leq DR - 2. \quad (4.16)$$

This definition makes sense specially because during convergence the $DCW_i[m]$ only can change by one unity at the same time.

The value of every t_{step_j} will be affected by fabrication dispersion in I_{CS_l} , R and in the value of SV . If the fabrication dispersion in I_{CS_l} is not considered, it could even prevent the digital-to-voltage conversion from being monotonic. On the other hand, dispersion in R and SV affects by the same amount all the t_{step_j} , calling into question neither the monotonicity nor the linearity of the overall digital-to-time conversion. In practice, the design of the DCDE should guarantee :

$$\frac{\sigma(t_{step_j})}{\overline{t_{step}}} \leq \epsilon, \quad \forall j, \quad (4.17)$$

where $\sigma(t_{step_j})$ is the standard deviation of t_{step_j} , $\overline{t_{step}}$ is the mean value of t_{step_j} (generally the same for all j), and ϵ is the relative t_{step} dispersion tolerated.

Recall from Section 4.2 that $|t_{res}| < t_{step}$. $\sigma(t_{step_j})$ must be set in such a way that the probability of having a *too high* t_{res} is as low as desired. What is a *too high* t_{res} depends on the desired SFDR of the time-interleaved ADC. From now on, only the dispersion in I_{CS_l} is considered.

The switchable current sources that provide I_{CS_l} are simple PMOS transistors or sets of parallel PMOS transistors, biased in saturation region when they are active. The short distance matching is defined as the matching of two identically designed devices placed close to each other. In CMOS technology,

the relative drain current measured from two identically designed transistors enjoys of a great short distance matching. On the other hand, the absolute value of this drain current could exhibit high variations from its nominal value. It advises against using differently sized and biased PMOS transistors. The best accuracy in the relative t_{step_j} is obtained by replicating an identically designed PMOS transistor as many times as necessary to obtain the desired I_{CS_l} . Let us call this PMOS transistor *basic transistor* or *basic current source*. $\overline{I_{step}}$ is the nominal current provided by any basic transistor biased in saturation region. For a thermometrical code, the actual current of the basic transistors is denoted I_{step_l} , and $I_{CS_l} = I_{step_l}$. For a binary code it is denoted $I_{step_{l,k}}$, and $I_{CS_l} = \sum_{k=0}^{2^l} I_{step_{l,k}}$.

These technological considerations lead us to use the Pelgrom model [50] to estimate the relative t_{step_j} dispersion. It relates the matching on the drain current of two identically designed devices to their area :

$$\frac{\sigma(I_{step})}{\overline{I_{step}}} = \frac{A_I}{\sqrt{W \cdot L}}, \quad (4.18)$$

where A_I is a short-distance relative drain current matching parameter³ and $W \cdot L$ the transistor area. From it, the relative t_{step_j} dispersion is computed as follows :

- For a **thermometrical code**, $Q_l(j) = 1$ if $l < j$, otherwise $Q_l(j) = 0$. Then, (4.16) can be rewritten as :

$$t_{step_j} = SV \cdot R \cdot \sum_{l=0}^{DR-1} [Q_l(j+1)I_{step_l} - Q_l(j)I_{step_l}] = SV \cdot R \cdot I_{step_{j+1}}. \quad (4.19)$$

So the value of $\overline{t_{step}}$ is :

$$\overline{t_{step}} = SV \cdot R \cdot \overline{I_{step}}, \quad (4.20)$$

and the value of the relative t_{step_j} dispersion is :

$$\frac{\sigma(t_{step_j})}{\overline{t_{step}}} = \frac{A_I}{\sqrt{W \cdot L}}, \quad \forall j, \quad (4.21)$$

i.e., the same relative dispersion than that of the drain current of basic transistors.

- For a **binary code**, the mean relative t_{step_j} dispersion⁴ is inductively derived in Appendix E. The final result is :

$$\frac{\sigma(t_{step})}{\overline{t_{step}}} = \sqrt{\frac{\sum_{i=0}^{DR-1} (2^{DR-i} - 1) 2^i}{2^{DR} - 1}} \frac{A_I}{\sqrt{W \cdot L}}. \quad (4.22)$$

³In general, for a given CMOS technology, there are three short-distance matching parameters : the current gain factor, the substrate factor and the threshold voltage. A short-distance relative drain current matching parameter A_I can be derived from the operation point of a transistor and the three previously mentioned short-distance matching parameters. It is further discussed in Appendix F. In this Chapter, A_I is used instead to simplify the writing.

⁴As shown in Appendix E, for a binary code the relative t_{step_j} dispersion is a function of j . The mean relative t_{step_j} dispersion is the mean value of $\sigma(t_{step_j})/\overline{t_{step}}$, denoted here $\sigma(t_{step})/\overline{t_{step}}$.

From it, the greater DR , the greater the mean relative t_{step_j} dispersion.

For high values of DR , the required area and power consumption of the basic current source for a binary code to meet the same ϵ parameter than a thermometrical code makes preferable the latter choice. In our work, the thermometrical code has been the chosen one.

Shift Register and Serial $DCW_i[m]$ Transmission

The previous paragraphs have shown that the thermometrical code is the best suited to code the $DCW_i[m]$ inside the DTBG. For this code, if the number of static storage cells is DR , then $0 \leq DCW_i[m] \leq DR$. Let us define the clock-skew correction range as $\max\{t_{e_i}\} - \min\{t_{e_i}\}$, where $\max\{t_{e_i}\}$ and $\min\{t_{e_i}\}$ denotes the highest and lowest t_{e_i} expected to be found in the clock generation system. The value of DR required by a calibration system that must handle these t_{e_i} limits is :

$$DR = \frac{\max\{t_{e_i}\} - \min\{t_{e_i}\}}{t_{step}}. \quad (4.23)$$

A great DR can be necessary if the clock-skew correction range is very large in comparison with t_{step} . Fortunately, due to the step-by-step convergence nature of the closed-loop dynamics, a random access to the static storage cells is not required (i.e., they are not static random access memories), which simplifies the design. In fact, this feature allows us to organize the static storage cells in a shift register, as shown in fig. 4.9. More precisely, it is a bidirectional shift

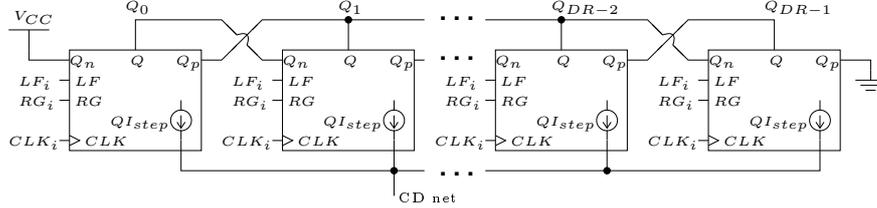


Figure 4.9: Diagram of a shift register of correction cells.

register, serial-in, parallel-out (SIPO).

DR correction cells are represented by boxes in fig. 4.9. The diagram of the proposed correction cell is shown in fig. 4.10. It is formed by a static storage

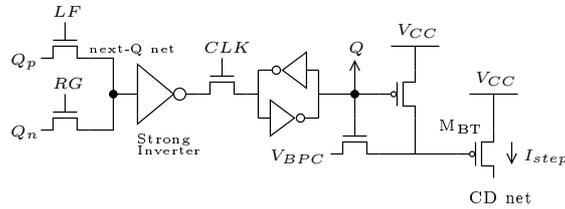


Figure 4.10: Diagram of a correction cell formed by a static storage cell, a basic current source and control transistors.

cell, the basic transistor denoted as M_{BT} , and some control transistors. The V_{BPC} voltage is the bias voltage applied to the basic transistors when $Q = 1$.

The static storage cells are formed by two cross-coupled inverters. The control transistors provide bidirectionality and synchronous behavior. The bidirectional shift operation is as follows : for CLK in *low* state, activating LF or RG allows to load the next-Q net in the l -th register with the present state of Q_{l+1} or Q_{l-1} respectively. For CLK in *high* state, both LF and RG are externally deactivated and a strong inverter is allowed to load Q_l with the state of next-Q net.

Because of the initial unknown state of all Q_l , a reset cycle is necessary before calibration. It is done by activating LF_i during DR periods of CLK_i . Note that a *low* state is constantly present at the top-right side of the shift register in fig. 4.9. This *low* state is propagated through all the registers during reset cycle. On the other hand, a *high* state is constantly present at the top-left side of the shift register. The *high* state and the *low* state are propagated through the registers during normal operation.

As shown, the shift register serves as serial-to-parallel converter. The CLK_i and LF/\overline{RG}_i serial interface minimizes the number of transmission lines between the DDSS and the i -th DCDE. If not used, the amount of wiring of a fully parallel architecture would make this circuit unfeasible even for moderate values of DR .

Depending on the value of DR and the number of channels, the area of the shift registers could be the most significant term when computing the total area of the calibration system. Therefore, the layout of the registers must be carefully designed to minimize it.

Current-to-Voltage Conversion

A simplified diagram of the DTBG has been previously shown in fig. 4.8. It is repeated in fig. 4.11 for reading convenience.

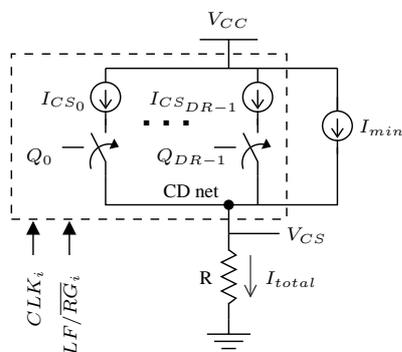


Figure 4.11: Simplified diagram of the DTBG.

In a real implementation, the resistor R could be replaced by a diode-connected NMOS transistor as long as the clock-skew correction range is small and the designer is aware of the different sizes of t_{step} at the extremes of this range. In any case, the monotonicity of the current-to-voltage conversion is not questioned.

To further homogenize the size of t_{step} , the output-impedance current mirrors can be augmented. In fact, the drain-source voltage of the basic transistors that provide I_{step_j} depends on V_{CS} in this diagram. Ideally, when the basic transistors are biased in saturation region, the value of I_{step_j} is independent

of V_{CS} . In practice, due to channel-length modulation [63], the basic current sources have a finite output impedance and I_{step_j} depends on V_{CS} , limiting the linearity of the digital-to-voltage conversion. To overcome it, enhanced output-impedance current mirrors are used [26]. Here, this technique does not modify the previously detailed registers, as shown in fig. 4.12. It simply adds an opamp

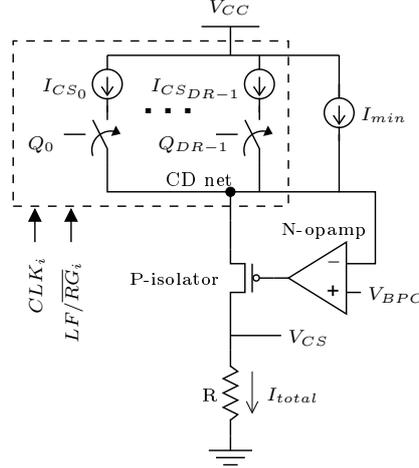


Figure 4.12: Diagram of the DTBG with enhanced output-impedance current mirrors.

(denoted N-opamp) and a PMOS transistor (denoted P-isolator) in the I_{total} path. They are shared by all the basic current sources. Their function is to keep the CD net voltage stable around V_{BPC} for all normal values of V_{CS} . Recall from fig. 4.10 that V_{BPC} is also the gate voltage of the active basic transistors, which guarantees that basic transistors are in saturation if they are active. The N-opamp and the P-isolator forms a feedback loop that increases the output impedance by a factor equal to one plus the loop gain [35]. The basic idea is that N-opamp modifies the gate voltage of P-isolator in such a way that the source voltage of P-isolator remains V_{BPC} while I_{total} can flow through it.

Depending on the availability of analog elements in a given CMOS technology, it can be interesting to avoid the use of resistors. The previous technique can again be used with a NMOS transistor instead of a resistor. It is shown in fig. 4.13. Now, the P-opamp and the N-isolator keep a NMOS transistor (denoted MOS res) in the triode region with a stable drain-source voltage of value V_{BNC} . It is true if $V_{BNC} < V_{CS} - V_{TH_n}$. Then, I_{total} can be written as :

$$I_{total} = k_n \left(\frac{W}{L} \right) \left[(V_{CS} - V_{TH_n})V_{BNC} - \frac{1}{2}V_{BNC}^2 \right], \quad (4.24)$$

where (W/L) is the aspect ratio of MOS res, V_{TH_n} the n-channel voltage threshold, and $k_n = \mu_n C_{ox}$, being μ_n the n-channel mobility of electrons and C_{ox} the gate capacitance per unit area.

The equation relating $t_{cal_i}[m]$, $DCW_i[m]$ and the previous parameters is derived in this paragraph. From (4.15), for a thermometrical code and assuming $t_{step_j} = t_{step} \forall j$, I_{total} can be rewritten as :

$$I_{total} = I_{step} \cdot DCW_i[m] + I_{min}. \quad (4.25)$$

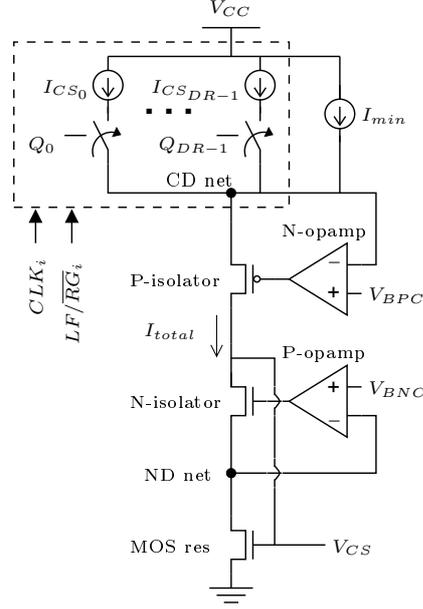


Figure 4.13: Diagram of the resistorless DTBG.

Substituting (4.25) in (4.24), V_{CS} can be isolated as a function of DCW_i . Now, substituting V_{CS} in (4.13)⁵, gives :

$$t_{cal_i}[m] = t_{step} \cdot DCW_i[m] + SV \left(V_{TH_n} + \frac{V_{BNC}}{2} + \frac{I_{min}}{k_n V_{BNC} \left(\frac{W}{L}\right)} - V_{CS_{min}} \right), \quad (4.26)$$

where

$$t_{step} = \frac{SV \cdot I_{step}}{k_n V_{BNC} \left(\frac{W}{L}\right)}. \quad (4.27)$$

Interesting, this equation shows that V_{BNC} can potentially change the value of t_{step} .

Defining

$$V_{CS_{min}} = V_{TH_n} + \frac{V_{BNC}}{2} + \frac{I_{min}}{k_n V_{BNC} \left(\frac{W}{L}\right)}, \quad (4.28)$$

the second term in (4.26) is cancelled. Note that if any parameter in (4.28) does not match between different DCDEs, t_{e_i} will increase.

Fig. 4.14 plots some voltage values of the resistorless DTBG versus $I_{step}DCW_i[m]$. This plot is obtained from DC electrical simulations.

⁵(4.13) is repeated here for reading convenience :

$$t_{cal_i} = SV \cdot (V_{CS} - V_{CS_{min}}).$$

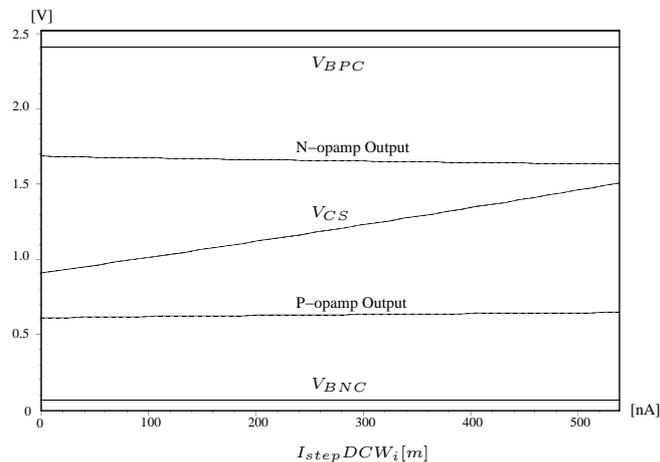


Figure 4.14: Plot of V_{BPC} , N-opamp output voltage, V_{CS} , P-opamp output voltage and V_{BNC} versus $I_{step} DCW_i [m]$.

4.4 Digital Detection Subsystem

4.4.1 Principle of Operation

This technique applies to a M -channels time-interleaved ADC. Considering the 0-th channel as the reference one, a digital clock-skew detection must be performed on each one of the remaining $M - 1$ channels. From the model shown in fig. 4.2, a mean of sensing a value proportional to $t_{res_i} [m]$ (or t_{e_i} in an open-loop configuration) is needed, where the proportionality factor is denoted K_{csd} . However, t_{e_i} cannot be directly observed, but it must be extracted from the digital output signal $y[n]$. Fig. 4.15 illustrates this idea. The value of K_{csd} and

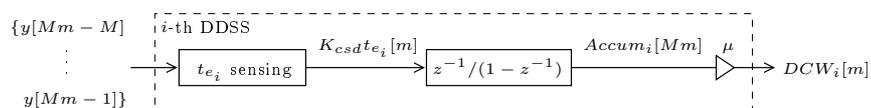


Figure 4.15: Preliminary diagram of the DDSS.

a hardware description of the t_{e_i} sensing block is analytically derived in the following paragraphs.

Let the input signal $x(t)$ be a sinusoidal signal,

$$x(t) = A_{in} \cos\left(\frac{\omega_{in}}{T} t + \phi_{in}\right). \quad (4.29)$$

Since this subsystem is analyzed in open-loop configuration, t_{e_i} is used instead of t_{res_i} . In closed-loop configuration, just replace t_{e_i} with t_{res_i} .

The cross-correlation $r_{fg}[l]$ of two ergodic signals $f[n]$ and $g[n]$ is defined as [47] :

$$r_{fg}[l] = \lim_{P \rightarrow \infty} \frac{1}{2P+1} \sum_{p=-P}^P f[p+l]g[p]. \quad (4.30)$$

The notation $r_{fg}[l]$ will be extensively used for writing convenience. Let the $\alpha_i[m]$ signal be the sampled signal by the i -th channel at the sampling instants

$$t_{s_i}[m] = MTm - (M-1-i)T + t_{e_i}, \quad (4.31)$$

The $\hat{\alpha}_i[m]$ is the i -th quantizer output. Let us neglect the effect of the quantizers from now on. The DC component of the signal resulting from $\hat{\alpha}_i[m] \cdot \hat{\alpha}_{i-1}[m]$, $\forall m$, is the 0 evaluated cross-correlation between $\hat{\alpha}_i[m]$ and $\hat{\alpha}_{i-1}[m]$. As shown in Appendix D, for a sinusoidal input signal, the $r_{\hat{\alpha}_i \hat{\alpha}_{i-1}}[0]$ is :

$$r_{\hat{\alpha}_i \hat{\alpha}_{i-1}}[0] = \frac{A_{in}^2}{2} \cos\left(\omega_{in} + \frac{\omega_{in}}{T}(t_{e_i} - t_{e_{i-1}})\right) + \overline{res_{i,i-1}[0]}, \quad (4.32)$$

for $1 \leq i \leq M-1$,

where $\overline{res_{i,i-1}[0]}$ is considered as a residual component.

Next, for the mentioned input signal, the DC component of the signal $\hat{\alpha}_0[m] \cdot \hat{\alpha}_{M-1}[m-1]$ is the +1 evaluated cross-correlation between $\hat{\alpha}_0[m]$ and $\hat{\alpha}_{M-1}[m]$:

$$r_{\hat{\alpha}_0 \hat{\alpha}_{M-1}}[1] = \frac{A_{in}^2}{2} \cos\left(\omega_{in} - \frac{\omega_{in}}{T}t_{e_{M-1}}\right) + \overline{res_{0,M-1}[1]}. \quad (4.33)$$

Recall that $t_{e_0} = 0$ because the channel zero is considered as the reference one. (4.32) and (4.33) can be linearized by Taylor series expansion up to the first derivative around $t_{e_i} - t_{e_{i-1}}$ and $t_{e_{M-1}}$ respectively [21] :

$$r_{\hat{\alpha}_i \hat{\alpha}_{i-1}}[0] \approx \frac{A_{in}^2}{2} \cos(\omega_{in}) + \delta(\omega_{in})(t_{e_i} - t_{e_{i-1}}) + \overline{res_{i,i-1}[0]}, \quad (4.34a)$$

for $1 \leq i \leq M-1$,

$$r_{\hat{\alpha}_0 \hat{\alpha}_{M-1}}[1] \approx \frac{A_{in}^2}{2} \cos(\omega_{in}) - \delta(\omega_{in})t_{e_{M-1}} + \overline{res_{0,M-1}[1]}, \quad (4.34b)$$

where $\delta(\omega_{in})$ is :

$$\delta(\omega_{in}) = \left. \frac{d\left(\frac{A_{in}^2}{2} \cos\left(\omega_{in} + \frac{\omega_{in}}{T}t_e\right)\right)}{dt_e} \right|_{t_e=0} = -\frac{A_{in}^2 \omega_{in}}{2T} \sin(\omega_{in}). \quad (4.35)$$

Note that the sign of $\delta(\omega_{in})$ is constant and known as long as

$$(l-1)\pi < \omega_{in} < l\pi, \quad l \in \mathbb{N}, \quad (4.36)$$

i.e., the input signal is a bandlimited signal. Particularly, if $0 < \omega_{in} < \pi$, then $\delta(\omega_{in}) < 0$. It can be used to unequivocally form a negative feedback loop.

In (4.34), only the terms proportional to t_{e_i} are of interest. For an unknown or unprecise input signal, the presence of the term $\frac{A_{in}^2}{2} \cos(\omega_{in})$ in both subequations in (4.34) prevents us from obtaining the t_{e_i} terms from simply the +1 and 0 cross-correlations. However, they can be isolated by the following arithmetic manipulations :

- First, the λ term is defined as :

$$\lambda = r_{\hat{\alpha}_0 \hat{\alpha}_{M-1}}[1] + r_{\hat{\alpha}_{M-1} \hat{\alpha}_{M-2}}[0] + \dots + r_{\hat{\alpha}_1 \hat{\alpha}_0}[0]. \quad (4.37)$$

Substituting (4.34) in (4.37), we have :

$$\lambda \approx M \frac{A_{in}^2}{2} \cos(\omega_{in}) + \sum_{i=1}^{M-1} \overline{res_{i,i-1}[0]} + \overline{res_{0,M-1}[1]}, \quad (4.38)$$

i.e, M times the undesired term plus the $\overline{res_{i,i-1}[0]}$ and $\overline{res_{0,M-1}[1]}$ terms.

- Now, to isolate the desired t_{e_i} terms, the following operations must be performed :

$$\delta(\omega_{in})t_{e_i} + \frac{\overline{res_{tot_i}}}{M} \approx \sum_{q=1}^i r_{\hat{\alpha}_q \hat{\alpha}_{q-1}}[0] - \frac{i}{M} \lambda, \text{ for } 1 \leq i \leq M-1. \quad (4.39)$$

where $\overline{res_{tot_i}}$ groups the $\overline{res_{i,i-1}[0]}$ and $\overline{res_{0,M-1}[1]}$ terms.

A rewriting of (4.39) substituting λ by its definition will allow us to find a practical implementation. Moreover, both sides of (4.39) are scaled by M to avoid the presence of fractional numbers :

$$\begin{aligned} M\delta(\omega_{in})t_{e_i} + \overline{res_{tot_i}} &\approx \\ (M-i) \sum_{q=1}^i r_{\hat{\alpha}_q \hat{\alpha}_{q-1}}[0] - i \sum_{q=i+1}^{M-1} r_{\hat{\alpha}_q \hat{\alpha}_{q-1}}[0] - i r_{\hat{\alpha}_0 \hat{\alpha}_{M-1}}[1], &\quad (4.40) \\ &\text{for } 1 \leq i \leq M-1, \end{aligned}$$

where

$$\begin{aligned} \overline{res_{tot_i}} &= \\ (M-i) \sum_{q=1}^i \overline{res_{q,q-1}[0]} - i \sum_{q=i+1}^{M-1} \overline{res_{q,q-1}[0]} - i \overline{res_{0,M-1}[1]}, &\quad (4.41) \\ &\text{for } 1 \leq i \leq M-1. \end{aligned}$$

From now on, let us assume that $\overline{res_{tot_i}}$ is zero up to Subsection 4.4.3. Substituting (4.30) in (4.40) :

$$\begin{aligned} M\delta(\omega_{in})t_{e_i} &\approx \\ \lim_{P \rightarrow \infty} \frac{1}{2P+1} \sum_{p=-P}^P \left[(M-i) \sum_{q=1}^i \hat{\alpha}_q[p] \hat{\alpha}_{q-1}[p] \right. &\quad (4.42) \\ \left. - i \sum_{q=i+1}^{M-1} \hat{\alpha}_q[p] \hat{\alpha}_{q-1}[p] - i \hat{\alpha}_0[p] \hat{\alpha}_{M-1}[p-1] \right], & \\ &\text{for } 1 \leq i \leq M-1. \end{aligned}$$

From (4.42), a hardware implementation is analytically derived in the following paragraphs.

Let us assume that $\hat{\alpha}_q[m] = 0$ if $m < 0$, and that $\lim_{P \rightarrow \infty} \frac{1}{2P+1} \sum_{p=-P}^P \{\cdot\}$ in (4.42) can be approximated by a finite operation provided that P is sufficiently large. Under these assumptions, renaming P for m , from (4.42) we find

$$K_{csd} t_{e_i} m \approx \sum_{p=0}^{m-1} \left[\sum_{q=1}^{M-1} \hat{\alpha}_q[p] \hat{\alpha}_{q-1}[p] c_i[q-1] + \hat{\alpha}_0[p] \hat{\alpha}_{M-1}[p-1] c_i[M-1] \right], \quad (4.43)$$

for $1 \leq i \leq M-1$, $m \geq 0$,

where

$$K_{csd} = M\delta(\omega_{in}), \quad (4.44)$$

and $c_i[n]$ is this finite vector :

$$c_i[n] = \{(M-i)_0, \dots, (M-i)_{M-1-i}, -i_{M-i}, \dots, -i_{M-1}\}, \quad (4.45)$$

for $1 \leq i \leq M-1$

where the subscripts indicate the position in the vector.

The contact point between the model used in Section 4.2 and the actual physical implementation is (4.43).

Let us look at (4.43) from the model point of view. The left hand side of (4.43) is well modelled by the i -th DDSS box of the closed-loop model shown in fig. 4.2. Since $\hat{\alpha}_q[m] = 0$ if $m < 0$, $t_{e_i}[m]$ verifies

$$t_{e_i}[m] = \begin{cases} t_{e_i}, & m \geq 0, \\ 0, & m < 0, \end{cases} \quad (4.46)$$

so

$$K_{csd} \sum_{p=-\infty}^{m-1} t_{e_i}[p] = K_{csd} t_{e_i} m, \text{ for } 1 \leq i \leq M-1, m \geq 0. \quad (4.47)$$

In the Z-domain, the transfer function of the left hand side operation is $K_{csd} \cdot z^{-1}/(1-z^{-1})$. This result has been previously used in Section 4.2.

Now, let us look at (4.43) from the physical implementation point of view. The right hand side of (4.43) can be rewritten in terms of $y[n]$:

$$Accum_i[Mm] = \sum_{p=0}^{m-1} \left[\sum_{q=1}^{M-1} \hat{\alpha}_q[p] \hat{\alpha}_{q-1}[p] c_i[q-1] + \hat{\alpha}_0[p] \hat{\alpha}_{M-1}[p-1] c_i[M-1] \right], \quad (4.48)$$

where

$$Accum_i[n] = \sum_{r=0}^{n-1} y[r] y[r-1] c_i[(r-1)_{\text{mod} M}], \quad (4.49)$$

where $(\cdot)_{\text{mod} M}$ denotes the modulo M operation. This equality is proved next.

Recall (2.2),

$$y[n] = \sum_{i=0}^{M-1} \hat{\alpha}_i \left[\frac{n-i}{M} \right],$$

where

$$\hat{\alpha}_i \left[\frac{n-i}{M} \right] = \begin{cases} \hat{\alpha}_i \left[\frac{n-i}{M} \right], & \text{if } \left[\frac{n-i}{M} \right] \in \mathbb{Z}, \\ 0, & \text{if } \left[\frac{n-i}{M} \right] \notin \mathbb{Z}, \end{cases}$$

From (2.2), $y[n-1]$ can be written as :

$$y[n-1] = \sum_{i=1}^{M-1} \hat{\alpha}_{i-1} \left[\frac{n-i}{M} \right] + \hat{\alpha}_{M-1} \left[\frac{n}{M} - 1 \right]. \quad (4.50)$$

Substituting (2.2) and (4.50) in (4.49), for $n = Mm$,

$$Accum_i[Mm] = \quad (4.51)$$

$$\sum_{r=0}^{Mm-1} \left(\sum_{j=0}^{M-1} \hat{\alpha}_j \left[\frac{r-j}{M} \right] \right) \left(\sum_{l=1}^{M-1} \hat{\alpha}_{l-1} \left[\frac{r-l}{M} \right] + \hat{\alpha}_{M-1} \left[\frac{r}{M} - 1 \right] \right) c_i[(r-1)_{\text{mod}M}].$$

Changing r for $Mp+q$, and $\sum_{r=0}^{Mm-1} \{\cdot\}$ for $\sum_{p=0}^{m-1} \sum_{q=0}^{M-1} \{\cdot\}$, (4.51) becomes (4.48).

The hardware implementation of the DDSS can be directly extracted from (4.49). It is shown in fig. 4.16, where the $c_{iP}[n]$ signals are the cyclic repetition of the

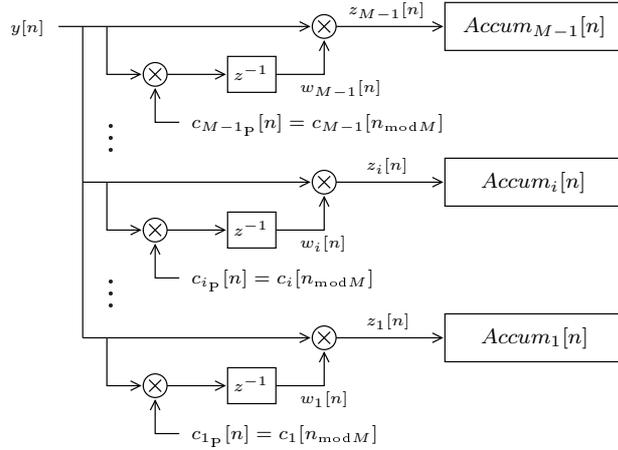


Figure 4.16: Diagram of the DDSS.

$c_i[n]$ vectors, the i -th row of the modulation matrix \mathbf{C} of size $(M-1) \times M$, the first row of which corresponds to $i=1$:

$$\mathbf{C} = \begin{pmatrix} M-1 & -1 & \dots & & -1 \\ M-2 & M-2 & -2 & \dots & -2 \\ \vdots & & & & \vdots \\ 1 & 1 & \dots & 1 & -(M-1) \end{pmatrix}. \quad (4.52)$$

To further simplify the hardware used by the DDSS, the weighted accumulators shown in fig. 4.17 incorporate the $c_{iP}[n]$ sequences.

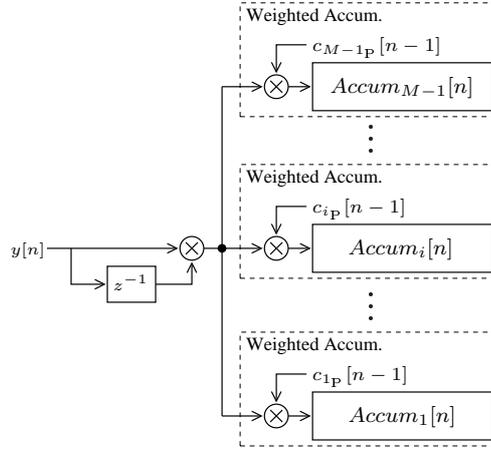


Figure 4.17: Simplified diagram of the DDSS.

4.4.2 Analysis for a multiple sinusoidal input signal

The following paragraphs show that the $x(t)$ input signal can be a more general signal than a simple sinusoidal signal. However, $x(t)$ must meet certain conditions for the DDSS to work properly. They are derived in Subsection 4.4.3.

Let $x(t)$,

$$x(t) = \sum_{\forall in} A_{in} \cos\left(\frac{\omega_{in}}{T}t + \phi_{in}\right), \quad (4.53)$$

be a bandlimited analog input signal, i.e., $0 < \omega_{in} < \pi$, $\forall in$. In the following paragraphs, only the case of two sinusoidal input signal is considered. Results from this case can be generalized to any number of sinusoidal input signals. As explained in Appendix D, two discrete-time sinusoidal signals at different frequencies are in general uncorrelated (null value). Therefore, the expressions in (4.32) and (4.33) can be generalized to hand a more complex input signal as that shown in (4.53) ignoring all the cross-correlations between signals of different frequencies :

$$r_{\hat{\alpha}_i \hat{\alpha}_{i-1}}[0] = \sum_{\forall in} \frac{A_{in}^2}{2} \cos\left(\omega_{in} + \frac{\omega_{in}}{T}(t_{e_i} - t_{e_{i-1}})\right) + \overline{res_{i,i-1}[0]}, \quad (4.54)$$

for $1 \leq i \leq M-1$.

$$r_{\hat{\alpha}_0 \hat{\alpha}_{M-1}}[1] = \sum_{\forall in} \frac{A_{in}^2}{2} \cos\left(\omega_{in} - \frac{\omega_{in}}{T}t_{e_{M-1}}\right) + \overline{res_{0,M-1}[1]}. \quad (4.55)$$

The rest of the analytical analysis of Subsection 4.4.1 can be adapted in the same way and the final result, the hardware implementation summarized by the \mathbf{C} matrix (4.52), still holds. The K_{cds} closed-loop parameter becomes :

$$K_{cds} = M \sum_{\forall in} \delta(\omega_{in}). \quad (4.56)$$

4.4.3 Conditions for Proper Operation

In despite of the generalization shown in Subsection 4.4.2, from a top-level point of view of the DDSS, input signal restrictions for $x(t)$ can be established for the DDSS to work correctly.

First Condition for Proper Operation

From (4.5), a negative feedback loop must be guaranteed for the DDSS to work properly. From (4.44), we observe that the sign of K_{csd} depends on $\delta(\omega_{in})$ or, in the case of a multiple sinusoidal input signal, $K_{c ds} = M \sum_{\forall in} \delta(\omega_{in})$. So, in general, the first condition for proper operation is

$$\sum_{\forall in} \delta(\omega_{in}) < 0. \quad (4.57)$$

Concerning $\delta(\omega_{in})$, from (4.35), fig. 4.18 illustrates the establishment of a nega-

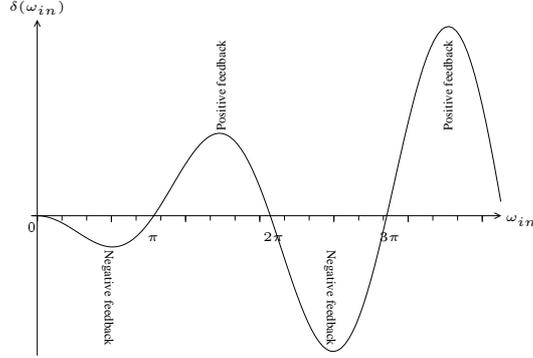


Figure 4.18: Illustration of the first condition for proper operation.

tive feedback loop as a function of ω_{in} . Specifically, $\delta(\omega_{in}) < 0$ if $|\omega_{in}| < \pi$. As a result, if $x(t)$ is a non-null bandlimited signal that verifies

$$X\left(\frac{\omega}{T}\right) = 0, \text{ if } |\omega| \geq \pi, \quad (4.58)$$

it can be unequivocally established a negative feedback loop. But $x(t)$ must not necessarily be a bandlimited signal to verify (4.57).

Second Condition for Proper Operation

For a bandlimited input signal as in (4.58), it must also verify

$$\int_{-\pi}^{\pi} \sum_{l=1}^{M-1} \Re \left\{ C_i^*[l] \hat{X}\left(\frac{\omega}{T}\right) \hat{X}\left(\frac{2\pi}{MT}l - \frac{\omega}{T}\right) e^{j\omega} \right\} d\omega = 0, \quad (4.59)$$

$$\forall t_{e_i}, \text{ for } 1 \leq i \leq M-1,$$

where $\Re\{\cdot\}$ denotes the real part of the argument, $\{\cdot\}^*$ denotes complex conjugation, $\hat{X}(\omega/T)$ is defined as

$$\hat{X}\left(\frac{\omega}{T}\right) = S_0(\omega)X\left(\frac{\omega}{T}\right), \quad (4.60)$$

being $S_0(\omega)$ defined as

$$S_0(\omega) = \frac{1}{M} \sum_{i=0}^{M-1} e^{j\omega \frac{te_i}{T}}, \quad (4.61)$$

and $C_i[l]$ is the l -th element of the DFT of $c_i[n]$.

If $x(t)$ does not meet (4.59), the accumulators of the DDSS become saturated even when clock-skews are null, preventing a correct operation. It is derived from a frequency domain point of view in the following paragraphs.

Due to the periodic nature of $c_{iP}[n]$, we can rewrite it as :

$$c_{iP}[n] = \sum_{l=0}^{M-1} C_i[l] e^{j \frac{2\pi}{M} ln}, \quad (4.62)$$

Note that $c_i[n]$ is just one period of $c_{iP}[n]$. From (4.52), it can be easily verified that $C_{iP}[0] = 0 \forall i$. So, in general, the spectrum of $c_{iP}[n]$ is :

$$C_{iP}(e^{j\omega}) = 2\pi \sum_{k=-\infty}^{\infty} \sum_{l=1}^{M-1} C_i[l] \delta \left(\omega - \frac{2\pi}{M} l - 2\pi k \right). \quad (4.63)$$

Let $w_i[n]$ be

$$w_i[n] = y[n-1] \cdot c_{iP}[n-1], \quad (4.64)$$

as shown in fig. 4.16. From (4.63) and (4.64), by the modulation property of the discrete-time Fourier transform, $W_i(e^{j\omega})$ is :

$$W_i(e^{j\omega}) = \sum_{l=1}^{M-1} C_i[l] Y \left(e^{j(\omega - \frac{2\pi}{M} l)} \right) e^{-j\omega}. \quad (4.65)$$

The i -th accumulator senses the DC component of the signal $z_i[n]$, defined as

$$z_i[n] = y[n] \cdot w_i[n]. \quad (4.66)$$

If there are no clock-skews, the sensed DC component must be equal to zero, otherwise the accumulator become saturated even when clock-skews are zero as a result of the non-zero value of $\overline{res_{tot_i}}$, preventing a correct operation. Analytically, this condition can be written as :

$$\begin{aligned} Z_i(e^{j0}) &= \frac{1}{2\pi} \int_{-\pi}^{2\pi} Y(e^{j\lambda}) W_i(e^{j(\omega-\lambda)}) d\lambda \Big|_{\omega=0} \\ &= \frac{1}{2\pi} \int_{-\pi}^{\pi} Y(e^{j\lambda}) W_i(e^{-j\lambda}) d\lambda = 0 \end{aligned} \quad (4.67)$$

From (2.22),

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{\infty} S_k(\omega) X \left(\frac{\omega}{T} - \frac{2\pi}{MT} k \right),$$

where

$$S_k(\omega) = \frac{1}{M} \sum_{i=0}^{M-1} e^{j(\omega - \frac{2\pi}{M} k) \frac{te_i}{T}} e^{-j \frac{2\pi}{M} ik}.$$

In absence of any clock-skew, according to (2.24),

$$S_k(\omega) = \begin{cases} 1 & \text{for } k = Ml, l \in \mathbb{Z} \\ 0 & \text{for all other } k, \end{cases}$$

i.e., only the alias signals associated to $k = Ml, l \in \mathbb{Z}$ are present in (2.22). So, from (4.40) evaluated for $t_{e_i} = 0$, i.e.,

$$\begin{aligned} \overline{res_{tot_i}} &= \\ (M-i) \sum_{q=1}^i r_{\hat{\alpha}_q \hat{\alpha}_{q-1}}[0] - i \sum_{q=i+1}^{M-1} r_{\hat{\alpha}_q \hat{\alpha}_{q-1}}[0] - i r_{\hat{\alpha}_0 \hat{\alpha}_{M-1}}[1], \\ &\text{for } 1 \leq i \leq M-1, \end{aligned}$$

and from (2.24), we known that the alias of the input signal at the origin of $\overline{res_{tot_i}}$ are those associated to $k = Ml, l \in \mathbb{Z}$. This deduction will be used later.

According to (2.24), (2.22) simplifies to

$$Y(e^{j\omega}) = \frac{1}{T} \sum_{k=-\infty}^{\infty} X\left(\frac{\omega}{T} - \frac{2\pi}{T}k\right). \quad (4.68)$$

If $x(t)$ is a bandlimited signal then, in the integration interval $[-\pi, +\pi]$ defined in (4.67), $Y(e^{j\omega})$ can be substituted in (4.67) by the following alias of $X\left(\frac{\omega}{T}\right)$:

$$Y(e^{j\omega})|_{-\pi < \omega < \pi} = \frac{1}{T} X\left(\frac{\omega}{T}\right). \quad (4.69)$$

The same can be done with $W_i(e^{j\omega})$:

$$\begin{aligned} W_i(e^{j\omega})|_{-\pi < \omega < \pi} &= \\ \frac{1}{T} \sum_{l=1}^{M-1} C_i[l] \left[X\left(\frac{\omega}{T} - \frac{2\pi}{MT}l\right) + X\left(\frac{\omega}{T} + \frac{2\pi}{MT}(M-l)\right) \right] e^{-j\omega}. \end{aligned} \quad (4.70)$$

From (4.70) and (4.69), (4.67) can be rewritten to obtain

$$\int_{-\pi}^{\pi} \sum_{l=1}^{M-1} \Re \left\{ C_i^*[l] X\left(\frac{\omega}{T}\right) X\left(\frac{2\pi}{MT}l - \frac{\omega}{T}\right) e^{j\omega} \right\} d\omega = 0, \quad (4.71)$$

for $t_{e_i} = 0, 1 \leq i \leq M-1$.

These properties of reals signals have been applied to derive (4.71):

$$X\left(\frac{\omega}{T}\right) = X^*\left(-\frac{\omega}{T}\right), \quad (4.72)$$

and

$$C_i[l] = C_i^*[M-l]. \quad (4.73)$$

The condition summarized by (4.71) is a necessary but not a sufficient condition. In fact, it guarantees that

$$\overline{res_{tot_i}} = 0, \quad (4.74)$$

for $t_{e_i} = 0, 1 \leq i \leq M-1$. However, as suggested by the expressions of $\overline{res_{i,i-1}[0]}$ and $\overline{res_{0,M-1}[1]}$ derived in Appendix D, it may happen that a particular signal verifies (4.74) for $t_{e_i} = 0, 1 \leq i \leq M-1$, but not for other t_{e_i} . To establish a necessary and sufficient condition, (4.74) must be verified in the presence of any clock-skew. This is derived in the next paragraph.

Recall that the alias of the input signal at the origin of $\overline{res_{tot_i}}$ are those associated to $k = Ml, l \in \mathbb{Z}$. In the presence of non-zero clock-skews, from (2.22), these alias are weighted by $S_0(\omega)$, a function of $t_{e_i}, 1 \leq i \leq M-1$. Because of this, we reformulate the condition (4.67) as :

$$\int_{-\pi}^{\pi} \widehat{Y}(e^{j\lambda}) \widehat{W}_i(e^{-j\lambda}) d\lambda = 0 \quad (4.75)$$

where, from (4.69),

$$\widehat{Y}(e^{j\omega}) \Big|_{-\pi < \omega < \pi} = \frac{1}{T} \widehat{X}\left(\frac{\omega}{T}\right), \quad (4.76)$$

being

$$\widehat{X}\left(\frac{\omega}{T}\right) = S_0(\omega) X\left(\frac{\omega}{T}\right), \quad (4.77)$$

and, from (4.70),

$$\widehat{W}_i(e^{j\omega}) \Big|_{-\pi < \omega < \pi} = \frac{1}{T} \sum_{l=1}^{M-1} C_i[l] \left[\widehat{X}\left(\frac{\omega}{T} - \frac{2\pi}{MT}l\right) + \widehat{X}\left(\frac{\omega}{T} + \frac{2\pi}{MT}(M-l)\right) \right] e^{-j\omega}. \quad (4.78)$$

Finally, (4.75) gives (4.59), i.e.,

$$\int_{-\pi}^{\pi} \sum_{l=1}^{M-1} \Re \left\{ C_i^*[l] \widehat{X}\left(\frac{\omega}{T}\right) \widehat{X}\left(\frac{2\pi}{MT}l - \frac{\omega}{T}\right) e^{j\omega} \right\} d\omega = 0,$$

$$\forall t_{e_i}, \text{ for } 1 \leq i \leq M-1.$$

4.4.4 Robustness of the DDSS

Robustness refers to the sensibility to fabrication dispersion. This measurement technique is implemented by digital circuit, so it does not suffer from dispersion itself. However, the gain and offset mismatch between channels of a time-interleaved ADC could interfere with the operation of this measurement technique. The following paragraphs show that this technique is not robust against these mismatches. Nevertheless, two solutions are proposed. These solutions allow the DDSS to correctly work even if gain and offset mismatch are present.

Robustness Against Offset and Gain Mismatch

For a clock-skew free time-interleaved ADC suffering from offset and gain mismatch, there is an equivalent input signal $x_{eq}(t)$ that provides the same discrete-time signal $y[n]$ in a completely ideal time-interleaved ADC. Fig. 4.19 illustrates it.

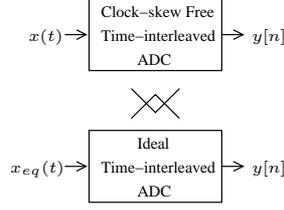


Figure 4.19: Illustration of the concept of the equivalent signal $x_{eq}(t)$.

For a zero clock-skew, $x_{eq}(t)$ must verify the necessary condition given in (4.71) for the DDSS to work properly, i.e.,

$$\int_{-\pi}^{\pi} \sum_{l=1}^{M-1} \Re \left\{ C_i^*[l] X_{eq} \left(\frac{\omega}{T} \right) X_{eq} \left(\frac{2\pi}{MT} l - \frac{\omega}{T} \right) e^{j\omega} \right\} d\omega = 0. \quad (4.79)$$

As shown in the following paragraphs, $x_{eq}(t)$ does not verify it.

Observing (2.10) and (2.15), $x_{eq}(t)$ can be written, in the frequency domain, as :

$$X_{eq} \left(\frac{\omega}{T} \right) = \quad (4.80)$$

$$\sum_{k=-(M-1)}^{M-1} G_k X \left(\frac{\omega}{T} - \frac{2\pi}{MT} k \right) \Pi_{\frac{\pi}{T}} \left(\frac{\omega}{T} \right) + \frac{2\pi}{T} \sum_{k=-\lfloor \frac{M}{2} \rfloor}^{\lfloor \frac{M}{2} \rfloor} \dot{O}_k \delta \left(\frac{\omega}{T} - \frac{2\pi}{MT} k \right),$$

where

$$\Pi_{\frac{\pi}{T}} \left(\frac{\omega}{T} \right) = \begin{cases} 1 & \text{for } -\frac{\pi}{T} \leq \frac{\omega}{T} \leq \frac{\pi}{T}, \\ 0 & \text{otherwise,} \end{cases} \quad (4.81)$$

and $\dot{O}_k = O_k$ except for M even and $\dot{O}_{\frac{M}{2}}$, being $\dot{O}_{\frac{M}{2}} = \frac{1}{2} O_{\frac{M}{2}}$.

Let us assume a zero $x(t)$ to specifically observe the effects of offset mismatch. Then, (4.79) gives

$$\sum_{l=1}^{M-1} \Re \left\{ C_i^*[l] \sum_{k=-\lfloor \frac{M}{2} \rfloor - l}^{\lfloor \frac{M}{2} \rfloor} \dot{O}_k \dot{O}_{-k+l} \cdot e^{j \frac{2\pi}{M} k} \right\} = 0. \quad (4.82)$$

This equality, that depends on the unknown values of O_k , is in general not verified, so this measurement technique is not robust against offset mismatch. However, for $M = 2$, (4.82) gives

$$\Re \left\{ C_i^*[1] \left(\dot{O}_0 \dot{O}_1 - \dot{O}_1 \dot{O}_0 \right) \right\} = 0. \quad (4.83)$$

The equality (4.83) is always verified. Since the offset mismatch terms are independent of clock-skews, it can be said that, for the $M = 2$ channel case, this measurement technique is robust against offset mismatch.

Now, let us assume all $O_k = 0$ to specifically observe the effects of gain mismatch. Consider a sinusoidal input signal,

$$X \left(\frac{\omega}{T} \right) = \frac{\pi}{T} e^{j \frac{\phi_{in}}{\omega_{in}} \omega} \left[\delta \left(\frac{\omega}{T} - \frac{\omega_{in}}{T} \right) + \delta \left(\frac{\omega}{T} + \frac{\omega_{in}}{T} \right) \right],$$

with $0 < \frac{\omega_{in}}{2\pi/M} < 1$ and M even to simplify the calculations. Then, (4.79) gives

$$\sum_{l=1}^{M-1} \Re \left\{ C_i^*[l] \left[\sum_{k=l-\frac{M}{2}+1}^{\frac{M}{2}-1} G_k G_{-k+l} \left(e^{j(\frac{2\pi}{M}k-\omega_{in})} + e^{j(\frac{2\pi}{M}k+\omega_{in})} \right) + \right. \right. \\ \left. \left. G_{1-\frac{M}{2}} G_{\frac{M}{2}} \cdot e^{j[\omega_{in}-\frac{2\pi}{M}(\frac{M}{2}-1)]} + G_{\frac{M}{2}} G_{1-\frac{M}{2}} \cdot e^{j(\pi-\omega_{in})} \right] \right\} = 0. \quad (4.84)$$

This equality, that depends on the unknown values of G_k , is in general not verified, so this measurement technique is not robust against gain mismatch. Interesting, for $M = 2$, (4.84) gives

$$\Re \left\{ C_i^*[1] \left(G_0 G_1 e^{j\omega_{in}} + G_1 G_0 e^{j(\pi-\omega_{in})} \right) \right\} = 0, \quad (4.85)$$

where $C_i[1]$, G_0 and G_1 are real numbers. The equality (4.85) is always verified. Although it is not done here, it can be shown that in general and even in the presence of clock-skew, for the $M = 2$ channels case, the left hand side of (4.40) remains exclusively a term proportionnal to t_{e_i} , being $\overline{res_{tot_i}}$ equal to zero, as long as (4.59) is verified. So it can be said that, for the $M = 2$ channel case, this measurement technique is robust against gain mismatch.

Offset Mismatch Insensitive DDSS

A slight modification in the diagram shown in fig. 4.17 can make the DDSS insensitive to offset mismatch. It is shown in fig. 4.20, where an offset mismatch

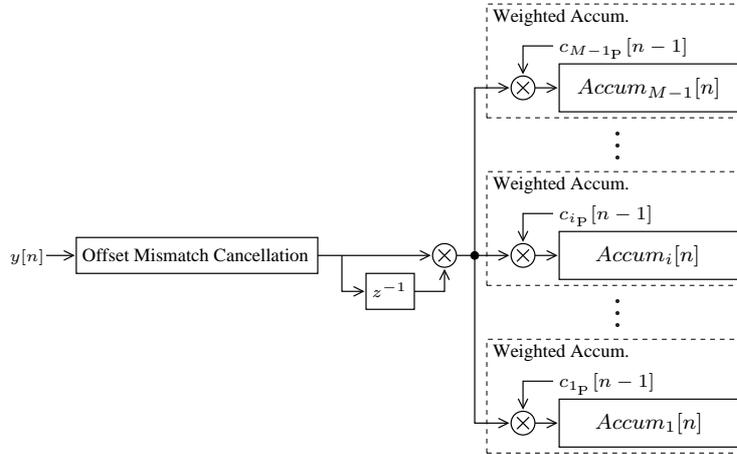


Figure 4.20: Diagram of an offset mismatch insensitive DDSS.

cancellation filter prevents the spectral components of $y[n]$ caused by offset mismatch from entering into the DDSS. The transfer function of this filter is

$$H_{OMC}(z) = 1 - z^{-M}, \quad (4.86)$$

where OMC stands for offset mismatch cancellation. $H_{OMC}(z)$ has a zero at each frequency where the spectrum components of $y[n]$ caused by offset mismatch appear.

Gain Mismatch Insensitive DDSS

As for offset mismatch, the measurement technique can become robust against gain mismatch with a slight alteration of the diagram shown in fig. 4.17. Intuitively, if only the sign of the input signal is to be used by the DDSS, the measured clock-skews will be insensitive to gain mismatch, because small gain variations do not change the sign of the sampled values. Fig. 4.21 shows the

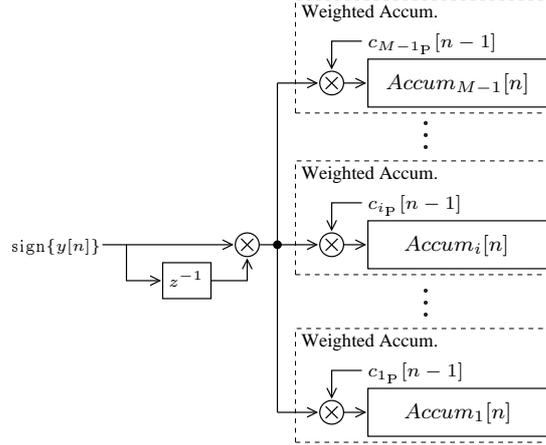


Figure 4.21: Diagram of a gain mismatch insensible DDSS.

resulting diagram of a gain mismatch insensitive DDSS. Only the MSB of $y[n]$ is used, i.e., its sign.

This modification prevents some of the assumptions made in Subsection 4.4.1 from holding. Nevertheless, the DDSS still works for a single sinusoidal input signal. It is shown in the following paragraphs.

Remarks on the DDSS Principle of Operation The modified DDSS is equivalent to the previous one preceded by a sign operation. This sign operation only changes the type of input signal that is injected to a non modified DDSS, so its operation remains the same as explained in Subsection 4.4.1. Fig. 4.22 illustrates the transformations of the input signal before entering the DDSS. For

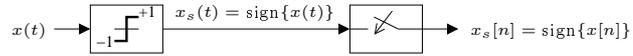


Figure 4.22: Sign and sampling operations.

example, for a sinusoidal input signal, $x_s(t)$ can be rewritten as [48] :

$$x_s(t) = \text{sign} \left\{ \cos \left(\frac{\omega_o}{T} t + \phi_o \right) \right\} = \sum_{r=1}^{\infty} A_r \cos \left(\frac{\omega_o}{T} r t + \phi_o \right), \quad (4.87)$$

where

$$A_r = \frac{2 \sin \left(\frac{\pi}{2} r \right)}{\pi r}. \quad (4.88)$$

Remarks on the Conditions for Proper Operation One obvious condition is that the sign of $x(t)$ must change at any t , otherwise the DDSS cannot work. From this affirmation, it seems clear that the modified DDSS works only for a restricted kind of input signals. That is why we limit our analysis at the single sinusoidal input signal case.

The $x_s(t)$ signal in (4.87) is a multiple sinusoidal signal of infinite bandwidth. Fortunately, from (4.88), the value of A_1 is higher than the values of the other A_r . We have numerically observed that if ω_o verifies $0 < \omega_o < \pi$, the first condition for proper operation, summarized by (4.57), is also verified, i.e., the signal components associated to other frequencies do not prevent the DDSS from working correctly. From an analytical point of view, the expression that gives us this result is not compact for the general case, and because of this it is not reproduced here.

Since $x_s(t)$ is not a bandlimited signal, the second condition for proper operation, as it is shown in (4.59), cannot be used. Neglecting the signal components associated to A_r for $r \geq 2$ is a reasonable assumption to understand the principle of operation. On the other hand, these components can potentially saturate the accumulators, preventing the subsystem from correctly operating. This reasoning, the same used in Subsection 4.4.3, is again used in the following paragraphs to derive a particular second condition for proper operation on the input signal frequency ω_o .

From Subsection 4.4.3, the equality (4.75),

$$\int^{2\pi} \widehat{Y}(e^{j\lambda}) \widehat{W}_i(e^{-j\lambda}) d\lambda = 0,$$

must be verified, where

$$\widehat{Y}(e^{j\omega}) = \quad (4.89)$$

$$S_0(\omega) \sum_{k=-\infty}^{\infty} \sum_{r=1}^{\infty} A_r \pi [e^{-j\phi_o} \delta(\omega - \omega_o r - 2\pi k) + e^{j\phi_o} \delta(\omega + \omega_o r - 2\pi k)].$$

and

$$\begin{aligned} \widehat{W}_i(e^{j\omega}) = \\ S_0(\omega) \sum_{k=-\infty}^{\infty} \sum_{r=1}^{\infty} \sum_{l=1}^{M-1} C_i[l] A_r \pi \left[e^{-j\phi_o} \delta\left(\omega - \omega_o r - 2\pi \frac{Mk+l}{M}\right) + \right. \\ \left. e^{j\phi_o} \delta\left(\omega + \omega_o r - 2\pi \frac{Mk+l}{M}\right) \right] e^{-j\omega}. \end{aligned} \quad (4.90)$$

Since $\widehat{Y}(e^{j\omega})$ and $\widehat{W}_i(e^{j\omega})$ are periodic signals with period 2π , if

$$\int_{-\infty}^{\infty} \widehat{Y}(e^{j\lambda}) \widehat{W}_i(e^{-j\lambda}) d\lambda = 0, \quad (4.91)$$

then (4.75) is verified. If all the arguments of $\delta(\cdot)$ in (4.89) and (4.90) are different, then (4.91) is true. This happens for

$$\omega_o \neq 2\pi \frac{(Mk+l)}{2rM}, \quad 1 \leq l \leq M-1, \quad k \text{ and } r \in \mathbb{Z}. \quad (4.92)$$

In practice, with real signals, if the input signal and the sampling frequency are independently generated, $\omega_o/2\pi$ is an irrational number, so (4.92) is verified.

Remarks on the Hardware of the DDSS A collateral consequence of using only the MSB of $y[n]$ it that the hardware of the adders and multipliers of the DDSS will be greatly simplified. On the other hand, this modification increases the variance of the accumulated values in the steady state, so a lower μ must be used in the feedback loop.

4.4.5 Interface with the DCDEs

As shown in Section 4.2, $DCW_i[m] = \lfloor \mu \cdot Accum_i[Mm] \rfloor$, where μ is some negative power of two, i.e., only some of the MSBs of $Accum_i[n]$ are used by the DCDE. The most efficient way of physically represent $Accum_i[n]$ is by using some binary weighted code, e.g., two's complement. However, as explained in 4.3.3, $DCW_i[m]$ is applied by the DCDE using a thermometer code. Because of that, an interface is needed between the DDSS and the DCDEs. Fig. 4.23 graphically represents it. A parallel-to-serial converter (denoted P-to-S) is used

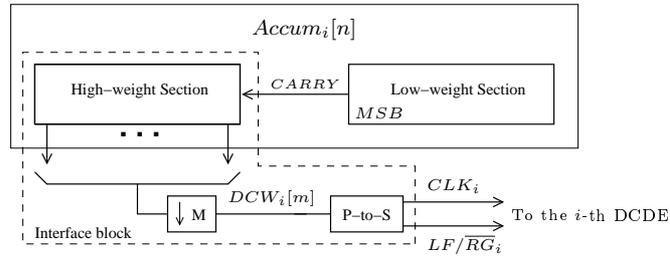


Figure 4.23: Diagram of the interface between the DDSS and the DCDE.

to generate CLK_i and LF/\overline{RG}_i . The *low-to-high* transitions of CLK_i indicate if a modification in the high-weight section of $Accum_i[n]$ has happened. If it is the case, the shift register used in the i -th DCDE must be updated. The level of LF/\overline{RG}_i indicates the shift sense, increasing (level *low*) or decreasing (level *high*) by one unity the stored value associated to $DCW_i[m]$.

As suggested by the dashed block in fig. 4.23, the interface operation can be thought as the downsampled parallel-to-serial conversion of the information provided by the carry bit and the MSB of the low-weight section of $Accum_i[n]$. In practice, it is not necessary to physically implement the high-weight section of $Accum_i[n]$ in the DDSS, because the shift register in the DCDE stores the same information. This simplifies the required hardware.

From now on, the low-weight section of $Accum_i[n]$ is simply called the accumulator. Note that this accumulator operates in a cyclic fashion, i.e., once the accumulator output has reached the highest binary word that can be stored, the immediately superior one is the lowest binary word, and *vice versa*.

To explain the principle of operation of the downsampled parallel-to-serial conversion, let us introduce the concepts of positive threshold crossings, negative threshold crossings (respectively denoted $+tx$ and $-tx$ and illustrated in fig. 4.24), and effective threshold crossings after M samples, denoted effective tx . A $+tx$ is the transition from an accumulator output inferior or equal to the highest binary word to one superior or equal to the the lowest binary

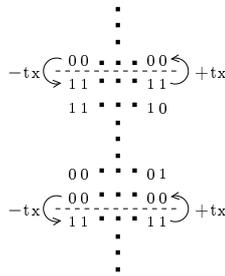


Figure 4.24: Illustration of the positive and negative threshold crossing concepts.

word. Reciprocally, a $-tx$ is the transition from an accumulator output superior or equal to the lowest binary word to one inferior or equal to the the highest binary word. The effective tx calculation after M samples carries out the downsampling operation between the DDSS and the DCDE. This is computed as follows : each time that a $+tx$ happens (i.e., the *CARRY* signal is *high* and *MSB* is *low*), a threshold crossing counter (from now on, tx counter) is increased one unity. On the other hand, each time that a $-tx$ happens, (i.e., the *CARRY* signal is *high* and *MSB* is *high*), tx counter is decreased one unity. After M samples, the effective tx is set to the resulting tx counter and the latter is reseted. Fig. 4.25 shows an example of timing of the interface for a $M = 2$

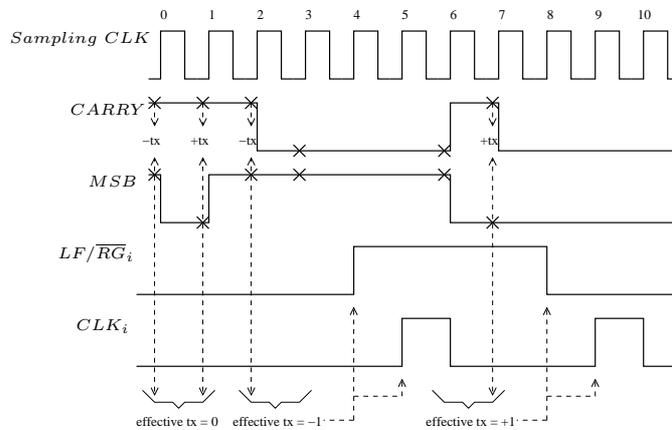


Figure 4.25: Example of timing of the interface between the DDSS and the DCDE for a $M = 2$ channel case.

channel case. A VHDL [1] code source describing a process with this behavior is shown in Appendix G. In our actual implementation, if effective $tx = 1$, then first LF/\overline{RG}_i is set to *low* and a sampling period later CLK_i performs a *low-to-high* transition. If effective $tx = -1$, then first LF/\overline{RG}_i is set to *high* and second, a sampling period later, CLK_i performs a *low-to-high* transition. Another particularity of our implementation is that the accumulator size is sufficiently large for the maximum absolute value of effective tx to be equal to one unity. It guarantees a maximum CLK_i transmission rate of only f_s/M .

4.5 Conclusion

A clock-skew calibration technique has been proposed in this Chapter. This technique can be classified into the category of mixed-signal techniques because of the analog nature of the correction technique and the digital nature of the measurement technique. In the following paragraphs the main features of both techniques are summarized reviewing the characteristics presented in Section 3.5.

4.5.1 Proposed Correction Technique

Here there is a commented list of its characteristics, summarized in table 4.1 together with the correction techniques shown in Section 3.4 :

- **Complexity** The complexity of the DCDEs depends on the multi-phase clock generator. In this work, M differential clock signals are extracted from a ring oscillator. From this assumption, $M - 1$ DTSECs are used to convert the clock signals from a differential format to a single-ended one and, at the same time, modify the added delay during the conversion. It is simpler than the adjustable delay cell used in Wu and Black's work. Moreover, due to the differential nature of the clock generator, M DTSECs are necessary even if no clock-skew calibration is done. So up to now, there is no extra hardware added. Next, $M - 1$ DTBG are needed. A DTBG is mainly composed of a linear current-to-voltage converter and correction cells. The area required by the former depends on the chosen architecture and technology. The area required by the latter depends on DR and the area per correction cell. In turn, on one hand, DR depends on the clock-skew correction range and the maximum uncorrected clock-skew tolerated after calibration, as shown in (4.23),

$$DR = \frac{\max\{t_{e_i}\} - \min\{t_{e_i}\}}{t_{step}}.$$

And on the other hand, the area per correction cell depends on technology. This parameter is used and found for a given technology in Chapter 5.

- **Robustness** Each DCDE is embedded in an independent closed-loop. Its feedback path is done in the digital domain, after sampling. It means that the consequences in terms of clock-skew of any dispersion both on the DCDE and on all the sampling clock path up to the sampling switch are merged in the global clock-skew that is to be corrected. It is an advantage over other calibration systems. For example, in [74], the detection is done neglecting the clock-skew introduced by the sampling switches and the DCDE itself.

On the other hand, special attention has been paid to keep as constant as possible t_{step} all over the clock-skew correction range, even if dispersion is present. From (4.11),

$$|t_{res_i}[m]| \leq t_{step},$$

so a constant t_{step} allows to precisely know the maximum uncorrected clock-skew $t_{res_i}[m]$. Design guidelines to limit and determine the t_{step} dispersion have been shown.

- **Input Restrictions** The DCDEs act directly over the sampling instants, so there is no input signal restrictions. It is in contrast with the digital correction techniques, where some kind of bandwidth limitation of the input signal is always present. Since the correction does not concern neither the input signal nor the digitalized samples, it can be said that there is no such a kind of limitation when using this correction technique.
- **Allowable M** This correction technique is appropriate for any number of time-interleaved channels.

	Complexity	Robustness	Input Restrictions	Allowable M
Author's	Low ^a	Yes	No	Any
Jamal <i>et al.</i> 's	High	Yes	Yes	2
Jin and Lee's	High	Yes	Yes	Any
Wu and Black's	Low	No	No	Any

Table 4.1: Characteristics of the studied correction techniques.

^aOnly a qualitative appreciation is given here. For details, see Chapter 5.

4.5.2 Proposed Measurement Technique

Here there is a commented list of its characteristics, summarized in table 4.2 together with the measurement techniques shown in Section 3.4 :

- **Complexity** Fig. 4.20 shows the basic digital blocs needed by a DDSS robust against offset mismatch. Let us enumerate it :
 - M delay cells and one adder at rate f_s for the offset mismatch cancellation filter.
 - One delay cell and one multiplier at rate f_s .
 - $M - 1$ weighted accumulators at rate f_s . The actual complexity of the weighted accumulator depends on M , being the $M = 2$ case the simplest. Note that just one weighted accumulator, with a modifiable $c_{iP}[n]$ sequence, will be used if the clock-skew calibrations are not to be performed simultaneously.

Finally, note that a DDSS robust against gain mismatch uses only the sign bit of $y[n]$. If this is the case, the complexity of the multipliers, filters and delay cells is greatly reduced. So, in comparison with the measurement technique proposed in [27], our technique is simpler.

- **Robustness** This measurement technique is implemented as a digital circuit, so it does not suffer from dispersion itself. Unfortunately, the presence of gain and offset mismatch prevent the DDSS from working properly.

To avoid this limitation, Section 4.4.4 contributes slight modifications to the basic DDSS that make it insensible to gain and offset mismatch. It means that even in the presence of these mismatches, the modified DDSS could be used to calibrate the sampling instants.

- **Input Restrictions** As described in Subsection 4.4.3, a negative feedback loop must be guaranteed for the DDSS to work properly. It depends on the analog input signal $x(t)$ and it is summarized by (4.57),

$$\sum_{\forall in} \delta(\omega_{in}) < 0.$$

Moreover, $x(t)$ must also verify (4.59),

$$\int_{-\pi}^{\pi} \sum_{l=1}^{M-1} \Re \left\{ C_i^*[l] \hat{X} \left(\frac{\omega}{T} \right) \hat{X} \left(\frac{2\pi}{MT} l - \frac{\omega}{T} \right) e^{j\omega} \right\} d\omega = 0,$$

$$\forall t_{e_i}, \text{ for } 1 \leq i \leq M - 1,$$

for the DDSS to work properly. If $x(t)$ does not meet this condition, the accumulators of the DDSS become saturated even when clock-skews are null, preventing a correct detection. This is a very restrictive input signal condition. For example, if $x(t)$ are composed of two sinusoidal input signals at normalized frequencies ω_A et ω_B , in general the DDSS cannot properly work if any of the following equalities is true :

$$2\omega_A M = 2\pi k \text{ or,} \quad (4.93a)$$

$$2\omega_B M = 2\pi k \text{ or,} \quad (4.93b)$$

$$(\omega_A + \omega_B) M = 2\pi k \text{ or,} \quad (4.93c)$$

$$(\omega_A - \omega_B) M = 2\pi k . \quad (4.93d)$$

- **Type of Calibration** As a consequence of the input signal restrictions and for a general case of input signal during normal operation, this technique should be used as a foreground calibration. It means that once the steady state has been reached in a hypothetical calibration cycle, the DDSS must be freezed during the normal operation cycle.
- **Test Signal** This measurement technique measures mismatches of the input signal paths between the channels. So an externally generated signal must be used to perform the calibration. The input restrictions allow us to use a not carefully generated signal, e.g., any periodic square signal at an oscillation frequency independent of the sampling frequency.
- **Allowable M** This measurement technique is appropriate for any number of time-interleaved channels.

Interesting, for the $M = 2$ channels case, the scheme shown in fig. 4.17 coincides with the proposed DDSS in [27], when using a delay cell instead of a Hilbert filter. In fact, the authors of [27] develop their algorithm from a spectral point of view, as shown in Appendix B.2.1. On the other hand, we have independently developed our algorithm from a correlation based point of

	Complexity	Robustness	Input Restrictions	Type of Measurement	Test Signal	Allowable M
Author's	(Very) Low	Yes	Yes	Foreground ^a	No ^b	Any
Jamal <i>et al.</i> 's	Low	Yes	Yes	Foreground ^a	No ^b	2
Jin and Lee's	High	No	Yes	Foreground ^a	Yes	Any
Wu and Black's	High	No	No	Background	No	Any

Table 4.2: Characteristics of the studied measurement techniques.

^a It is *Foreground* as long as the input restrictions are not verified.

^b An input signal is needed, but not necessarily internally and carefully generated.

view. The advantage of the correlation based analysis is that finding the general solution is a straightforward matter. The input signal condition (3.5)

$$\left| X\left(\frac{\omega}{T}\right) X\left(\frac{\pi}{T} - \frac{\omega}{T}\right) \right| = 0.$$

derived in [28] for the $M = 2$ channels case is similar⁶ to our general condition (4.59) when it is particularized for $M = 2$, in absence of any clock-skew :

$$\int_{-\pi}^{\pi} \Re \left\{ X\left(\frac{\omega}{T}\right) X\left(\frac{\pi}{T} - \frac{\omega}{T}\right) e^{j\omega} \right\} d\omega = 0,$$

We have partially published this multiple channel clock-skew detector first in [4] and it has been further developed in [5]. There is even a third similar work [17]. This one uses the same correlation based point of view used in our work. However, the hardware implementation is not clearly exposed and the input signal conditions for proper operation are not totally established.

⁶The input signal condition (3.5) is not correct. For example, it does not predict the gain and offset mismatch robustness of this measurement technique for the $M = 2$ channels case (see Appendix B.2.3). On the contrary, according to (3.5), this measurement technique is not robust.

Chapter 5

Description of the Demonstrator

5.1 Introduction

The mixed-signal clock-skew calibration technique explained in Chapter 4 is mainly aimed at system-on-a-chip (SoC) circuits. In our case, this means at least a fully-integrated time-interleaved ADCs. However, due to a lack of time, we have only designed and fabricated the clock generator subsystem. In order to verify in a real environment this technique, we use a demonstrator made from an integrated custom-built clock generator in a $0.35\mu\text{m}$ AMS¹ CMOS technology and other discrete commercial components described in Section 5.2 and 5.4. The operation of the demonstrator is described in Section 5.3.

5.2 Components of the Demonstrator

A block diagram of this demonstrator is shown in fig. 5.1. DTCG stands for digitally trimmable clock generator. This circuit and four commercial ADCs are welded on a test board. This board is connected to a commercial field programmable gate array (FPGA) placed on a development board. A signal generator injects the same input signal to the four ADCs. Additionally, an IBM PC² compatible, denoted simply PC, can be connected to the FPGA for measurement and displaying purposes.

Strictly speaking, the last two components are not part of the demonstrator.

Due to the specificity of the DCDE, no commercial circuit can be used to test this aspect of our calibration technique. A custom-built circuit, the DTCG, has been designed for it, putting together a multi-phase clock-generator and four DCDEs in a same chip. The implementation of both circuits are further discussed in Section 5.4.

On the other hand, a commercial FPGA, capable of implementing any moderately complex digital operation in real time, offers us the possibility of testing different functions and configurations of the DDSS. The FPGA used in our test

¹AMS stands for Austria Mikro Systeme

²IBM PC stands for International Business Machines Corporation personal computer

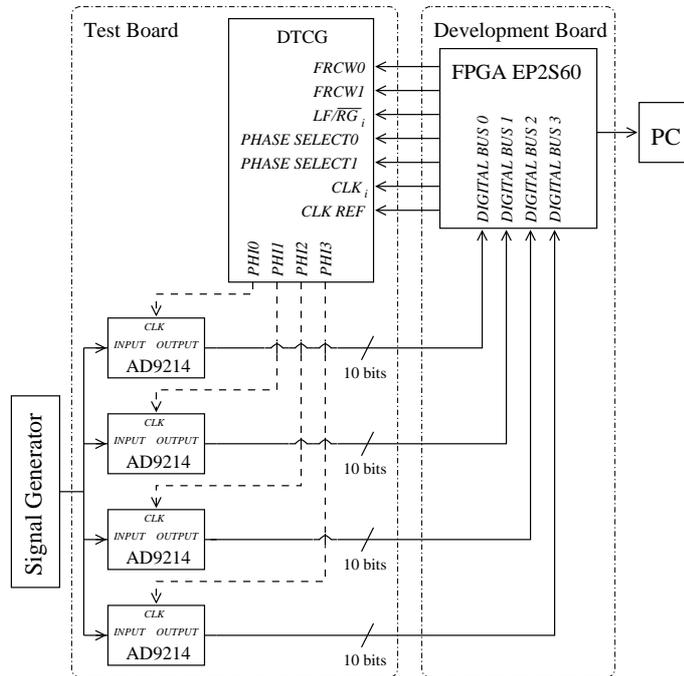


Figure 5.1: Diagram of the physical components of the demonstrator.

is a Stratix II EP2S60, in a Nios Development Board, Stratix II Edition [9]. The commercial ADCs are the AD9214 [12], 10 bits ADCs that can operate at a sampling rate up to 105 MHz.

5.3 Operation

Fig. 5.2 illustrates the operations that take place in each component of the demonstrator. In general terms, the signal is sampled by the ADCs, the sampled data is read, processed and stored in real time by the FPGA and the sampling instants are generated by a multi-phase clock generator implemented in the DTCG. Control signals generated by the FPGA can slightly advance or delay the sampling instants. Finally, the stored data can later be read by a PC station for FFT analysis and results plotting.

The frequency of the sampling clock signals is f_s/M . The value of f_s/M used during the tests is 25 MHz, hereafter referred to as f_s/M of interest.

The FPGA plays a main role in the calibration process as the master of the other components. To go into the operation details of the demonstrator, let us, first, briefly describe the input and output signals of the DTCG. Second, let us write and comment the algorithm executed by the FPGA using a pseudocode language.

5.3.1 Input and output signals of the DTCG

From fig. 5.1, the input and output signals of the DTCG are :

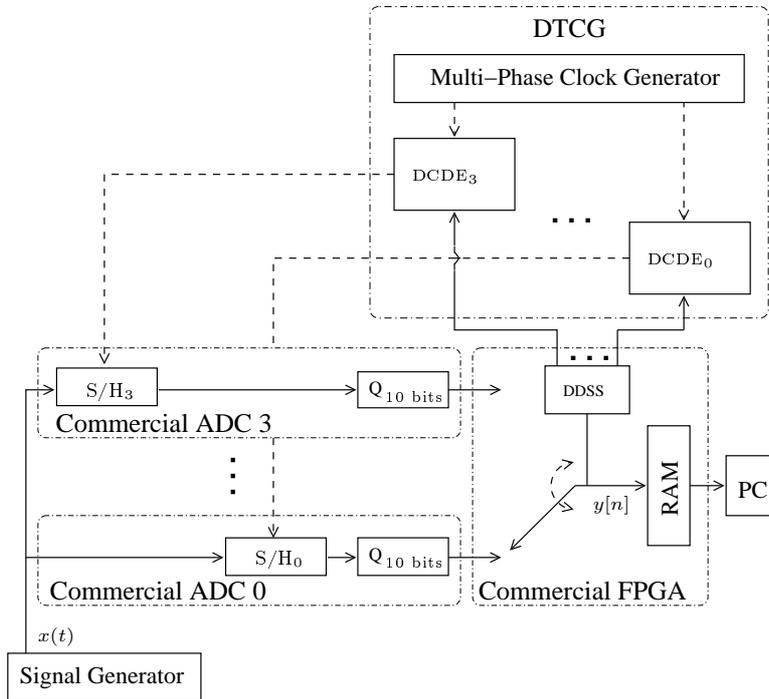


Figure 5.2: Functional diagram of the demonstrator.

- ***CLK REF*** This is reference clock signal used by the internal PLL of the DTCG.
- ***PHASE SELECT*** This is a two bits control signal that selects one of the four sampling clocks to be calibrated.
- ***CLK_i*** This is the clock signal used to operate the shift-register formed by the correction cells of the selected sampling clock.
- ***LF/RG_i*** This is a control signal that indicates which sense the selected shift-register changes in.
- ***FRCW*** This is a two bits control signal that selects one of the four available sizes of t_{step} (see Subsection 5.4.3).
- ***PHI0, ..., PHI3*** These are the four sampling clock signals.

5.3.2 Algorithm executed by the FPGA

From now on, verbatim font denotes pseudocode commands and `//` denotes comments in the code.

The subroutines to be sequentially executed are :

```
CALL step_size_selection
CALL resetting
CALL calibration
CALL pc_communication //optionally
```

The following paragraphs describe the first three subroutines.

step_size_selection The size of t_{step} is fixed at the beginning of the operation by means of the signal $FRCW$. It does not change through all the process. In pseudocode, we write :

```
SET FRCW //accordingly to the desired step size
```

reseting Reseting is initializing the digital values stored in the static memories of every correction cell to a known value. This operation must be performed independently for each sampling clock before calibration because the memories contains random values at the startup moment. No special circuitry has been added to the correction cells to perform this operation. This is a deliberate choice to keep their area as low as possible. Fig. 5.3 shows the state of the

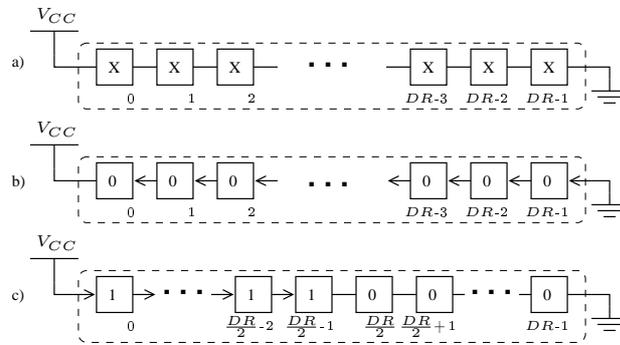


Figure 5.3: a) State of the static memories at the startup moment for a sampling clock. b) State at the end of the zeroing process. c) State at the end of resetting.

memories at three moments during the resetting process for the i -th sampling clock. X in fig. 5.3a denotes an unknown binary value. Fig. 5.3b shows the state of the memories at the end of a zeroing process. Once the state of all the memories is known, $DR/2$ memories are filled with *high* logic states. It sets $t_{cal_i}[m]$ at the middle of the clock-skew correction range.

In pseudocode, we write :

```
FOR each sampling clock //i.e. M sampling clocks
  //selecting a sampling clock
  SET PHASE_SELECT //accordingly to the sampling clock to be initialized
  //zeroing
  SET LF_RG_i="1"
  FOR each correction cell //i.e., DR correction cells
    create a low-to-high transition on CLK_i
  ENDFOR
  //filling with high logic states
  SET LF_RG_i="0"
  FOR half of the correction cells //i.e., DR/2
    create a low-to-high transition on CLK_i
  ENDFOR
ENDFOR
```

calibration The calibration algorithm is performed during a certain number of iterations, denoted $ITER_{limit}$ and called `iteration_limit` in the pseudocode. $ITER_{limit}$ must be great enough to allow the calibration algorithm to reach the steady state. Therefore, from Section 4.2, the necessary $ITER_{limit}$ depends on the value of t_{e_i} , K_{csd} , μ and t_{step} . In practice, for a known input signal frequency, a sufficiently great $ITER_{limit}$ is chosen so that the hypothetic highest t_{e_i} that is to be handled by the calibration system can be corrected. It can be determined by means of numerical simulations or simply by laboratory tests on the demonstrator.

Note that the calibration algorithm could be performed both simultaneously and sequentially for each sampling clock. Here, we execute it sequentially, requiring $(M - 1)ITER_{limit}$ iterations to fully calibrate the time-interleaved ADC.

In pseudocode, we write :

```

FOR each sampling clock to be corrected //i.e. M-1 sampling clocks
  //selecting a sampling clock
  SET PHASE_SELECT //accordingly to the sampling clock to be corrected
  //calibrating
  WHILE iteration_counter < iteration_limit
    generate a CLK_REF period
    read M samples from the M ADCs
    Update DCW_i
    IF there is a new DCW_i
      //updating the correction cells state
      SET LF_RG_i //accordingly to the new and precedent DCW_i
      create a low-to-high transition on CLK_i
    ENDIF
  ENDWHILE
ENDFOR

```

5.4 Digitally Trimmable Clock Generator

5.4.1 Overview

The DTCCG consists of a multi-phase clock generator and four DCDEs. It provides with four sampling clock signals nominally suitable for a $M = 4$ channels time-interleaved sampling. By means of digital trimming, the phases of the clock signals can be independently adjusted to compensate any fabrication dispersion. Fig. 5.4 shows a diagram of the elements of the DTCCG. The multi-phase clock generator consists of a voltage controlled ring oscillator embedded in a PLL. They are designed to operate in the frequency range between 12.5 MHz and 50 MHz. This multi-phase clock generator, also used in Wu and Black's work (see Subsection 3.4.2), has been first published in [39]. Some of its operation details are of interest in this work. They are discussed in Subsection 5.4.2. Subsection 5.4.3 is devoted to the physical implementation of the DCDEs.

and the $d\phi_i$ common mode signal $d\phi_{i_{CM}}$ as

$$d\phi_{i_{CM}} = \frac{d\phi_{i_p} + d\phi_{i_n}}{2}. \quad (5.2)$$

Equivalent definitions can be done from $d\phi_{o_p}$, $d\phi_{o_n}$, and from I_{res_p} , I_{res_n} . This delay cell gathers simplicity and good insensibility to supply variations together [10] [16]. The so-called symmetric load are two identically sized PMOS transistors. This is the key component to understand the principle of operation of these delay cells. Fig. 5.6 shows plots of a symmetric load I-V characteristics

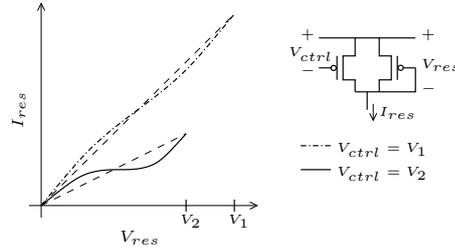


Figure 5.6: Plots of a symmetric load I-V characteristics at two different bias voltage V_{ctrl} .

at two different bias voltages V_{ctrl} . A variation in V_{ctrl} modifies the equivalent resistance of the symmetric load and hence, the added delay. Moreover, as long as V_{res} is inferior to V_{ctrl} , the first derivatives of these I-V characteristics are symmetric around $V_{ctrl}/2$.

If both $d\phi_{o_p}$ and $d\phi_{o_n}$ excursions verify

$$V_{cc} - V_{ctrl} < d\phi_{o_p} < V_{cc}, \quad (5.3a)$$

$$V_{cc} - V_{ctrl} < d\phi_{o_n} < V_{cc}, \quad (5.3b)$$

and

$$d\phi_{o_{CM}} = V_{cc} - V_{ctrl}/2, \quad (5.4)$$

the coupled noise in $d\phi_{i_{CM}}$ becomes just coupled noise in $d\phi_{o_{CM}}$ in a first order approximation [40]. It is illustrated in fig. 5.7, where it is assumed that the coupled noise in $d\phi_{i_{CM}}$ becomes coupled noise in $I_{res_{CM}}$. Since there is no common mode to differential conversion of noise, this noise does not become jitter.

In order to guarantee (5.3) and (5.4), a replica-feedback current source bias circuit is used to properly set V_{BN} for a given V_{ctrl} .

As drawbacks, the noise free $d\phi_{o_{CM}}$ depends on the required delay, and neither $d\phi_{o_p}$ nor $d\phi_{o_n}$ are rail-to-rail signals, but their excursion are limited according to (5.3).

Ring Oscillator Configuration

Our ring oscillator consist of four differential delay cells, even if only four of the available eight clock signals are used. These four differential delay cells, and not simply two, are needed for the ring oscillator to spontaneously oscillate [56]. A three differential delay cells configuration would allow us to demonstrate the

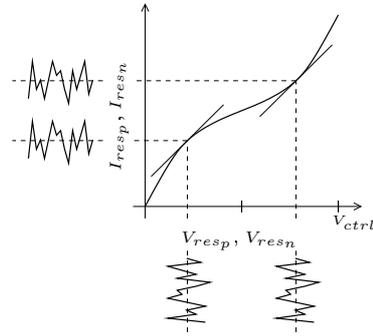


Figure 5.7: Illustration of the transformation of the coupled noise in $d\phi_{i_{CM}}$ into coupled noise in $d\phi_{o_{CM}}$.

operation for three and six single ADCs. This configuration is ruled out because the maximum number of ADCs that the development board can handle is four. We want to demonstrate the operation for at least two different configurations. So $M = 2$ and $M = 4$ are the only possibilities, which lead us to a four delay cells choice for the ring oscillator.

The control voltage that determines the oscillation frequency of the ring oscillator is V_{ctrl} . This oscillation frequency is f_s/M . As discussed in the paragraphs devoted to the differential delay cells, from (5.4), the value of $d\phi_{o_{CM}}$ depends on V_{ctrl} , so it also depends on f_s/M . In a ring structure, this is true indistinctly for $d\phi_{o_{CM}}$ and $d\phi_{i_{CM}}$. Fig. 5.8 shows the relation between f_s/M

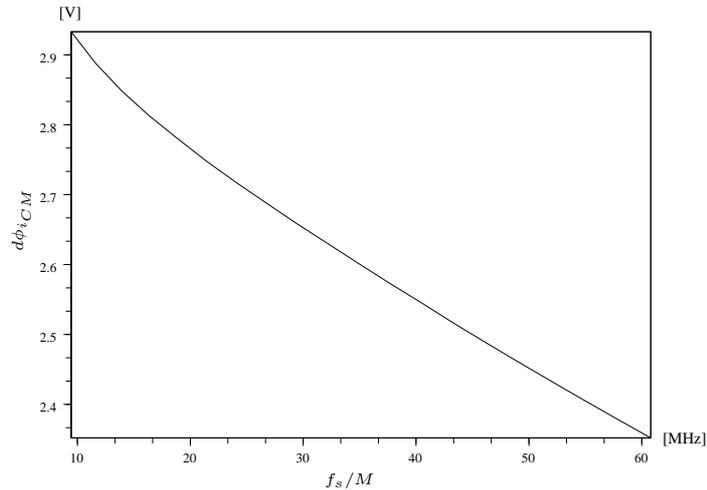


Figure 5.8: Plot of $d\phi_{i_{CM}}$ versus f_s/M .

and $d\phi_{i_{CM}}$ extracted from transient electrical simulations. This result will be used in Subsection 5.4.3.

PLL

The PLL provides us with a mean of minimizing the delay (deskewing) between $CLKREF$ and $PHI0$, making easy the overall synchronization task for the FPGA [75]. The same thing could have been done with a DLL. However, a PLL is preferred since the rms jitter associated at each sampling clock is the same due to the circular structure of the ring oscillator, while a DLL exhibits no equal rms jitter at the output of each delay cell.

The details of the PLL are out of the scope of this work. Let us simply signal that this is an analog self biased circuit, designed to be robust against supply noise.

5.4.3 Digitally Controlled Delay Element

Differential-To-Single Ended Converter

Fig. 5.9 shows the DTSEC, previously discussed in Subsection 4.3.2, for reading

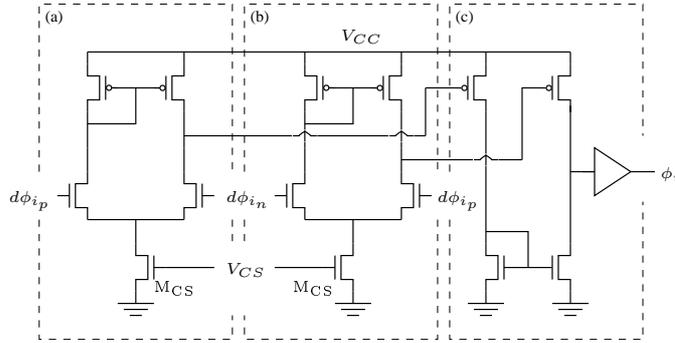


Figure 5.9: DTSEC and clock buffer.

convenience.

As we have explained in Subsection 5.4.2, the value of $d\phi_{i_{CM}}$ depends on the oscillation frequency of the ring oscillator, f_s/M . The operation point of the DTSEC depends on both V_{CS} and $d\phi_{i_{CM}}$. Any variation of these voltages can modify the expected voltage-to-time conversion factor SV and, hence, t_{step} . The following paragraphs and plots explain this phenomenon and show the expected values of SV for a f_s/M range between 12.5 MHz and 50 MHz and for V_{CS} equal or higher than 0.9 V.

Fig. 5.10 and 5.11 show the plot of *relative delay* versus V_{CS} for two different $d\phi_{i_{CM}}$ extracted from transient electrical simulations. The former plot is for $d\phi_{i_{CM}} = 2.4$ V, associated to $f_s/M = 50$ MHz. The latter plot is for $d\phi_{i_{CM}} = 2.8$ V, associated to $f_s/M = 12.5$ MHz. The slope of these graphs is the value of SV . From these plots we clearly observe the dependence of SV on V_{CS} . In principle, V_{CS} is set somewhat arbitrarily to be around 0.9 V. The lower the required V_{CS} variations, the more constant t_{step} is. As explained in Subsection 4.3.2, for V_{CS} voltages around values higher than 0.9 V, the expected t_{step} is expected to be lower.

Fig. 5.12 shows the plot of SV versus f_s/M , also extracted from transient electrical simulations, where SV has been calculated as the slope of *relative delay*

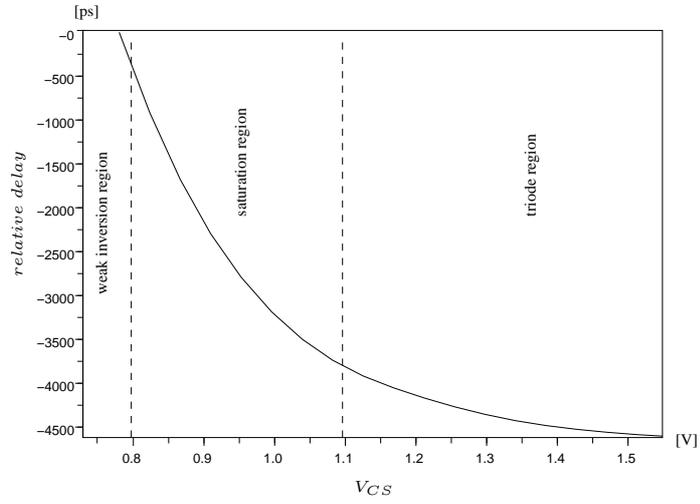


Figure 5.10: Plot of *relative delay* versus V_{CS} for a DTSEC and $d\phi_{i_{CM}} = 2.4$ V, $f_s/M = 50$ MHz.

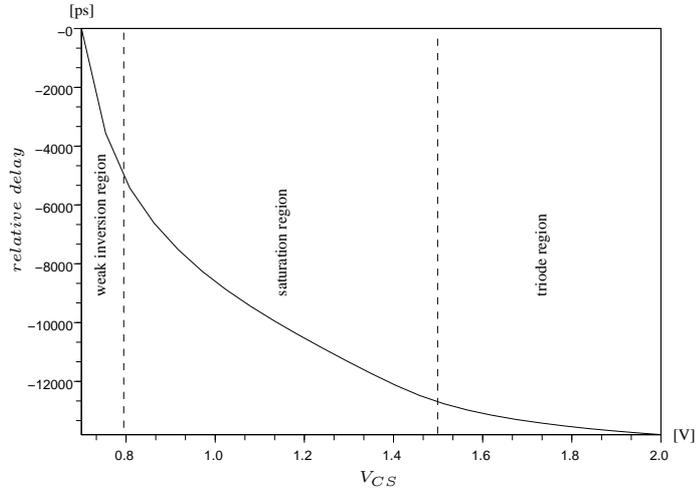


Figure 5.11: Plot of *relative delay* versus V_{CS} for a DTSEC and $d\phi_{i_{CM}} = 2.8$ V, $f_s/M = 12.5$ MHz.

for $V_{CS} = 0.9$ V. In the f_s/M range between 12.5 MHz and 50 MHz, SV takes values around -8 ns/V, with weak dependency on f_s/M or $d\phi_{i_{CM}}$. It means that, actually, the operation point is mainly set by V_{CS} . The results show in fig. 5.12 will be used in the following paragraphs to determine t_{step} at the f_s/M of interest around $V_{CS} = 0.9$ V.

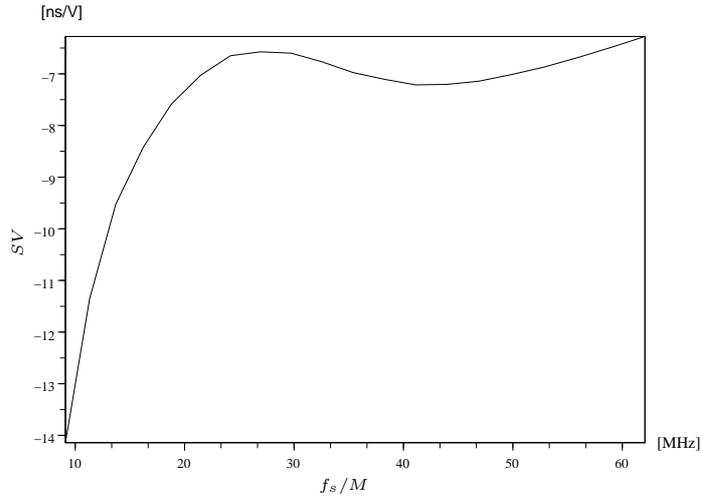


Figure 5.12: Plot of SV versus f_s/M .

Digitally Trimmable Bias Generator

The DTBG is mainly composed of digital circuits, except for the basic transistors, M_{BT} . Fig. 5.13 shows the diagram of one correction cell, previously

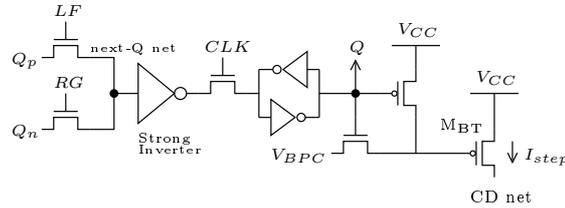


Figure 5.13: Diagram of one correction cell formed by a static storage cell, a basic transistor and control transistors.

discussed in Subsection 4.3.3, for reading convenience.

The dimensioning of M_{BT} must be done accordingly to the desired t_{step} dispersion. Here, for the sake of brevity, we neglect the dispersion in the current-to-voltage and the voltage-to-time conversion because they do not question the monotonicity of the overall digital-to-time conversion. We pay attention only to the dispersion of I_{step} . A careful designer must consider all the dispersion sources.

From (4.17) and (4.21), for a given relative t_{step} dispersion, denoted ϵ , the area of M_{BT} , $(W \cdot L)_{BT}$, must verify

$$(W \cdot L)_{BT} \geq \left(\frac{A_I}{\epsilon} \right)^2. \quad (5.5)$$

As shown in Appendix F, the short-distance relative drain current matching parameter A_I (in [m]) depends on the operation point of the basic transistor,

more specifically on V_{BPC} :

$$A_I \approx \sqrt{A_K^2 + \left(\frac{2A_{V_{TH_p}}}{V_{BPC} - V_{CC} - V_{TH_p}} \right)^2}, \quad (5.6)$$

being V_{TH_p} the p-channel saturation voltage threshold, A_K the short-distance matching parameter for the relative current gain factor (in [m]) and $A_{V_{TH_p}}$ the short-distance matching parameter for the PMOS threshold voltage (in [V·m]). The errors from the current gain factor and the threshold voltage are considered independent. Note that $V_{BPC} - V_{CC}$ is the gate-to-source voltage (V_{GS}) of M_{BT} . Intuitively, the lower $|V_{GS}|$, the more important the effects of the V_{TH_p} dispersion become.

On the other hand, for a transistor biased in saturation and for a given drain current I_{step} , the ratio $(W/L)_{BT}$ of this transistor also depends on V_{BPC} . If I_{step} is fixed to a very small value to minimize the power consumption, then it makes sense setting W to the minimum allowed by the technology, denoted W_{tech} . In this case, it is the value of L , and hence, the area of the transistors that depends on V_{BPC} :

$$(W_{tech} \cdot L)_{BT} = \frac{k_p W_{tech}^2 (V_{BPC} - V_{CC} - V_{TH_p})^2}{2I_{step}}, \quad (5.7)$$

where $k_p = \mu_p C_{ox}$, being μ_p the p-channel mobility of electrons.

According to the reasonings of the previous paragraph, fig. 5.14 shows the

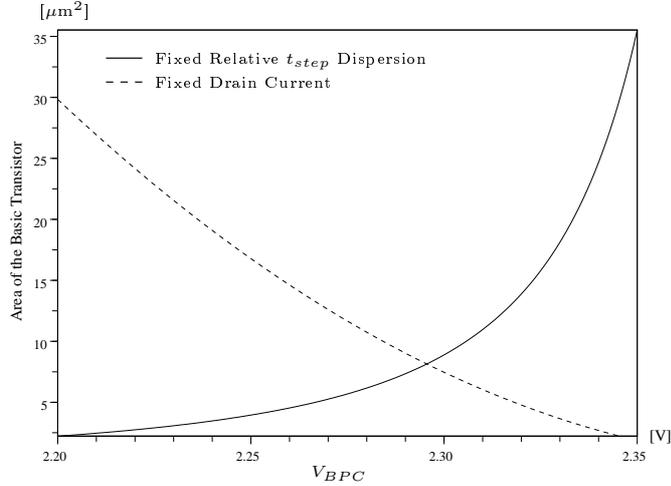


Figure 5.14: Plot of the area of the basic transistor versus V_{BPC} for a fixed relative t_{step} dispersion and a fixed drain current.

required area of M_{BT} for a fixed ϵ of 10% and a fixed I_{step} of 6.4 nA as a function of V_{BPC} . The crossing point determines the value of V_{BPC} , 2.3 V, and the area of the basic transistor, $7.2 \mu\text{m}^2$. The size of the basic transistor in a $W \times L$ format is $0.4 \mu\text{m} \times 17.9 \mu\text{m}$.

Fig. 5.15 shows the layout of one correction cell. The transistor on the right of the figure is the basic transistor. Due to its great length, it is designed as a

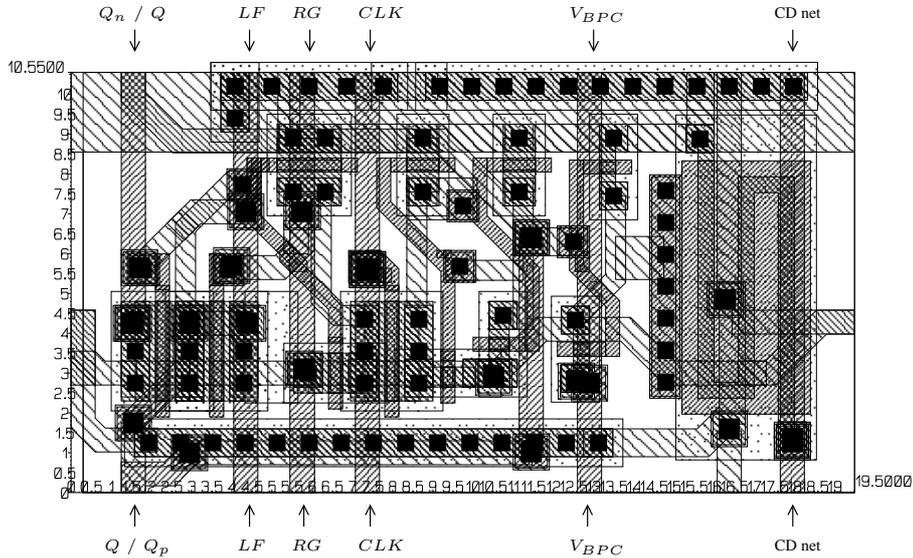


Figure 5.15: Layout of one correction cell.

snake-shaped transistor. All input and output signals are expressly placed over vertical axes. It greatly simplifies the connection task when doing the layout of *DR* correction cells. Moreover, by combining this layout and others rotated by 180 degrees, the layout of the entire shift register of correction cells can adopt any snake-shaped form. It can be useful to fill the remaining empty space in a layout, simplifying the placement task.

As shown in fig. 5.15, the area of one correction cell is $19.5 \times 10.55 \mu\text{m}^2$, i.e., $205.7 \mu\text{m}^2$.

The expected clock-skews in our test board are higher³ than in a SoC circuit. So the clock-skew correction range must be higher too and then, by virtue of (4.23),

$$DR = \frac{\max\{t_{e_i}\} - \min\{t_{e_i}\}}{t_{step}},$$

the number of necessary correction cells, *DR*, will also be higher. Fortunately, since we do not have any size restriction in our custom-built clock generator, we can use a t_{step} as small as that required in SoC circuits (according to Section 2.4, around 1 ps) while handling the typical clock-skews of our test board (around 500 ps). A sufficiently large *DR* is chosen : 1024 correction cells per sampling clock.

Fig. 5.16 shows the layout of the complete DTCG. Most of the area is occupied by four DTBGs (the *a* areas), while the others circuits (*b* for the PLL and ring oscillator and *c* for a bias voltage generator) are placed in the center occupying a

³From our observations, clock-skews are between one and two orders of magnitude (hundreds or thousands of picoseconds) higher than the measured clock-skews in previously published intergrated time-interleaved ADCs (tens of picoseconds).

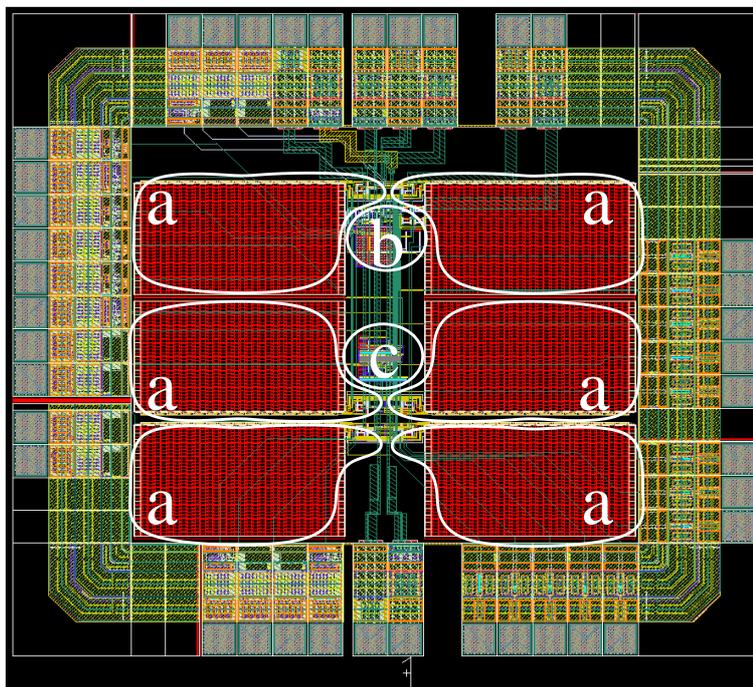


Figure 5.16: Layout of the complete DTCG.

comparatively very small area. Remind that this imbalance is due to the nature of our demonstrator.

Current-to-Voltage Conversion

The resistorless current-to-voltage converter shown in Subsection 4.3.3 is the chosen solution. This is not claimed here as the best possible choice. At the end of the following discussion about the current-to-voltage conversion, a brief comparison between our resistorless solution and the use of a simple resistor is done.

Fig. 4.13 is repeated in fig. 5.17 for reading convenience. The total consumption and area requirements of the N-opamp and P-opamp circuits are $6.12 \mu\text{A}$ and $236 \mu\text{m}^2$. The size of the transistor MOS res is $2 \mu\text{m} \times 1.75 \mu\text{m}$.

According to (4.27),

$$t_{step} = \frac{SV \cdot I_{step}}{k_n V_{BNC} \left(\frac{W}{L}\right)_{\text{MOS res}}},$$

being $(W/L)_{\text{MOS res}}$ the aspect ratio of MOS res, different values of V_{BNC} give us different values of t_{step} . By means of the digital signal $FRCW$, one between four available values of V_{BNC} can be chosen. At the same time, the value of I_{min} is updated in order to guarantee $V_{CS_{min}} = 0.875 \text{ V}$ for all $FRCW$. Table 5.1 summarizes these values. Besides, from fig. 5.12, a value of $SV = -6.6 \text{ ns/V}$ is extracted at the f_s/M of interest, 25 MHz, for $V_{CS} = 0.9 \text{ V}$. Table 5.2 summarizes the expected absolute value of t_{step} in ps, derived from (4.27).

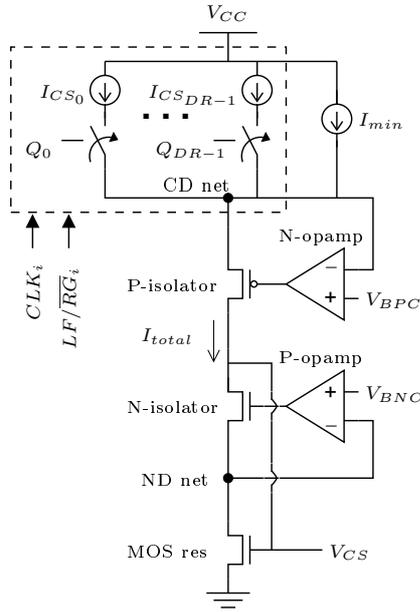


Figure 5.17: Diagram of the resistorless DTBG.

<i>FRCW</i>	V_{BNC} (V)	I_{min} (μA)
"00"	0.063	3.63
"01"	0.085	4.73,
"10"	0.128	6.51
"11"	0.295	9.57

Table 5.1: Values of V_{BNC} and I_{min} for a given *FRCW*.

<i>FRCW</i>	$ t_{step} $
"00"	3.32
"01"	2.46
"10"	1.63
"11"	0.71

Table 5.2: Expected absolute value of t_{step} in ps for a given *FRCW*.

Now, we will compare the resistorless current-to-voltage conversion circuit with a simple resistor. If a resistor is used as a current-to-voltage converter, (4.27) should be modified in the following way :

$$t_{step} = SV \cdot R \cdot I_{step}. \quad (5.8)$$

Obviously, I_{min} will be calculated as :

$$I_{min} = \frac{V_{CS_{min}}}{R}. \quad (5.9)$$

Table 5.3 shows the necessary R , I_{min} and area of the resistor to obtain the same t_{step} for $f_s/M = 25$ MHz, $V_{CS_{min}} = 0.9$ V, a given *FRCW*, and a resistor

<i>FRCW</i>	<i>R</i> (k Ω)	<i>I_{min}</i> (μ A)	Area (μm^2)
"00"	78.6	11.5	235.8
"11"	16.8	53.5	161.4

Table 5.3: Calculation of the necessary R , I_{min} and area of the resistor for $f_s/M = 25$ MHz, $V_{CS_{min}} = 0.9$ V and a given $FRCW$.

made from a high resistive polysilicon of width $2 \mu\text{m}$.

For our resistorless solution, I_{min} plus the bias current of P-opamp and N-opamp varies between $9.75 \mu\text{A}$ and $15.72 \mu\text{A}$, and the total required area is around $300 \mu\text{m}^2$. By comparing both I_{min} and area of the two solutions, we conclude that there are not important differences. A deeper analysis, including maybe noise sensibility and specially fabrication dispersion, is left to be done.

5.5 Conclusion

This chapter describes the demonstrator used to put into practice the overall calibration technique and, specially, the correction technique. At the same time, some details about this correction technique are highlighted.

The main information among these details is the area per correction cell parameter. In our circuit it is $205.7 \mu\text{m}^2$. This parameter can be used to estimate the area of a correction subsystem with the same t_{step} in SoC circuits. Another important information is the total consumption. It is inferior to $15.72 \mu\text{A}$, adding I_{min} and the bias current of P-opamp and N-opamp and neglecting I_{cal} , the consumption of the active correction cells⁴.

The total required area and consumption can be used as a criterion to compare two different techniques. This kind of comparison is done between our correction technique and that proposed by Jamal *et al.* [27] in the next paragraph.

The digital filters proposed by Jamal *et al.* in their 10-bits, 120-MSamples/s $M = 2$ time-interleaved ADC are estimated to require about 5mm^2 and about 190 mW in a $0.35\mu\text{m}$ CMOS technology as ours.

Let us now assume that the clock-skew correction range in a SoC circuit is 50 ps. From fig. 2.14, for a sinusoidal input signal at frequency 42 MHz⁵ and for $t_{step} = 2.3$ ps, the SFDR in a $M = 2$ channels case is about 70 dB, an acceptable SFDR in a 10-bits ADC. From (4.23), $DR = 22$. Only one channel has to be calibrated in a $M = 2$ channels time-interleaved ADC. So the total area required by this hypothetical correction system is $(22 \times 205.7 + 300)\mu\text{m}^2$, i.e., $4825\mu\text{m}^2$. As it is mentioned above, the total consumption is about $15.7 \mu\text{A}$, i.e., in our $V_{CC} = 3.3$ V technology, $52 \mu\text{W}$. So our correction technique is by far less power-hungry and requires much less area.

⁴In a SoC circuit, where only a small DR is necessary, this is an acceptable simplification.

⁵42 MHz is a 70% of $120 \text{ MHz}/2$, being 120 MHz the sampling frequency of the 10-bits ADC designed by Jamal *et al.*

Chapter 6

Measurements

6.1 Introduction

There are two key parameters in our mixed-signal clock-skew calibration technique: $|t_{step}|$ and $|t_{res}|$, being the latter defined as $|t_{res}| = |t_{res_i}[M \cdot ITER_{limit}]|$, i.e., the residual clock-skew in the steady state of the calibration operations performed on the i -th sampling clock.

The value of $|t_{step}|$ provides us with a parameter to evaluate the goodness of the correction operations carried out by the DCDE. The lower $|t_{step}|$, the finer the calibration can be.

As explained in Section 4.2, in the steady state, $|t_{res}|$ should verify $|t_{res}| \leq |t_{step}|$. A $|t_{res}|$ greater than $|t_{step}|$ means that the DDSS has not been able of reaching the minimum $|t_{res_i}|$ theoretically attainable with the actual DCDE used in the calibration system. It could happen if there is any phenomenon not considered in neither our simulation nor our analytical derivations.

These parameters can be easily measured by means of spectral analysis if a pure sinusoidal input test signal is used. As explained in Subsection 2.3.3, the presence of clock-skew importantly degrades the linearity of a time-interleaved ADC. For the $M = 2$ channels case, (2.26) gives the relation between $|t_{e_1}|$ and the SFDR limited by clock-skew in the digital spectrum domain for a sinusoidal input. This is repeated here for reading convenience:

$$|t_{e_1}| = \frac{\arctan\left(\frac{1}{\sqrt{\text{SFDR}_{\text{lin}}}}\right)}{\frac{\omega_{in}}{2T}}. \quad (6.1)$$

Moreover, the only spurious due to clock-skew is located at a frequency equal to $\pi - \omega_{in}$. This simplifies the task of measuring the SFDR due to clock-skew, provided that ω_{in} of our test signal is known in advance.

At the same frequency, $\pi - \omega_{in}$, another spurious signal due to gain mismatch arises (see Subsection 2.3.2). This is not an obstacle because the gain mismatch can accurately be removed off-line, once the samples have been stored, and prior to the $|t_{e_1}|$ extraction. This is done by, first, estimating separately the energy of the samples coming from each one of the two single ADCs and then, finely equaling these energies by means of a floating point multiplicative factor applied on one of the two sets of samples. Here there is a Scilab [8] code that performs these operations,

```

//estimating the gain mismatch
gain_mismatch = sqrt( sum( y(1:2:N_FFT).^2 )/sum( y(2:2:N_FFT).^2 ) );
//correcting the gain mismatch
y_gc(2:2:N_FFT) = gain_mismatch*y(2:2:N_FFT);
y_gc(1:2:N_FFT) = y(1:2:N_FFT);

```

where N_{FFT} is the length of the combined sets of samples and y_{gc} is the gain calibrated samples.

6.2 Test Bench

Fig. 6.1 shows a picture of the test bench. The signal generator is an Agi-

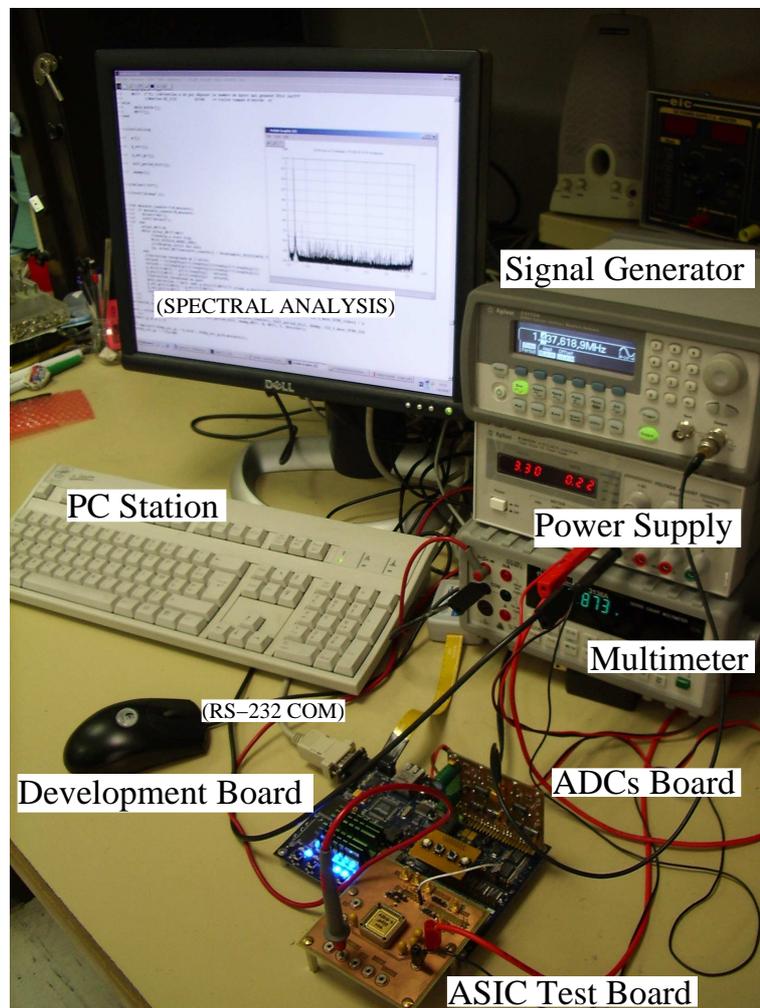


Figure 6.1: Picture of the test bench

lent 33220A, a 20 MHz Function/Arbitrary Waveform Generator. The spectral

analysis discussed in Section 6.1 is carried out by a PC station. The communication between this PC station and the development board is established via the RS-232 serial port. This communication is able of transmitting commands from the PC station to the ASIC test board and digitalized samples from the ADCs board to the PC station. Some Scilab scripts, conveniently introduced in Section 6.3 and Section 6.4, shows the use of functions based on a reading and writing management of the RS-232 serial port. On the development board side, a non-negligible amount of work has been done to develop VHDL code executed by the FPGA. This code manages the communications tasks and implements in real-time the digital detection algorithm. The whole of these tools allows us to implement the measurement procedures discussed in Section 6.3.

6.3 Measurement Methodology

6.3.1 $|t_{step}|$ Measurement Methodology

The demonstrator is given a $M = 2$ channels time-interleaved ADC configuration to carry out the measurements. A sinusoidal input test signal at a known frequency is digitalized. Now, the procedure to take one measure of the absolute value of $|t_{step}|$, $|t_{step}|$, is as follows :

1. The registers of both DCDEs are set to arbitrary initial states (referred as states A), so the overall time-interleaved ADC shows an arbitrary clock-skew $|t_{e1}|$, referred from now on as $|t_{eA}|$.
2. A FFT on a windowed set of digitalized samples of length N_{FFT} , $\dot{Y}_A(e^{j\omega})$, is then performed. Since the input signal frequency is known, the SFDR due to clock-skew can be extracted from $|\dot{Y}_A(e^{j(\pi-\omega_{in})})|^2$ as explained in Section 6.1. Fig. 6.2 shows an example of such a measure. In this example,

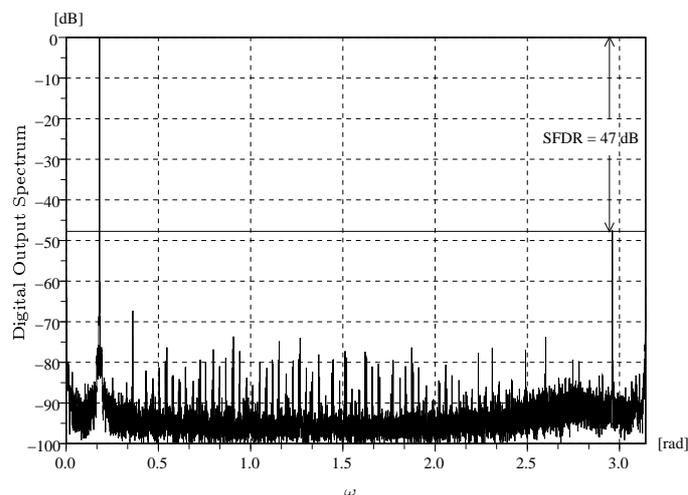


Figure 6.2: Measure of the SFDR due to clock-skew from a FFT on a windowed set of digitalized samples $\dot{Y}_A(e^{j\omega})$ for an arbitrary initial states of the DCDEs.

the input signal is located at a normalized frequency of 0.18 rad and the

spurious signal at 2.96 rad. Using (6.1), $|t_{e_A}|$ can be established, where the $\{\cdot\}$ operator stands for one measure of the argument. In our example, where $f_s = 50$ MHz, $|t_{e_A}| = 990$ ps.

3. The shift-register of one of the DCDEs are changed activating or deactivating a known number of correction cells, N_{steps} , so the overall time-interleaved ADC shows a new $|t_{e_1}|$, referred from now on as $|t_{e_B}|$. Here it is assumed that the sign of both t_{e_A} and t_{e_B} is the same. It can be assured with a reasonable confidence by using a low value of N_{steps} .
4. As in step 2, $|t_{e_B}|$ is found from a new FFT set of digitalized samples, $Y_B(e^{j\omega})$.
5. Finally, $|t_{step}|$ can be computed as

$$|t_{step}| = \left| \frac{|t_{e_A}| - |t_{e_B}|}{N_{steps}} \right|. \quad (6.2)$$

Due to noise (mainly sampling jitter and quantization noise), one measure could not be accurate enough to provide us with a reliable estimation. Refined estimations can be performed by averaging some measures. Let the operator $\{\hat{\cdot}\}$ be the average value of N_{meas} measures. Then, one estimation of t_{step} , denoted $t_{step}^{\hat{\cdot}}$, is computed as

$$|t_{step}^{\hat{\cdot}}| = \frac{\sum N_{meas} |t_{step}|}{N_{meas}}. \quad (6.3)$$

The standard deviation of $|t_{step}^{\hat{\cdot}}|$, $\sigma\{t_{step}^{\hat{\cdot}}\}$, is expected to decrease as $\sqrt{N_{meas}}$ when N_{meas} grows. A measure of $\sigma\{t_{step}^{\hat{\cdot}}\}$, $\dot{\sigma}\{t_{step}^{\hat{\cdot}}\}$, is computed as

$$\dot{\sigma}\{t_{step}^{\hat{\cdot}}\} = \frac{\dot{\sigma}\{t_{step}\}}{\sqrt{N_{meas}}}, \quad (6.4)$$

where $\dot{\sigma}\{t_{step}\}$ is the sample standard deviation of the N_{meas} available $|t_{step}|$.

Appendix H.1 shows a Scilab code source that performs these operations by sending the necessary commands to the FPGA-ASIC set.

6.3.2 $|t_{res}|$ Measurement Methodology

The procedure to measure $|t_{res}|$ is as follows :

1. Calibrate the clock-skew with a sinusoidal input test signal at a known frequency until the calibration system reaches the steady state and then stop the calibration. The input signal frequency should be set near the Nyquist frequency. As explained in Subsection 2.3.3, for high input signal frequencies the energy associated to the clock-skew error is higher than for low ones. This allows to reduce the calibration time and/or the size of the accumulator necessary to implement the clock-skew detection algorithm. For the same reason, the clock-skew related SFDR is lower for high input signal frequencies than for low ones. For very low $|t_{res}|$, this simplifies the task of distinguish the clock-skew related spurious signal from another merged non-linearities.

2. Perform a FFT on a windowed set of digitalized samples and then estimate $|t_{res}|$ by means of (6.1). Optionally, a periodogram can help to distinguish the spurious signal associated to a low $|t_{res}|$ from other non-linearities.

6.4 Measurement Results

6.4.1 $|t_{step}|$ Measurement Results

Table 6.1 summarizes the expected and estimated $|t_{step}|$ in ps for a given

<i>FRCW</i>	$ t_{step} $	$\hat{ t}_{step} $	$\hat{\sigma}\{\hat{ t}_{step} \}$
"00"	3.32	80.4	2.0
"01"	2.46	57.8	0.7
"10"	1.63	42.3	1.1
"11"	0.71	10.8	0.33

Table 6.1: Expected and estimated $|t_{step}|$, and estimated standard deviation in ps for a given *FRCW*.

FRCW as well as a measure of the standard deviation of the estimation. There is a constant disagreement factor of roughly 25 in $|\hat{t}_{step}|/|t_{step}|$, except for *FRCW*="11", where it is 15. The origin of this disagreement is likely to be a design mistake.

Measures involving the V_{CS} voltage of the DTBG have shown a disagreement factor of approximately 2 between the expected *SV* parameter at $V_{CS} = 0.9$ V and the actual one, contributing at the $|\hat{t}_{step}|/|t_{step}|$ disagreement factor.

As argued in Subsections 4.3.2 and 5.4.3, there is a strong dependence between the *SV* parameter and the V_{CS} voltage. Fig. 6.3 shows the evolution of

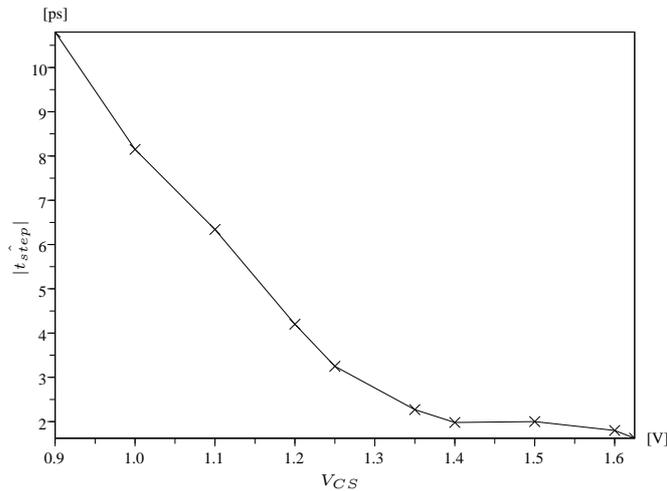


Figure 6.3: Estimated t_{step} as a function of V_{CS} .

$|\hat{t}_{step}|$ measured around different values of V_{CS} . A histogram of 150 $|\hat{t}_{step}|$ for a value of $V_{CS} = 1.6$ V is shown in Fig. 6.4. The observed $|\hat{t}_{step}|$ s are centered

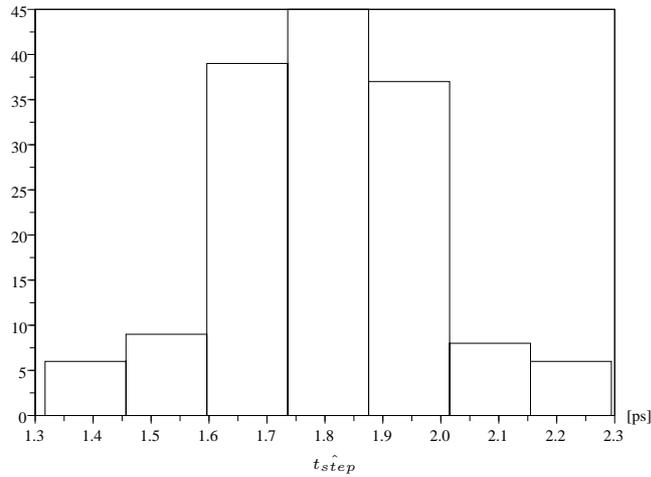


Figure 6.4: Histogram of $|t_{step}^{\wedge}|$.

around 1.8 ps with a standard deviation of 10%. Fig. 6.5 shows the histogram

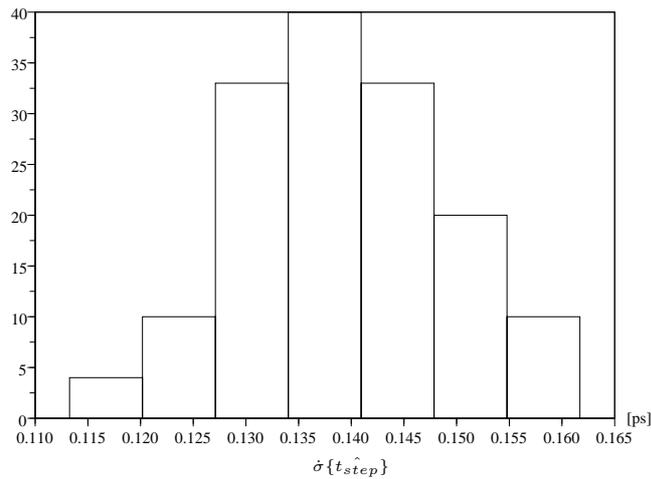


Figure 6.5: Histogram of $\hat{\sigma}\{|t_{step}^{\wedge}|\}$.

of $150 \hat{\sigma}\{|t_{step}^{\wedge}|\}$. These measures are centered at roughly 0.14 ps, slightly below the actual standard deviation observed from the histogram of $|t_{step}^{\wedge}|$, 0.18 ps. The parameters involved in the making of the histograms are $N_{meas} = 100$, $N_{FFT} = 4096$, $N_{steps} = 100$.

Both histograms corroborate the accuracy of our $|t_{step}|$ estimation.

Appendix H.2 shows a Scilab code source that performs these operations by sending the necessary commands to the FPGA-ASIC set.

6.4.2 $|t_{res}|$ Measurement Results

Fig. 6.6 shows a measure of SFDR=72.8 dB likely due to clock-skew from a FFT

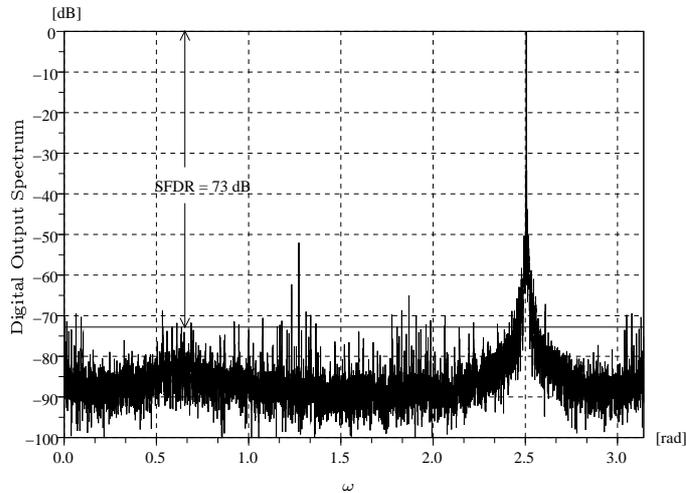


Figure 6.6: Measure of the SFDR due to clock-skew from a FFT on a windowed set of digitalized samples after calibration

on a windowed set of digitalized samples after calibration. This plot is the result of averaging 10 FFTs of length $N_{FFT} = 32768$. This SFDR is superior to the global SFDR shown in the figure. For example, the spurious signal at normalized frequency 1.3 rad is the second harmonic of the input signal. Because of this degraded global SFDR, maybe there are other contributors to the measured SFDR besides clock-skew. Let us assume that only clock-skew contributes to the measured SFDR. From (6.1), $|t_{res}| = 3.6$ ps, twice $|t_{step}|$ around $V_{CS} = 1.6$ V. This voltage was also the final V_{CS} voltage after calibration. As explained Subsection 6.3.2, the input signal frequency is set near the Nyquist frequency. It is a worst case scenario. Of course, after calibration, for a low input signal frequency as that shown in fig. 6.2, the clock-skew related spurious signal is at the same level than other non-linearities. This is shown in fig. 6.7.

This is a complicated measure because of the increasing importance of second-order effects. Fig. 6.8 shows detailed spectrums of the sampled signal around ω_{in} and $\pi - \omega_{in}$. From fig. 6.8b, spurious signals typically associated to some kind of signal modulation are observable all around ω_{in} . From fig. 6.8c, the not correctly cancelled images of these spurious signals are observable all around $\pi - \omega_{in}$. The spurious signal associated to the clock-skew (pointed out with an X) is found to be between the former ones and, in this example, it is of lesser power.

The origin of these spurious signals is uncertain. The signal modulation shown in fig. 6.8b could be caused by periodic jitter. However, simulations have shown that the spectral stamp shown in fig. 6.8c only appears if there are great disparities between the periodic jitter affecting the sampling clock of each channel. According to these simulations, these disparities are by far higher than the residual clock-skew or gain-mismatch. This suggests that there could be an external periodic coupled noise, different on each sampling clock.

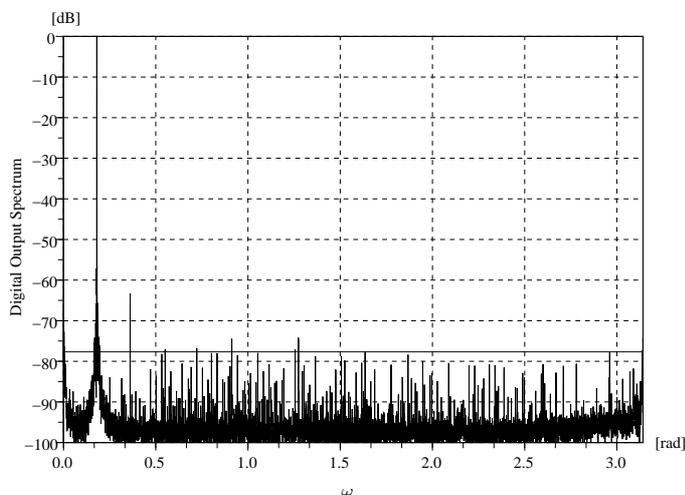


Figure 6.7: Digital output spectrum for a low input signal frequency after calibration

6.5 Conclusion

In principle, an actual $|t_{step}|$ of 10.8 ps for $V_{CS} = 0.9$ V and $FRCW = "11"$ prevents us from having a clock-skew calibrator that substantially improves the state of the art reached by the clock-edge reassignment technique. A $|t_{step}|$ around 1 ps is needed to make possible such improvement. Fortunately, both the reference sampling clock phase and the calibrated sampling clock phase can be independently adjusted. The former is manually set in such a way that the final V_{CS} associated to the latter in the steady state is around 1.6 V. As explained in this chapter, $|t_{step}|$ around this value of V_{CS} is only 1.8 ps.

Of course, manipulating the reference sampling clock phase is not what was initially planned. This is an ad hoc solution we have resorted to in order to get around our design mistakes as well as higher than expected initial clock-skews. A well-designed calibration system in a fully integrated time-interleaved ADC should not demand such kind of adjustments. But at least our demonstrator allows us to show that the mixed-signal clock-skew calibration technique is feasible and has the potentiality of attaining residual clock-skew errors as low as the measured 3.6 ps. This is done in a highly hostile environment of interconnected discrete components where our demonstrator corrects initial clock-skews of thousands of picoseconds.

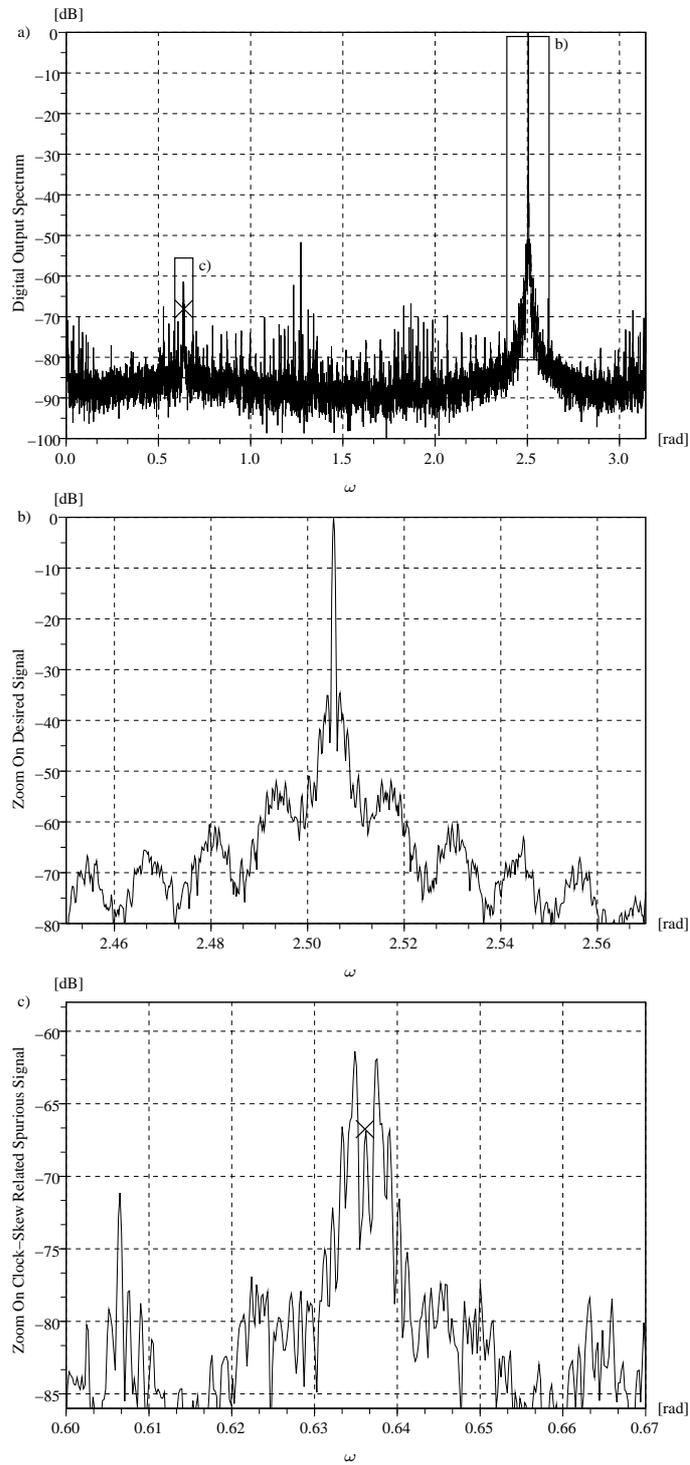


Figure 6.8: a) Global spectrum of the sampled signal b) Detailed spectrum around ω_{in} c) Detailed spectrum around $\pi - \omega_{in}$

Chapter 7

Conclusions

A detailed review and classification of the existing techniques to minimize or cancel clock-skew effects is accomplished in Chapter 3. Research contributions concerning some of these techniques are discussed in Appendix A, B, and C.

The main research contribution is detailed in Chapter 4. There, a new technique to minimize clock-skew effects in time-interleaved ADCs is presented. Among the different solutions existing in the literature, ours is classed as a calibration technique, more specifically as the only mixed-signal one. Its mixed-signal nature allows at the same time to make the most of the simplicity of analog clock-skew correction techniques and the robustness of digital clock-skew detection ones. Tables 4.1 and 4.2 in Section 4.5 summarize and compare the characteristics of the proposed calibration technique with the existing ones. The more remarkable characteristics are reminded in the following two paragraphs.

An implementation on FPGA of our digital clock-skew detection technique has been performed. This technique has been analytically studied and its advantages and limitations have been highlighted. They are repeated here :

- The detection technique can handle a M -channel general case.
- The use of simply the sign of the digitalized signal dramatically simplifies the required hardware as well as provides with an intrinsic robustness against gain mismatch.
- The use of a simple offset-mismatch cancellation filter provides with robustness against this type of mismatch.
- Analytically derived conditions that the input signal must verify for the detection subsystem to work properly prevent background calibration for a general kind of input signal. However, the input signal restrictions are lax enough to allow the use of easy-to-generate signal tests in a foreground calibration.

An implementation on an ASIC of our analog clock-skew correction technique has been designed, manufactured and measured. Even if the design process must be revised before claiming a good mastery of the implementation, a granularity as fine as 1.8 ps has been observed. Moreover, this implementation gives us a first idea of the area and power consumption requirements of our correction technique. From this data, a comparison with a purely digital correction

technique is carried out in the conclusion section of Chapter 5. It reveals that the correction technique requires clearly less power and area.

Both implementations, that of the detection technique as well as that of the correction technique, have been embedded in a closed-loop to form a complete clock-skew calibration system. The stability of this closed-loop has been experimentally verified in a highly hostile environment of interconnected discrete components with a high presence of noise and non-linearities. A residual clock-skew of 3.6 ps has been observed after calibration. This clock-skew is twice the granularity of the used correction system, an unexpected value. As explained in Chapter 6, this measure is likely subject to a coupled phase noise on the sampling clock signals from some external noise source. This should not be a problem in a fully-integrated time-interleaved ADC, where the residual clock-skew is expected to be inferior to the granularity of the correction system.

As a perspective, in order to track clock-skew variations due to operation temperature, component ageing or stress, a hypothetical fully-integrated time-interleaved ADC could incorporate a simple test signal generator. In fact, since any clock-like signal or sinusoidal signal are valid for test as long as their frequencies are roughly known, this generator could likely be as simple as a free-running ring-oscillator, although this point must be verified.

In a futuristic software defined radio context, resolutions as high as 16 bits could be required for large input signal bandwidths. It implies a t_{step} far below 1 ps. Obtaining such a small t_{step} value, for a reasonable t_{step} dispersion, can be done by increasing both the area and the power consumption of the correction system. The precise tradeoffs depend on the technology and the implementation. However, the area and the power consumption used in our demonstrator suggest that the proposed technique has the potentiality of reaching very small t_{step} values while keeping these parameters reasonable.

The demonstrator can be viewed as the first step in a long-term research project of a fully-integrated time-interleaved ADC where at least three calibration systems will coexist : a clock-skew, a gain-mismatch and an offset-mismatch calibration. There exist moderately complex gain-mismatch and offset-mismatch calibration techniques. In this work, we have tried to find a clock-skew calibration technique as simple and robust as its gain-mismatch and offset-mismatch counterparts.

Appendix A

General Case Correction Filters

The clock-skews in a M -channels time-interleaved ADC can be digitally corrected by $M - 1$ filters. The following paragraphs shows a step-by-step analytical methodology to find the impulse response of these filters in a M -channels time-interleaved ADC. They are placed as indicated in fig. A.1. Let the value

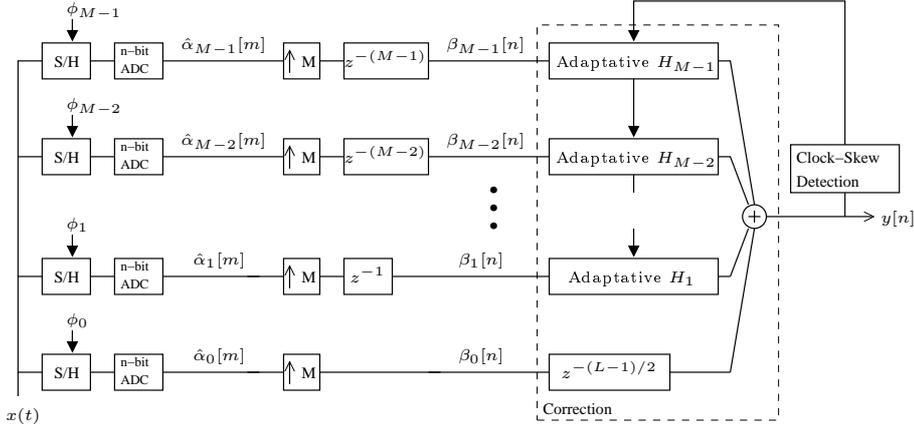


Figure A.1: General diagram of a M -channels all-digital calibration technique.

of the t_{e_i} clock-skews, $1 \leq i \leq M - 1$, be known. This value is provided by the measurement subsystem. From 2.21, the $\beta_i[n]$ signals in fig. A.1 are, in the frequency domain :

$$\beta_i(e^{j\omega}) = \frac{1}{MT} \sum_k b_{ik}(\omega) X \left(\frac{\omega}{T} - \frac{2\pi}{MT} k \right), \quad k \in \mathbb{Z}, \quad (\text{A.1})$$

where, the $b_{ik}(\omega)$ coefficient is defined as :

$$b_{ik}(\omega) = e^{j(\omega - \frac{2\pi}{M}k) \frac{t_{e_i}}{T}} e^{-j \frac{2\pi}{M} ik}, \quad (\text{A.2})$$

i.e., a factor associated in the i -th channel to the k -th alias signal $X \left(\frac{\omega}{T} - \frac{2\pi}{MT} k \right)$. For notation convenience, the k -th alias signal will be denoted $X_k(\omega)$ from now

on.

Note that $b_{0k}(\omega)$ is considered error free, i.e., $t_{e_0} = 0$. Because of that, the zeroth-channel does not need a correction filter, just a delay.

Now, let us define the $H(e^{j\omega})$ vector as :

$$H(e^{j\omega}) = (H_1(e^{j\omega}), \dots, H_i(e^{j\omega}), \dots, H_{M-1}(e^{j\omega})), \quad (\text{A.3})$$

where $H_i(e^{j\omega})$ is the frequency response of the filter of the i -th channel. The aim of these filters is to cancel the undesired $X_k(\omega)$ in the digital addition that forms the $y[n]$ global output.

Let $X(\frac{\omega}{T})$ be a bandlimited signal :

$$-\pi f_s < \frac{\omega}{T} < \pi f_s \quad (\text{A.4})$$

In this situation, not all the alias signals are present at a given discrete-time frequency. It is illustrated for a four-channels example in fig. A.2. So let SB_K ,

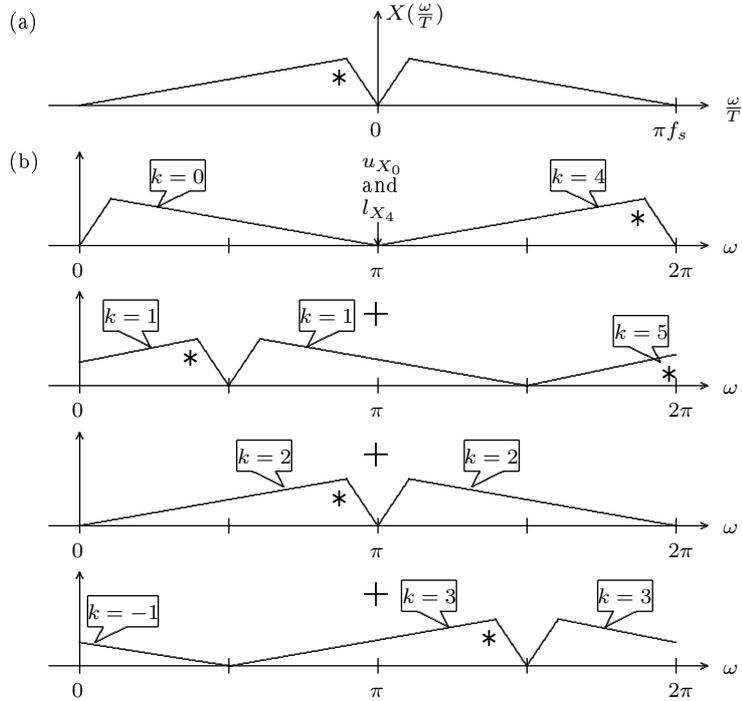


Figure A.2: (a) Bandlimited analog input signal. (b) Alias decomposition of $\beta_i[n]$ for $0 \leq \omega \leq 2\pi$ and l_{X_0} and u_{X_4} examples.

$K \in \mathbb{Z}$, be spectrum subbands. Both the bandwidth and the position of SB_K depend on M , the number of channels. Let the SB_K lower bound, denoted l_{SB_K} , be :

$$l_{SB_K} = \frac{2\pi}{M}(K-1) - \pi. \quad (\text{A.5})$$

Let the SB_K upper bound, denoted u_{SB_K} , be :

$$u_{SB_K} = \frac{2\pi}{M}K - \pi. \quad (\text{A.6})$$

So $\omega \in SB_K$ if $\omega \in [l_{SB_K}, u_{SB_K})$. By virtue of (A.4), the lower discrete-time frequency where some energy of $X_k(\omega)$ can be found is superior to l_{X_k} :

$$l_{X_k} = \frac{2\pi}{M}k - \pi. \quad (\text{A.7})$$

The highest discrete-time frequency where some energy of $X_k(\omega)$ can be found is inferior to u_{X_k} :

$$u_{X_k} = \frac{2\pi}{M}k + \pi. \quad (\text{A.8})$$

Obviously, u_{X_k} and l_{X_k} verify :

$$u_{X_k} > l_{X_k} \quad (\text{A.9})$$

From these definitions, we can find which $X_k(\omega)$ actually have some energy in a given SB_K . In fact, for some energy of $X_k(\omega)$ to be found in SB_K , its bounds l_{X_k} and u_{X_k} must verify at the same time :

$$l_{X_k} < u_{SB_K} \quad (\text{A.10a})$$

$$u_{X_k} > l_{SB_K} \quad (\text{A.10b})$$

Substituting these elements by their definitions and using the previous inequalities, we have that if k verifies

$$K - M \leq k \leq K - 1, \quad (\text{A.11})$$

then some energy of $X_k(\omega)$ are partially present in SB_K . There are up to M different $X_k(\omega)$ in each SB_K . For example, for the four-channels case, in SB_3 , $X_{-1}(\omega)$, $X_0(\omega)$, $X_1(\omega)$ and $X_2(\omega)$ can be found.

Now we will show that the filters have different analytical expressions for each subbands. This kind of filters are called multilevel filters [66].

Let $H_{iK}(e^{j\omega})$ be the frequency response of the i -th filter for $\omega \in SB_K$. By analogy, $H_K(e^{j\omega})$ is the $H(e^{j\omega})$ vector for $\omega \in SB_K$. The undesired $X_k(\omega)$ terms verify that $k \neq l \cdot M$, $l \in \mathbb{Z}$. These undesired $X_k(\omega)$ are cancelled by adding all the filtered signals and those from the unfiltered $i = 0$ channel. For $X_k(\omega)$, $k \in [K - M, \dots, K - 1]$ except $k = l \cdot M$, $l \in \mathbb{Z}$, the previous sentence can be analytically written as :

$$b_{0,k}(\omega)X_k(\omega) + \sum_{i=1}^{M-1} H_{i,K}(e^{j\omega})b_{i,k}(\omega)X_k(\omega) = 0, \quad \omega \in SB_K, \quad (\text{A.12})$$

It simplifies to :

$$\sum_{i=1}^{M-1} H_{i,K}(e^{j\omega})b_{i,k}(\omega) = -b_{0,k}(\omega). \quad (\text{A.13})$$

(A.13) can be written in matrix form considering the $M - 1$ undesired $X_k(\omega)$ for a given SB_K :

$$H_K(e^{j\omega}) \cdot B_K(\omega) = -(b_{0,K-M}(\omega), \dots, b_{0,K-1}(\omega)), \quad \omega \in SB_K, \quad (\text{A.14})$$

where :

$$B_K(\omega) = \begin{pmatrix} b_{1,K-M}(\omega) & \dots & b_{1,K-1}(\omega) \\ \vdots & & \vdots \\ b_{M-1,K-M}(\omega) & \dots & b_{M-1,K-1}(\omega) \end{pmatrix}. \quad (\text{A.15})$$

Note that $B_K(\omega)$ is a $(M - 1) \times (M - 1)$ matrix. For example, in a $M = 4$ channel case, this system equation for the SB_3 subband is :

$$H_3(e^{j\omega}) \cdot B_3(\omega) = -(b_{0,-1}(\omega), b_{0,1}(\omega), b_{0,2}(\omega)), \quad 0 \leq \omega < \frac{\pi}{2}, \quad (\text{A.16})$$

where :

$$B_3(\omega) = \begin{pmatrix} b_{1,-1}(\omega) & b_{1,1}(\omega) & b_{1,2}(\omega) \\ b_{2,-1}(\omega) & b_{2,1}(\omega) & b_{2,2}(\omega) \\ b_{3,-1}(\omega) & b_{3,1}(\omega) & b_{3,2}(\omega) \end{pmatrix}. \quad (\text{A.17})$$

Finally, $H_K(e^{j\omega})$ is found doing :

$$H_K(e^{j\omega}) = -(b_{0,K-M}(\omega), \dots, b_{0,K-1}(\omega)) \cdot [B_K(\omega)]^{-1}. \quad (\text{A.18})$$

It is out of the scope of this work to find the conditions for the inverse $B_K(\omega)$ to exist. Other works show the possibility of perfect reconstruction of $x(t)$ assuming $t_{e_i} \ll T$ [55] [19]. It suggests that $B_K(\omega)$ can actually be inverted in any normal situation in time-interleaved ADCs.

These steps must be repeated for each SB_K to find the frequency responses for any 2π radians long frequency range. The impulse responses are derived from the frequency response by the Frequency Sampling Method and the Inverse Discrete Fourier Transform [2]. All the filters generated in this way are observed to have an impulse response with real coefficients. In general, the $H(e^{j\omega})$ filters should have an infinite impulse response and be noncausal. In a real time system, it is not feasible, and the natural choice is implementing causal FIR filters of L taps that approximates the ideal ones. In [55], the impulse responses are derived using a least square method that minimizes the reconstruction error.

The calibrated $y[n]$ global output is not exactly the uniformly sampled $x(t)$. It is not a perfect reconstruction method, even if ideal filters are employed. There are a residual gain and a phase distortion which depend on t_{e_i} clock-skew. It is not a major drawback because they could be neglected in many applications. More details are given in Subsections B.1.2 and B.3.2 for the $M=2$ and $M=4$ cases respectively. Perfect reconstruction (assuming ideal filters) can be obtained adding one more filter (the 0-th correction filter) to the method presented here, as it is done in [55].

Appendix B

The Jamal *et al.*'s Calibration Technique

The methodology shown in Appendix A is applied to derive the correction filter used by Jamal *et al.* [27] for the two-channels case in Section B.1. In Section B.2, a detailed analytical analysis of the clock-skew measurement technique used in Jamal *et al.*'s work [27] [28] is shown. Finally, some simulation results are shown in Section B.3.

B.1 Jamal *et al.*'s Correction Filter

In the following paragraphs the method introduced in Appendix A is used to find the impulse response of the digital correction filter used in [27] for a two-channels time-interleaved ADC as that shown in fig. B.1. Then, the residual gain and

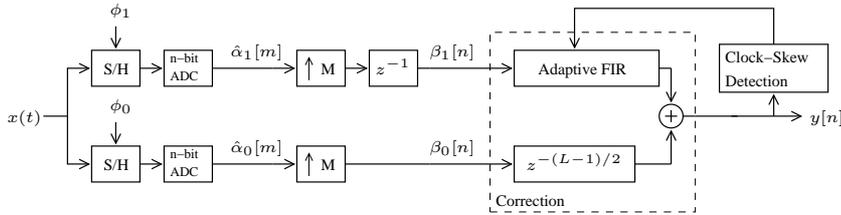


Figure B.1: General diagram of the Jamal *et al.*'s calibration technique.

phase distortions from the correction filter that prevent perfect reconstruction are derived.

B.1.1 Analytical Development of the Correction Filter

From A.2, for the two-channels case, the $b_{ik}(\omega)$ coefficients are :

$$b_{ik}(\omega) = e^{j\omega \frac{t_{e_i}}{T}} e^{-j\pi \frac{t_{e_i}}{T} k} e^{-j\pi i k}, \quad (\text{B.1})$$

where $t_{e_0} = 0$ and $t_{e_1} = t_e$.

Now, the frequency response of the filter in any 2π radians long frequency

range can be used to analytically derive the impulse response by means of the Inverse Discrete-Time Fourier Transform. Let us chose $SB_1 = [-\pi, 0)$ and $SB_2 = [0, \pi)$. The frequency responses of $H_{1,1}(e^{j\omega})$ in SB_1 and $H_{1,2}(e^{j\omega})$ in SB_2 are independently derived :

For $\omega \in SB_1 = [-\pi, 0)$, applying A.18, we find :

$$H_{1,1}(e^{j\omega}) = -b_{0,-1}[b_{1,-1}]^{-1}. \quad (\text{B.2})$$

Substituting,

$$H_{1,1}(e^{j\omega}) = -1[-e^{j\omega(\frac{t_e}{T})}e^{+j\pi(\frac{t_e}{T})}]^{-1}. \quad (\text{B.3})$$

Simplifying,

$$H_{1,1}(e^{j\omega}) = e^{-j\omega(\frac{t_e}{T})}e^{-j\pi(\frac{t_e}{T})}. \quad (\text{B.4})$$

For $\omega \in SB_2 = [0, \pi)$, applying A.18, we find :

$$H_{1,2}(e^{j\omega}) = -b_{0,1}[b_{1,1}]^{-1}. \quad (\text{B.5})$$

Substituting,

$$H_{1,2}(e^{j\omega}) = -1[-e^{j\omega(\frac{t_e}{T})}e^{-j\pi(\frac{t_e}{T})}]^{-1}. \quad (\text{B.6})$$

Simplifying,

$$H_{1,2}(e^{j\omega}) = e^{-j\omega(\frac{t_e}{T})}e^{j\pi(\frac{t_e}{T})}. \quad (\text{B.7})$$

The combined $H_{1,1}(e^{j\omega})$ and $H_{1,2}(e^{j\omega})$ frequency responses gives :

$$H(e^{j\omega}) = e^{-j\omega(\frac{t_e}{T})}e^{+j\pi(\frac{t_e}{T})\text{sign}(\omega)}, \quad -\pi \leq \omega < \pi. \quad (\text{B.8})$$

Finally, the impulse response is found by the Inverse Discrete-Time Fourier Transform from (B.8). The result is :

$$h[n] = -\frac{\sin\left(\pi\frac{t_e}{T}\right)}{\pi\left(n - \frac{t_e}{T}\right)}. \quad (\text{B.9})$$

B.1.2 Residual Gain and Phase Distorsions from the Correction Filter

A clock-skew trace remains on the desired alias signals that arises in the global output $y[n]$ when the signals from the zeroth and first channel are added. Fig. B.2 illustrates the alias decomposition of $\beta_1[n]$, the signal in channel 1, when $x(t)$ is a band-limited analog input signal, $-\pi f_s < \omega < \pi f_s$. This clock-skew trace adds a gain and phase distorsions. To derive them, let us enumerate the error-related alias phases before and after filtering in in channel 1 for $0 \leq \omega < \pi$:

- For $k = 0$, before filtering, the error-related alias phase in channel 1 is $\omega t_e/T$. After filtering, it becomes $+\pi t_e/T$.
- For $k = 1$, before filtering, the error-related alias phase in channel 1 is $\omega t_e/T - \pi t_e/T$. After filtering it becomes null. It allows the cancellation of this undesired alias by adding the signal in channel 0.

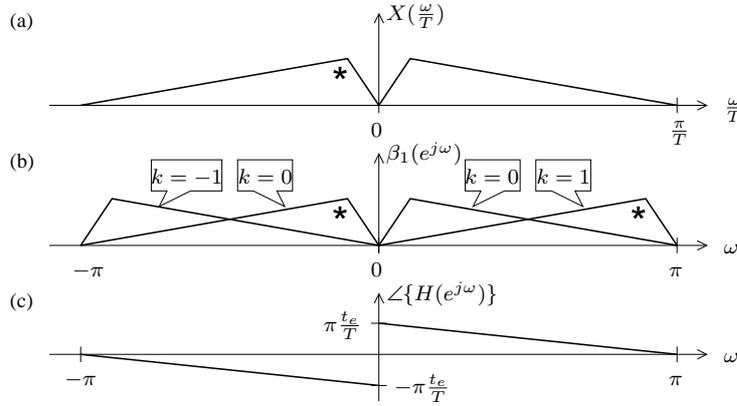


Figure B.2: (a) Band-limited analog input signal. (b) Alias decomposition of the $\beta_1[n]$ digital signal for $-\pi < \omega < \pi$. (c) Complex phase of the correction filter.

So $Y(e^{j\omega})$, for $0 \leq \omega < \pi$, is :

$$Y(e^{j\omega}) = \frac{1}{2T}X\left(\frac{\omega}{T}\right) + \frac{1}{2T}X\left(\frac{\omega}{T}\right)e^{+j\pi\frac{t_e}{T}} = \frac{1}{T}X\left(\frac{\omega}{T}\right)\cos\left(\pi\frac{t_e}{2T}\right)e^{+j\pi\frac{t_e}{2T}}. \quad (\text{B.10})$$

For a small clock-skew, it could be negligible. For example, for a clock-skew $t_e/T < 1\%$, the cosines-related loss is smaller than $1.1 \cdot 10^{-3}$ dB and the phase shift smaller than 0.9 degrees.

B.2 Jamal *et al.*'s Measurement Technique

B.2.1 Principle of Operation

In the following paragraphs an analytical analysis of the clock-skew measurement technique used in Jamal *et al.*'s work [27] [28] is shown.

From 2.22, for a two channels time-interleaved ADC and when the analog input signal is a complex exponential signal at normalized frequency ω_{in} , the frequency domain expression of $y[n]$ is given by :

$$Y(e^{j\omega}) = \sum_{k=-\infty}^{\infty} S_k 2\pi \delta(\omega - \omega_{in} - \pi k), \quad (\text{B.11})$$

where S_k are :

$$S_k = S_k(\omega_{in}) = \frac{1}{2} \begin{cases} \left(1 + e^{j\omega_{in}\frac{t_e}{T}}\right), & k \text{ even,} \\ \left(1 - e^{j\omega_{in}\frac{t_e}{T}}\right), & k \text{ odd.} \end{cases} \quad (\text{B.12})$$

Observing the differences between the k odd and even cases, the following can be said :

- If $t_e = 0$, $S_{k_{\text{odd}}} = 0$.

- The phase difference between $S_{k_{\text{even}}}$ et $S_{k_{\text{odd}}}$ is :

$$\angle S_{k_{\text{even}}} - \angle S_{k_{\text{odd}}} = \text{sign}\{t_e\} \frac{\pi}{2}, \quad (\text{B.13})$$

where $\text{sign}\{\cdot\}$ denotes the sign function and $\angle\{\cdot\}$ denotes complex phase.

Exploiting these spectral properties gives a way to detect and measure the clock-skew. It is explained in the following paragraphs.

The diagram of the clock-skew detector is repeated here for convenience. Let

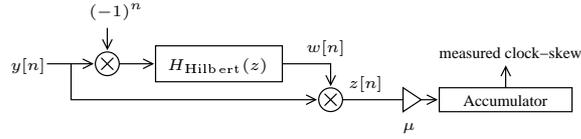


Figure B.3: Diagram of the clock-skew detector.

the fig. B.4 be the digital spectrum of the signals $y[n]$ and $w[n]$ for $0 \leq \omega < 2\pi$

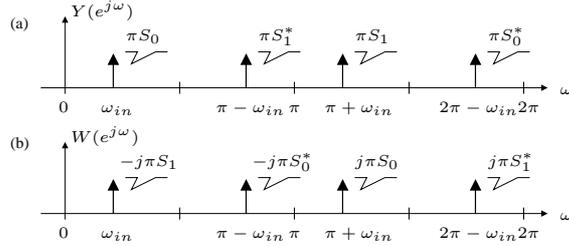


Figure B.4: Digital spectrum of the signals (a) $y[n]$, and (b) $w[n]$ for a sinusoidal input signal.

and a sinusoidal input signal. This figure shows that the chopped operation, i.e., the signal multiplication by $(-1)^n$, produces an exchange between the spectral energy at the input signal frequency ω_{in} (where the S_0 factors are placed originally) and the energy at the undesired image signal frequency $\pi - \omega_{in}$ (where the S_1 factors are placed originally). The ideal discrete-time Hilbert filter, the frequency response of which is $-j\text{sign}\{\omega\}$, introduces a extra phase shift on the chopped signal, giving $w[n]$. The result of multiplying $y[n]$ and $w[n]$ is $z[n]$. Finally, an accumulator sense the DC component of $z[n]$. It is derived here :

$$\begin{aligned} Z(e^{j0}) &= \frac{1}{2\pi} \int_0^{2\pi} Y(e^{j\lambda}) W(e^{j(\omega-\lambda)}) d\lambda \Big|_{\omega=0} \\ &= j\pi (S_0 S_1^* - S_1 S_0^*) \delta(0) \\ &= j\pi r_0 r_1 \left(e^{\text{sign}\{t_e\} \frac{\pi}{2}} - e^{-\text{sign}\{t_e\} \frac{\pi}{2}} \right) \delta(0) \quad (\text{B.14}) \\ &= -2\pi r_0 r_1 \sin\left(\text{sign}\{t_e\} \frac{\pi}{2}\right) \delta(0) \\ &= -2\pi \text{sign}\{t_e\} r_0 r_1 \delta(0), \end{aligned}$$

where $r_0 = |\cos(\omega_{in} t_e / 2T)|$ and $r_1 = |\sin(\omega_{in} t_e / 2T)|$, the modulus of S_0 and

S_1 respectively. For $\omega_{in}t_e/2T \ll 1$, B.14 simplifies to :

$$Z(e^{j0}) \approx -2\pi \frac{\omega_{in}t_e}{2T} \delta(0). \quad (\text{B.15})$$

Then, the DC component of $z[n]$ is $-\frac{\omega_{in}t_e}{2T}$. It can be shown that without the Hilbert filter, $Z(e^{j0})$ is zero. A one-tap approximation for the ideal Hilbert filter can be used. It is just a delay of one sample. There is a detailed discussion about the effects of this approximation in [28].

The output of this accumulator drives the correction filter forming a negative feedback loop.

B.2.2 Conditions for Proper Operation

The value of the DC component of $z[n]$ is proportional to the clock-skew provided that the analog input signal does not contain any components at ω_{in}/T and $(\pi - \omega_{in})/T$ at the same time. According to [28], the $x(t)$ analog input signal for the clock-skew detector to work properly must verify :

$$\left| X\left(\frac{\omega}{T}\right) X\left(\frac{\pi}{T} - \frac{\omega}{T}\right) \right| = 0. \quad (\text{B.16})$$

It can be intuitively understood in the frequency domain. Fig. B.5.a shows an analog input signal that does not verify (B.16). Fig. B.5.b shows the undesired

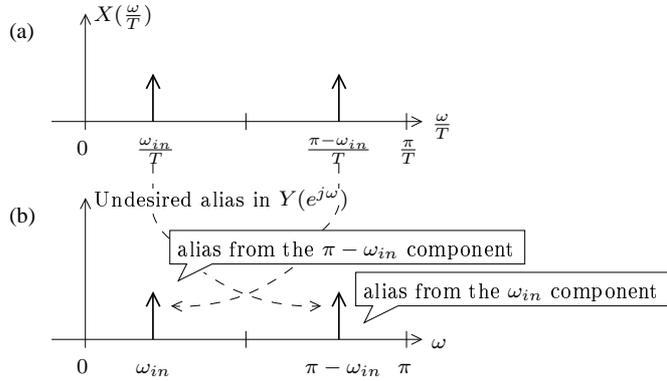


Figure B.5: (a) Digital spectrum of analog input signal that does not verify (B.16). (b) Undesired alias signal resulting from clock-skew.

digital alias signal resulting from clock-skew. The desired and undesired alias are all merged, so there are no way of distinguishing between them. The value of the DC component of $z[n]$ from (B.14) will be in general different from zero, even if no clock-skew exist. Then the accumulator will diverge and the coefficients of the correction filter will be incorrect.

B.2.3 Robustness of the Technique

Robustness refers to the sensibility to fabrication dispersion. This measurement technique is implemented as a digital circuit, so it does not suffer from dispersion itself. However, the gain and offset mismatch between the channels of

the time-interleaved ADC could interfere with the operation of a measurement technique. The following paragraphs shows that this technique is robust facing these mismatches.

Offset Mismatch

Let us analyze the robustness against offset mismatch in the time-domain for a one-tap approximation to the Hilbert filter, i.e, just a delay cell. The clock-skew detector can be considered as robust if the presence of offset mismatch does not affect the accumulated value, i.e., it is null in the long term.

Let o_0 be the offset of the channel 0, and o_1 the offset of the channel 1. Let us observe the downsampled accumulator output when there is no input signal, just offset, so $y[2m] = o_0$ and $y[2m - 1] = o_1$:

$$Accum[2m] = \sum_{l=-\infty}^{2m-1} y[l]y[l-1](-1)^{l-1} = \quad (B.17)$$

$$\sum_{p=-\infty}^m \{y[2p-1]y[2p-2] - y[2p-2]y[2p-3]\} = \sum_m (o_1o_0 - o_0o_1) = 0.$$

So the offset components cancel each other in the accumulator every two samples.

Gain Mismatch

Let us analyse the robustness against gain mismatch in the time-domain for a one-tap approximation to the Hilbert filter, i.e, just a delay cell. The clock-skew detector can be considered as robust if the presence of gain mismatch does not prevent the accumulated value from being proportional to the clock-skew.

Let g_0 be the gain of the channel 0, and g_1 the gain of the channel 1, so the digital output entering the accumulator is $\hat{y}[2n] = g_0y[2n]$ and $\hat{y}[2n - 1] = g_1y[2n - 1]$, where $y[n]$ is the digital output for a gain mismatch free system. The accumulator output becomes :

$$Accum[n] = \sum_{l=-\infty}^{n-1} \hat{y}[l]\hat{y}[l-1](-1)^{l-1} = \quad (B.18)$$

$$g_0g_1 \sum_{l=-\infty}^{n-1} y[l]y[l-1](-1)^{l-1}.$$

It shows that the gain mismatch simply scales the accumulated value, not preventing clock-skew from being correctly sensed.

B.3 Simulation Results

B.3.1 Simulation Parameters and Results

The expanded Jamal *et al.*'s calibration technique, for a $M = 4$ channels case, has been simulated. The correction filters have been generated as explained

in Appendix A. The four-channels measurement system used is presented in Section 4.4.

Gain and offset mismatch errors are not present in the simulated system. The input signal is a pure sine wave with amplitude the full scale of the converters, ideal 10 bits uniform quantizers. The relative clock-skews are : on channel 3, $\frac{t_{e3}}{T} = 0.0082$. On channel 2, $\frac{t_{e2}}{T} = 0.0041$. On channel 1, $\frac{t_{e1}}{T} = -0.0041$. The actual correction subsystem is an adaptive FIR filter formed by 31 coefficients of a finite precision of 13 bits.

Fig. B.6 shows the SNDR for the calibrated and uncalibrated output signal.

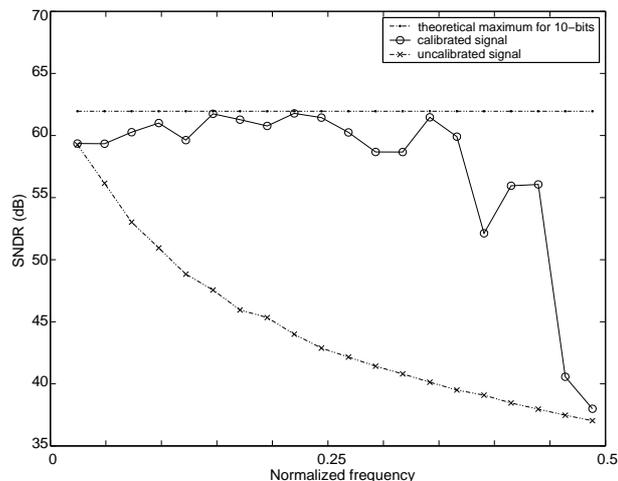


Figure B.6: SNDR measured from simulations for a sinusoidal input signal.

After convergence, the SNDR of the calibrated signal is around 60 dB (near the theoretical maximum for a 10 dB quantized signal) for normalized input signal frequencies up to approximately 0.35. The SNDR decreases for high input signal frequencies due to the filter truncation. The SNDR is not decreasing monotonically because of the finite precision.

B.3.2 Residual Gain and Phase Distorsions from the Correction Filters

After calibration, the global frequency response between an ideally sampled input signal and $y[n]$ due to the correction subsystem is shown in fig. B.7. As it has been said, the gain and phase distorsion could be neglected depending on the application.

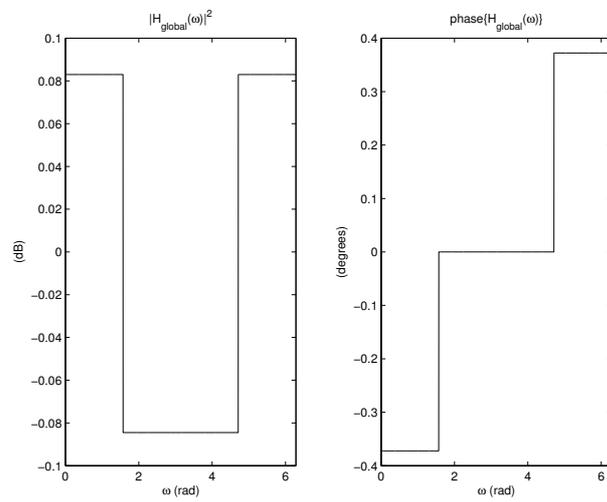


Figure B.7: Frequency response between an ideally sampled input signal and $y[n]$ due to the correction subsystem.

Appendix C

Restriction in Jin and Lee's Measurement Technique

Let us assume that the signal $r(t)$ in fig. 3.14 is zero, so the DC component of the signal $\hat{\alpha}_i[m]$ must be zero for the measurement technique to work properly. A more concise input signal restriction in the frequency domain is derived below.

Since $\hat{\alpha}_i[m] = \beta_i[Mm + i]$, then, in the frequency domain,

$$\beta_i(e^{j\omega}) = \hat{\alpha}_i(e^{j\omega M})e^{-j\omega i}. \quad (\text{C.1})$$

From (C.1) and (2.21),

$$\hat{\alpha}_i(e^{j\omega}) = \frac{1}{MT} \sum_{k=-\infty}^{\infty} X\left(\frac{\omega}{MT} - \frac{2\pi}{MT}k\right) e^{j\left(\frac{\omega}{MT} - \frac{2\pi}{MT}k\right)(iT+t_{e_i})}. \quad (\text{C.2})$$

This equation, for $\omega = 0$ and equaling to zero, gives :

$$\sum_{k=-\infty}^{\infty} X\left(\frac{2\pi}{MT}k\right) e^{j\frac{2\pi}{MT}k(iT+t_{e_i})} = 0, \quad \forall t_{e_i}. \quad (\text{C.3})$$

Due to the $\forall t_{e_i}$ condition, (C.3) can be simplified to

$$\left| X\left(\frac{2\pi}{MT}k\right) \right| = 0, \quad \forall k \in \mathbb{Z}.$$

Appendix D

Analysis of cross-correlation

This Appendix analytically derives (4.54)

$$r_{\hat{\alpha}_i \hat{\alpha}_{i-1}}[0] = \sum_{\forall i_n} \frac{A_{in}^2}{2} \cos\left(\omega_{in} + \frac{\omega_{in}}{T}(t_{e_i} - t_{e_{i-1}})\right) + \overline{res_{i,i-1}[0]},$$

$$\text{for } 1 \leq i \leq M - 1.$$

as a generalization of the two sinusoidal input signals case. A similar development can be done for (4.55). The results here can be used to justify (4.32) too, where only one sinusoidal input signal is considered.

To do so, first, the result of $\hat{\alpha}_i[m+l] \cdot \hat{\alpha}_{i-1}[m]$ for two sinusoidal input signals is found. Then, the constant terms non filtered by the $\lim_{P \rightarrow \infty} \frac{1}{2P+1} \sum_{p=-P}^P \{\cdot\}$ operators (denoted $\text{DC}_P\{\cdot\}$ from now on) are signaled.

For reading convenience, we repeat the definition of the cross-correlation $r_{fg}[l]$ of two ergodic signals (4.30) :

$$r_{fg}[l] = \text{DC}_P\{f[p+l]g[p]\}.$$

If $\alpha_i[m] = x(t_{s_i}[m])$, where

$$t_{s_i}[m] = MTm - (M - 1 - i)T + t_{e_i},$$

and

$$x(t) = A_A \cos\left(\frac{\omega_A}{T}t + \phi_A\right) + A_B \cos\left(\frac{\omega_B}{T}t + \phi_B\right),$$

then $\alpha_i[m]$ is explicitly :

$$\begin{aligned} \hat{\alpha}_i[m] = & A_A \cos\left[\omega_A Mm - \omega_A(M - 1 - i) + \frac{\omega_A}{T}t_{e_i} + \phi_A\right] \\ & + A_B \cos\left[\omega_B Mm - \omega_B(M - 1 - i) + \frac{\omega_B}{T}t_{e_i} + \phi_B\right]. \end{aligned} \quad (\text{D.1})$$

The $\hat{\alpha}_i[m+l] \cdot \hat{\alpha}_{i-1}[m]$ signal is¹ :

¹This trigonometric identity has been used :

$$A \cos(a) \cdot B \cos(b) = \frac{AB}{2} [\cos(a+b) + \cos(a-b)]$$

$$\begin{aligned}
& \hat{\alpha}_i[m+l] \cdot \hat{\alpha}_{i-1}[m] = \\
& \frac{A_A^2}{2} \left\{ \cos \left[2\omega_A Mm + \omega_A Ml - 2\omega_A(M-1-i) - \omega_A + 2\frac{\omega_A}{T}t_{e_i} + 2\phi_A \right] + \right. \\
& \quad \left. \cos \left[\omega_A Ml + \omega_A + \frac{\omega_A}{T}(t_{e_i} - t_{e_{i-1}}) \right] \right\} + \\
& \frac{A_B^2}{2} \left\{ \cos \left[2\omega_B Mm + \omega_B Ml - 2\omega_B(M-1-i) - \omega_B + 2\frac{\omega_B}{T}t_{e_i} + 2\phi_B \right] + \right. \\
& \quad \left. \cos \left[\omega_B Ml + \omega_B + \frac{\omega_B}{T}(t_{e_i} - t_{e_{i-1}}) \right] \right\} + \\
& \frac{A_A A_B}{2} \left\{ \cos \left[(\omega_A + \omega_B)Mm + \omega_A Ml - \omega_A(M-1-i) - \omega_B(M-i) + \frac{\omega_A}{T}t_{e_i} + \frac{\omega_B}{T}t_{e_{i-1}} + \phi_A + \phi_B \right] + \right. \\
& \quad \left. \cos \left[(\omega_A - \omega_B)Mm + \omega_A Ml - \omega_A(M-1-i) + \omega_B(M-i) + \frac{\omega_A}{T}t_{e_i} - \frac{\omega_B}{T}t_{e_{i-1}} + \phi_A - \phi_B \right] \right\} + \\
& \frac{A_B A_A}{2} \left\{ \cos \left[(\omega_B + \omega_A)Mm + \omega_B Ml - \omega_B(M-1-i) - \omega_A(M-i) + \frac{\omega_B}{T}t_{e_i} + \frac{\omega_A}{T}t_{e_{i-1}} + \phi_B + \phi_A \right] + \right. \\
& \quad \left. \cos \left[(\omega_B - \omega_A)Mm + \omega_B Ml - \omega_B(M-1-i) + \omega_A(M-i) + \frac{\omega_B}{T}t_{e_i} - \frac{\omega_A}{T}t_{e_{i-1}} + \phi_B - \phi_A \right] \right\}.
\end{aligned}
\tag{D.2}$$

Evaluated for $l = 0$, (D.2) gives :

$$\hat{\alpha}_i[m] \cdot \hat{\alpha}_{i-1}[m] = \tag{D.3}$$

$$\cos \left[\omega_A + \frac{\omega_A}{T}(t_{e_i} - t_{e_{i-1}}) \right] + \cos \left[\omega_B + \frac{\omega_B}{T}(t_{e_i} - t_{e_{i-1}}) \right] + res_{i,i-1}[m, 0],$$

where the first, third, fifth, sixth and eighth $\cos[\cdot]$ terms in (D.2) are grouped into $res_{i,i-1}[m, l]$. The $\cos[\cdot]$ terms the arguments of which are independent of m are not filtered by $DC_m\{\cdot\}$, i.e., their contribution to the accumulated value is not zero. The first and second terms in (D.3) are independent of m and they are the ones used to write (4.54). The $res_{i,i-1}[m]$ term is in general filtered, i.e.,

$$DC_m\{res_{i,i-1}[m, 0]\} = \overline{res_{i,i-1}[0]} = 0. \tag{D.4}$$

But carefully examining (D.2), we observe that if

$$2\omega_A M = 2\pi k \text{ or,} \tag{D.5a}$$

$$2\omega_B M = 2\pi k \text{ or,} \tag{D.5b}$$

$$(\omega_A + \omega_B)M = 2\pi k \text{ or,} \tag{D.5c}$$

$$(\omega_A - \omega_B)M = 2\pi k, \tag{D.5d}$$

where $k \in \mathbb{N}$, then $res_{i,i-1}[m, 0]$ is independent of m too. Therefore, $\overline{res_{i,i-1}[0]}$ may not be zero and (4.54) may be incomplete. It suggests that there must be some kind of input signal restriction. It is formally studied in Subsection 4.4.3 for a general bandlimited signal.

Appendix E

Relative t_{step_j} Dispersion for a Binary Code

In this Appendix the mean relative t_{step_j} dispersion is inductively derived when a binary code is used in the DTBG.

For a binary code, (4.16) can be rewritten as :

$$t_{step_j} = SV \cdot R \cdot \sum_{l=0}^{DR-1} [Q_l(j+1)I_{CS_l} - Q_l(j)I_{CS_l}] = SV \cdot R \cdot \sum_{l=0}^{DR-1} D_l(j)I_{CS_l}, \quad (E.1)$$

where $D_l(j) = [Q_l(j+1) - Q_l(j)]$ and

$$I_{CS_l} = \sum_{k=0}^{2^l} I_{step_{l,k}}, \quad (E.2)$$

where $I_{step_{l,k}}$ are considered as independent variables of mean $\overline{I_{step}}$ and relative variance given by the Pelgrom model used in (4.18),

$$\frac{\sigma(I_{step})}{\overline{I_{step}}} = \frac{A_I}{\sqrt{W \cdot L}}.$$

$D_l(j) = 1$ means that 2^l basic current sources the currents of which from I_{CS_l} are turned on when DCW_i changes from j to $j+1$, $D_l(j) = -1$ means that these basic current sources are turned off, and $D_l(j) = 0$ means that they remain in their previous state.

The value of $\overline{t_{step}}$ is

$$\overline{t_{step}} = SV \cdot R \cdot \overline{I_{step}}, \quad (E.3)$$

the same than for a thermometrical code.

The relative t_{step_j} dispersion depends on j . More specifically, the dispersion depends on the total number of basic current sources that change their state when DCW_i changes from j to $j+1$. It is denoted $N_{CS}(j)$, that stands for

j	$D_2(j)$	$D_1(j)$	$D_0(j)$	$N_{CS}(j)$	DR
0	0	0	1	1	1
1	0	1	-1	3	2
2	0	0	1	1	
3	1	-1	-1	7	3
4	0	0	1	1	
5	0	1	-1	3	
6	0	0	1	1	

Table E.1: $D_2(j)$, $D_1(j)$, $D_0(j)$ and $N_{CS}(j)$ values for $DR = 1, 2$ and 3 .

Number of switched Current Sources, in table E.1. This table summarizes the values of D_l and N_{CS} when $DR = 1, 2$ and 3 for $0 \leq j \leq 2^{DR} - 2$.

The relative t_{step_j} dispersion is computed from $N_{CS}(j)$:

$$\frac{\sigma(t_{step_j})}{t_{step}} = \sqrt{N_{CS}(j)} \frac{\sigma(I_{step})}{I_{step}} = \sqrt{N_{CS}(j)} \frac{A_I}{\sqrt{W \cdot L}}. \quad (E.4)$$

From table E.1, the relative t_{step_j} dispersion can be as low as $A_I/\sqrt{W \cdot L}$, for any j even, or as high as $\sqrt{(2^{DR} - 1)}A_I/\sqrt{W \cdot L}$, for $j = 2^{DR-1} - 1$. Now, from (E.4), if j is considered an uniformly distributed discrete random variable from 0 to $2^{DR} - 2$, the mean relative t_{step} dispersion is :

$$\frac{\sigma(t_{step})}{t_{step}} = \sqrt{\sum_{j=0}^{DR-2} \frac{N_{CS}(j)}{2^{DR} - 1} \frac{A_I}{\sqrt{W \cdot L}}} \quad (E.5)$$

Observing table E.1, a pattern for $\sum_{j=0}^{DR-2} N_{CS}(j)$ can inductively be extracted. The final result is :

$$\frac{\sigma(t_{step})}{t_{step}} = \sqrt{\frac{\sum_{i=0}^{DR-1} (2^{DR-i} - 1) 2^i}{2^{DR} - 1} \frac{A_I}{\sqrt{W \cdot L}}}. \quad (E.6)$$

Appendix F

Derivation of the Short-distance Drain Current Matching Parameter

In this Appendix the short-distance relative drain current matching parameter A_I (in [m]) is derived from the short-distance relative current gain factor matching parameter A_K (in [m]) and the short-distance saturation threshold voltage matching parameter $A_{V_{TH}}$ (in [V·m]). It is done for transistors biased in saturation at a given gate-to-source voltage, denoted V_{GS} .

Let us first define these parameters and their respective matching parameters accordingly to the Pelgrom model [50]. The actual drain current I_D and its matching parameter are modeled as

$$I_D = \overline{I_D} + \Delta I_D, \quad (\text{F.1a})$$

$$\frac{\sigma(\Delta I_D)}{\overline{I_D}} = \frac{A_I}{\sqrt{W \cdot L}}, \quad (\text{F.1b})$$

where $\overline{\cdot}$ denotes the mean value operator, $\Delta \cdot$ the absolute mismatch error of zero mean on the parameter, $\sigma(\cdot)$ the standard deviation and $W \cdot L$ the transistor area. Similarly, let us assume these models for the current gain K and the saturation threshold voltage V_{TH} :

$$K = \overline{K} + \Delta K, \quad (\text{F.2a})$$

$$\frac{\sigma(\Delta K)}{\overline{K}} = \frac{A_K}{\sqrt{W \cdot L}}, \quad (\text{F.2b})$$

$$V_{TH} = \overline{V_{TH}} + \Delta V_{TH}, \quad (\text{F.3a})$$

$$\sigma(\Delta V_{TH}) = \frac{A_{V_{TH}}}{\sqrt{W \cdot L}}, \quad (\text{F.3b})$$

Now, the actual value of the drain current for a real transistor is discussed before obtaining the dependency of A_I on A_K , $A_{V_{TH}}$ and V_{GS} .

Considering fabrication dispersion, the actual saturation drain current I_D can be written as

$$I_D = \left(1 + \frac{\Delta K}{\bar{K}}\right) \bar{K} \left[V_{GS} - \bar{V}_{TH} \left(1 + \frac{\Delta V_{TH}}{\bar{V}_{TH}}\right)\right]^2. \quad (\text{F.4})$$

Let us assume that both ΔK and ΔV_{TH} are statistically independent and of zero-mean. Note that, in this case, the mean drain current \bar{I}_D of a mismatch free transistor biased in saturation can be written as

$$\bar{I}_D = \bar{K} (V_{GS} - \bar{V}_{TH})^2, \quad (\text{F.5})$$

Retaining only the first order errors, (F.4) can be rewritten as

$$I_D = \bar{I}_D \left(1 + \frac{\Delta I_D}{\bar{I}_D}\right), \quad (\text{F.6})$$

where

$$\Delta I_D \approx \frac{\Delta K}{\bar{K}} - \frac{2\Delta V_{TH}}{V_{GS} - \bar{V}_{TH}}.$$

From (F.6), the relative drain current error standard deviation, $\sigma(\Delta I_D)/\bar{I}_D$ is

$$\frac{\sigma(\Delta I_D)}{\bar{I}_D} \approx \sqrt{\frac{\sigma^2(\Delta K)}{\bar{K}} + \left(\frac{2\sigma(\Delta V_{TH})}{V_{GS} - \bar{V}_{TH}}\right)^2}. \quad (\text{F.7})$$

Applying the mismatch parameter definitions (F.2b) and (F.3b), (F.7) can be rewritten as

$$\frac{\sigma(\Delta I_D)}{\bar{I}_D} \approx \sqrt{\left(\frac{A_K}{\sqrt{W \cdot L}}\right)^2 + \left(\frac{2}{V_{GS} - \bar{V}_{TH}} \frac{A_{V_{TH}}}{\sqrt{W \cdot L}}\right)^2}. \quad (\text{F.8})$$

From (F.8) and (F.1b), we get

$$A_I \approx \sqrt{A_K^2 + \left(\frac{2A_{V_{TH}}}{V_{GS} - \bar{V}_{TH}}\right)^2}. \quad (\text{F.9})$$

Appendix G

VHDL Source Code of Interface Block

```
--  
  
-- Filename:   interface.vhd  
-- Author:    David Camarero  
-- Description:  
--   Interface between a binary coded accum  
--   and a thermometrically coded register.  
-----  
  
LIBRARY IEEE;  
USE IEEE.std_logic_1164.ALL;  
  
ENTITY interface IS  
  GENERIC( M_channels : NATURAL);  
  PORT(    Sampling_CLK: IN  STD_LOGIC;  
         N_RESET      : IN  STD_LOGIC;  
         CARRY        : IN  STD_LOGIC;  
         MSB          : IN  STD_LOGIC;  
         LF_RG_i      : OUT STD_LOGIC;  
         CLK_i        : OUT STD_LOGIC  
        );  
END interface;  
  
ARCHITECTURE arch OF interface IS  
  BEGIN  
    PROCESS(Sampling_CLK, N_RESET)  
      VARIABLE tx_counter:INTEGER RANGE -1 TO +1;  
      VARIABLE effective_tx:INTEGER RANGE -1 TO +1;  
      VARIABLE time_counter: NATURAL RANGE 0 TO M_channels-1;  
      BEGIN  
        IF N_RESET='0' THEN -- resetting all variables and signals  
          time_counter:=0;  
          tx_counter:=0;  
        END IF;  
      END PROCESS;  
    END ARCHITECTURE arch;
```

```

        effective_tx:=0;
        LF_RG_i<='0';
        CLK_i<='0';
ELSIF rising_edge(Sampling_CLK) THEN
    -- increasing time_counter
    time_counter:=(time_counter+1)MOD(M_channels);
    -- setting next_com
    IF time_counter=0 THEN
        effective_tx:=tx_counter; -- updating effective_tx
        tx_counter:=0;
    END IF;
    IF CARRY='1' THEN
        IF MSB='1' THEN
            tx_counter:=tx_counter-1;
        ELSIF MSB='0' THEN
            tx_counter:=tx_counter+1;
        END IF;
    END IF;
    -- applying effective_tx
    IF time_counter=0 THEN
        IF effective_tx=1 THEN -- LF_RG_i updating
            LF_RG_i<='0';
        ELSIF effective_tx=-1 THEN
            LF_RG_i<='1';
        END IF;
        CLK_i<='0'; -- resetting CLK_i (M_channels=2 case)
    ELSIF time_counter=1 THEN -- CLK_i updating
        IF effective_tx/=0 THEN
            CLK_i<='1';
        END IF;
    ELSE
        CLK_i<='0'; -- resetting CLK_i (M_channels>2 cases)
    END IF;
END IF;
END PROCESS;
END arch;
--

```

Appendix H

Scilab Source Code for Measurements

H.1 $|t_{step}|$ Measure Source Code

```
//This Scilab script performs one measure of t_step.

//Headers
exec(home+"/Scilab/scilab-3.1.1/mylib/spectral_estimation.sci");
exec(home + "/Scilab/scilab-3.1.1/mylib/ReadSamples_RS232/loader.sce");
exec(home + "/Scilab/scilab-3.1.1/mylib/Write_RS232/loader.sce");

//defining commands from the PC to the FPGA
//The following integer numbers are interpreted by the FPGA
D_ADQUI_COM = 0; //data acquisition command
LF_COM=1; //this command sets a new t_cal
//(it turns off N_steps correction cells)
RG_COM=2; //this command sets a new t_cal
//(it turns on N_steps correction cells)

//ONE MEASURE parameters
DATA_TYPE = "signed";
DATA_WIDTH = 8;
N_FFT= 2^12;
fin=1.4376179e6;
N_meas=100;
N_steps=100;

//declaring variables
y=[]; //read samples
y_gc=[]; //gain-mismatch free samples

meas_counter=0;
for meas_counter=1:N_meas
    //extracting t_e_A
```

```

//-----
//sending RG_COM command
//this command sets a new t_cal
//(it turns on N_steps correction cells)
Write_RS232(RG_COM);
//sending D_ADQUI_COM command
//this command stores ans sent to be read N_FFT samples
Write_RS232(D_ADQUI_COM);
//reading samples
y = ReadSamples_RS232(DATA_TYPE, DATA_WIDTH, N_FFT);
//foreground gain correction
gain_mismatch = sqrt( sum( y(1:2:N_FFT)^2 )/sum( y(2:2:N_FFT)^2 ) );
y_gc(1:2:N_FFT) = y(1:2:N_FFT);
y_gc(2:2:N_FFT) = gain_mismatch*y(2:2:N_FFT);
//fft analysis
SFDR_lin_A(meas_counter) = spectral_estimation(y_gc);
//estimating t_e_A from SFDR_lin_1
t_e_A(meas_counter) = atan(1/sqrt(SFDR_lin_A(meas_counter)))/(pi*fin);

//extracting t_e_B
//-----
//sending LF_COM command
//this command sets a new t_cal
//(it turns off N_steps correction cells)
Write_RS232(LF_COM);
//sending D_ADQUI_COM command
//this command stores ans sent to be read N_FFT samples
Write_RS232(D_ADQUI_COM);
//reading samples
y = ReadSamples_RS232(DATA_TYPE, DATA_WIDTH, N_FFT);
//foreground gain correction
gain_mismatch = sqrt( sum( y(1:2:N_FFT)^2 )/sum( y(2:2:N_FFT)^2 ) );
y_gc(1:2:N_FFT) = y(1:2:N_FFT);
y_gc(2:2:N_FFT) = gain_mismatch*y(2:2:N_FFT);
//fft analysis
SFDR_lin_B(meas_counter) = spectral_estimation(y_gc);
//estimating t_e_B from SFDR_lin_B
t_e_B(meas_counter) = atan(1/sqrt(SFDR_lin_B(meas_counter)))/(pi*fin);

end

//computing statistics
inst_t_step(1:N_meas) = (1/N_steps)*(t_e_A(1:N_meas) - t_e_B(1:N_meas));
mean_t_step = mean(inst_t_step);
stdev_t_step = (1/sqrt(N_meas))*stdev(inst_t_step);

//printing results
mprintf("\n\n");
mprintf("mean_t_step=%.2e\n",mean_t_step);
mprintf("stdev_t_step =%.2e\n", stdev_t_step);

```

H.2 $|t_{step}|$ Histogram Source Code

```
//This Scilab script performs a histogram of t_step.

//Headers
exec(home+"/Scilab/scilab-3.1.1/mylib/spectral_estimation.sci");
exec(home + "/Scilab/scilab-3.1.1/mylib/ReadSamples_RS232/loader.sce");
exec(home + "/Scilab/scilab-3.1.1/mylib/Write_RS232/loader.sce");

//HISTOGRAM parameters
N_hist = 150;
N_clas_t_step_hist = 7;
N_clas_std_hist = N_clas_t_step_hist;

//declaring variables
y=[]; //read samples
y_gc=[]; //gain-mismatch free samples

//HISTOGRAM loop
for N_hist_counter =1:N_hist
    mprintf("\nN_hist_counter=%d of %d\n",N_hist_counter, N_hist);
    //t_step MEASURE SCRIPT
    exec("t_step_measure.sce"); //see t_step measure source code appendix
    mean_t_step_hist(N_hist_counter) = mean_t_step ;
    stdev_t_step_hist(N_hist_counter) = stdev_t_step ;
end

xset("window",0)
xtitle("histogram mean_t_step ");
histplot(N_clas_t_step_hist,mean_t_step_hist, normalization=%f);

xset("window",1)
xtitle("histogram stdev_t_step ");
histplot(N_clas_std_hist,stdev_t_step_hist, normalization=%f);
```


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