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Architecture and design of a reconfigurable RF  
sampling receiver for multistandard applications

Anis LATIRI



To the memory of my father . . .



# Remerciements

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# Abstract

The fast development of wireless communication systems requires more flexible and cost effective radio architectures. A long term goal is the software defined radio, where communication standards are chosen by reconfiguration of hardware. Direct analog to digital conversion of the radio frequency (RF) signal is still unrealistic at present time, due to the high requirements imposed on the analog to digital converter. This motivates the need for a highly flexible RF analog front-end that can be fully integrated in low cost digital deep-submicron CMOS processes.

Different techniques for shifting the RF and analog circuit design complexity to digitally intensive domain were developed recently. These techniques are based on direct RF sampling and discrete-time analog signal processing and allow for a great flexibility and reduction of cost and power consumption in a reconfigurable design environment.

These concepts have been used in this thesis to develop a reconfigurable discrete-time radio receiver front-end. The circuit, which consists mainly of a transconductance low noise amplifier and two discrete-time analog signal processing stages, performs RF sampling, anti-alias filtering, frequency downconversion, decimation and lowpass filtering.

To validate the flexibility and reconfigurability of the receiver, GSM and 802.11g communication standards have been addressed and adopted during system level study. The frequency plan and filtering scheme decided for each standard were made different to fully analyze and validate the flexibility of the architecture. The circuit has been designed in 90nm CMOS technology and first measurement results demonstrated the functionality of the receiver.

Additionally, a fully passive 2<sup>nd</sup> order discrete-time sinc type anti-alias filter has been described and included in the proposed receiver. Based on capacitive ratios for coefficient weighting, this filter is intended to considerably improve the alias filter rejection, which is one of the major problems reported in present discrete-time receivers. By changing the input sampling rate, the anti-alias filter can be tuned to different RF frequency bands and is hence suitable for true multi-standard operations.

**Keywords:** radio receivers, multi-standard, RF sampling, discrete time, analog signal processing, anti-aliasing filter



# Résumé étendu

## Introduction

Le développement rapide des communications sans fil et l'émergence de nouveaux standards ont sollicité la demande pour des récepteurs radio multi-modes à faible coût. Pour des applications mobiles, un haut niveau d'intégration, une grande flexibilité et une faible consommation sont les principales données à respecter. Parmi les approches possibles pour le multi-standards, on retrouve la solution Software Defined Radio (SDR), qui consiste à concevoir une chaîne de réception qui soit totalement reconfigurable par logiciel. Au passage d'un schéma de réception radio classique vers une architecture SDR, la majorité du traitement du signal effectué au niveau de la chaîne de réception est translatée en numérique, ce qui impose des contraintes beaucoup plus sévères sur le convertisseur ADC (large bande, dynamique et taux d'échantillonnage assez élevés). La consommation excessive qui en résulte rend impossible l'implémentation du SDR dans les téléphones mobiles.

Des techniques de traitement du signal analogique à temps discret (basées notamment sur les capacités commutées) peuvent être utilisées ici afin d'alléger les contraintes imposées sur l'ADC. De plus, ce type de traitement présente l'avantage d'être flexible et parfaitement reprogrammable. D'un autre côté, l'évolution de la technologie submicronique permet désormais d'échantillonner directement les signaux en bande RF. En combinant l'échantillonnage RF au traitement du signal analogique temps discret, il est alors possible d'obtenir un récepteur radio adapté au multi-standards et à la software radio de façon plus générale. Dans cette perspective, le signal RF reçu à l'antenne serait amplifié, échantillonné puis traité de façon analogique temps discret, avant d'être finalement numérisé par l'ADC. Ce type de récepteur nécessite cependant un filtrage anti-alias avant échantillonnage qui doit être à la fois performant et totalement reconfigurable.

Cette thèse a deux objectifs bien spécifiques. Le premier est de proposer une architecture reconfigurable pour un récepteur multi-standards, basée sur l'échantillonnage passe-bande RF et sur le traitement de signal analogique à temps discret. Bien que plusieurs réalisations de tels récepteurs aient été déjà rapportées, peu d'entre elles ont essayé d'adresser différentes normes de communication afin de valider réellement l'aspect reconfigurabilité. Dans le travail de thèse, les normes GSM900 et 802.11g (qui présentent des caractéristiques assez différentes) ont été choisies comme références pour valider les mécanismes de reconfiguration et par conséquent la reprogrammabilité du récepteur.

Le deuxième objectif de cette thèse est d'étudier et proposer de nouvelles structures de filtrage anti-alias d'ordres élevés. Un filtre en peigne de second

ordre entièrement passif a été analysé et implémenté dans le récepteur proposé. Ce filtre se présente comme un filtre FIR à temps discret dont les coefficients sont implémentés à l'aide de rapports capacitifs. Il permet d'améliorer la réjection d'alias sans surcoût de consommation et présente l'avantage d'être totalement reconfigurable.

## Architecture du récepteur

Le récepteur proposé repose sur une architecture assez semblable à celles des radios à temps discret décrites dans la littérature. Cependant, il est supposé atteindre de meilleures performances en terme de réjection d'alias (grâce au filtre en peigne de second ordre) et permet d'implémenter deux modes de communication différents.

L'architecture du récepteur est représentée Figure 1. Elle comporte un filtre RF, un amplificateur faible bruit à transconductance (LNTA), deux étages de traitement de signal analogique à temps discret (DTASP) et deux convertisseurs analogique numérique.

Le signal d'entrée RF est d'abord filtré, amplifié et converti en courant. Il est ensuite traité par un premier étage analogique à temps discret, où il subit des opérations de filtrage IIR/FIR et une translation en fréquences vers une première fréquence intermédiaire. Un deuxième étage de traitement permet de réduire la fréquence d'échantillonnage et de filtrer le signal à fréquence intermédiaire avant la conversion analogique numérique.

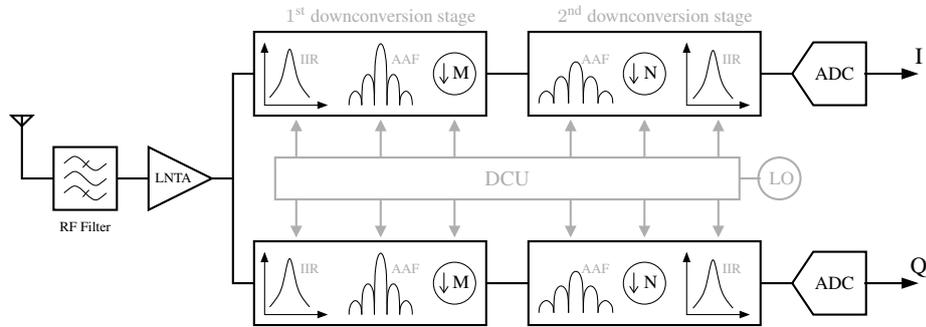


Figure 1. Architecture du récepteur à échantillonnage RF

Le courant en sortie du LNTA est intégré pendant une période  $\frac{1}{4F_c}$  ( $F_c$  étant la fréquence du canal RF) à travers une capacité histoire (formant le filtre IIR) et une capacité unitaire (appartenant au filtre anti-repliement) de façon continue et commutée entre les voies en quadrature I et Q. Il en résulte un flux d'échantillons temps discret à une fréquence  $2F_c$  par voie I/Q.

Le filtrage IIR, réalisé par un simple pôle, est nécessaire en sortie du LNTA afin d'éviter toute saturation en présence d'éventuels signaux bloqueurs. Le second étage permet ensuite de réduire le taux d'échantillonnage (décimation) tout en évitant le repliement des signaux adjacents (filtre FIR) et d'apporter le filtrage canal nécessaire (IIR) afin de respecter la dynamique d'entrée de l'ADC.

## Plan de fréquences

Le plan de fréquence utilisé en mode GSM est donné Figure 2. Le signal utile est toujours centré à la moitié de la fréquence d'échantillonnage (récepteur en  $F_s/2$ ) afin d'éviter les dégradations liées au bruit en  $1/f$  et aux produits d'intermodulation d'ordre 2.

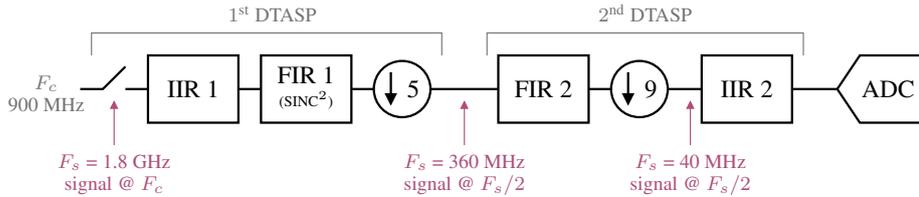


Figure 2. Plan de fréquences en mode GSM

Le premier rapport de décimation est imposé par le filtrage anti-repliement, la réjection étant directement proportionnelle au rapport de la bande passante par la fréquence d'échantillonnage. Dans le cas du GSM, il a été décidé de réduire la fréquence d'échantillonnage à 360 MHz en sortie du premier étage de traitement analogique, soit un rapport de décimation  $M_1$  égal à 5.

Le second étage doit adapter le taux d'échantillonnage à la fréquence de fonctionnement de l'ADC, soit 40 MHz. Le deuxième rapport de décimation  $M_2$  a donc été fixé à 9, le signal utile se retrouvant ainsi en sortie à une fréquence de 20 MHz.

Le plan de fréquence utilisé en mode 802.11g est donné Figure 3. Le signal utile s'étalant sur plus de 10 MHz de bande passante, le bruit en  $1/f$  devient alors moins significatif. L'architecture en  $F_s/2$  ne présente plus de réels intérêts et il devient donc envisageable de traduire le signal directement en bande de base.

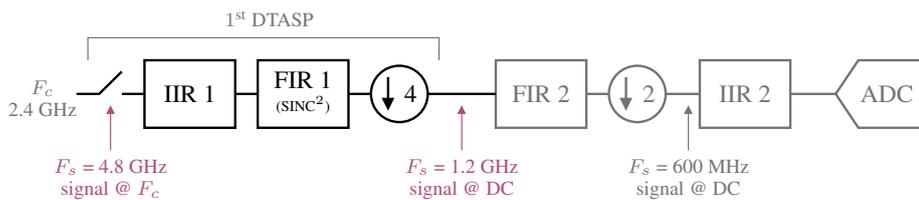


Figure 3. Plan de fréquences en mode 802.11g

Le signal RF est tout d'abord échantillonné à la fréquence  $2F_c$  (de façon similaire au mode GSM). Les filtres IIR et anti-alias du premier étage restent centrés autour du canal RF (schéma en  $F_s/2$ ). Le signal est ensuite traduit en bande de base par l'utilisation d'un facteur de décimation pair ( $M_1 = 4$ ).

Le deuxième étage de traitement analogique à temps discret (non implémenté dans le circuit actuel) réalise une seconde série de filtrages IIR/FIR ainsi qu'une décimation par 2 afin de conditionner le signal et permettre sa numérisation par un convertisseur analogique numérique dédié.

## Filtre anti-repliement

Le filtrage anti-repliement réalisé en tout début de chaîne de conversion doit être centré sur la fréquence canal  $F_c$  et présenter des zéros de transmission aux fréquences des alias situés à  $F_c \pm kF_s$ . En traitement de signal numérique, il est possible de réaliser facilement des filtres passe bande si la fréquence centrale est la moitié de la fréquence d'échantillonnage ( $F_s/2$ ). Ceci explique la raison pour laquelle le signal RF est échantillonné à la fréquence  $2F_c$  en tout début de chaîne.

Les coefficients du filtre anti-repliement de second ordre proposé ici ont été calculés à partir de la fonction de transfert d'un filtre en peigne (moyenne glissante) de longueur égale au rapport de décimation  $M = 2F_c/F_s$ . En élevant au carré la fonction de transfert puis en effectuant une transformation passe bas vers passe haut ( $z^{-1} \rightarrow -z^{-1}$ ), on obtient les coefficients d'un filtre de second ordre centré en  $F_c$  et ayant des zéros de transmission tous les  $kF_s$ . La fonction de transfert du filtre anti-repliement est donnée par :

$$H(z) = \mathcal{T}_{L \rightarrow H} \left( \sum_{k=0}^{M-1} z^{-k} \right)^2 = \left( \sum_{k=0}^{M-1} (-1)^k z^{-k} \right)^2$$

Les coefficients qui en découlent sont donnés dans le Tableau 1 pour les deux modes de fonctionnement (GSM et 802.11g). Notons que la longueur du filtre est égale à  $2M$  (ce qui équivaut à une durée de traitement égale à  $2T_s$ ) et qu'il faut donc disposer de deux chaînes d'intégration en parallèle afin de conserver un taux d'échantillonnage égal à  $1/T_s$ .

mode	↓ M ratio	FIR coefficients
GSM	5	[+1 -2 +3 -4 +5 -4 +3 -2 +1 0]
WIFI	4	[+1 -2 +3 -4 +3 -2 +1 0]

Tableau 1. Coefficients du filtre FIR en modes GSM et 802.11g

Les coefficients du filtre sont implémentés au niveau circuit en utilisant une technique de division de charges passive. Chaque coefficient se voit affecter un vecteur de  $M$  capacités unitaires. Le courant d'entrée est d'abord intégré sur le vecteur entier durant une période  $T_i = T_c/4$ . Afin de réaliser le  $k^{eme}$  coefficient, on vient ensuite prélever la charge stockée uniquement sur  $k$  capacités unitaires du vecteur, réalisant ainsi une fraction  $|\alpha_k| = k/M$  de la charge initialement intégrée. Le signe et la partie complexe de chaque coefficient sont formés ultérieurement lors de la connexion des  $k$  capacités vers la sortie du filtre (connexion directe ou inversée vers une des deux voies en quadrature). La division de charges est présentée Figure 4 pour le mode GSM, où l'implémentation des coefficients du filtre anti-repliement nécessite un vecteur de 5 capacités unitaires par coefficient.

Une structure à trois voies parallèles à entrelacement temporel a été utilisée afin de conserver un taux d'échantillonnage égal à  $1/T_s$  en sortie du filtre anti-alias (cf. Figure 5 pour le mode GSM). A un instant  $t$  donné, deux voies sont connectées en entrée et intègrent le courant d'entrée, tandis que la troisième voie est connectée en sortie pour la lecture de la charge puis est réinitialisée. La complémentarité entre les coefficients des voies parallèles permet d'utiliser le

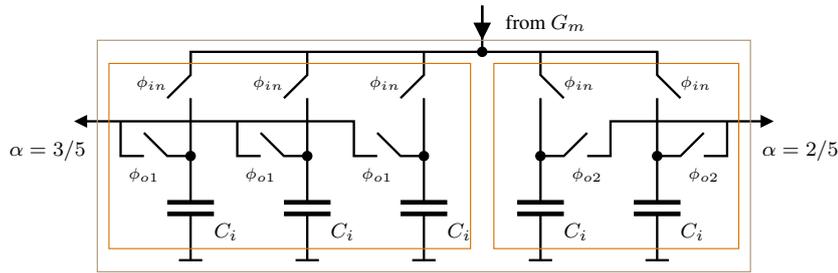


Figure 4. Implémentation des coefficients par division de charges

même vecteur de  $M$  capacités unitaires pour la réalisation de deux coefficients différents, réalisant ainsi un gain considérable en surface et en nombre de signaux de commande.

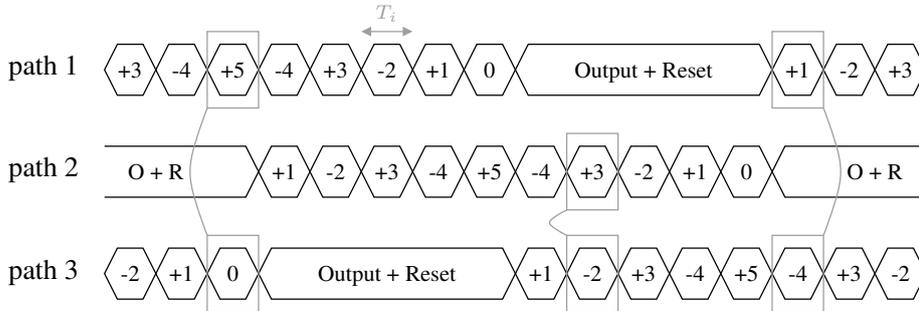


Figure 5. Voies d'intégrations parallèles en mode GSM

Les performances du filtre anti-repliement proposé sont limitées uniquement par les disparités capacitatives (mismatch inhérent à la technologie utilisée). Pour des disparités de l'ordre de  $\sigma(\Delta C/C) = 0.1\%$ , la profondeur des zéros de transmission est limitée à 75 dB, soit la moitié de la réjection calculée théoriquement. Les performances du filtre proposé restent néanmoins meilleures à celles d'un simple filtre anti-alias d'ordre un. Notons également que la complexité liée à la structure du filtre croît en fonction du nombre et des valeurs des coefficients à implémenter. Le nombre de signaux de commande nécessaires augmente la consommation du bloc numérique responsable de la génération des phases d'horloge, ainsi que la pollution générée par la commutation signaux de commande dans les parties analogiques sensibles du circuit.

## Étude système du récepteur

L'étude système du récepteur proposé s'est limitée à la spécification et la répartition des gains, bruits et filtrages le long de la chaîne de réception. L'amplificateur faible bruit LNTA étant le seul bloc actif du récepteur, le bruit rajouté par les blocs en amont doit être le plus bas possible. Notamment, la perte de gain liée aux capacités parasites et au moyennage passif des charges devront être minimisés. Le filtrage nécessaire est principalement dicté par les dynamiques en sortie du LNTA et à l'entrée du convertisseur analogique numérique. Ce filtrage

se traduit au niveau circuit par les valeurs des capacités histoires des filtres IIR, une fois la valeur des capacités unitaires fixée.

Une analyse nodale a été effectuée sur un circuit simplifié représentant le premier étage de traitement analogique à temps discret (Figure 6). Cette analyse a permis d'obtenir les tensions aux bornes des capacités rotatives et histoires (avec un gain de temps considérable par rapport à des simulations électriques standards) et d'en déduire les valeurs réelles des gains et filtrages IIR pour des valeurs de capacités données.

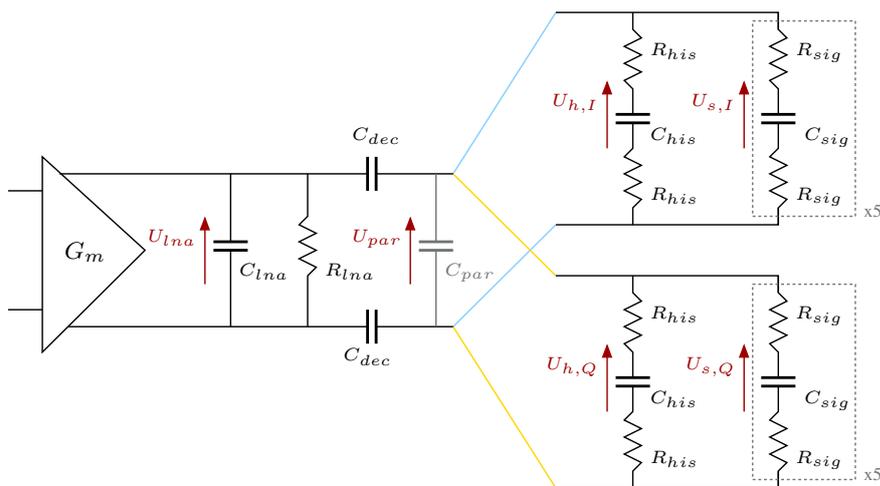


Figure 6. Schéma électrique utilisé lors de l'étude système

La contribution en bruit thermique des deux étages de traitement analogique à temps discret a été minutieusement calculée et a permis d'extraire les valeurs des capacités unitaires et rotatives des filtres FIR anti-repliement. Les gains et bruits des différents étages de la chaîne de réception sont résumés dans le Tableau 2 pour le mode GSM et permettent d'estimer la valeur de la sensibilité que pourra atteindre le récepteur ( $-102\text{dBm}$  en GSM900, soit le minimum requis par la norme).

		ANTENNA	SWITCH	SAW	LNTA	SINC2	FIR2/IIR2	ADC
Noise Figure	dB	0.0	1.0	2.8	2.5			
Noise Contribution	$V^2$					1.27E-11	8.89E-11	1.99E-10
Power Gain	dB	0.0	-1.0	-2.8				
Voltage Gain	dB				24.4	-2.28	0.0	0.0
Output Signal Level	dBm	-102.0	-103.0	-105.8				
	dBVrms				-81.4	-83.7	-83.7	-83.7
Output Noise Level	dBm	-121.0	-121.0	-121.0				
	dBVrms				-94.1	-96.1	-94.8	-92.7
SNR	dB	19.0	18.0	15.2	12.7	12.5	11.1	9.1

Tableau 2. Contributions gain/bruit des blocs en mode GSM

Au final, l'étude système permet de déterminer le nombre et les valeurs des capacités (unitaires et histoires), ainsi que les valeurs des résistances des switches utilisés dans les étages analogiques. Ces valeurs sont reprises par la suite lors de la conception du récepteur au niveau circuit.

## Conception du circuit

Le front-end RF a été conçu en technologie STMicroelectronics CMOS 90nm et comprend, comme détaillé précédemment, un amplificateur faible bruit à transconductance (LNNTA), deux étages de traitement analogique à temps discret (DTASP), deux convertisseurs analogiques numériques, ainsi qu'un bloc numérique pour la génération des phases d'horloge (DCU). Un grand soin a été apporté au dessin des masques (*layout*) et particulièrement à celui des capacités unitaires et histoires, afin d'assurer de bonnes performances en terme de filtrage anti-repliement en dépit des disparités technologiques qui peuvent exister.

### LNA à transconductance

L'amplificateur faible bruit à sortie courant est représenté Figure 7. Il est constitué principalement d'un étage à transconductance suivi d'un étage de sortie cascode.

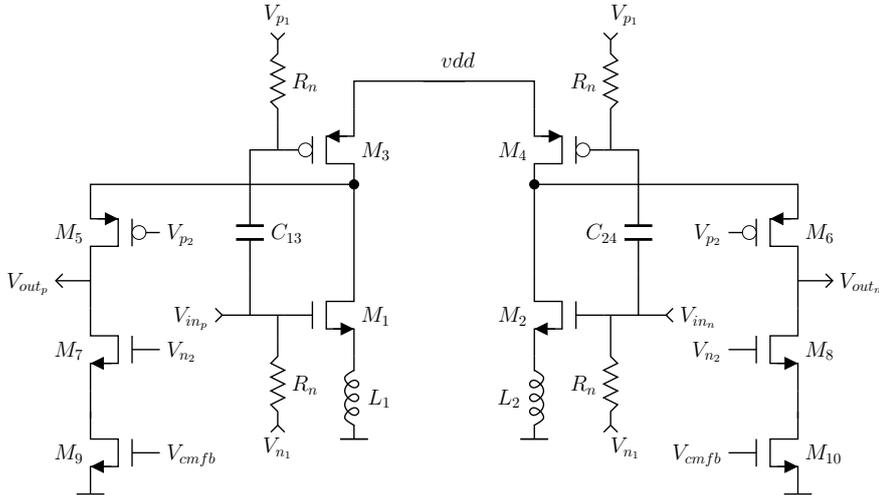


Figure 7. Schéma électrique du LNA à transconductance

La transconductance est réalisée à l'aide de deux paires différentielles NMOS ( $M_1, M_2$ ) et PMOS ( $M_3, M_4$ ). Les inductances  $L_1$  et  $L_2$  assurent une partie de l'adaptation d'impédance en entrée, le reste étant réalisé en éléments discrets sur la carte de test. Un étage double cascode, constitué des transistors  $M_5 - 8$ , est utilisé afin d'augmenter l'impédance de sortie du LNNTA. Notons que la capacité parasite due à ces mêmes transistors résulte en une perte de gain non négligeable, posant un problème de conception et un compromis entre impédance et capacité parasite en sortie du bloc LNNTA.

### Premier étage DTASP

Le premier étage de traitement analogique à temps discret comprend un filtre IIR en sortie de l'amplificateur faible bruit à transconductance, ainsi que le filtre anti-repliement en peigne d'ordre deux. Des mécanismes de reconfiguration ont

été rajoutés au niveau circuit afin d'adapter la structure des filtres et les valeurs des capacités histoires utilisées au mode de fonctionnement du récepteur.

### Filtre IIR

Le filtre IIR du premier étage analogique est constitué principalement d'une capacité histoire et de quatre switches (cf. Figure 8). Le filtre est identique pour les deux voies en quadrature I/Q, à l'exception des signaux de commande qui sont déphasés de  $\pi/2$ . Les deux filtres IIR sont connectés aux nœuds communs  $dec_P$  et  $dec_N$  en sortie du LNTA (après les capacités de découplage).

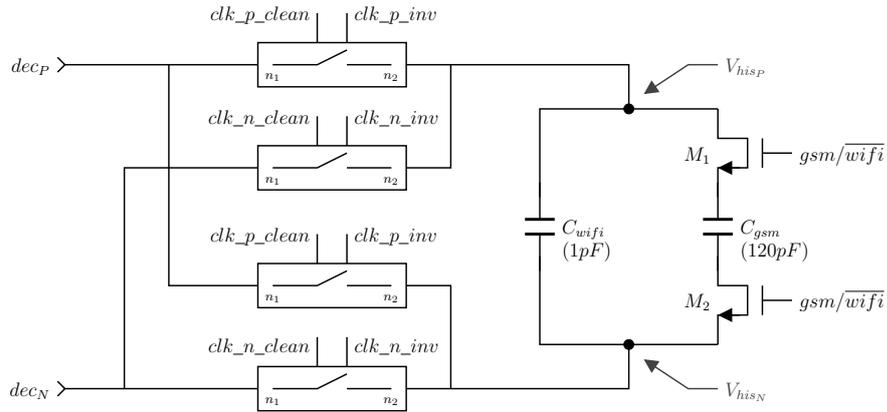


Figure 8. Schéma du premier filtre IIR (voie I)

Les switches sont cadencés de sorte à ce que chaque capacité histoire est retournée à une fréquence  $2F_c$ . La structure différentielle du filtre et l'utilisation de transistors factices (pour la réalisation des switches) permettent de minimiser la dégradation liée aux phénomènes d'injection de charges et de propagation des phases d'horloge.

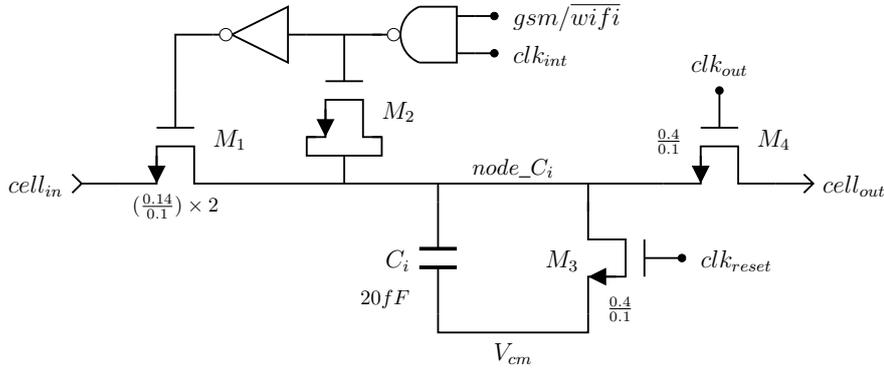
La valeur de la capacité histoire est contrôlée par le signal de commande  $gsm/wifi$  qui permet d'ajuster la réjection du filtre IIR en fonction du mode de fonctionnement du récepteur.

### Filtre anti-repliement

Comme décrit précédemment, les coefficients entiers du filtre anti-repliement ont été implémentés au niveau circuit à l'aide de rapports capacitifs. En suivant une approche hiérarchique, le filtre peut être vu comme une combinaison de trois bancs de capacités, chacun composé de  $L$  cellules de coefficients, chacune d'elles étant composée de  $L$  cellules unitaires.

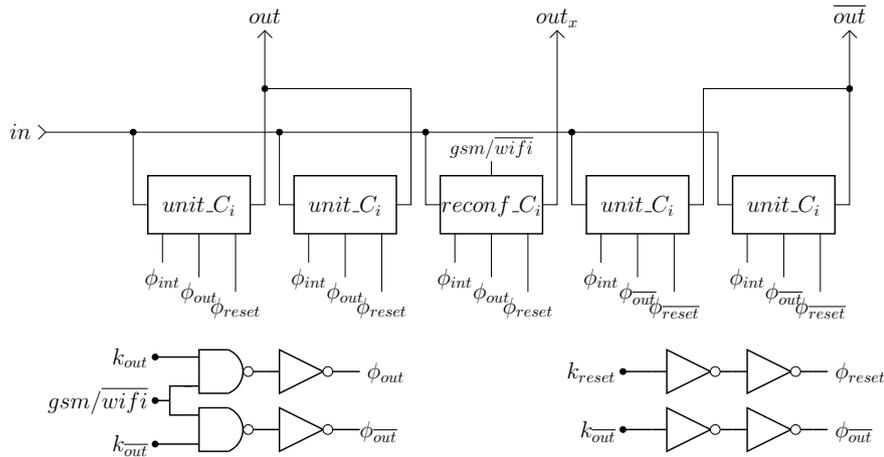
Le filtre anti-repliement a été dimensionné au tout début pour le mode GSM. Puis, des mécanismes de reconfiguration ont été rajoutés pour adapter la structure au mode 802.11g. Notons qu'il est possible d'adapter le filtre à d'autres standards de communication, mais la complexité de mise en œuvre et le nombre de signaux de contrôle augmenteraient de façon drastique.

Le schéma électrique d'une cellule unitaire reconfigurable est donné Figure 9. Chaque cellule est composée d'une capacité  $C_i$  et de trois switches correspondant aux phases d'intégration, de réinitialisation et de lecture de la charge stockée.

Figure 9. Cellule unitaire reconfigurable du filtre SINC<sup>2</sup>

La valeur de la capacité unitaire a été calculée lors de l'étude système et permet d'obtenir le meilleur rapport gain/bruit du premier étage de traitement analogique. Les transistors des switches ont été dimensionnés en fonction de la résistance  $R_{sig}$  calculée également lors de l'étude système. Des transistors factices sont rajoutés afin de minimiser l'injection des charges sur la capacité unitaire  $C_i$ . La commande du switch d'intégration est contrôlée par le bit de reconfiguration  $gsm/\overline{wifi}$  et permet d'activer ou non la cellule unitaire en fonction du mode de communication choisi.

Les cellules unitaires sont organisées ensuite en cellules de coefficients, dont le schéma de principe est donné en Figure 10. Chaque coefficient est composé de  $L$  cellules unitaires ( $L = 5$  en mode GSM) partageant une même entrée. Trois connexions différentes sont possibles en sortie, selon si le coefficient garde le même signe (positif ou négatif) ou change de signe en fonction du mode de fonctionnement. Les connexions en sortie sont également gérées à ce niveau par le bit de contrôle  $gsm/\overline{wifi}$ .

Figure 10. Coefficient reconfigurable du filtre SINC<sup>2</sup>

Au niveau hiérarchique supérieur, trois de bancs de capacités sont formés par

voie I/Q, chacun de ces bancs étant constitués de  $2L$  cellules de coefficients dont les connexions en entrée et sortie sont paramétrables. Le filtre anti-repliement  $\text{SINC}^2$  est relié au deuxième étage de traitement analogique uniquement en mode GSM. En mode 802.11g, un filtrage IIR à simple pôle est rajouté en sortie du filtre anti-repliement et le signal est ensuite amplifié puis connecté à une sortie du circuit.

## Deuxième étage DTASP

A l'image du premier étage de traitement analogique, le deuxième étage DTASP comprend un filtre FIR réalisant un filtrage anti-repliement et une décimation, ainsi qu'un filtre IIR réalisant une partie du filtrage canal. Le deuxième filtre FIR est moins complexe que le filtre  $\text{SINC}^2$ , puisqu'il s'agit d'implémenter des coefficients unitaires sous la forme  $[+1 -1 +1 -1]$ . La cellule unitaire utilisée à ce niveau est représentée Figure 11.

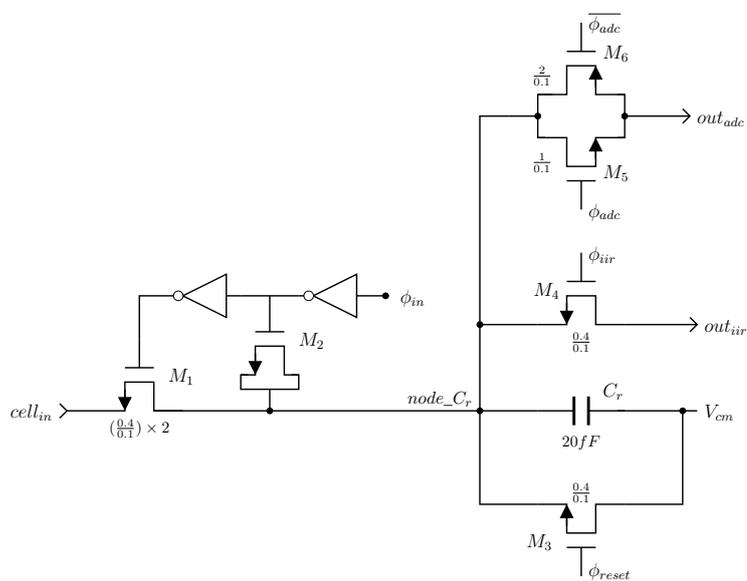


Figure 11. Cellule unitaire du filtre FIR du second DTASP

Chaque capacité unitaire est connectée à l'entrée du filtre FIR, puis à la capacité histoire du filtre IIR, puis à l'entrée de l'ADC et est enfin réinitialisée avant le début de la phase suivante. La valeur de la capacité a été calculée lors de l'étude système (compromis entre perte de gain et bruit). Les résistances des divers switches dépendent du temps alloué à chaque sous phase et de la constante de temps RC liée au transfert des charges.

## Convertisseur analogique numérique

Le modulateur  $\Sigma\Delta$  utilisé en mode GSM pour la conversion du signal  $F_s/2$  en fin de chaîne est représenté Figure 12. Le modulateur utilise un filtre de boucle passe haut de second ordre à capacités commutées ainsi qu'un quantificateur à

3 niveaux, et permet d'atteindre une résolution théorique de 12 bits pour une pleine échelle de 0.2 Vpp en différentiel.

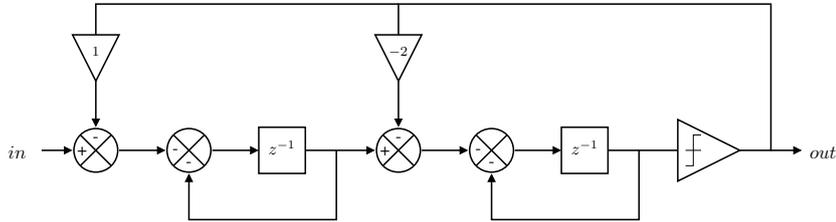


Figure 12. Architecture du modulateur  $\Sigma\Delta$  utilisé en mode GSM

## Layout du circuit intégré

Le dessin des masques du filtre anti-repliement a été étudié avec attention afin de limiter les effets des disparités technologiques sur les performances en termes de filtrage. Il a été démontré que l'appariement des capacités unitaires était nécessaire uniquement au niveau des cellules de coefficient, et non pas au niveau du filtre global.

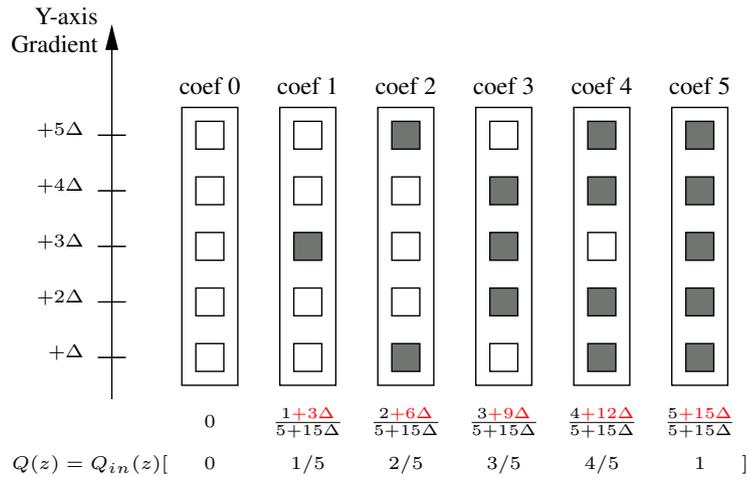


Figure 13. Annulation du gradient au niveau des coefficients du filtre  $SINC^2$

Le placement des capacités unitaires a donc été réalisé de sorte à annuler tout gradient linéaire pouvant avoir lieu suivant un axe horizontal ou vertical, comme le montre la Figure 13. Notons également que l'annulation des gradients a été également étudiée au niveau supérieur du filtre anti-repliement, à travers un placement optimal des cellules de coefficients le long de l'axe horizontal.

## Résultats de mesures

Le front-end RF du récepteur double mode proposé, dont une microphotographie est donnée Figure 14, a été implémenté et fabriqué en technologie

standard STMicroelectronics CMOS 90nm. La surface de la partie active du circuit est de  $0.91\text{mm}^2$  et celle du circuit entier est de  $2.5\text{mm}^2$ . Le circuit a été encapsulé dans un boîtier TQFP44L 44 broches.

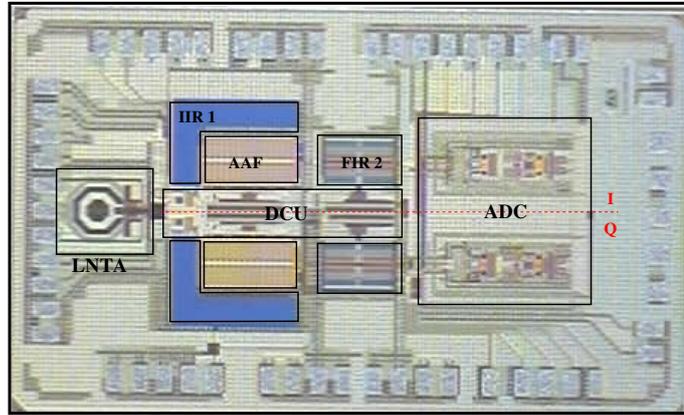


Figure 14. Microphotographie du récepteur RF proposé

La carte d'évaluation utilisée pour le test du circuit prototype est représentée Figure 15. Le signal RF d'entrée est d'abord divisé par un coupleur  $0^\circ - 180^\circ$ , puis acheminé vers les entrées différentielles du LNTA. Un réseau LC est utilisé pour affiner l'adaptation d'impédance. Un second signal RF, à une fréquence  $4F_c$ , est connecté à l'entrée horloge CLK du récepteur. Le mode de fonctionnement du circuit est contrôlé par un signal logique *gsm/wifi*.

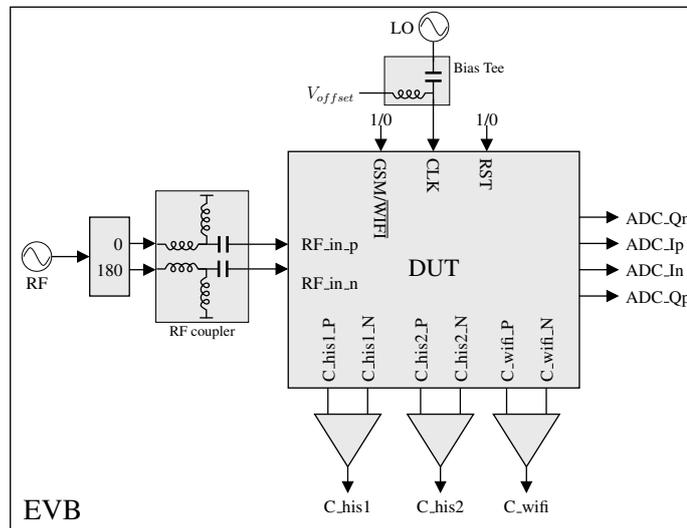


Figure 15. Schéma de la carte d'évaluation

L'évaluation des étages de traitement analogiques à temps discret est rendue possible grâce aux signaux suivants :

- $V_{his1,P}$  et  $V_{his1,N}$  : tension différentielle aux bornes de la capacité histoire du premier filtre IIR (voie I), disponible dans les deux modes GSM/802.11g
- $V_{his2,P}$  et  $V_{his2,N}$  : tension différentielle aux bornes de la capacité histoire du second filtre IIR (voie I), disponible uniquement en mode GSM
- $V_{wifi,P}$  et  $V_{wifi,N}$  : tension différentielle en sortie du filtre anti-repliement (voie I), disponible uniquement en mode 802.11g

Ces signaux sont analysés à l'aide d'oscilloscopes et/ou d'analyseurs de spectre. Les sorties numériques du modulateur  $\Sigma\Delta$  sont analysées à l'aide d'un analyseur logique et sont également utilisées pour l'évaluation de la chaîne de réception entière.

Le plan de test suivant a été adopté pour la validation du fonctionnement et la mesure des performances du front-end RF proposé. Toutes les mesures ont été effectuées en mode GSM puis en mode 802.11g.

1. Phase de débogage
2. Mesure de la consommation électrique
3. Gain du circuit en fonction de la fréquence/puissance du signal d'entrée
4. Réjection des filtres IIR & du filtre anti-repliement

La première série de mesures effectuées sur le circuit ont prouvé le bon fonctionnement du récepteur et surtout la reconfiguration correcte du schéma de filtrage en fonction du mode de communication choisi. La consommation électrique des divers blocs analogiques et numériques est donnée en Tableau 3. Les valeurs obtenues en simulation et en mesures sur carte s'accordent parfaitement.

Pin	Name	Voltage	GSM @ 3.6Ghz		802.11g @ 4Ghz
			measure	simulation	measure
9	vdd_ana_1	1.25 v	8 mA	7.4 mA	7.7 mA
22	vdd_dig_1	1.25 v	22 mA	23.4 mA	22.8 mA
23	vdd_LO	1.25 v	36 mA	24.7 mA	24.3 mA
26	vdd_dig_2	1.25 v	14 mA	16.4 mA	--
27	vdd_ana2	1.25 v	43 $\mu$ A	56 $\mu$ A	--

Tableau 3. Consommation électrique du front-end RF

Les résultats de simulations et de mesures concernant le gain en tension des divers blocs analogiques sont donnés en Tableau 4. A l'exception d'une perte de gain inattendue en mode GSM, tous les autres résultats sont en quasi concordance.

Gain (dB)	LNTA		SINC <sup>2</sup>		DTASP2	
	meas	sim	meas	sim	meas	sim
GSM @945Mhz	34.6	37.4	N/A	-1.83	-14.51	-2.28
WIFI @1.01Ghz	34.9	36.1	-0.12	-0.2	N/A	

Tableau 4. Gain en tension des divers étages analogiques

La réjection des filtres IIR en mode GSM est donnée Figure 16. La réjection du second étage ( $C_{hist2}$ ) s'accorde avec les valeurs obtenues lors de l'étude système et suite aux simulations électriques du circuit.

La réjection du premier étage analogique est cependant moins élevée que prévu, ce qui pourrait être causé par des valeurs de capacités parasites bien plus élevées que celles estimées par l'extracteur post layout.

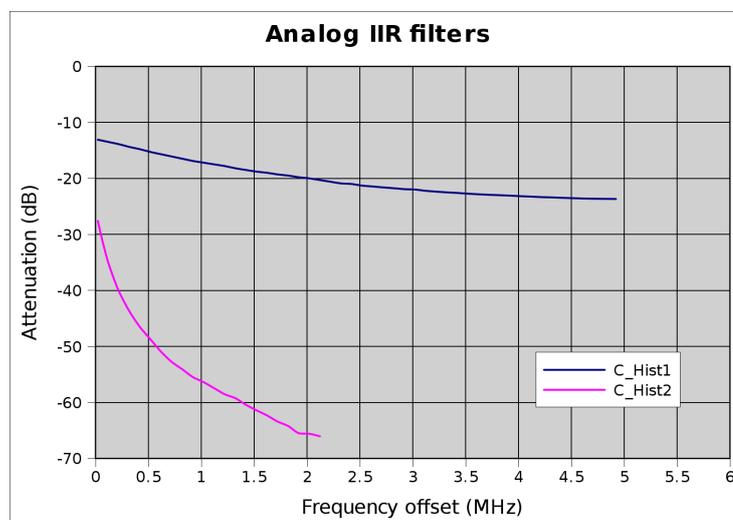


Figure 16. Réjection des filtres IIR en mode GSM

## Conclusion

La première partie de la thèse a été consacrée à la revue des architectures de réception radio les plus couramment utilisées dans les systèmes de communication sans fil, en mettant l'accent sur les aspects de reconfiguration, intégration et de faible consommation). Dans le cadre de la Radio Logicielle, les récepteurs à échantillonnage RF et les techniques de traitement de signal analogique à temps discret sont de plus en plus utilisés.

Le premier objectif de cette thèse a été d'étudier et de proposer une architecture de réception reconfigurable basée sur les concepts ci-dessus. Un récepteur RF temps discret à échantillonnage RF a été effectivement proposé et mis en œuvre en technologie CMOS 90nm. Les normes GSM900 et 802.11g ont été choisies comme cibles pour l'étude système et la validation de la reconfigurabilité du récepteur (différents plans de fréquences et systèmes de filtrage ont été adoptés pour chaque norme). Le récepteur est composé d'un LNA à transconductance, deux étages de traitement de signal analogique à temps discret pour la translation en fréquences, le filtrage anti-repliement, la décimation et une partie du filtrage canal. En changeant le taux d'échantillonnage ainsi que certains paramètres au niveau du circuit, il a été possible d'adapter le récepteur RF à différentes bandes RF et d'adapter le filtrage en fonction des spécifications exigées par chaque norme.

Le deuxième objectif de la thèse était d'étudier le problème de repliement de spectre, propre aux architectures à sous-échantillonnage et de trouver de nouveaux schémas de filtrages plus performants, complètement reconfigurables et à faible consommation électrique. Dans ce cadre, un filtre anti-repliement à temps discret de second ordre en  $\text{SINC}^2$  a été proposé et implémenté dans le récepteur RF. Basé principalement sur des matrices de capacités commutées, ce filtre permet d'obtenir une réjection assez élevée et présente l'avantage d'être totalement reconfigurable, et donc parfaitement adapté aux applications multi-standards.

Les premières séries de mesures effectuées sur le circuit prototype ont permis de démontrer le bon fonctionnement du récepteur. La conception d'une carte de test dédiée est cependant nécessaire afin de continuer la validation du récepteur et d'estimer les performances en terme de gain et de filtrage. Plusieurs améliorations pourraient être apportées au circuit actuel, afin notamment de réduire la consommation électrique et d'augmenter le nombre de standards pouvant être adressés.



# Symbols and Abbreviations

$1/f$	Flicker noise
$\alpha_k$	Filter tap coefficient
$\phi_k$	$k$ -th sampling phase
$\mu$	Carrier mobility
$\sigma$	Standard deviation
$\Delta$	Process gradient
$C_B$	Buffer capacitor
$C_H$	History capacitor
$C_R$	Rotating capacitor
$C_{par}$	Parasitic capacitance
$C_{ox}$	Gate oxide capacitance
$F_c$	Channel frequency
$F_s$	Sampling frequency
$G_m$	Transconductance
$H(z)$	Transfer function
$M$	Decimation ratio
$S(f)$	Spectral density
$T_i$	Integration period
$T_s$	Sampling period
$V(t)$	Voltage signal
$V_{cc}$	Supply voltage
$V_{TH}$	Threshold voltage
AAF	Anti-alias filter
ADC	Analog to digital converter
CMOS	Complementary metal oxide semiconductor
DAC	Digital to analog converter
DCU	Digital control unit
DTASP	Discrete time analog signal processing
FFT	Fast Fourier Transform
FIR	Finite impulse response
GSM	Global system for mobile communications
I/Q	In-phase/Quadrature
IF	Intermediate frequency
IIR	Infinite impulse response
LNA	Low noise amplifier
LNTA	Low noise transconductance amplifier

LO	Local oscillator
NF	Noise figure
PSD	Power spectrum density
RF	Radio frequency
SAW	Surface acoustic wave
SDR	Software defined radio
SINC	Sinus cardinal
SNR	Signal to noise ratio

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# Chapter 1

## Introduction

### Motivation and aim of the research

Recent trends in cellular radio terminals towards smaller handsets, and the proliferation of radio standards around the world place many demands on the future of radio terminals. Software Defined Radio (SDR) is an enabling technology which may provide a solution for the realisation of multiband, multimode radio terminals by defining radio functionality in software [36]. This allows the radio terminal to be adapted to different systems or customised for various services by reprogramming the radio functionality.

A possible solution for increasing both the receiver integration level and reconfigurability is to transfer the signal sampling and analogue-to-digital (A/D) interface from the baseband to higher frequencies, i.e. to an IF, or optimally directly to RF, and to use a high-speed A/D converter to enable further signal processing to take place in the digital domain. As an inherent advantage, digital signal processing allows elimination of the non-idealities of analogue signal processing, such as device noise and non-linearities, and of component mismatches.

Technological progress towards diminished transistor feature size, especially in pure CMOS processes, also favours an increased level of digital signal processing in receiver implementation [44]. A fully software-defined radio [8], and even a partially programmable radio supporting multiple wireless standards would directly benefit from radio architectures based mostly on digital signal processing and digital controllability. However, using an architecture based on a high resolution bandpass A/D converter at a high frequency imposes very demanding requirements on the dynamic range of the converter and results in an increased overall power consumption.

Instead of directly converting a high frequency RF signal into digital form, bandpass sampling can be used to perform frequency downconversion prior to A/D conversion. This helps decreasing the overall power dissipation and allows the use of discrete-time digital signal processing techniques (in an analog implementation) to achieve a high integrability in an advanced CMOS technology. It has proved difficult, however, to realize the required appropriate bandpass anti-alias filtering and obtain adequate noise performance in high-frequency operation with elementary implementations of subsampling circuits [11].

The current thesis concentrates on two specific points. The first one is to

investigate and implement a reconfigurable architecture for a multi-standard receiver [32], based on the concepts of RF bandpass sampling and discrete-time analog signal processing. Although several implementations of such discrete-time receivers have already been reported [14, 42], only few of them have tried to target different communication standards in order to truly validate the multi-standard capability [4, 39]. In the current work, a reconfigurable discrete-time receiver based on RF sampling is actually proposed. The GSM900 and 802.11g standards (which have very different specifications and requirements) are chosen as target standards to validate the implemented reconfiguration mechanisms and hence the reconfigurability of the receiver.

The second aim of the thesis is to study and propose new solutions for enhanced anti-alias filtering. A fully passive second order sinc-type anti-alias filter [33] is analyzed in the current work and implemented in the proposed RF sampling receiver. Basically, the filter is constructed as a discrete-time FIR filter with tap coefficients implemented through capacitive ratios. In addition to offering an improved alias rejection, the proposed filter does not result in power consumption increase and is above all adapted for multi-standard receiver operations.

## Organisation of the thesis

The thesis is organized as follows. A short review of wireless receiver architectures is presented in Chapter 2. The concept of Software Defined Radio is introduced and some of the best architecture candidates for multi-standard receivers are described. The discrete-time RF sampling receiver and the principle of frequency downconversion by subsampling are presented in Chapter 3. This chapter also presents the fundamentals of charge-domain sampling and describes how this technique can be utilized to implement anti-aliasing and elementary filtering functions in discrete-time RF sampling receivers. Chapter 4 presents the proposed reconfigurable receiver with its main innovations (dual-mode operation and improved anti-alias filtering) and details the system level study of the architecture. Chapter 5 details the circuit level design of the circuit and points out the major circuit problems encountered during the design of discrete-time receivers. Chapter 6 presents preliminary results of measurements performed on the implemented prototype circuit. A summary of thesis work and perspectives for future work are finally presented in conclusion.

## Major contributions

- Discrete-time RF sampling receiver in CMOS technology
- GSM and 802.11g dual-mode reconfigurable receiver architecture
- Second order discrete-time anti-alias filter with improved rejection
- System level study and noise analysis of discrete-time receivers

## Chapter 2

# Overview of wireless receiver architectures

### 2.1 Introduction

This chapter offers a review of the radio receiver architectures that are the most widely used in today's wireless communications systems. The advantages of these architectures are discussed in terms of performance, suitability for integration and also in terms of reconfigurability and multi-standard capability. The concept of Software Defined Radio is then introduced and some of the hardware requirements that are imposed on the RF front-end part are presented. The multi-standard concept which is leading the path towards software defined radios is then addressed and some of the best candidate architectures for multi-standard radios are finally presented.

### 2.2 Overview of receiver architectures

When developing and designing RF receiver for a wireless mobile communication system, designers first determine what type of architecture will be employed based on requirements of performance, cost, power consumption, and robust implementation. This section present the architectures of the RF receivers that are practically applicable to the mobile stations of wireless communication systems.

RF front-end receivers are defined from the antenna to the analog to digital converter and are usually formed by different devices and circuits operating at radio frequency (RF) band, intermediate frequency band (IF) and analog baseband. The Analog to Digital converter (ADC) is often used as a boundary between the RF receiver and its digital counterpart. However, this boundary is getting ambiguous with the state of the art of ADCs running at higher and higher sampling rates, in which case, the ADC will be certainly also considered as part of the RF receivers [12].

At present most RF transceivers in wireless communication systems are using the superheterodyne architecture. This architecture has the best performance if compared with the others, and therefore it has been the most popular transceiver architecture since it was invented in the 1910s [12]. Capable of multi-mode oper-

ations with great cost saving and no increasing extra parts, the direct conversion or homodyne architecture has emerged and became a very popular radio architecture for wireless mobile communication systems. To overcome some issues of direct conversion architecture, a modified architecture referred to as low IF architecture was then created. Some wireless communication receivers especially based on the CMOS technology started to employ this architecture to cope with the flicker noise and the DC offset problems of the direct conversion. Following this same order, this section will first discuss the superheterodyne architecture, then the direct conversion (zero-IF) and low-IF architectures.

### 2.2.1 Superheterodyne receiver

The superheterodyne architecture is probably the most commonly employed in current wireless systems. It consists in mixing an incoming signal with an offset frequency local oscillator (LO) to generate an intermediate frequency (IF) signal in the receiver case. In a superheterodyne transceiver, the frequency translation process may be performed more than once, and thus it may have multiple intermediate frequencies and multiple IF blocks. The superheterodyne architecture that is based on a two-stage downconversion scheme (dual-IF) is the most used in today's RF receivers (illustrated in Fig. 2.1).

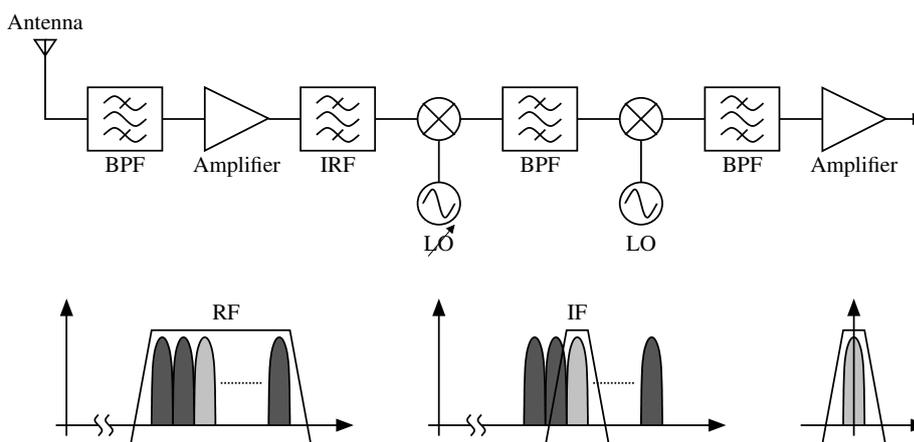


Figure 2.1: Superheterodyne receiver architecture

The out-of-band blocking signals are reduced by an RF bandpass filter placed immediately after the antenna. The signal is then amplified by an LNA, which must have a sufficiently low noise to allow detection of weak signals but must also have the dynamic range to handle in-band interferers. The bandpass filter is usually insufficient to reduce signals at the image frequency to the system noise level, and so a second image filter is inserted prior to mixing. To ensure that the image is sufficiently far away from the wanted signal to allow effective filtering, a relatively high first intermediate frequency must be chosen (for 1 to 2 GHz RF systems an IF of 100-200 MHz is common).

The mixer must still handle the complete dynamic range of the in-band signal. After the mixer, a SAW filter can be used to achieve the channel filtering. At these frequencies the SAW filter is small but usually has a large in-band loss

when complete channel filtering is to be achieved. The output drive of the mixer must therefore boost the signal level to allow for this loss.

Once the interfering channels have been attenuated, the signal is boosted to a high level (it can be limited if a constant-amplitude modulation scheme is used). The signal is then reduced to baseband frequency for demodulation. It is of course possible to split the channel filtering between the two intermediate frequencies. This will require a greater dynamic range in the second mixer.

This architecture requires the synthesis of two local oscillators, and their frequencies must be chosen so that spurious responses from the radio are kept to a minimum. This aspect of frequency planning, which will not be discussed in more detail here, is a well-understood design process which requires considerable care and experience.

This design requires several external filters and therefore does not lend itself to easy integration as the pin count increases. Moreover, the filters are usually single ended and hence achieving isolation between pins becomes an issue. In particular, the channel filter will often need to provide 50 dB of attenuation at key frequencies, thus implying that greater isolation must be achieved between the pins and with respect to signal ground if the filter response is not to be degraded. The image filter can be eliminated if an image-rejecting mixer is used. This will prevent the need to come off chip after the LNA and makes an LNA plus image-reject mixer a useful integrated building block.

### 2.2.2 Direct conversion receiver

Direct conversion receivers are widely listed and documented in the literature [3, 50]. Direct conversion means that the RF signal is directly downconverted to baseband without intermediate frequency stages, and therefore it is also referred to as zero-IF. The direct conversion architecture (illustrated in Fig. 2.2) has many attractive features and offer the best opportunity for integrated systems because of its simplicity.

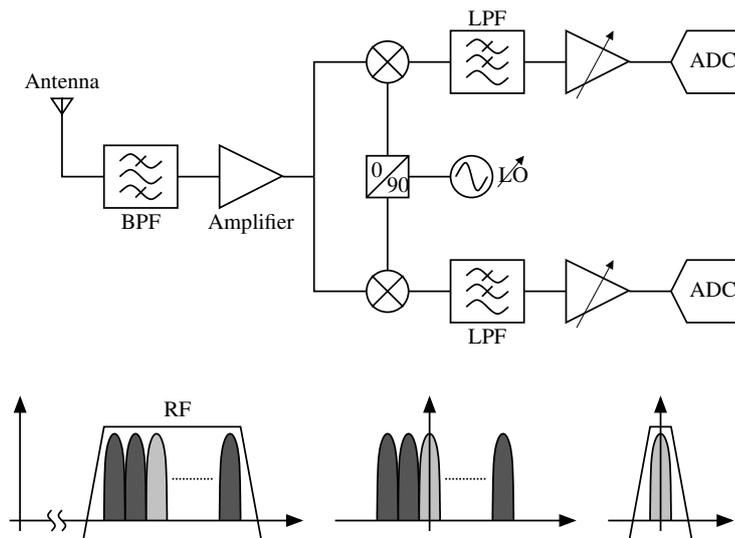


Figure 2.2: Homodyne receiver architecture

Once again, an RF bandpass filter is placed at the input. The LNA's output is passed into the mixer. The LNA must handle the same dynamic range as for the superheterodyne architecture and it must have enough gain to lift weak signals above the noise of the mixer. The mixer however, now converts directly to baseband. Thus the signal is its own image, and channel filtering can now be carried out by low-pass baseband filters. Only one local-oscillator frequency needs to be synthesised, and frequency planning is straightforward. Moreover, the expensive IF passive filter (SAW filter) can now be eliminated, and then the cost and size of the overall transceiver are reduced.

The channel filtering of the direct conversion receiver is performed at baseband using an active lowpass filter. The bandwidth of the active filter can be designed as adjustable. Thus, it is easy to design the direct conversion receiver for multi-mode operations with a common analog baseband circuitry and even a common RF front-end.

The configuration of the direct conversion radio may seem simpler than that of the superheterodyne radio, but its implementation is much more difficult since there are a number of technical challenges in the direct conversion receiver [12].

The main issue is associated with DC signals which are generated by imperfections in the mixer. These signals are implicitly in-band and it is therefore difficult to filter them from the wanted signal. It is necessary to keep them sufficiently below the signal. Unfortunately, the amplification that can be applied to the signal before mixing is limited by the level of in-band interferers which must not overload the mixer.

The main issue is associated with DC offsets that arise from many sources. Imbalance in the mixers will lead to a DC output. This is generally a constant quantity and could be cancelled with suitable circuitry. Any leakage of the local oscillator to the input of the receiver will also result in a DC signal being generated. If this leakage is via radiation coupling into the antenna, then this may vary with the local environment. Finally, non-linearities in the mixer may cause signals to be generated at DC from other interferers. The latter mechanisms can be time varying, and any offset cancellation needs to be able to respond to time variation. It is only when special precautions are taken to cancel DC offsets that direct-conversion architectures can be used.

I/Q mismatches are other associated problems due to the quadrature down-conversion in homodyne receivers. Because the down-converted signal is located at zero frequency, flicker noise or  $1/f$  noise of devices will also corrupt the information signal. More details of the direct-conversion issues are given in [50].

### 2.2.3 Low-IF receiver

The low-IF receiver (illustrated in Fig. 2.3) combine the advantage of both superheterodyne and homodyne receivers [55]. The received RF signal is down-converted to IF by an LO, where the intermediate frequency can be as low as half to two times the bandwidth of the desired signal. The main advantage of the low IF architecture over the direct conversion one is that this architecture has no DC offset problem because the desired signal is off the DC by the IF.

Properly choosing the low IF can remove the low frequency interference product that results from AM demodulated out of band interferers (due to second order nonlinearities). In addition, the low IF architecture is also able to significantly reduce the near DC flicker noise impact on the receiver performance.

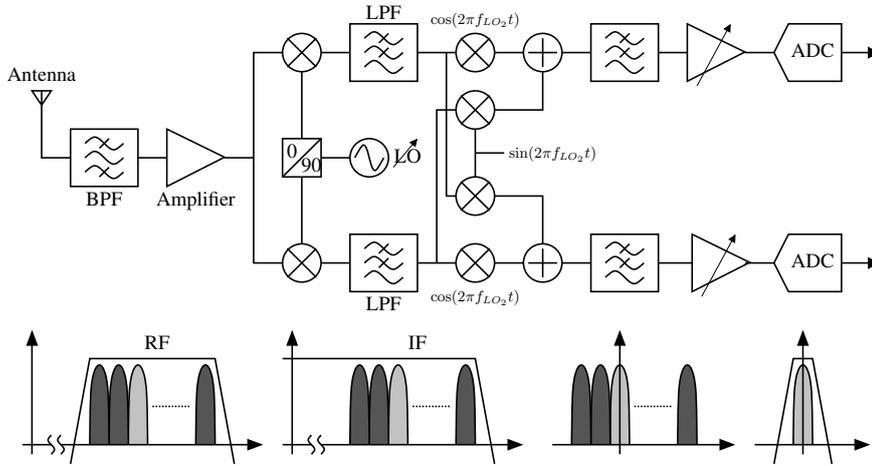


Figure 2.3: Low-IF receiver architecture

This architecture, thus, is quite attractive for the highly integrated transceivers based on the CMOS technology (which is more concerned by the flicker noise than other technologies such as GaAs).

The main issue of the low IF receiver architecture is the image problem, since the IF is too low to separate the image from the desired signal by means of a bandpass filter in the RF stage. The imbalance between I and Q channel signals in the low IF receiver determines the possible maximum image rejection. To achieve high image rejection, it is necessary to minimize the imbalance of the I and Q signals by means of complex quadrature downconversion [56] or by a combination of the quadrature downconversion and complex bandpass filtering [21].

A generic wideband receiver evolved from the conventional receiver architecture, shown in Fig. 2.3, has been used in cellular phone base stations to support multiple wireless communication standards and to meet the rapidly increasing demands of cellular services [71]. In this application, multiple channels at the RF are selected by the first tunable LO instead of a single channel in superheterodyne receivers. All the selected channels are translated to baseband by the second LO with a fixed frequency and then digitized in a wideband A/D converter for I and Q components respectively [34, 35, 53]. The number of simultaneous channels that can be received would be limited by the digital signal processing capability.

## 2.3 Software defined radio

A software defined radio (SDR) [6, 38] is a form of transceiver in which ideally all aspects of its operation are determined using versatile, general-purpose hardware whose configuration is under software control [31]. The concept of software defined radio was originally conceived for military applications. It consists of a single radio receiver to communicate with different types of military radios using different frequency bands and modulation schemes. This concept is starting to be introduced into commercial applications.

As technology progresses, an SDR can move to an almost total SR, where the digitization is at (or very near to) the antenna and all of the processing required for the radio is performed by software running on high-speed digital signal processing elements [61]. The ideal case is doing sampling and digitization directly on an RF signal. Due to the presence of strong interferers around weak RF information signal, an A/D converter with a higher dynamic range up to around 100 dB might be needed. However, it is hard to achieve by current A/D converter technology.

### 2.3.1 Ideal SDR architecture

A possible architecture for an ideal software defined radio [31] is shown in Fig 2.4. Note that the A/D converter is assumed to have a built-in anti-alias filter and that the D/A is assumed to have a built-in reconstruction filter.

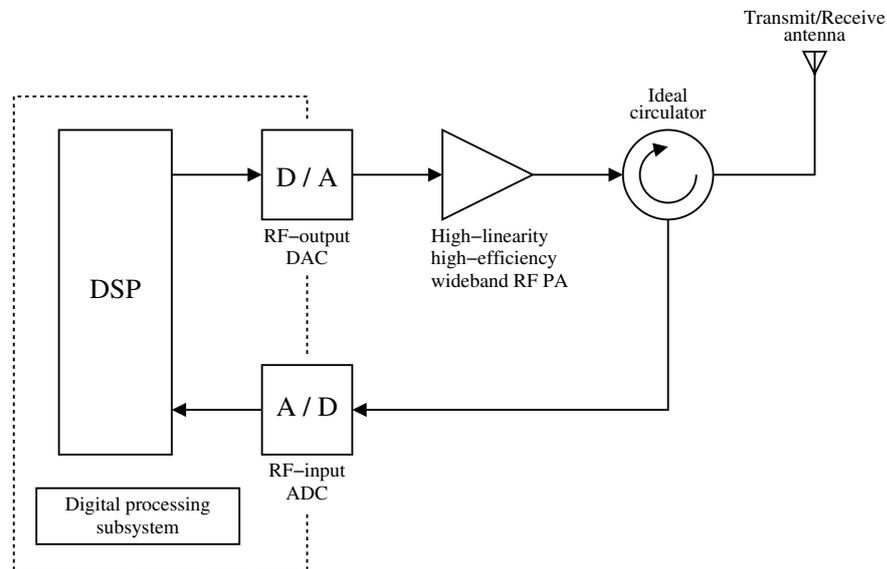


Figure 2.4: Ideal software defined radio architecture

The ideal software defined radio has the following features [31]:

- The modulation scheme, channelisation, protocols, and equalisation for transmit and receive are all determined in software within the digital processing subsystem.
- The ideal circulator is used to separate the transmit and receive path signals, without the usual frequency restrictions placed upon this function when using filter based solutions. This component relies on perfect matching between itself, the antenna and power amplifier impedances and so is unrealistic in practice (based upon typical transmit/receive isolation requirements). Since duplexers are usually fixed frequency components, their elimination is a key element in a multi-band or even multi-standard radio. Note that the circulator would also have to be very broadband, which most current designs are not.

- The linear (or linearised) power amplifier ensures an ideal transfer of the RF modulation from the DAC to a high-power signal suitable for transmission, with low adjacent channel emissions. Note that this function could also be provided by an RF synthesis technique, in which case the DAC and power amplifier functions would effectively be combined into a single high power RF synthesis block.
- Anti-alias and reconstruction filtering is clearly required in this architecture. It should be, however, relatively straightforward to implement, assuming that the ADC and DAC have sampling rates of many gigahertz. Current transmit, receive, and duplex filtering can achieve excellent roll-off rates in both cellular and base station designs. The main change would be in transforming them from bandpass (where relevant) to lowpass designs.

### 2.3.2 Hardware requirements

The ideal hardware architecture, shown in Fig. 2.4, imposes some difficult specifications upon each of the elements in the system. Some of these specifications can be summarised as follows [31]:

1. Antenna: A frequency range of almost 5 octaves is required, together with a realistic gain/loss figure around 0 dBi. Combined with the handset requirements of small size, omnidirectional coverage and low cost, the physical realization of this component becomes extremely challenging.
2. Circulator or duplexer: A high isolation and a broadband coverage range are needed. In the case of a conventional, filter-based duplexer, this latter requirement is impossible to achieve with current technologies.
3. A/D converter: The sampling rate of the converter, if Nyquist sampling directly at RF, would need to be at least 4.4 GHz and, in reality, much more (to allow for a realistic anti-alias filter roll-off). This is an extremely hard specification, particularly with current technology.
4. Receiver anti-alias filtering: Based on the two-times Nyquist sampling converters discussed above, an attenuation of 60 dB is required around 18 MHz from the channel edge. This would be extremely difficult, if not impossible, to achieve in a bandpass filter capable of tuning from 100 MHz to 2.2 GHz. Improvements in sampling rates (for a given converter resolution) will, however, allow this requirement to be relaxed and may enable some limited forms of SDR to be realised without such high performance filtering needing to be included.

The specifications outlined here and the components required to realise them are clearly not available with current technology and may not be achievable, in many cases, for a considerable period.

## 2.4 Multi-standard receivers

As previously mentioned, software defined radios are still not feasible today due to technology limitations and it is hence more reasonable to speak about multi-

standard receivers [2]. A multi-standard receiver can be realized by implementing different receivers for different standards into a single receiver. However, the area and power consumption would be extremely high. Instead, a well-designed architecture of a multi-standard receiver should optimally share the available hardware resources and make use of the tunable and programmable devices. A proper system specification should be defined for each of the involved standards. Moreover, for battery powered devices it is more important that a highly integrated solution is used so that the area and power consumption are considerably reduced [55]. From the view of multi-band multi-mode radio communications and the placement of the A/D converter, both the homodyne receiver and the subsampling receiver are candidates for SDR implementation because the A/D converter directly has an interface to RF or higher IF signals [9, 45, 60, 69]. From the view of high level integration, the homodyne receiver, low-IF receiver and the subsampling receiver are most suitable.

### 2.4.1 Previous realizations

A single chip multi-mode receiver for four standards (GSM 900, DCS 1800, PCS 1900 and W-CDMA), was designed with a zero-IF architecture [52]. All the problems associated with the homodyne receiver, e.g., LO leakage, DC-offset, I/Q mismatches and flicker noise, inevitably happen and are treated in many different ways. The corresponding block diagram of the receiver is shown in Fig. 2.5.

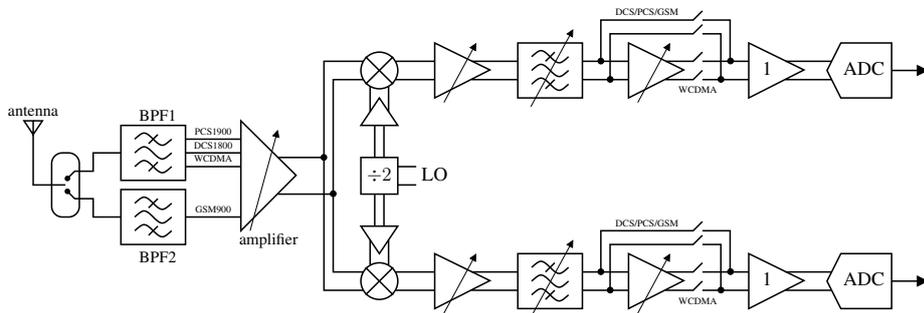


Figure 2.5: Multi-standard receiver using zero-IF architecture

The selection among different standards is realized by an external digital controller and the hardware is shared as much as possible by different standards. Four different standards use two different channel selection filters. A divide-by-two circuit is used to provide quadrature LO signals for the mixers. The LO signal is generated on-chip such that the LO leakage on the PCB is eliminated and the LO leakage to the RF input is better suppressed. The baseband circuit has two operation modes, one for WCDMA and the other for DCS1800/PCS1900/GSM900.

Another fully integrated multi-standard radio receiver was designed in low-IF toward mobile terminals that support five wireless communication standards, Bluetooth, two GSM standards (DCS1800 for Europe, PCS1900 for USA), UMTS, 802.11a/b/g [5]. Bluetooth provides a wireless link between the radio terminal and other peripherals (e.g., headphone), and it should be active

all the time, while the other four standards covering five frequency bands are activated by an RF switch.

### 2.4.2 RF sampling architecture

The main idea of the RF sampling architecture, as illustrated in Fig. 2.6, is signal discretization in time close to the antenna [18]. The difference with an ideal software radio is that some discrete-time signal processing is performed in the analog domain prior to the A/D conversion.

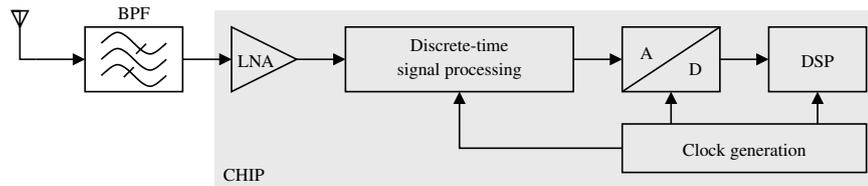


Figure 2.6: RF sampling receiver architecture

This architecture relaxes the performance requirements for the A/D converter [18]. First, the power dissipation in the A/D converter can be reduced to a reasonable level for mobile terminal applications, thanks to a reduced sampling rate and lower dynamic range. Next, the analog input bandwidth of the A/D converter can be reduced as well. These benefits pave a way for the implementation of a highly integrable software radio.

The discrete-time signal processing offers several benefits. By tuning the sampling rate, different RF bands can be selected and downconverted to IF. This feature increases the flexibility of the receiver in a multi-band multi-standard operation. According to the literature study, there is an increasing interest in this RF sampling architecture because of its flexibility. This receiver will be studied in details in the next chapter.

## 2.5 Conclusion

This chapter introduced the concepts of software defined radios and multi-standard receivers. Several receiver architectures were presented and discussed in terms of reconfigurability. The RF sampling architecture is one of the most promising architectures in the path towards software radios. In this thesis, the RF sampling architecture was chosen as a reference for the realization of a multi-standard receiver. The advantages and current problems of this architecture will be studied first and then a prototype receiver will be proposed to address some of its problems.



## Chapter 3

# Study of the RF sampling receiver

### 3.1 Introduction

As mentioned in the previous chapter, in order to maximize the reconfigurability of software radio receivers, digitization should occur as close to the antenna as possible. Bandpass sampling (also called subsampling) allows the digitization of bandpass signals at RF or intermediate frequencies with no significant increase of the sampling rate.

Bandpass sampling enables the realization of a more flexible receiver and allows many radio functions to be defined in software. However, this same concept has associated problems such as noise and interference folding and aperture jitter [47, 24].

This chapter gives a global overview of RF sampling receivers and discusses their advantages and major limitations. A general study of charge sampling, which is a technique used intensively in RF sampling receivers is also presented. First, the concepts of both subsampling and charge sampling are presented. Then, state-of-the-art realizations of RF sampling receivers based on these concepts are listed. The major problems encountered with such architectures are addressed throughout this chapter and an innovative architecture will be proposed to address some of these problems.

### 3.2 Bandpass sampling

The bandpass sampling also referred to as subsampling or harmonic sampling is the technique of sampling at rates lower than the highest frequency of interest to achieve frequency conversion from RF to low IF or baseband through intentional aliasing and to be able to exactly reconstruct the information content of the sampled analog signal if it is a bandpass signal [46, 59].

The sampling rate requirement is no longer based on the RF carrier, but rather on the information bandwidth of the signal. Thus the resulting processing rate can be significantly reduced.

### 3.2.1 Basics of bandpass sampling

The sampling theory (Nyquist criterion) shows that, in order to avoid aliasing and to completely reconstruct a given signal, the sampling rate must be at least twice the highest frequency component in the signal. In the case of baseband signals, the useful information covers the entire band from zero frequency to cutoff frequency. However, the RF signals used in the wireless communications are usually narrow-band but centered on high frequency carriers, in which case, the minimum sampling rate (in its classical definition) would be quite unrealistic [12].

The bandpass sampling theorem shows that the minimum uniform sampling rate to avoid aliasing depends on the signal bandwidth instead of the highest frequency of interest. The minimum sampling rate for aliasing-free can be as low as twice of the signal bandwidth if the carrier frequency of the signal is properly chosen. However, the minimum sampling rate  $f_{s,min} = 2 \cdot BW$  (where  $BW$  is the signal bandwidth) is just a theoretical value, given that any imperfection in an implementation based on this sampling rate can cause aliasing if no margins are considered.

Assume that a band-pass analog signal has its lowest frequency of interest  $f_L$  and the highest frequency of interest  $f_H$  (the bandwidth of the signal equals  $BW = f_H - f_L$ ). The bandpass analog signal can be exactly reconstructed after sampling and digitizing if the sampling rate  $f_s$  meets the following two inequalities [62]:

$$\frac{(n-1)f_s}{2} < f_L \quad \text{and} \quad f_H < \frac{nf_s}{2}$$

where  $n$  is an integer given by  $1 \leq n \leq \lfloor f_H/BW \rfloor$  (where  $\lfloor \cdot \rfloor$  denotes the largest integer). A sampling rate  $f_s$  that meets these two inequalities ensures that the resulting spectra of the sampled signal has no overlapping or aliasing, as clearly shown in Fig. 3.1.

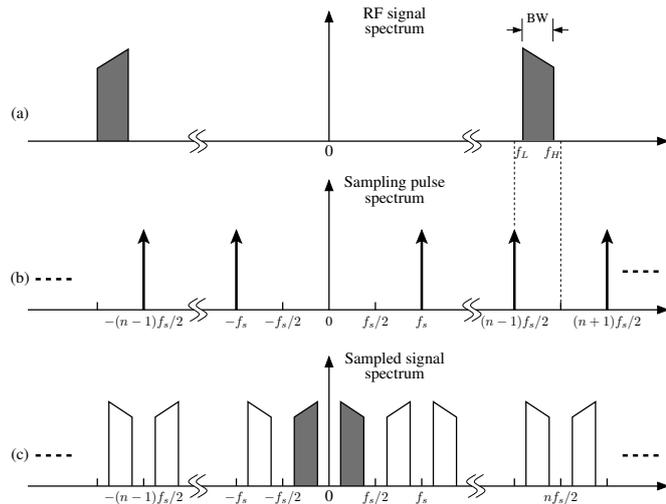


Figure 3.1: Spectra of bandpass sampling (a) RF signal spectrum, (b) sampling pulse spectrum and (c) sampled signal spectrum

From the previous inequalities, we can determine the acceptable uniform sampling rates for aliasing-free to be:

$$\frac{2f_H}{n} \leq f_s \leq \frac{2f_L}{n-1} \quad (3.1)$$

The maximum allowable value  $n_{max}$  for the bandpass signal with the lowest and highest frequencies  $f_L$  and  $f_H$  is thus equal to:

$$n_{max} = \lfloor \frac{f_H}{f_H - f_L} \rfloor$$

Equation (3.1) can be described graphically as shown in Fig. 3.2 for  $n = 1, 2, \dots, 5$  (where the normalized sampling frequency  $f_s/BW$  versus the normalized highest frequency  $f_H/BW$  is plotted as presented in [62]). The areas inside the wedges are the permissible zones for sampling without aliasing. The shadowed area represents the sampling rates that result in aliasing.

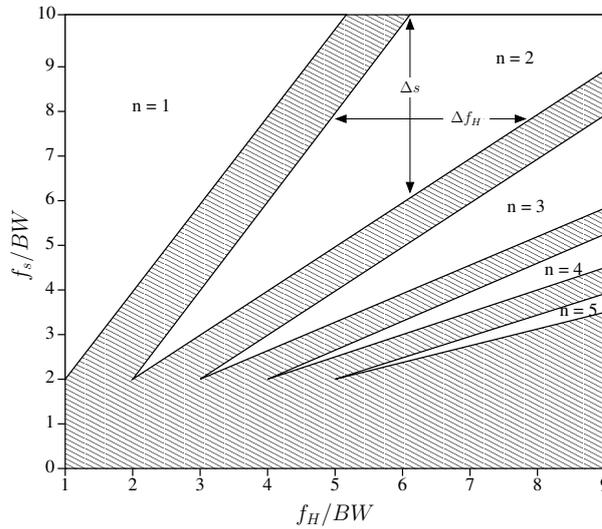


Figure 3.2: Permissible zones for uniform sampling without aliasing

It is apparent that the aliasing-free ranges of the sampling rate and the highest signal frequency of interest,  $\Delta s$  and  $\Delta f_H$ , increase with normalized sampling rate and the highest signal frequency. The smaller the integer number  $n$  is, the broader the permissible area for sampling without aliasing will be. The value of  $n$  is usually lower than 10 when the bandpass sampling technique is used for converting an RF signal to a low IF or baseband signal [12].

### 3.2.2 Problems of subsampling

#### Noise spectrum aliasing

It is known that a resistor charging a capacitor gives rise to a total thermal noise with power  $kT/C$  [51], where  $k$  is Boltzmann constant,  $T$  is the absolute temperature and  $C$  is the capacitance. The on-resistance of the switch will

introduce thermal noise at the output. The noise is stored on the capacitor along with the instantaneous value of the input voltage when the switch turns off. As shown in Fig. 3.3, the resistor  $R_{on}$  and sampling capacitor  $C$  construct a lowpass filter with a transfer function of:

$$H(f) = \frac{1}{1 + j2\pi f R_{on} C} \quad (3.2)$$

with the 3dB bandwidth of  $f_{3dB} = 1/(2\pi R_{on} C)$ . Thermal noise is known as additive white gaussian noise (AWGN) in communication theory, i.e. having a delta-function autocorrelation with a flat Power Spectral Density (PSD).

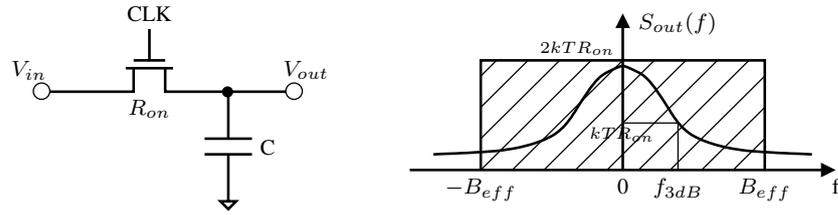


Figure 3.3: Illustration of effective noise bandwidth

The PSD of thermal noise introduced by the resistor  $R_{on}$  can be given as  $S_{in}(f) = 4kTR_{on}$  with a one-sided representation, or  $S_{in}(f) = 2kTR_{on}$  with a two-sided representation. The corresponding noise PSD at the output of lowpass filter is given by:

$$S_{out}(f) = S_{in}(f)|H(f)|^2 = 2kTR_{on} \frac{1}{1 + 4\pi^2 f^2 R_{on}^2 C^2} \quad (3.3)$$

by a two-sided representation, and the total noise power is obtained as

$$P_{out} = \int_{-\infty}^{\infty} S_{out}(f) df = \frac{kT}{C} \quad (3.4)$$

The output noise of the lowpass filter performed by the RC network can be made equivalent to AWGN with a constant PSD within an effective noise bandwidth  $B_{eff}$ . Both noise sources share the same noise power  $kT/C$  (Fig. 3.3), thus:

$$P_{out} = \frac{kT}{C} = 2kTR_{on} \cdot B_{eff}$$

and

$$B_{eff} = \frac{1}{4R_{on}C} = \frac{\pi}{2} f_{3dB}$$

The effective noise bandwidth of the sampling device  $B_{eff}$  depends on the ON resistance in the switch and the sampling capacitance, and it is normally larger than the maximum frequency of the input signal.

When using bandpass sampling, the wideband  $kT/C$  noise will be folded due to the effect of subsampling [48] such that the resulting SNR is lower than the

equivalent lowpass sampling system in the presence of the same noise source. The SNR degradation in dB is given as [58]:

$$\text{SNR}_{\text{deg}} \approx 10 \log_{10} \frac{B_{\text{eff}}}{B} \cdot \frac{B}{F_s/2} = 10 \log_{10} \frac{2B_{\text{eff}}}{F_s} \quad (3.5)$$

The effect of noise aliasing can be also described graphically and is illustrated in Fig. 3.4.

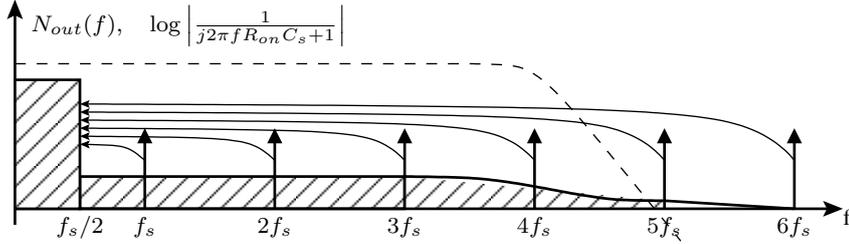


Figure 3.4: Noise aliasing due to subsampling

### 3.3 Charge sampling

Sampling circuits used as front-ends of DT signal processing blocks, such as switched capacitor (SC) filters or DT A/D converters, have conventionally been based on the direct sampling of voltage signals [30]. However, the filtering properties of elementary voltage sampling circuits are inefficient, usually resulting in a high noise figure and in a need for highly selective additional anti-aliasing filters when used for subsampling downconversion of high-frequency signals. Recently, circuits based on the integrative sampling of current signals, often referred to as charge-domain sampling circuits [42, 7, 70], have gained interest for use as high-frequency front-ends of DT signal processing blocks, due to their inherent simplicity of combining both continuous and discrete-time filtering functions into high-frequency sampling. This section presents the basics of the charge-domain sampling technique and discusses the filtering properties of high frequency samplers based on it.

#### 3.3.1 Elementary charge sampling circuit

The operating principle of an elementary active integrator based integrating charge-domain sampling circuit is described in Fig. 3.5. Note that a realization based on a passive integrator is also possible [30].

The input voltage  $V_{in}$  of the sampler is transformed to a corresponding current using a transconductance cell with gain  $G_m$ . The output current of the transconductor is integrated into a feedback connected sampling capacitor  $C_s$  for a determinate period of length  $T_i$  controlled by the clock signal  $p_{int}$ . After the current integration period, the settled output voltage is read out (clock phase  $p_{out}$ ) at a rate  $f_s = 1/T_s$  and the sampling capacitor is discharged (clock phase  $p_{reset}$ ) prior to integration of a new sample.

Neglecting circuit non-idealities and assuming that the active integrator performs perfect integration of the input current, the ideal time-domain output

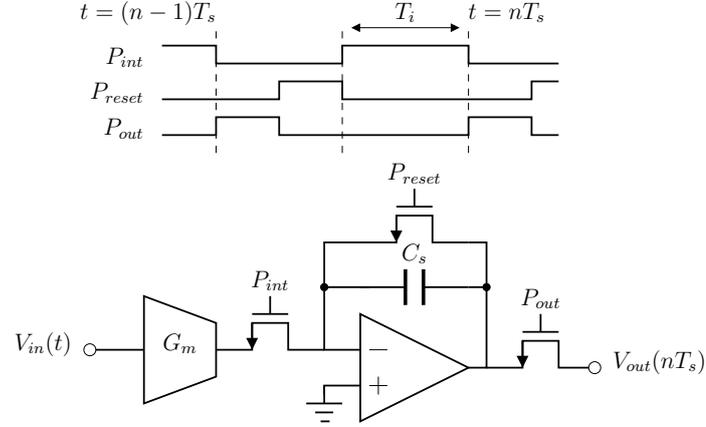


Figure 3.5: Active charge sampling circuit

voltage of the charge-domain sampler at the  $n^{\text{th}}$  sampling moment can be written as:

$$V_{out}(t = nT_s) = \frac{1}{C_s} \cdot \int_{nT_s - T_i}^{nT_s} I_{in}(u) du = \frac{G_m}{C_s} \cdot \int_{nT_s - T_i}^{nT_s} V_{in}(u) du \quad (3.6)$$

which can be interpreted as a time-domain convolution of the sampling clock pulse and the input current signal  $I_{in}(t) = G_m V_{in}(t)$ .

The elementary charge-domain sampling process can be represented by two subsequent signal processing operations: (1) a continuous time filtering due to integration of the signal current within a time window, followed by (2) an output voltage sampling at a rate  $f_s = 1/T_s$ . The response of the charge sampler for a sinusoidal input signal  $V_{in}(t) = \cos(2\pi ft)$  can be calculated in the time domain by evaluating the integral in (3.6) which yields:

$$V_{out}(nT_s) = \frac{G_m}{C_s} \cdot A(f) \cdot \cos[2\pi fnT_s + \Phi(f)] \quad (3.7)$$

where the amplitude  $A(f)$  of the output signal as a function of input signal frequency (ideal magnitude response of the sampler), can be expressed as:

$$A(f) = |H_{\text{sinc}}(f)| = \frac{G_m}{C_s} \cdot \left| \frac{\sin(\pi f T_i)}{\pi f} \right| \quad (3.8)$$

The magnitude response of the  $\sin(x)/x$  (sinc) type lowpass filter of the integrating charge sampler, according to (3.8), is depicted in Fig. 3.6. For comparison, the amplitude response of a simple voltage sampler with an equal 3-dB bandwidth limitation (due to the RC time constant of the sampling switch resistance and sampling capacitance) is also shown in the figure [30].

The current integration produces notches at multiples of the inverse of the integration period length  $1/T_i$ . The ideal 3-dB bandwidth of the charge sampler is approximately  $f_{3dB} \approx 0.44/T_i$ , while the voltage gain at DC is  $G_m T_i / C_s$ . As with the RC lowpass response, the sidelobes of the sinc response fall off at a rate of 20 dB/decade, the attenuation near the first sidelobe being around 13 dB.

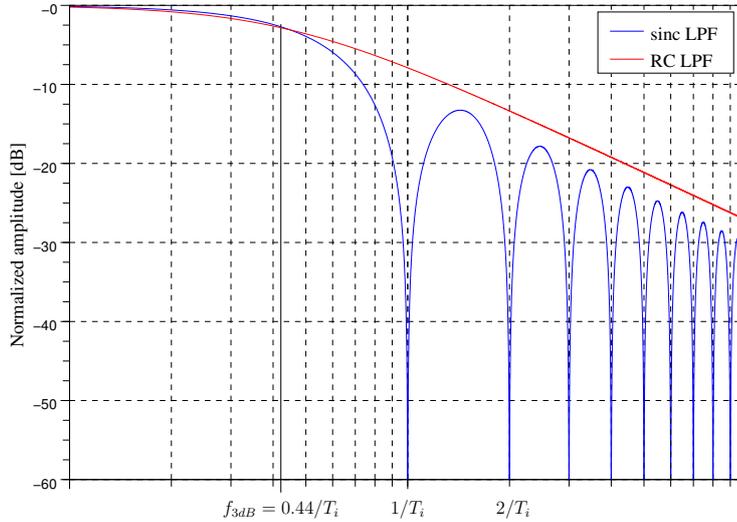


Figure 3.6: Magnitude responses of voltage and charge sampling circuits

However, the lowpass sinc response attenuates the high frequency components more than the simple RC lowpass response, providing a better anti-aliasing filtering embedded into the sampling operation.

Note that when the  $G_m$  cell is not limiting the input bandwidth, the 3-dB bandwidth of the integrating charge sampler is determined only by  $T_i$  and not by the circuit parameters of the sampler realization. This provides more freedom in selection the sampling capacitance without limiting the bandwidth of the sampler [30].

The integration period length  $T_i$  and the output sampling period  $T_s$  of the integrating charge sampler are two distinct parameters. The input bandwidth is set by  $T_i$ , whereas the spectral location and Nyquist bandwidth of the sampled signal are determined by  $T_s$ . An optimal narrowband built-in anti-aliasing filtering can be achieved by selecting  $T_i = T_s$ , which places the notches of the lowpass sinc response on top of the multiples of  $f_s$ , hence suppressing the undesirable signal components aliasing near DC in the sampling process.

### 3.3.2 Elaborated charge sampling structures

In addition to the integration phase, the elementary charge sampler also requires an output read-out phase and a reset phase (for capacitor discharge). This places a constraint on the minimum  $T_s$ , and hence on the maximum output sampling rate  $f_s = 1/T_s$  in relation to the integration period  $T_i$ . The output sampling frequency of the charge sampler can be increased without sacrificing the integration period length by means of the time-interleaved sampling operation illustrated in Fig. 3.7.

In time-interleaved charge sampling, one capacitor is integrating the input current while the other one is being read out and reset. This arrangement allows one integration period to transfer the integrated charge to the subsequent stage and to discharge the integration capacitor. The resulting output sampling period of the sampler is  $T_s = T_i$ , hence resulting in optimal placement of the

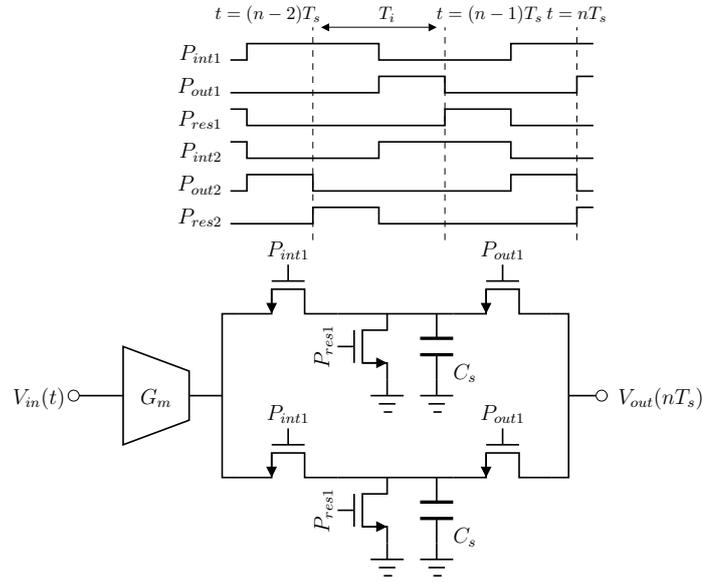


Figure 3.7: Time interleaved charge sampling

sinc response zeros. If longer time slots for output read-out and resetting are required, more than two integrator units can be used in the time-interleaved charge-sampling operation.

Current sampling within a time window inherently produces a bandwidth limiting CT sinc-type frequency response for charge sampling circuits. The frequency response of the elementary integrating charge sampler is not, however, very useful for embedded anti-aliasing filtering in the sampling of high-frequency bandpass signals due to its lowpass nature. The integrative charge sampling principle can be extended to general (including bandpass type) discrete-time finite impulse response (FIR) filtering. The principle of a general charge sampling circuit with a built-in FIR filtering function is illustrated in Fig. 3.8 [30].

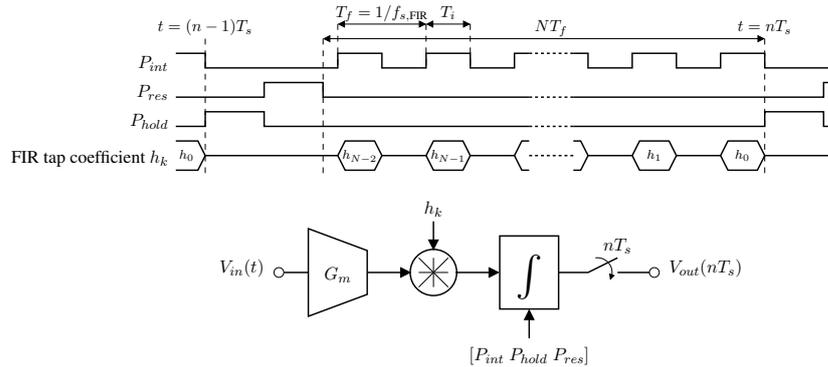


Figure 3.8: Charge sampling with embedded FIR filtering

Instead of integrating only one sample, several successive current samples are integrated into the sampling capacitor of the integrator stage during the

output sampling period  $T_s$  in the charge sampling FIR filter operation.

As for the elementary charge sampler, the integrator can be implemented either as a simple capacitor or as a closed-loop active integrator stage. The integrated current samples are each weighted within the integration time window of length  $T_i$  by multiplying the signal current by a given coefficient  $h_k$ , where  $k = 0, \dots, N - 1$  refers to the  $k^{\text{th}}$  integrated sample. The time delay between adjacent integrated current samples is  $T_f$ . After the integration of  $N$  weighted current samples, the output voltage of the sampler is held and read out by a subsequent DT circuit stage at the final output sampling rate  $f_s = 1/T_s$ . The sampling capacitor of the integrator unit is discharged prior to a new sampling cycle.

The ideal time domain output voltage of the charge FIR sampler at the  $n^{\text{th}}$  output sampling moment can be written as:

$$V_{out}(nT_s) = \frac{G_m}{C_s} \cdot \sum_{k=0}^{N-1} h_k \cdot \int_{nT_s - kT_f - T_i}^{nT_s - kT_f} V_{in}(t) dt \quad (3.9)$$

from which the ideal transfer function of the charge FIR sampler can be derived as:

$$H_{\text{FIR}}(f) = \frac{V_{out}(f)}{V_{in}(f)} = \frac{G_m}{C_s} \cdot \frac{1 - e^{-j2\pi f T_i}}{j2\pi f} \cdot \sum_{k=0}^{N-1} h_k z^{-k} \Big|_{z=e^{j2\pi f T_f}} \quad (3.10)$$

Two distinct filtering responses can be recognized in the transfer function of (3.10). The first part denotes the lowpass sinc response due to the gated integration of the current, whereas the latter part describes the DT FIR filtering response resulting from the summation of the  $N$  weighted, time-delayed current samples. Note that since the FIR filtering response of the sampler is determined only by the number of integrated samples  $N$  and their corresponding integration weights  $h_k$ , the general charge-domain FIR sampler can in principle be designed to realize any FIR filtering function of any type (i.e. lowpass, highpass, real-valued or complex-valued bandpass) embedded into the sampling operation.

The complexity and accuracy of the sampler's FIR filtering response is determined only by the tap coefficient resolution of the current multiplier unit and by the non-idealities of the physical circuit implementation [30].

## 3.4 State-of-the-art realizations

This section briefly presents the state of the art concerning circuit realizations based on RF bandpass sampling and charge sampling techniques. Previous anti-alias filtering implementations are also enumerated.

### 3.4.1 RF sampling receivers

Discrete-time RF sampling receivers were introduced for the first time by Texas Instruments. The concept was then intensively used and studied by many research teams all over the world. The first discrete-time RF sampling receiver that was presented by Texas Instruments used bandpass charge sampling combined with an  $N^{\text{th}}$  order FIR moving average filter and a 1<sup>st</sup> order IIR filter

for Bluetooth standard [42, 43, 54]. The corresponding schematic and the appropriate clock scheme are shown in Fig. 3.9. The charge sharing among  $C_H$  and  $C_R$  realizes a single pole recursive IIR operation. The combination of the sinc function, the FIR moving average filter, and the IIR operation provides a certain noise aliasing suppression.

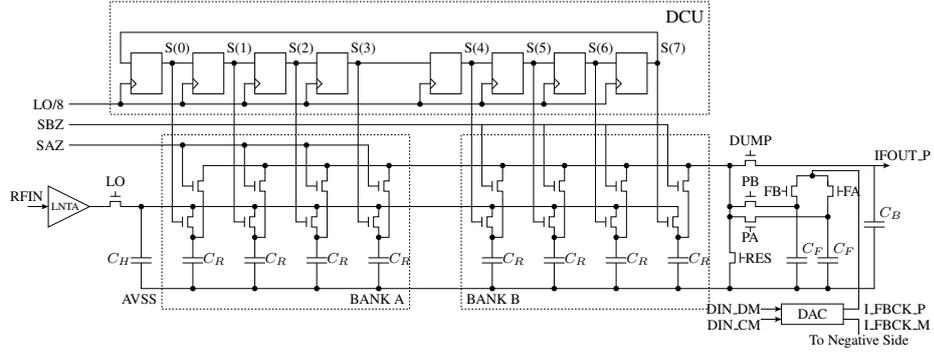


Figure 3.9: TI's first discrete-time RF sampling receiver

Texas Instruments applied then the same concept for designing a fully integrated quad-band GSM/GPRS receiver in 90nm CMOS technology [41, 40]. The receive chain used discrete-time analog signal processing to down-convert, down-sample, filter and analog-to-digital convert the received signal. The anti-alias filter was implemented as a first order sinc filter.

Jakonis et al. worked on different CMOS sampling mixer circuits for frequency downconversion [15, 17, 16]. They also proposed a 2.4GHz RF sampling receiver front-end in  $0.18\mu\text{m}$  CMOS technology [14]. The receiver architecture (depicted in Fig. 3.10) was based on switched capacitor techniques for sampling, filtering and downconverting the RF signal.

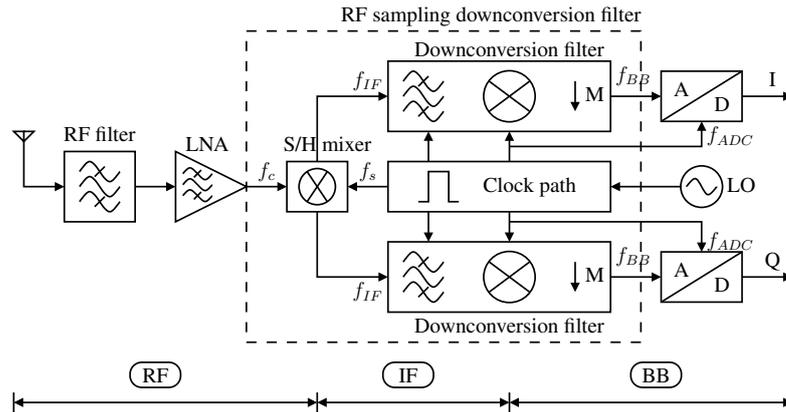


Figure 3.10: Jakonis's RF sampling receiver front-end

The sampler was built here as a voltage-domain sampler and the anti-alias filter is constructed as a discrete-time voltage bandpass FIR filter (by contrast with the continuous-time sinc anti-alias filter used in TI's receiver).

Abidi et al. proposed a discrete-time receiver [2, 4] using the same concepts of continuous time anti-alias filtering, signal downconversion and FIR/IIR filtering as initially introduced by Texas Instruments. This receiver architecture is shown in Fig. 3.11 and uses a wideband low noise amplifier [8] and a second order sinc type anti-alias filter [37].

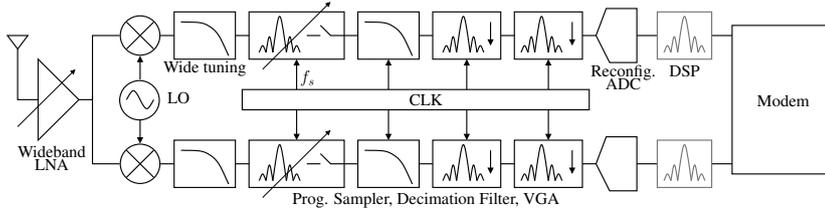


Figure 3.11: Abidi's discrete-time RF sampling receiver

STMicroelectronics proposed a discrete-time RF sampling receiver in CMOS 90nm technology for the GSM standard [19, 39]. The main difference with the above realizations resides here in the fact that the intermediate frequency used during signal downconversion steps is half the sampling rate ( $F_s/2$ ). The architecture is depicted in Fig. 3.12.

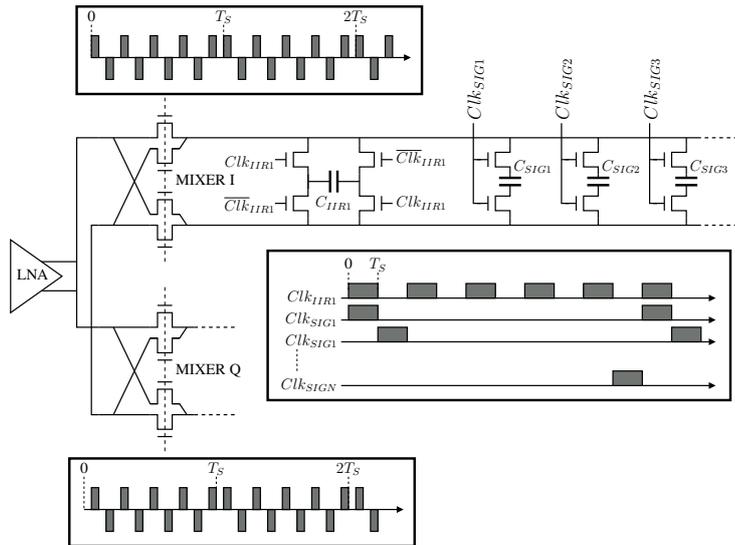


Figure 3.12: STMicroelectronics  $F_s/2$  discrete-time sampling receiver

The receiver architecture takes advantage of zero-IF architectures (limited image frequency rejection, real filters, ...) while escaping the impact of flicker noise and second-order front-end non-linearity. This receiver was studied in detail in the beginning of the current thesis work and it was decided to address and improve the anti-alias filtering capability of this receiver by studying and proposing an innovative filtering solution.

Interesting to note is the fact that, although intended for multi-standard applications and even for software defined radios, most of the receiver realizations

presented above have supported only one communication standard (or a quad standard with almost the same specifications).

In this thesis, a discrete-time RF sampling receiver is proposed for a GSM900 and 802.11g dual-mode operation. Each mode has its own frequency plan and filter partitioning (depending of the standard specifications). This attempt should validate the reconfiguration mechanisms and point out the main difficulties (both at system and circuit levels) that might exist when dealing with multi-standard receivers.

### 3.4.2 Charge sampling circuits

Karvonen et al. noticed the advantage of using the intrinsic continuous-time sinc function in charge sampling and proposed a quadrature charge-domain sampler with embedded FIR and IIR filtering functions [27, 22, 21]. The composite filtering of the CT built-in sinc function in charge sampling and the embedded FIR, IIR filtering functions integrated into the sampling process would improve the noise aliasing suppression. The function of discrete-time FIR filtering is realized by the multiple accumulation of charge into the sampling capacitors [28, 29]. Different integration of input current results in different sequences of weights that correspond to the filtering coefficients.

Gang Xu was also interested in charge sampling circuits. In his research work, he provides a theoretical basis for the charge sampling technique and presents a model of the charge domain sample-and-hold circuit [68, 65, 66]. He also implements charge FIR filters [67, 64] based on the principle of charge sampling.

Besides bandpass charge sampling, it is also possible to introduce FIR and IIR filtering into bandpass voltage sampling. For bandpass charge sampling, the frequency downconversion is realized by decimating a high rate integrated value. However, it is possible to realize sampling, filtering and frequency downconversion at the same time in the process of voltage sampling by using complex FIR filtering [57, 56].

### 3.4.3 Anti-alias filtering

As already mentioned in the study of bandpass sampling, the anti-alias filter has a major role as it prevents unwanted interferers to fold on top of the desired signal and degrade the receiver performances. For stringent communication standards such as GSM, more than 100 dB of alias rejection are required (in case of bandpass sampling) and can be achieved only by using high-order filters. Works on such anti-alias filters have been reported in the literature, most of them requiring an active elements when implemented on circuit.

In [37], a  $\text{sinc}^2$  filter (intended for software defined radios) was designed by cascading two  $G_m - C$  integrators. The filter was implemented in  $0.13 - \mu\text{m}$  CMOS technology and 45dB of alias rejection was measured at the first zero (notch) using a 40 MHz sampling rate.

A complex bandpass third-order sinc-type FIR filter was implemented in [28, 26] using a current mode active switch network. The filter implementation required an active element (for integrating the input current on capacitors).

In this thesis, a fully passive second order sinc-type anti-alias filter is proposed. The filter is based on coefficient weighting through capacitive ratios and

does not necessitate active elements (except the input transconductance element), hence reducing the power consumption. The filter is intended for use in the proposed GSM900 and 802.11g dual-mode discrete-time receiver.

### 3.5 Conclusion

This chapter introduced the concepts of bandpass sampling (for frequency down-conversion) and charge domain sampling (for inherent anti-alias filtering). Previous realizations of discrete-time RF sampling receivers were also presented.

In the next chapter, a discrete-time receiver architecture will be proposed, with the two major contributions being (1) multi-standard capability by supporting both GSM900 and 802.11g standards and (2) fully passive second order anti-alias filtering for improved alias rejection.



# Chapter 4

## Proposed receiver architecture

### 4.1 Introduction

In this chapter, we present the architecture of the proposed receiver front-end and detail the system level design as well. It is important to note from the start that the performances of the receiver are closely dependent on various circuit parameters, which imposes a minimum knowledge of the circuit topology even at system level. Although some circuit schematics will be briefly presented here, the reader is invited to refer to the next chapter for further details concerning the front-end circuit design.

The targeted GSM900 and 802.11g communication standards are first presented, focusing on their most important specifications. The block diagram of the receiver is then presented along with the frequency plans for both modes. The second order anti-alias filter is detailed and the computation of the FIR coefficients explained. The reconfigurability and control mechanisms for switching between both communication modes are also described. Finally, the RF system design is detailed, with a special focus on filtering requirements and gain/noise analysis.

### 4.2 Targeted standards

This section gives a brief summary and description of the communication standards under consideration. It was decided to validate the reconfigurability of the proposed receiver using the GSM 900 and 802.11g standards. This choice was motivated by the complementarity between these two standards in term of signal bandwidth, power levels and filtering requirements.

It was also decided that system level design would focus primarily on gain, noise and filtering. The linearity aspect will not be taken into account during system specification but will be, nevertheless, simulated and measured later through intermodulation tests. Hence, only noise figure and filtering requirements will be discussed in this section. For further details, the reader is referred to the official specifications of GSM [1] and 802.11g [13] standards.

### 4.2.1 GSM specifications

GSM is the acronym for “Global System for Mobile Communications” and is certainly the most widely used cellular standard in the world. GSM is based on Time-Division Multiple Access (TDMA) and Frequency-Division Duplexing (FDD). It also uses a Gaussian Minimum Shift Keying (GMSK) modulation scheme. It has a transmit band of 890-915 MHz and a receive band of 945-960 MHz. Each communication channel is 200 KHz wide and allows eight multiplexed users, for a final data rate of 270 kb/s.

#### Sensitivity and noise figure requirements

The GSM reference sensitivity level is shown in Table 4.1, along with the signal to noise ratio required to maintain the minimum BER outlined in the standard ( $10^{-3}$ ) and with the resulting noise figure as well.

Sensitivity (dBm)	Input Noise (dBm)	SNR <sub>min</sub> (dB)	NF (dB)
-102	-120.8	9	9.8

Table 4.1: GSM sensitivity and signal levels

#### Blocking requirements

The blocking profile for GSM 900 is shown in Fig. 4.1. By far, one of the most difficult specifications to meet is the 3 MHz blocker which is typically 76 dB above the carrier. The blocking test for GSM is performed by applying a GMSK modulated desired signal 3dB above the reference sensitivity level, together with a simple sinewave at discrete increments of 200 kHz from the desired signal.

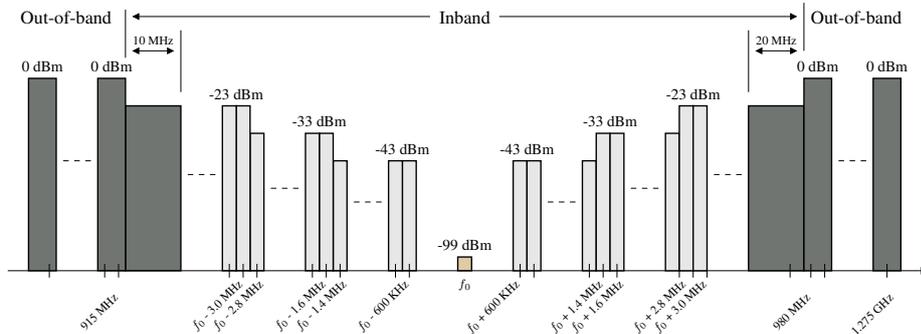


Figure 4.1: Blocking profile for GSM 900

The GSM standard allows for “spurious response frequencies”, which are a set of exceptions that relax the requirements in a selected range of frequencies. This can be helpful in situations where an out-of-band blocker happens to be  $kF_s$  away from the carrier frequency, in which case it also becomes an aliasing interferer.

When a spurious response frequency is selected the blocking requirement is relaxed to -49 dBm at the frequency which the blocker is applied. For each com-

munication channel, 6 inband and 24 out-of-band frequencies may be selected with a maximum of three adjacent frequencies assigned as spurious response exceptions.

### Adjacent requirements

The reference interference ratio for adjacent channels ( $C/I_a$ ) is specified in Table 4.2. Also called “Adjacent Channel Selectivity”, this criteria gives a measure of the receiver’s ability to process a desired signal while rejecting a strong signal in an adjacent frequency channel.

	$C/I_a$ (dB)	Channel level (dBm)
signal channel ( $F_0$ )	–	-82
1 <sup>st</sup> adjacent ( $F_0 \pm 200$ KHz)	-9	-73
2 <sup>nd</sup> adjacent ( $F_0 \pm 400$ KHz)	-41	-41
3 <sup>rd</sup> adjacent ( $F_0 \pm 600$ KHz)	-49	-33

Table 4.2: GSM adjacent channel selectivity

In the proposed receiver, most of the GSM channel filtering is performed in the analog domain, but should be completed digitally after the A/D conversion in order to meet the standard specifications.

### 4.2.2 802.11g specifications

Introduced in 2003, the 802.11g WLAN standard combines the best of both 802.11a and 802.11b. Also called WIFI, it works in the 2.4 GHz and operates at a maximum data rate of 54 Mbit/s. The modulation scheme used in 802.11g is Orthogonal Frequency Division Multiplexing (OFDM) for all data rates above 20 Mbit/s. It also implements Complementary Code Keying (CCK) at lower data rates, for full backward compatibility with 802.11b standard.

In Europe, the 802.11g standard operates in the 2400 - 2484 MHz frequency range and allows both non-overlapping (3 channels) and overlapping (7 channels) modes, as shown in Fig. 4.2. Each communication channel is 20 MHz wide.

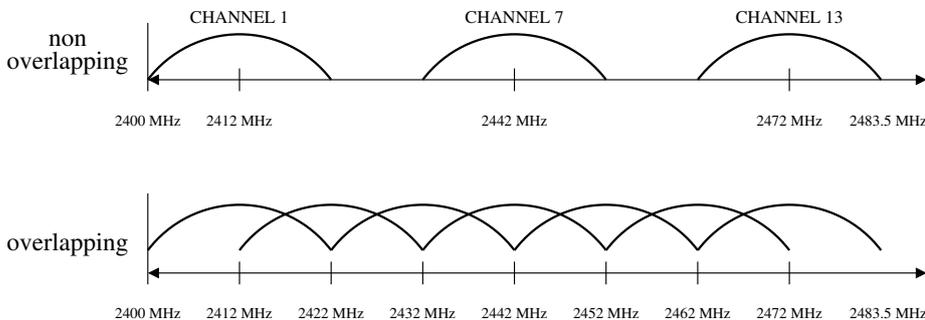


Figure 4.2: 802.11g European operating channels

### Sensitivity and noise figure requirements

The 802.11g minimum input level sensitivity is shown in Table 4.3 for a data rate of 54 Mbit/s. The required signal-to-noise ratio is defined for a packet error rate (PER) of 10%. Note that the receiver sensitivity is given for a specific data rate, because each modulation scheme has its own SNR requirements. In general, the higher the data rate, the higher the SNR required and hence the higher the receiver sensitivity level. During the design of the proposed receiver, we will concentrate only on the 54 Mbit/s transmission mode.

Sensitivity (dBm)	Input Noise (dBm)	SNR <sub>min</sub> (dB)	NF (dB)
-65	-101.8	21.1	15.7

Table 4.3: 802.11g sensitivity and signal levels

Each OFDM channel is split into 64 subcarriers, but only 53 subcarriers are actually carrying useful signal data. For the computation of the input noise level, it was thus considered that thermal noise is integrated only over a 53/64 fraction of the 20 MHz channel bandwidth, giving :

$$N_{\text{Floor}} = -173.8 + 10 \log\left(\frac{53}{64} \cdot 20\text{MHz}\right) = -101.8\text{dBm}$$

### Adjacent channel rejection

The adjacent channel rejection is measured by setting the desired signal's power 3 dB above the reference sensitivity level and raising the power of the interfering signal (also an OFDM signal) until a PER of 10% is caused. The power difference between the interfering and the desired channel is the corresponding adjacent channel rejection. The 802.11g standard specifies a minimum rejection for both the adjacent (N+1) and the alternate (N+2) channels, as shown in Fig. 4.3.

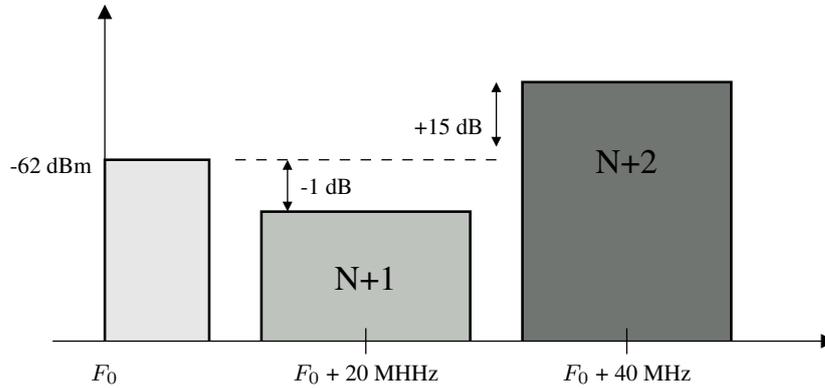


Figure 4.3: 802.11g adjacent channel rejection

### Alias rejection

By contrast with GSM standard, the 802.11g specifications are less precise about out-of-band blockers and interferers. Co-existence with other wireless standards

in the 2.4 GHz band (such as Bluetooth) and vicinity to 3G spectrum bands makes it even more difficult to accurately predict the nature and power levels of the aliasing components.

This prediction requires a minimum knowledge of the sampling frequencies used within the receiver front-end. In the proposed design, it will be assumed a maximum level of  $-20$  dBm for the aliasing components (which could simulate the folding of a WCDMA channel from the UMTS band).

### 4.2.3 Scaled-down version of 802.11g

When the design of the receiver front-end was initiated, it was at first planned to implement GSM 900 and 802.11g standards. The different frequency plans and filtering schemes imagined for each standard provided an excellent way for the validation of the receiver's reconfigurability.

However, as the project progressed, it became clear that the implementation of the 802.11g standard would suffer some limitations. Due to time constraints, it was indeed impossible to design an LNTA for the 2.4 GHz band.

As an alternative, it was then proposed to re-use the GSM mode LNTA (which bandwidth extended to over 1.1 GHz) and implement a scaled-down version of the 802.11g standard. In this version, the frequency band would be shifted from 2.4 to 1.0 GHz and the channel bandwidth reduced accordingly by a factor  $1/2.4$ . All the 802.11g standard specifications (sensitivity, adjacent channel rejection) would, however, remain unchanged.

Even if the true 802.11g standard is not supported, implementing both GSM and WIFI scaled-down version is sufficient to validate the reconfigurability of the receiver. Moreover, by respecting the same standard specifications, we ensure full functionality in real 802.11g mode for future versions of the receiver (with a dedicated 2.4 GHz LNTA).

## 4.3 Architecture overview

The proposed receiver is similar in principle to the state-of-the-art discrete-time radios described in the previous chapter [19, 41]. It is supposed, however, to show better alias rejection performances (thanks to the second order FIR filter) and was designed as a fully reconfigurable dual-mode receiver.

The architecture of the receiver is presented in Fig. 4.4. It comprises an RF filter, a transconductance LNA, two discrete-time analog signal processing stages and analog to digital converters. The RF input signal is first filtered, amplified and converted to a current. It is then fed to a first DTASP block, where it gets IIR/FIR filtered and quadrature downconverted to a first intermediate frequency. A second downconversion stage further decimate the sampling ratio and filters the IF signal before it gets finally A/D converted.

### 4.3.1 RF stage

As already mentioned, RF filters limit the reconfigurability of multistandard receivers and current research works toward the suppression of these filters. In the proposed design, it was however decided to keep the RF filter, as it relaxes the requirements on both the LNA and anti-alias filter.

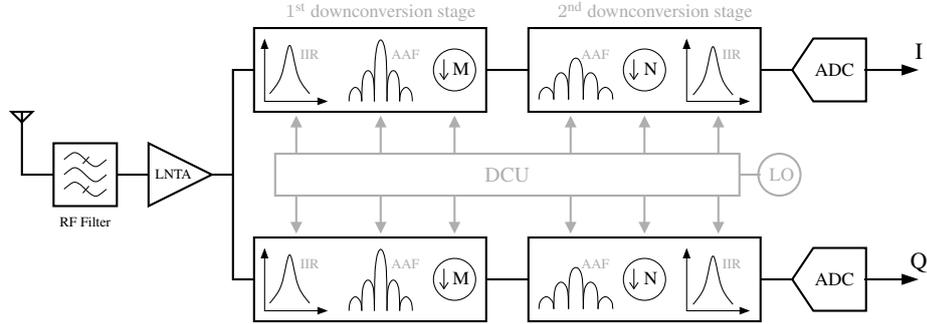


Figure 4.4: Proposed receiver architecture

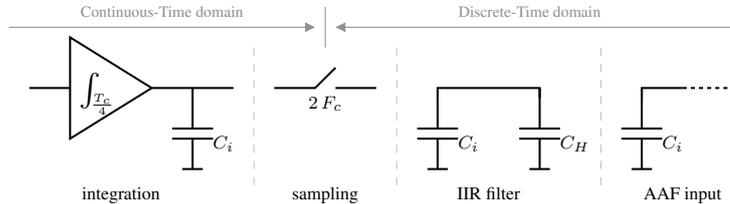
In the current topology, only one transconductance LNA is used and the input current is permanently switched between the in-phase and quadrature paths. This minimizes the I/Q gain mismatches and improves the image rejection of the receiver. The downside is that the integration period is halved in this case, which in turn halves the LNA gain. Great attention must also be paid to the generation of the clock signals. In fact, overlapping between I/Q successive sampling phases can shorten the quadrature paths and destruct the signal's content.

### 4.3.2 First DTASP stage

The LNTA output current is integrated during a  $T_c/4$  time interval, on both a history capacitor (from the IIR filter) and a unit capacitor (from the AAF stage), alternately between the I and Q paths. This results in a sampled data stream with a sampling rate of  $2F_c$  per quadrature path.

The IIR filter is as usual required to prevent the LNTA's output from saturating and is made of a single pole. However, by contrast to the previous GSM receiver, it is now preceding the AAF/decimation stage, meaning that the history capacitors will be switched at a rate of  $2F_c$  rather than  $F_s$ .

It is not obvious to define the boundary between the continuous and discrete time domains due to the simultaneity of current integration and IIR filtering. The operation of the 1<sup>st</sup> DTASP block is fractioned in Fig. 4.5 and although virtual, it may help for a better understanding.

Figure 4.5: Fractioned operation of the 1<sup>st</sup> DTASP block

The operation can be viewed as a series connection of first a current integrator, then a voltage sampler and finally a discrete-time IIR filter. The transition from continuous-time to discrete-time occurs at the output of the simplistic

sampler. The first decimation stage is preceded by a 2<sup>nd</sup> order anti-alias filter, which should theoretically square the rejection achieved in the previous design. The desired signal is downconverted through the decimation process to a first intermediate frequency and fed to a second DTASP block.

The operation of the first DTASP stage is somehow different from the previous realizations in that it doesn't use mixers. The input current is now integrated on the unit capacitors in always the same direction (no more switching).

The RF signal is sampled at a frequency rate of  $2F_c$  which results in a first spectrum folding, depicted in Fig. 4.6.

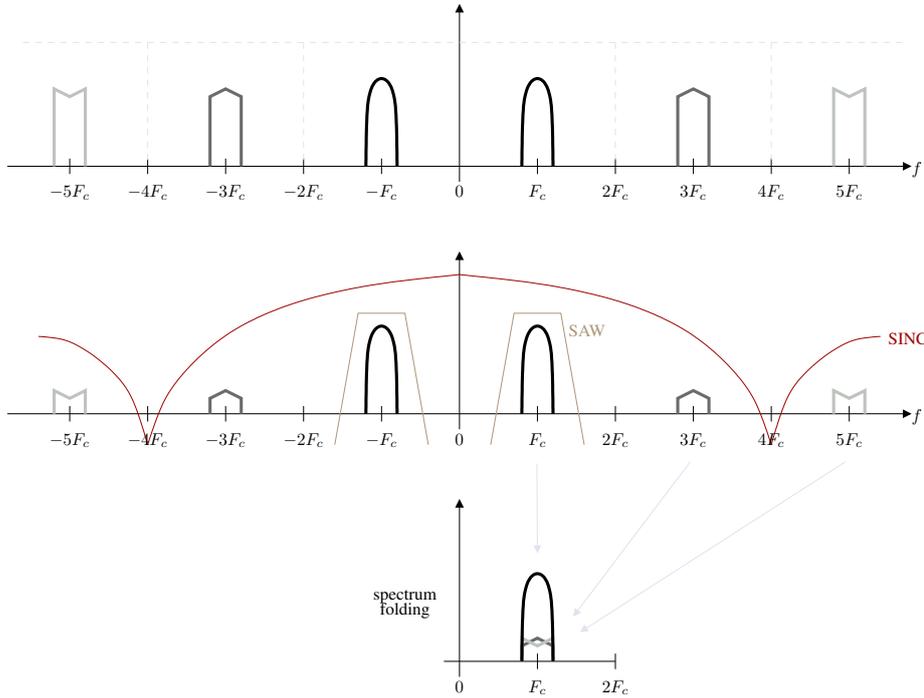


Figure 4.6: Spectrum folding during first sampling

It is important to note that this first sampling doesn't have any dedicated anti-alias filter and benefits only from the attenuations brought by the RF SAW and continuous-time *sinc* filters. The desired signal at frequency  $F_c$  is not shifted during the sampling process. The alias component located at frequency  $3F_c$  is folded on top of the desired signal. In GSM mode, this alias will still have a considerable power level even after attenuation (by SAW and *sinc* filters) and may require the use of frequency exceptions to meet the standard specifications [1].

### 4.3.3 Second DTASP stage

This stage performs a second decimation of the sampling rate and further reduces the signal dynamic through a second IIR filter (one single pole). The decimation is less critical in this stage as it profits from the previous IIR filtering and a first order anti-alias filter was sufficient in this case. The signal

is downconverted to a second intermediate frequency and is directly fed to the A/D converter.

#### 4.3.4 A/D conversion

In the proposed receiver, it was decided to reuse the  $\Sigma\Delta$  modulator of the previous design for the analog to digital conversion in GSM mode.

$\Sigma\Delta$  modulators are indeed suitable for narrow band standards, where the quantification noise can be efficiently shifted out from the signal bandwidth. However, to keep these performances with wideband standards, it is also necessary to increase the oversampling ratio, the number of bits or the modulator's order, which leads to more design complexity. Hence, replacing the architecture of the A/D converter becomes the best alternative in this case.

In WIFI mode, it was preferred to use a SAR (Successive Approximation Register) converter, instead of reconfiguring the GSM  $\Sigma\Delta$  modulator or using another one. Actually, the current version of the proposed receiver does not include any A/D converter for the 802.11g mode. It was supposed, however, that a 8 bits SAR converter (designed at STMicroelectronics [39]) will be used in the future and the receiver was specified at system level for full compatibility with this converter.

## 4.4 Frequency plan

The frequency plans proposed for each of the GSM/WIFI modes are detailed in this section. Values for decimation ratios, sampling and intermediate frequencies will be given as well.

### 4.4.1 GSM mode

The frequency plan of the GSM mode is depicted in Fig. 4.7 for one quadrature path. The desired signal is always centered at half the sampling frequency ( $F_s/2$ ) to avoid degradations caused by flicker noise and IM2 products and is assured by setting the decimation ratios to odd values.

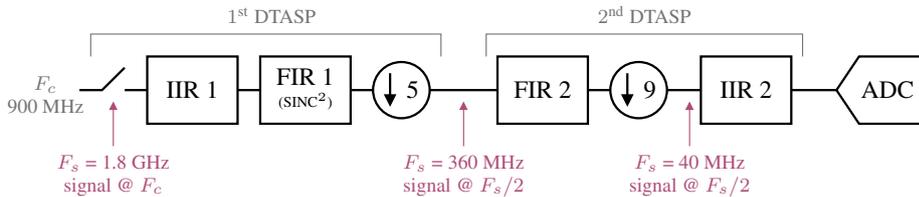


Figure 4.7: GSM mode frequency plan

The first decimation ratio is dictated by the anti-alias requirement, since alias rejection is directly proportional to signal bandwidth over sampling frequency ratio. For a second order anti-alias filter, this rejection is given by :

$$20 \log \left( \frac{2F_s}{BW} \right)^2 \geq P_{\text{alias}} - S_{\text{dBm}} + \text{SNR}_{\text{min}}$$

which imposes a minimum sampling frequency of :

$$F_{s,min} = \frac{200 \text{ kHz}}{2} \cdot 10^{(-111/40)} \simeq 60 \text{ MHz}$$

Note that this expression does not account for the attenuation brought by the SAW filter, and even in this case, has resulted in a considerably low sampling frequency. This is however a theoretical value. In practice, capacitor mismatches at circuit level degrade the notches of the anti-alias filter and forces the use of much higher sampling frequencies.

Also, setting a low value for the sampling frequency results in a high decimation ratio, which in turn increases the complexity of the filter circuit design (longer rotating capacitor banks). It was decided, here, to set the first decimation ratio to  $M_1 = 5$ , leading to a sampling frequency of 360 MHz and to a first intermediate frequency of 180 MHz.

The second DTASP stage must adapt the sampling rate to the 40 MS/s  $\Sigma\Delta$  ADC constraint. The second decimation ratio is then set to  $M_2 = 360/40 = 9$  and the signal is downconverted to a second intermediate frequency of 20 MHz.

#### 4.4.2 802.11g mode

In 802.11g mode, the large channel bandwidth makes the flicker noise less significant.  $F_s/2$  architecture does not provide advantage anymore and the desired signal can be downconverted and processed directly at DC (Zero IF). The RF signal is first sampled at twice the channel frequency ( $2F_c$ ), similarly to the GSM mode. IIR and anti-alias filters are still centered around the RF channel ( $F_s/2$  scheme). The signal is then downconverted to DC by setting the decimation ratio to an even value.

In this configuration, the RF stage remains unchanged and the anti-alias filter is the only block that has to be reconfigured. Note however, that the sampling frequency reaches in real WIFI mode a value of  $4F_c \simeq 9.6$  GHz (when considering both I/Q paths) which puts severe constraints on both analog and digital parts. It is indeed difficult to obtain sharp  $T_c/4$  edges at such high frequencies and technology limits are quickly reached. For the current implementation of the receiver, only the scaled-down version of the 802.11g standard will be actually supported and sampling at twice the channel frequency is not problematic ( $4F_c \simeq 4.0$  GHz).

The frequency plan for WIFI mode is given in Fig. 4.8. Only the first DTASP stage is actually implemented on circuit. The second downconversion stage and the A/D converter are added to give a complete illustration of a possible future version of the receiver.

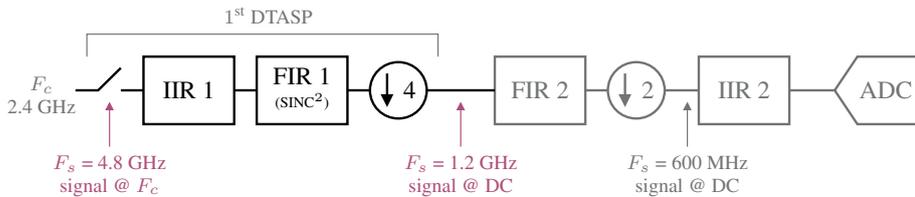


Figure 4.8: WIFI mode frequency plan

Like in GSM mode, the first decimation ratio is dictated by the alias rejection requirements. Using the same second order anti-alias filter, the minimum sampling frequency is now equal to :

$$F_{s,min} = \frac{20 \text{ MHz}}{2} \cdot 10^{(-20+65+21.1)/40} \simeq 450 \text{ MHz}$$

Again, the sampling frequency was set to a much higher value than the minimum required, to account for notch degradations at circuit level. The decimation ratio was set to  $M_1 = 4$  in order to facilitate the reconfigurability of the anti-alias filter. Once downconverted to DC, the signal is buffered and outputted for measurement. The second DTASP stage (which is not implemented) includes a first order anti-alias filter, a decimation by  $M_2 = 2$  and a single pole IIR filter. The sampling rate is lowered to 600 MHz and the signal is fed to the SAR converter for digitization.

## 4.5 Second order anti-alias filter

As previously mentioned, one major goal of the thesis work was to address the lack of alias rejection noticed within state-of-the-art discrete time receivers. For this, a second order anti-alias filter was proposed and implemented in the first downconversion stage. By contrast to [37], where two active transconductance amplifiers were required, the proposed AAF is fully passive and is based only on switched capacitors. The discrete-time operation of the filter is presented here using a digital signal processing approach.

### 4.5.1 Principle

In the first downconversion stage, the anti-alias filter should be centered at  $F_c$  and should have notches at frequencies  $F_c \pm kF_s$ . In digital signal processing, bandpass filters can be easily designed if centered at half the frequency of operation ( $F_s/2$ ). This explains why the first sampling frequency, at the beginning of the receive path, was set to  $2F_c$ .

The construction of the AAF will be presented with two different approaches. The first one is based on a comb filter transformation, while the second one uses classic pole-zero placement.

#### Comb filter transformation

In this approach, we start with a comb filter (moving average) having a length equal to the first decimation ratio  $M = 2F_c/F_s$ . Then, we square the transfer function and perform a lowpass to highpass transformation ( $z^{-1} \rightarrow -z^{-1}$ ) to obtain a second order filter centered at half the sampling rate (i.e. at the channel frequency  $F_c$ ). The transfer function of the anti-alias filter is expressed by :

$$\begin{aligned} H(z) &= \mathcal{T}_{L \rightarrow H} \left( \sum_{k=0}^{M-1} z^{-k} \right)^2 \\ &= \left( \sum_{k=0}^{M-1} (-1)^k z^{-k} \right)^2 \end{aligned} \quad (4.1)$$

The resulting FIR filter coefficients are given in Table 4.4 for both GSM and WIFI modes. Note that the length of the coefficient vector is greater than the decimation ratio  $M$ , which means that a time period larger than  $M/2F_c = T_s$  is required to output a single sample.

mode	↓ M ratio	FIR coefficients
GSM	5	[+1 -2 +3 -4 +5 -4 +3 -2 +1 0]
WIFI	4	[+1 -2 +3 -4 +3 -2 +1 0]

Table 4.4: FIR filter coefficients for GSM and WIFI modes

By appending a zero, the length of the FIR coefficient vector becomes equal to  $2M$  (equivalent to a time period of  $2T_s$ ), meaning that at least two parallel paths will be required. This point will be further detailed later in this section.

### Pole-zero placement

The construction of the anti-alias filter by pole-zero placement offers more control over the location of the notches. Instead of having a double zero at the exact center of the aliasing frequencies, it is possible to place two distinct zeros at the edges of each aliasing channel band (i.e.  $F_c \pm kF_s \pm BW/2$ ). This can be useful in the case of a wideband standard. The resulting frequency response is compared in Fig. 4.9 to the double zero filtering (in WIFI mode). Depending on the location of the notches, the rejection can be made higher either at the borders or at the center of the aliased channel band.

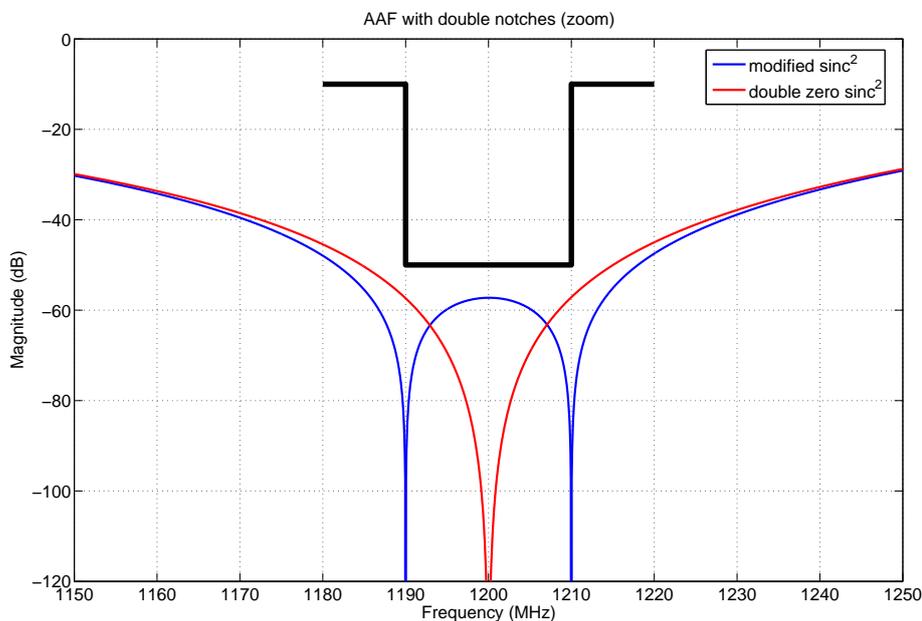


Figure 4.9: Notch placement in anti-alias filtering

In the case of a distinct notches placement, the FIR transfer function can

be retrieved directly from the expression of the zeros, which gives :

$$\begin{aligned} H(z) &= \prod_{k=1}^{M-1} (1 - z_k z^{-k}) \quad \text{where } z_k = e^{j2\pi(F_c \pm BW/2 + kF_s)/2F_c} \\ &= \sum_{k=0}^{2M-2} b_k z^{-k} \end{aligned}$$

The resulting FIR filter coefficients are given in Table 4.5 for the WIFI mode. Scilab simulations show that any imprecision or quantification attempt over these coefficients severely degrade the sharpness of the notches. Actually, it is not possible to reach such fractional accuracy when using standard analog processing techniques. This usually makes impractical the circuit implementation of these filtering functions.

k	0	1	2	3	4	5	6
$b_k$	+1	-1.9998	+2.9993	-3.9983	+2.9993	-1.9998	+1
$E[b_k]$	+1	-2	+3	-4	+3	-2	+1

Table 4.5: FIR coefficients in distinct zeros configuration

It is interesting to note that the integer part of these coefficients results in the same values as for the previous double zeros configuration. For the proposed receiver, the second order anti-alias filter will be based on this first scheme as it can be more easily implemented.

#### 4.5.2 Coefficient implementation

The FIR filter coefficients are implemented at circuit level using a passive charge division technique [33]. A set of  $M$  unit capacitors is assigned to each coefficient. The input current is first integrated on the whole set of unit capacitors during an integration period  $T_i = T_c/4$ . Then, to form the  $k^{th}$  tap coefficient, only  $k$  capacitors are selected and connected to the output. In this way, only a fraction  $|\alpha_k| = k/M$  of the initial integrated charge will be actually used. The sign and complex nature of each coefficient  $\alpha_k$  will be defined next, when connecting the capacitor array to the output (direct or inverted connection, real or imaginary path). The charge division is depicted in Fig. 4.10 for the GSM case, where the implementation of each coefficient requires  $M = 5$  unit capacitors.

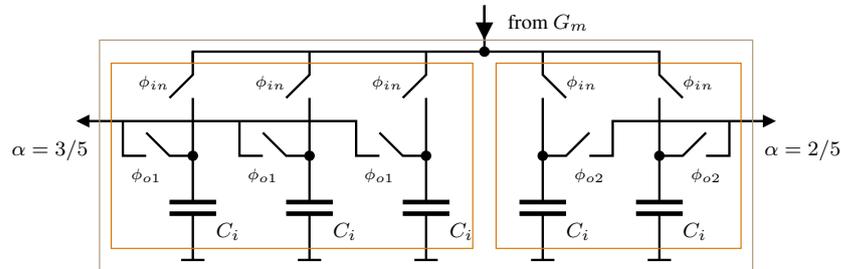


Figure 4.10: Coefficient implementation through charge division

As previously mentioned, the length of the FIR filter is nearly equal to  $2T_s$  (twice the output sampling period) and a time-interleaved structure is thus necessary to keep the sampling rate at the desired value of  $F_s$ . Additional time must be reserved for charge read-out and reset operations and three parallel paths will be finally implemented, as illustrated in Fig. 4.11 for the GSM mode.

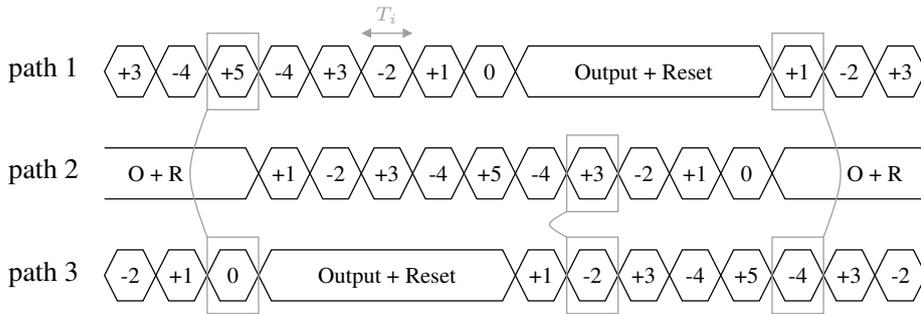


Figure 4.11: Arrangement of parallel integration paths in GSM mode

It is interesting to note the existence of an M-complementarity between the coefficients of any two of the three parallel paths. A single capacitor array can therefore be used to form two complementary coefficients at the same time. When using a capacitor array to form an  $\alpha_k$  coefficient, it is also possible to form the  $\alpha_{|M-k|}$  complementary coefficient by simply collecting the charge on the remaining  $M - k$  capacitors (Fig. 4.10). This optimised scheme can reduce power consumption and save up to 50% of the anti-alias filter circuit area.

At circuit level, the filter will be composed of three distinct banks of M capacitor arrays, properly arranged to emulate three parallel integration paths with a global sampling rate of  $F_s$ . Each output sample will require the combination of two banks, and at the same time, each bank will contribute for two consecutive output samples (L-complementarity). This time-interleaved operation is better described in Fig. 4.12.

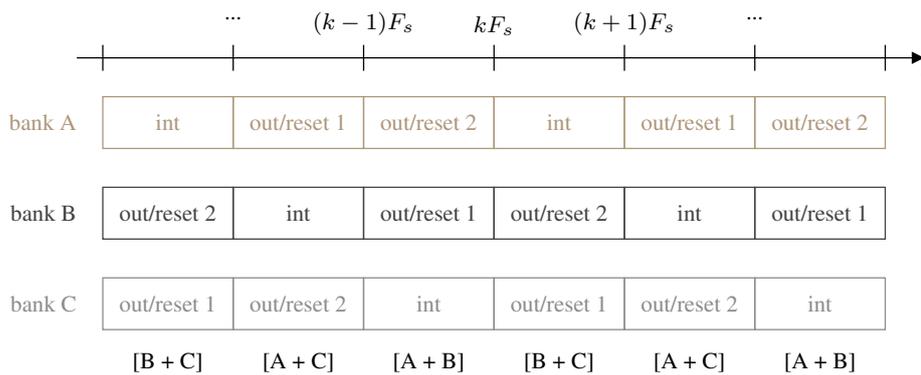


Figure 4.12: Timing diagram for interleaved AAF operation

A comparison with the anti-alias filter from the previous GSM receiver can be established at this point. Each rotating capacitor is now replaced by more than 40 switched capacitors. The number of required clock phases has jumped

from 4 (mixer signals I+ Q+ I- Q-) to more than 30. The complexity of the second order AAF is thus order of magnitude higher, and even if the filter is fully passive, it should be noted that the digital control unit considerably increase the overall power consumption. The complexity of the proposed anti-alias filter is nearly the same as for high order filters based on switched current division techniques [20, 25, 23].

### 4.5.3 Rejection estimation

By contrast with the previous GSM receiver, the alias rejection is not altered here by the LNA output capacitor because the unit capacitors of the AAF stage are not rotated around  $C_{LNA}$  (mixer effect). The LNA parasitic capacitor may lead some gain loss but does not affect the depth of the notches.

The limitation of the proposed anti-alias filter comes actually from circuit level mismatches. Accuracy on the FIR coefficients depends on how much the input current is equally divided between the M unit capacitors of each coefficient cell (Fig. 4.10). If the layout is made symmetrical, accurate division is then limited only by capacitor mismatches. The degradation of the notches is simulated in Fig. 4.13 with the predicted mismatch value for the current technology and capacitor type ( $\sigma(\Delta C/C) = 0.1\%$ ).

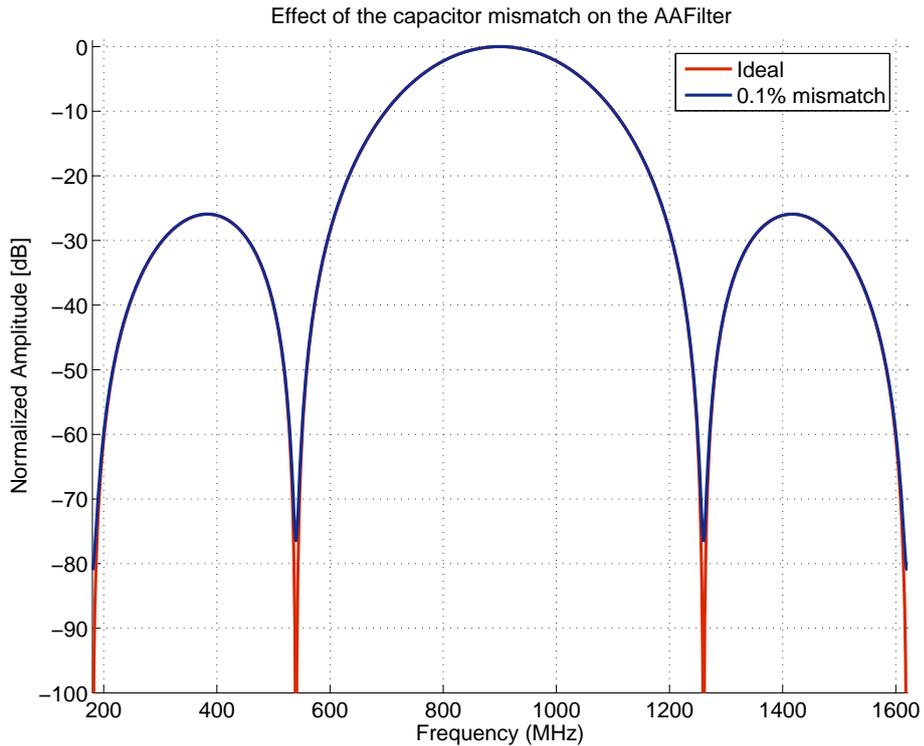


Figure 4.13: Notch degradation due to circuit level mismatches

The alias rejection in GSM mode is estimated to 75 dB, which is almost half the theoretical value. The performances of the proposed filter are considerably

degraded by circuit mismatches, but are still superior to the rejection of the first order AAF. Moreover, capacitor mismatches are expected to lower with technology scaling and in consequence, the alias rejection will less degrade with design portability.

## 4.6 Receiver system design

The system level design consists in defining the block specifications of a pre-defined architecture, given one or more target communication standards [12]. Although prior to circuit implementation, system level design often requires a minimum knowledge of the circuit's topology. In the case of a discrete time receiver based on switched capacitors, parameters such as the number of unit capacitors and the on-resistance of the unit switches may be required. This is because such parameters affect all of the gain, noise and filtering performances and hence must be taken into account at an early stage. System level and circuit level design phases are in this way mutually dependent, which forces the designer to loop several times through the specification/design/extraction process.

It should be noted that for clarity reasons, various circuit aspects will to be introduced at this point. The reader is nevertheless referred to the next chapter for a more detailed analysis of these aspects.

### 4.6.1 Design guidelines

As previously mentioned, the system level study will focus mainly on the distribution of gain, noise and filtering along the receive path.

**Gain/Noise** As the transconductance LNA is the only active stage within the receiver, the noise added by the following blocks must be kept as low as possible. Gain losses due to parasitic capacitances and charge averaging between successive filtering stages must be minimized. To optimize the overall noise figure of the receiver, the gain and noise contribution of each block must be determined analytically and then solved. This operation usually leads to the optimal value that should be used for the unit capacitors.

**Filtering** The required filtering is dictated by the available dynamic ranges at both the output of the LNTA and at the input of the A/D converter. In-band blockers and adjacent channels must be sufficiently filtered to fit into the available ADC dynamic range. Usually, the required rejections determine the values of the different history capacitors, once the values of the unit capacitors are fixed.

The circuit parameters to be specified here are illustrated in Fig. 4.14 and consist basically in values of capacitors and switches on-resistances. These parameters are most of the time correlated and they usually affect gain, noise and filtering at the same time, which is at the origin of the system design complexity. For example, the on-resistance of the unit switches must be kept low not to affect the IIR filtering, which in turn can result in higher parasitic capacitances (larger transistors) and leads thus to gain and IIR losses.

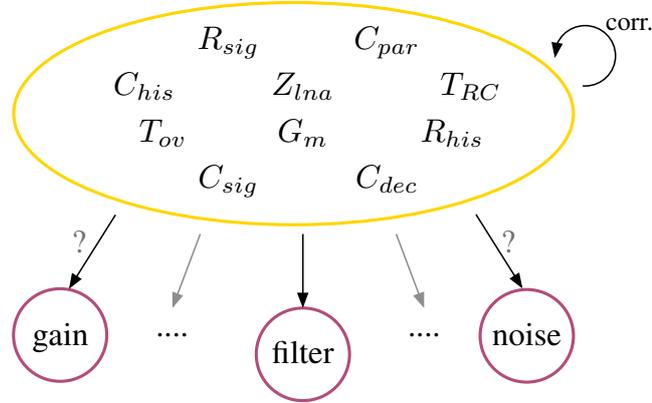


Figure 4.14: Circuit parameters to be specified at system level

For the proposed architecture, the most problematic point to analyze is the transition from continuous time to discrete time domains. This transition happens at the output of the LNA and the signal processing performed at this level cannot be expressed in standard  $s$  or  $z$  domains. Thus, not all the circuit parameters can be specified analytically (by solving a system of equations) and transient analysis simulations are most of the time required to complete the specification task.

#### 4.6.2 System level description

A simplified schematic showing the connection of the LNTA to the first DTASP stage is given in Fig. 4.15. In this schematic, the LNTA is represented by a transconductance stage  $G_m$  that converts the input RF voltage into a current signal. The LNA output impedance is efficiently modeled by the  $C_{lna}$  capacitor and  $R_{lna}$  resistor, which values are extracted from transistor level simulations.

The first DTASP stage is connected to the LNTA output via two decoupling capacitors  $C_{dec}$  in order to set a different DC level at each side. Both the in-phase and quadrature paths are illustrated on the schematic. In each path, the IIR filter stage is represented by a history capacitor  $C_{his}$  and two resistors  $R_{his}$  that account for the ON resistance of the capacitor switches. Similarly, the input stage of the anti-alias filter is represented by  $M$  parallel branches, each one containing a unit capacitor  $C_{sig}$  and two resistors  $R_i$ .

The  $C_{par}$  capacitor connected between nodes  $X_p$  and  $X_n$  represents the sum of the parasitic capacitances contributed by the switch transistors, the  $C_{dec}$  capacitors and all the metal layers used for routing. The  $C_{par}$  capacitor is always connected in parallel to the unit capacitors  $C_{sig}$  and a fraction of the input RF current is integrated on this capacitor, resulting in a considerable gain loss (possibly more than 3 dB). Note also that the  $C_{par}$  capacitor is constantly shared between the in-phase and quadrature paths which degrades the image rejection of the receiver.

As previously mentioned, the values of the resistors and capacitors illustrated in Fig. 4.15 strongly affect the performances of the receiver and the optimisation of these values is only possible through transient simulations (due to the complex

nature of the signal processing performed at the LNA's output). Transient simulations using a Spice like simulator are however time consuming and it was instead decided to perform a nodal analysis on Scilab.

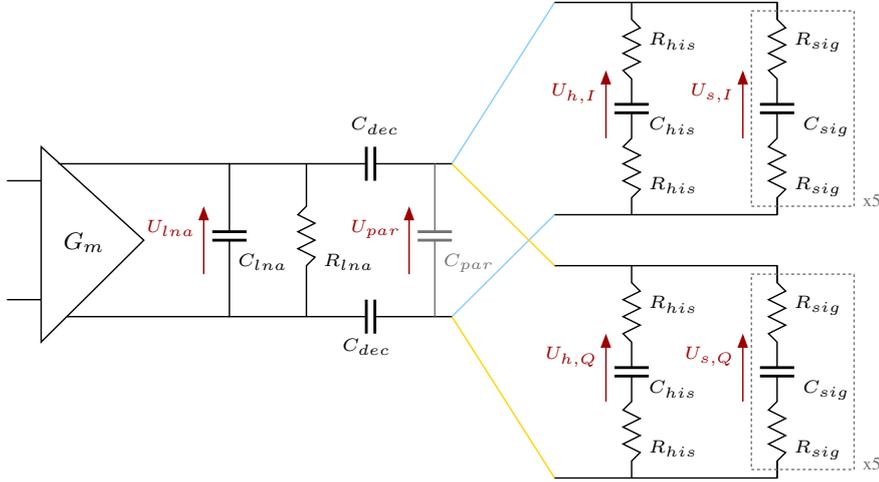


Figure 4.15: Simplified circuit schematic for system analysis

Nodal analysis is the most popular method for determining the node voltages of a given electrical circuit. It relies on Kirchhoff's voltage and current laws to describe the behaviour of the network. The resulting equations are arranged in matrix and solved to find the node voltages of the circuit.

To analyze the behaviour of the simplified circuit in Fig. 4.15, we first define the node voltages to be solved, as follows:

- $U_{lna}$  voltage at the output of the LNTA
- $U_{par}$  voltage across the parasitic capacitor  $C_{par}$
- $U_{h,I}$  and  $U_{h,Q}$  voltages across the I/Q history capacitors
- $U_{s,I}$  and  $U_{s,Q}$  voltages at the input of the I/Q SINC<sup>2</sup> filters

Then we apply Kirchhoff's first laws to the circuit and arrange the resulting differential equations in a matrix form:

$$A \cdot \frac{dU}{dt} + B \cdot U = C \cdot e^{j\omega t}$$

It is possible here to model the overlapping between the integration phases and evaluate its effects on the performances of the first DTASP stage. The A, B and C matrices are constructed for each of the following operating phases:

1.  $\phi_I$  phase: only the I branch is connected to the output of the LNTA
2.  $\phi_Q$  phase: only the Q branch is connected to the output of the LNTA
3.  $\phi_{ov}$  phase: corresponds to an overlapping phase during which both I and Q branches are connected to the output of the LNTA and where charge sharing between quadrature branches occurs

4.  $\phi_{nl}$  phase: corresponds to the case where the I and Q switch commands are low and during which the input current is lost through the LNTA output impedance and the  $C_{par}$  parasitic capacitor

The mathematics behind the solving of the differential system of equations are explained in Appendix A throughout the Scilab program code. The simulations based on the nodal analysis proved out to be very useful at the beginning of the system study. By entering the values of the capacitors and resistors in Fig. 4.15, it was possible by running the program to get the value of parameters such as:

- Voltage gain of the first DTASP stage for an RF signal centered at  $F_c$
- IIR rejection at a given offset frequency from the RF channel
- Dynamic range at the output of the LNTA in presence of strong in-band blockers

The effects of (1) the parasitic capacitor, (2) the on-resistance of the switches and (3) the LNTA finite output impedance, on gain and filtering can be observed and measured separately. Note that the simulated performances perfectly match the theoretical ones when the parasitic capacitor and switch on-resistance are nulled and when an infinite value is assigned to the LNTA output impedance. Note also that the combination of these three effects results in an important gain loss (not less than 12 dB) and also in a considerable filtering degradation.

The first DTASP stage is simulated for different combinations of capacitor and resistor values until the optimal case (which maximizes the gain and IIR rejection) is found. This usually results in an upper limit for the parasitic capacitor and the switch on-resistances. Actually, the optimization process is much more complex due to the dependence of the parasitic capacitor to many circuit parameters (switch transistor width, history capacitor size, layout routing, ...).

The main advantage of nodal analysis over standard electrical simulation is the considerable reduction of simulation time. This comes from the fact that, here, the time step is fixed and it is sufficient to compute only one simulation point at the end of each sampling phase. Besides, the manual resetting of the  $U_{s,I}$  and  $U_{s,Q}$  node voltages allows to reuse the same unit capacitor over and over. This is not possible with a Spice simulator and thus all the unit capacitors of the anti-alias filter must be considered in the netlist (with all the corresponding clock phases), which dramatically increases the size of the network and hence the computation time.

It is also possible to model the circuit in Fig. 4.15 using a behavioral language such as Verilog-A or VHDL-AMS. The nodal analysis was preferred however, for the ease of interfacing and post-processing offered by Scilab. Finally, note that the performed nodal analysis was purely linear and so did not take into account nor model circuit nonlinearities (such as voltage dependence of the switch on-resistance).

### 4.6.3 Gain/Noise analysis

In this section, we derive the gain and noise contributions of all the circuit blocks, starting from the antenna to the A/D converter. Then, we compute the noise figure of the overall receiver and check whether the minimum output SNR is respected. The analysis is detailed here for only the GSM mode, but performances can be derived for the 802.11g mode in a similar manner.

### Front-end module

In GSM mode, the total insertion loss through the antenna switch and SAW filter is typically about 3.8 dB. For a received signal at reference sensitivity, the signal and noise levels at the input of the LNTA are around -105.8 dBm and -121 dBm respectively, resulting in a minimum SNR of 14.2 dB at LNTA input.

### First DTASP stage

As previously mentioned, the LNTA is the only active stage in the receiver and thus must provide enough gain to compensate for all the following signal attenuations. The maximum gain that must be provided by the LNTA is imposed by the case of RF signals at sensitivity level.

For RF inputs with much higher levels, an attenuation mechanism must be inserted to prevent saturation and subsequent nonlinearities within the following stages. For example, a dummy impedance can be placed at the output of the LNTA. When switched on, this impedance would drive a fraction of the RF current to ground, hence performing a signal attenuation. A more elaborated solution is to redesign the LNTA and implement a variable  $G_m$  transconductance, which value would be adjusted using an AGC algorithm. Note that no attenuation mechanisms were implemented in the proposed receiver as focus was primarily put on reference sensitivity and weak RF inputs.

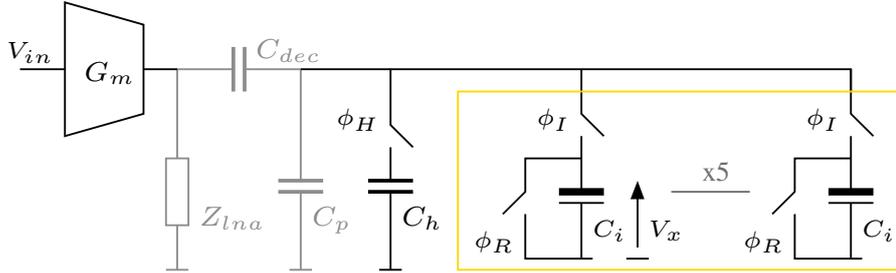


Figure 4.16: Noise at LNTA and IIR stage

The integration of the LNTA current across the unit capacitors of the anti-alias filter ( $M = 5$  in GSM mode) is depicted in Fig 4.16. The voltage gain corresponding to RF current integration is given by:

$$G_1 = \left| \frac{V_x}{V_{in}} \right| = \frac{1}{5C_i} \int_{T_c/4} G_m v_{RF}(t) dt = \frac{G_m}{5C_i} \cdot \frac{1}{\sqrt{2\pi F_c}}$$

where the term in  $1/(\sqrt{2\pi F_c})$  is the gain at the channel frequency  $F_c$  of the continuous time *sinc* filter resulting from the integration of the RF current during  $1/(4F_c)$  time period. Note that the history capacitor does not appear in this formula, simply because the gain of the IIR filter is unity at frequency  $F_c$ .

The parasitic capacitance  $C_p$  contributes to a first degradation of the voltage gain. In fact, every  $T_c/4$  period, a fraction of the LNTA current is integrated into the  $C_p$  capacitor and then charge shared over time. This can be seen as an IIR filter operating at a frequency  $4F_c$  and centered at DC (because the  $C_p$  capacitor is never rotated). The resulting gain degradation can be written as:

$$\begin{aligned}
G_{1,deg} &= \left| \frac{5C_i}{(C_p + C_h + 5C_i) - z^{-1}C_p + z^{-2}C_h} \right| \quad \text{where } z = e^{\frac{j2\pi F_c}{4F_c}} = j \\
&= \left| \frac{5C_i}{(C_p + C_h + 5C_i) + jC_p - C_h} \right| \\
&= \frac{5C_i}{\sqrt{(5C_i + C_p)^2 + C_p^2}}
\end{aligned}$$

The gain degradation due to the parasitic capacitor is considerable. At circuit level, the parasitic capacitance  $C_p$  is expected to be twice as large as the signal capacitance  $5C_i$ , hence degrading the voltage gain by a factor of 11 dB !

Actually, the gain degradation is worse due to the LNTA finite output impedance which deviates a considerable fraction of the output current. This effect cannot be formulated as it was the case for the parasitic capacitor, but it can be confirmed by simulation. Using the Scilab program and setting the LNTA output impedance to an extremely high value, the simulated voltage gain (including the degradation due to the parasitic capacitor) perfectly matches the theoretical one. When setting the output impedance back to its actual value, an additional gain degradation of more than 6 dB becomes visible. This rises the total gain loss through the first DTASP stage to more than 17 dB, which is quite problematic especially regarding the achievable reference sensitivity.

A simplified schematic of the anti-alias filter is illustrated in Fig. 4.17. Every two integration periods ( $2T_s$ ), the capacitors are properly connected to the output and realize the anti-alias filtering function.

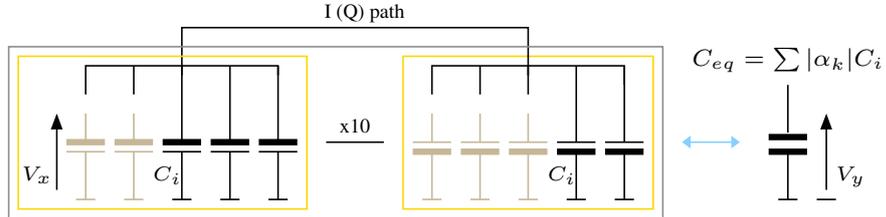


Figure 4.17: Equivalent schematic of the AAF stage

The various unit capacitors of the anti-alias filter can be viewed as one single capacitor  $C_{eq}$  holding the sum of the unit charges. The voltage  $V_y$  across this equivalent capacitor can be written as:

$$\begin{aligned}
C_{eq} \cdot V_y(z) &= \alpha_1 C_i \cdot V_x z^{-1} + \alpha_2 C_i \cdot V_x z^{-2} + \dots + \alpha_{2M_1} C_i \cdot V_x z^{-2M_1} \\
&= C_i \sum_{k=1}^{2M_1} \alpha_k z^{-k} \cdot V_x(z) \quad \text{where } z = e^{\frac{2\pi f}{2F_c}}
\end{aligned}$$

The gain of the anti-alias filter at the channel frequency  $F_c$  is thus given by:

$$G_2 = \left| \frac{V_y}{V_x} \left( z = e^{\frac{2\pi F_c}{2F_c}} = -1 \right) \right| = \left| \frac{\sum_k \alpha_k (-1)^k}{\sum_k |\alpha_k|} \right| = 1$$

Note that the gain is not affected here by the parasitic capacitances (bottom plate capacitance and switch drain capacitance) that may exist at individual

nodes  $V_x$ . This is because these parasitic capacitors are always in parallel with the unit capacitors  $C_i$  and thus only modify their value but never result in charge losses.

### Second DTASP stage

The connection between the first and second DTASP stages is shown in Fig. 4.18. Every sampling period  $T_s$ , the charge from the anti-alias filter is shared with a unit capacitor  $C_r$  from the second stage FIR filter. This passive charge sharing is inherently lossy, as only a fraction of the incoming charge is actually transferred to the second DTASP stage. The signal loss is proportional to  $C_{eq}/(C_{eq} + C_r)$  and can be minimized by lowering the value of the rotating capacitor  $C_r$  (which is however limited by thermal noise).

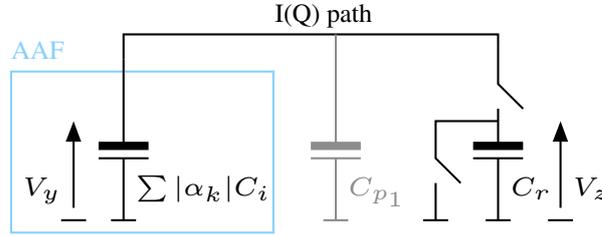


Figure 4.18: Input of the second DTASP stage

The gain is further degraded by the parasitic capacitance  $C_{p1}$  at the interface between the first and second DTASP stages. This capacitance realizes an IIR filter centered at DC and thus affects the gain much more in GSM mode than in 802.11g mode (where the signal is downconverted to DC). The signal loss can be derived as previously by writing down the charge transfer equation:

$$(C_{eq} + C_r + C_{p1}) \cdot V_z = C_{eq} \cdot V_y + C_r \cdot 0 + C_{p1} \cdot V_z z^{-1} \quad \text{where } z = e^{\frac{2\pi f}{F_s}}$$

which gives in GSM mode:

$$G_3 = \left| \frac{V_z}{V_y}(z = -1) \right| = \frac{C_{eq}}{C_{eq} + C_r + 2C_{p1}}$$

This attenuation is in the order of 2 to 3 dB, which rises the total signal loss throughout the receive path to approximately 20 dB in GSM mode.

The output of the second DTASP stage is illustrated in Fig. 4.19. The  $M_2$  rotating capacitors are connected together to the buffer capacitor  $C_b$ . This realizes the second FIR filtering, decimation and IIR filtering at the same time. The gain of the IIR filter at the new channel frequency  $F_s = F_c/M$  is derived from the following charge transfer equation:

$$(9C_r + C_b) \cdot V_b = C_r (V_z - V_z \cdot z^{-1} + \dots + V_z \cdot z^{-8}) - C_b \cdot V_b z^{-1}$$

$$V_b = \frac{C_r}{(9C_r + C_b) + C_b z^{-1}} \sum_{k=0}^8 (-1)^k z^{-k}$$

which gives, as expected, a unity gain at channel frequency:

$$G_4 = \left| \frac{V_b}{V_z}(z = -1) \right| = \frac{C_r}{9C_r + C_b - C_b} \cdot 9 = 1$$

The voltage on the rotating capacitors is finally sampled by the A/D converter input stage. This time, an active sample and hold operation is performed and hence no signal losses occur.

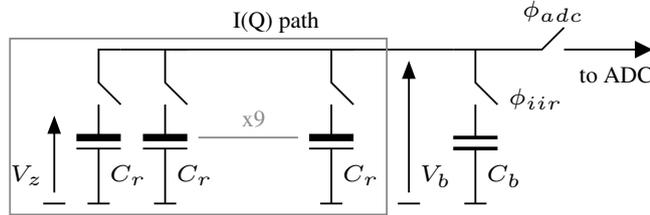


Figure 4.19: Output of the second DTASP stage

### Receiver noise figure

The noise contribution of the two DTASP stages is detailed in Appendix B. This noise contribution consists mainly of the thermal noise of the various switches which is integrated on the unit capacitors and then combined with every charge sharing operation. In an ideal case, the noise added by the ADC should be made by only to the quantisation noise. In reality, the noise added by the ADC can be much higher (due to the amplifiers noise for example).

The gain and noise contributions of the different stages in GSM mode are summarized in Table 4.6 for an RF input at sensitivity level.

		ANTENNA	SWITCH	SAW	LNTA	SINC2	FIR2/IIR2	ADC
Noise Figure	dB	0.0	1.0	2.8	2.5			
Noise Contribution	$V^2$					1.27E-11	8.89E-11	1.99E-10
Power Gain	dB	0.0	-1.0	-2.8				
Voltage Gain	dB				24.4	-2.28	0.0	0.0
Output Signal Level	dBm	-102.0	-103.0	-105.8				
	dBVrms				-81.4	-83.7	-83.7	-83.7
Output Noise Level	dBm	-121.0	-121.0	-121.0				
	dBVrms				-94.1	-96.1	-94.8	-92.7
SNR	dB	19.0	18.0	15.2	12.7	12.5	11.1	9.1

Table 4.6: Gain and noise contributions in GSM mode

For the proposed discrete-time receiver, the overall noise figure was easier to compute by summing the noise contributions of the different blocks, rather than by deriving individual noise figures and combining them using Friis's formula. This is because almost all blocks are passive and thus the noise at the output of these blocks is simply the sum of the input noise and the contributed noise, without handling any gain factor. A signal to noise ratio is also computed at the output of each stage, to give a clearer vision of how much the signal is affected throughout the receiver.

The signal and noise levels are expressed in units of dBm for the first three stages and then in units of dBVrms, which is totally independent from the stage impedances and hence simplifies the gain/noise analysis.

The evolution of signal and noise levels throughout the receiver is illustrated in Fig. 4.20. The receiver should meet the GSM sensitivity specification by a narrow margin. This performance can be improved in the future by increasing

the transconductance of the LNTA, which is the only way to compensate for all the signal losses throughout the passive stages.

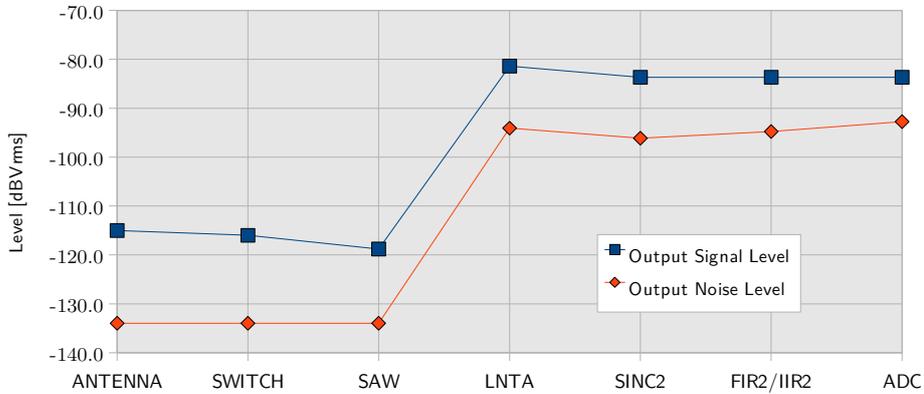


Figure 4.20: Signal and noise levels in GSM mode

#### 4.6.4 Filtering requirements

In the proposed receiver, the filtering requirements are dictated by the dynamic range available at the input of the ADC. All blockers and adjacent channels (at the power levels given in the standard specifications) must be sufficiently reduced not to saturate the input of the ADC. The LNTA output is also in concern and the first IIR filter must ensure that the in-band blockers, especially the 3MHz blocker, do not exceed the supported output dynamic range (which is circuit specific and equal to  $0.9V_{pp,diff}$  for the given LNTA).

The ADC input dynamic range is divided in GSM mode as shown in Fig 4.21. All blockers and adjacent channels must be reduced to fit in the ADC full-scale with a minimum margin of 6dB (taking into consideration fading margin and crest factor for a GMSK modulated signal).

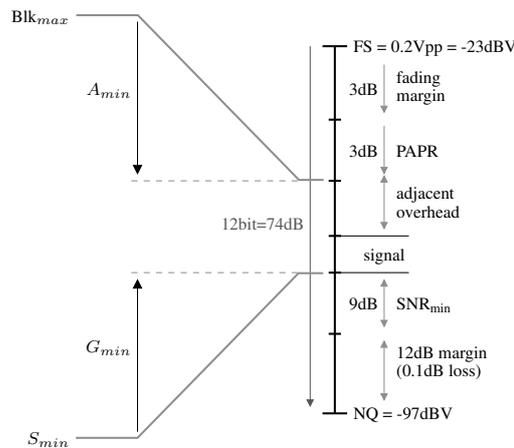


Figure 4.21: ADC input dynamic range partitioning in GSM mode

The power levels of the different blockers and adjacent channels throughout the receiver in GSM mode are given in Table 4.7 and are also plotted in Fig. 4.22.

	ANTENNA	SWITCH	SAW	LNTA	SINC2	IIR2	ADC	
Blocker Levels (dBV)	@600KHz	-56	-57	-59.8	-27.1	-29.4	-48.0	-48.0
	@1.6MHz	-46	-47	-49.8	-22.3	-24.6	-51.6	-51.6
	@3.0MHz	-36	-37	-39.8	-16.5	-18.8	-51.2	-51.2
	1 <sup>st</sup> OFB	-33	-34	-36.8	-17.9	-20.2	-65.2	-65.2
Adjacent Levels (dBV)	@200KHz	-86	-87	-89.8	-54.3	-56.6	-66.1	-66.1
	@400KHz	-54	-55	-57.8	-23.8	-26.0	-41.2	-41.2
	@1.6MHz	-46	-47	-49.8	-17.1	-19.4	-38.0	-38.0
Largest Blocker (dBV)	-33	-34	-36.8	-16.5	-18.8	-38.0	-38.0	

Table 4.7: Blocker & Adjacent levels in GSM mode

The rejection of the first IIR filter was adjusted to just the minimum required to keep the 3MHz blocker below the -10dBV<sub>rms</sub> requirement (as stronger rejections lead to larger history capacitors). The second IIR filter is then dimensioned accordingly and adds the amount of filtering required to fit into the ADC input dynamic range.

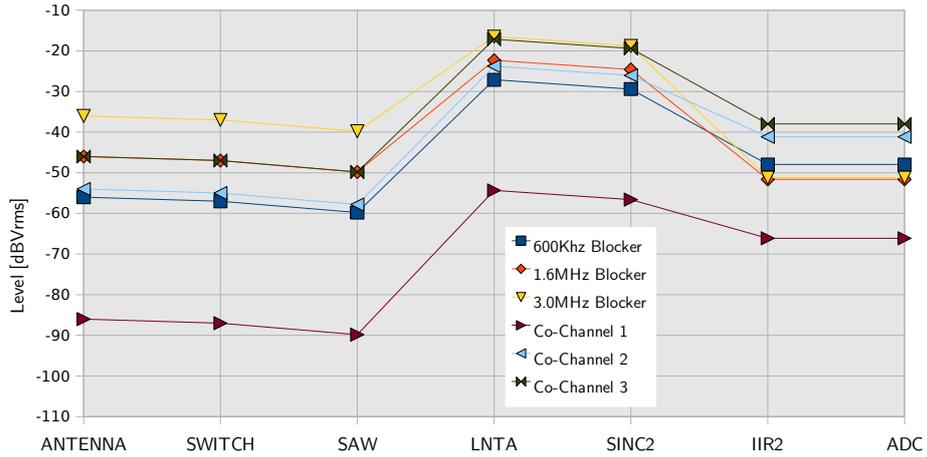


Figure 4.22: Blocker & Adjacent levels in GSM mode

The methodology described above also applies to the 802.11g mode. It was decided for the proposed receiver to keep the same value of unit capacitors for both modes (to avoid using extra switches and control signals and hence reduce the complexity of the circuit). When switching between GSM and 802.11g modes, only the value of history capacitors  $C_h$  and  $C_b$  are changed. The filtering requirements are more relaxed in 802.11g than in GSM mode and thus result in considerably smaller history capacitors.

## 4.7 Conclusion

This chapter presented the architecture of the proposed receiver front-end and the frequency plans used for each of the targeted communication standards (GSM900 and 802.11g). The structure of the anti-alias SINC<sup>2</sup> filter and the computation of the tap coefficients were also detailed.

The system level study focused mainly on the distribution of gain, noise and filtering along the receive path and resulted in specifications for circuit parameters such as the values of unit/history capacitors and on-resistance of unit switches.

Note that the system level study becomes more complex when the number of targeted standards is increased and that it may require different values for the unit capacitors used in the analog processing stages, which in turn would dramatically increase the complexity of the circuit design.



# Chapter 5

## Receiver front-end design

### 5.1 Introduction

In this chapter, we present the circuit design of the proposed receiver front-end. The block specifications described in the previous chapter are used here as guidelines for transistor and capacitor sizing of the entire front-end circuitry. The receiver front-end is implemented in 90nm CMOS technology (STMicroelectronics cmos090gp\_7M2T\_50A design kit).

The RF section, including the RF filter and the transconductance LNA will be discussed at first. Then, the discrete-time analog signal processing blocks will be presented in details (IIR1 filter, anti-alias filter, second downconversion stage). The anti-alias filter, which is certainly the most innovative part of the design, will be studied using a hierarchical bottom up methodology. The digital control unit that generates all the clock phases required by the front-end is also detailed. The  $\Sigma\Delta$  modulator used in GSM mode is briefly presented as well. Finally, some layout considerations are presented and the importance of this design step and its effects on the final performances of the entire receiver are pointed out.

### 5.2 RF section

#### 5.2.1 RF filter

The common role of an RF filter is to pass a desired signal band centered at a given RF frequency and attenuate surrounding out of band blockers. In RF sampling receivers, this filter also attenuates the aliasing components related to the first decimation stage. In this case, the attenuation brought by the RF filter will add to the one given by the dedicated anti-alias filter, hence improving the overall alias rejection of the Rx chain.

Two different RF SAW filters were used in the dual-mode receiver as a *backup* for the alias filtering (one filter per GSM/WIFI mode). It is intended to remove these filters in future versions, once the attenuation of the sole AAF stage becomes sufficient to meet the standards' specifications. Note, however, that the suppression of the RF filter will put severe constraints on the LNA as it will result in a wider input signal range.

### GSM mode

The RF SAW filter used in GSM mode is manufactured by EPCOS (ref. [B7705](#)). It is a low-loss and low amplitude ripple filter designed for the receive path of EGSM systems. It has a usable passband of 35 MHz and performs an unbalanced to balanced signal transformation. The main characteristics of the SAW filter (at 25 °C) are summarized in Table 5.1.

	min.	typ.	max.	
Center frequency	–	942.5	–	MHz
Bandwidth	925.0	–	960.0	MHz
Maximum insertion attenuation	–	2.7	3.2	dB
Amplitude ripple (p-p)	–	0.9	–	dB

Table 5.1: Characteristics of the GSM mode SAW filter

The transfer function of the GSM RF filter is shown in Fig. 5.1. The out-of-band attenuation exceeds 50 dB and is in accordance with the minimum rejection planned at system level. The nearest alias components (which fall at 540 MHz and 1260 MHz respectively) will be attenuated by at least 50 dB prior to the first decimation.

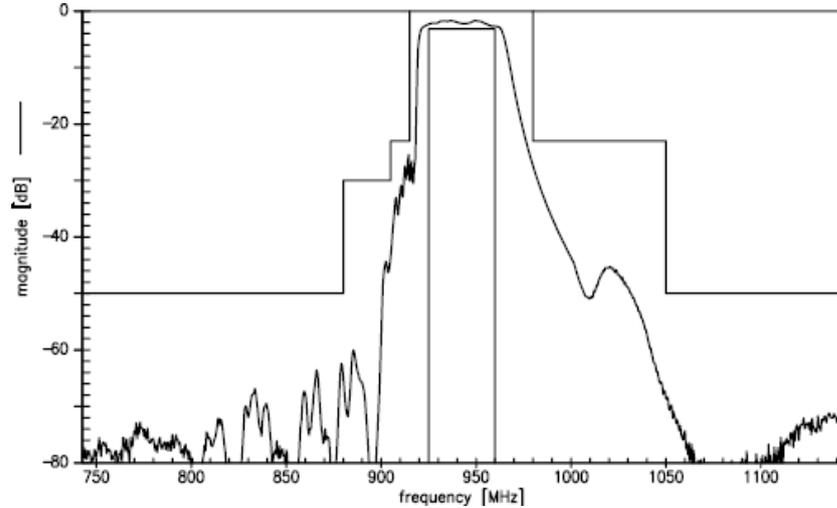


Figure 5.1: SAW filter transfer function in GSM mode

### WIFI mode

A possible RF filter for the WIFI mode could be the [B9413](#) model from EPCOS, which is a SAW filter designed for both wireless LAN and bluetooth standards and which the main characteristics are given in Table 5.2. For the scaled-down version of the 802.11g, we suppose the same insertion and out-of-band attenuations but shift the center frequency and divide the bandwidth of the RF filter by a factor of 2.4.

	min.	typ.	max.	
Center frequency	–	2441.75	–	MHz
Bandwidth	2400.0	–	2483.5	MHz
Maximum insertion attenuation	–	2.0	2.8	dB
Out-of-band attenuation	–	50	–	dB

Table 5.2: SAW filter characteristics in WIFI mode

### 5.2.2 Transconductance LNA

The transconductance LNA used in the receiver front-end is actually a re-use from a previous GSM Rx test chip that was designed at STMicroelectronics Crolles. The LNTA is presented in Fig. 5.2 and can be viewed as a combination of a transconductance stage and a cascode stage.

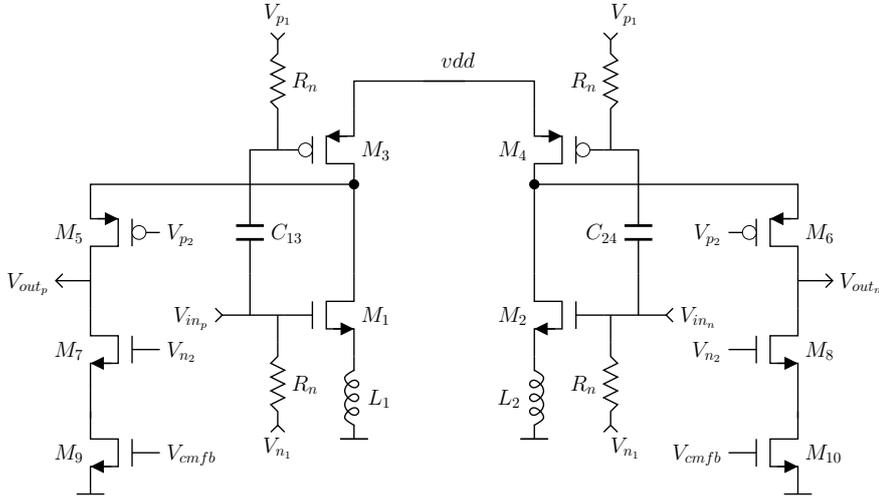


Figure 5.2: Schematic of the LNA transconductance stage

The transconductance of the LNA stage was initially based only on the NMOS transistor pair ( $M_1, M_2$ ) and the achieved  $G_m$  was far below the targeted value of  $80mS$ . The problem was solved by profiting from the transconductance of the PMOS transistors ( $M_3, M_4$ ) as well, which was realized by adding the  $C_{13}$  and  $C_{24}$  capacitors and thus connecting the input signal to the PMOS transistors. Note that the biasing of transistors  $M_{1-4}$  is DC coupled through resistive loads.

The ( $L_1, L_2$ ) degenerated inductors contribute to the impedance matching of the input. The remaining part of the impedance matching is performed off-chip using a dedicated LC network and will be discussed later.

The output of the dual N-P transconductance is then fed into a double cascode stage in order to increase the output impedance of the overall circuit. Increasing the width of transistors  $M_{5-8}$  also increases the output impedance of the LNTA but results at the same time in large parasitic capacitors at the output nodes (which in turn results in gain losses). Actually, the compromise that exists between these two parameters limits the achievable output impedance of



common mode voltage to a value  $V_{cm}$ . Component values of the ideal model were extracted from typical case AC simulations of the real LNTA.

### 5.3 First IIR filter

The first IIR filtering stage is mainly composed of the history capacitor and its driving switches, as depicted in Fig. 5.5. The IIR blocks used for the in-phase and quadrature paths are identical and differs only by the clock signals applied on them. The IIR stages are connected to the common nodes  $dec_P$  and  $dec_N$  at the LNTA output (after the decoupling capacitors).

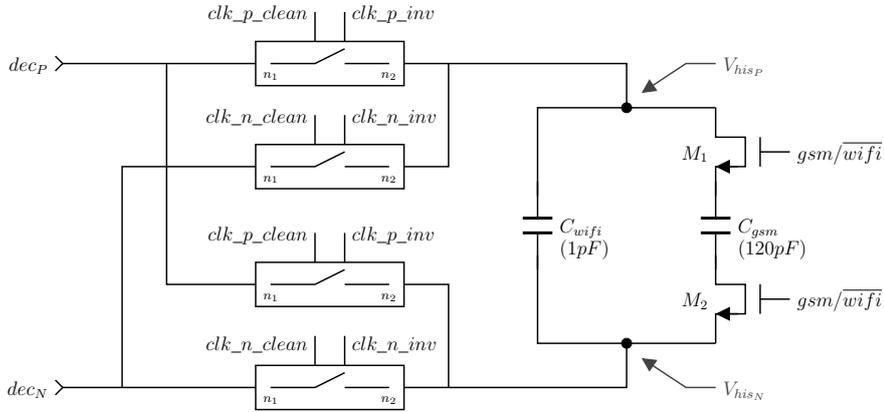


Figure 5.5: Schematic of the first IIR stage (I path)

During each integration phase, charge sharing occurs between the history capacitor, the LNTA and one rotating capacitor from the anti-alias filter. The configuration of the four switches makes the history capacitor *rotate* around the common nodes at twice the channel frequency  $2f_c$ .

#### 5.3.1 History capacitor switches

The four switches connecting the history capacitor to the common nodes are all identical. The schematic of a single switch is given in Fig. 5.6. It is composed of two NMOS transistors controlled by complementary clock signals. The  $M_2$  transistor acts as a dummy switch and reduces charge injection and clock feedthrough on the history capacitor [63]. This technique together with the differential sampling mechanism considerably decrease the errors introduced during sampling of the input signal.

The transistor  $M_1$  operates in triode region and hence its on-resistance  $R_{his}$  is given by :

$$R_{his} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH} - V_{DS})}$$

by noting  $V_{DD,clk}$  the high level of the applied clock signal and under the assumption that  $V_{DS} \approx 0$  (deep triode region), the on-resistance of  $M_1$  can be written as :

$$R_{his} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD,clk} - V_{in} - V_{TH})} \quad (5.1)$$

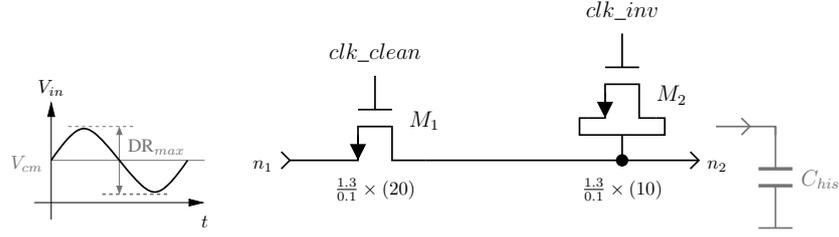


Figure 5.6: Schematic of the history capacitor switch

At this point, we shall introduce a circuit parameter that was not discussed in the previous chapter, which is the common mode voltage level  $V_{cm}$  at nodes  $dec_P$  and  $dec_N$ . This parameter was not of importance at system level, as all the specifications (gain, noise, capacitor values, ...) were computed using differential signals and that common mode levels at the various stages of the receiver were not concerned.

In order to lower the on-resistance of transistor  $M_1$ , (5.1) suggests that the input signal should be kept at a low level by a proper selection of the common mode voltage  $V_{cm}$ . Actually, the common mode is set a value slighter greater than half the dynamic range of the input signal. In GSM mode, the dynamic range at the LNTA output may extend to  $0.9V$  differential peak-to-peak, which converts to  $0.9/4 = 0.225V$  single-ended peak. The common mode level was thus fixed to a value of  $V_{cm} = 0.25V$ , allowing a voltage margin of  $25mV$ .

The width of transistor  $M_1$  is computed using the  $R_{his}$  value returned by the system level simulations in Chapter 4. By setting  $V_{in}$  equal to  $2V_{cm}$  (worst case), we then have :

$$W = \frac{L}{R_{his}\mu_n C_{ox}(V_{DD} - 2V_{cm} - V_{TH})} \quad (5.2)$$

The parasitic capacitances of the switches used in the IIR filter stage are shown in Fig. 5.7. Capacitors  $C_{2,3}$  are connected in parallel to the history capacitor and can be ignored as their value is orders of magnitude lower than  $C_{his}$ . However, capacitor  $C_1$  is important as it vastly contributes to the total parasitic capacitance  $C_{par}$  between nodes  $dec_P$  and  $dec_N$ , which in turn leads to severe gain losses.

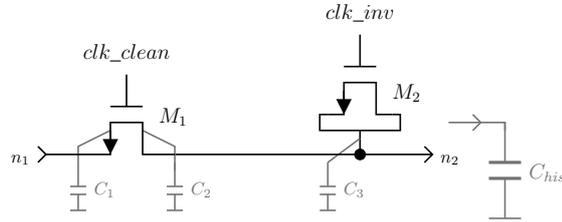


Figure 5.7: Parasitic capacitors of the IIR filter switches

As the transistor  $M_1$  operates in triode region, the parasitic capacitance  $C_1$  at its source terminal can be expressed as :

$$C_1 = WLC_{ox}/2 + WC_{ov} \quad (5.3)$$

where  $C_{ox}$  and  $C_{ov}$  are the gate oxide capacitance per unit area and the overlap capacitance per unit width respectively.

Although (5.3) can be used to approximate the value of the parasitic capacitance  $C_1$ , it is more desirable to extract this parameter from electrical simulations. Simulators such Spectre or Eldo are usually based on more elaborated models of the MOS capacitance, leading to more precise estimations of the capacitance  $C_1$ .

Actually, the values of the parasitic capacitances were extracted using the *captab* option in Spectre simulator. This option, available when performing DC simulations, allows the printing of all the node-to-node capacitances inside a given circuit. The value of  $C_1$  is thus obtained by simply printing the total capacitance at the source of transistor  $M_1$ . Note that the value of  $C_1$  is dependent of the input signal level and gets higher with small values of  $V_{in}$  (which at the same time leads to smaller values of  $R_{his}$ ).

### 5.3.2 Clock buffers

The complementary clock signals required by the history capacitor switches are derived from the main clock phases  $clk\_hist\_p$  and  $clk\_hist\_n$  using double inverter stages. This is depicted in Fig. 5.8.

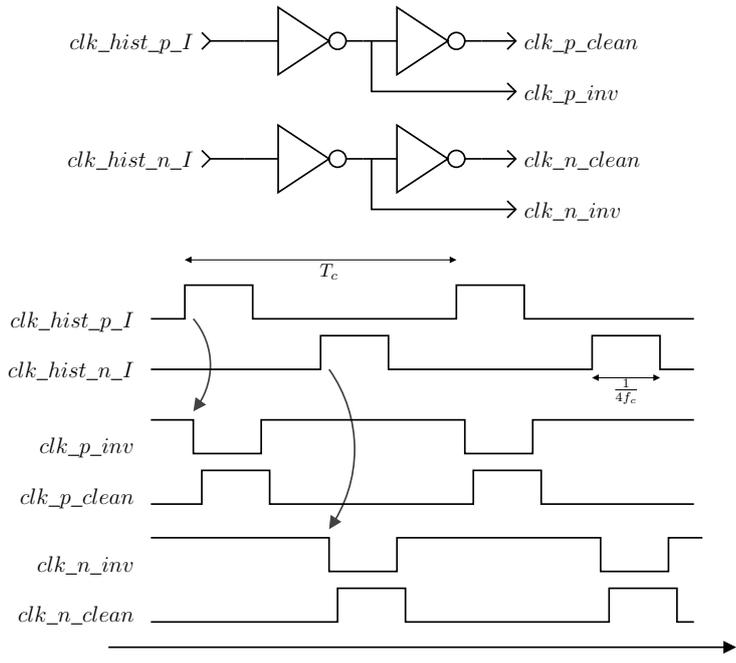


Figure 5.8: Buffering of the IIR clock phases

The role of these buffers is to amplify the clock phases coming from the DCU enough to drive the large switch transistors with a minimum RC time constant. Indeed, the capacitance seen at the gate of transistors  $M_1$  and  $M_2$  (Fig. 5.6) is so large that the DCU would not be able to properly drive the switches without a previous amplification.

Buffering of digital signals can be realized in different ways, depending on the number of inverters in use and on the scale factor between consecutive inverters. In this design, only two inverters with a scale factor of 2:1 were used to buffer the clock phases. Scaling of the inverters was based on the fan-out of the DCU's logic gates and the actual capacitance seen at the gates of  $M_1$  and  $M_2$ .

More important than the propagation delay through the clock buffers, is the synchronization with the clock phases of the rotating capacitors from the anti-alias filter. In fact, one must assure that the synchronization of the IIR and AAF clock phases still holds even after buffering, otherwise gain loss and image rejection problems may rise.

### 5.3.3 Reconfigurability

The value of the history capacitor is actually variable and depends on the receiver's mode. This is achieved by simply adding a pair of NMOS transistors  $M_{ctrl}$  acting as switches and controlled via the  $gsm/wifi$  control bit (Fig. 5.5). In WIFI mode, the transistors are turned off, the  $C_{gsm}$  capacitor is disconnected and the history capacitor equals only  $C_{wifi}$ . In GSM mode,  $M_{ctrl}$  transistors are turned on and the total capacitance seen at  $V_{his_P}$  and  $V_{his_N}$  nodes becomes equal to  $C_{gsm} + C_{wifi} \simeq C_{gsm}$ .

Note that the resistance  $R_{his}$  of the system model in GSM mode (see Chapter 4) has now increased by the on-resistance of transistors  $M_{ctrl}$ . This later was made very small by setting the transistors width to a high value. This prevents the total  $R_{his}$  resistance from increasing but results, at the same time, in larger parasitic capacitors (switches  $M_{ctrl}$ ). Hopefully, these parasitic capacitors remain connected to the history capacitor always in the same manner (no criss cross), which does not result in gain losses.

### 5.3.4 Output buffers

Recall from chapter 4 that the voltage across the history capacitor is a low frequency signal (as it represents the DC envelope of the RF input signal) and hence it can be easily buffered and outputted for testing purposes. Actually, this is the only possible way for measuring the gain of the LNTA stage.

A source follower ("common-drain" stage) connected on both sides of the history capacitor (nodes  $V_{his_P}$  and  $V_{his_N}$  on Fig. 5.5) is used to probe the signal and is presented in Fig. 5.9.

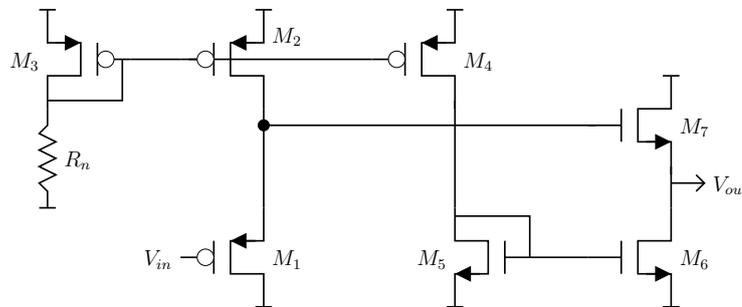


Figure 5.9: Output buffer

## 5.4 Anti-alias filter

This section presents the structure of the anti-alias filter at circuit level. As already described in section 4.5, the AAF is a repeating sequence of integer coefficients, each one corresponding to a certain capacitor ratio. Using a top-down approach, the 2<sup>nd</sup> order AAF can be viewed as a combination of three capacitor banks, each bank is composed of L coefficient cells and each coefficient cell is in turn composed of L unit cells.

The anti-alias filter was first designed for the GSM mode only. Then, new types of unit/coefficient cells were introduced and the interconnections at some hierarchical levels were rethought, in order to make the AAF reconfigurable and adapt the resulting filter response to the WIFI mode. To give a glimpse of the actual complexity, simply note that the implemented 2<sup>nd</sup> order AAF required over 300 switched capacitors and 36 clock phases.

Although this approach limits the reconfigurability of the AAF filter to only GSM and WIFI modes, it considerably reduces its complexity at circuit level. More generic topologies for implementing a wider range of filtering functions and achieving full reconfigurability can be thought of and will be discussed later in this chapter.

The structure of the anti-alias filter will be presented using a bottom-up approach starting from the unit cells. The filters for the I and Q paths are identical. They have different clock phases for the integration period but share the same output and reset clock phases.

### 5.4.1 Unit cell

The anti-alias filter can be viewed as a proper and complex arrangement of hundreds of unit cells. As shown in Fig. 5.10, a unit cell is mainly composed of a unit capacitor and three switches for the integration/reset/output phases.

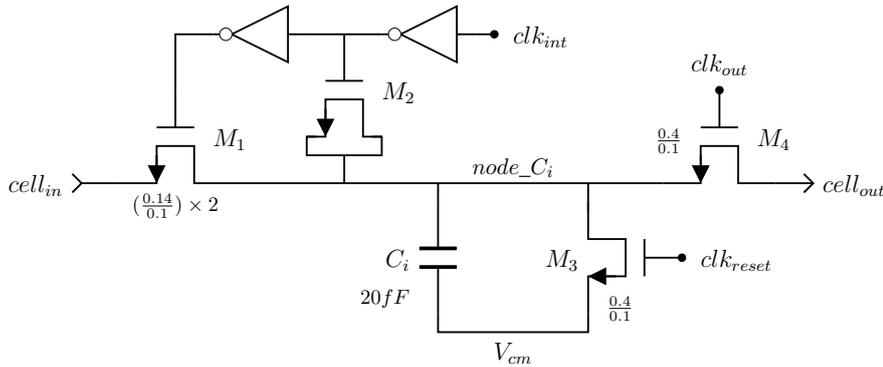


Figure 5.10: Schematic of the SINC<sup>2</sup> unit cell

The value of the unit capacitor was computed at system level and resulted from a gain/noise optimisation. The on-resistance  $R_{sig}$  extracted from the Scilab simulations sets the width of the sampling transistor  $M_1$ . A dummy switch ( $M_2$ ) was inserted to lower the charge injection and clock feedthrough to the unit capacitor  $C_i$ . Transistors  $M_3$  and  $M_4$  were sized according to the allotted time for reset and output phases respectively.

The bottom plate of  $C_i$  and the source terminal of  $M_3$  are both connected to  $V_{cm}$  instead of being grounded. During the reset phase, the residual charge on the unit capacitor is cleared and the top plate of  $C_i$  is precharged to  $V_{cm}$ . This bias voltage is then charge shared with the history capacitor to set the common mode voltage on  $V_{decP}$  and  $V_{decN}$  nodes to the desired  $V_{cm}$  value.

Some unit cells may need to sample the input current only in GSM mode and must be deactivated when switching to WIFI. This is accomplished using the reconfigurable unit cell of Fig. 5.11.

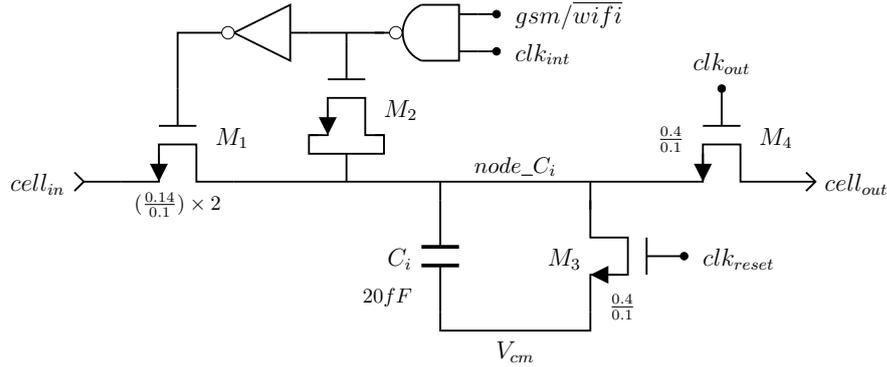


Figure 5.11: Schematic of the SINC<sup>2</sup> reconfigurable unit cell

The sampling switch is now controlled via a logic NAND gate and is permanently deactivated by setting the  $gsm/wifi$  bit to zero. Note that the reset and output switches are not concerned at this point.

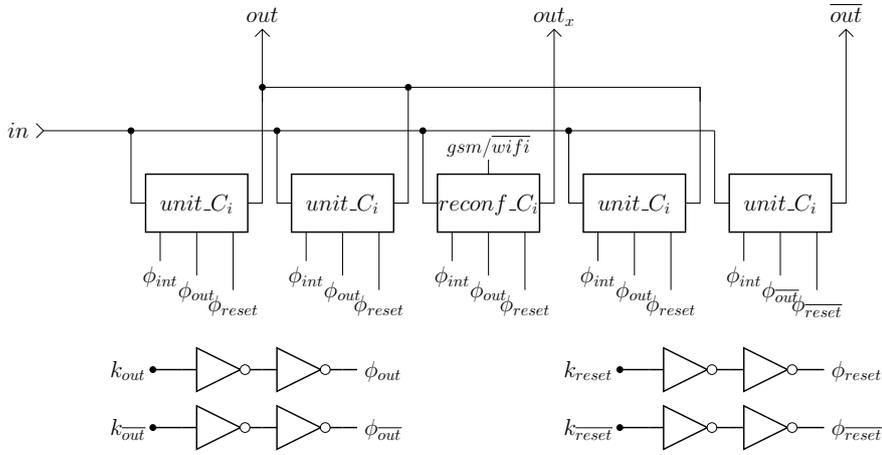
#### 5.4.2 Coefficient cell

Every coefficient of the SINC<sup>2</sup> filter is made of  $L$  unit capacitors. These capacitors integrate the input current all together during the sampling period. Then, by reading the charge accumulated on  $k$  from  $L$  capacitors, we obtain a coefficient  $\alpha_k = k/L$ .

The schematic of a coefficient cell is presented in Fig. 5.12 and is composed of four unit cells and one reconfigurable cell, resulting in  $L = 5$  for GSM mode and  $L = 4$  for WIFI mode. Note that a gain loss of  $20 \log(5/4) \simeq 2dB$  would have arisen if all of the five unit capacitors were used in WIFI mode. This explains why disconnecting all the unused capacitors is mandatory.

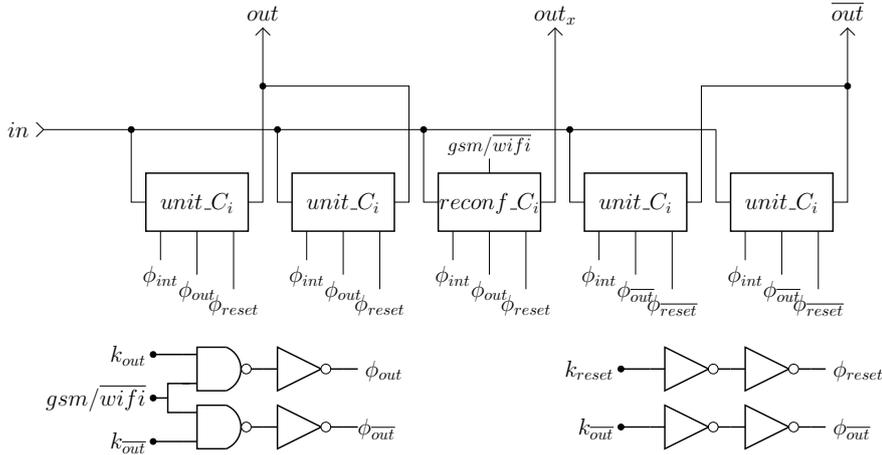
All the unit cells share the same input and are controlled by the same clock sampling phase  $\phi_{int}$ . The  $L$ -complementarity presented at system level is implemented at this stage. The  $L$  unit cells are divided in two groups, resulting in charge fractions of  $k/L$  and  $(L - k)/L$ . The first group is controlled using  $k_{out}$  and  $k_{reset}$  clock phases, the second one using  $\overline{k_{out}}$  and  $\overline{k_{reset}}$  respectively. The composition of the two groups depends on the desired coefficient to be implemented. Fig. 5.12 gives the example of coefficient  $1/5$  (or  $4/5$ ) in GSM mode, which becomes also  $1/4$  (or  $3/4$ ) in WIFI mode.

The coefficient cell has two outputs for the  $L$ -complementary groups ( $out$  and  $\overline{out}$ ) and a third output dedicated to the reconfigurable cell ( $out_x$ ). These outputs will be routed at an upper level to the final AAF filter outputs  $sinc^2_{outP}$  and  $sinc^2_{outN}$  depending on the required coefficients signs.

Figure 5.12: Example of a  $\text{SINC}^2$  coefficient cell (coef\_14)

The special output  $out_x$  is required to disconnect the capacitor of the reconfigurable cell from the output of the AAF in WIFI mode, in order to avoid gain losses. Indeed, during charge sharing between the AAF coefficient cells and a rotating capacitor from the 2<sup>nd</sup> DTASP block (output phase), a second gain loss of  $20 \log(19/16) = 1.5\text{dB}$  would happen if the GSM unused capacitors are left connected.

When switching from GSM to WIFI, the decimation ratio changes from  $M=5$  to  $M=4$  and the FIR filter length is reduced by 3 coefficients (one per integration path). A reconfigurable coefficient cell that would be active only in GSM mode was created for this purpose and is presented in Fig. 5.13.

Figure 5.13: Reconfigurable  $\text{SINC}^2$  coefficient cell

The sampling clock phase  $\phi_{int}$  for this coefficient is disabled from the DCU when operating in WIFI mode. The output phases  $k_{out}$  and  $k_{out_bar}$  are combined with the control bit  $gsm/wifi_bar$  using NAND gates which completely disconnects the coefficient cell from the output of the  $\text{SINC}^2$  filter.

Many alternatives exist for the reconfigurability of the anti-alias filter, but the proposed solution is by far the simplest one, requiring the least possible modifications of the filter circuitry and clock phases generation block.

### 5.4.3 Capacitor bank

The arrangement of coefficient cells into one capacitor bank is illustrated in Fig. 5.14.

Five coefficient cells are needed for the positive path and five others for the negative path. The capacitor bank requires five clock sampling phases and two sets of output/reset phases. The coefficient cells are properly arranged and result in sequences [1 2 3 4 5] (or [4 3 2 1 0]) in GSM mode and [1 2 3 4] (or [3 2 1 0]) in WIFI mode.

The sign of the coefficients is implemented at this stage. A positive coefficient is obtained if the input and output of the corresponding coefficient cell are both connected to the positive (or negative) path. A negative coefficient is obtained when the input and output of the coefficient cell are not both connected to the same positive/negative path.

Switching from GSM to WIFI is problematic here. Indeed, half of the FIR filter coefficients change from positive to negative sign or vice versa. The least complex solution consists in connecting the outputs from the different coefficient cells to intermediate nodes ( $P_P$ ,  $P_N$ ,  $N_x$ , ...). These nodes would be next routed to the final SINC<sup>2</sup> filter outputs through static switches (driven by the *gsm/wifi* control bit). The names of the intermediate nodes are significant. For example,  $P_N$  means that this node will be routed to the positive AAF output *sinc<sup>2</sup>\_out<sub>P</sub>* in GSM mode and to the negative one in WIFI mode. Also,  $N_x$  means that the node will be connected to the *sinc<sup>2</sup>\_out<sub>N</sub>* output in GSM mode but will be left unconnected in WIFI mode.

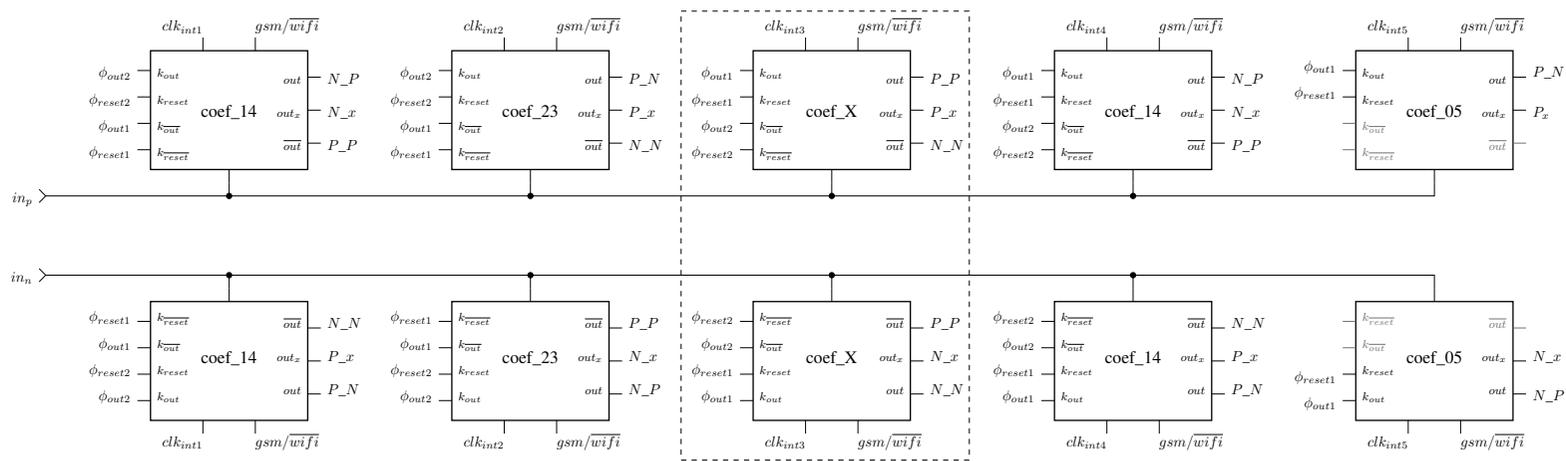


Figure 5.14: Arrangement of SINC<sup>2</sup> coefficients into bank

### 5.4.4 Top view

The top view of the anti-alias filter for one I/Q quadrature path is shown in Fig. 5.15. It is composed of three capacitor banks (corresponding to the three integration paths) and static switches for the reconfiguration of the coefficient signs.

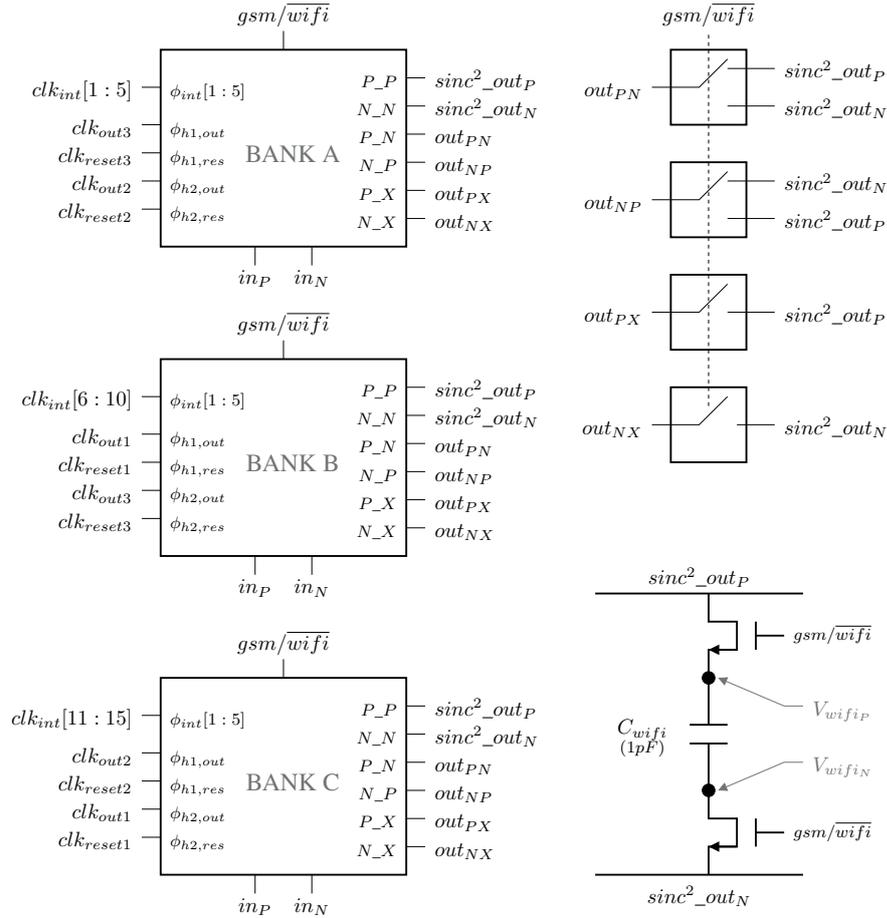


Figure 5.15: Top view of the anti-alias filter

In WIFI mode, the RF signal is downconverted to DC due to the decimation by an even ratio ( $M=4$ ). It is hence possible to buffer the differential signals from the AAF and output them off-chip for testing purposes. A second IIR filter is realized by connecting a capacitor  $C_{wifi}$  with a value of  $1pF$  differentially at the output of the AAF stage, only in WIFI mode.

## 5.5 Second DTASP block

The second DTASP block performs both FIR and IIR filtering operations and is activated only in GSM mode. It is constructed using unit cells that are arranged

into rotating banks and is less complex than the AAF stage owing to the fact that the required FIR coefficients are in the more simpler form of  $[+1 -1 +1 -1]$ .

### 5.5.1 Unit cell

The unit cell at the base of the 2<sup>nd</sup> FIR filter stage is presented in Fig. 5.16. It is composed of one unit capacitor  $C_r$  and four switches corresponding to the four phases  $\phi_{in}$   $\phi_{iir}$   $\phi_{adc}$  and  $\phi_{reset}$  of normal operation.

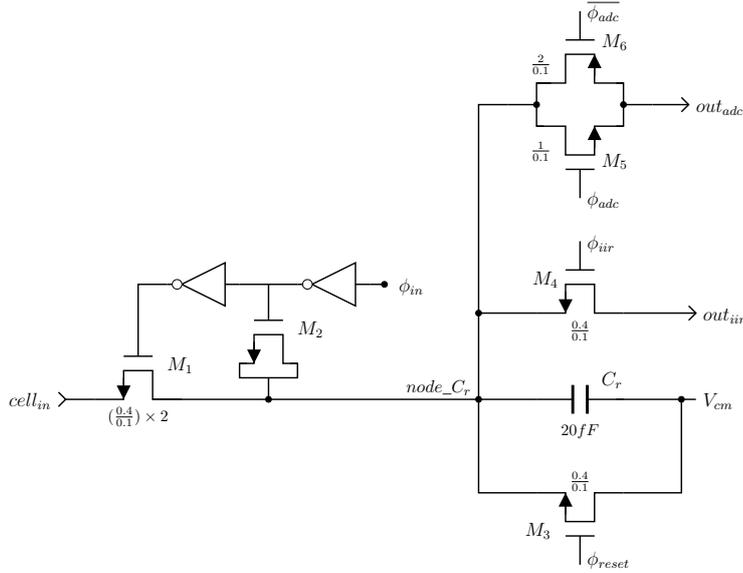


Figure 5.16: Schematic of the FIR2 unit cell

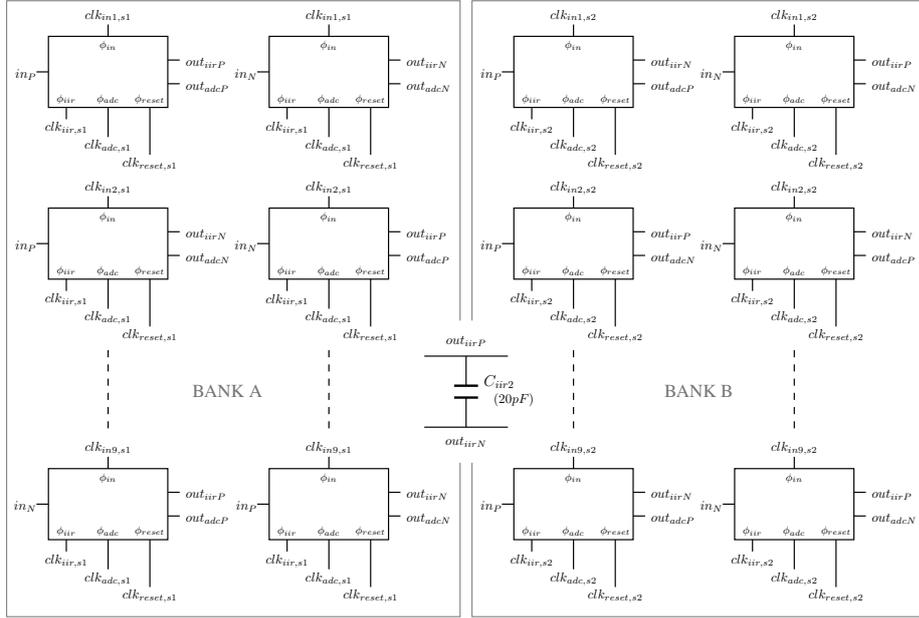
The value of the  $C_r$  capacitor was already fixed at system level. For each switch transistor, the on-resistance was computed according to the RC time constant, the phase duration and the required sampling accuracy. Taking the example of the reset phase, the on-resistance of transistor  $M_3$  can be extracted from :

$$R_{ON} \leq \frac{T_{reset}}{C_r \cdot \ln(1 - A)} \quad (5.4)$$

where  $T_{reset}$  is the duration of the reset phase and  $A$  is the required accuracy and is usually set to a value of 99.9% ( $7\tau$ ). The required accuracy can also be linked to ADC resolution. Indeed, incomplete charge sharing operations due to large RC time constants results in errors on the sampled signal, but are not of importance as long as they do not exceed  $1/2LSB$  of the ADC input dynamic range.

### 5.5.2 Top view

The arrangement of the unit cells into a working FIR/IIR filter is shown in Fig. 5.17. The 2<sup>nd</sup> DTASP block required a total of  $2 \times 2 \times 9 = 36$  units cells and  $2 \times (9 + 3) = 24$  clock phases.

Figure 5.17: Top view of the 2<sup>nd</sup> DTASP block

By contrast with the 1<sup>st</sup> IIR stage where the history capacitor was rotated at twice the channel frequency, the buffer capacitor  $C_{buf}$  realizing the 2<sup>nd</sup> IIR filter is here kept static. Actually, it is the unit cells that are rotated (required to center the IIR pole at  $Fs/2$ ) by inverting their connections to the buffer capacitor every other time.

## 5.6 Digital Control Unit

The role of the DCU is to generate the 69 clock phases required by the analog filtering stages. It is an entirely digital block with boosted logic gates designed to operate at frequencies above 5 GHz. The DCU takes as input a square clock signal at four times the channel frequency ( $4F_c$ ), a reset signal and the control bit  $gsm/\overline{wifi}$ .

The DCU is probably the most important block of the receiver front-end and can be thought of as an orchestra conductor. A well designed DTASP will never achieve good performances if the DCU is not perfectly elaborated as well. Indeed, improper generation of the clock phases may result in gain and image rejection losses and even a complete dysfunction of the entire front-end.

The design of the DCU must be carefully checked. After verifying its functionality through transient simulations, the DCU must be checked against worst cases (parasitics, process, temperature, power supply). This is mandatory because there is no access to the clock phases from the outside world and once the circuit is processed, it is almost impossible to check the DCU's operation.

The DCU was designed as a clocked sequential system, meaning that all the clock phases were made synchronous to the master clock. In this way, we ensure that the different filtering stages are synchronous with each other and

that adjacent clock phases are toggled simultaneously at  $V_{DD}/2$ . The major drawback of this technique is that it generates huge current peaks on the power supply, requiring a large amount of decoupling capacitors to limit the drop on the voltage supply.

### 5.6.1 D flip-flop cell

D flip-flops are intensively used inside the DCU to keep the clock phases synchronized. To achieve operating frequencies above 5 GHz, the D flip-flop must be as simple as possible. A classic nine transistors scheme [49] was used here, as shown in Fig. 5.18.

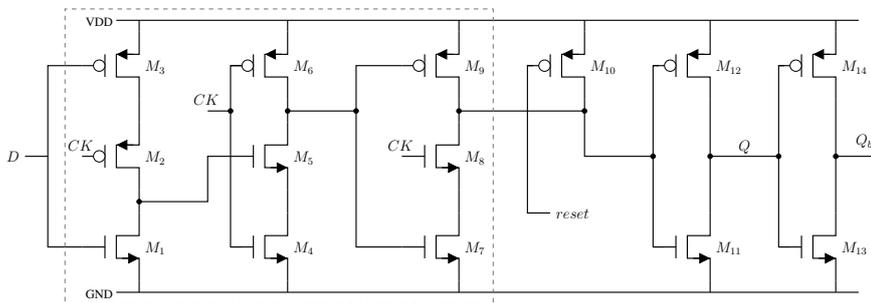


Figure 5.18: Schematic of the D flip-flop

Each flip-flop is supposed to drive a large capacitive load (logic gates, flip-flops, output buffers). Two inverter stages were thus added to sufficiently buffer the complementary  $Q/Q_b$  outputs, at the cost of a larger propagation delay.

The input data is sampled at the falling edge and the output is toggled at the rising edge of the clock. An asynchronous active-low reset was implemented by inserting a PMOS transistor at the output of the 9 transistors stage.

### 5.6.2 Clock phases generation

The DCU is composed of four different blocks for the generation of the IIR1, AAF, DTASP2 and ADC clock phases respectively. These blocks make use of D flip-flop token rings every time a repeating sequence of successive sampling phases is required. Fig. 5.19 illustrates the generation of the sequence  $[I_P Q_P I_N Q_N]$  that feeds the first IIR filter stage.

In this example, four D flip-flops are placed in series and the token is shifted from left to right on every rising edge. A mechanism based on NMOS transistors and a PMOS pull-up resistor is used to guarantee a single token inside the loop all the time.

When the input of the first flip-flop is pulled-up, a new token is injected inside the loop. This happens only when no other tokens are detected at the output of the first  $M-1$  flip-flops, assuring thus the uniqueness of the token.

Thanks to this checking mechanism, the token ring is guaranteed to start working correctly at power-up and does never require resetting. Actually, it does not suffer from any meta-stability problem and is robust against many circuit perturbations. However, a problem rises when the ring becomes relatively long.

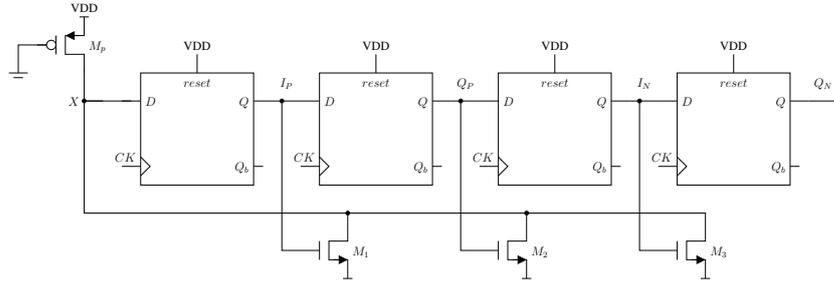


Figure 5.19: Generation of the history capacitors clock phases

The generation of the sampling phases of the SINC<sup>2</sup> filter required a ring of thirty D flip-flops and also a total of thirty transistors, resulting in a large capacitance at node  $X$ . Usually, the on-resistance of the NMOS transistors must be kept lower than  $R_P$  (usually one tenth) to maintain a detectable logic '0'. Unfortunately, increasing the width of the NMOS transistors also increases the total capacitance at node  $X$  resulting in a large RC time constant. When operating at high frequencies, problems for re-inserting the token into the ring may appear (due to the large time constant), resulting in phase jumps or irregular successive sampling phases. Transient simulations confirmed the limitation of this structure to frequencies around 4.5 GHz.

The problem was solved by using the token ring presented in Fig. 5.20. In this configuration, the D flip-flop loop is closed by connecting the output of the last flip-flop to the input of the first one and no pull-up or pull-down transistors are used.

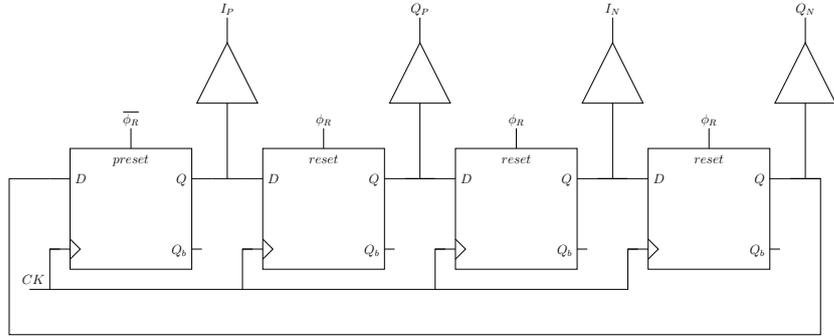


Figure 5.20: Improved version of the token ring

Note that the first flip-flop of the token ring is actually presettable, by contrast with the remaining flip-flops. In this structure, an initial reset phase is required. During this phase, all the outputs are set to '0', except for the first flip-flop which is set to '1'. After disabling the reset signal, the token starts shifting inside the loop at every clock sample.

The new structure is now limited only by the speed (propagation delay) of the D flip-flops and can operate at frequencies far above 5 GHz, regardless of its actual length. However, any circuit perturbation may insert one or more other tokens inside the loop, which results in simultaneous sampling clock phases.

This is the major drawback of the structure and can be addressed only by resetting the DCU every time the circuit seems to behave oddly.

In addition to the token rings, the DCU also incorporates many combinatory logic blocks. These blocks are in charge of the output/reset phases for the AAF and all the clock phases for the DTASP2 and  $\Sigma\Delta$  ADC. The design concept of these blocks is illustrated in Fig. 5.21.

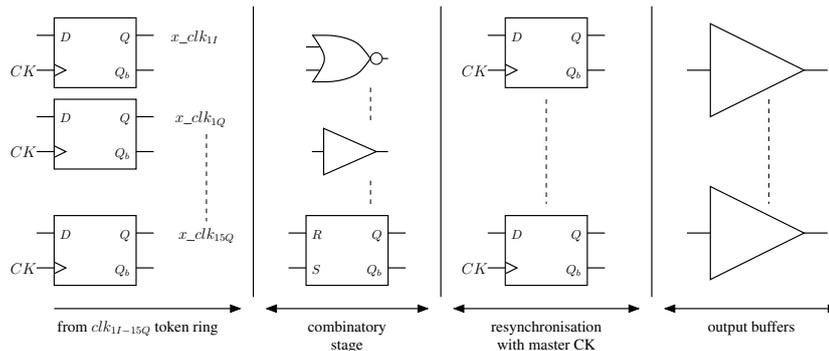


Figure 5.21: Design concept for clock phases generation

Intermediate clock phases from the SINC<sup>2</sup> token ring are first fed to a huge combinatory stage (composed mainly of NOR gates, inverters, buffers and RS flip-flops). The outputs of this combinatory stage are then resynchronized with the master clock using D flip-flops and are finally buffered.

The total propagation delay through the whole combinatory stage should be kept as low as possible. This is actually the limiting factor of the entire DCU. With high operating frequencies, the propagation delay may exceed the period of the clock signal, compromising the functioning of the DCU.

### 5.6.3 DCU reconfigurability

The digital control unit must be able to adapt the generation of the clock phases to the actual communication mode. When switching from GSM to WIFI, the clock phases for the 2<sup>nd</sup> DTASP must be completely deactivated. Concerning the SINC<sup>2</sup> filter, some sampling phases must be kept to zero in order to not activate their corresponding coefficient cells.

The global reset signal for the DCU section in charge of the DTASP2 clock phases was logically combined with the *gsm/wifi* control bit, thus setting all the phases to zero during WIFI mode.

The token ring in charge of the AAF sampling clock phases was modified, by inserting pass gates at specific points between the series flip-flops. This is illustrated in Fig. 5.22 for the sequence  $[clk_{2I} \ clk_{2Q} \ clk_{3I} \ clk_{3Q} \ clk_{4I}]$ .

In GSM mode, the pass gates are transparent and a complete sequence of sampling phases is generated. In WIFI mode, the pass gates change the trajectory of the token and bypass the flip-flops corresponding to the non required sampling phases. A logic '0' is fed into these flip-flops to maintain their outputs to zero. The sequence of Fig. 5.22 becomes in WIFI mode equal to  $[clk_{2I} \ clk_{2Q} \ clk_{4I} \ clk_{4Q}]$  and the sampling phases for the coefficient cells 3I and 3Q are deactivated.



use) with a minimum RC time constant. Using DC simulations with the *captab* option enabled, the value of this load capacitance was estimated to  $3.8pF$  !

The LO buffer has a first output for the IIR1+AAF sections of the DCU and a second one for the DTASP2 section. Routing of these two outputs must be as symmetrical as possible to limit the clock skew that may appear between the different sections of the DCU.

Oversizing of the LO buffer transistors (to lower the global RC time constant) resulted in an excessive power consumption, almost equal to the power consumption of the entire DCU. This point is problematic and should be addressed in the future. By reconsidering the structure of the DCU, the number of D flip-flops may be reduced, which in turn will reduce the size of the LO buffer and its power consumption.

### 5.6.5 Simulated performances

The timing diagram of the entire clock phases is shown in Fig. 5.24 for the GSM mode. This diagram can be used to contrast the design of discrete-time receivers with more conventional architectures (that require far fewer clock signals).

The DCU was first simulated in typical case to check whether the clock phases were generated in the desired way. Then, the maximum operating range of the DCU was determined by varying parameters such as input clock frequency, voltage supply, temperature and process corners. These simulations were performed on a post-layout extracted view of the whole DCU / LO buffer, to also account for the parasitic capacitors.

The maximum operating range of the DCU was extracted from transient simulations realized under the worst case conditions listed in Table 5.3.

Conditions	
PLS Extraction	Cc / RCMAX
Temperature	105° C
Process corner	SSA (Slow Slow Analog)

Table 5.3: Test conditions for evaluating the DCU performances

The maximum input frequency  $f_{LO}$  and the minimum voltage supply under which the DCU still operates correctly are listed in Table 5.4. The limitation over the frequency range is due to the propagation delays through the combinatory stage.

	min.	typ.	max.	
LO input frequency $f_{LO}$		4	6.5	GHz
Voltage supply $V_{DD}$	1.0	1.2		V

Table 5.4: Maximum operating range of the DCU

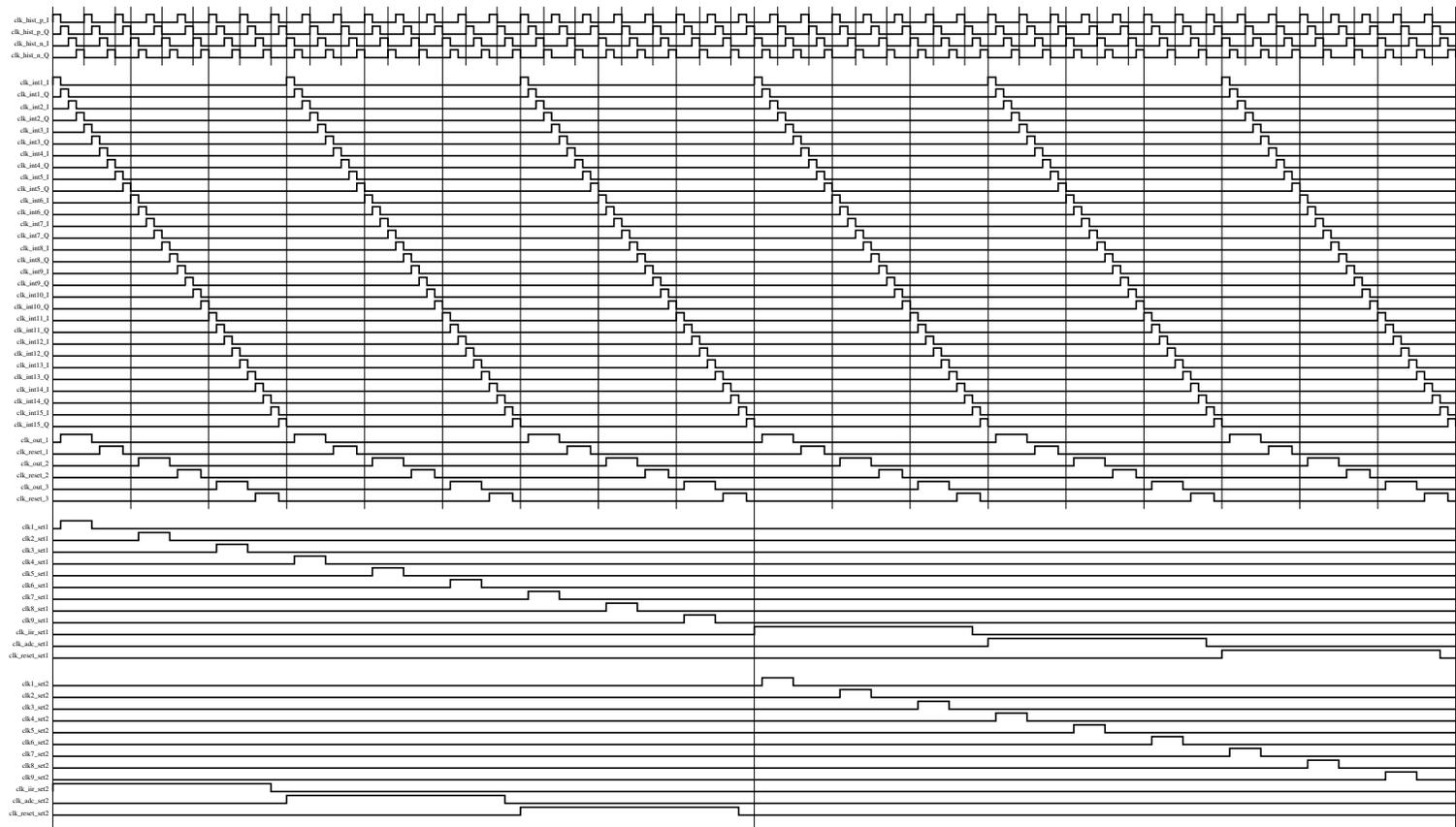


Figure 5.24: Timing diagram of the entire clock phases in GSM mode

The real 802.11g mode requires a master clock frequency of  $4 \times 2.4 = 9.6$  GHz and hence cannot be implemented using the current DCU structure. Unless switching to a more advanced CMOS technology, a possible alternative may consist in using a differential master clock at  $2 \times 2.4 = 4.8$  GHz and modifying the DCU accordingly. This solution, however, would result in overlapping I/Q clock phases and would require the use of two  $G_m$  transconductors to isolate the I/Q paths.

## 5.7 A/D converter

This section briefly presents the  $\Sigma\Delta$  modulator used in GSM mode to digitize the  $F_s/2$  signal at the end of the receiver chain. As for the LNA stage, the modulator is actually a re-use from a previous GSM Rx test chip that was designed at STMicroelectronics Crolles.

The modulator is based on a high-pass switched capacitor (SC) 2<sup>nd</sup> order architecture with a 3-level internal quantizer and was designed to achieve a 12-bit resolution with a full scale of  $0.2 V_{pp}$  differential.

The architecture of the  $\Sigma\Delta$  modulator is given in Fig. 5.25. The discrete-time coefficients of the modulator are the same as in a theoretical low-pass 2<sup>nd</sup> order architecture, except that the second DAC coefficient is inverted.

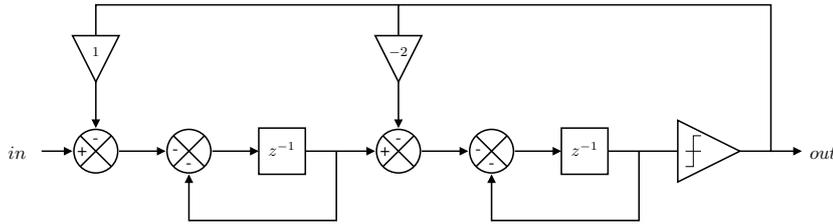


Figure 5.25: Architecture of the  $\Sigma\Delta$  modulator

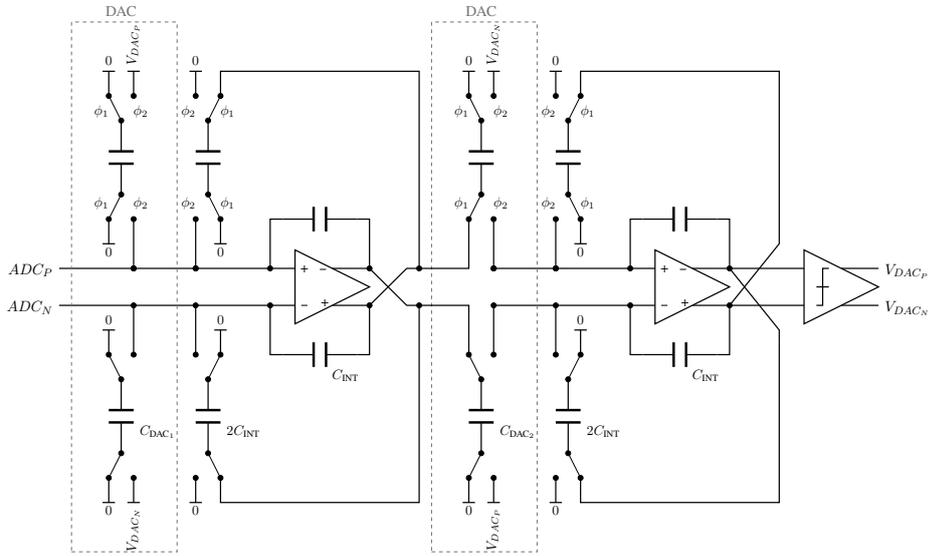
The schematic of the  $\Sigma\Delta$  modulator is shown in Fig. 5.26. The charges stored on the capacitor banks of the 2<sup>nd</sup> DTASP block are directly integrated by the first resonator.

During the sampling phase  $\phi_1$ , the output voltage of each resonator is stocked on a  $2C_{int}$  size capacitor. During the following integration phase  $\phi_2$  (which coincides with the  $clk_{adc}$  phase of the DTASP2), the charge accumulated on a  $2C_{int}$  capacitor is transferred into the opposite integration capacitor. This results in the following resonator transfer function:

$$V_{out} = \frac{9C_r}{C_{int}} \frac{z^{-1}}{1 + z^{-1}} V_{in} \quad (5.5)$$

where  $9C_r$  corresponds to the total capacitance seen from the DTASP2 output. Note that it was necessary to rescale all the  $C_{int}$  capacitors when re-using the  $\Sigma\Delta$  modulator in order to keep the same loop gain.

Two-stage A/AB-class operational amplifiers were used here for the integrators [10], allowing a high slew-rate that is not limited by static current. A Miller RC pole-compensation was used, as well as two common-mode feedbacks based on resistive dividers.

Figure 5.26: Schematic of the  $\Sigma\Delta$  ADC

The quantizer is composed by an A-class preamplifier stage (that calculates and amplifies the difference between the differential input signal and the comparison levels), followed by an inverter-based comparator. The saturated output signal is rectified by inverters and stored in a D-latch.

## 5.8 Layout considerations

A great attention should be paid to the layout of the receiver front-end as it deeply influences performances such as gain, linearity and filtering. The choice of the capacitor structure may also be crucial in such discrete-time receivers.

### 5.8.1 Capacitor layout

The mismatch between unit capacitors limits the depth of the AAF notches and is hence the most important criteria for the choice of the capacitor structure. Technology characterization proved that MOM (Metal Oxide Metal) capacitors is the structure presenting the lowest mismatch when relatively small capacitors are used (here, 20 fF). Selecting MOM structures for the layout of the unit capacitors was also motivated by the good linearity they usually achieve.

All unit capacitors were designed using five inter-digitized metal levels (from M1 to M5), as demonstrated in Fig. 5.27. The area of the unit capacitor was kept relatively small and a square form factor was selected to increase the global density of the coefficient cells and hence minimize the total area of the anti-alias filter.

The QuickCap tool was used to accurately extract the value of the unit capacitor from the layout view. Successive readjustments of the capacitor dimensions were then performed until the desired value was finally reached.

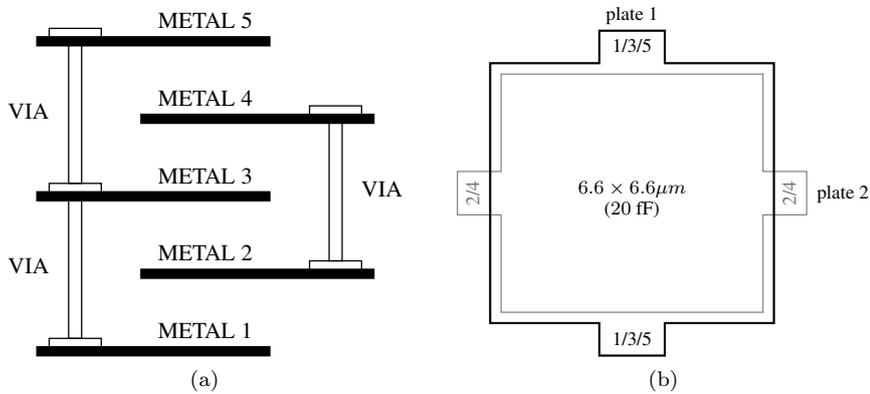


Figure 5.27: Unit capacitor layout: (a) Cross section (b) Top view

Concerning the history capacitor, a layout structure with good linearity and extremely high density was required. A novel structure combining both MOM inter-digitized and fringed capacitor techniques was used to achieve high density and hence minimize the total area of the history capacitor. This is depicted in Fig. 5.28.

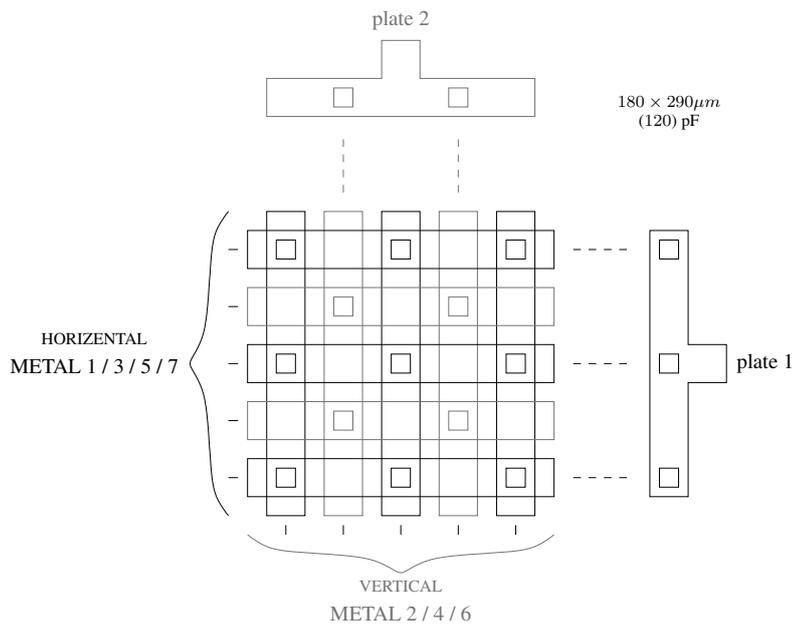


Figure 5.28: History capacitor layout

All the available metal levels (from M1 to M7) are used in this structure. The total  $C_{his}$  capacitance is formed by the fringe capacitances created at each metal level and also by the MOM capacitances resulting from the inter-digitized metal levels. A density of  $2.22 \text{ fF}/\mu\text{m}^2$  was achieved through this structure and a total area of  $0.1 \text{ mm}^2$  was required for the two I/Q history capacitor.

### 5.8.2 Gradient cancellation techniques

The layout of the anti-alias filter was extremely well studied and great efforts have been made in order to limit the effects of process variations on the final AAF performances.

Recall from system level study that the depth of the AAF notches is related to the accuracy on the filter coefficients and to the fact that they should remain equal to integer values. At circuit level, integer ratios  $k/M$  can be realized within coefficient cells, if all of the  $M$  unit cells are completely identical.

When no mismatch exists between the  $M$  capacitors of a coefficient cell and when the unit cells are placed and routed in exactly the same way, the input current would divide equally between these  $M$  paths, which would result later in an integer ratio.

During each output phase,  $2M$  coefficient cells are connected together and share their corresponding charges to form an output sample. At this point, any capacitor mismatch between the coefficient cells would not matter. This is because the integer ratios were already created during the integration phase (by current splitting) and are not created during the output phase, by contrast with a voltage sampling scheme. This is clear from the expression of the voltage at the output of the anti-alias filter :

$$\begin{aligned}
 V_{out}(z) &= \frac{\sum Q_k}{\sum C_k} \\
 &= \frac{1}{\sum C_k} (Q_1(z^{-1}) + Q_2(z^{-2}) + \dots + Q_{2M}(z^{-2M})) \\
 &= \frac{1}{\sum C_i + C_r} \left( \frac{1}{5} Q_{in}(z^{-1}) - \frac{2}{5} Q_{in}(z^{-2}) + \frac{3}{5} Q_{in}(z^{-3}) + \dots + 0 \right) \\
 &= \frac{Q_{in}(z)}{\sum C_i + C_r} \cdot H_{\text{SINC}^2}(z) \tag{5.6}
 \end{aligned}$$

where the values of the unit capacitors  $C_i$  modify only the global gain, without affecting the filter's coefficients and hence the depth of the resulting notches.

It is now clear that matching of the unit capacitors is required only within each coefficient cell, meaning that only every  $M=5$  unit capacitors should be matched together. This is more simple (and also more realistic) than having to match all of the 150 unit capacitors of the entire filter.

Actually, it was not desirable to match the unit capacitors together (using cross-coupling techniques) due to their already large number. If every unit capacitor was to be divided into two or four smaller capacitors, the complexity of the layout would have extended to an unreasonable level. It was instead preferable to suppress the effects of process gradients through an optimized placement of the unit capacitors.

The layout of an AAF capacitor bank is illustrated in Fig. 5.29. The  $M$  unit capacitors of each coefficient cell were arranged in a vertical array, hence minimizing the effects of gradients along the horizontal axis.

The placement of the complementary unit cells was also optimized to suppress linear gradients (for example, the gate oxide capacitance  $C_{ox}$ ) along the  $y$ -axis. This is achieved by keeping the total variation of the selected capacitances proportional to the implemented coefficient.

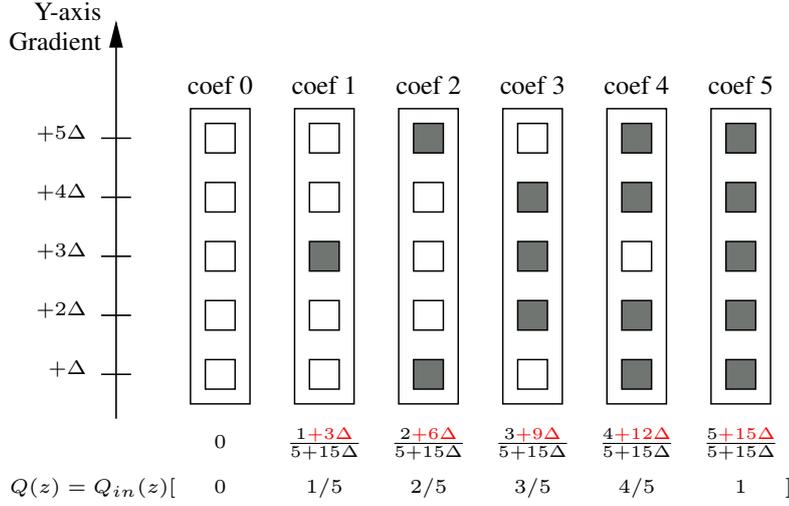


Figure 5.29: Gradient cancellation within AAF coefficients

For example, the coefficient  $\alpha = 3/5$  is constructed using the middle three unit capacitors. When the input current is integrated into the coefficient cell, the charge accumulated on these three unit capacitors is given by :

$$\begin{aligned}
 Q_3(z) &= Q_{in}(z) \cdot \frac{C_3}{\sum_k C_k} \\
 &= Q_{in}(z) \cdot \frac{(C + 2\Delta) + (C + 3\Delta) + (C + 4\Delta)}{\sum_{k=1}^5 (C + k\Delta)}
 \end{aligned}$$

resulting in a coefficient equal to :

$$\alpha = \frac{Q_3}{Q_{in}}(z) = \frac{3C + 9\Delta}{5C + 15\Delta} = \frac{3}{5}$$

which proves that the placement scheme of Fig. 5.29 indeed cancels linear gradients along the y-axis. The proposed layout structure is thus robust against both vertical and horizontal process gradients, assuring that the AAF performances are only limited by technology systematic mismatches.

Gradient cancellation was also implemented at the AAF top level, through an optimal placement of the coefficient cells along the horizontal axis.

Equation (5.6) states that capacitor mismatches between coefficient cells affect only the gain at the AAF output. Recalling that successive output samples are generated by three different combinations of the capacitor banks, this would result in a periodically varying output gain (with a period of  $3T_s$ ). This is similar to gain mismatches in time-interleaved systems and results in SNR degradation and folding of components at  $F_s/2 \pm kF_s/3$  frequencies over the desired signal.

To keep the gain at the AAF output constant over successive samples, the variation of  $\sum C_i$  total capacitance must be the same during the three possible bank combinations. This was achieved by optimally placing the AAF coefficients cells along the horizontal axis, as illustrated in Fig. 5.30.

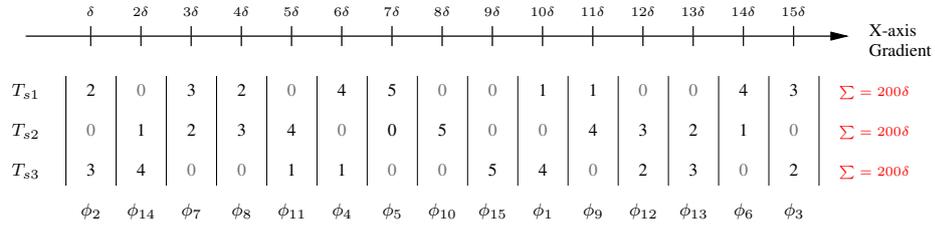


Figure 5.30: Gradient cancellation at AAF top level

The specific placement of the coefficient cells along the x-axis actually assures that the variation of the total capacitance ( $= 200\Delta$ ) would be the same for the three  $T_{s_i}$  successive output phases. The gain mismatch is thus cancelled using this optimal scheme.

The placement of the coefficient cells was found by trial and error and was first optimized for GSM mode. To limit the complexity of the design, it was decided to use this same placement also for WIFI mode, even if non optimal. Hopefully, the achieved gradient cancellation was almost as good as in GSM mode.

## 5.9 Conclusion

This chapter presented the circuit design of the proposed receiver front-end and detailed the reconfiguration mechanisms implemented within the analog and digital blocks. A hierarchical bottom up methodology was used for the design of the anti-alias filter and helped reducing both the complexity and the development time of this stage.

It is shown that the analog signal processing is considerably affected by parasitic capacitors and circuit mismatches, requiring the use of gradient cancellation techniques along with an optimized layout placement and routing.

It is also shown that the design of fully generic and reconfigurable DTASP stages can be too complex and even impractical with the current architecture schemes. In this case, a possible and interesting solution may consist in using a field programmable array of coefficient cells (for the analog processing) associated to an FPGA core (for the generation of the clock phases).

# Chapter 6

## Experimental results

### 6.1 Introduction

This chapter presents the prototype circuit implementation of the dual-mode discrete-time receiver that was proposed and detailed in the previous chapters. The device under test and the evaluation board used for measurements are first described. Some measurement results (focusing primary on gain and filtering) are then given and compared to the expected performances.

Due to time constraints, it has not been possible to design an evaluation board specifically dedicated for the presented circuit prototype. The measurements were actually performed using a borrowed evaluation board that was designed for a previous and resembling test chip. Unfortunately, the difference in pinout placement (between both circuits) did not allow for a complete and precise evaluation of the proposed circuit.

A set of preliminary measurement results is presented here, to prove the correct functionality of the circuit. For a more precise performance evaluation, it is necessary however, to design a fully dedicated test board.

Besides, the evaluation of the anti-alias filter (which is one major contribution in thesis work) is confronted with additional problem (due to the narrow bandwidth of the LNTA currently used) and might not be measured with high accuracy.

### 6.2 DUT and bench description

#### 6.2.1 Chip layout and packaging

The proposed receiver front-end test chip, shown in Fig. 6.1 was implemented and fabricated using the STMicroelectronics 90nm CMOS technology (with standard process options).

The active core area is  $0.91\text{mm}^2$  and the total chip area is  $2.5\text{mm}^2$ . Different power supply and ground pads were used to reduce crosstalk between the noisy digital part and the sensitive analog blocks. Almost all the unused on-chip area was filled with decoupling capacitors that were connected to the power supplies and reference voltages for a better stabilization. The circuit was packaged in a

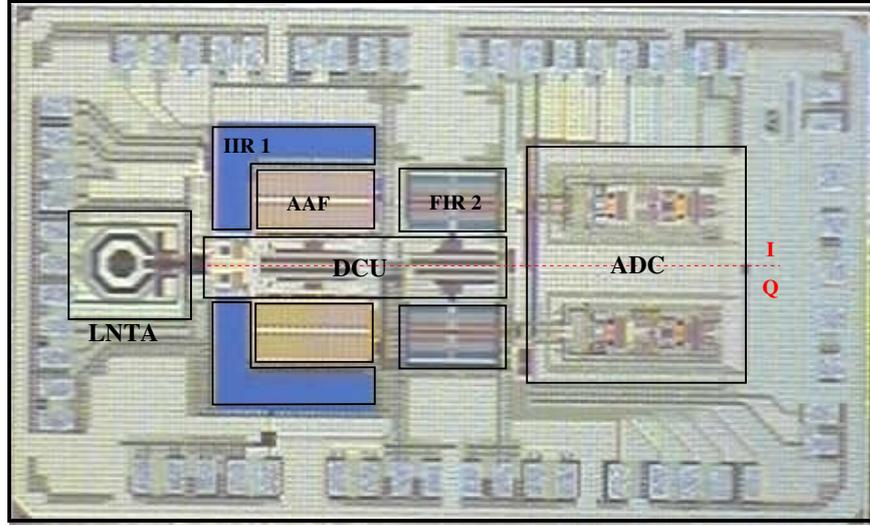


Figure 6.1: Chip microphotograph of the proposed discrete-time receiver

TQFP44L ( $10 \times 10 \times 1.4$ ) slug version and gold bondings were used to connect the on-chip I/O pads to the package pins.

### 6.2.2 Evaluation board description

A synaptic of the evaluation board is given in Fig. 6.2. The signal from the RF generator is divided by a  $0^\circ - 180^\circ$  coupler and then fed to the differential inputs of the LNTA. An LC network was added on board and adjusted for impedance matching at the receiver RF input.

A second RF signal at  $4F_c$  frequency is fed to the receiver CLK input. A bias tee is used to couple the AC signal from the RF generator with a constant offset voltage (common mode). In this way, the clock signal applied at the CLK input is a sine wave at  $4F_c$  frequency and centered at  $V_{offset} = V_{dd}/2 \approx 0.6v$ .

The operating mode of the receiver is controlled by the GSM\_WIFI pin (high level for GSM, low level for 802.11g) and should be set before starting the receiver. A reset signal must be applied to the circuit in order to reset the internal digital logic block and hence start the normal operation of the receiver.

The following analog signals were buffered on chip and outputted to allow the evaluation of the receiver:

- $V_{his1,P}$  and  $V_{his1,N}$  : differential voltage across the history capacitor of the first IIR stage (I path), available in both modes
- $V_{his2,P}$  and  $V_{his2,N}$  : differential voltage across the history capacitor of the second IIR stage (I path), available only in GSM mode
- $V_{wifi,P}$  and  $V_{wifi,N}$  : differential voltage at the output of the anti-alias filter (I path), available only in 802.11g mode

These analog outputs are converted from differential to a single ended voltage (using external differential amplifiers in unity gain configuration) and them measured using analog oscilloscopes and/or spectrum analyzers.

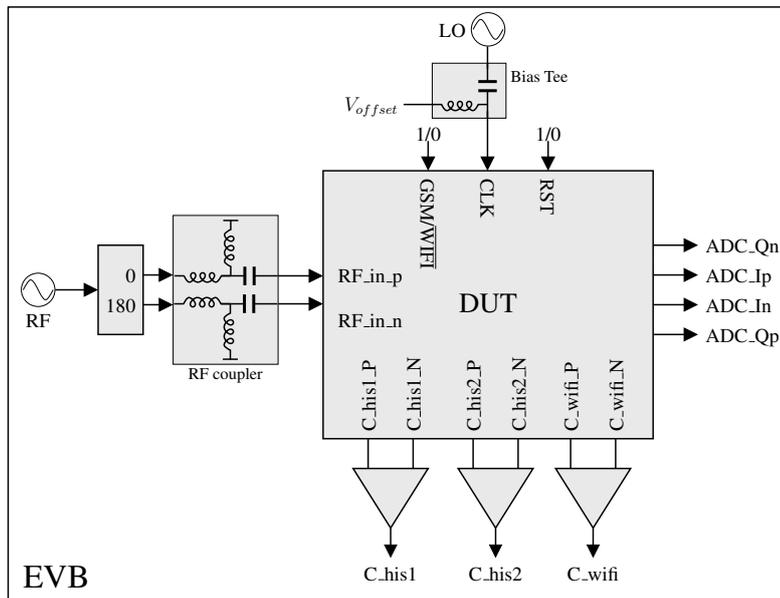


Figure 6.2: Evaluation board synaptic

The outputs of the  $\Sigma\Delta$  modulator ( $I_p$ ,  $I_n$ ,  $Q_p$  and  $Q_n$ ) are also available for evaluation. These outputs are acquired using a logic analyzer and then sent to a computer for further processing.

### 6.2.3 Validation plan overview

The following test plan was adopted for the validation and performance measurement of the proposed receiver front-end. All measurements were performed twice, a first time in GSM mode and a second time in 802.11g mode.

1. Debug phase
2. Current consumption
3. Gain
  - gain vs frequency
  - gain vs RF input power
4. Filters
  - IIR filter rejection
  - Anti-alias filter rejection

### 6.2.4 Notes on ADC analysis

In GSM mode, FFT (Fast Fourier Transform) analyses can be performed on the acquired ADC samples in order to plot the spectrum of the downconverted signal. At this point, the RF signal frequency should be carefully selected in order to get accurate results.

In normal operation, an RF signal at frequency  $F_c = 945MHz$  is first sampled at  $2F_c$  rate and then decimated twice by  $M = 5$  and  $L = 9$  ratios.

The sampling rate at which the ADC  $\Sigma\Delta$  modulator is operated is thus equal to  $F_{s,ADC} = 2 \cdot 945/5/9 = 42MHz$ . When an FFT analysis is performed with  $N_{FFT} = 2^{15} = 32768$  points, a frequency resolution of  $\Delta f = F_{s,ADC}/N_{FFT} = 1281.738Hz$  can be reached.

For gain and filtering measurements at 20 kHz offset from carrier, the nearest FFT frequency bin is located at:

$$F_{bb} = \lfloor \frac{20kHz}{\Delta f} \rfloor \cdot \Delta f = 19.22kHz$$

This RF signal frequency should be thus set to  $F_c = 945.01922MHz$  for optimal FFT analysis and spectrum estimation in GSM mode.

## 6.3 Measurement results

### 6.3.1 Debug phase

The debug phase consisted in adjusting the board and environment settings (reference voltages, supply voltages, LO amplitude and offset voltage) for correct and optimal functioning of the receiver under test. The following observations and comments were derived during the debug phase:

- The receiver logic block is very sensitive to the amplitude and offset of the master clock ( $4F_c$  frequency clock). The offset voltage that is DC coupled at the CLK input of the receiver must be set around  $V_{offset} = 0.65v$  and the amplitude of the RF sine must be increased if higher frequency rates are used.
- The logic block seems to be unstable as the outputs of the receiver vanish after a period of several minutes, requiring a hardware reset. This may come from the topology adopted for the sequential stages inside the logic block (that generates the clock sampling phases).
- Switching from GSM to 802.11g during normal operation (by changing the logic level applied on the GSM\_WIFI pin) disturbs the functioning of the receiver and requires a hardware reset. This is also related to the design of the logic block, which was not supposed to support mode switching without a reset phase.

Apart from the previous observations, the receiver seemed to be fully functional and operated in a normal way in both modes, all over the RF frequency range of [500 MHz - 1200 MHz], corresponding to a master LO clock frequency of [2GHz - 4.8 GHz].

The current consumptions on the different power supplies were measured and are listed in Tab. 6.1. The measurement results are in complete concordance with simulations for the GSM mode. Notice how the power consumption of the discrete-time receiver is only due to the digital blocks, the analog stages being fully passive.

The power consumption of the proposed receiver is relatively high compared to the discrete-time circuit realizations reported in the literature. This is mainly due to the synchronous implementation of the digital logic and to the oversizing of the clock buffers. The power consumption can be greatly reduced in the future by optimizing the design of the digital blocks.

Pin	Name	Voltage	GSM @ 3.6Ghz		802.11g @ 4Ghz
			measure	simulation	measure
9	vdd_ana_1	1.25 v	8 mA	7.4 mA	7.7 mA
22	vdd_dig_1	1.25 v	22 mA	23.4 mA	22.8 mA
23	vdd_LO	1.25 v	36 mA	24.7 mA	24.3 mA
26	vdd_dig_2	1.25 v	14 mA	16.4 mA	--
27	vdd_ana2	1.25 v	43 $\mu$ A	56 $\mu$ A	--

Table 6.1: Voltage supply current consumption

### 6.3.2 Gain evaluation

Following the debug phase, the gain of the prototype circuit was estimated by measuring the analog output voltages in both modes.

#### Gain versus RF frequency

The gain of the receiver was first measured versus RF frequency. The level of the RF input signal was set to  $P_{in} = -35dBm$  and the RF frequency was swept from 500MHz to 1200MHz by 5MHz increment. At the same time, the frequency of the clock signal was also swept accordingly to keep  $f_{LO} = 4 \cdot f_{RF}$  at every step (the RF signal is actually offset by 20kHz not to measure a DC constant). The measured output voltages are given in Fig. 6.3 and Fig. 6.4 for GSM and 802.11g modes respectively.

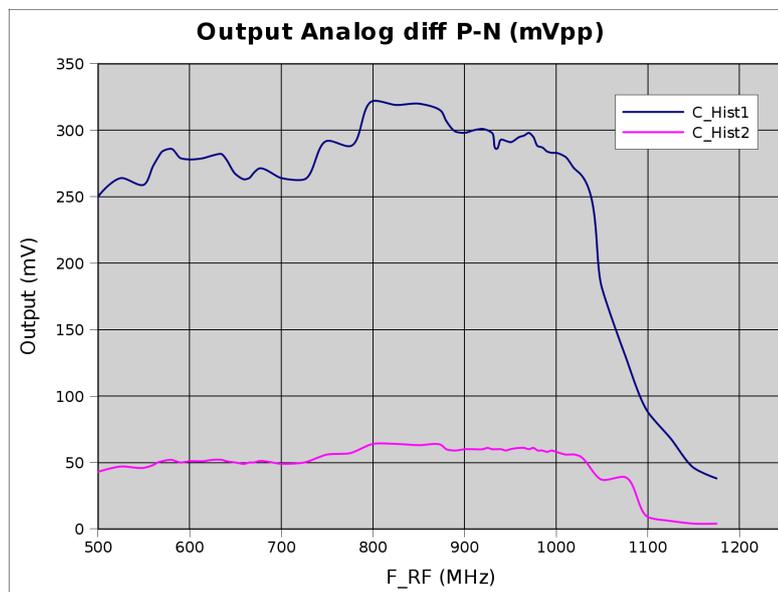


Figure 6.3: Gain versus RF input frequency (GSM mode)

It is seen from these graphics that the gain of the receiver (mainly the gain of the LNTA) is almost constant in the range of frequencies [500MHz - 1050MHz] which corresponds to the bandwidth of the transconductance LNA.

In GSM mode, an important signal loss is noticeable at the output of the second DTASP stage. This problem may come from the connection between

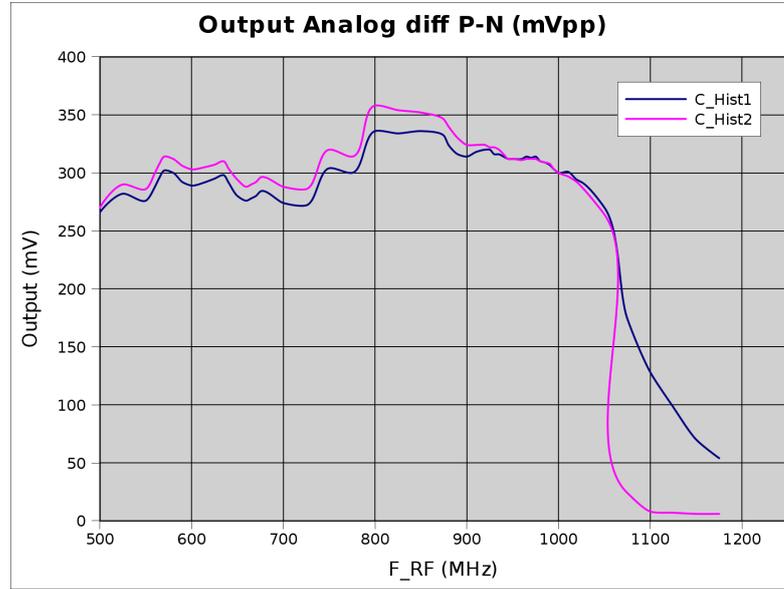


Figure 6.4: Gain versus RF input frequency (802.11g mode)

the first and second DTASP stages, although not visible in simulations. Further investigations are required to locate more precisely the source of the problem. This is a problematic point, as the signal level at the output of the second DTASP stage is very low and doesn't allow for sensitivity measurements (as in this case, the output signal would be at noise floor level).

In 802.11g mode, the gains at the output of the anti-alias filter is slightly lower than the gain at the output of the first IIR stage. This is in accordance with electrical simulations and corresponds to a small signal loss through the anti-alias filter.

The gain of the first DTASP stage can be calculated by the following formula:

$$G_1 = 20 \log \frac{1.53 \times V_{hist1}}{2\sqrt{2}}$$

where  $V_{hist1}$  is the voltage at first history capacitor (expressed in differential peak-peak voltage  $V_{pp,diff}$ ) and the 1.53 factor comes from the on-chip output buffer gain (which is  $0.65 = 1/1.53$ ).

The measurement and simulation results concerning the voltage gains of the different analog stages are compared in Tab. 6.2. Apart from the unexpected gain drop in GSM mode, all the remaining results are almost in concordance.

Gain (dB)	LNTA		SINC <sup>2</sup>		DTASP2	
	meas	sim	meas	sim	meas	sim
GSM @945Mhz	34.6	37.4	N/A	-1.83	-14.51	-2.28
WIFI @1.01Ghz	34.9	36.1	-0.12	-0.2	N/A	

Table 6.2: Voltage gain at intermediate stages

### Gain versus RF input power

The gain of the receiver is next measured at a variable RF input level. The frequency of the RF input signal was fixed and the power level was swept from -70dBm to -15dBm by 5dBm increment. The measured output voltages are plotted in Fig. 6.5 and Fig. 6.6 (logarithmic Y-scale) for GSM and 802.11g modes respectively.

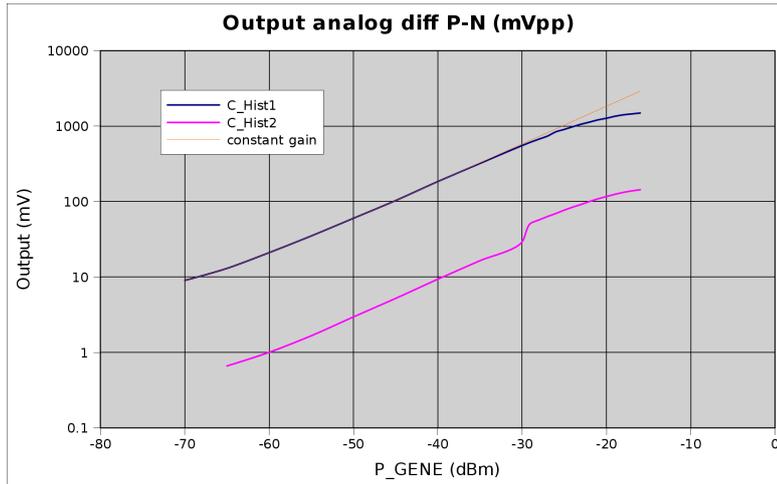


Figure 6.5: Gain versus RF input level (GSM mode)

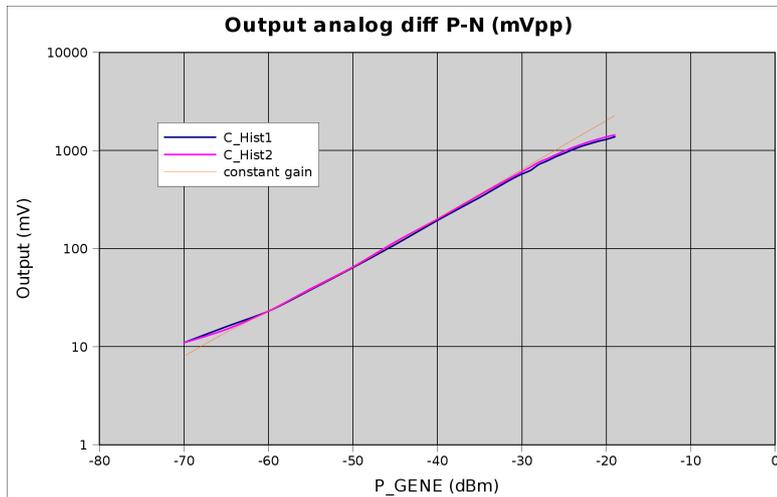


Figure 6.6: Gain versus RF input level (802.11g mode)

In both modes, the gain of the receiver stays constant with the RF input signal level. The 1-dB compression point can be extracted from these graphics when plotted in logarithmic scale.

### 6.3.3 Filtering evaluation

The filter response of the IIR filter stages is given in Fig. 6.7 for the GSM mode. The rejection of the second IIR stage ( $C_{hist2}$ ) is in accordance with both system level and electrical simulations. The rejection of the first IIR filter is however more flat than expected.

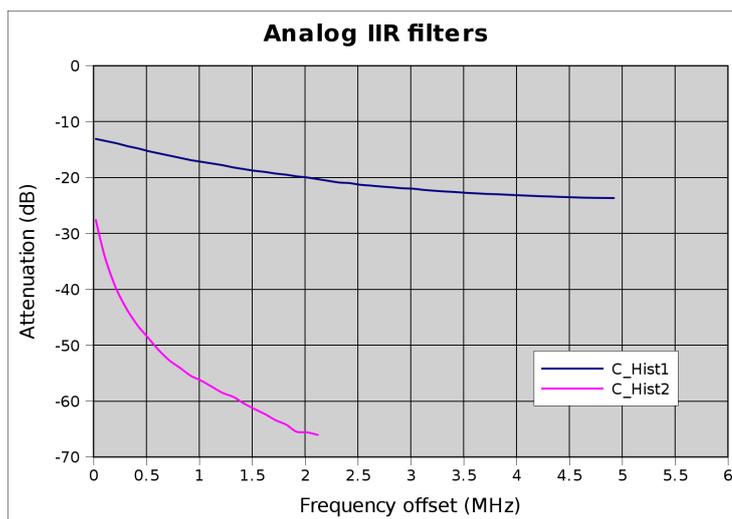


Figure 6.7: IIR filters response in GSM mode

## 6.4 Conclusion

This chapter presented the results of the preliminary measurements that were performed on the proposed dual-mode discrete-time receiver and proved the functionality of the prototype circuit. The reconfigurability of the receiver was validated as different behaviours and filtering functions were observed when switching between GSM and 802.11g modes.

The measured circuit gain in GSM mode was shown to be lower than expected (compared to simulation results) and may be caused by higher parasitic capacitors than estimated through post-layout extractions.

The design of a dedicated evaluation board is planned in the future to allow complete and more precise measurements of the proposed receiver.

# Chapter 7

## Conclusion

### Summary

The first part of the thesis reviewed some of the radio receiver architectures that are mostly used in today's wireless communication systems (with focus on reconfigurability, high integration and low power), in search for new receiver architectures suitable for multistandard applications and more generally for Software Defined Radio (SDR). Under the concept of SDR, RF sampling receivers using bandpass sampling, charge-domain sampling and discrete-time analog signal processing techniques become more and more attractive.

The first aim of this thesis has been to investigate and propose a reconfigurable receiver architecture based on the above concepts. A discrete-time RF sampling receiver was actually proposed and implemented in 90nm CMOS technology. The GSM900 and 802.11g standards were chosen as targets for the system study and the validation of the receiver reconfigurability (as different frequency plans and filtering schemes were adopted for each standard). The receiver was composed of a transconductance LNA, two stages of discrete-time analog signal processing for frequency downconversion, anti-alias filtering, decimation and partial channel filtering. By changing the sampling rate and some circuit level parameters, it was possible to tune the receiver to different RF bands and adjust the filtering specifications according to the targeted standard requirements.

The second aim of the thesis was to address the aliasing problem present in bandpass sampling based architectures and find new filtering schemes with higher rejections, complete reconfigurability and preferably low power consumption. For this, a discrete-time second order sinc-type anti-alias filter was proposed and included in the RF sampling receiver. Using only passive switched capacitor arrays, the filter allowed for improved rejection and low power consumption at the same time. Moreover, the structure and coefficient of the FIR filter were made reconfigurable to adjust its filtering response to the communication standard in use and hence perfectly fit into a multistandard receiver.

## Future work

The preliminary measurements performed on the prototype circuit receiver front-end showed correct functionality of the receiver. Design of a dedicated evaluation board and additional measurements are however necessary to complete the validation of the receiver architecture and estimate the performances in term of gain and filtering.

To improve the rejection of aliased components, the anti-alias FIR filter could be designed to have more coefficients. This would allow the possibility of setting the filter structure, length and order (with possibly higher orders) by software, depending on the communication standard and its specific filtering requirements.

To further validate the flexibility of RF sampling receivers and the possibility of their use for true multistandard (and software defined radio) applications, additional standards must be targeted and implemented by these receivers. The system level study would be however more complex and time consuming in this case.

At circuit level, programmable field capacitor arrays (in analogy with FPGA) can be an attractive possibility for implementing fully reconfigurable discrete-time analog signal processing stages. Different frequency plans and filter partitioning schemes (which can be translated in terms of unit capacitor number, size and switching) can be stored in memory in the RFIC digital stage. Depending on the communication standard, the analog blocks would be programmed in a specific way to implement the corresponding stored receiver architecture scheme.

# Appendix A

## Scilab code

```
function[A,B,C,w,Nvar,Nfrq,Nsts]=EQDiff(Rl,C1,Cd,Cp,Rr,Cr,Rh,Ch);

// Global variables
global choice;
global I Q N1 I_Q;
global Gm Isg Ia1 Ia2 Ial;
global Fspe Ispe;

Gm = 80e-3;

// Signal, adjacent, blocker and alias levels

Isg = Gm*10^((-103-4-13+3)/20);
Wsg = 2*%pi*1800e6*(1/2+1/18000); // @ Fcarrier = 900.1 MHz

Ial = Gm*10^((-13-4-13+3)/20);
Wal = 2*%pi*1800e6*(1/2+1/5+2/18000); // @ Falias = 1260.2 MHz

Ia1 = Gm*10^((-99-33-4-13+3)/20);
Wa1 = 2*%pi*1800e6*(1/2+16/18000); // @ Fcarrier + 1.6 Mhz

Ia2 = Gm*10^((-23-4-13+3)/20);
Wa2 = 2*%pi*1800e6*(1/2+30/18000); // @ Fcarrier + 3 MHz

// Depending on the desired test case
select choice

case 1 then // signal at sensitivity level
Ilna = 0.5*[Isg Isg];
w = [Wsg;-Wsg];

case 2 then // signal + blocker
Ilna = 0.5*[Isg Isg Ia2 Ia2];
w = [Wsg;-Wsg;Wa2;-Wa2];
```

```

case 3 then // IIR rejection
Ilna = 0.5*[Ia2 Ia2 Ia2 Ia2];
w = [Wsg;-Wsg;Wa2;-Wa2];

case 4 then // Alias rejection (not yet implemented)
Ilna = 0.5*[Isg Isg Ial Ial];
w = [Wsg;-Wsg;Wal;-Wal];

case 5 then // Filter attenuation at a given frequency
disp('signal frequency (offset @Fc)');
Fspe_Hz = input('');
Wspe = 2*%pi*(900e6+Fspe_Hz);
Fspe = 9001 + Fspe_Hz/100e3;
disp('signal level (dBv)');
Ispe_dBv = input('');
Ispe = Gm*10^((Ispe_dBv+3)/20);
Ilna = 0.5*[Ispe Ispe];
w = [Wspe;-Wspe];

else // all signals at RF input
Ilna = 1e-5*ones(1,8);
w = [Wsg;-Wsg;Wal;-Wal;Wa1;-Wa1;Wa2;-Wa2];

end;

Nfrq = length(Ilna);

// -----
// Nodal Analysis (1)
// Circuit netlist description

// Variables are the node voltages: Ulna Upar Uh_I Ur_I Uh_Q Ur_Q
Nvar = 6;

// Possible states are: I/Q/I_Q/NL
// (I phase, Q phase, overlapping, high impedance path)
Nsts = 4;
A = zeros(Nvar,Nvar,Nsts);
B = zeros(Nvar,Nvar,Nsts);
C = zeros(Nvar,Nfrq,Nsts);

// The differential equations describing the state of the system
// during the 4 phases are organised as follows:
// A . dU/dt + B . U = C . exp(%i.w.t)

// Constant set of differential equations
Cst_A=[ Rl*(Cl+Cd/2) -Rl*Cd/2 0 0 0 0 ];
Cst_B=[ 1 0 0 0 0 ];
Cst_C=[ Rl*Ilna ];

```

```
// Description of I/Q integration phases
I_A=[ -Cd/2 Cd/2+Cp Ch Cr 0 0;
      0 0 2*Rh*Ch 0 0 0;
      0 0 0 2*Rr*Cr 0 0;
      0 0 0 0 Ch 0;
      0 0 0 0 0 Cr ];
```

```
I_B=[ 0 0 0 0 0 0;
      0 -1 1 0 0 0;
      0 -1 0 1 0 0;
      0 0 0 0 0 0;
      0 0 0 0 0 0 ];
```

```
I_C=[zeros(5,Nfrq)];
```

```
Q_A=[ -Cd/2 Cd/2+Cp 0 0 Ch Cr;
      0 0 0 0 2*Rh*Ch 0;
      0 0 0 0 0 2*Rr*Cr;
      0 0 Ch 0 0 0;
      0 0 0 Cr 0 0 ];
```

```
Q_B=[ 0 0 0 0 0 0;
      0 -1 0 0 1 0;
      0 -1 0 0 0 1;
      0 0 0 0 0 0;
      0 0 0 0 0 0 ];
```

```
Q_C=[zeros(5,Nfrq)];
```

```
A(:, :, I) = [Cst_A; I_A];
B(:, :, I) = [Cst_B; I_B];
C(:, :, I) = [Cst_C; I_C];
```

```
A(:, :, Q) = [Cst_A; Q_A];
B(:, :, Q) = [Cst_B; Q_B];
C(:, :, Q) = [Cst_C; Q_C];
```

```
// Case where both I and Q path are disconnected
```

```
Nl_A=[ -Cd/2 Cd/2+Cp 0 0 0 0;
      0 0 Ch 0 0 0;
      0 0 0 Cr 0 0;
      0 0 0 0 Ch 0;
      0 0 0 0 0 Cr ];
```

```
Nl_B=[ 0 0 0 0 0 0;
      0 0 0 0 0 0;
      0 0 0 0 0 0;
```

```

        0 0 0 0 0 0;
        0 0 0 0 0 0 ];

N1_C=[zeros(5,Nfrq)];

A(:,:,N1) = [Cst_A;N1_A];
B(:,:,N1) = [Cst_B;N1_B];
C(:,:,N1) = [Cst_C;N1_C];

// Overlapping between I and Q paths

I_Q_A=[ -Cd/2 Cd/2+Cp Ch      Cr      Ch      Cr;
         0      0      2*Rh*Ch 0      0      0;
         0      0      0      2*Rr*Cr 0      0;
         0      0      0      0      2*Rh*Ch 0;
         0      0      0      0      0      2*Rr*Cr ];

I_Q_B=[ 0 0 0 0 0 0;
        0 -1 1 0 0 0;
        0 -1 0 1 0 0;
        0 -1 0 0 1 0;
        0 -1 0 0 0 1 ];

I_Q_C = [zeros(5,Nfrq)];

A(:,:,I_Q) = [Cst_A;I_Q_A];
B(:,:,I_Q) = [Cst_B;I_Q_B];
C(:,:,I_Q) = [Cst_C;I_Q_C];

endfunction;

// -----
// Main program
// Define circuit parameters & call EQDiff function

clc;
getf("EQDiff.sce");

PLOT_TRANSIENT = 0;
PLOT_SPECTRUM  = 1;

global choice;
global I Q;
global N1 I_Q;
global Gm Isg Ia1 Ia2 Ial;
global Fspe Ispe;

I = 1; Q = 2; N1 = 3; I_Q = 4;

```

```

printf('Make your choice : \n');
printf('[1] siganl @ sensi. level \n');
printf('[2] signal + blocker @3MHz \n');
printf('[3] IIR rejection \n');
printf('[4] alias rejection \n');
printf('[5] enter a given Fin & Pin config.\n');
choice = input('');
printf('\n');

//-----
// Circuit parameters settings

Rlna = 6e3;      // LNTA output impedance
Clna = 50e-15;  // real & imaginary parts

Cdec = 1.5e-12; // Decoupling capacitor value

Chis = 120e-12; // History capacitor value
Rhis = 70;      // ON resistance of Chis switches

Ncap = 5;
Csig = 10e-15;  // Unit capacitor value
Rsig = 2.7e3;   // ON resistance of Csig switches

// Parasitic capacitance definition
Cpar_ih = 55e-15;
Cpar = Cpar_ih + (Cdec*0.015)/2 + 33e-15;
printf('Parasitic capacitance: Cpar = %.2e\n',Cpar);

[A,B,C,w,Nvar,Nfrq,Nsts]=EQDiff(Rlna,Clna,Cdec,Cpar, ...
Rsig/Ncap,Ncap*Csig,Rhis,Chis);

//-----
// Nodal Analysis (2)

// Matrix diagonalization & basis change

Pass = zeros(Nvar,Nvar,Nsts); // matrix eigenvectors
Pinv = zeros(Nvar,Nvar,Nsts); // inverse matrix
E     = zeros(Nvar,Nfrq,Nsts); // new basis coefficients
VP    = zeros(Nvar,1,Nsts);    // state values

for k = 1 : Nsts
    [Pass(:,:,k),Diag] = spec(inv(A(:,:,k))*B(:,:,k));
    VP(:,:,k) = diag(Diag);
    Pinv(:,:,k) = inv(Pass(:,:,k));
    E(:,:,k) = (Pinv(:,:,k)*inv(A(:,:,k))*C(:,:,k))./(VP(:,:,k) ...
    *ones(1,Nfrq)+%i*ones(Nvar,1)*w');
end

```

```

clear A B C Diag;

// Sampling matrix
// Node voltages are multiplied at every sampling phase
// Reset unit capacitors & rotate history capacitor
//
//      Ulna  Udec  Uh_I  Ui_I  Uh_Q  Ui_Q
Sampling = [1    0    0    0    0    0 ;
            0    1    0    0    0    0 ;
            0    0   -1    0    0    0 ;
            0    0    0    0    0    0 ;
            0    0    0    0   -1    0 ;
            0    0    0    0    0    0 ] ;

// Definition of the operation scenario
// Setting of carrier frequency and overlapping time
Fc = 900e6;
Tc = 1/Fc;
Trc = 0;

if (Trc < 0) then
    // both I and Q paths are disconnected
    Tnr = -Trc;
    sequence = [I N1 Q N1];
    seq_time = [Tc/4-Tnr Tnr Tc/4-Tnr Tnr];
elseif (Trc > 0)
    // overlapping between I and Q integration phases
    sequence = [I I_Q Q I_Q];
    seq_time = [Tc/4-Trc Trc Tc/4-Trc Trc];
else
    // ideal case of distinct I and Q phases
    sequence = [I Q];
    seq_time = [Tc/4 Tc/4];
end

seq_size = length(sequence);

// Simulation settings
Nstart = 4000; // transient samples to throw away
Nsamples = 18000; // useful samples
Nstop = Nstart + Nsamples;

// Initialisation
U = zeros(Nvar,1); // nodes voltages initially at zero
index = 0; // current state = sequence[index]
nSample = 0; // number of last sample
time = 0; // start time of current phase

```

---

```

tNextState = 0;          // end time of current phase
Samples = zeros(Nsamples,Nvar+1);  // array of stored samples

// Simulation main loop
while (nSample<Nstop)

    // find the next state of the system
    index = index + 1;
    state = sequence(index);

    // find the time duration of this state
    tNextState = time + seq_time(index);

    // Node voltages at the end of the current state
    V = Pinv(:, :, state)*U;
    V = (V-E(:, :, state)*exp(w*i*time)).*exp(VP(:, :, state) ...
        *(time-tNextState))+E(:, :, state)*exp(w*i*tNextState);
    U = Pass(:, :, state)*V;

    // sample node voltages if at the end of the sequence
    if (index == seq_size) then
        index = 0; // start the sequence again
        nSample = nSample + 1; // increment number of samples
        if (nSample>Nstart) then
            Samples(nSample-Nstart,:) = [time U']; // store the sample
        end
        U = Sampling*U; // sampling of node voltages
    end
    time = tNextState; // update time pointer
end

// Data post-processing

// Plot transient node voltages
if PLOT_TRANSIENT then
    scf(1); clf;
    mix = (-1).^(0:Nsamples-1)';
    plot(Samples(:,1),mix.*Samples(:,2),'b'); // v_lna
    plot(Samples(:,1),mix.*Samples(:,3),'r'); // v_par
    plot(Samples(:,1),mix.*Samples(:,4),'g'); // v_his_I
    plot(Samples(:,1),mix.*Samples(:,5),'k'); // v_sig_I
    xgrid; legend('v_lna','v_par','v_hisQ','v_sigQ');
end

// Spectral analysis
F = (0:Nsamples-1)*2*Fc/Nsamples;
v_sig = Samples(:,5);
V_sig = 20*log10(abs(fft(v_sig/Nsamples))+1e-14);
if PLOT_SPECTRUM then

```

```

    scf(2); clf;
    plot(F, V_sig, 'r');
    xgrid; legend('FFT signal C_R');
end

Ceq = 1/(1/Clna+2/Cdec)+Cpar;
z = exp(-2*%pi*i*(Fc+100e3)/4/Fc);
IIR_100kHz = abs(5*Csig/(5*Csig+Cpar+Chis-Cpar*z+Chis*z^2));
IIR_100kHz = 20*log10(IIR_100kHz);
G_lnta_theo = 20*log10(Gm/(sqrt(2)*%pi*Fc)/(5*Csig));
G_bloc_theo = G_lnta_theo + 20*log10(5*Csig/(5*Csig+Cpar));
G_bloc_simu = max(V_sig) - 20*log10(Isg/2/Gm);

select choice
case 1 then
    printf('G_bloc_theo = %.2f\n', G_bloc_theo);
    printf('G_bloc_simu = %.2f\n', G_bloc_simu);

case 2 then
    v_lna_out_max_pp_diff = 2*max(abs(Samples(:,2)))

case 3 then
    z1 = exp(-2*%pi*i*(Fc+3e6)/4/Fc);
    IIR_3MHz = abs(5*Csig/(5*Csig+Cpar+Chis-Cpar*z1+Chis*z1^2));
    IIR_3MHz = 20*log10(IIR_3MHz);
    reject_3MHz_theo = IIR_100kHz - IIR_3MHz;
    reject_3MHz_simu = V_sig(9002) - V_sig(9031);
    printf('\n reject_3MHz_theo = %.1f \n', reject_3MHz_theo);
    printf('reject_3MHz_simu = %.1f \n', reject_3MHz_simu);

case 5 then
    G_lnta_iir = V_sig(Fspe)-20*log10(Ispe/2/Gm)

else disp('no results');
end;

```

# Appendix B

## Noise analysis

This appendix presents a noise analysis of the discrete time analog signal processing blocks. The thermal noise from the reset, sampling and output switches is combined and added along the different operating phases of the filters.

It is assumed here that all the circuit blocks are linear. The total output noise is hence obtained by using the superposition principle. The history capacitor  $C_h$  and buffer capacitor  $C_b$  are ignored in the following study, considering their large values which make their contribution to thermal noise negligible.

### First DTASP stage

The noise contributed by the first DTASP stage comes from the switching of the different unit capacitors. An equivalent noise model is given in Fig. B.1 for a coefficient cell of the SINC<sup>2</sup> anti-alias filter.

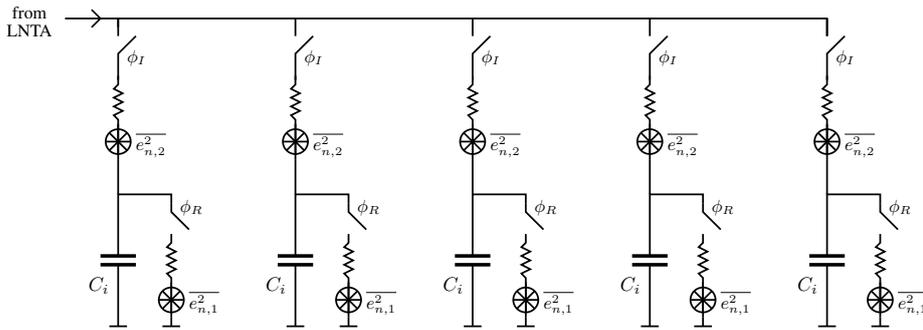


Figure B.1: Thermal noise sources in a coefficient cell

During the reset phase  $\phi_R$ , the unit capacitors are discharged through the common node  $V_{cm}$  and each one samples a noise voltage of  $\sqrt{kT/C_i}$  due to the ON resistance of the reset switches. During the integration phase, the unit capacitors are connected in parallel to the output of the LNTA. The noise voltage at the end of this phase is the combination of (1) the thermal noise from the reset switches and (2) the thermal noise from the integration switches.

The noise voltages of  $\sqrt{kT/C_i}$  which are due to the reset switches are uncorrelated and hence are square added once the unit capacitors are connected in parallel. The resulting noise power stored on each unit capacitor is given by:

$$e_{n,1}^2 = \frac{\sum Q^2}{(\sum C_i)^2} = \frac{\sum C_i^2 (kT/C_i)}{(5C_i)^2} = \frac{5C_i kT}{25C_i^2} = \frac{kT}{5C_i}$$

which can be seen otherwise as the sum of five uncorrelated random variables with a standard deviation of  $\sqrt{kT/C_i}$  (and hence divided by a factor  $\sqrt{5}$ ).

The noise contribution from the integration switches can be evaluated by analyzing the noise from each switch separately and summing them using the superposition principle. An equivalent circuit to describe the integration switches  $\phi_I$  noise contribution is shown in Fig. B.2.

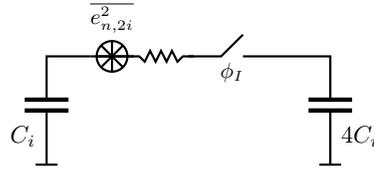


Figure B.2: Equivalent circuit for the integration switch noise contribution

When considering only a single integration switch, we see that its corresponding unit capacitor  $C_i$  is actually in series with the remaining capacitors  $4C_i$ . The noise contribution from the integration switches is hence given by:

$$e_{n,2}^2 = 5 \cdot kT \left( \frac{1}{C_i} + \frac{1}{4C_i} \right) \cdot \left( \frac{C_i}{4C_i + C_i} \right)^2 = \frac{kT}{4C_i}$$

where the first term in parenthesis accounts for thermal noise related to the capacitors in series and the term in squared parenthesis accounts for the voltage division between  $C_i$  and  $4C_i$ .

By summing the noise contributions from the reset and integration switches of the five unit capacitors, the total noise power at the end of the integration phase can be finally written as:

$$e_{n,3}^2 = e_{n,1}^2 + e_{n,2}^2 = \frac{kT}{5C_i} + \frac{kT}{4C_i} = \frac{9kT}{20C_i}$$

The last operating phase of the first DTASP stage is the output phase, where the unit capacitors of the coefficient cells are connected together to a rotating capacitor from the second DTASP stage. The noise power at the end of this phase is the combination of (a) the thermal noise  $e_{n,3}^2$  from the reset and integration phases, (b) the thermal noise from the reset switch of the rotating capacitor  $C_r$  and (c) the thermal noise from all the output switches. As previously, these three contributions will be studied separately and then summed to evaluate the total noise power added by the first DTASP stage. An equivalent circuit is given in Fig. B.3 to better illustrate the noise combination process.

The thermal noise contributions  $e_{n,3}^2$  from the reset and integration switches of the unit capacitors (25 capacitors in GSM mode) are divided (capacitive voltage divider) and then added. The noise addition is not straightforward however, because the 25 contributions  $e_{n,3}^2$  cannot be considered this time as uncorrelated

and hence do not simply add in power. This is because the capacitors from the same coefficient cell have actually the same noise power. The noise contributions are thus root square added, as follows:

$$\begin{aligned}
 e_{n_{4,a}}^2 &= \left[ \frac{9kT}{20C_i} + \left( \sqrt{\frac{9kT}{20C_i}} + \sqrt{\frac{9kT}{20C_i}} \right)^2 + \dots \right] \cdot \left( \frac{C_i}{25C_i + C_r} \right)^2 \\
 &= \frac{9kT}{20C_i} \left[ \sum_{k=1 \dots 5 \dots 1} k^2 \right] \cdot \left( \frac{C_i}{25C_i + C_r} \right)^2 \\
 &\simeq 38 \cdot \frac{kT}{C_i} \cdot \left( \frac{C_i}{25C_i + C_r} \right)^2
 \end{aligned}$$

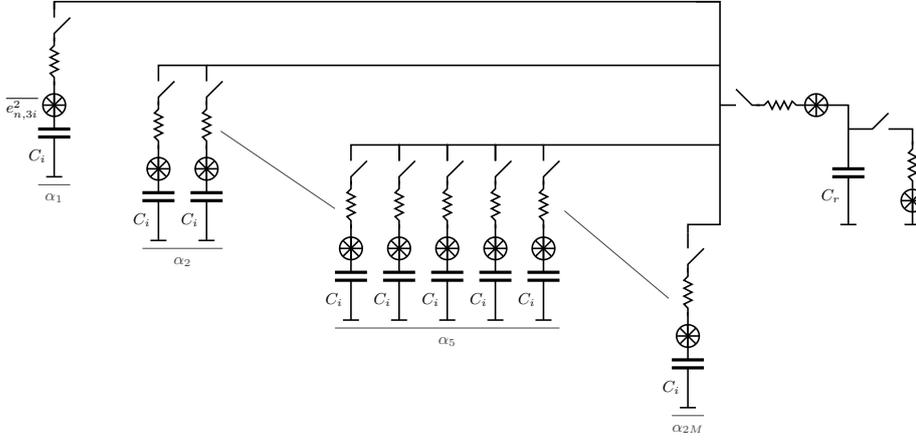


Figure B.3: Noise model for the output of the 1<sup>st</sup> DTASP stage

At the start of the output phase, the thermal noise  $kT/C_r$  accumulated during the reset phase of the capacitor  $C_r$  is divided over all the capacitors, giving rise to a noise contribution of:

$$e_{n_{4,b}}^2 = \frac{kT}{C_r} \cdot \left( \frac{C_r}{25C_i + C_r} \right)^2$$

The noise contribution of the output switches can be estimated in a similar way to the integration switches. The analysis can be made easier by considering all the output switches as a single switch connected to the  $C_r$  capacitor. This assumption is actually true because the output switches are in series and operate at the same time. The noise contribution is hence given by:

$$\begin{aligned}
 e_{n_{4,c}}^2 &= kT \cdot \left( \frac{1}{C_r} + \frac{1}{25C_i} \right) \cdot \left( \frac{C_r}{25C_i + C_r} \right)^2 \\
 &= kT \cdot \frac{25C_i + C_r}{25C_i C_r} \cdot \left( \frac{C_r}{25C_i + C_r} \right)^2 \\
 &= \frac{kT}{25C_i} \cdot \frac{C_r}{25C_i + C_r}
 \end{aligned}$$

The total noise power added by the first DTASP stage is simply the sum of the noise contributions  $e_{n_{4,a}}^2$  to  $e_{n_{4,c}}^2$  (which are uncorrelated) and is given by:

$$\begin{aligned} e_{n_4}^2 &= e_{n_{4,a}}^2 + e_{n_{4,b}}^2 + e_{n_{4,c}}^2 \\ &= \frac{kT}{25C_i + C_r} \left[ \frac{38C_i + C_r}{25C_i + C_r} + \frac{C_r}{25C_i} \right] \end{aligned}$$

Note finally that this noise power must be divided by the oversampling ratio  $BW/F_{s_1}$  as only the fraction of thermal noise located inside the signal bandwidth is in concern here, finally leading to:

$$e_{\text{DTASP1}}^2 = \frac{kT}{25C_i + C_r} \left[ \frac{38C_i + C_r}{25C_i + C_r} + \frac{C_r}{25C_i} \right] \cdot \frac{BW}{F_{s_1}} \quad (\text{B.1})$$

which is the noise power considered during the overall noise figure computation.

## Second DTASP stage

The noise contribution of the second DTASP stage comes from the switches connecting the FIR filter capacitors  $C_r$  to the buffer capacitors  $C_b$  and then to the input stage of the ADC (Fig. B.4). Note that the noise contribution of the reset switches has been included in the noise added by the first DTASP stage and will not be considered here.

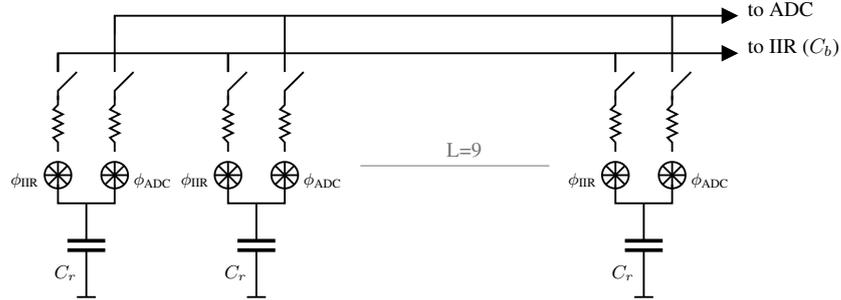


Figure B.4: Noise sources through the 2<sup>nd</sup> DTASP stage

The noise contribution of the averaging switches during the IIR phase (which is also the same for the ADC phase) is given by:

$$\begin{aligned} e_{n_6}^2 &= 9 \left[ kT \cdot \left( \frac{1}{C_r} + \frac{1}{8C_r} \right) \cdot \left( \frac{C_r}{C_r + 8C_r} \right)^2 \right] \\ &= 9 \left[ kT \cdot \frac{9}{8C_r} \cdot \left( \frac{1}{9} \right)^2 \right] = \frac{kT}{8C_r} \end{aligned}$$

and the total noise power contributed by the second DTASP stage can be finally expressed as:

$$e_{\text{DTASP2}}^2 = 2 \cdot \frac{kT}{8C_r} \cdot \frac{BW}{F_{s_2}} = \frac{kT}{4C_r} \cdot \frac{BW}{F_{s_2}} \quad (\text{B.2})$$

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