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# Modulateur $\Sigma\Delta$ passe-haut et application dans la réception multistandards

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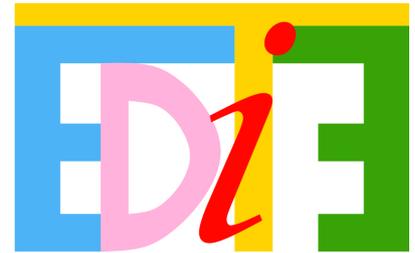
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# Thèse

présentée pour obtenir le grade de docteur  
de l'Ecole Nationale Supérieure des Télécommunications  
Spécialité : Electronique et Communications

Hasham Ahmed KHUSHK

Modulateur  $\Sigma\Delta$  passe-haut  
et application dans la réception  
multistandards

Soutenance le 27 novembre 2009 devant le jury composé de

Philippe Benabes  
Dominique Dallet  
Patrick Garda  
Dominique Morche  
Patrick Loumeau  
Van Tam Nguyen

Rapporteurs  
Examineurs  
Directeurs de thèse



*To my parents, my brothers and sisters.*

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## Abstract

In high-pass (HP)  $\Delta\Sigma$  modulator the signal band is located at  $F_s/2$ , as opposed to  $dc$  for the traditional low-pass (LP)  $\Delta\Sigma$  modulator. Thus the noise shaping completely covers the low frequency noises such as  $1/f$  noise and offset, and they have no effect on the performance of the HP modulator, which is not the case in a LP modulator. This inherent immunity against low frequency noises makes HP  $\Delta\Sigma$  modulator the preferred choice for noise-sensitive applications like Discrete-time  $F_s/2$  receivers, bio-medical instrumentation, time-interleaved  $\Delta\Sigma$  architectures etc.

In this thesis, research has been carried out at various abstraction levels to optimize the HP  $\Delta\Sigma$  modulator operation. A top-down approach is adopted to achieve this objective. Beginning with the RF receiver architecture, the newly created  $F_s/2$  receiver is selected for its enhanced compatibility with HP  $\Delta\Sigma$  modulator as compared to other state of the art receiver architectures namely zero-IF and low-IF receivers.

After the receiver topology, the next level of design i-e  $\Delta\Sigma$  modulator architecture is addressed. For this, a detailed study on state-of-the-art LP  $\Delta\Sigma$  modulator topologies is carried out, including various second-order topologies, higher-order single loop structures and MASH structures. We illustrate the latest generation of MASH structures which are free from digital cancellation filters and thus do not require digital calibration techniques to counter the mismatch between analog and digital components: Multi-stage closed loop (MSCL) and its enhanced version Generalized multi stage closed loop (GMSCL). The system-level modeling of various circuit level parameters of traditional second-order structure called Boser structure is illustrated. This study provides us with specifications for transistor level design.

Since the low-frequency noise problem poses challenges for the use of LP modulators in high-resolution applications, the contemporary topologies of LP modulators are converted for HP operation. We also propose a new second-order unity-STF architecture which is advantageous over other topologies in terms of complexity and performance. Behavioral modeling of the proposed structure's circuit-level parameters is carried out, which furnishes us with its specifications. These specifications are compared with other second-order topologies. Since the second-order modulator is unable to provide the required performance, the cascaded or MASH structures for HP operation are explored and a novel technique to improve the traditional MASH topologies in terms of input dynamic range and highest-achieved SNR is proposed. The proposed single-stage second-order topology is used as an individual stage of this new cascade structure. But the mismatch and noise leakage problems still exist in this structure, so GMSCL topology is adopted for HP operation and its structure is modified to incorporate the proposed second-order topology. A recently proposed technique is applied on the quantizer to increase the dynamic range of the converter and to eliminate the need of Dynamic Element Matching (DEM) by diminishing DAC non-linearities. Detailed comparison of performance in the face of circuit non-idealities is performed between HP and LP modulators' various topologies. It provides interesting information about various shortcomings and advantages of HP structures over LP ones.

The next level of design is the conception of a suitable switched-capacitor high-pass

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filter for HP  $\Delta\Sigma$  modulator. The absence of a suitable HP filter has been the main bottle-neck in the realization of HP modulators. Traditional implementations of HP filters revolved around switched capacitor integrator to extract HP filter function. These were inadequate as they resulted in increased power consumption, surface area and reduced bandwidth. But a new scheme has been recently introduced, which resolves these issues and brings the performance of HP filter close to an integrator. We study and analyse three different types of switched-capacitor implementations of HP filter and compare them on the basis of consumption, noise immunity and speed and finally select the best one which has a performance comparable to that of switched-capacitor integrator.

The final abstraction level is the transistor level design of the proposed GMSCL HP architecture, which is performed in 65nm CMOS process. Much attention is given to the design of operational transconductance amplifier since it is the major building block of high pass filters and is the most power consuming element. The target applications are UMTS with 3.84MHz conversion band at 80dB dynamic range and WiMAX with 25MHz bandwidth at 52dB dynamic range.

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# Résumé Étendu

## Introduction

La prolifération des standards sans fil et la diminution de la taille des terminaux radio en même temps pousse vers la matérialisation du concept nouvellement créé de Software Defined Radio (SDR). Ce système de communication est prévu pour réaliser des terminaux radio multibande, multimode en définissant des fonctionnalités de la radio dans les logiciels [1]. De cette façon, le terminal radio est adapté aux différents protocoles et personnalisé pour divers services par seulement une reprogrammation de la fonctionnalité de la radio.

Cependant, ceci rend difficile la conception de récepteurs RF. Dans un SDR idéal, la solution pour augmenter à la fois l'intégration et la reconfiguration du récepteur est fourni par le transfert de l'interface de conversion analogique-numérique juste après l'antenne. L'avantage intrinsèque de ce plan est que le traitement du signal numérique supprime les non idéalités associées au traitement du signal analogique: bruit dispositif, les non-linéarités, désappariements des composants, etc. L'évolution des technologies CMOS vers des transistors de plus petites tailles est également favorable à une augmentation du niveau de traitement du signal numérique dans la mise en œuvre du récepteur [2].

Aujourd'hui, le traitement numérique peut fonctionner à une fréquence très élevée et peut ainsi traiter des signaux à haute fréquence. La limite entre le front-end RF et bande de base numérique est déplacé à plus haute fréquence, mais pas encore à la fréquence RF. Un des points limitant majeur est la conception du convertisseur analogique-numérique (CAN) qui peut convertir le signal aux hautes fréquences. Avec les technologies CMOS actuelles, il n'est pratiquement pas possible de concevoir un CAN qui convertit le signal directement en RF.

Cependant, le traitement doit être effectué autant que possible dans le numérique en raison de la faiblesse des coûts, de la possibilité de reconfiguration et de stabilité. Pour avancer dans cette direction, un récepteur fondé sur le sous-échantillonnage a été proposé. Le signal RF est sous-échantillonné dès que possible. La descente en fréquence est réalisé par le sous-échantillonneur avec le traitement des signaux en temps discret. Un cas particulier de récepteur RF qui utilise un sous-échantillonnage temps discret est  $F_s/2$  IF récepteur [3, 4]. Cette architecture réduit la fréquence du signal de RF à un IF de  $F_s/2$  (moitié de la fréquence d'échantillonnage), rendant ainsi le modulateur  $\Sigma\Delta$  passe-haut (PH) le choix naturel pour les CAN. Ce CAN est d'une complexité très réduite par rapport au modulateur  $\Sigma\Delta$  passe-bande (PB).

Outre l'avantage de convertir directement en IF, le modulateur  $\Sigma\Delta$  PH a le potentiel

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d'éliminer efficacement les DC-offsets et les bruits à basse fréquence, comme le bruit de scintillement [5, 6, 7], qui sont une source de préoccupation dans les modulateurs  $\Sigma\Delta$  passe-bas traditionnels. Cette caractéristique est particulièrement intéressante pour les convertisseurs  $\Sigma\Delta$  à entrelacement temporel où l'offset du canal est suffisamment enlevé par une opération PH [8].

En dépit de ces avantages potentiels, le concept de modulation  $\Sigma\Delta$  PH n'a pas reçu beaucoup d'attention, principalement en raison de sa mise en œuvre difficile et les incertitudes quant à sa stabilité et ses performances en présence de non-idéalités de circuit. La difficulté a été la mise en œuvre du filtre passe-haut, qui a la même importance qu'un intégrateur pour le modulateur  $\Sigma\Delta$  passe-bas. La mise en œuvre traditionnelle implique une boucle autour d'un intégrateur; c'est une solution très coûteuse en raison de l'augmentation de la consommation d'énergie et de la surface. Toutefois, récemment, une nouvelle architecture du filtre PH a été proposée. Elle permet de se débarrasser des inconvénients de l'architecture traditionnelle et propulse donc un intérêt renouvelé pour les modulateurs  $\Sigma\Delta$  PH.

Compte tenu de ses potentialités, cette thèse est axée sur la modulation  $\Sigma\Delta$  PH en général et son application au mode multi-récepteurs sans fil en particulier. Nos objectifs consistent à étudier son principe, ses performances et la stabilité et à le comparer à des modulateurs passe-bas, d'une part et de l'appliquer pour atteindre multi-modal fonctionnalité du récepteur sans fil sur l'autre.

Pour atteindre ces objectifs, une nouvelle architecture de modulateur  $\Sigma\Delta$  PH simple boucle à fonction de transfert de signal (STF) unitaire a été proposée. Elle est ensuite utilisée pour construire une architecture PH: "Generalized-Multi-Stage-Closed-Loop (GM-SCL)". Le modulateur PH proposé doit fournir les spécifications du standard EDGE/GSM, tandis que la structure GMSCL PH est utilisée pour les standards UMTS/WLAN.

## Architecture du Récepteur RF

Les front-end RF de différentes architectures de récepteur radio concurrentes, sont discutés dans ce chapitre. La topologie Superhétérodyne de récepteur RF est la plus populaire commercialement en raison de sa performance. Pour répondre à l'augmentation des contraintes sur le frontal du récepteur, y compris l'intégrabilité et de reconfiguration, de nouvelles topologies de récepteur sont en cours d'introduction. Le récepteur Digital IF est exposé, qui est un type d'architecture superhétérodyne où le signal est numérisé au niveau de IF. Le récepteur à conversion directe présente l'avantage de la simplicité et le nombre de composants réduit. Il se débarrasse des éléments qui ne sont pas intégrables. Mais il a des problèmes de désappariement entre les voies I et Q, du DC-offset et du bruit de scintillement qui corrompent le signal. Le récepteur Low-IF se débarrasse des problèmes associés au récepteur à conversion directe, mais il introduit son propre problème de l'image. Pour cela, les filtres de rejet d'images doivent être utilisés mais sont coûteux en consommation et en surface. Pour rendre les récepteurs intégrables, reconfigurable et flexible (réalisation du concept de radio logicielle), la technique d'échantillonnage passe-bande est utilisée. Elle contribue à réduire le nombre de composants analogiques en numérisant

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le signal à des stades antérieurs dans le frontal du récepteur. Une application de cette technique de réception est l'architecture récemment introduit :  $F_s/2$  IF récepteur. Son schéma de principe est illustré dans la Fig. 1.

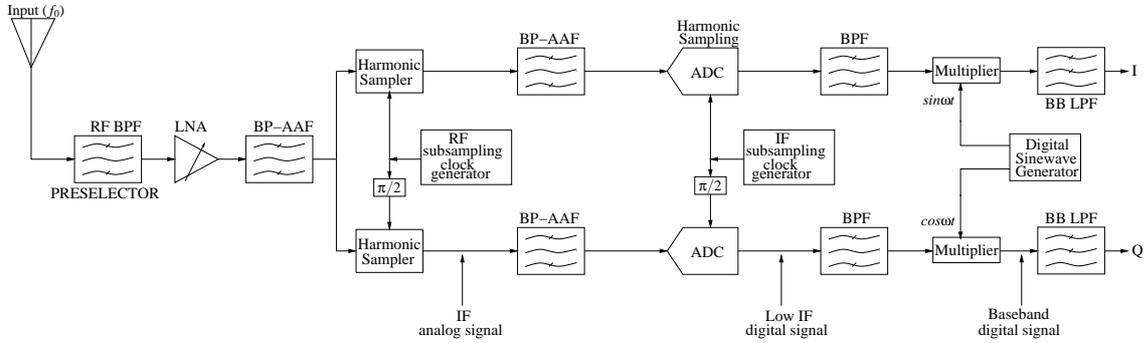


Figure 1: L'architecture du Récepteur  $F_s/2$  IF

Il résout les problèmes des récepteurs à conversion directe et des récepteurs à faible IF, tout en conservant les avantages de chacun d'eux. Dans cette architecture, la fréquence d'échantillonnage est choisie de telle sorte que après la descente en fréquence, le signal utile tombe à la moitié de la fréquence d'échantillonnage. En conséquence, l'image est le conjugué du signal, et donc évite des filtres de rejection de la bande image. En outre, puisque le signal est centré à  $IF = F_s/2$ , le DC-offset des différents composants, bruit de scintillement et les produits des non-linéarités du second ordre (IP2) ne dégrade pas le signal. Le bruit de scintillement est bien ce qui limite généralement les implémentations CMOS des architectures zéro-IF, pour des normes à bande étroite. Pour numériser directement ce signal, un type spécial de CAN avec des modulateurs  $\Sigma\Delta$  PH est nécessaire.

Une chaîne de réception RF de ce type qui traite les deux protocoles sans fil: GSM et WiFi est défini dans [3]. L'architecture de récepteur est illustrée à la Fig. 2.

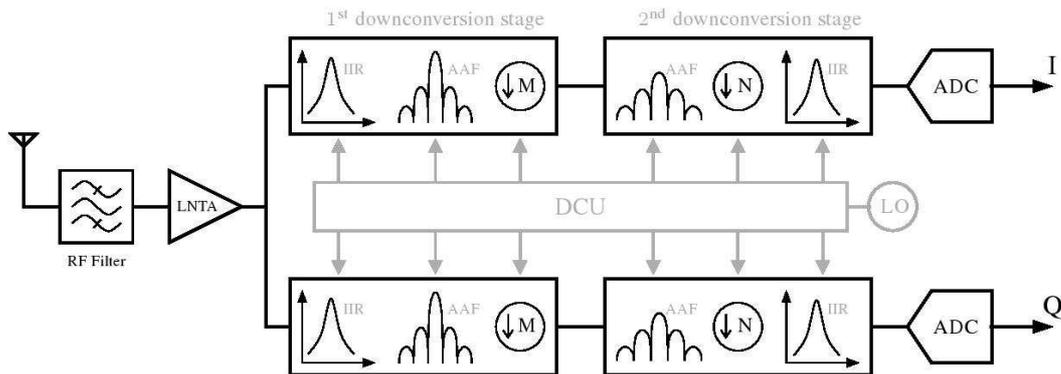


Figure 2: Dual-Mode  $F_s/2$  Récepteur d'échantillonnage en temps discret [3]

Il se compose d'un filtre RF, un Low Noise Transconductance Amplifier (LNTA), deux étages de traitement du signal à temps discret analogiques (DTASPs) et d'un CAN. Le

signal d'entrée RF est d'abord filtré, amplifié et converti en un courant. Il est ensuite transmis à la première tranche DTASP, où il est filtré et remis en quadrature à la première fréquence intermédiaire. Une deuxième étape de translation vers les basses fréquences décime encore le taux d'échantillonnage et filtre le signal IF, avant qu'il soit enfin numérisé.

### Les Plans de Fréquence proposés

Après l'étude de l'état-de-l'art des récepteurs RF, et compte tenu des performances des CANs disponibles, le plan de fréquences illustré à la Fig. 3 est proposé. Notez que contrairement au frontal du récepteur présenté plus tôt [3], l'architecture  $F_s/2$  est adoptée à la fois pour les deux protocoles pour ne pas être sensible au bruit de scintillement et au DC-offset dans le traitement du signal.

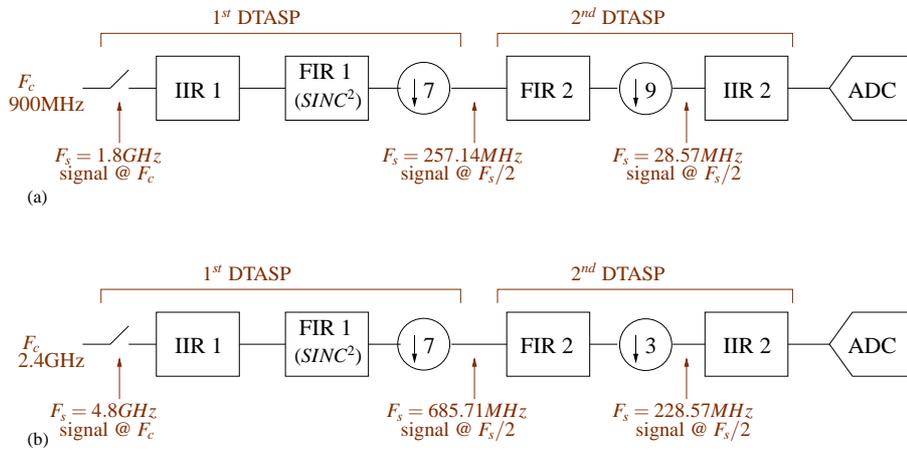


Figure 3: (a) Plan de Fréquence en mode GSM, (b) Plan de Fréquence en mode WIFI

Le CAN pour le mode GSM fonctionne à la vitesse 28.57MHz, tandis que le CAN pour le mode WiFi est configuré pour fonctionner à 228.57MHz.

Dans les travaux de recherche effectués dans notre laboratoire, tous les blocs dans la chaîne de récepteur multi-mode de fonctionnement ont déjà été conçus [3], avec un accent particulier sur la conception d'un filtre anti-repliement [9]. L'objectif de ce travail de recherche est de proposer et de concevoir un CAN à partir d'un modulateur  $\Sigma\Delta$  PH qui peut prendre en charge plusieurs normes sans fil et être intégré dans la chaîne de réception déjà conçue.

### Modulateur $\Sigma\Delta$ et Sa Modélisation au Niveau Système

Le principe de base du CAN  $\Sigma\Delta$  est qu'il échange la résolution de sortie avec la vitesse de conversion. Dans un tel CAN, le signal analogique est converti en un code de faible résolution à une fréquence beaucoup plus élevée que le taux de Nyquist, et puis le bruit de quantification en excès est éliminé par les filtres numériques [10]. Ainsi, plus le rapport de suréchantillonnage du CAN  $\Sigma\Delta$  est élevé, plus les contraintes sur les blocs analogiques sont

relâchées. Fig. 4 montre le schéma de base d'un modulateur  $\Sigma\Delta$  et de son modèle linéaire correspondant. Le modulateur Sigma-Delta se compose d'un chemin feedforward formé par un filtre de boucle et un quantificateur de  $B$ -bits, et un chemin de rétroaction négative qui les entoure, en utilisant un convertisseur numérique-analogique (CNA) à  $B$ -bits aussi [11]. Dans le modèle linéaire comme l'illustre dans la Fig. 4, le CNA est supposé être idéal et l'erreur de quantification injectée est supposée être un bruit blanc additif. Bien que cette approximation n'est pas valable pour les quantificateurs avec une faible résolution, il est néanmoins utilisé pour la simplicité des calculs.

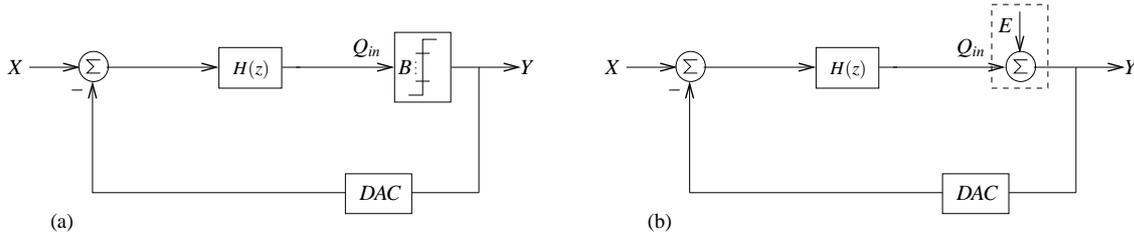


Figure 4: Modulateur  $\Sigma\Delta$  de Base (a) Schéma, (b) Correspondant modèle linéaire

Le filtre de boucle est tout simplement un intégrateur qui peut être facilement mis en œuvre avec des techniques à capacités commutées. Pour un modulateur  $\Sigma\Delta$  généralisé d'ordre  $L$ , les fonctions de transfert sont:

$$STF(z) = z^{-L} \quad (1)$$

$$NTF(z) = (1 - z^{-1})^L \quad (2)$$

Pour parvenir à une fonction de transfert d'ordre  $L$ ,  $L$  blocs de base soit  $L$  intégrateurs sont nécessaires. Fig. 5 montre les réponses en fréquence des  $NTF$ s pour différentes valeurs de  $L$ . Lorsque l'ordre du modulateur est supérieur à un, la réponse en fréquence de la  $NTF$  présente la caractéristique des filtres passe-haut. Plus on augmente l'ordre du modulateur, plus le bruit sera rejeté en basses fréquences.

De cette façon, le signal de sortie pour le modèle idéal linéaire peut être écrite comme:

$$Y(z) = X(z)z^{-L} + E(z)(1 - z^{-1})^L \quad (3)$$

Le modulateur  $\Sigma\Delta$  du second ordre est populaire car il fournit un bon compromis entre performance et complexité. Il peut également être utilisé comme un bloc de base pour des modulateurs d'ordre supérieur. Plusieurs architectures de second ordre sont proposées dans la littérature, notamment Boser-structure [12], Silva-structure [13] et Oberst-structure [14]. Leurs avantages et inconvénients sont examinés en détails. Puisque le modulateur de second ordre ne produit pas une performance suffisante pour de nombreuses applications, d'autres modulateurs qui permettent une mise en forme du bruit d'ordre supérieur sont étudiés en détail. Il existe deux grandes familles de modulateur d'ordre supérieur 1) les modulateurs d'ordre supérieur en simple boucle, 2) les multi-boucles ou des structures

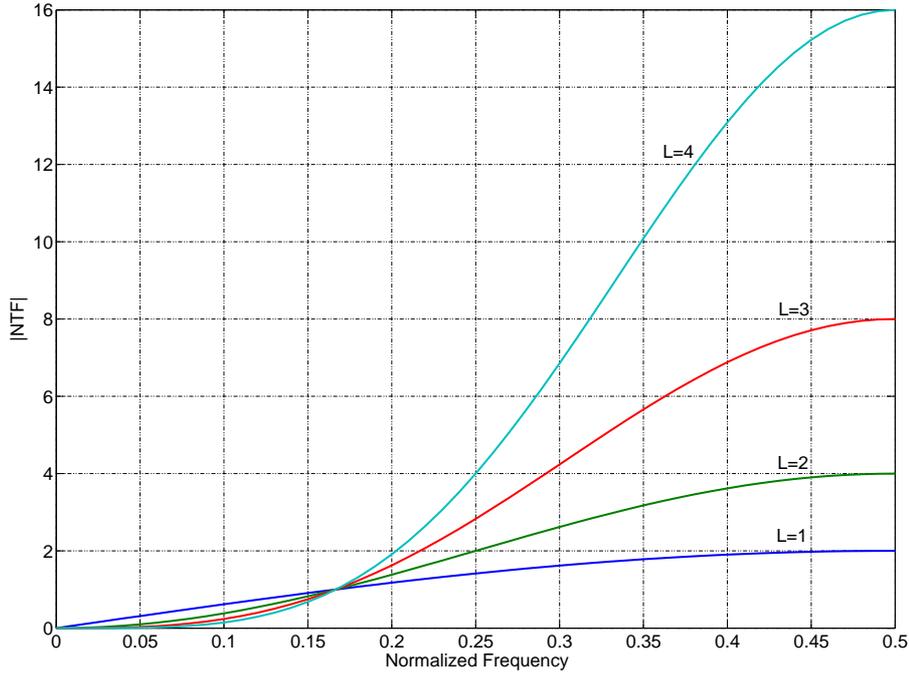


Figure 5: Réponses en fréquence de NTFs pour modulateurs des ordres  $L$  différentes

MASH (Multi-stAge noise SHaping). Quatre techniques importantes pour une mise en forme de bruit plus élevée en simple boucle existent: le Cascade d'Intégrateurs avec Distributed Feedback (CIFB), le Cascade de Résonateurs avec Distributed Feedback (CRFB), le Cascade d'Intégrateurs avec Distributed Feedforward (CIFF), le Cascade de Résonateurs avec Distributed Feedforward (CRFF). Dans les structures MASH, les topologies les plus performantes sont Generalized Multi-Stage Closed Loop (GMSCL) [15, 16] et les modulateurs  $\Sigma\Delta$  MASH robustes [17].

## Modélisation au Niveau Système

La modélisation au niveau système aide à déterminer les spécifications des éléments constitutifs fondamentaux de modulateur  $\Sigma\Delta$ . Elle est la première étape dans la conception de circuits intégrés analogiques. Aux fins de la modélisation au niveau système, la structure classique de Boser [12] est choisie. La modélisation est effectuée pour la gigue d'horloge, le bruit thermique du commutateur et le bruit des amplificateurs-operationnels (ampli-op). La modélisation au niveau des ampli-op comprend la saturation, le gain-DC fini, le produit gain-bande passante fini et le "slew rate" fini. Les non-idéalités du comparateur: le DC-offset et l'hystérésis sont également pris en compte. Il se trouve qu'on a besoin d'un ampli-op avec  $\pm 1.3V_{ref}$  de dynamique de sortie, 40dB de gain-DC,  $5F_s$  de produit GBW et  $1.8F_s$  SR pour atteindre une performance proche de l'état idéal.

## Modulateur $\Sigma\Delta$ Passe-Haut

Le principe de fonctionnement du modulateur  $\Sigma\Delta$  PH est le même que celui du modulateur  $\Sigma\Delta$  passe-bas: le bruit de quantification est mis en forme hors de la bande du signal par un filtre de boucle. La différence réside dans le placement de la bande du signal. Dans le cas de modulateur  $\Sigma\Delta$  PH, il se situe à  $F_s/2$ , où  $F_s$  est la fréquence d'échantillonnage, par rapport à une bande passante en bande de base pour le modulateur  $\Sigma\Delta$  passe-bas. Ainsi, la transformation d'un passe-bas en modulateur passe-haut est une transformation passe-haut à passe-bas de la fonction de transfert bruit de quantification. Cette transformation permet au modulateur  $\Sigma\Delta$  PH d'être complètement insensible aux bruits de basses fréquences.

### Structure d'Unité-STF proposée

Une nouvelle structure dont la STF est unitaire et qui pallie les insuffisances des architectures de modulateur existantes est proposée. Cette topologie de conversion passe-haut est illustrée à la Fig. 6. Il s'agit d'une structure mixte "feedforward-feedback" dans laquelle le signal attaque le comparateur directement. Le signal utile est annulé à l'entrée de deux filtres passe-haut. Ainsi le problème des distorsions du signal utile par le deuxième ampli-op, associé à l'architecture à base de Oberst, a été adressé. Les filtres passe-haut sont mis en œuvre à l'aide de filtres à retard, ce qui élimine la question de l'augmentation de la charge sur l'ampli-op mis en œuvre dans le premier filtre passe-haut, ce qui n'est pas le cas dans la structure de base Oberst. Les problèmes relatifs à la topologie à base de Silva ont été résolus en changeant le chemin auxiliaire feedforward, tel que montré dans la Fig. 6.

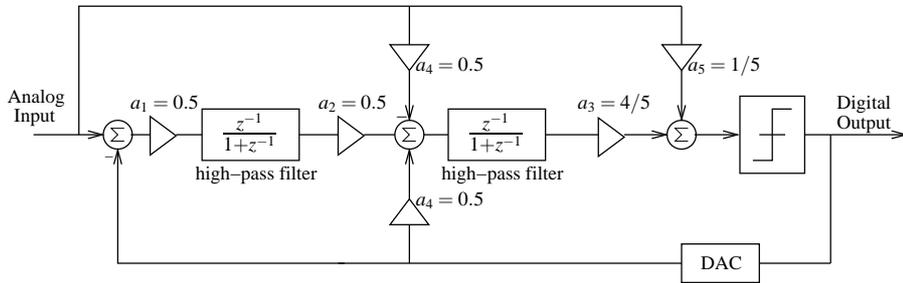


Figure 6: Structure proposée pour l'unité-STF modulateur  $\Sigma\Delta$  passe-haut

Ceci détend les exigences imposées à l'additionneur puisqu'il n'y a que deux branches à ajouter comparé aux trois branches requises dans la structure à base de Silva. Dans ce cas, l'implémentation de cet additionneur passivement, implique une atténuation plus faible du signal ce qui réduit les exigences de conception du quantificateur. La charge sur le premier ampli-op a également été réduite car il n'y a pas de condensateur feedforward à charger.

### Analyse Comparative des Modulateurs $\Sigma\Delta$ PH Boucle Unique

Nous comparons les quatre architectures (Boser, Silva, Oberst, Proposée) en prenant comme critère, les contraintes imposées à l'ampli-op. Les excursions de filtres passe-haut

sont un paramètre important pour la comparaison, car ils sont directement liés à la variation de tension de l'ampli-op mise en œuvre dans les filtres passe-haut. Nous voulons garder ces excursions à un niveau minimal pour simplifier la conception des ampli-op. D'autres non-idéalités comme le gain-DC fini, le GBW fini et SR fini dépendent de l'architecture du modulateur et du flux du signal dans la topologie.

Les quatre architectures avec les valeurs des coefficients, utilisées pour l'analyse de comparaison sont présentées dans la Fig. 7.

### Excursions de Sortie des Filtres Passe-Haut

Les histogrammes montrant les excursions de sortie de deux filtres passe-haut dans les quatre topologies en compétition sont présentés sur la Fig. 8

Les résultats présentés sur la Fig. 8 montrent que la structure PH basée sur celle de Boser a la plus grande excursion pour le premier filtre, ce qui est normal puisque il traite à la fois le signal utile et le bruit de quantification. Toutes les autres structures ont les mêmes excursions pour le premier filtre passe-haut parce qu'elles traitent juste le bruit de quantification. Ces excursions sont bien dans la fourchette des  $-V_{ref} \leftrightarrow V_{ref}$ , soit le pas de quantification et sont facilement réalisables. La tension de saturation de l'amplificateur opérationnel est normalement fixée par le pas de quantification soit la gamme de tension  $-V_{ref} \leftrightarrow V_{ref}$ , mais puisque les excursions de la structure basée sur celle de Boser dépasse cette gamme, nous devons concevoir des ampli-op avec des dynamiques de sortie plus élevées, ce qui augmentera la consommation électrique, qui peut devenir importante dans les technologies à basse tension.

L'excursion du deuxième filtre passe-haut est très inférieur pour la structure à base de Silva, puis vient l'architecture proposée, et enfin les structures de Boser et Oberst. Mais tous sont bien à l'intérieur de l'excursion de la quantification et sont donc faciles à réaliser.

### L'effet des Non-Idéalités de l'Ampli-Op

La performance du filtre passe-haut est directement liée à la performance fournie par son ampli-op. Les non-idéalités des amplificateurs opérationnels dont le DC-gain fini et non linéaire, le fini GBW et le SR fini provoquent un transfert incomplet de la charge dans les capacités commutées (SC) mise en œuvre dans le filtre passe-haut qui est une cause majeure de dégradation des performances de modulateurs  $\Sigma\Delta$  PH.

**DC-Gain Fini** la résolution les équations de transfert de charge pour le filtre PH standard, en présence de l'ampli-op avec un DC-gain fini révèle que la fonction de transfert exacte pour le premier filtre PH est la suivante:

$$H_{practical}(z) = 0.5 \frac{\frac{A_0}{A_0+3.51} z^{-1}}{1 + \frac{A_0-0.99}{A_0+3.51} z^{-1}} \quad (4)$$

Où  $A_0$  représente le gain-DC de l'ampli-op. En utilisant l'Éqn. 4 comme la fonction de transfert pour le premier filtre passe-haut, toutes les architectures discutées plus tôt ont été simulées pour différentes valeurs de  $A_0$  pour comparer l'effet de cette non-idéalité

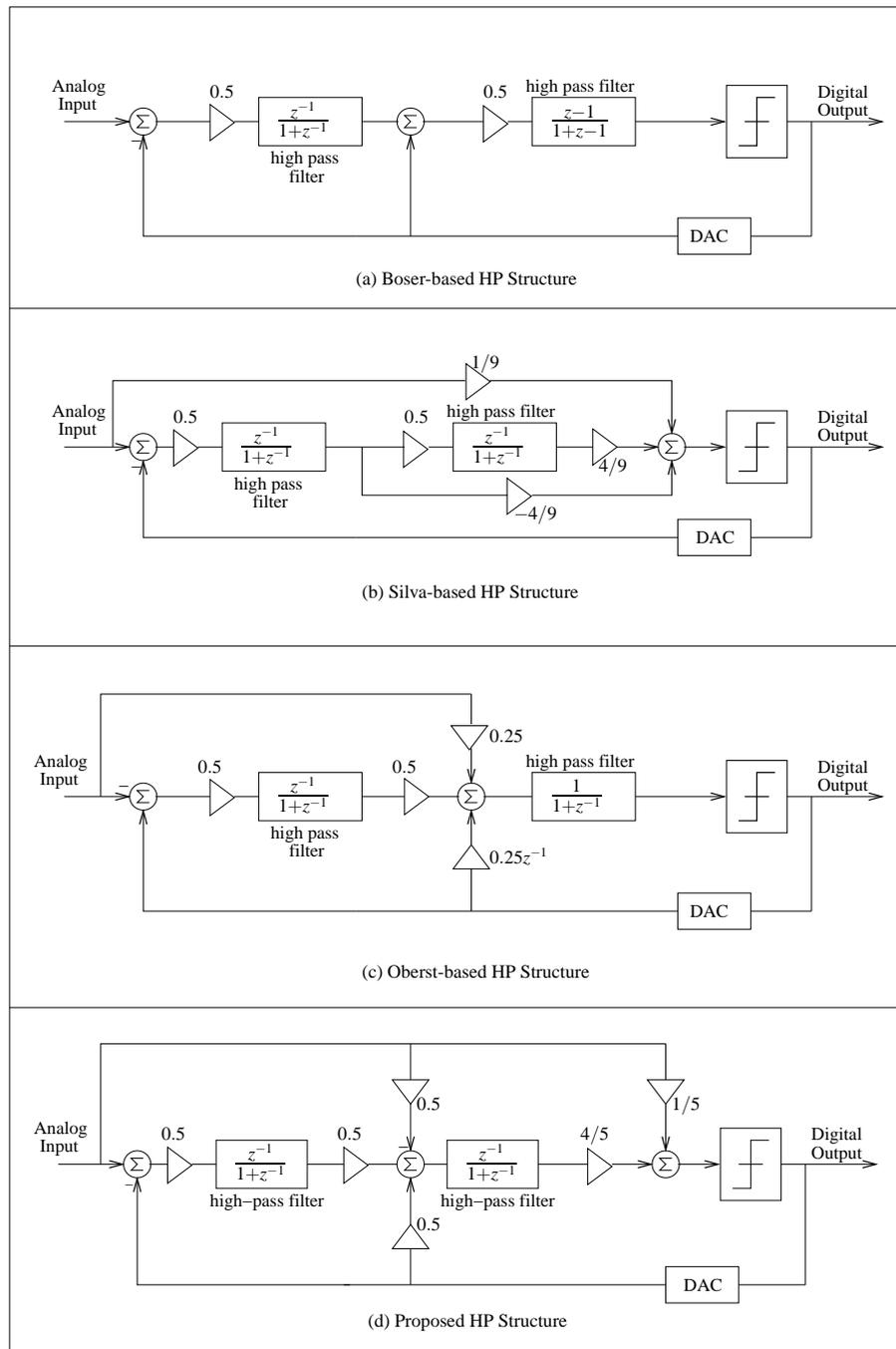


Figure 7: Quatre structures utilisées pour l'analyse comparative

sur les différentes architectures. Le signal d'entrée est une sinusoïde avec une amplitude de 0,4 normalisée par rapport à l'étape de quantification soit  $-8\text{dBFS}$  et sa fréquence vaut  $0.4993F_s$ . Le résultat de la simulation est montré dans la Fig. 9.

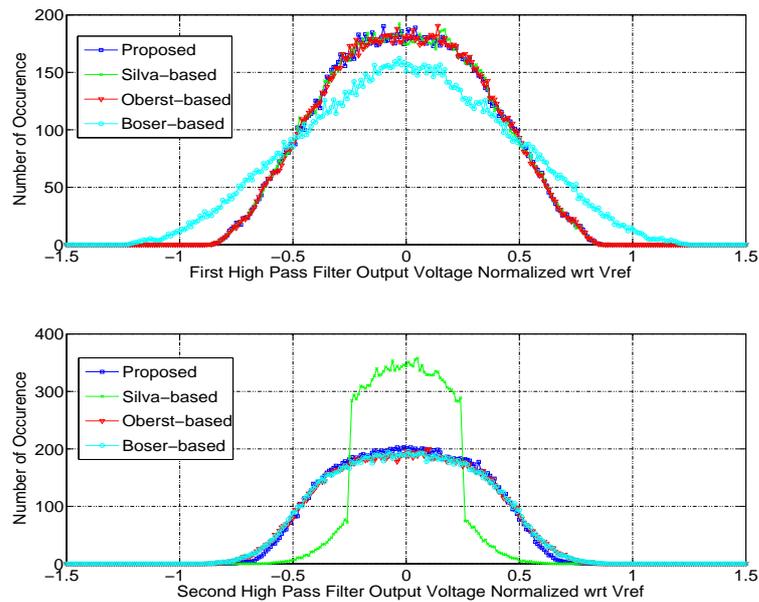


Figure 8: Comparaison d'excursion de sortie des filtres passe-haut à  $V_{in}=-8\text{dBFS}$

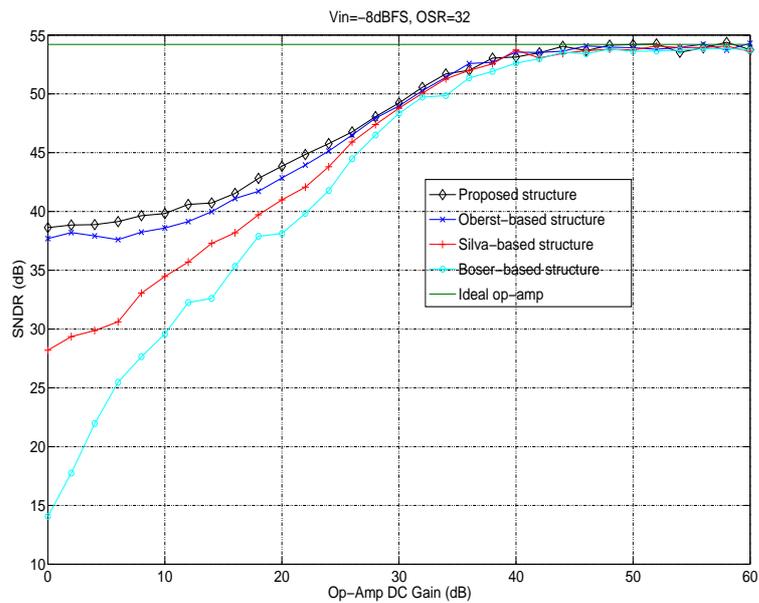


Figure 9: SNR vs. DC-Gain d'Ampli-Op

Cette figure montre que toutes les architectures requièrent un ampli-op avec un gain-DC de 45 dB pour acquérir le rapport signal sur bruit de quantification (SQNR) pour l'amplitude d'entrée fixée. On peut constater que l'architecture proposée est plus robuste que les autres architectures en présence d'un gain-DC faible.

**Le Gain-Bandwidth Product Fini et Le Slew Rate Fini** avec les contraintes supplémentaires de GBW fini et SR fini, la fonction de transfert du filtre HP devient:

$$v_{out}(t) = v_{out}(nT_s - T_s) + V_s - \text{sgn}(V_s)SR_s\tau e^{-\left(\frac{T_s}{2\tau} - \frac{|V_s|}{SR_s\tau} + 1\right)} \quad (5)$$

où  $V_s$  est donné par:

$$V_s = -(1 + \beta)v_{out}(nT_s - T_s) + b\alpha v_{in}(nT_s - T_s/2) \quad (6)$$

où  $v_{out}$  est la sortie du filtre,  $T_s = 1/F_s$  est la période d'échantillonnage,  $v_{in}$  est l'entrée du filtre et  $\tau = (3 + b)/2\pi GBW$  est la constante de temps de l'ampli-op utilisé dans le filtre. La valeur de la constante de temps  $\tau$  est dérivée dans l'annexe. B. Le GBW fini et le SR fini de l'ampli-op produisent des harmoniques dans le spectre de la sortie dégradant ainsi le SNDR. Nous avons effectué des simulations de différentes architectures en faisant varier les valeurs de SR et nous avons observé le SNDR. Cette procédure est répétée pour deux valeurs différentes de GBW de l'ampli-op. Les résultats sont illustrés dans la Fig. 10:

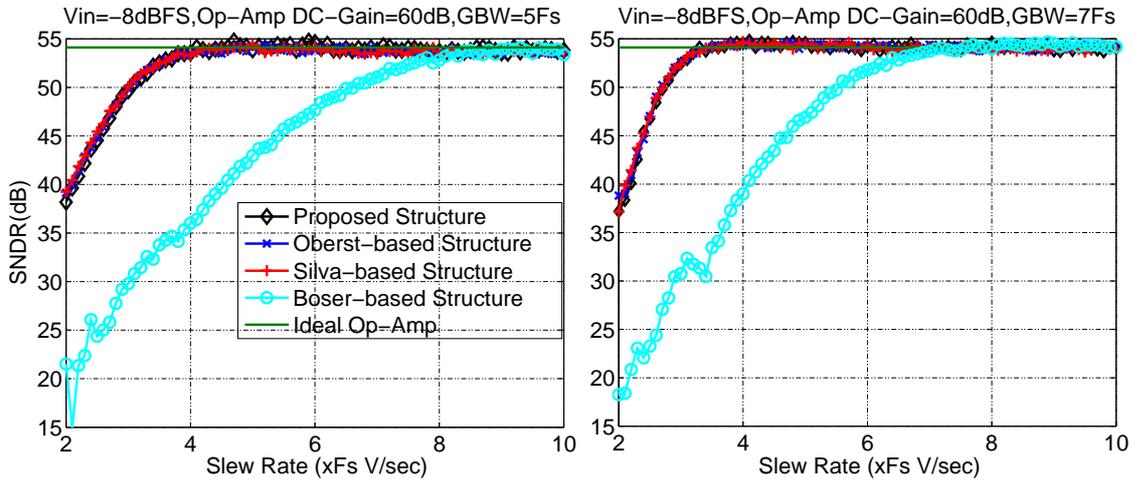


Figure 10: La dégradation des SNDR pour différentes architectures en fonction de SR d'ampli-op

Les résultats montrent qu'au moins un SR de  $4F_s(V/sec)$  est nécessaire pour les structures feedforward pour établir la performance requise, tandis que pour la structure à base de Boser, un SR de  $8.5F_s(V/sec)$  est nécessaire pour garantir le SNDR optimal pour un GBW de  $5F_s$ . Toutes les architectures feedforward ont des meilleures performances comparées à la structure de Boser.

## Les Structures des Modulateurs $\Sigma\Delta$ PH à Boucles Multiples

Dans une structure multi-étages ou MASH, chaque étage est réalisé par un modulateur  $\Sigma\Delta$  différent. L'erreur de quantification d'un étage est l'entrée de l'étage suivant. La sortie de l'étage suivant est donc une approximation de cette erreur de quantification. Les filtres

numériques sont conçus de manière à annuler les erreurs de quantification de tous les étages sauf le dernier. La Fig. 11 montre une architecture générique du modulateur  $\Sigma\Delta$  Cascade 2-1 PH basé sur la topologie proposée du modulateur de seconde ordre.

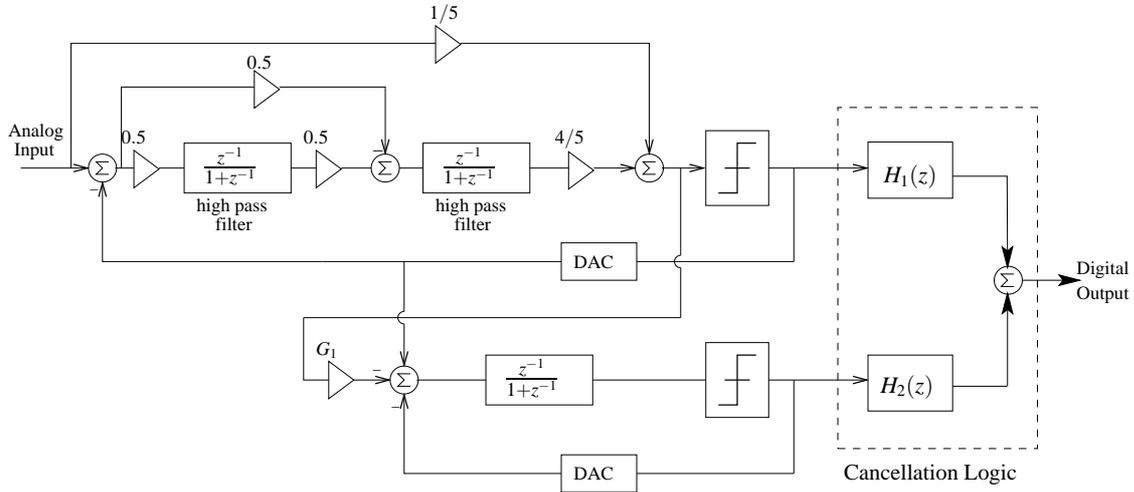


Figure 11: Architecture générique de la cascade de modulateur  $\Sigma\Delta$  HP basé sur la structure proposée

$G_1$  est l'estimation du gain de quantification du premier étage. Nous montrons que l'amélioration des performances peut être obtenue par une approximation plus précise et systématique du gain de quantification  $G_1$  comme l'illustré à la Fig. 12.

Le problème associé à des structures MASH, c'est qu'il faut qu'il y ait un bon appariement entre les filtres numériques et la NTF analogique. En cas de discordance, le SNDR se dégrade. Du point de vue de la fabrication, les filtres numériques sont assez précis alors qu'il ya un degré d'imprécision dans la mise en œuvre de la partie analogique. L'inexactitude des coefficients analogiques est une conséquence directe du désappariement des rapports des condensateurs dans le circuit. D'autres imperfections analogiques qui changent la NTF et STF des différents étages de MASH et par conséquent entraînent une fuite du bruit de quantification en raison de l'inadéquation des filtres numériques avec des circuits analogiques sont dus aux gain-DC fini, GBW fini et SR fini des amplificateurs. La correction adaptative numérique de ces erreurs analogique est une zone très étudiée. Cette calibration peut être effectuée hors ligne [18], en ligne [19, 20, 21, 22, 23] ou par injection de signal de test [24]. Toutes ces techniques sont au prix d'une augmentation de la complexité des circuits et de la consommation.

### L'architecture Generalized Multi Stage Close Loop

Le problème du désappariement entre les composants analogiques et les filtres numériques dans les structures traditionnelles de MASH en raison de nonidéaliétés a conduit à une nouvelle génération de structures MASH qui sont exemptes de filtres d'annulation du bruit de quantification. De cette façon, nous réduisons la complexité des circuits mais augmen-

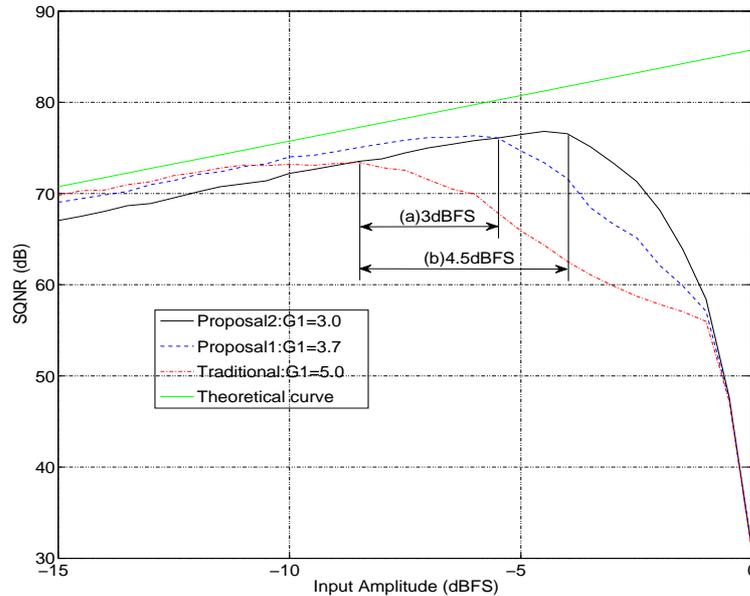


Figure 12: SNR en fonction du signal d'entrée pour trois cascade  $\Sigma\Delta$  PH modèles, (une augmentation) de la plage dynamique atteint par la proposition 1 de plus de l'architecture classique (b) Augmentation de la plage dynamique réalisé par Proposition 2 sur l'architecture classique

tons la robustesse du circuit en éliminant la sensibilité aux imperfections du circuit. La première architecture de cette nature est présentée dans [25]. Cette structure est appelée multi-stage closed loop (MSCL). Chaque étage de cette structure est un modulateur simple d'ordre un et une réaction globale est introduite à partir de la sortie, qui est la somme de la production de tous les comparateurs. Une version améliorée de cette structure est Generalized multi-stage closed loop (GMSCL). Il s'agit essentiellement d'une structure cascade 2-2, mise en œuvre à chaque étage comme une structure feedforward, et une réaction globale est utilisée à partir de la sortie comme le montre la Figure. 13.

Il est à noter que l'additionneur avant le premier étage de comparaison peut être réalisée passivement dans le GMSCL PH proposé et montré dans la Fig. 13, puisque les deux coefficients sont inférieurs à l'unité.

### L'architecture Generalized Multi Stage Close Loop avec Plage Dynamique Étendue

La structure de GMSCL HP proposée souffre des non-linéarités du CNA 2.5bit dans la boucle de rétroaction. Pour contrer ce problème, une technique récemment proposée [26] a été appliquée au modulateur. Elle évite l'utilisation coûteuse des techniques traditionnelles comme Dynamic Element Matching (DEM) et augmente la plage dynamique globale du modulateur. La technique consiste à utiliser un quantificateur linéaire (1 bit ou 1.5bits) dans la boucle principale, puis d'en extraire le bruit de quantification et en l'amenant à

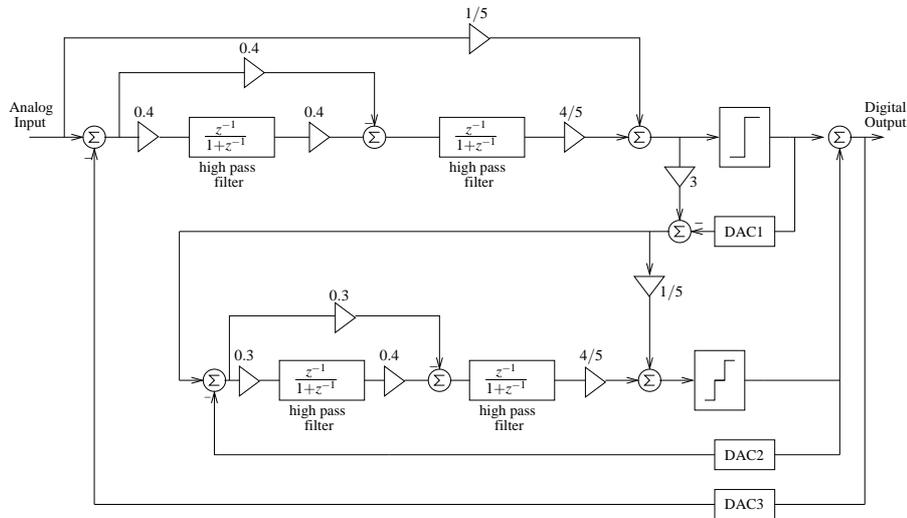


Figure 13: GMSC PH structure basée sur la structure proposée

un quantificateur auxiliaire multi-bits. Les sorties des deux quantificateurs principaux et auxiliaires sont renvoyées à la boucle via leur CNAs respectifs. La configuration qui en résulte est un modulateur de la Fig. 14.

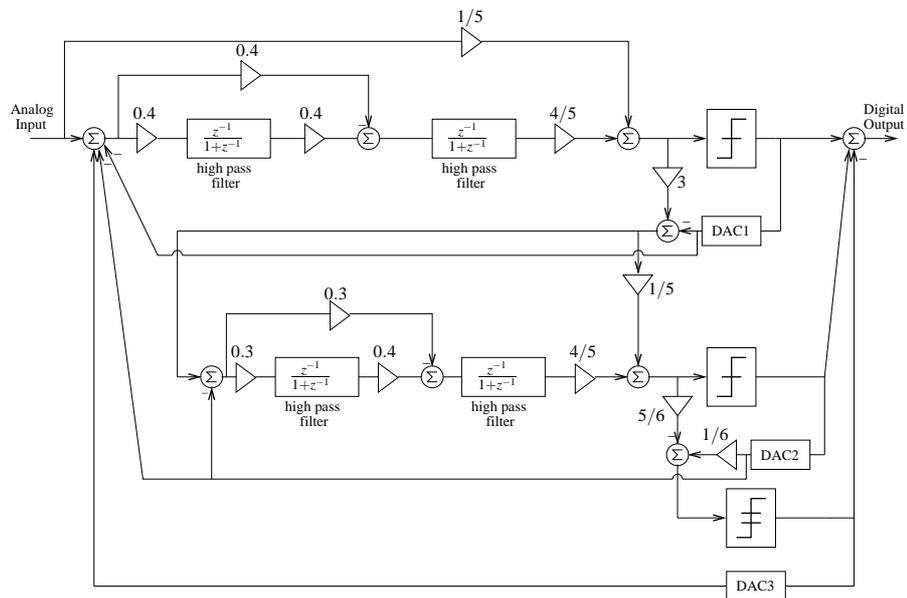


Figure 14: GMSC PH proposé avec DR étendu

Pour montrer l'efficacité de l'architecture proposée, des simulations comportementales ont été réalisées dans MATLAB. Pour comparer les architectures équivalentes, le quantificateur du deuxième étage de la topologie en Fig. 13 a été réalisé avec 5-niveaux de sortie et

il utilise quatre comparateurs. L'architecture proposée (Fig. 14) a un comparateur et un quantificateur auxiliaire 4-niveaux dans la deuxième étape et donc quatre comparateurs. La modélisation des non-linéarités du CNA de moyenne 0 et de variance 1% a été introduite dans ces deux structures. Le résultat de la simulation présentée à la Fig. 15 montre que la structure proposée fournit une performance 7dB meilleure que l'architecture traditionnelle du point de vue du SNR et 4dB d'amélioration de la performance du point de vue de la DR.

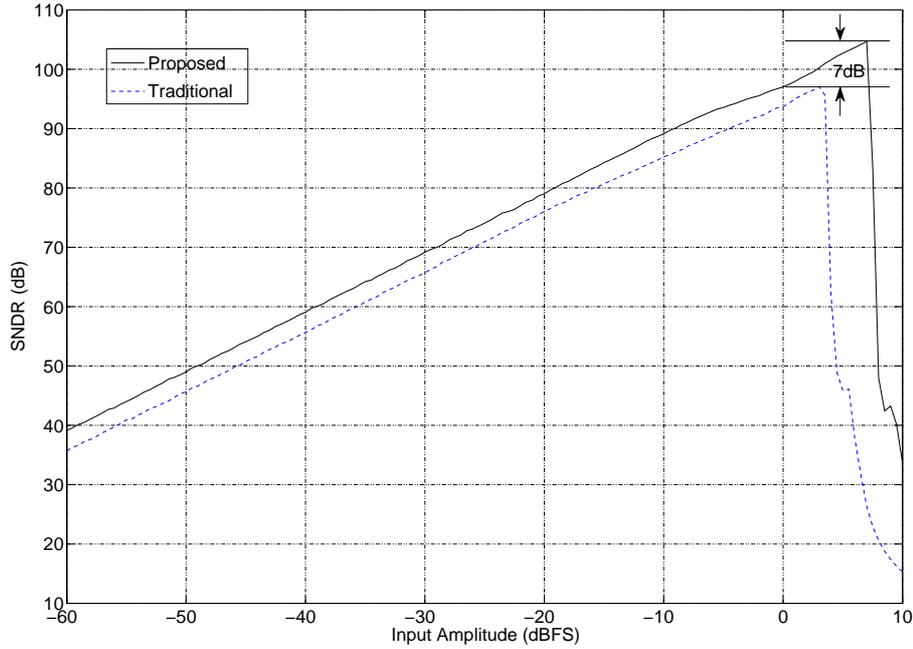


Figure 15: Comparaison des performances de deux structures GMSCl PH avec 1% non-linéarités du CNA

## L'implémentation du Filtre Passe-Haut

Le filtre passe-haut est une composante majeure de modulateur  $\Sigma\Delta$  PH. La fonction de transfert pour le filtre PH est réalisé en appliquant la transformation,  $z \rightarrow -z$ , à un intégrateur basé sur un circuit à capacités commutées:

$$H_{passe-bas}(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (7)$$

Il en résulte:

$$H_{PH}(z) = \frac{-z^{-1}}{1 + z^{-1}} \quad (8)$$

Ce filtre a un zéro à  $DC$  par opposition à un zéro à  $F_s/2$  pour l'intégrateur à capacités commutées. Il y a trois filtres PH dans l'état de l'art: filtre à base d'intégrateur, filtre à base de chopper et filtre amélioré.

### Le Filtre à Base d'Intégrateur

La première mise en œuvre du filtre PH illustrée dans la Fig. 16 a été présentée dans [27] pour l'implémentation du modulateur  $\Sigma\Delta$  passe-bande.

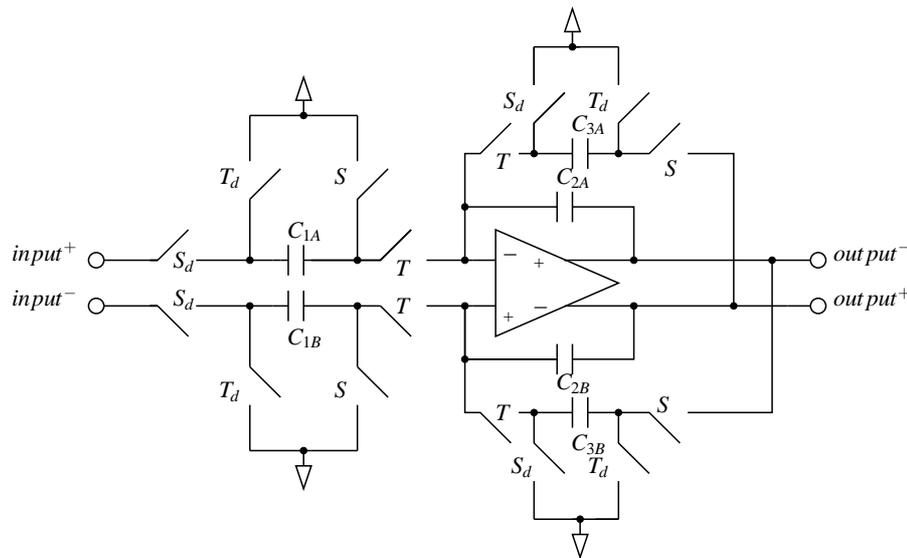


Figure 16: Filtre PH faite par une boucle de rétroaction autour de l'intégrateur

Il est conçu par l'introduction d'une boucle supplémentaire de feed-back autour de l'intégrateur, de telle sorte que la fonction de transfert pour le filtre HP est réalisé. Les problèmes associés à cette mise en œuvre comprennent une sensibilité accrue au bruit des ampli-op [28], une haute contribution du bruit thermique des interrupteurs, une grande superficie et une consommation d'énergie élevée.

### Le Filtre à Base de Chopper

La deuxième implémentation montrée dans la Fig. 17, est basée sur l'approche de la modulation du signal d'entrée pour le ramener en bande de base, puis le signal est intégré par l'intégrateur, et ensuite modulé pour remonter à la fréquence IF.

Toutefois, le traitement du signal se produit encore en bande de base au sein de l'intégrateur. Les avantages obtenus par le déplacement à IF sont perdues une fois que le signal est modulé vers la bande de base dans le domaine analogique, réintroduisant la nécessité d'utiliser les techniques dites de "chopper stabilization (SHC)" et "correlated double sampling (CDS)".

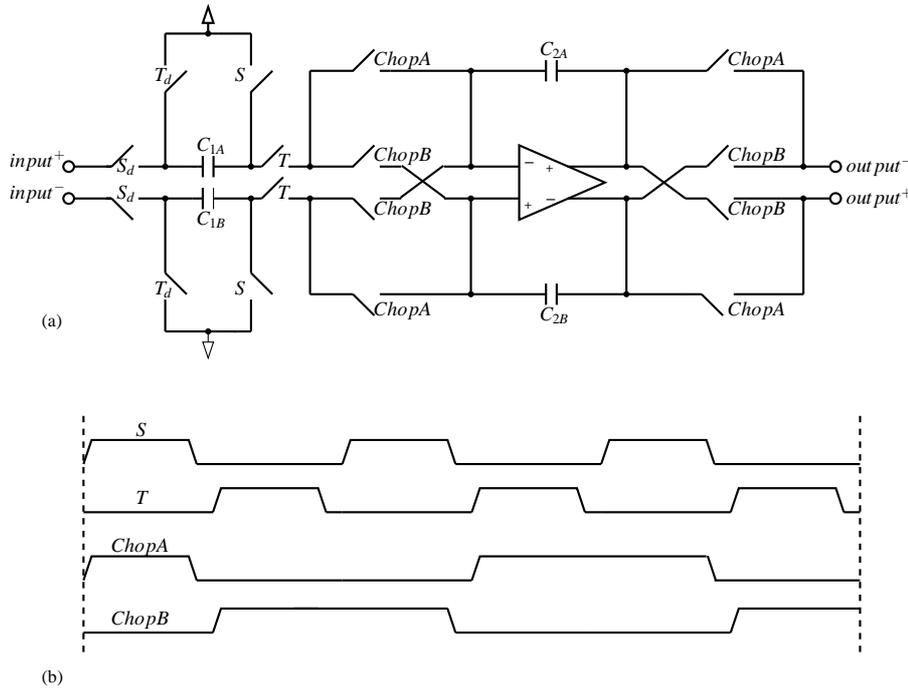


Figure 17: (a) Filtre PH fait en hachant l'entrée et la sortie du signal d'intégrateur, (b) Son chronogramme associé

## Le Filtre Amélioré

Une meilleure implémentation du filtre PH est proposée dans [29] et est représentée dans la Fig. 18. Cette mise en œuvre ne souffre pas des inconvénients des deux précédentes implémentations. L'opération de base est telle que la charge est échantillonnée sur  $C_{1A}$  au cours de la phase  $S$ . Sur la phase  $T$ , cette charge est transférée à  $C_{2A}$  pour les cycles d'horloge impairs et à  $C_{2B}$  sur des cycles d'horloge pairs.  $C_{1B}$  fonctionne d'une manière similaire.

Cette mise en œuvre est meilleure que le filtre à base d'intégrateur parce qu'il n'y a pas de boucle de rétroaction supplémentaire autour de l'intégrateur. Cela a des implications différentes avantageuses: elle prend beaucoup moins de superficie, il réduit la charge capacitive sur l'ampli-op et par conséquent la consommation d'énergie, il améliore les performances de bruit du filtre et il améliore la stabilité car elle ne dépend plus de l'appariement exact des condensateurs. Cette structure résout également le problème des bruits de basse fréquence associés à la structure à base de chopper, tout le traitement du signal est complété au niveau IF de fréquence, donc le DC-offset et le bruit  $1/f$  ne brulent plus le signal utile.



Paramètre	À Base d'Intégrateur	À Base de Chopper	Amélioré
Bruit Commutateur	$\frac{5kT}{C_s}$	$\frac{4kT}{C_s}$	$\frac{4kT}{C_s}$
Bruit Ampli-Op	$41 \times \frac{e^2_{amp1}}{F_s} \times B$	$17 \times \frac{e^2_{amp1}}{F_s} \times B$	$1 \times \frac{e^2_{amp1}}{F_s} \times B$
DC-Gain Fini	$\alpha = \frac{A_0}{A_0 + 3.5}$	$\alpha = \frac{A_0}{A_0 + 1.5}$	$\alpha = \frac{A_0}{A_0 + 1.5}$
GBW Fini	$\tau = \frac{3 + b}{2\pi GBW}$	$\tau = \frac{1 + b}{2\pi GBW}$	$\tau = \frac{1 + b}{2\pi GBW}$
Bruit de Scintillement	Non	Oui	Non
DC-Offset	Non	Oui	Non
Superficie	Elevée	Faible	Faible

Table 1: La performance de trois filtres PH en présence de bruit et de non-idéalités

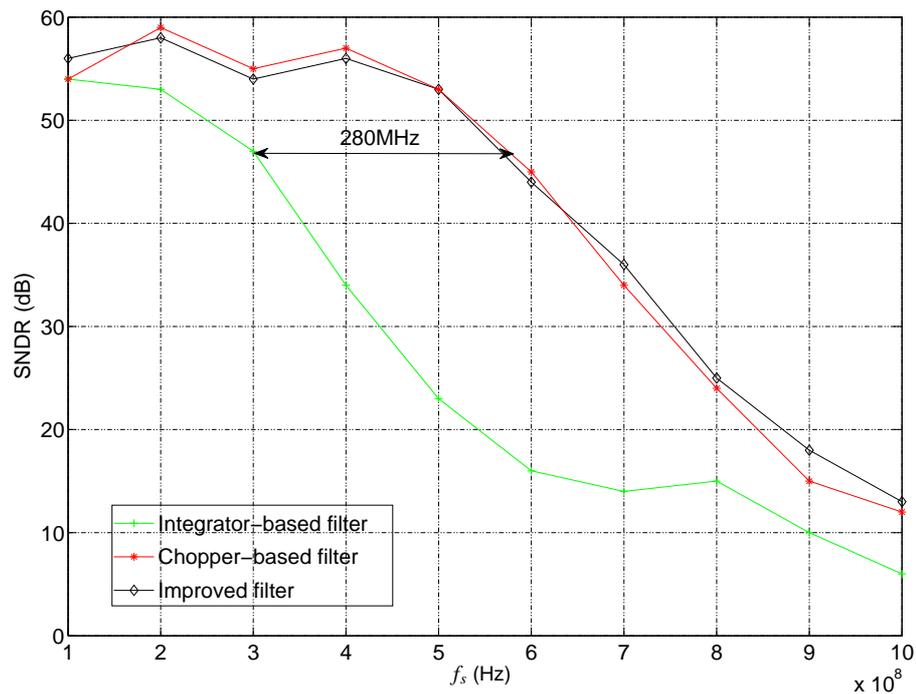


Figure 19: Performance du modulateur PH proposé en utilisant trois filtres PH à haute fréquence d'échantillonnage

une fréquence d'échantillonnage qui est supérieure à 280MHz par rapport à la fréquence d'échantillonnage la plus élevées possible pour le filtre à base d'intégrateur en utilisant la même ampli-op. En d'autres termes, à la même consommation d'énergie, le modulateur réalisé avec un filtre à base d'intégrateur peut convertir moins de bande passante que le modulateur construit avec les deux autres topologies de filtre.

Dans la deuxième expérience, nous prouvons la réjection excellente du bruit obtenu par le filtre amélioré par rapport aux deux autres topologies. Le bruit de l'amplificateur opérationnel ramené à l'entrée a été généré en MATLAB. Il est injecté dans le circuit en ajoutant une source de tension à chaque entrée de l'ampli-op. Les valeurs de cette source de tension sont lues à partir de MATLAB. Le circuit pour le modulateur PH proposé, construit avec la topologie de filtre amélioré, y compris les sources de bruit de l'ampli-op est illustré dans la Fig. 20.

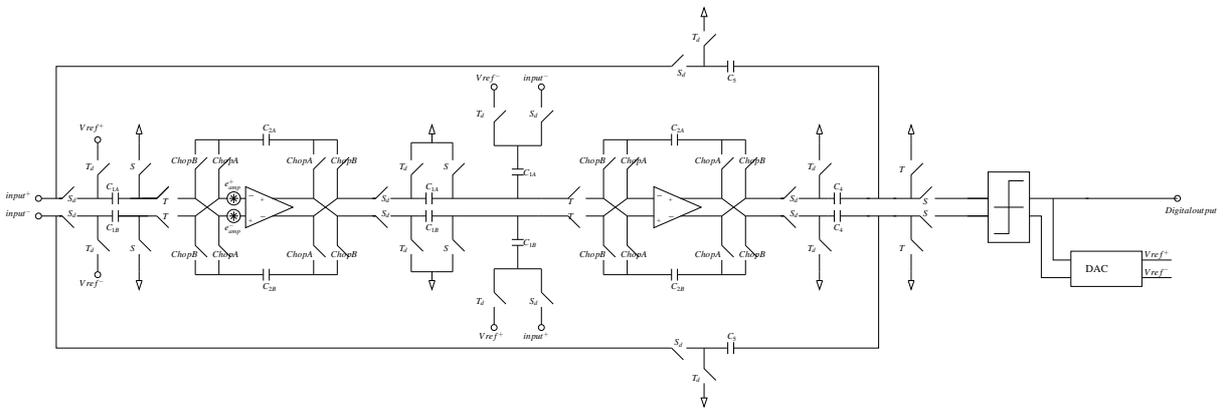


Figure 20: Injection de bruit dans le modulateur

$e_{amp}^+$  et  $e_{amp}^-$  sont les sources de bruit généré en MATLAB et lu directement dans SPECTRE. Le résultat de la simulation de l'injection du bruit dans les trois filtres est indiqué sur la Fig. 21.

Cette figure montre que le filtre à base d'intégrateur et le filtre amélioré réussissent à éviter le bruit de basse fréquence-bruit de scintillement, tandis que dans le filtre à base de chopper, le bruit de scintillement corrompt la bande du signal et en résulte la réduction de la SNR. Pour un OSR de 32, le filtre à base d'intégrateur, le filtre à base de chopper et le filtre amélioré donnent une SNDR de 55dB, 52dB et 21dB respectivement. Ainsi, 3dB de SNR est perdu à cause de la désavantageuse mise en forme du bruit d'ampli-op à haute fréquence dans la structure à base d'intégrateur et 30dB sont gaspillées en raison de la corruption du signal utile par le bruit à basse fréquence dans la structure à base de chopper. Ces caractéristiques font du filtre amélioré un choix idéal pour la grande vitesse et haute résolution à consommation réduite.

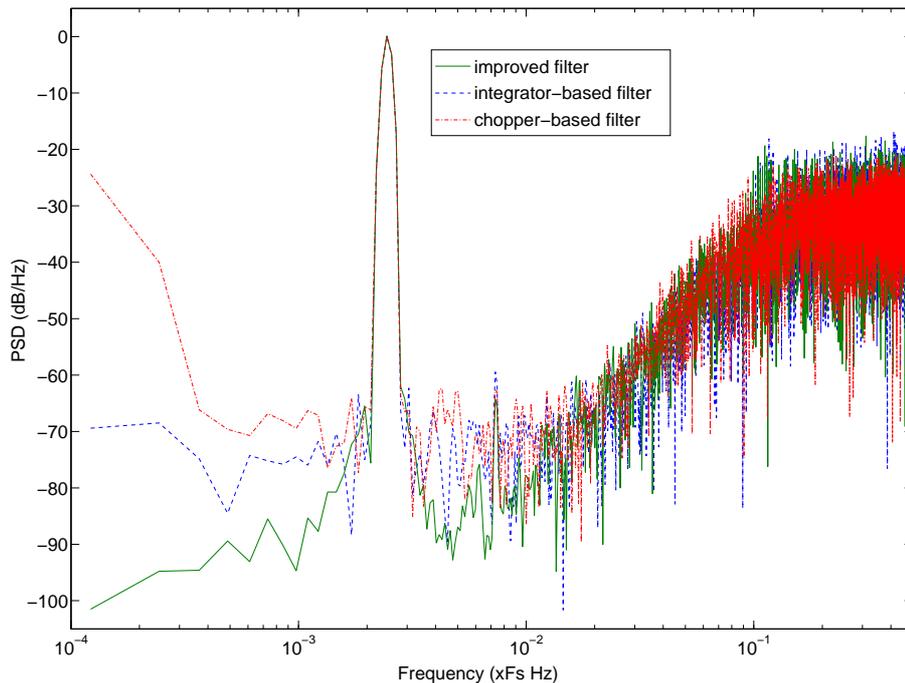


Figure 21: Spectre de sortie de modulateur en présence de bruit d'ampli-op pour les trois filtres

## La Conception en 65nm CMOS

Le CAN développé au niveau système dans les chapitres précédents a été conçu au niveau transistor en CMOS 65nm. Ce CAN est conçu pour satisfaire les exigences de performance des normes spécifiées dans le Tableau. :

Au vu de la diversité des exigences de performance, il devient évident que le CAN doit être reconfigurable. La reconfiguration est fournie par le changement de la fréquence d'échantillonnage ( $F_s$ ) et de l'ordre du modulateur ( $M$ ). Dans le mode GSM/EDGE, puisque la bande passante du signal est faible, une  $F_s$  de 28.57MHz ( $OSR = \frac{28.57MHz}{2 \times 135KHz} \approx 105$ ) et une mise en forme du 2ème ordre du bruit avec un seul bit de quantification sont utilisés. Ainsi, le deuxième étage de la structure GMSCL PH est désactivée dans le mode GSM/EDGE pour réduire la consommation. Pour le mode de fonctionnement UMTS/WLAN, la fréquence d'échantillonnage est élevée à 228.57MHz et l'ordre du modulateur est porté à 4, avec un étage supplémentaire de quantificateur auxiliaire.

## Le Schéma Global du Circuit

Le schéma du modulateur en mode GSM est présenté dans sa version non différentielle pour plus de simplicité dans la Fig. 22. Le commutateur d'entrée du modulateur est de type "bootstrap" pour satisfaire les exigences de linéarité. Les autres commutateurs sont des commutateurs CMOS. La capacité d'échantillonnage à l'entrée du modulateur est choisie

Standard	GSM/EDGE	UMTS	WLAN
Taux de conversion	270KHz	3.84MHz	25MHz
Bande passante du signal	135kHz	1.92MHz	12.5MHz
Fréquence d'échantillonnage ( $F_s$ )	28.57MHz	228.57MHz	228.57MHz
Ordre du Modulateur ( $P$ )	2	4+aux. quantizer	4+aux. quantizer
SNR	80dB	80dB	52dB

Table 2: ADC Spécification

égale à  $600fF$  pour répondre aux spécifications de bruit thermique.

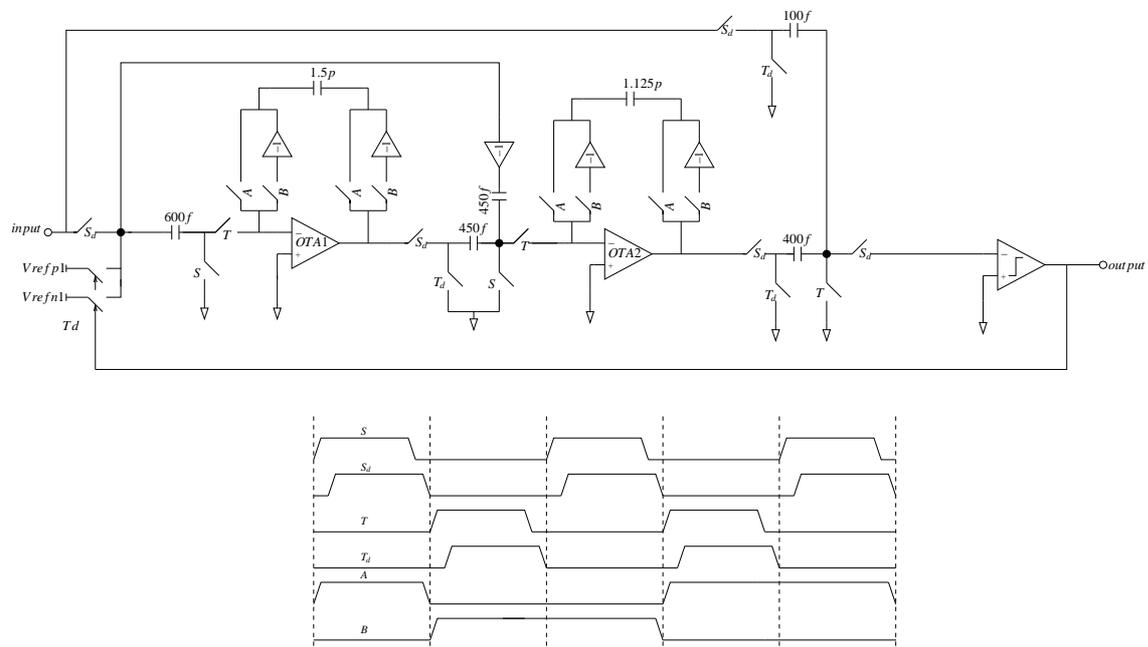


Figure 22: Modulateur global non différentiel en mode GSM avec son chronogramme associé

Le modulateur utilisé est du 2ème ordre avec l'architecture proposée et un quantificateur 1 bit. Ce modulateur fournit les performances nécessaires de SNDR pour un OSR de 84. La taille des condensateurs diminue avec le flux de signal en raison de l'augmentation de la mise en forme du bruit.

Le schéma du modulateur non différentiel en mode ULAN est présenté sur la Fig. 23. Il utilise la structure proposée-GMSCL PH avec une dynamique améliorée par l'ajout d'un quantificateur auxiliaire dans le dernier étage comme décrit précédemment.

La mise en œuvre au niveau transistor d'un CAN multi-mode fonctionnant sur le principe du modulation  $\Sigma\Delta$  passe-haut est présenté. Le CAN a deux modes de fonc-

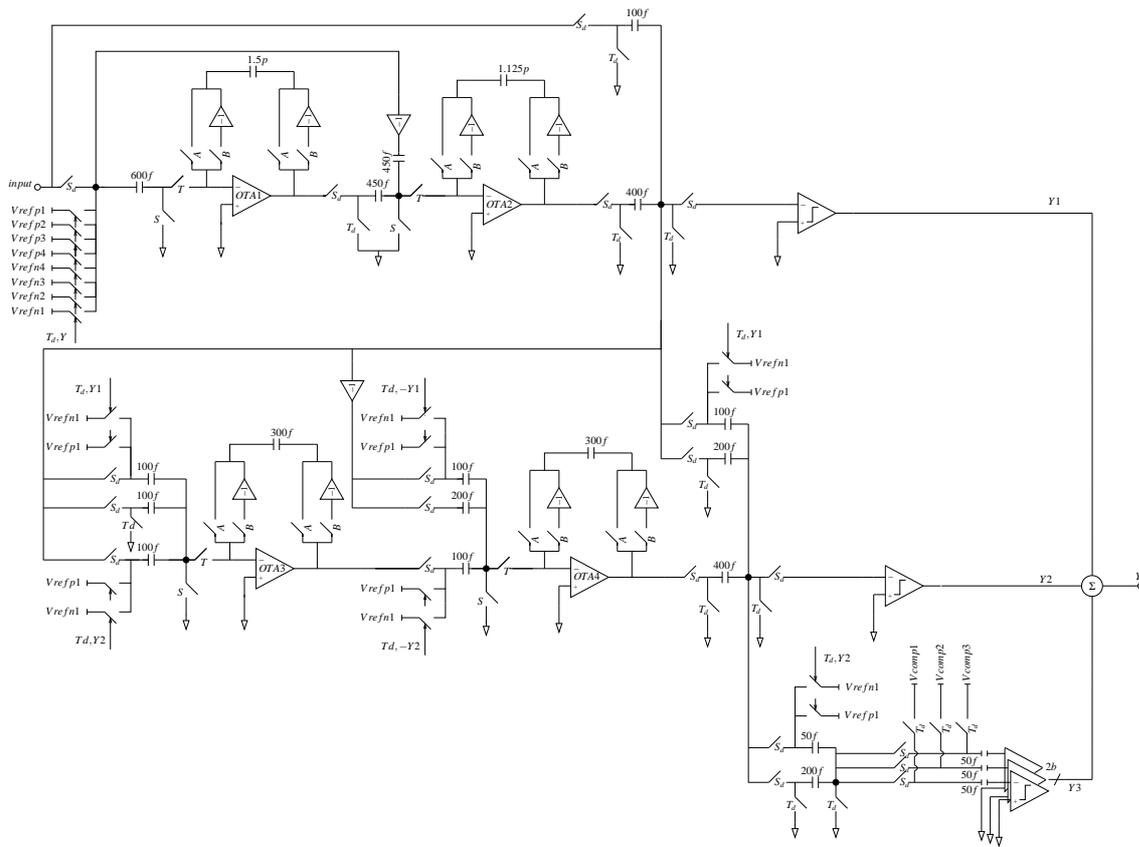


Figure 23: Modulateur global non différentiel en mode UMTS/WLAN

tionnement: GSM/EDGE et UMTS/WLAN. Cette reconfiguration permet une économie d'énergie significative.

## Les Résultats de Simulations

La simulation électrique avec des OTA (et le circuit CMFB), quantificateur et CNA implementés au niveau transistor est effectuée avec succès pour le mode GSM. Le spectre de sortie à l'entrée pleine échelle est illustré dans la Fig. 24. Comme présenté dans la figure, la résolution de 80-dB est atteinte à l'OSR minimum de 84 et de la fréquence d'échantillonnage de 28.57MHz.

Pour les modes UMTS/WiFi de fonctionnement, une distorsion importante est observée dans la bande du signal. Le résultat de la simulation propre de ces modes est prévu dans une extension éventuelle de ce travail de recherche.

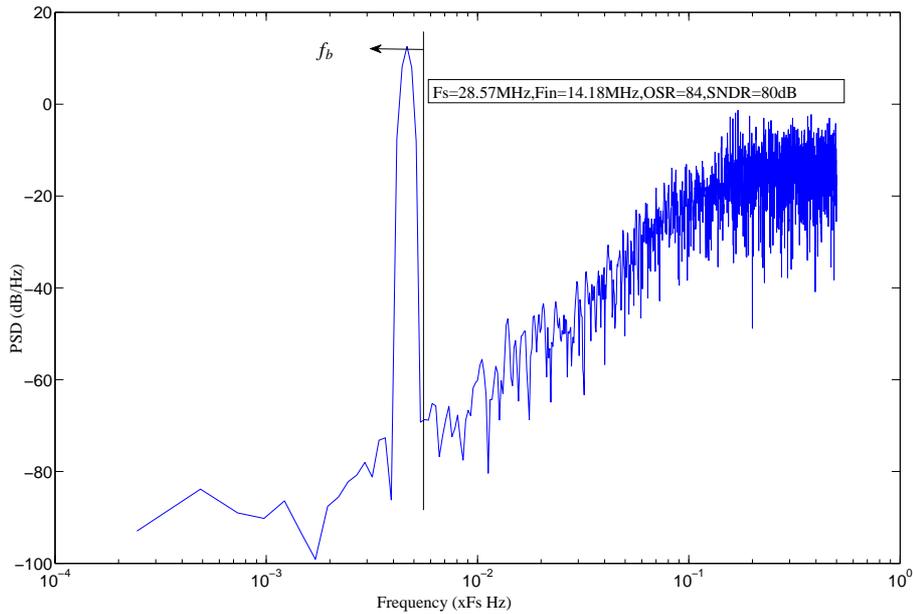


Figure 24: Résultat de simulation en mode GSM

## Conclusion

La première partie de cette thèse a présenté les architectures de récepteur radio pour les systèmes de communication sans fil d'aujourd'hui du point de vue de la reconfiguration, intégrabilité et consommation d'énergie. Un pas en avant important vers la mise en œuvre de la notion de SDR sont les récepteurs d'échantillonnage RF qui utilisent le sous-échantillonnage pour réduire la fréquence de signal de RF à IF. De cette façon, le traitement du signal en temps discret, qui est fortement intégrable, est introduit dès le début. En utilisant le sous-échantillonnage, les exigences de vitesse sur les blocs suivants sont assouplies. Le défi dans ce scénario est le filtrage anti-repliements pour minimiser la corruption du signal par des brouilleurs en-bande et hors-bande. Ceci est accompli par des filtres à capacités commutées passifs. L'état de l'art des récepteurs utilise une downconversion en deux étapes, chaque étape à l'aide de sous-échantillonnage, afin de parvenir à un compromis acceptable entre la fréquence du signal abaissée en fréquence et le filtrage anti-repliement. Bien que, avec l'augmentation des performances des CAN, il est devenu possible d'utiliser la "downconversion" en une seule étape pour diminuer le nombre de composants. Le sous-échantillonnage est réalisé de telle manière que le signal est placé à  $F_s/2$  pour profiter des avantages des deux: zéro-IF et low-IF. Dans ce scénario, le candidat naturel pour le CAN est le modulateur  $\Sigma\Delta$  PH.

La deuxième partie de cette thèse a examiné l'état de l'art des modulateurs  $\Sigma\Delta$ . Commencant par des architectures classiques feed-back, ensuite les récentes architectures feed-forward sont discutés avec leurs avantages et leur inconvénients. Les modulateurs d'ordre supérieur à boucle unique et modulateurs en plusieurs étages, qui sont inévitables pour des applications nécessitant une haute résolution, sont également exposés. La modélisation au

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niveau du système du modulateur classique: Boser second ordre [12] est effectuée afin de démontrer les exigences relatives pour les ampli-op dans cette topologie.

La troisième partie est liée à l'étude du modulateur  $\Sigma\Delta$  PH. Ce dernier rejette le bruit de quantification en basse fréquence. La bande du signal est située à environ la moitié de la fréquence d'échantillonnage, il est donc compatible avec le récepteur  $F_s/2$  IF en temps discret et, en outre, totalement à l'abri des DC-offsets et du bruit de scintillement. Diverses topologies existantes de modulateur  $\Sigma\Delta$  passe-bas sont présentées après leur adaptation au fonctionnement PH, et une nouvelle architecture du second ordre ayant une STF unitaire est proposée. Elle soulage les problèmes liés à l'architecture traditionnelle feedforward en supprimant la nécessité d'un additionneur actif. Une nouvelle technique pour concevoir des structures en cascade ou MASH est également proposée ce qui augmente la dynamique en entrée du modulateur. Cette technique est basée sur l'étude systématique du gain de quantification du premier étage et l'adaptation de filtres numériques avec ce gain. Un état de l'art des architectures des modulateurs  $\Sigma\Delta$  multi-étages, ce qui est libre de filtres numériques d'annulation, appelé Generalized-Multi-Stage-Closed-Loop (GMSCL) est conçu pour un fonctionnement PH. Enfin, un quantificateur auxiliaire est ajouté dans le deuxième étage, afin d'augmenter la gamme dynamique en entrée et de diminuer l'effet des non-linéarités du CAN global. Une comparaison entre les modulateurs  $\Sigma\Delta$  PH et passe-bas est également réalisée. Elle révèle que les modulateurs PH sont plus sensibles à la gigue d'horloge ce qui augmente les contraintes sur le circuit de génération d'horloge. Les modulateurs passe-bas d'autre part sont de plus en plus sensibles à l'hystérésis dans le comparateur nécessitant un plan pour réduire les exigences sur le comparateur.

La quatrième partie de ce travail de recherche visait à sélectionner la meilleure architecture du filtre PH qui est l'élément de base de modulateur  $\Sigma\Delta$  PH. Après une analyse comparative approfondie des trois topologies en compétition, celle qui a été introduite récemment et basée sur l'alternance des condensateurs est sélectionnée. Ses avantages de réduction de la consommation et du bruit sont prouvés analytiquement et par simulations.

Enfin, une implementation multi-standard, multi-mode d'un CAN en CMOS 65nm est présentée. Il a trois modes de fonctionnement: GSM, UMTS et WiFi/WiMax. En mode GSM, le modulateur  $\Sigma\Delta$  PH de second ordre proposé est utilisé, tandis que pour l'UMTS et le WiFi/WiMax le modulateur GMSCL PH du quatrième ordre avec un quantificateur auxiliaire est utilisé pour la conversion.

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# Chapter 1

## Introduction

### 1.1 Motivation and Goals

The proliferation of wireless standards and the diminution of radio-terminals' size at the same time is pushing towards the materialization of newly created concept of software defined radio (SDR). This communication system is expected to realise multiband, multimode radio terminals by defining radio functionality in software [1]. This way, the radio terminal is adapted to different protocols and customized for diverse services by just reprogramming the radio functionality.

This, however, makes the RF-receiver design a challenging task. In an ideal SDR, the solution for increasing both the receiver integration and reconfigurability is provided by transferring the analog-to-digital-conversion interface from the baseband to RF i-e just after the antenna. The inherent advantage of this scheme is that the digital signal processing eliminates the non-idealities associated with analog signal processing i-e device noise and non-linearities, components mismatch etc. The evolution of CMOS technologies towards smaller transistor feature sizes also favours an increased level of digital signal processing in receiver implementation [2].

Nowadays the DSP can operate at a very high frequency and can thus process high frequency signals. The boundary between the RF front-end and the digital baseband is moved to higher frequency, but not yet at RF frequency. The major bottleneck is the design of analog-to-digital-converter (ADC) which can convert the signal at high frequencies. With the current CMOS technologies, it is practically not possible to design an ADC which converts the signal directly at RF.

However, the processing has to be carried out as much as possible in digital due to the low costs, reconfigurability possibility and stability. To go forward in this direction, sub-sampling receiver was proposed. The RF signal is sub-sampled as soon as possible. The frequency downconversion is carried out by the sub-sampler with discrete-time signal processing. One special case of RF receiver which uses discrete-time subsampling is  $F_s/2$  IF receiver [3, 4]. This architecture downscales the frequency from RF to an IF of  $F_s/2$  (one-half of the sampling frequency), thereby making High-Pass (HP)  $\Delta\Sigma$  modulator the natural choice for ADC. This ADC is of much reduced complexity as compared to Band-

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Pass (BP)  $\Delta\Sigma$  modulator.

Besides the advantage of converting directly at IF, HP  $\Delta\Sigma$  modulator has the potential to efficiently eliminate the dc-offsets and low-frequency noises like flicker noise [5, 6, 7] which are a source of concern in traditional LP  $\Delta\Sigma$  modulators. This feature is particularly interesting for time-interleaved  $\Delta\Sigma$  converters where the channel-offset is sufficiently removed by HP operation [8], and a simple digital channel equalization technique would minimize effectively the channel gain mismatch effect [30].

In spite of these potential advantages, the concept of HP  $\Delta\Sigma$  modulation has not received much attention, mostly due to its difficult implementation and the uncertainty about its stability and performance in the presence of circuit nonidealities. The basic hindrance block has been the implementation of high pass filter, which is analogous to an integrator in LP  $\Delta\Sigma$  modulator. The traditional implementation involves a feedback loop around an integrator and is an expensive solution because of increased power consumption and surface area. However, recently a new architecture of HP filter has been proposed, which gets rid of the drawbacks of the traditional one and hence propels a renewed interest in HP  $\Delta\Sigma$  modulators.

Keeping in view its potentials, this thesis is focused on HP  $\Delta\Sigma$  modulator in general and its application to multi-mode wireless receivers in particular. Our objectives consist of studying its principle, its performance and stability and comparing it to LP modulators on one hand and applying it to achieve multi-modal wireless receiver functionality on the other.

To achieve these objectives, a new unity signal-transfer-function (STF) single-loop HP  $\Delta\Sigma$  modulator architecture has been proposed. It is then used to construct a HP generalized-multi-stage-closed-loop (GMSCL) architecture. The proposed HP unity-STF single-loop modulator provides the specifications of EDGE/GSM standard, while the HP GMSCL structure is used for UMTS/WLAN standards.

## 1.2 Organization

We use a top-down approach to present our work. Beginning with the radio receiver architecture in Chapter 2, we explain the newly created concept of  $F_s/2$  receiver and compare it with other state of the art receiver architectures i.e zero-IF and low-IF receivers.

After having chosen the receiver topology, we move on to the next level of design i.e  $\Delta\Sigma$  modulator architecture. For this we embark on a detailed state-of-the-art study on LP  $\Delta\Sigma$  modulators in Chapter 3. This includes various second-order topologies, higher-order single-loop structures and MASH structures. We also discuss the latest generation of MASH structures which are free from digital cancellation filters and thus do not require digital calibration techniques to counter the mismatches between analog and digital components. Multi-stage closed loop (MSCL) is one of these structures and its enhanced version is Generalized multi stage closed loop (GMSCL) [15, 16]. This follows by a system-level modeling of various circuit level parameters of traditional second-order structure called Boser structure. This study provides us with specifications for transistor level design.

In Chapter 4, the problems associated with LP modulators are identified, leading to

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their natural solution: HP modulators. The principle of HP modulation is exposed followed by various second-order topologies. We propose a new second-order feedforward architecture which is advantageous over contemporary topologies in terms of complexity and performance. Behavioral modeling of the proposed structure's circuit-level parameters is carried out, which furnishes us with its specifications. These specifications are then compared with other second-order topologies. We, then present cascaded or MASH structures for high-pass operation and propose a novel technique to improve the traditional MASH topologies in terms of input dynamic range and highest-achieved SNR. The proposed single-stage second-order topology is used as an individual stage of this new cascade structure. GMSCL is adopted for high-pass operation and its structure is modified to extract more SNR out of it. Finally a recently proposed technique is applied on the quantizer to increase the dynamic range of the converter and to eliminate the need of Dynamic Element Matching (DEM) by diminishing DAC non-linearities. This technique consists of employing an auxiliary quantizer to process the quantization error of the main quantizer.

The next level of design is the conception of a suitable switched-capacitor HP filter for HP  $\Delta\Sigma$  modulator, which is the subject of Chapter 5. We study and analyse three different types of switched-capacitor implementations of HP filter and compare them on the basis of consumption, noise immunity and speed and finally select the best one which has a performance comparable to that of switched-capacitor integrator.

In Chapter 6, we present the transistor level design of a reconfigurable multi-mode ADC in 65nm 2P7M CMOS process which uses the HP  $\Delta\Sigma$  architectures proposed in the preceding chapters. Much attention is given to the design of operational transconductance amplifier since it is the major building block of high pass filters and is the most power consuming element. Alongwith the design of OTA, comparator, DAC and passive adder's design is also detailed. Finally in Chapter 7, we present the perspectives and future research directions.

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## Chapter 2

# RF Receiver Architecture

### 2.1 Introduction

When designing an ADC, it has to be kept in mind that it will be used in what type of RF front-end receiver architecture. Thus the ADC techniques change in accordance with the overall receiver topology. RF front-end receiver is currently defined as the chain of elements from antenna to the ADC. This chain consists of various devices and circuits working at radio frequency band (RF), intermediate frequency band (IF) and analog baseband. ADC is often considered as the boundary between the RF and digital parts of the receiver, but with the advancements in ADCs design which are running at higher and higher sampling rates with each new technology, the ADCs and the associated digital signal processors can now be labelled as IF or even RF devices. Under these circumstances, ADCs and some portion of digital signal processing will soon become a part of RF front-end receiver. Radio receiver architecture choice is driven by many factors, including integration capability, reconfigurability, cost, performance etc. At present, most commercial implementations of RF transceivers are using superheterodyne architecture because of its superior performance compared to other topologies. But the recent advancements in CMOS technologies and integrability of more and more components have triggered interest in the more recent receiver architectures like direct conversion receiver (or zero-IF receiver or homodyne receiver) and low-IF receivers. Direct conversion receiver achieves great cost saving by removing completely the IF portion and providing the gain in baseband section of the receiver which is completely integrable. Multimode operation is also easily supported by direct-conversion receiver without any component addition. The problems inherent in zero-IF receiver have led to the creation of a modified structure called low-IF structure. The wireless receivers based on CMOS technologies have a preference for low-IF architecture because it gets rid of the problems of dc-offset and flicker noise which are serious in CMOS circuits. The latest evolution in the field of wireless receiver design is IF bandpass sampling receiver which uses the principle of subsampling to bring down the RF signal to IF by voluntary aliasing. The factor behind the success of this receiver is the enhancement of the sampling rate and resolution of the ADCs with an acceptable power consumption. This receiver be considered as another step towards the realization of the concept of software

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radio. An interesting class of this receiver structure is  $F_s/2$  IF receiver which combines the advantages of both direct-conversion and low-IF receivers. In this chapter, the various reception schemes are discussed in order of their arrival in the wireless arena i-e Superheterodyne receiver, Digital-IF receiver, Direct Conversion receiver, Low-IF receiver, IF Bandpass sampling receiver and its application to the  $F_s/2$  IF receiver. Special attention is paid to the suitability of these schemes to the  $\Delta\Sigma$  modulators in general and high-pass  $\Delta\Sigma$  modulators in particular.

## 2.2 Superheterodyne Receiver

The superheterodyne architecture is the classical and the most common receiver topology which appeared in 1910s. It consists of mixing an incoming signal with an offset frequency local oscillator (LO) at more than one point in the receiver chain to bring down the signal from RF to multiple IF stages. The most common superheterodyne structure in today's radio receivers consists of two-stage downconversion i-e two IFs. The reason for using two-stage downconversion is that it achieves an acceptable compromise between image rejection and adjacent channel suppression [31]. Fig. 2.1 shows a simple two-stage down-conversion superheterodyne architecture.

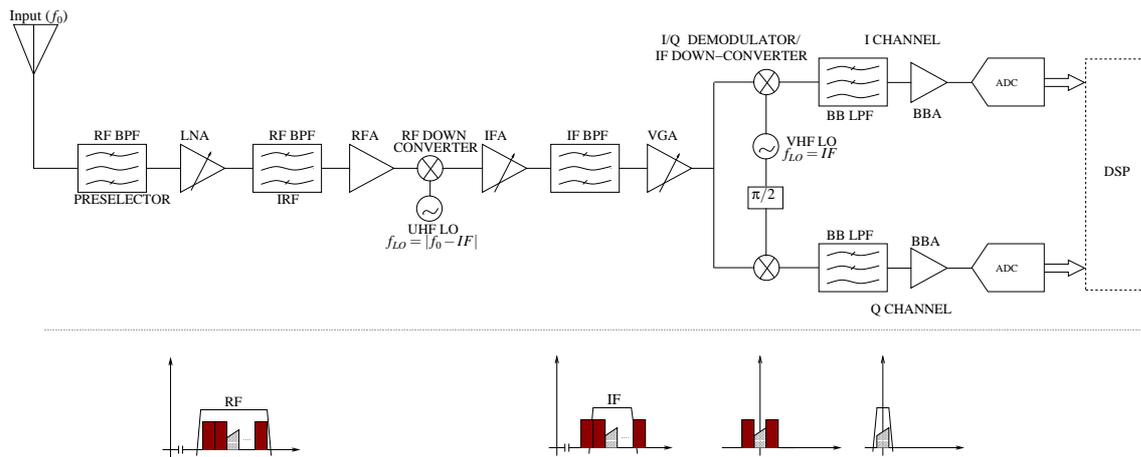


Figure 2.1: Superheterodyne receiver architecture and signal flow

The signal flow through its different building blocks can be explained as following: First of all, the out of band blockers are attenuated by the RF bandpass filter, thus it has to be designed separately for each standard. Moreover, it is an off-chip device thus posing a problem for complete receiver integration. The signal is then amplified by an LNA, which must have a sufficiently low noise so as not to corrupt the useful weak signals and at the same time it must have enough dynamic range to handle the inband interferers. The unwanted signals are still present at the image frequency since the RF bandpass filter is usually incapable of attenuating them to the system noise level, therefore an image reject filter is used before the mixer to diminish these images. As a design technique, the first

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intermediate frequency must be chosen relatively high so that the image is sufficiently far away from the signal. This results in reduced constraints on the image reject filter and allows effective filtering. The next device in the chain is a mixer whose function is to bring down the signal from RF to a relatively high IF. The mixer must handle the complete dynamic range of the input signal. After the mixer, the signal passes through yet another band pass filter to achieve the channel filtering. Like the previous band pass filters, this filter is implemented as an off chip surface acoustic wave (SAW) filter accompanied by a high in-band loss. The output drive of the mixer must therefore boost the signal level to compensate for this loss. The signal is then reduced to baseband by another mixer. The operation of channel selection has been shared by bandpass filters at two IFs in the system with the penalty of increased dynamic range in the second mixer. Now that the signal is clean from images and interferers, it is amplified to be finally fed to the ADC. The major disadvantage of this receiver architecture is the use of external filters which render it difficult for integration. Moreover, the filters are usually single ended and hence achieving good isolation between pins becomes necessary to reduce interference between them. To circumvent the problem of external filters, image-reject architectures have been proposed [32, 33] but they are unable to give good performance because of gain and phase mismatches resulting in imperfect image suppression. Because of its inherent problems, Superheterodyne architecture is no more the preferred choice of the designers for wireless communication systems. Both high-pass and low-pass  $\Delta\Sigma$  modulators can be used with this receiver architecture depending on the value of second intermediate frequency. If it is equal to zero, then low pass modulator has to be used; and if it is equal to  $f_s/2$ , then high-pass modulator has to be employed for ADC operation. If the IF is something between zero and  $f_s/2$ , then bandpass modulator is the only choice which is an expensive solution.

## 2.3 Digital-IF Receiver

An interesting modification of superheterodyne structure is digital-IF structure. The idea behind this architecture is to transfer the IF-block signal processing from analog to digital domain. As shown in Fig. 2.2, the incoming signal is digitized after being down-converted from RF to IF and hence the rest of the signal processing, for example second set of mixing and filtering is performed in the digital domain. After digitization, the signal is mixed with the quadrature phases of a digital sinusoid, and low-pass filtered to yield the quadrature baseband signals. The major advantage of this approach is that the digital processing avoids the problem of I and Q mismatch.

The hindrance block in this signal flow is the performance requirements on the ADC. The signal level attacking the ADC is very weak in this design, so it is a tough task to design the ADC which keeps the quantization and thermal noise levels below the signal level. Secondly, since the IF bandpass filter alone cannot sufficiently filter the adjacent interferers, the nonlinearity of the ADC has to be kept so small that the corruption of the signal by intermodulation products is minimized. In addition, the ADC needs to have high dynamic range to cater for signal level variations due to path loss and multipath fading. Another constraint on ADC is that it must support an input bandwidth which is at least

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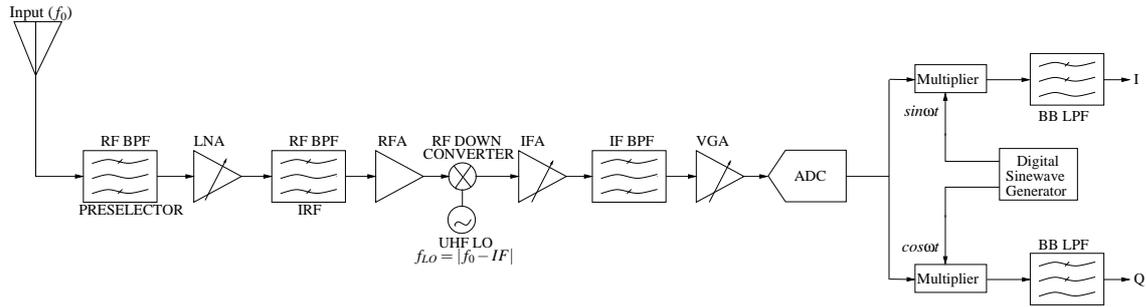


Figure 2.2: Digital-IF receiver

equal to the value of IF while maintaining an acceptable figure of merit. To alleviate these problems partially, the idea of subsampling in the sample and hold circuit of the ADC is introduced. This reduces the input bandwidth requirement of the ADC and hence the power consumption. The potential of the Digital-IF and Sampling-IF has made them the subject of active research [34, 35, 36].

## 2.4 Direct Conversion Receiver

Direct conversion receiver gets its name because it downconverts the signal directly from RF to baseband without using any intermediate frequency stages. It is also known with the names of zero-IF receiver or homodyne receiver. It was invented many decades ago, but always remained unsuccessful because of the problems that could not be resolved due to its discrete implementations. In the 90s it again came to limelight, because of several reasons: Its potential to be integrated in advanced cmos technologies because of reduced RF element count and technical homogeneity [37], elimination of image related problems encountered in superheterodyne receivers because in homodyne receiver the signal is its own image and thus is not troublesome.

The direct conversion receiver architecture is shown in Fig. 2.3. An RF bandpass filter placed at the input is the only off-chip element in this receiver. The LNA must handle the same dynamic range as for the superheterodyne receiver and it must boost the weak signals above the noise floor injected by the mixer. The mixer modulates the signal directly to baseband. The quadrature I and Q channels have to be separated necessarily at this point for typical phase and frequency modulated signals in this receiver architecture; the reason is that the two sidebands of the RF spectrum contain different information and result in indistinguishable mixture if they overlap with each other without being separated out in two phases. Only one local-oscillator frequency needs to be synthesized rendering the frequency planning a straightforward task. Since the IF is zero, the signal is its own image and hence the need for expensive image reject filters is avoided. The only filtering required is channel filtering which is carried out by active low-pass filters as opposed to passive IF filters (SAW filters) in superheterodyne receiver. These active filters are easily amenable to monolithic integration resulting in the reduced cost and size of overall transceiver. Another advantage of using active low-pass filters is that their bandwidth can

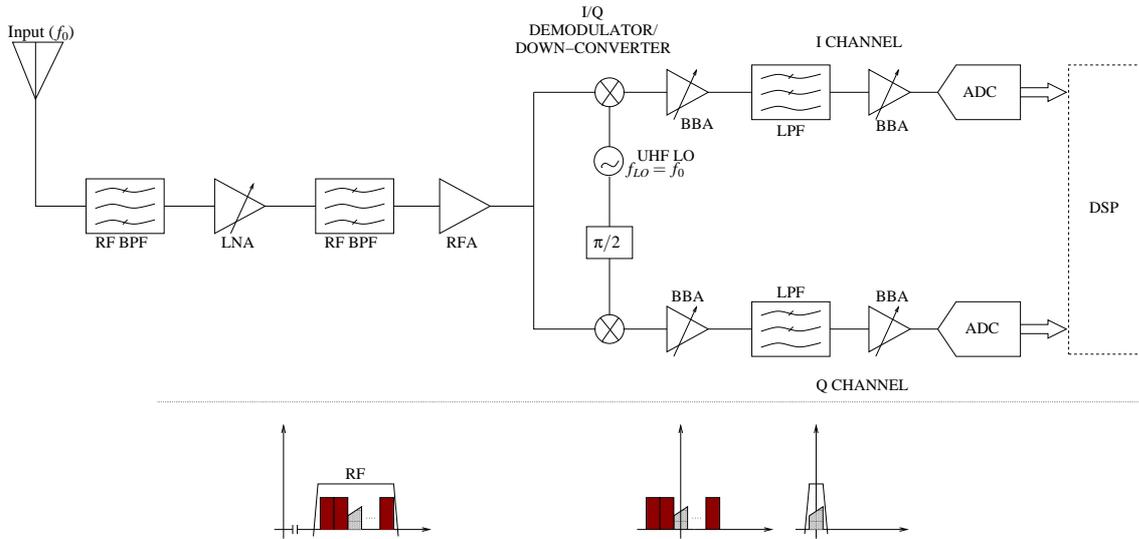


Figure 2.3: Direct conversion receiver architecture and signal flow

be designed as adjustable. This makes the receiver reconfigurable and a good candidate for multimode operation. It is important to note that reconfiguration is achieved with a common adjustable analog baseband circuitry without using a dedicated filter for each standard. With all these advantages, direct conversion receiver is still considered problematic because of the issues involved in its implementation. The major hindrances are dc-offset (specially time-varying), I/Q mismatch and flicker noise. DC-offsets are mainly injected into the signal while performing the operation of mixing. These are generated by imperfections in the mixer. Since they are implicitly in-band, it is difficult to filter them from the wanted signal. In this case, it becomes necessary to keep their value sufficiently below the useful signal to achieve the required signal to noise ratio. Unfortunately, the amplification provided by LNA is not enough for this purpose and is limited by the level of in-band interferers. Thus the dc-offset can be much greater in magnitude than the desired baseband signal. Many sources contribute to the generation of these offsets. Imbalance in the two mixers leads to a dc signal. Leakage signal from the local oscillator to the input of the mixer or the input of the LNA also results in dc offsets. This process is known as self-mixing. These two dc-offsets are generally invariable with time and can be cancelled with suitable circuitry. Time variable self-mixing is much more complicated to handle. This situation arises when LO signal leaks to the antenna, it radiates this signal into the environment and consequently this signal comes back to the receiver after being reflected from the moving objects. Since the input signal changes with time, the dc-offset generated also changes with time. Nonlinearities in the mixer may also cause moving dc-signal due to other interferers. This necessitates an adaptive offset cancellation scheme [31]. I/Q imbalance is other associated problem due to quadrature down-conversion in these receivers. Since the down-converted signal resides near zero frequency, flicker noise or  $1/f$  noise of devices is also of serious concern in the back-end blocks. In these type of

receivers, even-order distortion also becomes an issue. These problems have limited this architecture to use within a limited set of applications [38, 39, 40]. For direct conversion receivers, low-pass modulator is the only choice for ADC since the signal occupies baseband. Like direct-conversion receiver, low-pass ADC also suffers from dc-offsets and flicker noise destroying the useful signal. Special and expensive techniques have to be used to reduce the harmful effect of these low frequency noises in low-pass  $\Delta\Sigma$  modulator.

## 2.5 Low-IF Receiver

Keeping in view the limitations of ZIF structures, a new receiver architecture called low-IF receiver was introduced in late 90s [41, 42, 43]. The LO frequency is offset from the carrier frequency by a small, but nonzero amount, as a result the downconverted signal is away from dc by this small IF. This receiver architecture combines the advantages of both superheterodyne and homodyne receivers. Since the signal resides at IF, dc-offsets do not corrupt the useful signal. On the other hand, it reduces the RF filters count by bringing the signal directly to a sufficiently low IF where filtering can be performed by on-chip low-pass filters. Even-order distortion products have less effect as is the case in any bandpass system. And in addition, low-IF receiver is also immune to flicker noise since the signal is away from low frequencies where flicker noise is high. This feature makes low-IF receiver the first choice for highly integrated transceivers in advanced cmos technologies which are getting more and more flicker noise. An special case of Low-IF receiver, called  $f_s/2$  receiver is shown alongwith its associated signal flow in Fig. 2.4. In this type of receiver [4], the IF is forced to be equal to half the sampling frequency of the ADC.

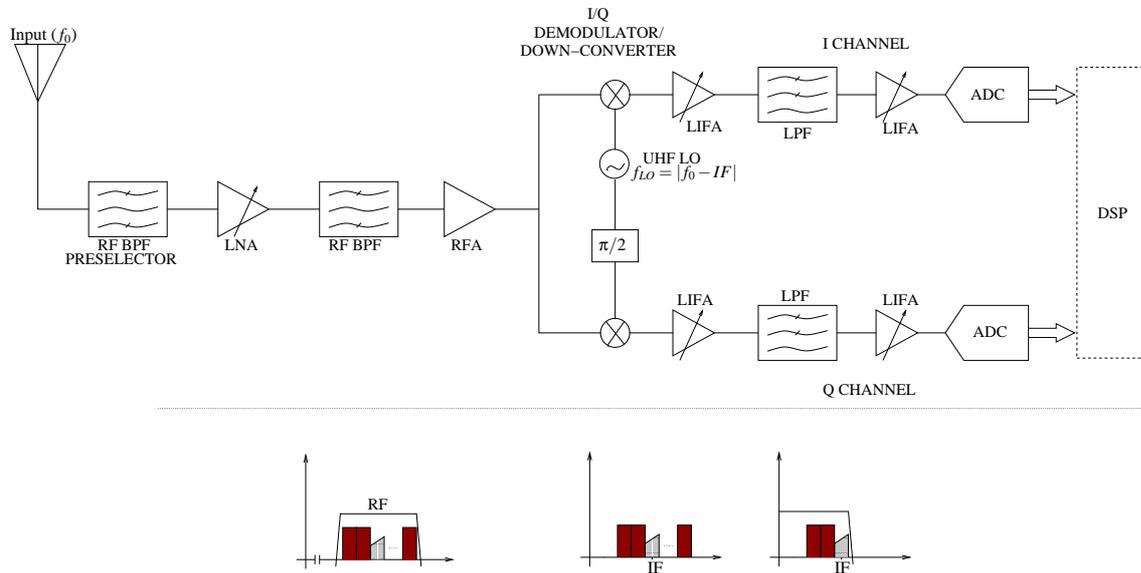


Figure 2.4: Low-IF receiver architecture and signal flow

The main challenge in the design of low-IF receiver is reducing the image signal level.

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In ZIF structure, the image signal is equal to the desired signal and hence a relatively small image rejection ( $\approx 25\text{dB}$ ) proves sufficient for many applications [42]. This level of performance is provided by standard quadrature image reject mixers. On the other hand, image signal in low-IF receivers is not related to the useful signal and can be more than 20dB larger [42, 43]. This calls for an image rejection in the range of 60-80dB [43]. To achieve high image rejection, it is necessary to minimize the imbalance between I and Q signal paths. Numerous techniques have been applied to achieve a good balance between quadrature signal paths, including complex quadrature downconversion [44] and a combination of the quadrature downconversion and complex bandpass filtering [45]. Another design aspect of low-IF receiver is the choice of IF. Low IF reduces the image-rejection capability of the receiver; high IF, on the other hand increases the constraints on the ADC which has to function at at least twice the IF. To address this issue, a recent implementation of low-IF receiver for GSM uses two stage down conversion; first IF is set at 200MHz which is dictated by anti-aliasing requirements then this signal is downconverted once more to 20MHz to meet the 40MHz sampling frequency of ADC. Two possible choices, in case of using  $\Delta\Sigma$  type ADC in this receiver scheme are high-pass and band-pass  $\Delta\Sigma$  modulator. Band-pass  $\Delta\Sigma$  modulator is not the preferred solution because of two reasons: 1) it is complicated to design requiring more surface and power, 2) Since the IF has to be less than  $f_s/2$  for this kind of ADC, this makes the design of image-rejection schemes even more difficult. Therefore the best choice of ADC for this receiver flow is high-pass  $\Delta\Sigma$  modulator as is chosen in [4].

## 2.6 Bandpass Sampling Receiver

The RF-receiver architectures are evolving towards the realization of the concept of software radio. In an ideal software defined radio, the ADC is placed in the RF front-end after the antenna and operates at the sampling frequency which is twice the greatest carrier frequency, and the rest of the processing is performed by powerful digital signal processors. The main issue in the implementation of this idealistic receiver architecture is that, with the current technology it is not possible to design circuits that can process samples at such high rates and with acceptable power consumption for mobile stations. To circumvent this problem, the concept of band-pass sampling receiver has been introduced which inherits some features of the ideal software radio. In the band-pass sampling receiver (also known as harmonic sampling receiver), the RF signal is sampled at a rate lower than the highest frequency of interest to achieve frequency down-conversion by intentional aliasing and to reduce the speed requirements on the following blocks. In this scheme, the sampling rate requirement is no longer based on the RF carrier, but on the bandwidth of the useful signal resulting in a significant reduction in the processing rate. This scheme, at a first glance, seems to simplify the receiver architecture, as the analog RF front-end contains only band-pass filters and low-noise amplifiers followed by a powerful ADC carrying out bandpass sampling and digitizing. The issue here is that the ratio of the RF carrier to the undersampling (subsampling ratio) rate cannot be kept high. The reason being that due to spectrum folding, the noise of the whole band is aliased back into the useful signal band

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causing a significant increase in the noise density and hence the deterioration of signal to noise ratio. The higher the subsampling ratio, the higher the noise density in the signal band. Keeping in view this problem, the band-pass sampling can be applied in the super-heterodyne receiver at the point of I/Q down-converter to reduce the subsampling ratio without exerting extra pressure on the following blocks.

### 2.6.1 Theory of bandpass sampling

The sampling theory (Nyquist criterion) shows that, in order to avoid aliasing and to completely reconstruct a given signal, the sampling rate must be at least twice the highest frequency component in the signal. In the case of baseband signals, the useful information covers the entire band from zero frequency to cutoff frequency. However, the RF signals used in the wireless communications are usually narrow-band but centered on high frequencies carriers, in which case, the minimum sampling rate (in its classical definition) would be quite unrealistic. The bandpass sampling theorem shows that the minimum uniform sampling rate to avoid aliasing depends on the signal bandwidth instead of the highest frequency of interest. The minimum sampling rate for aliasing-free can be as low as twice of the signal bandwidth if the carrier frequency of the signal is properly chosen. However, the minimum sampling rate  $f_{s,min} = 2 \cdot BW$  (where  $BW$  is the signal bandwidth) is just a theoretical value, given that any imperfection in an implementation based on this sampling rate can cause aliasing if no margins are considered. Assume that a band-pass analog signal has its lowest frequency of interest  $f_L$  and the highest frequency of interest  $f_H$  (the bandwidth of the signal equals  $BW = f_H - f_L$ ). The bandpass analog signal can be exactly reconstructed after sampling and digitizing if the sampling rate  $f_s$  meets the following two inequalities [46]:

$$\frac{(n-1)f_s}{2} < f_L \quad \text{and} \quad f_H < \frac{nf_s}{2}$$

where  $n$  is an integer given by  $1 \leq n \leq \lfloor f_H/BW \rfloor$  (where  $\lfloor \cdot \rfloor$  denotes the largest integer). A sampling rate  $f_s$  that meets these two inequalities ensures that the resulting spectra of the sampled signal has no overlapping or aliasing, as clearly illustrated in Fig. 2.5.

From the previous inequalities, the acceptable uniform sampling rates which result in aliasing-free downconversion can be calculated to be:

$$\frac{2f_H}{n} \leq f_s \leq \frac{2f_L}{n-1} \quad (2.1)$$

The maximum allowable value  $n_{max}$  for the bandpass signal with the lowest and highest frequencies  $f_L$  and  $f_H$  is thus equal to:

$$n_{max} = \frac{f_H}{f_H - f_L}$$

Equation. 2.1 can be described graphically as shown in Fig. 2.6 for  $n = 1, 2, \dots, 5$  (where the normalized sampling frequency  $f_s/BW$  versus the normalized highest frequency

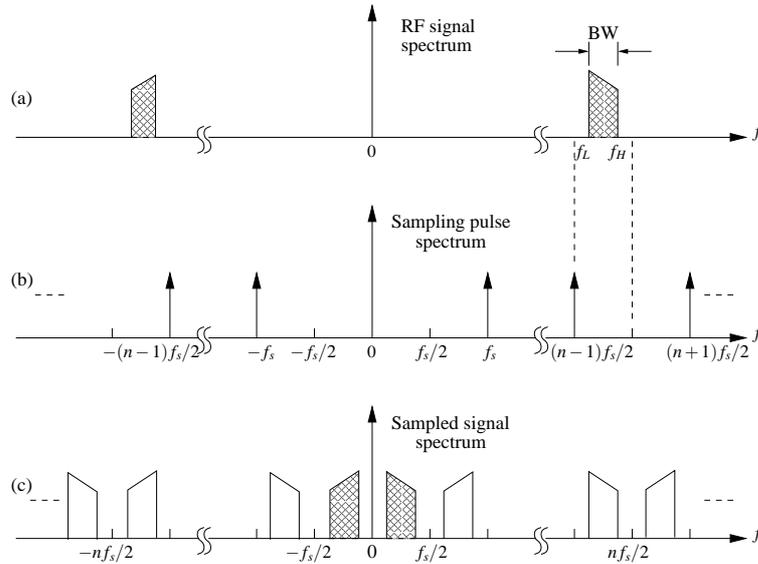


Figure 2.5: Spectra of bandpass sampling (a) RF signal spectrum, (b) sampling pulse spectrum and (c) sampled signal spectrum

$f_H/BW$  is plotted as presented in [46]). The areas inside the wedges are the permissible zones for sampling without aliasing. The shadowed area represents the sampling rates that result in aliasing.

It is apparent that the aliasing-free ranges of the sampling rate and the highest signal frequency of interest,  $\Delta s$  and  $\Delta f_H$ , increase with normalized sampling rate and the highest signal frequency. The smaller the integer number  $n$  is, the broader the permissible area for sampling without aliasing will be. The value of  $n$  is usually lower than 10 when the bandpass sampling technique is used for converting an RF signal to a low IF or baseband signal [47].

## 2.6.2 Drawback of subsampling - Noise spectrum aliasing

It is known that a resistor charging a capacitor gives rise to a total thermal noise with power  $kT/C$  [48], where  $k$  is Boltzmann constant,  $T$  is the absolute temperature and  $C$  is the capacitance. The on-resistance of the switch will introduce thermal noise at the output. The noise is stored on the capacitor along with the instantaneous value of the input voltage when the switch turns off. As shown in Fig. 2.7, the resistor  $R_{on}$  and sampling capacitor  $C$  construct a lowpass filter with a transfer function of:

$$H(f) = \frac{1}{1 + j2\pi f R_{on} C} \quad (2.2)$$

with the 3dB bandwidth of  $f_{3dB} = 1/(2\pi R_{on} C)$ . Thermal noise is known as additive white gaussian noise (AWGN) in communication theory, i.e. having a delta-function autocorrelation with a flat Power Spectral Density (PSD).

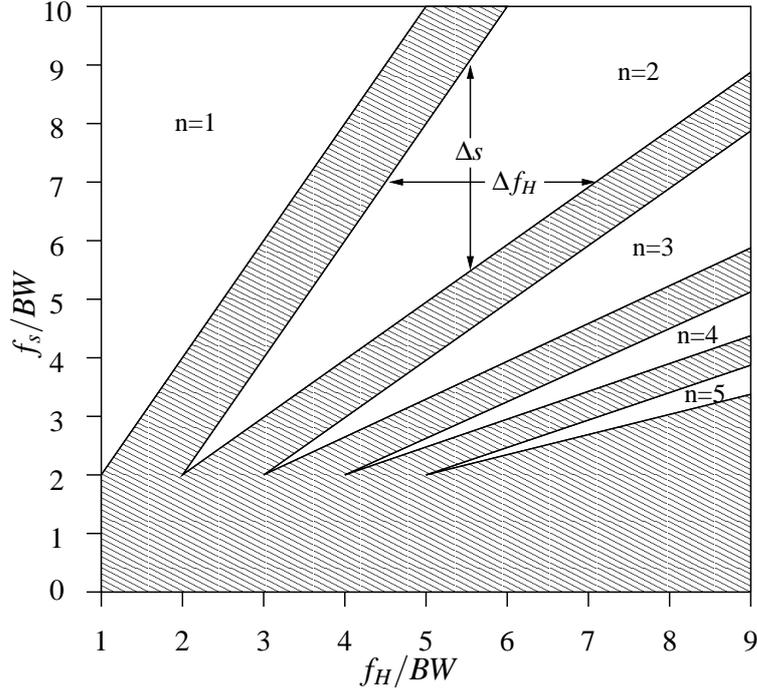


Figure 2.6: Permissible zones for uniform sampling

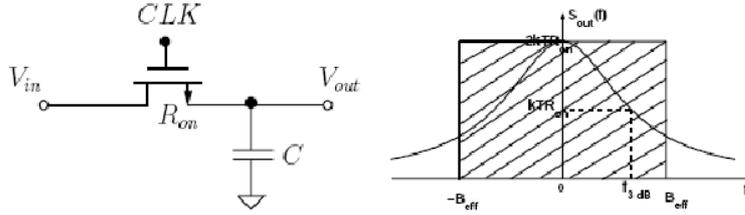


Figure 2.7: Graphical illustration of effective noise bandwidth

The PSD of thermal noise introduced by the resistor  $R_{on}$  can be given as  $S_{in}(f) = 4kTR_{on}$  with a one-sided representation, or  $S_{in}(f) = 2kTR_{on}$  with a two-sided representation. The corresponding noise PSD at the output of lowpass filter is given by:

$$S_{out}(f) = S_{in}(f)|H(f)|^2 = 2kTR_{on} \frac{1}{4\pi^2 f^2 R_{on}^2 C^2} \quad (2.3)$$

by a two-sided representation, and the total noise power is obtained as:

$$P_{out} = \int_{-\infty}^{\infty} S_{out}(f)df = \frac{kT}{C} \quad (2.4)$$

The output noise of the lowpass filter performed by the RC network can be made equivalent to AWGN with a constant PSD within an effective noise bandwidth  $B_{eff}$ . Both

noise sources share the same noise power  $kT/C$  (Fig. 2.7), thus:

$$P_{out} = \frac{kT}{C} = 2kTR_{on} \cdot B_{eff}$$

and

$$B_{eff} = \frac{1}{4R_{on}C} = \frac{\pi}{2} f_{3dB}$$

The effective noise bandwidth of the sampling device  $B_{eff}$  depends on the ON resistance of the switch and the sampling capacitance, and it is normally larger than the maximum frequency of the input signal. When using bandpass sampling, the wideband  $kT/C$  noise will be folded due to the effect of subsampling [49] as illustrated in Fig. 2.8.

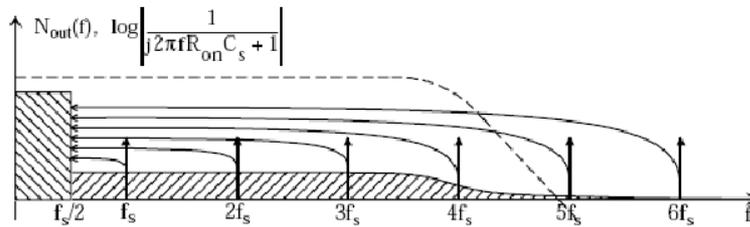


Figure 2.8: Noise aliasing due to subsampling

In this way, the resulting SNR is lower than the equivalent lowpass sampling system in the presence of the same noise source. The SNR degradation in dB is given as [44]:

$$SNR_{deg} \approx 10 \log_{10} \frac{B_{eff}}{B} \cdot \frac{B}{F_s/2} = 10 \log_{10} \frac{2B_{eff}}{F_s} \quad (2.5)$$

In addition to  $kT/C$  noise, strong interfering channels placed on alias frequencies are also folded on top of the useful signal as a result of bandpass sampling, as shown in Fig. 2.9. This corrupts the useful signal irreversibly forcing the need of efficient anti-aliasing mechanism.

### 2.6.3 Bandpass Receiver Configuration

A block diagram of the bandpass-sampling radio receiver architecture is presented in Fig. 2.10.

In this receiver architecture, harmonic sampling is used in the RF stage to bring down the signal frequency from RF to a low IF. The choice of the low-IF is tricky because it has to be high enough to avoid the aliasing on one hand and it has to be low enough so that the ADC and the subsequent DSP can support it. An important thing to notice about this structure is that its analog block configuration is much simpler than the classical architectures presented previously. This structure is also known as digital direction conversion receiver. Its RF front-end consists of two stages of gain adjustable LNA to achieve a low noise figure and certain gain control range and an RF band-pass SAW filter to suppress

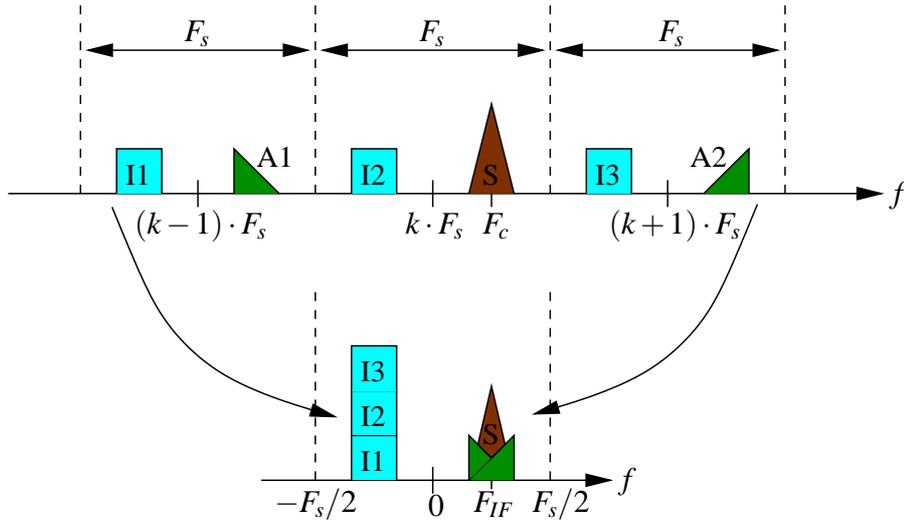


Figure 2.9: Interferers' aliasing due to subsampling

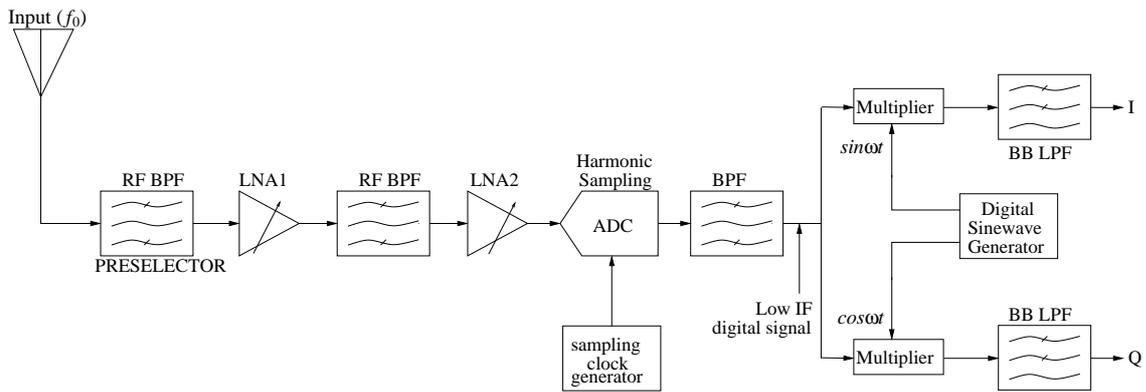


Figure 2.10: Bandpass RF sampling receiver architecture

out-of-band interferers and decrease the aliased noise. The filtered and amplified RF signal is then subsampled at the ADC, and the analog RF signal is converted to low-IF digital signal. The low-IF digital signal after being equally split in two branches is mixed with a pair of quadrature digital LO signals generating base-band digital I and Q signals. Digital low-pass filters are then applied to the base-band I and Q signals to perform channel filtering. Since the channel filtering is only carried out in the digital domain, the signal attacking the ADC contains strong in-band interferers, and hence, it must have enough dynamic range to deal with both strong interference and weak useful signal.

The technique of band-pass sampling is not only used for RF signals but also for IF signals. The subsampling of IF signal takes place in a superheterodyne receiver as illustrated in Fig. 2.11.

The remarkable difference between the subsampling superheterodyne receiver and the

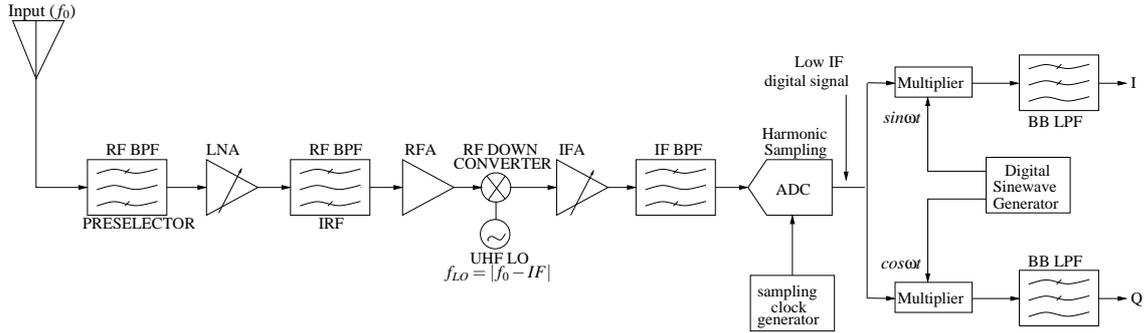


Figure 2.11: Bandpass IF sampling receiver architecture

classical superheterodyne receiver is that the ADC in the former is moved forward to the IF block output i.e the output of the IF SAW filter. The sampling rate of the ADC is close to a subharmonic of the IF:

$$f_s = \frac{f_{IF} - f_{LIF}}{n} \quad (2.6)$$

where  $n = \lfloor \frac{f_{IF}}{f_s} \rfloor$ . The ADC output, which is a digital signal at IF, is converted to base-band I and Q signals by the digital quadrature down-converter. The base-band I and Q signals then pass through low-pass filters which act as channel filters to diminish the interferers near the desired signal.

The key challenge in the band-pass sampling architecture is the design of ADC. With the current CMOS technologies in view, the ADC for a band-pass sampling IF signal is more realistic than for a band-pass sampling RF signal. The bandwidth requirement for ADC is much less when subsampling an IF signal as compared to when subsampling an RF signal. The dynamic range requirement for the ADC used in band-pass sampling of an IF signal is also relaxed (usually 5 to 6 bits) than that applied in band-pass sampling of an RF signal. The reason is that the IF SAW filter in the former case suppresses the interference level before the signal attacks the ADC and hence reduces the dynamic range requirement of the ADC.

#### 2.6.4 $F_s/2$ IF Bandpass-Sampling Receiver

One interesting category of band-pass sampling receivers is  $F_s/2$  IF bandpass sampling receiver. This receiver architecture is exposed in Fig. 2.12. It was proposed by STMicroelectronics and implemented as a discrete-time RF sampling receiver in CMOS 90nm technology for the GSM standard [4, 50]. The main difference with the earlier realizations resides in the fact that the intermediate frequency used during downconversion steps is half the sampling rate ( $F_s/2$ ). This imposes the following constraint while doing the subsampling to bring down the signal from carrier frequency  $F_c$  to intermediate frequency  $F_s/2$ :

$$F_s = \frac{F_c}{N + 1/2} \quad (2.7)$$

The RF signal after being passed through low-noise amplifier and bandpass filters is subsampled at first stage from RF to IF. At this stage it is impossible to downconvert the signal directly to low-IF because the sampling frequency is dictated by the anti-alias requirement [4]. To meet GSM requirements, a sampling frequency of 200MHz ( $F_c/4.5$ ) was proposed in [4]. If an ADC is used at this sampling frequency, it needs unreasonable power consumption. Therefore another stage of subsampling-based downconversion is needed, which brings down the signal at 40MHz which is digitized directly by the high-pass  $\Delta\Sigma$  modulators (ADCs).

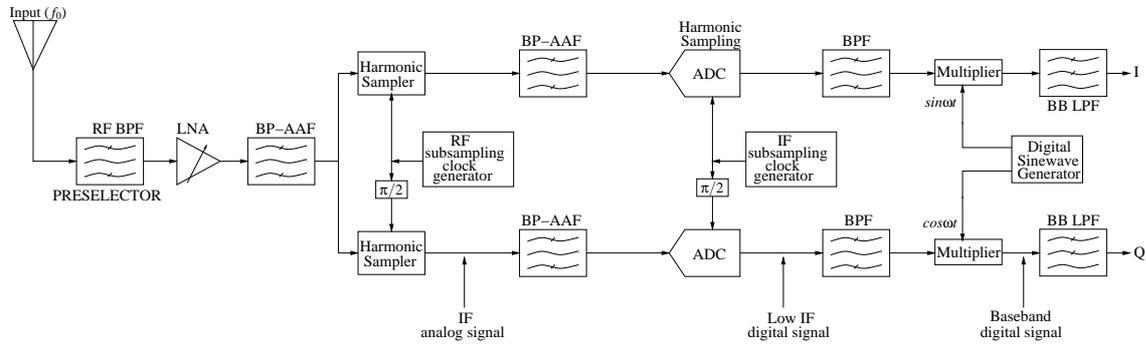


Figure 2.12:  $F_s/2$  IF sampling receiver architecture

The fact that the signal is forcibly placed at  $F_s/2$  after downconversion makes this receiver design to take the advantages of both zero-IF and low-IF structures. Like zero-IF structures, there is no image signal problem since the image is the conjugate of the useful signal itself. Hence, the expensive image reject filters are avoided. Similarly, like low-IF structures, this solution ensures - with no complexity increase with respect to low-pass filters - that flicker noise and second-order nonlinearity products (IP2) do not degrade the signal. Flicker noise is indeed what limits the CMOS implementations of zero-IF architecture for narrow-band standards. To enhance the anti-aliasing capability of this circuit, a completely passive anti-aliasing circuit is proposed in [9]. With the similar receiver architecture as [4, 50], and using this better anti-aliasing technique [9], an RF receiver chain is defined in [3] which addresses two wireless protocols i-e GSM and WiFi. This receiver scheme is illustrated in Fig. 2.13 and its functionality is explained in detail in the following sections.

It comprises of an RF filter, a transconductance LNA, two discrete-time analog signal processing stages (DTASPs) and ADCs. The RF input signal is first filtered, amplified and converted to a current. It is then fed to the first DTASP block, where it gets IIR/FIR filtered and quadrature downconverted to the first intermediate frequency. A second down-conversion stage further decimates the sampling rate and filters the IF signal before it is finally digitized.

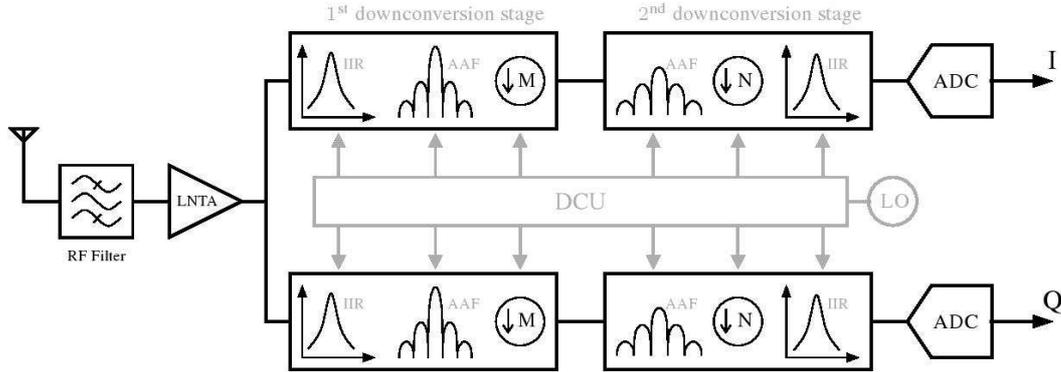


Figure 2.13: Dual-Mode  $F_s/2$  discrete-time sampling receiver [3]

#### 2.6.4.1 RF Stage

RF filters limit the reconfigurability of multistandard receivers and current research works towards the suppression of these filters. In this design however, the RF filter was conserved, as it relaxes the requirements on both the LNA and anti-alias filter. Only one transconductance LNA is used and its current is permanently switched between the in-phase and quadrature paths. This minimizes the I/Q gain mismatches and improves the image rejection of the receiver. The drawback is that the integration period is halved, which in turn halves the LNA gain. Great attention must be paid to the generation of the clock signals because a slight overlapping between I/Q successive sampling phases can shorten the quadrature paths and corrupt the useful signal.

#### 2.6.4.2 First DTASP Stage

The LNTA output current is integrated during a  $T_c/4$  time interval, alternately between the I and Q paths. This results in a sampled data stream with a sampling rate of  $2F_c$  per quadrature path. The IIR filter is employed to prevent the LNTA's output from saturating and is made up of a single pole. However, in contrast to the previous GSM receiver [4], in this receiver architecture, it precedes the AAF/decimation stage, resulting in the capacitors' switching at a rate of  $2F_c$  rather than  $F_s$ . The operation of the 1st DTASP block is illustrated in Fig. 2.14 for comprehension.

It is a series combination of current integrator, voltage sampler and discrete-time IIR filter. The transition from continuous-time to discrete-time occurs at the output of the simplistic sampler. The first decimation stage is preceded by a 2nd order anti-alias filter, which theoretically squares the rejection achieved in the previous design. The desired signal is downconverted through the decimation process to a first intermediate frequency and fed to a second DTASP block. The RF signal is sampled at a rate of  $2F_c$  which results in a first spectrum folding, depicted in Fig. 2.15.

It is important to note that this first sampling doesn't have any dedicated anti-alias filter and benefits only from the attenuations brought by the RF SAW and continuous-time sinc filters. The desired signal at frequency  $F_c$  is not shifted during the sampling process,

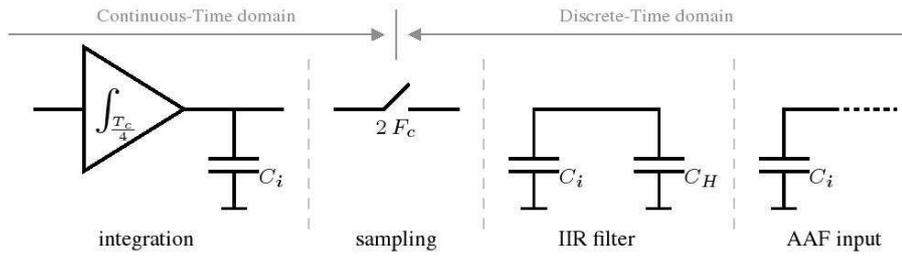


Figure 2.14: Operation of the 1st DTASP block [3]

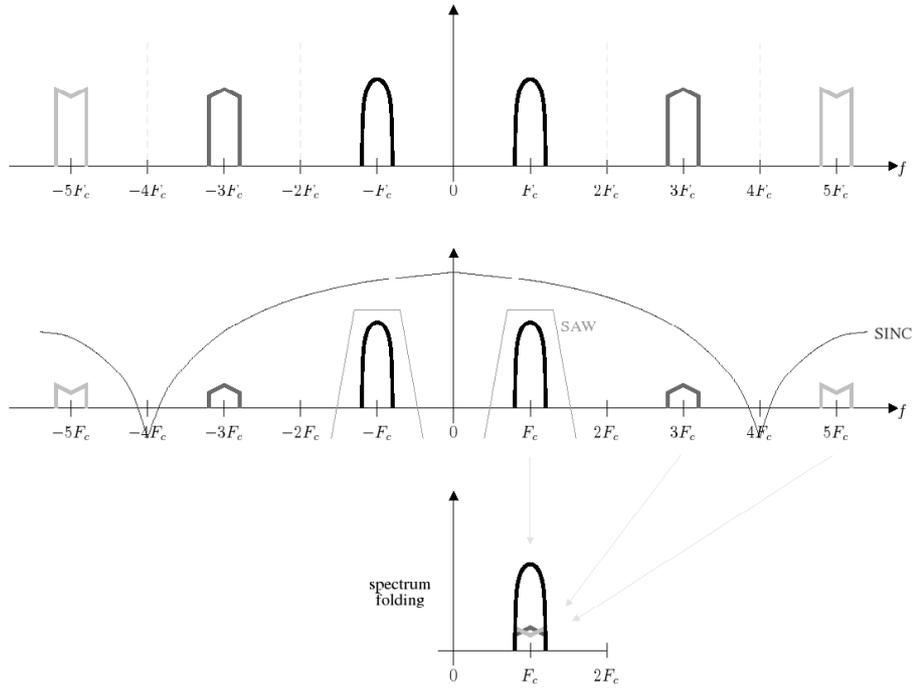


Figure 2.15: Spectrum folding during first sampling

and combines with its own conjugate image located at  $-F_c$ . This is not problematic as the channel spectrum is symmetric. The alias component located at frequency  $3F_c$  is folded on top of the desired signal. In GSM mode, this alias will still have a considerable power level even after attenuation by SAW and sinc filters and may require the use of frequency exceptions to meet the standard specifications [51].

### 2.6.4.3 Second DTASP Stage

This stage performs a second decimation of the sampling rate and further reduces the signal dynamic through a single-pole IIR filter. The decimation is less critical in this stage as it profits from the previous stage's IIR filtering and a first order anti-alias filter is sufficient in this case. The signal is downconverted to a second intermediate frequency and is directly

fed to the ADC.

#### 2.6.4.4 Frequency Plans

The frequency plans of this receiver architecture, adopted for each of the GSM/WIFI modes, are detailed in this section. Values for decimation ratios, sampling and intermediate frequencies are derived as well.

**GSM Mode** The frequency plan of the GSM mode is depicted in Fig. 2.16. The desired signal is always centered at half the sampling frequency ( $F_s/2$ ) to avoid degradations caused by flicker noise and IP2 products and is assured by setting the decimation ratios to odd values.

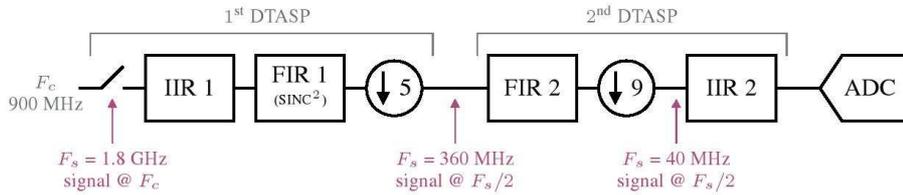


Figure 2.16: GSM mode frequency plan [3]

The first decimation ratio is dictated by the anti-alias requirement, since alias rejection is directly proportional to signal bandwidth over sampling frequency ratio. For a second order anti-alias filter, this rejection is given by:

$$20\log\left(\frac{2F_s}{BW}\right)^2 \geq P_{alias} - S_{dBm} + SNR_{min} \quad (2.8)$$

which imposes a minimum sampling frequency of:

$$F_{s,min} = \frac{200KHz}{2} \cdot 10^{-111/40} \simeq 60MHz \quad (2.9)$$

Note that this expression does not account for the attenuation brought by the SAW filter, and even in this case, has resulted in a considerably low sampling frequency. This is however a theoretical value. In practice, capacitor mismatches at circuit level degrade the notches of the anti-alias filter and force the use of much higher sampling frequencies.

Another drawback of setting a low value for the sampling frequency is that, it results in a high decimation ratio, which in turn increases the complexity of the filter circuit design (longer rotating capacitor banks). The first decimation ratio was therefore set to  $M_1 = 5$ , leading to a sampling frequency of 360 MHz and to a first intermediate frequency of 180 MHz.

The second DTASP stage had to adapt the sampling rate to the 40 MS/s  $\Delta\Sigma$  ADC constraint. The second decimation ratio was thus set to  $M_2 = 360/40 = 9$  and the signal was downconverted to a second intermediate frequency of 20 MHz.

**WiFi Mode** In WiFi mode, owing to the large channel bandwidth, the flicker noise becomes less significant.  $F_s/2$  architecture is not considered necessary anymore and the desired signal is downconverted and processed directly at DC (Zero IF). The RF signal is first sampled at twice the channel frequency ( $2F_c$ ), as in the GSM mode. IIR and anti-alias filters are still centered around the RF channel. The signal is then downconverted to DC by setting the decimation ratio to an even value.

In this configuration, the RF stage remains unchanged and the anti-alias filter is the only block that has to be reconfigured. The frequency plan for WiFi mode is given in Fig. 2.17. Only the first DTASP stage was actually implemented on circuit. The second downconversion stage and the ADC are added to give a complete illustration of the receiver.

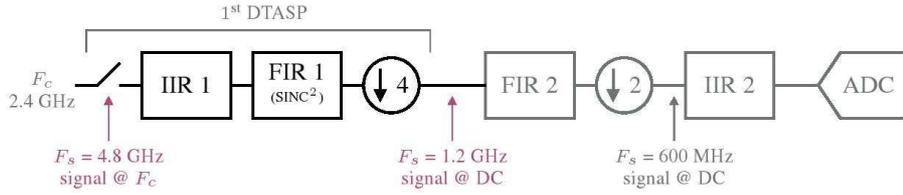


Figure 2.17: WiFi mode frequency plan [3]

Like in GSM mode, the first decimation ratio is dictated by the alias rejection requirements. Using the same second order anti-alias filter, the minimum sampling frequency is now equal to :

$$F_{s,min} = \frac{20MHz}{2} \cdot 10^{(-20+65+21.1)/40} \simeq 450MHz \quad (2.10)$$

The sampling frequency was set to a much higher value than the minimum required, to account for notch degradations at circuit level. The decimation ratio was set to  $M_1 = 4$  in order to facilitate the reconfigurability of the anti-alias filter. Once downconverted to DC, the signal is buffered and outputted for measurement. The second DTASP stage (which was not implemented) includes a first order anti-alias filter, a decimation by  $M_2 = 2$  and a single pole IIR filter. The sampling rate is lowered to 600 MHz and the signal is fed to the ADC for digitization.

#### 2.6.4.5 Proposed Frequency Plans

After studying the recent state-of-the-art RF receiver front-ends, and keeping in view the available ADC performances which are detailed in the next chapters, the frequency plan illustrated in Fig. 2.18 is proposed. Note that in contrast to the receiver front-end presented earlier [3],  $F_s/2$  architecture is adopted for both the protocols to stay clear from Flicker noise and dc-offsets throughout the signal processing.

The ADC for GSM mode runs at the speed of 28.57MHz, while the ADC for WiFi mode is configured to operate at 228.57MHz.

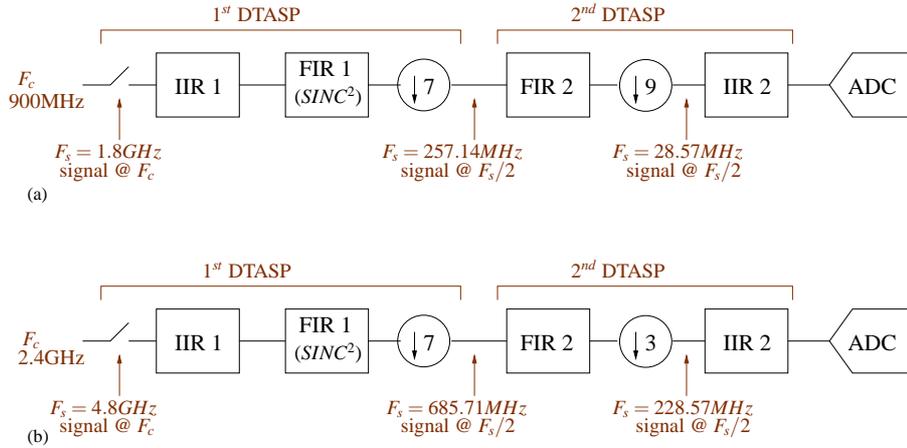


Figure 2.18: (a) GSM mode frequency plan, (b) WIFI mode frequency plan

## 2.7 Conclusion

The RF front-ends of various competing radio receiver architectures are discussed in this chapter. Superheterodyne receiver topology is the most commercially popular RF receiver because of its performance. To cater for the increased constraints on receiver front-ends these days, including integrability and reconfigurability, newer and innovative receiver topologies are being introduced. Digital IF receiver is exposed, which is a type of Superheterodyne architecture where the signal is digitized in the IF stage. Direct Conversion receiver is explained which has the advantages of simplicity and reduced component count. It gets rid of the components which are difficult to be integrated. But it has the problems of imbalance between I and Q signal paths, dc-offset and flicker noise directly corrupting the signal. Low-IF receiver gets rid of the problems associated with direct-conversion receiver but it introduces its own problem i.e image signal corrupting the useful signal after down-conversion. Image-reject filters need to be introduced which are expensive. To make the receivers integrable, reconfigurable and flexible (realization of software radio concept), the technique of bandpass sampling is used which helps in reducing the analog component count by digitizing the signal at earlier stages in the front-end receiver. One application of this reception technique is the recently introduced receiver architecture :  $F_s/2$  IF receiver. It solves the problems of both direct-conversion and low-IF receivers, while enjoying the advantages of both of them. In this architecture, the sampling frequency is selected such that after downconversion, the useful signal falls at half of the sampling frequency. As a result, the image is the conjugate of the signal, hence avoiding the image-reject filters. Moreover, since the signal is centered at  $IF = F_s/2$ , the dc-offsets of various components and device flicker noise do not corrupt the signal. To directly digitize this signal, a special kind of ADC, called high-pass  $\Delta\Sigma$  modulator, is required.

In the research work conducted at our laboratory, all the blocks in the receiver chain for multi-mode operation have already been designed [3], with a special focus on efficient anti-alias filter design [9]. The objective of the rest of this research work is to propose and

design an efficient ADC i.e high-pass  $\Delta\Sigma$  modulator that can support multiple wireless standards and be integrated in the receiver chain already designed.

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## Chapter 3

# $\Delta\Sigma$ Modulator and System Level Modeling

### 3.1 Introduction

ADCs with high resolution are widely used in the areas of instrumentation, measurement, telecommunications, digital signal processing, consumer electronics, etc. With the advancements in the Very Large Scale Integration (VLSI) technologies, the focus is shifted on oversampling and  $\Delta\Sigma$  converters for applications requiring high precision analog-to-digital conversion with narrow bandwidth [52, 12, 10, 53]. They are preferred because of their inherent relaxed sensitivity to analog circuit errors and reduced analog processing as compared to other analog-to-digital conversion techniques. These advantages come at the expense of relatively large amount of digital processing and the working of the major part of circuit at a clock rate which is much higher than the analog-to-digital conversion rate. Because of using higher clock rates and feedback loop, these converters tend to be robust in the face of analog circuit imperfections [52] and do not require trimmed components which are considered necessary in conventional high precision Nyquist rate ADCs. Because of these reasons high precision  $\Delta\Sigma$  ADCs can be implemented using high density VLSI processes. These processes are optimized for digital circuitry where analog accuracy is sacrificed for circuit density and speed. Thus, the integration capability of  $\Delta\Sigma$  ADCs in these processes makes it possible to design integrated, smaller, robust and less expensive systems.

$\Delta\Sigma$  ADC is a system which consists of a  $\Delta\Sigma$  modulator followed by a digital decimation filter. The  $\Delta\Sigma$  modulator over-samples the input signal i-e performs sampling at a rate much higher than the nyquist rate. The ratio of this rate to the Nyquist rate is called over-sampling ratio (OSR). After over-sampling, it typically performs very coarse analog-to-digital conversion at the resulting narrow-band signal. By using coarse digital-to-analog conversion and feedback, the quantization error introduced by the coarse quantizer is spectrally shaped i-e the major portion of the noise power is shifted outside the signal band. This process is called quantization noise shaping. The digital decimation filter removes the out-of-band portion of the quantization error and brings back the output rate to Nyquist

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rate.

This entire process of oversampling coupled by quantization noise shaping and decimation filtering results in high precision ADC despite the fact that coarse ADC and DAC are used. In particular, 1-bit ADC and 1-bit DAC are often employed which have the added advantage that static errors in their outputs only affect the gain and offset of the system without introducing any distortion. Another advantage of oversampling is the relaxed requirements on analog anti-aliasing filter because much of the required anti-aliasing functionality is provided by the digital decimation filter.

In this chapter, the principle of  $\Delta\Sigma$  modulation is explained, single-loop second-order architectures are exposed and various higher order topologies are discussed. Multibit quantizer techniques along with their inherent problems and their solutions are presented. Continuous time (CT)  $\Delta\Sigma$  modulators are introduced, followed by recently published hybrid (CT and DT) structures. In the end, system level modeling of various components, including quantizer, op-amp and comparator is presented along with simulation results.

### 3.2 Working Principle

The basic working of  $\Delta\Sigma$  ADC is that it exchanges output resolution with conversion speed. In such ADC, the analog signal is converted into a low resolution code at a frequency much higher than the Nyquist rates, and then the excess quantization noise is removed by the following digital filters [10]. Thus, if OSR is high, the oversampling  $\Delta\Sigma$  ADCs are very suitable for CMOS VLSI digital technology, because they do not require high performance analog building blocks. Fig. 3.1 shows the basic block diagram of a Delta-Sigma modulator and its corresponding linear model. The Delta-Sigma modulator consists of a feedforward path formed by a loop filter and a  $B$ -bit quantizer, and a negative feedback path around them, using a  $B$ -bit DAC [11]. In the linear model as illustrated in Fig. 3.1, the DAC is assumed to be ideal and the injected quantization error is assumed as an additive white noise approximation. Although this approximation is not valid for low-resolution quantizers, it is nonetheless used for simplicity of calculations.

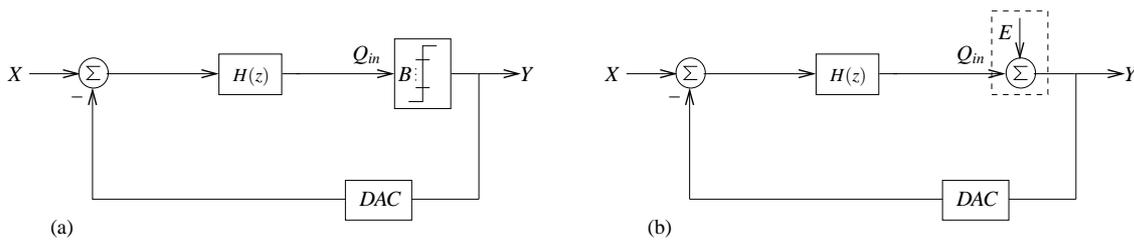


Figure 3.1: Basic  $\Delta\Sigma$  Modulator (a) Block diagram, (b) Corresponding linear model

In this way, the modulator can be considered as a two-input, one-output linear system. The signal transfer function,  $STF(z)$  of this system is:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1 + H(z)} \quad (3.1)$$

and the noise transfer function,  $NTF(z)$  is:

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \quad (3.2)$$

By using superposition principle, the output signal is obtained as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \quad (3.3)$$

By properly selecting the loop filter, the signal transfer function and the noise transfer function of a theoretical 1st order  $\Delta\Sigma$  modulator yield in the  $z$ -domain:

$$STF(z) = z^{-1} \quad (3.4)$$

$$NTF(z) = (1 - z^{-1}) \quad (3.5)$$

Solving Eqns. 3.1 and 3.4 gives:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (3.6)$$

Note that loop-filter is simply an integrator which can be easily implemented with switched-capacitor techniques. For a generalized  $L$ th order  $\Delta\Sigma$  modulator, the transfer functions become:

$$STF(z) = z^{-L} \quad (3.7)$$

$$NTF(z) = (1 - z^{-1})^L \quad (3.8)$$

To achieve a transfer function of  $L$ th order,  $L$  basic building blocks i-e  $L$  integrators are required. Fig. 3.2 plots the frequency responses of  $NTF$ s with different values of  $L$ . When the modulator order is higher than one, the frequency response of  $NTF$  presents the characteristic of high-pass filters. The higher the order  $L$  is, the more quantization error energy is suppressed at low frequencies.

In this way, the output signal for the ideal linear model can be written as:

$$Y(z) = X(z)z^{-L} + E(z)(1 - z^{-1})^L \quad (3.9)$$

The input signal  $X(z)$  experiences just  $L$  delays as it passes through the modulator, while the quantization noise  $E(z)$  experiences an  $L$ th order high-pass filtering as it makes its way through  $L$ th order  $\Delta\Sigma$  modulator. If the quantization step is small compared to the quantizer input amplitude, the quantization error can be assumed to be a random process. Taking  $\Delta$  as the quantization step, the quantization error is bound between  $[-\Delta/2 \leftrightarrow \Delta/2]$  with a uniform probability density of  $1/\Delta$  [54]. The variance of the quantization error is calculated as:

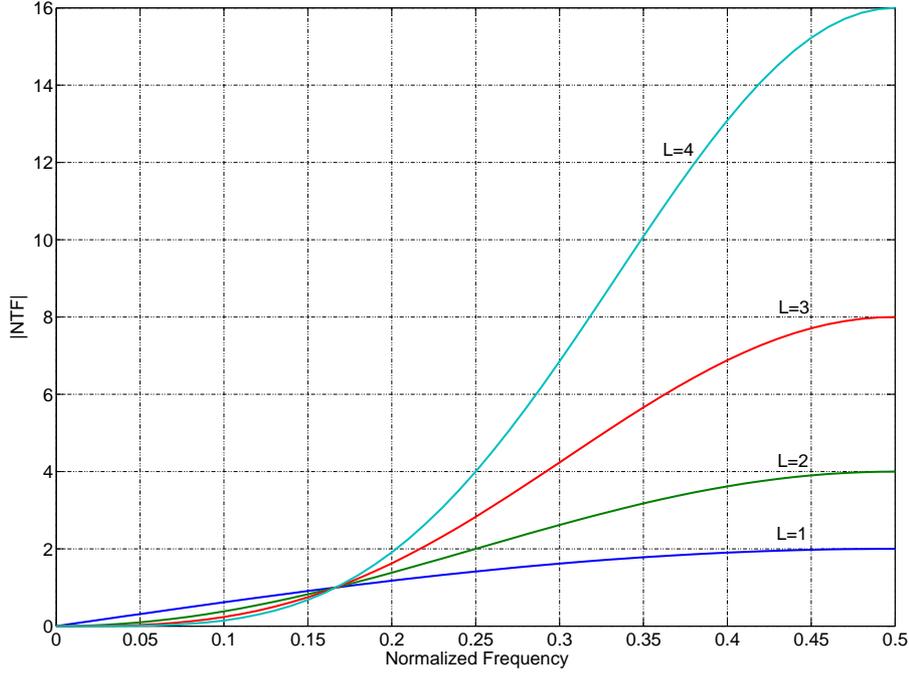


Figure 3.2: Frequency responses of NTFs for different modulator orders  $L$

$$\overline{e^2} = \sigma^2(e) = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \quad (3.10)$$

Hence, the in-band power of the filtered quantization error is found to be:

$$P_Q = \int_{-f_b/2}^{f_b/2} \frac{\Delta^2}{12} |NTF(f)|^2 df \approx \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}} \quad (3.11)$$

Ideally, the full-scale range of the modulator input is approximately given by that of the quantizer. In a  $B$ -bit quantization case, this range equals  $\pm(2^B - 1)\Delta/2$ , so the full-scale input amplitude is  $(2^B - 1)\Delta/2$  and its power at the ADC output can be approximated to:

$$P_{signal} \cong \frac{(A_{FS})^2}{2} = \frac{((2^B - 1)\frac{\Delta}{2})^2}{2} \approx 2^{2B-3}\Delta^2 \quad (3.12)$$

Using Eqns. 3.11 and 3.12, the dynamic range (DR) of an ideal oversampling noise-shaping converter yields:

$$DR(dB) \approx 10 \log_{10} \left[ \frac{3(2L+1)}{2} \frac{OSR^{2L+1}(2^B - 1)^2}{\pi^{2L}} \right] \quad (3.13)$$

The theoretical DR is a function of the modulator order  $L$ , oversampling ratio  $OSR$ , and the numbers of bits in the quantizer  $B$ . Equation 3.13 reveals that an additional bit in

the internal quantizer can roughly obtain a 6-dB improvement of DR. This improvement is independent of the OSR, while the improvement obtained with increasing the order  $L$  is dependent on it. The DR of a theoretical  $L$ th-order Delta-Sigma converter increases with OSR in  $(L + 1/2)$  bits/octave. This is shown in Fig. 3.3, where the DR is plotted as a function of the oversampling ratio and the modulator order, in case of a single-bit internal quantizer.

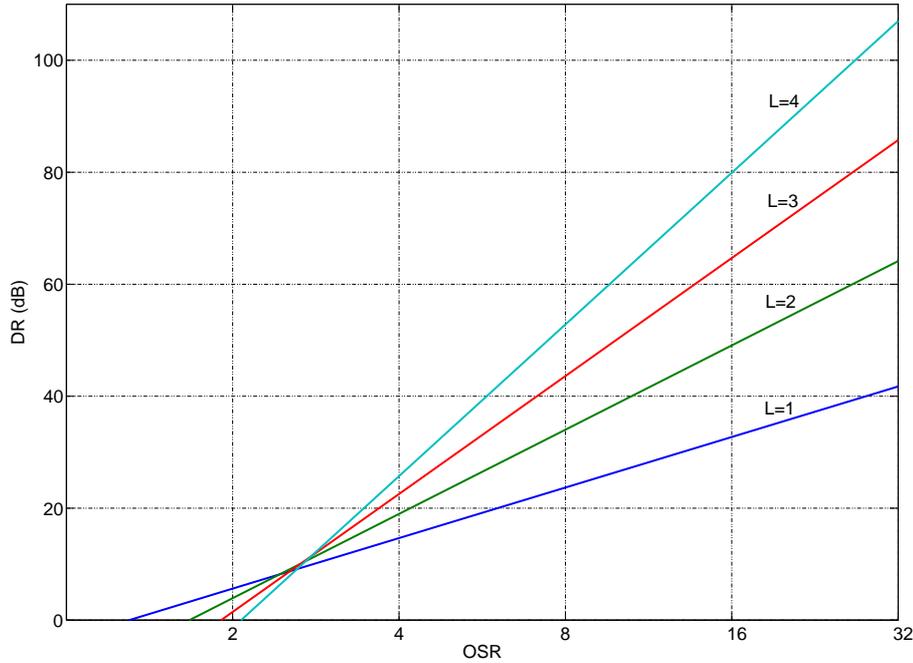


Figure 3.3: DR vs OSR of  $L$ th-order theoretical  $\Delta\Sigma$  modulators

Note that for  $\text{OSR} > 4$ , the combined action of oversampling and noise-shaping considerably improves performance. It implies that oversampling is the essential condition for extracting advantage out of noise shaping. On the other hand, since sampling frequency is directly limited by the technology and the slew-rate of opamps, it can not be infinitely increased. Therefore, using multibit quantizer is becoming the common method to improve the DR, since the modulator has to be designed at a low OSR to maximize the signal bandwidth.

### 3.2.1 Stability

In order to get a stable modulator, the input of the quantizer must be not saturated. The input of the quantizer as illustrated in Fig. 3.1 can be calculated as in [10]:

$$Q_{in}(z) = STF(z)X(z) + (NTF(z) - 1)E(z) \quad (3.14)$$

Therefore, the gain of the  $|NTF(z) - 1|$  or  $|NTF(z)|$  should be small. However, note from Fig. 3.2 that the gain of noise transfer functions of the form  $(1 - z^{-1})^L$  increases

rapidly in the high-frequency region. The maximum gain  $\|NTF\|_\infty$  is equal to  $2^L$  at  $f = f_s/2$ , thereby, exhibiting unbounded states, if  $L > 2$ . Consequently, the theoretical increase of performance by using high-order  $\Delta\Sigma$  modulator at certain OSR is not achievable in practice [10]. In general, instability appears at the modulator output as a large-amplitude low-frequency oscillation, leading to long strings of alternating +1's and -1's [10]. High-order quantization error shaping can be achieved by either single-loop through suppression of out-of-band gain or cascading the Delta-Sigma modulators of only 1st- and/or 2nd-order.

### 3.3 Second-Order $\Delta\Sigma$ Modulator Architectures

First-order  $\Delta\Sigma$  modulator has the advantages of being simple, robust and stable. Despite these good points, its overall performance in terms of resolution and idle-tone generation is inadequate for most applications. Second-order  $\Delta\Sigma$  modulator overcomes these disadvantages at the expense of increased circuit complexity and reduced signal range. In this section, we present various state-of-the-art 2nd-order  $\Delta\Sigma$  modulator architectures along with their associated pros and cons.

#### 3.3.1 Boser Structure

A classical and widely used structure of second-order modulator was proposed by Bernard E. Boser in [12]. This modulator is shown in Fig. 3.4

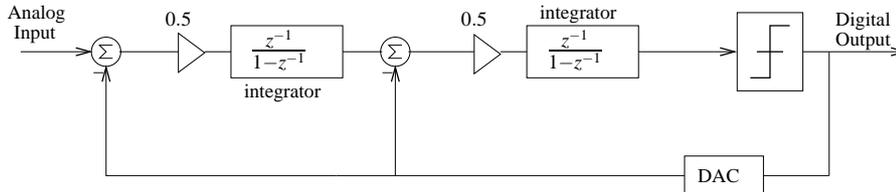


Figure 3.4: Boser Modulator

There are three distinguishing features of this arrangement that make it a good configuration. First advantage is that it employs forward path delay in both integrators, thus rendering it easy for implementation in sampled-data analog circuits. The second feature is that the signal entering each integrator is attenuated by a factor of 0.5, thus reducing the voltage swing requirements of the op-amps implementing the integrators. The third positive point of this structure is that there is no adder before the quantizer, in contrast to the feed-forward structures. This adder can be quite complicated to design. The output of second integrator is fed directly into the quantizer, without undergoing attenuation, resulting in an easy design of quantizer.

### 3.3.1.1 Linear Analysis

To carry out the linear analysis, we replace the non-linear component of the system i.e. quantizer by its linear model. This model, shown in Fig. 3.5, approximates the non-linear quantizer by a gain  $G$  called ‘quantizer gain’ in series with an additive gaussian noise source uncorrelated with the input signal. This approximation, which is valid when the quantization step is small as compared to the signal amplitude, is also used for low-resolution quantizers, where it is not verified.

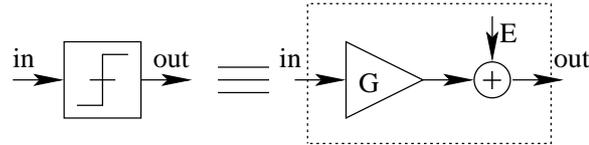


Figure 3.5: Linear model of quantizer

Using this model of the quantizer gain, the signal transfer function (STF) of the boser-based HP modulator is found to be:

$$STF = \frac{0.25Gz^{-2}}{D(z^{-1})} \quad (3.15)$$

and the noise transfer function (NTF) is calculated to be:

$$NTF = \frac{(1 - z^{-1})^2}{D(z^{-1})} \quad (3.16)$$

where  $G$  is the quantizer gain and,

$$D(z^{-1}) = 1 - (2 - 0.5G)z^{-1} + (1 - 0.25G)z^{-2}$$

Assuming a hypothetical value of 4 for the quantizer gain (which is not correct as demonstrated in the next chapter, but simplifies the calculation), results in the famous STF of:

$$STF = z^{-2} \quad (3.17)$$

and NTF of:

$$NTF = (1 - z^{-1})^2 \quad (3.18)$$

Note that STF is an all pass filter and NTF is a low pass filter having a zero at  $F_s/2$  thus attenuating the noise around signal band.

### 3.3.1.2 Disadvantage of Boser Structure

Boser-based structure is basically a feedback-only structure. The input signal has to traverse through all the integrators to reach the quantizer. The principal disadvantage of this structure thus stems from the fact that the signal entering the integrators consists of not only the quantization noise, but also the input signal. Any op-amp non-linearity in the integrators directly generates the input signal harmonics in the signal band, thus degrading the signal-to-noise-and-distortion-ratio (SNDR).

### 3.3.2 Silva Structure

José Silva working at Oregon State University revolutionized the  $\Delta\Sigma$  architectures by proposing a new architecture in [13] which took care of the shortcoming of Boser architecture. His proposed architecture is shown in Fig. 3.6

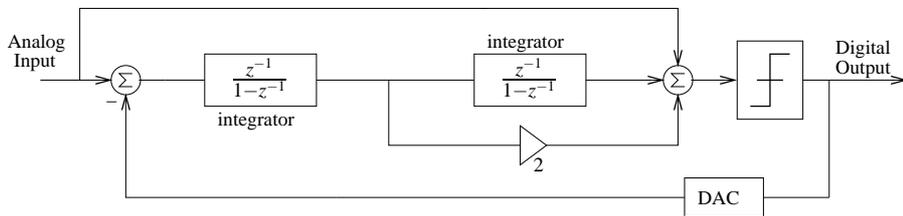


Figure 3.6: Silva Modulator

This architecture is basically feedforward in nature; input signal is fed directly to the quantizer and thus does not have to traverse the integrators. As a result, the non-linearities of the op-amps constituting the integrators do not distort the input signal. This is why, this architecture is also called low-distortion architecture. The refined version of this architecture with optimized coefficients is presented in [55] and shown in Fig. 3.7.

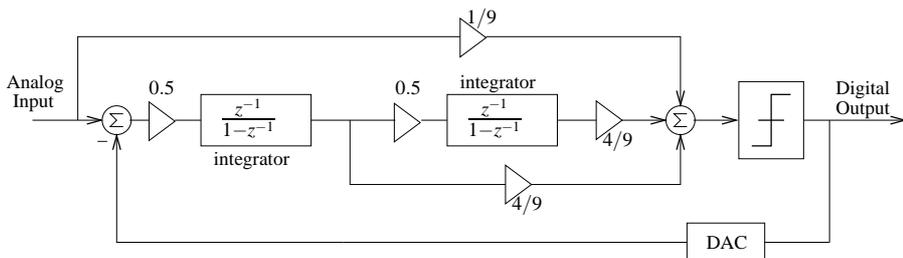


Figure 3.7: Optimized version of Silva Structure (Rusu Structure)

It has to be noted that the sum of the coefficients before the comparator is one; with this set of coefficients, the adder can be implemented passively. Passive adder reduces the power consumption of the circuit by avoiding the use of an op-amp (active adder). Using an active adder is basically equivalent to utilizing the resources of a third-order modulator while getting the performance of only a second-order modulator.

### 3.3.2.1 Linear Analysis

Replacing the quantizer by its linear model as shown in Fig. 3.5 and discussed in Section. 3.3.1.1 and performing the analysis of refined Silva-based structure results in the STF of:

$$STF = \frac{G/9}{D(z^{-1})} \quad (3.19)$$

and similarly the NTF is found to be:

$$NTF = \frac{(1 - z^{-1})^2}{D(z^{-1})} \quad (3.20)$$

where  $G$  is the quantizer gain and,

$$D(z^{-1}) = 1 - (2 - \frac{2G}{9})z^{-1} + (1 - \frac{G}{9})z^{-2}$$

Assuming a value of 9 for  $G$  (for the ease of calculation) results in:

$$STF = 1, NTF = (1 - z^{-1})^2 \quad (3.21)$$

Since STF is one, the input signal is cancelled out at the input of first integrator and hence the linearity requirements of the op-amp are very relaxed resulting in its easy design.

### 3.3.2.2 Disadvantages of Silva Structure

The Silva structure uses one adder before the quantizer. It can be implemented as either passive or active adder. In the case of using a passive adder, we reduce the signal swing at the 2nd integrator output because of additional parasitic capacitances of the summing node [14]. Passive adder also increases the design requirements of comparator because its input signal is attenuated and thus it needs higher sensitivity. The other possibility is using an active adder. Active adder on the other hand involves an opamp, which increases the power consumption of the modulator. The second problem associated with this structure is that the first opamp has to charge both the sampling capacitor of the second opamp, and the feedforward capacitor which is used for implementing the adder. Thus it increases the capacitive loading on the amplifier hence augmenting its power consumption.

### 3.3.3 Oberst Structure

A new modulator architecture has been proposed recently in literature [14], which is halfway between feedback and feedforward architectures. Its operation is illustrated in Fig. 3.8. This modulator uses the advantages of both Boser and Silva structures i-e there is no adder before the quantizer and the input signal attacks directly the second integrator, thus the first integrator, which is the most critical one does not process the input signal resulting in relaxed requirements of the opamp. The distortions generated in the second integrator are first-order noise-shaped and hence are less critical.

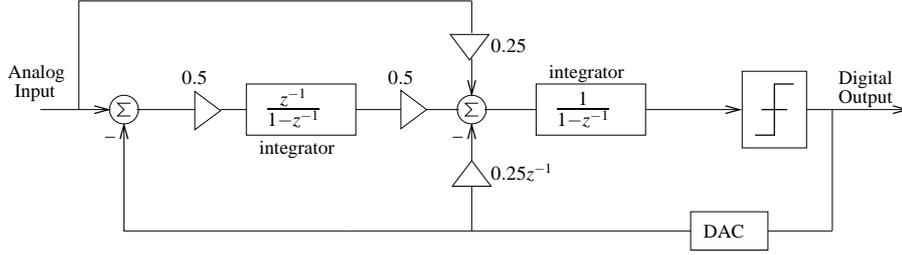


Figure 3.8: Oberst Structure

### 3.3.3.1 Linear Analysis

Replacing the quantizer by its linear model as shown in Fig. 3.5 and discussed in Section. 3.3.1.1 and performing the analysis of Oberst structure results in the STF of:

$$STF = \frac{G/4}{D(z^{-1})} \quad (3.22)$$

and similarly the NTF is found to be:

$$NTF = \frac{(1 - z^{-1})^2}{D(z^{-1})} \quad (3.23)$$

where  $G$  is the quantizer gain and,

$$D(z^{-1}) = 1 - \left(2 - \frac{G}{2}\right)z^{-1} + \left(1 - \frac{G}{4}\right)z^{-2}$$

Assuming a value of 4 for  $G$  results in:

$$STF = 1, NTF = (1 - z^{-1})^2 \quad (3.24)$$

Unity STF results in the cancellation of useful signal at the input to the first integrator, and hence the non-linearities of its op-amp do not generate distortions. On the other hand, the signal entering the second integrator contains a portion of input signal, hence its non-idealities corrupt the useful signal appearing at the output.

### 3.3.3.2 Disadvantages of Oberst Structure

The Oberst architecture is still constrained by the nonlinearities of the opamp which implements the second integrator, even though they are first-order noise shaped. The other disadvantage arises from the fact that the second integrator is a delay less filter and thus the capacitive loading on the opamp comprising the first filter increases during the integration phase, since it has to charge both its own feedback capacitor and the sampling capacitor of the next filter. The third disadvantage is the use of small coefficients 0.25 for second integrator in this architecture. For the implementation of this small coefficient, we have to use an integration capacitor of  $(1/0.25)C_s = 4C_s$ , which makes a big capacitor value and thus results in higher power consumption for charging this capacitor. The

fourth disadvantage is the presence of feedback with a delay. This complicates the design necessitating an extra capacitor.

### 3.4 Higher-Order $\Delta\Sigma$ Modulator Architectures

There are two existing techniques to achieve higher-order  $\Delta\Sigma$  modulation 1) Single loop higher order 2) MASH (Multi-stage noise SHaping) or cascaded higher order. Single loop architectures are affected by the instability of modulator due to excess gain of NTF in high frequencies. To counter this problem various techniques have been adopted which attenuate the NTF gain in high frequencies at the expense of higher NTF gain at low frequencies thus degraded signal to quantization ratio (SQNR). MASH topologies on the other hand are unconditionally stable since they are formed by cascade of lower order modulators. They are prone to noise leakage because of analog and digital components mismatch.

#### 3.4.1 Single-Loop Higher-Order

As discussed earlier in Section. 3.2 and shown in Fig. 3.2, the gain of the noise transfer function of the form  $(1-z^{-1})^L$  increases exponentially in the high-frequency region reaching its maximum value  $\|NTF\|_{\infty}$  of  $2^L$  at  $f = F_s/2$ , where  $L$  is the modulator order. For single loop modulator with one bit internal quantizer to remain stable, Lee's rule [56] dictates that this gain must be smaller than 1.5. There are two techniques to attenuate the NTF gain at high frequencies, the first one converts NTF to Butterworth filter while the other one changes NTF to inverse Chebyshev filter. Both of these techniques result in loss of SQNR due to higher gain of NTF in the signal band. Butterworth filter is obtained by a classic cascade of integrators by choosing the appropriate coefficients. It has an NTF of the form:

$$NTF_{Butterworth} = \frac{(1-z^{-1})^L}{D(z)} \quad (3.25)$$

Where  $(1-z^{-1})^L$  is the noise-shaping factor, and  $D(z)$  is the  $L$ th-order polynomial which reduces the NTF gain at high frequencies. Since, all the zeros are placed on dc, the NTF has a good response at dc level, but it degrades at higher frequencies [10].

NTF can be further improved by placing notches in the signal band for further shaping of the quantization noise, while preserving its controlled high-frequency gain, and therefore maintaining the modulator stability. This type of response is provided by inverse Chebyshev filter which is realized by placing local feedback loops around integrators to form resonators [57]. NTF achieved with this filter is given by:

$$NTF_{inverseChebyshev} = \frac{(1-z^{-1})^L G(z)}{D(z)} \quad (3.26)$$

where  $G(z)$  results in generating optimal complex-conjugate pairs of zeros which create ripples at the stop band of the signal. The zeros are optimally spread over the band resulting in in-band noise power reduction of 13dB relative to the Butterworth filter for

4th order modulator [58]. As a result, the maximum achievable SQNR of  $L$ th-order inverse Chebyshev filters is higher than that of Butterworth filters. However, in comparison with the theoretical NTF, the in-band noise attenuation of both alternatives is poor.

### 3.4.1.1 Cascade of integrators with distributed feedback (CIFB) structure

The generalized  $L$ th-order cascade of integrators with distributed feedback as well as distributed input coupling (CIFB) structure is shown in Fig. 3.9. It consists of  $L$  cascaded delaying-integrators, with the feedback signal as well as the input signal being fed to each integrator with different weight factors  $a_i$  and  $b_i$  respectively.

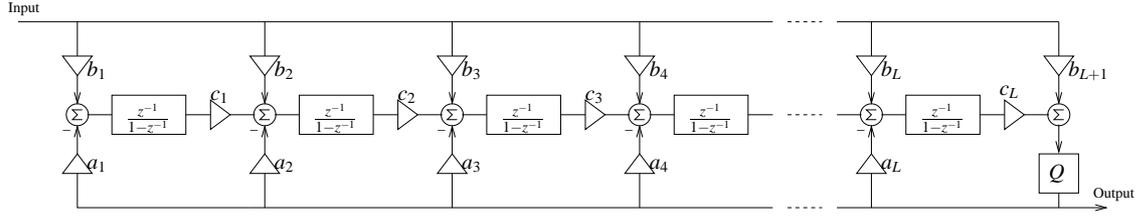


Figure 3.9: Generalized  $L$ th-order CIFB structure

The scaling coefficients  $c_i$  are used to control the output excursions of integrators. The NTF of this configuration is of the form:

$$NTF = \frac{(1 - z^{-1})^L}{D(z)} \quad (3.27)$$

where,

$$D(z) = a_1 c_1 c_2 \cdots c_L z^{-L} + a_2 c_2 c_3 \cdots c_L z^{-L+1} (1 - z^{-1}) + \cdots + a_L c_L z^{-1} (1 - z^{-1})^{L-1} + (1 - z^{-1})^L \quad (3.28)$$

Note that this NTF has Butterworth filter characteristics with  $L$  zeros at dc. Coefficients  $a_i$  alongwith scaling coefficients  $c_i$  determine the pole locations of NTF and have non-zero values to stabilise the modulator. The STF is given by:

$$STF = \frac{b_1 c_1 c_2 \cdots c_L z^{-L} + b_2 c_2 c_3 \cdots c_L z^{-L+1} (1 - z^{-1}) + \cdots + b_{L+1} (1 - z^{-1})^L}{D(z)} \quad (3.29)$$

where  $D(z)$  is given in Eqn. 3.28. This indicates that the  $b_i$  and  $c_i$  determine the STF zeros while  $a_i$  and  $c_i$  fix the poles. There is some latitude in choosing the zeros of the STF, and hence  $b_i$ . A good choice is  $b_i = a_i$  for all  $i \leq L$  and  $b_{L+1} = 1$  [59], which results in unity STF. Thus, the input signal is not processed by any integrator and the loop filter only processes the quantization noise. This has two advantages: 1) op-amp output swings are reduced, 2) the unavoidable nonlinearities of the integrators do not introduce harmonic distortion into the output signal.

### 3.4.1.2 Cascade of resonators with distributed feedback (CRFB) structure

A modification of CIFB structure which implements cascade of resonators instead of integrators thus called CRFB structure is shown in Fig. 3.10. Much better SQNR performance is achieved as NTF zeros are distributed on unit circle producing notches in the signal band and hence creating an inverse Chebyshev filter response.

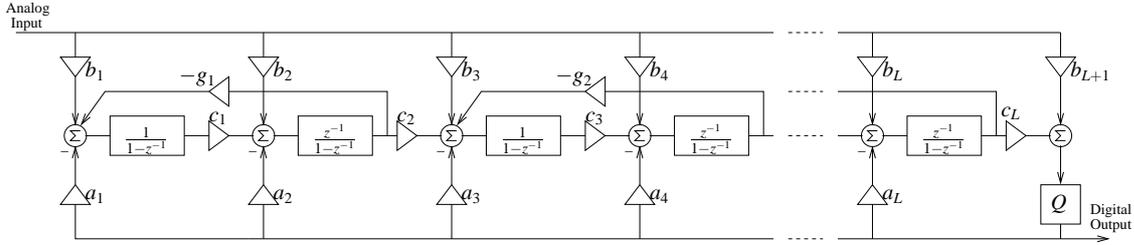


Figure 3.10: Cascade of resonators with distributed feedback (CRFB structure)

If the modulator order is even, the normalized zero frequencies are given by [60]:

$$\omega_i \approx \sqrt{g_i} \quad (3.30)$$

In case of odd-modulator order  $L$ , a plain integrator is used, preferably in the input stage to minimize the input-referred noise contribution from subsequent stages.

All the resonators have one delay-free integrator to ensure that the poles stay on unit circle. In case of switched-capacitor implementations, using a combination of delay-free and delaying integrators increases the speed requirements of the amplifiers used. Therefore delaying integrators only are used for resonators. The poles in such situations fall outside the unit circle. To stabilise the resonators, they are placed in stable feedback system which prevents local oscillations.

### 3.4.1.3 Cascade of integrators with distributed feedforward (CIFF) structure

An alternative procedure to realize the NTF is using feedforward, rather than feedback, signal paths. A topology constructed from cascaded integrators and feedforward branches is shown in Fig. 3.11

The NTF is given by:

$$NTF = \frac{(1 - z^{-1})^L}{D(z)} \quad (3.31)$$

where,

$$D(z) = a_L c_1 c_2 \cdots c_{L-1} z^{-L} + a_{L-1} c_2 c_3 \cdots c_{L-2} z^{-L+1} (1 - z^{-1}) + \cdots + a_1 z^{-1} (1 - z^{-1})^{L-1} + (1 - z^{-1})^L \quad (3.32)$$

An interesting case is,  $b_i = 0$  for all  $i \leq L$  and  $b_1 = b_{L+1} = 1$ . This results in unity STF structure [60], and hence the low-distortion characteristic as discussed for CIFB structure.

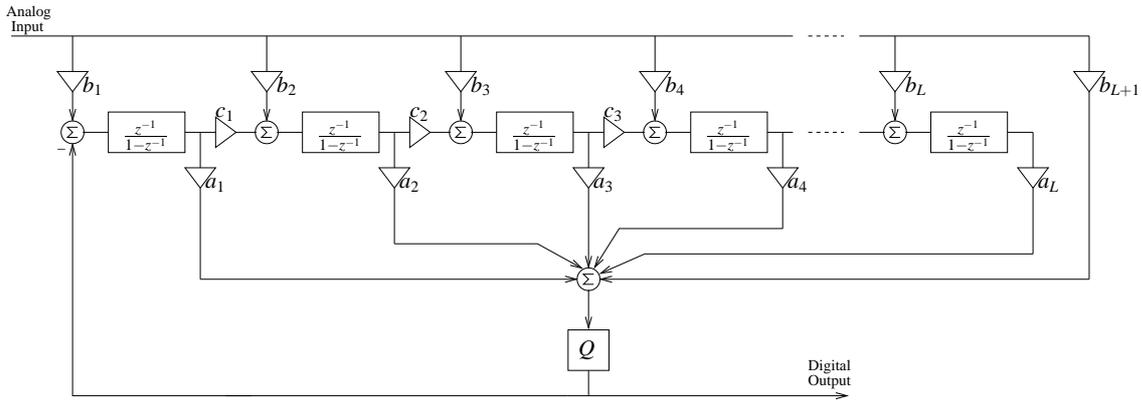


Figure 3.11: Cascade of integrators with distributed feedforward (CIFF structure)

#### 3.4.1.4 Cascade of resonators with distributed feedforward (CRFF) structure

High SQNR version of CIFF is CRFF structure with local feedback loops around integrators. It implements inverse Chebyshev filter response by optimally placing zeros in signal band. Fig. 3.12 illustrates the CRFF topology, where for simplicity only the first and last input weight factors are included, to obtain the low-distortion structure.

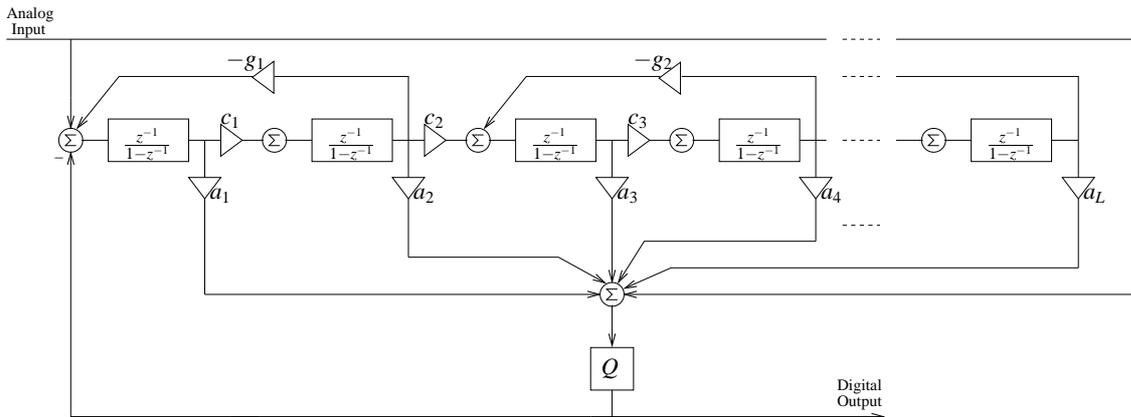


Figure 3.12: Cascade of resonators with distributed feedforward (CRFF structure)

A fifth-order, four-bits internal quantizer CRFF structure with 12.5MHz bandwidth and 14-bits resolution, consuming 200mW is presented in [61].

### 3.4.2 Multi-Stage Modulators

At low values of over-sampling ratio (OSR), it is not possible to obtain high SNR values in a single-quantizer modulator simply by raising the order of the loop filter, since stability considerations limit the permissible input signal amplitude for higher-order loops, which counteracts the improved noise suppression. The SNR can still be increased by using more



approximation of this quantization error. The digital filters  $H1(z)$  and  $H2(z)$  are designed so as to cancel the quantization error of first stage in the output.

### 3.4.3.1 Linear Analysis

From Fig. 3.5, using linear model of the quantizer presented in Section. 3.3.1.1, the output of first-stage modulator is,

$$Y1 = \frac{0.2G1}{D(z)}X + \frac{(1 - z^{-1})^2}{D(z)}E1 \quad (3.33)$$

where  $G1$  is the first-stage quantizer gain and,

$$D(z) = 1 - (2 - 0.4G1)z^{-1} + (1 - 0.2G1)z^{-2}$$

and similarly the output of second-stage modulator is,

$$Y2 = \frac{-G2z^{-1}}{1 - (1 - G2)z^{-1}}E1 + \frac{1 - z^{-1}}{1 - (1 - G2)z^{-1}}E2 \quad (3.34)$$

where  $E1$  is the quantization noise of first-stage and is the input of the second-stage with the polarity reversed, and  $G2$  is the quantizer gain of second-stage.

For a hypothetical case (which is not the optimized case), to simplify the calculations,  $G1 = 4$  and  $G2 = 1$  are employed to determine the quantization error cancellation filters  $H1(z)$  and  $H2(z)$ . With these values of quantizer gains, Eqns. 3.33 and 3.34 become:

$$Y1 = X + (1 - z^{-1})^2E1$$

$$Y2 = -z^{-1}E1 + (1 + z^{-1})E2 \quad (3.35)$$

Now solving the equation,

$$Y1 \cdot H1 + Y2 \cdot H2 = z^{-1}X + (1 - z^{-1})^3E2 \quad (3.36)$$

leads to very simple digital filters,

$$H1 = z^{-1}$$

and,

$$H2 = (1 + z^{-1})^2$$

Fig. 3.14 illustrates the SQNR performance of 2-1 cascade structure with the cancellation filters and quantizer gains as discussed above, and compares it to the ideal third-order modulator response. It shows that the cascade modulator follows well the ideal curve in low input region, but starts to become unstable near -10dBFS.

The problem associated with MASH structures is that there is a high level of matching needed between analog coefficients and digital filters. In case of any mismatch, the SNDR performance is degraded. From fabrication point of view, digital filters are quite precise

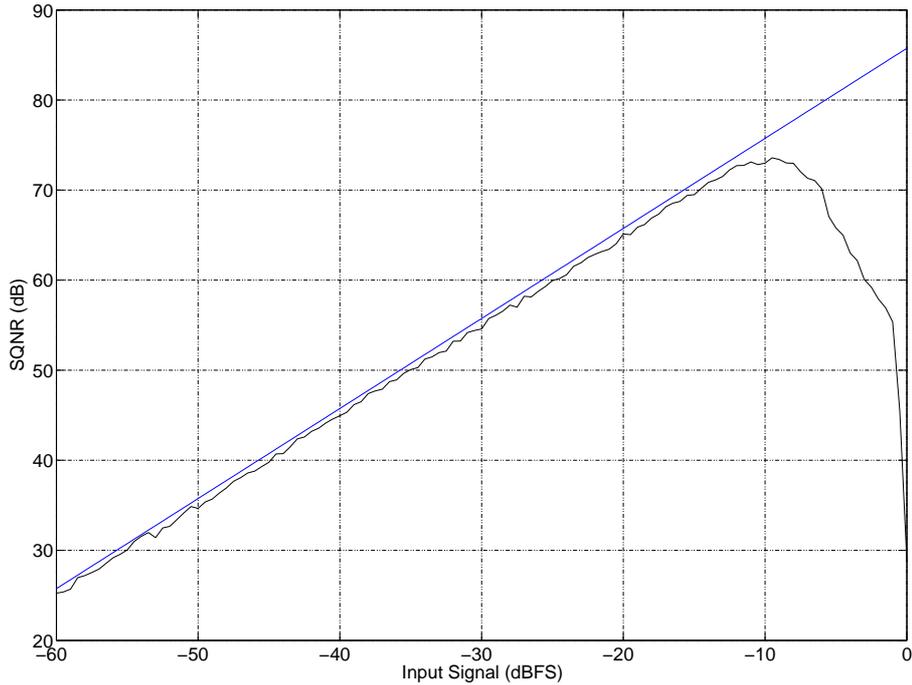


Figure 3.14: SQNR performance of classic cascade 2-1  $\Delta\Sigma$  modulator structure

while there is a degree of inaccuracy involved in analog coefficients implementation. To give an idea of performance degradation, we perform monte-carlo simulation of the cascade 2-1 structure by varying the analog coefficients and fixing the digital filters. The 8192 points monte-carlo simulation has been carried out by varying all the coefficients with an standard deviation of 1%. The input signal is set at -8dBFS. The histogram of the resulting output is shown in Fig. 4.22, it has a mean of 72.8dB and an standard deviation of 0.5dB.

Analog coefficients' inaccuracy is a direct consequence of the capacitor ratio mismatch in the circuit. Other analog imperfections that change the NTF and STF of individual MASH stages and consequently result in leakage of the quantisation due to the mismatch of digital filters with analog circuits are finite dc-gain, finite GBW product and finite SR of the amplifiers. Adaptive digital correction of these analog errors is a widely investigated area. This adaptive calibration can be carried out off-line [18], on-line [19, 20, 21, 22, 23] or by test-signal injection [24]. All of these techniques come at the price of increased circuit complexity and power consumption.

### 3.4.4 Advanced MASH Structures

The problem of mismatch between analog components and digital filters in traditional MASH structures due to nonidealities has led to the new generation of MASH structures which are free from quantization noise cancellation filters. This has two advantages, 1) the circuit complexity reduces and 2) the modulator becomes less sensitive to analog circuitry imperfections thereby enhancing the circuit robustness. The first cascade architecture of

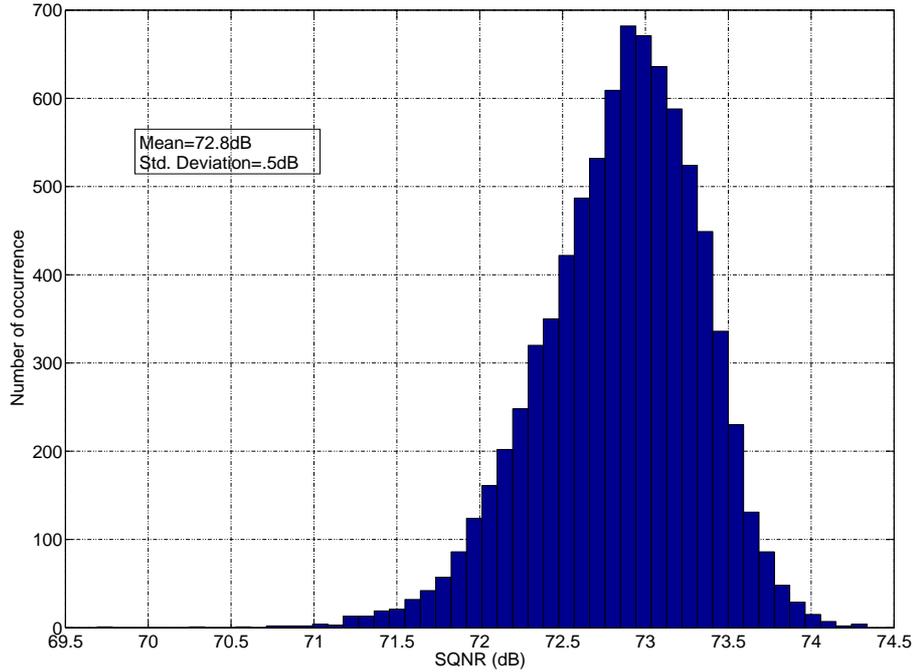


Figure 3.15: Classic cascade 2-1 architecture's sensibility to analog and digital components' mismatches

this nature is presented in [25]. This structure is called multi-stage closed loop (MSCL). Every stage in this structure is a single-order modulator and a global feedback is introduced from the output, which is the sum of the output of all comparators. An enhanced version of this structure is Generalized multi-stage closed loop (GMSCL) [15, 16]. This is basically a cascade 2-2 structure, with each stage implemented as a feedforward structure, and a global feedback is used from the output. This structure is shown in Fig. 3.16.

Another such type of architecture is Sturdy MASH  $\Delta\Sigma$  modulator presented in [17] and illustrated in Fig. 3.17.

Like GMSCL structure, the SMASH structure is less sensitive to opamp gain and coefficient errors than the traditional MASH structure: finite opamp gain and coefficient mismatch will affect the zeros of the overall NTF, and the error will be suppressed by the second loop. This is because both STF and NTF are achieved by means of fully analog components, in contrast with the traditional MASH structure in which digital filters form the overall noise transfer function.

### 3.5 Multibit Modulators

With the expression for DR of an ideal  $L$ th-order,  $B$ -bits internal quantizer  $\Delta\Sigma$  modulator given by:

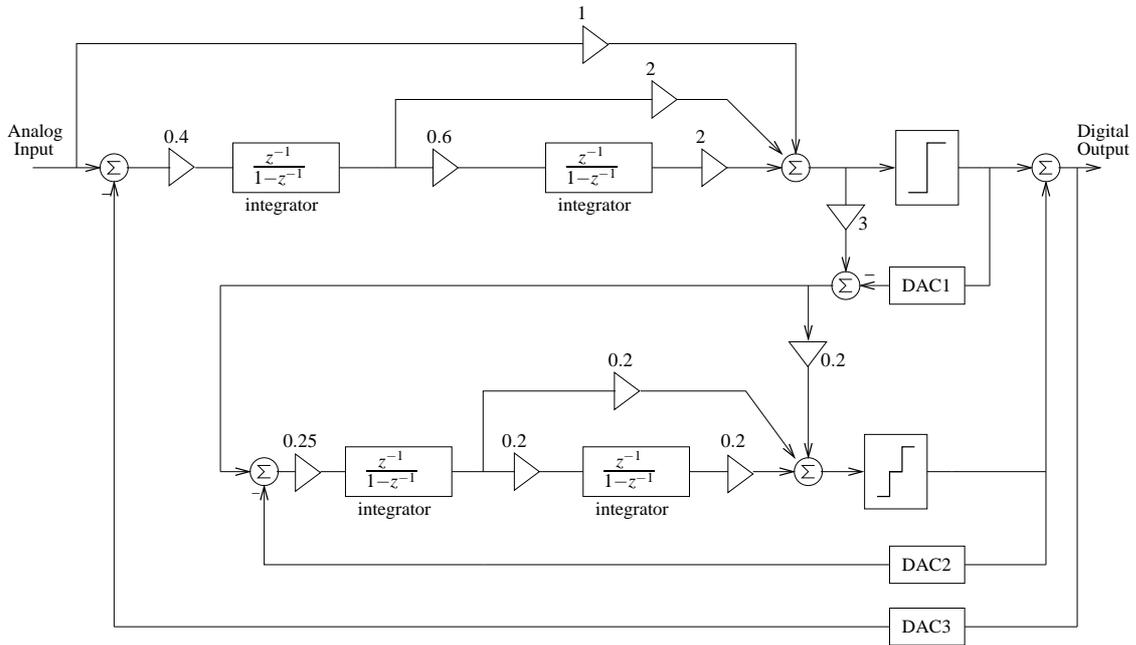


Figure 3.16: Generalized multi-stage closed loop (GMSCL)

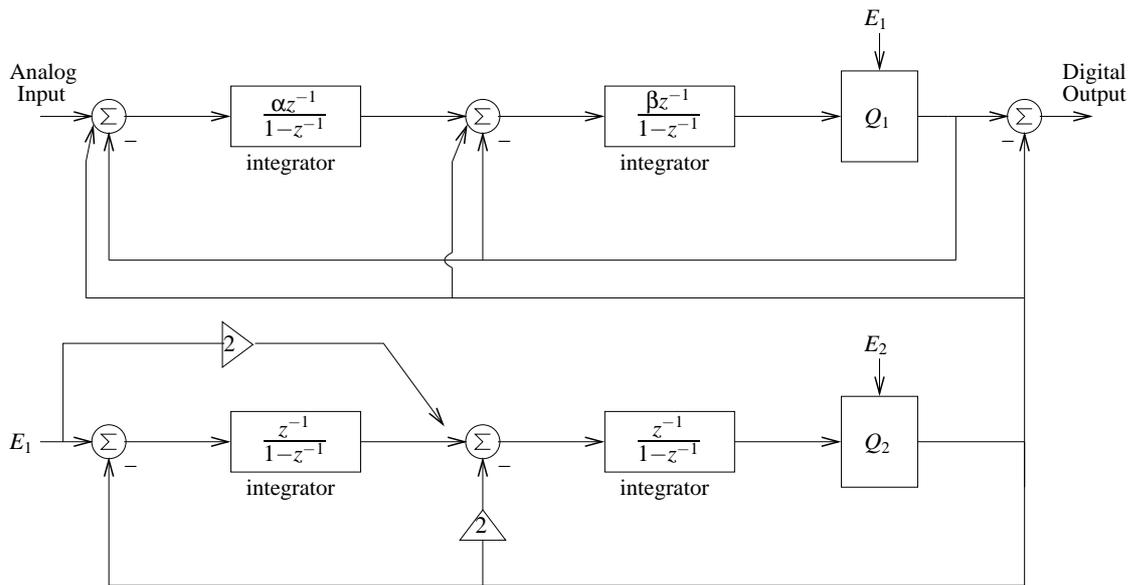


Figure 3.17: Sturdy MASH (SMASH) structure

$$DR(dB) \approx 10 \log_{10} \left[ \frac{3}{2} \frac{(2L+1)}{\pi^{2L}} OSR^{2L+1} (2^B - 1)^2 \right] \quad (3.37)$$

it can be deduced that with each additional bit in the quantizer, 6dB of DR (equivalent to 1-bit resolution) is gained. Another advantage is the stable operation of the modulator for an increased range of signal levels [60]. As a general rule, the lower the resolution of the quantizer used, the more suspicious the designer should be about instability. There are two principal disadvantages of multibit quantizers: 1) The quantizer is realized generally by flash ADC, whose complexity increases exponentially with the number of bits. Hence this number can seldom exceed 4 or 5. 2) The nonlinearities caused by uneven spacings of the DAC levels degrade the SNDR performance of the system. The filtering of these nonlinearities is a highly researched domain, so a number of techniques have been proposed in the literature to counter them. These techniques can be broadly classified into analog corrections and digital calibrations. In the analog domain, the most commonly used ones are element rotation (also called data-weighted averaging) [63, 64], individual level averaging [65], vector based mismatch shaping [66] and tree-structure element selection [67]. All these techniques use the unit-element DAC structure [60], but each uses a different strategy for the selection of the unit elements for a given digital input code. These techniques flatten the nonlinearity of the multibit DAC into a pseudo-random noise and perform noise-shaping to reduce in-band noise power. Since these schemes rely on oversampling and noise shaping, they are ineffective for low values of OSR, which is the case for wideband converters. Digital calibration techniques, on the other hand, acquire the DAC errors in a digital form, and then nullify their effects in the digital domain. These corrections can be made just once at the power up of the circuit [68], or they can be run as a background process during normal operation [69]. It can be noted that a multibit quantizer can be used in the second stage of a MASH structure without the need for any correction of its DAC nonlinearity [70]. This is due to the fact that the second-stage output comprising its DAC nonlinearity is multiplied by the NTF of first stage in the form of digital filter  $H_2(z)$ . Since this filter has a highpass characteristic, the nonlinearity error of the second-stage DAC is suppressed in the baseband. Another reason for insensitivity of MASH structure to second-stage DAC nonlinearity is that this stage processes only the quantization noise of the first stage. And hence DAC nonlinearity of this stage does not generate any signal harmonic distortion, but only adds small noise, which is usually tolerable.

### 3.6 Continuous Time and Hybrid (Continuous Time/Discrete Time) Modulators

The initial implementations of  $\Delta\Sigma$  modulators used continuous-time (CT) loop filters [71], but with the advent of SC circuits, the focus has been shifted to DT loop filters. SC circuits are attractive because they exhibit good accuracy and good linearity. In addition, the difference equations which describe an SC circuit are independent of the clock rate, and hence the transfer function of an SC circuit scales naturally with the clock frequency. In contrast, CT filters generally have inferior linearity and accuracy. The time-constants of a CT filter are subject to large variation and furthermore do not track the clock rate. Consequently, the time-constants of a CT loop filter typically require calibration and that calibration is only valid for a single clock frequency. In addition, CT implementations are

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highly sensitive to the clock jitter. Despite these disadvantages, the CT implementations of  $\Delta\Sigma$  modulator are gaining increasing interest for two important reasons:

1. CT modulators possess inherent anti-aliasing, with the degree of alias suppression equivalent to the the degree of quantization-noise suppression [60]. Inherent anti-aliasing simplifies system design by eliminating the anti-alias filter, which typically must precede DT implementations. Inherent anti-aliasing also improves system performance, since it also eliminates the noise-folding associated with sampling the input signal. By using CT loop filter, the sampling of the signal takes place at the output of the filter in contrast to the DT loop filter where sampling is done at the input of the filter. Thus, imperfections of the sampling process, and the folding of the wideband noise, both take place at a much less sensitive point in the loop.
2. The theoretical limit on the clock rate of a CT modulator is determined by the regeneration time of the quantizer and the update rate of the feedback DAC, whereas in an SC modulator the clock rate is limited by the opamp settling requirements to about 25%  $\rightarrow$  30% of the unity-gain frequency  $f_u$  of the amplifiers within it. In practice, a CT modulator can operate with a clock frequency (and thus achieve a signal bandwidth) which is 2-4 times greater than that which can be achieved with SC techniques, but with a lower linearity and accuracy. The reason for this increased bandwidth is that the settling error in an SC stage depends exponentially on the  $f_u/F_s$  ratio, and hence the error grows rapidly when this ratio drops below about 4. By contrast, the error introduced by opamp bandwidth in a CT modulator increases only gradually when  $f_u/F_s$  is reduced. Recent CT modulators have achieved bandwidths of 10 MHz in 0.18-  $\mu\text{m}$  CMOS technology [72], [73] and 15 MHz [74] and 20 MHz [75] in 0.13- $\mu\text{m}$  CMOS technology, all with a resolution of 11 bits or more. These results suggest that CT implementations are capable of operating at signal bandwidths difficult to achieve with DT designs while still maintaining a high resolution.

These two advantages are driving the fresh interest for CT  $\Delta\Sigma$  modulators with bandwidths in the multi-MHz range. Some recent publications are using hybrid CT/DT solutions for A/D conversion that combine the benefits of CT and DT circuits, while minimizing the problems associated with CT design. The hybrid solution presented in [76] uses cascade 2-1 architecture shown in Fig. 3.18, where the second-order first stage is implemented in CT, while the first-order second stage is a DT circuit.

The first-stage is implemented completely as CT circuit to achieve the maximum anti-aliasing benefit of CT operation and to minimize the settling requirements for the first-stage sampling circuit. However, the second stage of the proposed cascaded modulator can be implemented as either a CT or a DT modulator without affecting noise shaping of the first-stage sampling error. Furthermore, because the output of the CT first stage is already a sampled-data signal, the antialiasing performance of the overall modulator is the same for either a CT or DT second-stage implementation. Although a CT second stage would provide the benefits of CT design, including slower, lower power amplifiers and improved attenuation of second-stage sampling errors, there are several disadvantages to a

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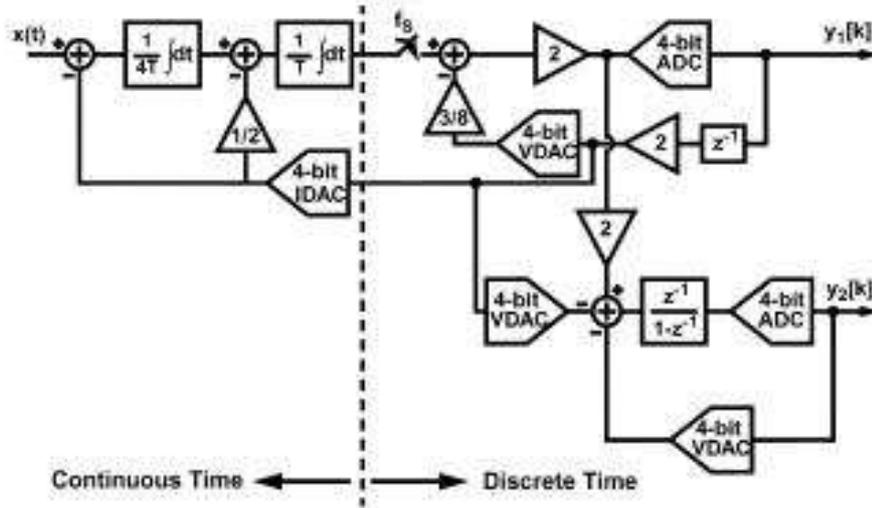


Figure 3.18: Hybrid (CT/DT)  $\Delta\Sigma$  modulator [76]

CT second stage. The first-stage sampling circuit would see a resistive input, requiring a low-output-impedance stage for the sampling circuit amplifier. Because this circuit is a SC circuit operating at a high sampling rate, the first-stage sampling circuit amplifier must be a fast single-stage design, and therefore driving a resistive load would be difficult. A CT second stage would also require an additional feedback path to stabilize the loop against excess loop delay, adding to the implementation complexity. Moreover, the extra stabilizing path would require an additional summing junction at the input of the quantizer, which would necessitate another amplifier and active sampling. This amplifier would operate as a DT circuit, negating the low-power amplifier benefit of a CT design. Because a CT implementation of the second stage would likely require an additional sampling amplifier, a DT second stage implementation will dissipate approximately the same power as a CT implementation. Furthermore, the first-stage sampling circuit driving a DT second stage will see a capacitive, rather than resistive, load when driving a DT second stage. Although the DT integrator amplifier will suffer incomplete settling because of the high sampling rate targeted in this research, those errors will be shaped by the second-order first stage, mitigating their impact on the overall modulator performance. For these reasons, and because a DT second stage would not affect the anti-aliasing performance of the modulator, a DT implementation was identified as the lowest power option for the second stage of the modulator.

### 3.7 System Level Modeling

System level modeling helps in determining the specifications of fundamental building blocks of  $\Delta\Sigma$  modulator. It is the first step in the design of analog integrated circuits. Based on the results of system level modeling, a transistor-level design using sophisticated tools like Cadence design suite is undertaken. For the purpose of system level modeling,

the classic Boser structure [12] is chosen. In this section, modeling is performed for clock jitter, switches' thermal noise and opamp noise. Modeling at the level of opamp includes saturation, finite dc-gain, finite gain-bandwidth product and slew rate. Comparator non-idealities of dc-offset and hysteresis are also taken into account.

### 3.7.1 Clock Jitter

The operation of an SC circuit depends on complete charge transfers during each of the clock phases [77]. Once the analog signal has been sampled, the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of clock jitter on an SC circuit is completely described by computing its effect on the sampling of the input signal. This also means that the effect of clock jitter on a modulator is independent of the structure or order of the modulator. Clock jitter results in a nonuniform sampling time sequence, and produces an error which increases the total error power at the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the modulator input signal. The error introduced when a sinusoidal signal with amplitude  $A$  and frequency  $f_{in}$  is sampled at an instant which is in error by an amount  $\delta$  is given by:

$$x(t + \delta) - x(t) \approx 2\pi f_{in} \delta A \cos(2\pi f_{in} t) = \delta \frac{d}{dt} x(t) \quad (3.38)$$

This effect is simulated at behavioral level by taking the input sample at an instant which differs from the ideal instant by  $\delta$ :

$$x[n] = x(nT_s + \delta) \quad (3.39)$$

In the model, it is assumed that the sampling uncertainty  $\delta$  is a Gaussian random process with standard deviation  $\Delta\tau$ . Whether oversampling is helpful in reducing the error introduced by the jitter depends on the nature of the jitter. Since we assume the jitter white, the resultant error has uniform power-spectral density (PSD) from 0 to  $F_s/2$ , with a total power of  $(2\pi f_{in} \Delta\tau A)^2/2$ . In this case, the total error power will be reduced by the oversampling ratio [12].

### 3.7.2 Switch and Op-Amp Noise

The most important noise sources affecting the operation of an SC  $\Delta\Sigma$  modulator are the thermal noise associated to the sampling switches and the intrinsic noise of the operational amplifiers. These effects can be successfully simulated at the behavioral level by using the model of a “noisy” integrator [78] shown in Fig. 3.19. It includes the thermal noise of the switches and op-amp noise. Each noise source and its relevant model will be described in the following paragraphs.

#### 3.7.2.1 Switch Thermal Noise

Thermal noise is caused by the random fluctuation of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band, limited

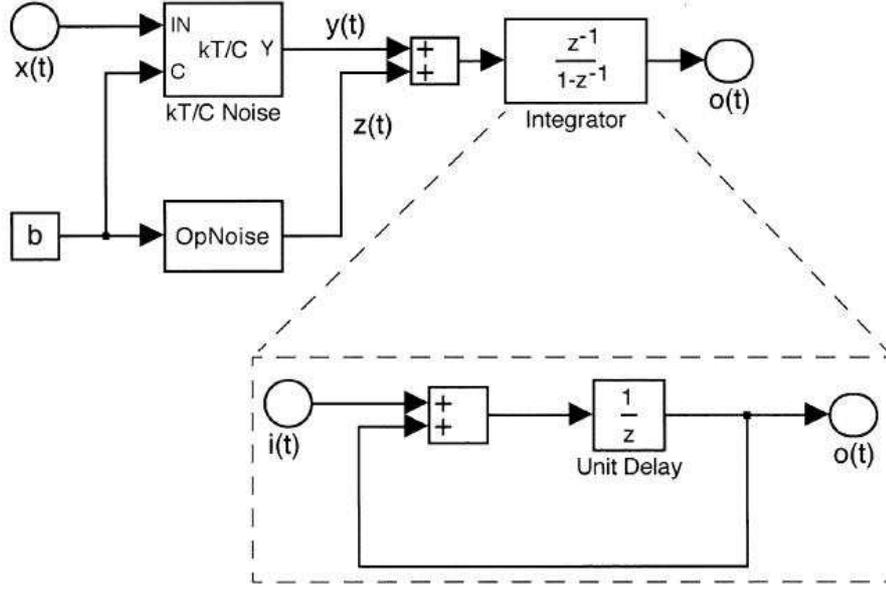


Figure 3.19: Noisy integrator model [78]

only by the time constant of the switched capacitors or the bandwidth of the operational amplifiers. Referring to the SC implementation of integrator shown in Fig. 3.22, the sampling capacitor  $C_s$  is in series with a switch, with finite resistance  $R_{on}$ , that periodically opens, thus sampling a noise voltage onto  $C_s$ .

The total noise power can be found by evaluating the integral [10]:

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1 + (2\pi f R_{on} C_s)^2} df = \frac{kT}{C_s} \quad (3.40)$$

where  $k$  is the Boltzmann's constant,  $T$  the absolute temperature, and  $4kTR_{on}$  the noise power spectral density associated with the switch on-resistance. The switch thermal noise voltage  $e_T$  (usually called  $kT/C$  noise) is then superimposed to the input voltage  $x(t)$  leading to

$$\begin{aligned} y(t) &= [x(t) + e_T(t)] b \\ &= \left[ x(t) + \sqrt{\frac{kT}{C_s}} n(t) \right] b \end{aligned} \quad (3.41)$$

where  $n(t)$  denotes a Gaussian random process with unity standard deviation and  $b = C_s/C_i$  is the coefficient of the integrator. The integrators or resonators of an SC  $\Delta\Sigma$  modulator may include more than one SC input branch, each contributing to the total noise power. Each branch has to be modeled with a separate noise source.

### 3.7.2.2 Op-amp Noise

The total noise voltage of the operational amplifier referred to the integrator input can be modelled as an additive gaussian noise. In this model, only thermal noise is considered, while flicker noise and dc offset are neglected. Indeed, in low-pass modulators, flicker noise and dc offset are typically canceled by means of auto-zero, correlated double sampling, or chopper stabilization techniques, while they are not important in highpass or bandpass architectures. The noise power can be evaluated through a transistor-level noise simulation of the complete integrator in the proper clock phase, including feedback, sampling and load capacitors. The resulting output referred noise PSD has to be integrated over the whole frequency spectrum, eventually taking into account the degradation of the thermal noise PSD introduced by the auto-zero or correlated double sampling techniques [79], and then divided by  $b^2$  in order to refer the obtained noise power to the integrator input; where  $b$  is the integrator gain. It is important to note that only the contribution of the sampled noise is considered, assuming that no continuous-time paths are present across the modulator (this is typically the case in SC modulators due to the presence of a latched quantizer).

### 3.7.3 Op-amp Non-Idealities

The  $\Delta\Sigma$  modulator operation depends on the performance of integrators, which can be considered as its major building blocks. The integrators are in turn dependent on the functioning of their own building blocks i.e op-amps. Operational amplifiers' non-idealities including finite and nonlinear dc-gain, finite gain-bandwidth product (GBW) and finite slew rate (SR) cause incomplete transfer of charge in the switched-capacitor (SC) implementation of integrators which is a major cause of performance degradation of  $\Delta\Sigma$  modulators. Several articles in the literature have discussed these effects and established their behavioural models to study their effect on integrators [80, 78, 81], which form the basis of traditional low-pass  $\Delta\Sigma$  modulators. We will discuss each non-ideality separately in the following sections.

#### 3.7.3.1 Saturation

Saturation of an opamp output is due to the limited voltage swing that it can provide. In the latest CMOS technologies, small values of voltage supplies make the opamp output voltage swing very limited. Excessive output excursions of integrators are undesirable because of saturation or voltage clipping at the output of op-amps comprising integrators; if the output voltage exceeds opamp's output voltage swing, the clipping occurs which may also render the system unstable. Small output excursions of integrators are desirable also because they minimize the opamp output swing requirement resulting in the design of an opamp with good values of other performance parameters like gain, bandwidth and consumption. If an integrator has an output range which exceeds the quantization step, it will overload the comparator and render the system unstable. Thus output excursion is an important parameter to measure at system level. System level simulations have been carried out using MATLAB to study the output excursions of both integrators in Boser modulator. Ten sets of  $1.1 \times 2^{14} = 18022$  point simulations with each set at a random

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integrator initial state, have been carried out. The first 1638 points have been truncated to remove the transient effects. The ten sets of histograms of have been averaged for final results. The input signal is a sinusoid with an amplitude of 0.4 normalized with respect to quantization step i-e -8dBFS (dB with reference to full scale). The system level simulations have been performed with sampling frequency normalized to one and input signal frequency of  $0.5 - 6.7139e - 4 = 0.4993$ .

The histogram showing the output excursions of two integrators are presented in Fig. 3.20

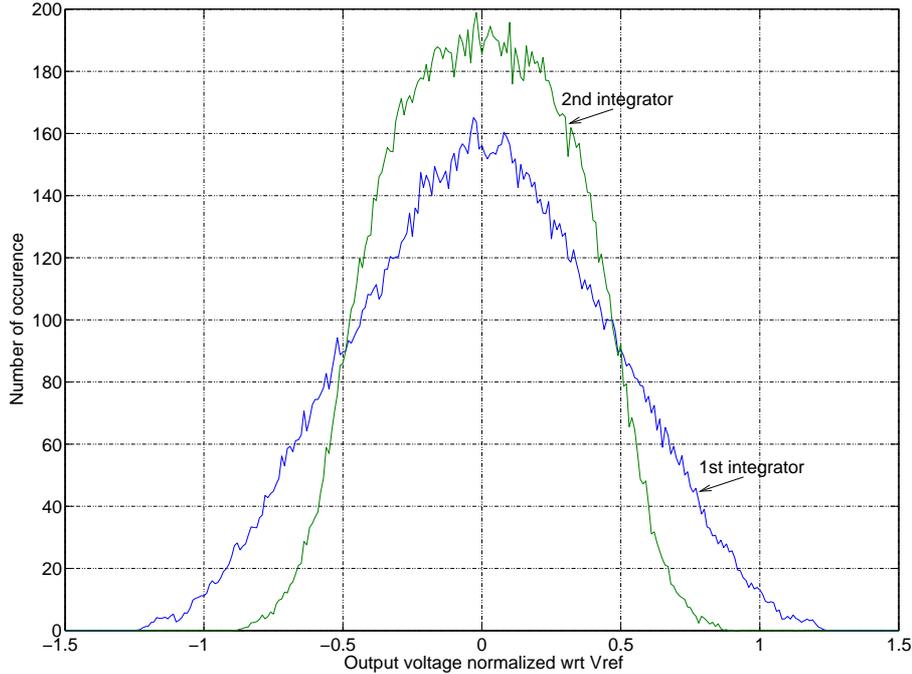


Figure 3.20: Integrators' output excursion at  $V_{in}=-8\text{dBFS}$

The results presented in Fig. 3.20 show that the output excursions are more significant in the first integrator, which is expected since it processes the difference of the useful signal and the quantization noise directly; unlike the second integrator which processes the signal after it has undergone an attenuation equal to the first integrator's coefficient. The saturations voltage of operational amplifier is normally set by quantization step i-e the voltage range  $-V_{ref} \leftrightarrow V_{ref}$ , but since first integrator's excursion exceeds this range, we have to design opamps with higher voltage swings, thus increase the power consumption, which can become significant in low-voltage technologies.

The second integrator's excursion is less than the first one, and well inside the quantization step and is thus easily realized.

From another point of view, simulations to model the op-amp saturation have been performed by clipping the integrator output at  $\pm V_{ref}$ . That is any output greater than  $V_{ref}$  has been forced to be at  $V_{ref}$  and any output less than  $-V_{ref}$  has been forced to be at  $-V_{ref}$ . The resulting simulation result is shown in Fig. 3.21:

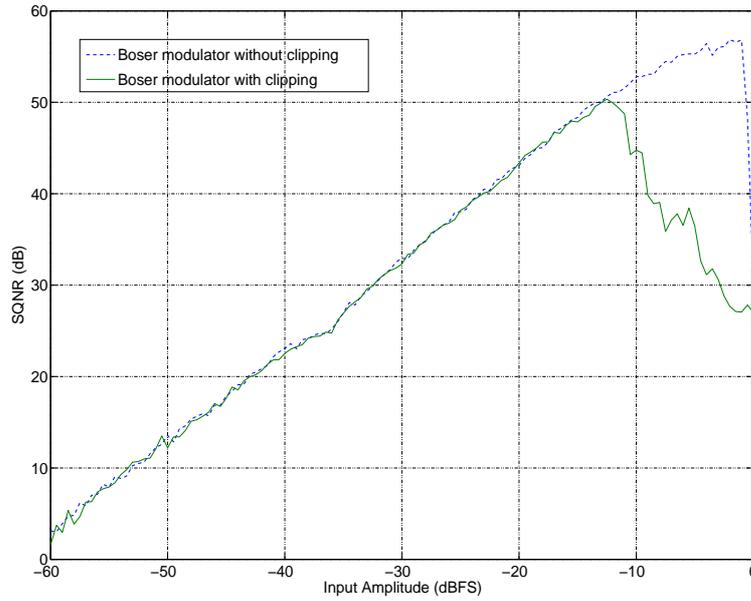


Figure 3.21: Plot of SNR Vs Input Signal in the presence of filter clipping at  $\pm V_{ref}$

As expected, the structure is affected by output saturation since it has large excursions. As we increase the input sinusoid amplitude, the output excursion becomes larger and larger and at one point becomes unstable because of clipping. Thus the first opamp has to be designed with voltage swing higher than  $\pm V_{ref}$  to achieve a good SQNR performance.

### 3.7.3.2 Finite DC-Gain

An ideal delayed integrator with a gain  $b$  is described by  $z$ -domain transfer function:

$$H_{ideal}(z) = b \frac{z^{-1}}{1 - z^{-1}} \quad (3.42)$$

Although delay-less filters can be used to realize the desirable NTF, most often delayed-integrators are used in the first stage of the modulators as they are easily implemented in SC design. The operational amplifier finite open-loop dc-gain  $A_O$  introduces errors in this ideal transfer function. This effect can be represented mathematically by:

$$H_{practical}(z) = b \frac{\alpha z^{-1}}{1 - \beta z^{-1}} \quad (3.43)$$

where  $\alpha$  and  $\beta$  are less-than-unity quantities and represent gain degradation and filter leakage (or gain and pole location perturbation) respectively. Gain degradation results in only a fraction of the input signal being added to the output and filter leakage results in only a fraction of the last output being added to the input.

To work out the values of  $\alpha$  and  $\beta$ , let us take the standard SC implementation of integrator illustrated in Fig. 3.22:

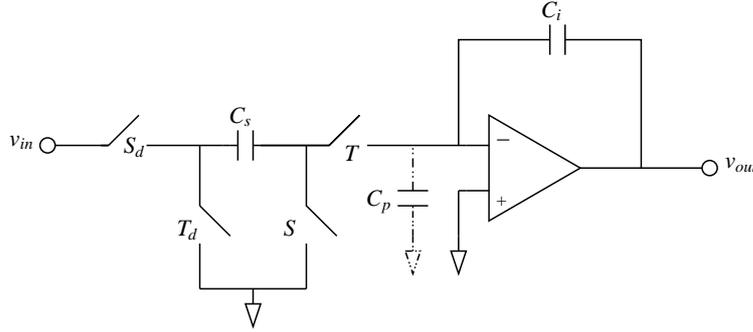


Figure 3.22: Integrator implementation in a SC circuit

Where  $C_p$  represents the input parasitic capacitance of the op-amp, parasitic capacitance of the switches and the plates of capacitors connected to the negative input of the op-amp. Solving charge-transfer equations for this filter, keeping in view the charge-conservation law, the practical transfer function in terms of capacitances and op-amp dc-gain  $A_0$  is given by:

$$H_{practical}(z) = \frac{C_s}{C_i} \frac{\frac{A_0}{\frac{C_s}{C_i} + \frac{C_p}{C_i} + A_0 + 1} z^{-1}}{1 - \frac{\frac{C_p}{C_i} + A_0 + 1}{\frac{C_s}{C_i} + \frac{C_p}{C_i} + A_0 + 1} z^{-1}} \quad (3.44)$$

where  $\frac{C_s}{C_i} = b$  is the gain of the filter and  $\frac{C_p}{C_i} = p$  is the gain of the parasitic voltage. Replacing these values in Eqn. 3.44:

$$H_{practical}(z) = b \frac{\frac{A_0}{b+p+A_0+1} z^{-1}}{1 - \frac{p+A_0+1}{b+p+A_0+1} z^{-1}} \quad (3.45)$$

The value of  $b$  for the Boser modulator is 0.5, assuming a reasonable value of 0.01 for  $p$ , the exact transfer function of the first integrator turns out to be:

$$H_{practical}(z) = 0.5 \frac{\frac{A_0}{A_0+1.51} z^{-1}}{1 - \frac{A_0+1.01}{A_0+1.51} z^{-1}} \quad (3.46)$$

Therefore the values of  $\alpha$  and  $\beta$  are given by:

$$\alpha = \frac{A_0}{A_0 + 1.51}, \quad \beta = \frac{A_0 + 1.01}{A_0 + 1.51} \quad (3.47)$$

Using Eqn. 3.46 as the transfer function for the first integrator, the Boser modulator is simulated at a range of values of  $A_0$  to identify the effect of this non-ideality. The input signal is a sinusoid at an amplitude of 0.4 normalized with respect to quantization step i.e -8dBFS at frequency of  $0.4993fs$ . The simulation result is shown in Fig. 3.23:

This figure shows that the Boser architecture requires the 40dB op-amp dc-gain to attain the ideal SQNR performance.

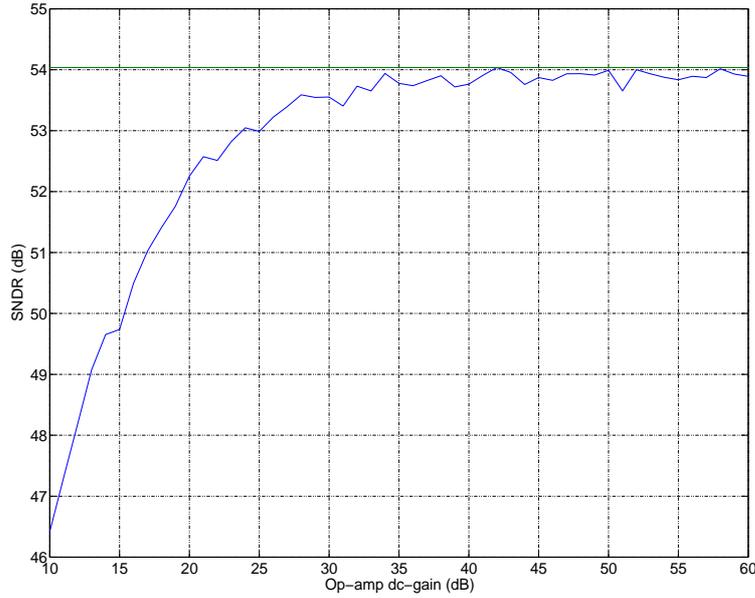


Figure 3.23: SNR vs. Op-Amp DC-Gain

### 3.7.3.3 Finite Gain-Bandwidth Product and Slew Rate

Finite Gain-Bandwidth Product (GBW) and Slew Rate (SR) are responsible for incomplete or inaccurate charge transfer in SC circuits. In the case of integrator, finite GBW of the op-amp forces only a fixed fraction of the new charge in each charge transfer phase of the clock ( $T$ ) to get stored in the integrating capacitor of the filter. This is due to the non-zero time constant,  $\tau = (1 + b)/2\pi GBW$  as derived in Annex. A. The fact that in each clock cycle there is a charge transfer error which is proportional to the input of the filter, results in distortion at the output of the modulator. With the assumption of a single-pole model for the op-amp, the output transient of the integrator during  $n$ th integration phase is represented by:

$$v_{out}(t) = \beta v_{out}(nT_s - T_s) + b\alpha v_{in}(1 - e^{-\frac{t}{\tau}}), \quad 0 < t < \frac{T_s}{2} \quad (3.48)$$

where  $v_{out}$  is the output of the integrator,  $T_s = 1/F_s$  is the sampling period,  $v_{in}$  is the input of the integrator and  $\tau$  is the time constant of the op-amp which makes up the integrator. If this integrator represents the first integrator of the Bosser modulator,  $v_{in}$  is given by:

$$v_{in} = x(nT_s - T_s/2) - y(nT_s - T_s) \quad (3.49)$$

where  $x$  is the input of the modulator and  $y$  is the output of the modulator. In case of infinite GBW of the op-amp,  $\tau$  falls to zero and Eqn. 3.48 reduces to Eqn. 3.43, while the values of  $\alpha$  and  $\beta$  are given by Eqn. 3.47. Finite GBW on the other hand, reduces

the gain of the filter which in turn reduces the value of the new input to be added to the output.

Slew rate of an op-amp is the maximum rate of voltage change that it can provide at its output. Unfortunately it is practically a finite quantity that is dependant on the bias current of the op-amp and its load capacitance:

$$SR_s = \frac{I_{max}}{C_L} \quad (3.50)$$

where  $I_{max}$  is the maximum current that can be supplied by the op-amp and is equivalent to twice the bias current of a single branch of a differential implementation.  $C_L$  is the load capacitance on the op-amp during the integration phase and is composed of all the capacitances connected to the op-amp during this phase. Eqn. 3.50 can be called the SR-supply by the op-amp. SR-demand on the other hand is characterised by maximum slope of the curve drawn by charge transfer eqn. 3.48. This curve finds its maximum slope at  $t = 0$ , given by:

$$SR_d = \frac{d}{dt}v_{out}(t)|_{max} = \frac{b\alpha v_{in}}{\tau} \quad (3.51)$$

Now, two possibilities arise because of this supply and demand issue:

1. The value of SR-demand given by Eqn. 3.51 is lower than the value of SR-supply of the op-amp given by Eqn. 3.50. In this case, there is no SR limitation and the charge transfer continues to function as specified by Eqn. 3.48 during the whole integration phase (until  $t = T_s/2$ )
2. The second possibility is that the SR-demand of the charge transient exceeds the SR-supply of op-amp. In this case, the op-amp undergoes slewing and provides a linear charge transfer in contrast to the exponential charge transfer given in Eqn. 3.48. It continues to supply constant current equivalent to its maximum current until the current demand becomes lower than its maximum current ( $t < t_0$ ). This corresponds to a linear voltage change curve (having a constant slope). This maximum slope is the SR-supply of the op-amp. This concept is illustrated graphically in Fig. 3.24.

The charge transfer transient can now be represented by Eqns:

$$v_{out}(t) = \beta v_{out}(nT_s - T_s) + SR_s t, \quad t \leq t_0 \quad (3.52)$$

$$v_{out}(t) = \beta v_{out}(nT_s - T_s) + (b\alpha v_{in} - SR_s t_0) * (1 - e^{-\frac{t-t_0}{\tau}}), \quad t > t_0 \quad (3.53)$$

where  $SR_s t_0$  is the value reached by  $v_{out}(t)$  at  $t = t_0$  where the limitation of SR ends i-e  $SR_d$  equals  $SR_s$ .

Imposing the condition for the continuity of the derivatives of Eqns. 3.52-3.53 in  $t_0$ , we obtain:

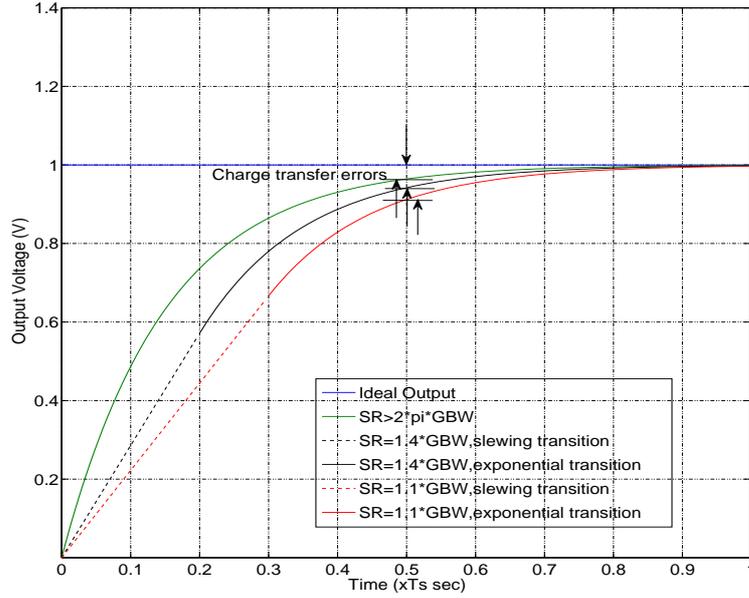


Figure 3.24: Increase in settling error due to slew rate reduction

$$t_0 = \frac{b\alpha v_{in}}{SR_s} - \tau \quad (3.54)$$

If  $t_0 > T_s/2$  Eqn. 3.52 holds for the whole clock period. Otherwise, using the value of  $t_0$  from Eqn. 3.54 in Eqn. 3.53, we obtain:

$$v_{out}(t) = \beta v_{out}(nT_s - T_s) + V_s - \text{sgn}(V_s)SR_s\tau e^{-\left(\frac{T_s}{2\tau} - \frac{|V_s|}{SR_s\tau} + 1\right)} \quad (3.55)$$

where  $V_s$  is given by:

$$V_s = b\alpha v_{in} \quad (3.56)$$

Finite SR supplied by the op-amp results in changing the gain of the integrator in a non-linear fashion and produces harmonics in the output degrading the SNDR. Simulations have been performed for Boser architecture by varying the values of  $SR_s$  and observing the output SNDR at two different values of GBW. The result is illustrated in Fig. 3.25.

The results show that atleast a  $SR_s$  of  $1.8F_s(V/sec)$  is necessary to guarantee the optimum SNDR.

### 3.7.4 Comparator Non-Idealities

The effect of the comparator non-idealities in the operation of the  $\Delta\Sigma$  modulators is much lower than those of the integrator because of the position that the comparator occupies in the modulator loop. A possible input offset in the comparator when referred to the modulator input is attenuated by the DC gains of the integrators that precede it in the loop.

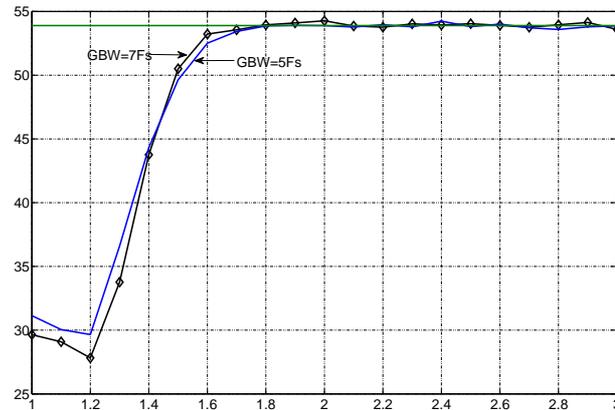


Figure 3.25: SNDR degradation for Boser structure as a function of op-amp SR

Therefore, with the increase in modulator order  $L$ , the modulator becomes increasingly insensitive to such an error. The impact of dc-offset at the comparator input on the performance of Boser structure is demonstrated in Fig. 3.26. It can be deduced that this structure is insensitive to comparator dc-offset.

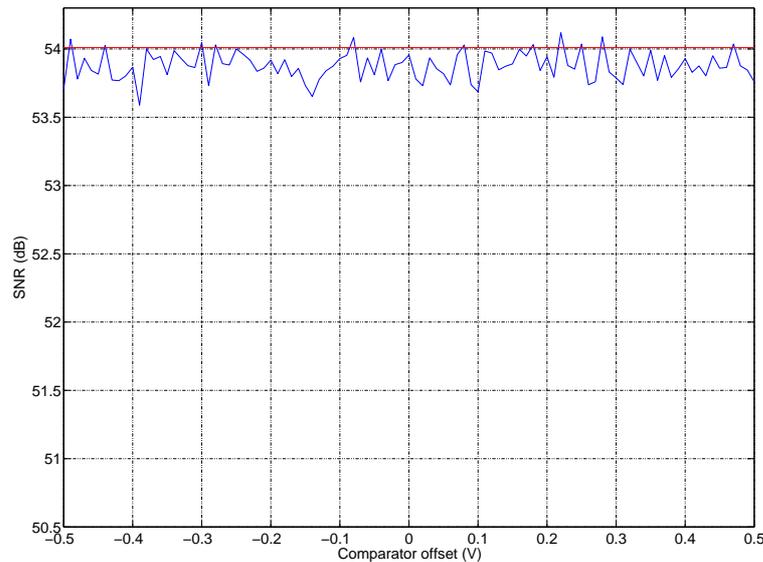


Figure 3.26: Offset effect on the Boser structure

The other comparator non-ideality is hysteresis. Its error is shaped in the same manner as quantization noise. Hysteresis leads to a loss of resolution because the signals next to the comparison threshold experience a resistance to change the output state even when the signal level may have surpassed such a threshold. This phenomenon exists in both state

changes generating a hysteresis cycle as illustrated in Fig. 3.27.

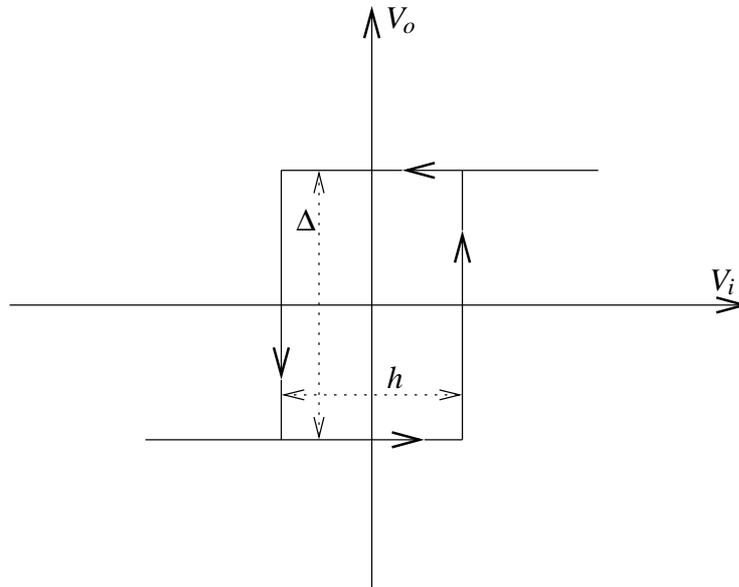


Figure 3.27: Transfer curve of a comparator with hysteresis

It is due to the fact that the comparator has a memory of the previous state, so an overdrive is necessary to make it commute to the correct state. The damage the hysteresis incurs on the performance of Boser structure is shown in Fig. 3.28.

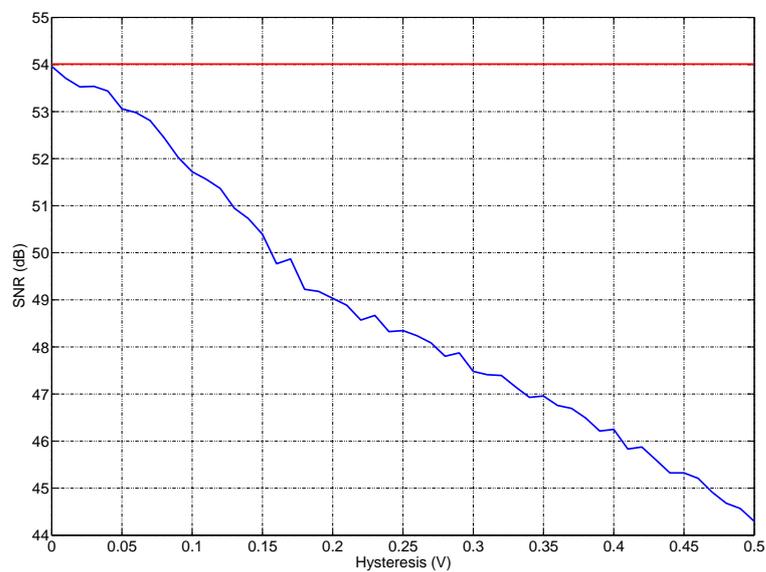


Figure 3.28: Hysteresis impact on the performance of Boser structure

It is evident that hysteresis has a highly deteriorating effect on the performance. At

hysteresis of 13% of full-scale, 3dB of resolution (equivalent to half bit) is lost. The output spectrum showing increased inband noise due to hysteresis is exposed in Fig. 3.29.

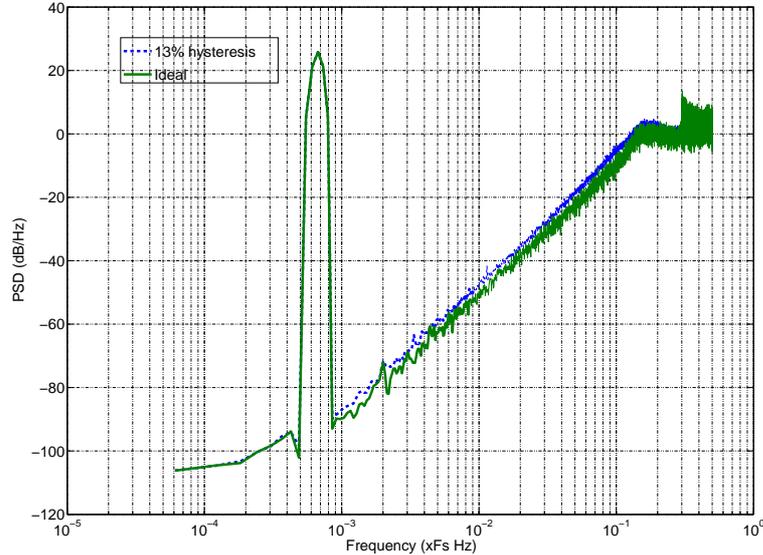


Figure 3.29: Output spectrum in presence of Hysteresis

In addition to this type of hysteresis, which is deterministic, there is another of random nature. It is a typical error of the latched comparators with a reset phase during which the memory of the previous state must be fully erased. Due to the deficiencies of the real devices, this process leaves certain residues of the previous state, leading to an uncertainty zone. In this zone the output of the comparator is not determined only by its input, but in addition, by the previous state and the transitions of the signals resetting the latch. In [12], it is shown that in an  $L$ th-order modulator, the inband power of the error due to the comparator hysteresis can be approximated by  $P_h = 4h^2\pi^{2L}/[(2L+1)M^{(2L+1)}]$ .

### 3.8 Conclusion

In this chapter, the principle of  $\Delta\Sigma$  modulator has been presented. The state-of-art second-order topologies are presented. Since second-order modulator does not provide the required conversion performance, two broad classifications of higher-order configurations namely single-loop and multi-stage or MASH topologies are elaborated. Some latest versions of MASH topologies which are free from noise-leakage or mismatch problems are also illustrated. System level modeling is carried out on Boser structure for circuit level parameters like op-amp dc-gain, gain-bandwidth-product, slew rate etc. This helps in finding the specifications of the main building blocks like op-amp and comparator. It is found that an op-amp with  $\pm 1.3V_{ref}$  voltage-swing, 40dB dc-gain,  $5F_s$  GBW product and  $1.8F_s$  SR will provide the near-to-ideal performance.

## Chapter 4

# High-Pass $\Delta\Sigma$ Modulator

### 4.1 Introduction

The traditional low-pass  $\Delta\Sigma$  modulation, described in the preceding chapter, can perform a very good job if the inherent circuit noises are ignored. In practice, however, the circuit low frequency noise such as flicker noise, offset voltage of the op-amp (offset noise) and clock feedthrough noise, always exists and degrades the performance of the  $\Delta\Sigma$  modulators seriously. Two major techniques, namely the correlated double sampling [82, 83] and chopper stabilization [83, 84, 85] have been proposed and applied to the operational amplifier (op-amp). These solutions, however, have not achieved a significant noise reduction and the performance still remains degraded. A new design technique to counter the low-frequency noise problem has been proposed in [6] which is called high-pass  $\Delta\Sigma$  modulator. In this architecture, the chopper stabilization technique is applied to the  $\Delta\Sigma$  modulator rather than to the op-amp to mitigate the noise efficiently.

In this chapter, the principle of high-pass  $\Delta\Sigma$  modulation is explained, its traditional architecture is exposed and a new architecture is proposed. The performances of these structures are compared in the presence of op-amp non-idealities. Then the cascaded version of high-pass modulator is discussed and a novel technique is presented. In the end, the latest generation of cascaded structures i.e multi stage closed loop is explained and is applied to high pass modulators.

### 4.2 Principle

The working principle of high-pass (HP)  $\Delta\Sigma$  modulator is the same as that of low-pass (LP)  $\Delta\Sigma$  modulator, i.e. the quantization noise is shaped away from the signal band by a loop filter. The difference lies in the placement of the signal band. In the case of HP  $\Delta\Sigma$  modulator, it is located at  $F_s/2$ , where  $F_s$  is the sampling frequency, compared with a pass-band at  $dc$  for the LP  $\Delta\Sigma$  modulator. Thus, the transformation of a low-pass to high-pass modulator is a high-pass to low-pass transformation for the quantization noise transfer function. It is also the low frequency to high frequency transformation for a signal. This transformation makes the HP  $\Delta\Sigma$  modulator completely immune to low frequency

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noise.

The  $z \rightarrow -z$  transformation in  $z$ -domain corresponds to the LP to HP modulator transformation. The HP  $\Delta\Sigma$  modulator is thus realized by applying the transformation,  $z \rightarrow -z$ , to a LP  $\Delta\Sigma$  modulator.

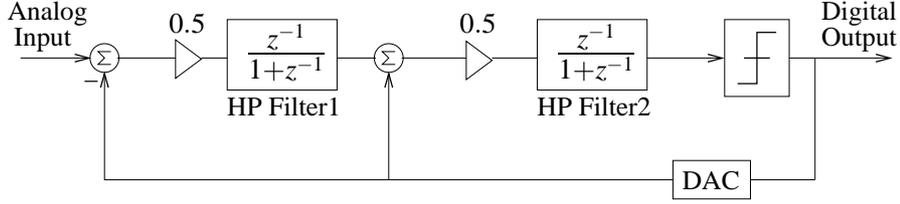


Figure 4.1: Single-stage second-order HP  $\Delta\Sigma$  modulator

Fig. 4.1 shows the second-order HP  $\Delta\Sigma$  modulator [6]. The signal coming into the HP  $\Delta\Sigma$  modulator is a high frequency signal that is obtained by down-converting the RF signal to IF which is set at  $F_s/2$ . It then goes through the HP modulator. The quantization noise is shaped to low frequency region. The output signal of the modulator is chopped (multiplied by a sequence of 1,-1,1,-1,...) back to low frequency region. A low pass filter eliminates not only the most of quantization noise but also the low frequency noise in the same time and brings back the output rate to Nyquist rate.

Assuming the quantization noise,  $E(z)$  to be an additive white noise source uncorrelated with the input signal as in the linear analysis of a conventional  $\Delta\Sigma$  modulator [10], the output of the second-order HP  $\Delta\Sigma$  modulator in  $z$ -domain, is then written as,

$$Y(z) = z^{-2}X(z) + (1 + z^{-1})^2E(z) \quad (4.1)$$

The  $z \rightarrow -z$  transformation has changed the zero of quantization noise transfer function in the  $z$ -domain from  $z = 1$  to  $z = -1$ , the noise suppression region has been shifted from dc to  $F_s/2$ . The signal transfer function is an all-pass filter, so the input signal in the frequency band around  $F_s/2$  goes through the modulator. In a similar manner, the transfer function for the HP filter is realised by applying this transformation to a SC integrator,

$$H_{lp}(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (4.2)$$

Consequently, the Switched Capacitor (SC) integrator transfer function given by 4.2 transforms to a HP filter 4.3 once the transformation,  $z \rightarrow -z$  is applied. This filter has a zero at dc, compared with a zero at  $F_s/2$  for the SC integrator.

$$H_{hp}(z) = \frac{-z^{-1}}{1 + z^{-1}} \quad (4.3)$$

The  $z \rightarrow -z$  transformation changes the zero of quantization noise transfer function in the  $z$ -domain from  $z = 1$  to  $z = -1$ , i-e it shifts the noise suppression from dc to  $F_s/2$ . The signal transfer function is an all-pass filter, so the input signal in the frequency band around  $F_s/2$  goes through the modulator.

The dynamic range of a HP  $\Delta\Sigma$  modulator can be estimated in the same manner as that of a LP modulator. The result is that the HP modulator provides the same performance as the LP modulator. For a generalized  $L^{\text{th}}$  order HP modulator,  $L + 1/2$  bit of resolution is gained for every doubling of the oversampling ratio. Moreover, the quantization noise being shaped out to baseband, it completely covers the low frequency noise such as  $1/f$  noise, and offset has no effect on the performance of the HP modulator, which is not the case in a LP modulator.

## 4.3 Single-Loop HP $\Delta\Sigma$ Modulator Structures

### 4.3.1 Boser-based Structure

A classical structure of HP modulator is presented in [6]. It is obtained by applying  $z \rightarrow -z$  transformation to the LP second-order modulator proposed by Bernard E. Boser in [12] and presented in Sec. 3.3.1 on Page 68. This HP modulator is shown in Fig. 4.1.

The linear analysis of this structure, performed on the same lines as for its LP counterpart, results in the STF of:

$$STF = \frac{0.25Gz^{-2}}{D(z^{-1})} \quad (4.4)$$

and the noise transfer function (NTF) is calculated to be:

$$NTF = \frac{(1 + z^{-1})^2}{D(z^{-1})} \quad (4.5)$$

where  $G$  is the quantizer gain and,

$$D(z^{-1}) = 1 + (2 - 0.5G)z^{-1} + (1 - 0.25G)z^{-2}$$

In classical literature, value of quantizer gain is assumed to be 4, which results in the famous STF of:

$$STF = z^{-2} \quad (4.6)$$

and NTF of:

$$NTF = (1 + z^{-1})^2 \quad (4.7)$$

Note that STF is an all pass filter and NTF is a low pass filter having a zero at  $F_s/2$  thus rejecting all the noise around signal band. A brief description of the advantages and disadvantages of Boser structure is given in Sec. 3.3.1.

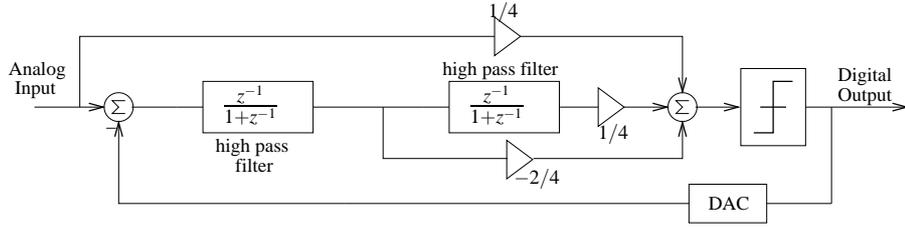
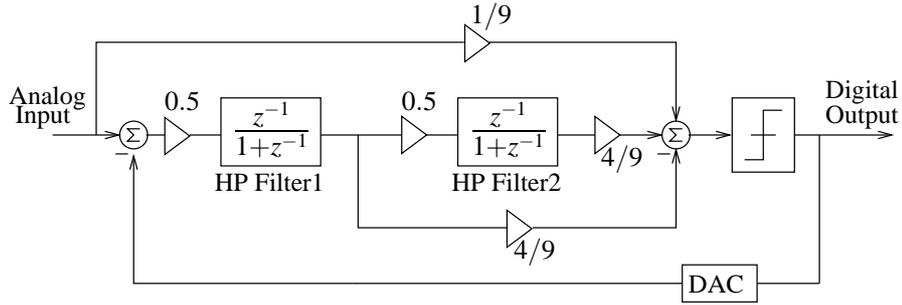
Figure 4.2: Silva-based Structure for High Pass  $\Delta\Sigma$  Modulator

Figure 4.3: Optimized version of Silva-based Structure

### 4.3.2 Silva-based Structure

Silva structure is presented in Sec. 3.3.2 on Page 70. This topology, adapted for high-pass operation, is shown in Fig. 4.2

The refined version of this low-distortion architecture with optimized coefficients is presented in [55] for low-pass operation. Its high-pass version is shown in Fig. 4.3.

The linear analysis of this optimized architecture gives an STF of:

$$STF = \frac{G/9}{D(z^{-1})} \quad (4.8)$$

and the NTF of:

$$NTF = \frac{(1 + z^{-1})^2}{D(z^{-1})} \quad (4.9)$$

where  $G$  is the quantizer gain and,

$$D(z^{-1}) = 1 + (2 - \frac{2G}{9})z^{-1} + (1 - \frac{G}{9})z^{-2}$$

Assuming a value of 9 for  $G$  results in:

$$STF = 1, NTF = (1 + z^{-1})^2 \quad (4.10)$$

The consequence of unity STF is that the input signal is cancelled out at the input of first high pass filter/mirrored integrator and therefore the linearity requirements of the op-

amp constituting this filter are relaxed. The disadvantages of Silva structure are discussed in Sec. 3.3.2.2.

### 4.3.3 Oberst-based Structure

The state-of-the-art in the series of second-order  $\Delta\Sigma$  modulator topologies is Oberst structure [14], which is discussed in 3.3.3 on Page 71. The high-pass version of this structure is illustrated in Fig. 4.4.

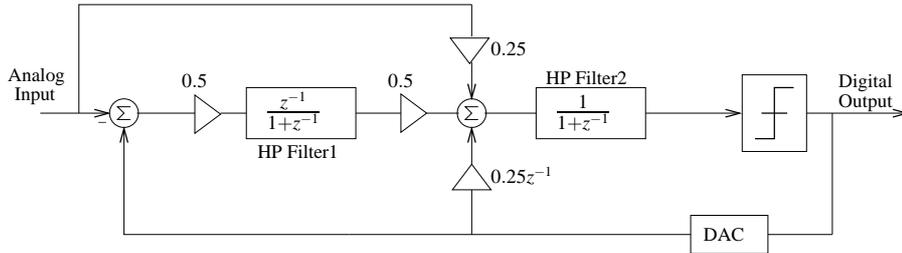


Figure 4.4: Oberst-based Structure for High Pass  $\Delta\Sigma$  Modulator

For an information on the benefits brought by this architecture and its inherent problems, please refer to Sec. 3.3.3.

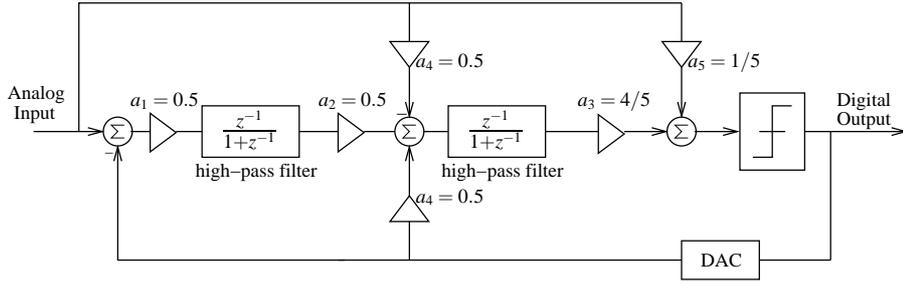
### 4.3.4 Proposed Unity-STF Structure

A new unity-STF structure has been proposed which mitigates the shortcomings of the existing modulator architectures. This topology for high-pass conversion is shown in Fig. 4.5. This is a mixed feedback feedforward structure in which the signal attacks the comparator directly. The useful signal is cancelled at the input of both high-pass filters. Thus the problem of second opamp distorting the useful signal, associated with the Oberst-based architecture, has been addressed. Both the high-pass filters are implemented as delayed filters, thus eliminating the issue of increased loading on opamp implementing the first high-pass filter, which is not the case in Oberst-based structure. The issues related to Silva-based topology have been resolved by changing the auxiliary feedforward path from around the second high-pass filter to around the first high-pass filter as shown in the Fig. 4.5.

This relaxes the requirements on the adder since there are only two branches to add as opposed to three branches in Silva-based structure. Implementing this adder as passive adder, now results in lesser attenuation of the signal thus reducing the design requirements of the quantizer. The loading on the first opamp has also been reduced as there is no feedforward capacitor to charge.

#### 4.3.4.1 Linear Analysis

As did earlier for Boser-based and Silva-based structures, replacing the quantizer by its linear model shown in Fig. 3.5 and performing the analysis results in an STF of:

Figure 4.5: Proposed Structure for Unity-STF High-Pass  $\Delta\Sigma$  Modulator

$$STF = \frac{G/5}{D(z^{-1})} \quad (4.11)$$

and similarly the NTF is found to be:

$$NTF = \frac{(1 + z^{-1})^2}{D(z^{-1})} \quad (4.12)$$

where  $G$  is the quantizer gain and,

$$D(z^{-1}) = 1 + (2 - \frac{2G}{5})z^{-1} + (1 - \frac{G}{5})z^{-2}$$

Assuming a value of 5 for  $G$  results in:

$$STF = 1, NTF = (1 + z^{-1})^2 \quad (4.13)$$

The important result in this analysis is that the quantizer gain has been reduced to 5 in this structure as compared to quantizer gain of 9 in Silva-based structure, while keeping the same high pass filter coefficients. This means that the signal entering the quantizer of proposed architecture is 9/5 times (2.5dB) higher than that of Silva-based structure, thus reducing the sensitivity requirements of the quantizer and is also useful in the design of cascade architecture as discussed in a later section.

#### 4.3.4.2 Refining the Proposed Architecture

The proposed structure has been further refined by optimizing the coefficients and optimizing the position of NTF zero. To optimize the coefficients, the effect of changing coefficients on SNR has been studied. While calculating effect of one coefficient, all other coefficients are kept constant at  $a_1 = 0.5, a_2 = 0.5, a_3 = 0.8, a_4 = 0.5, a_5 = 0.2$ . This simulation shows that SNR is sensitive to a ratio between  $a_1$  and  $a_4$ . SNR is insensitive to all the other coefficients. It is to be noted however that we are using 1-bit quantizer. SNR might be sensitive to other coefficients when we use multi-bit quantizer.

To find an optimum relation between  $a_1$  and  $a_4$ , we performed detailed simulations varying the two variables simultaneously. Simulation results are shown in Fig. 4.6

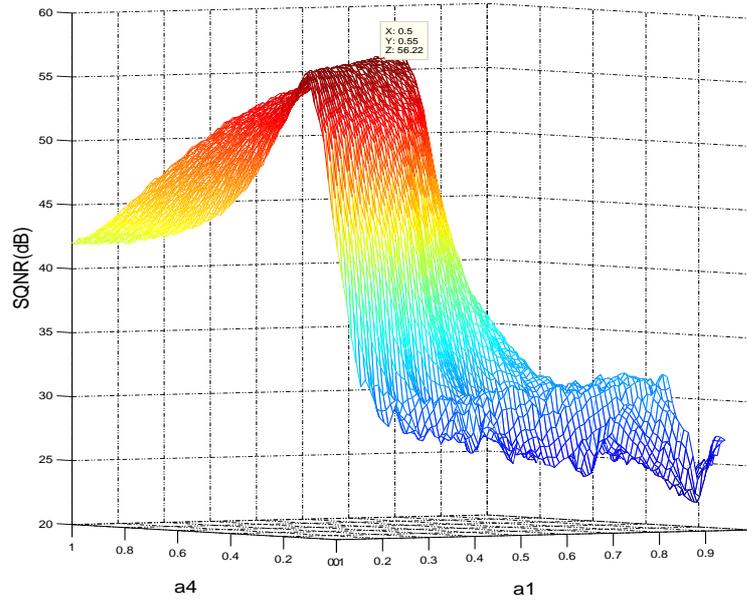


Figure 4.6: Coefficient Sweeping for Proposed Architecture

Results show that the ratio of  $a_4/a_1 = 1.1$  gives the best SNR. We further confirmed this result by carrying out the simulation at multiple input signal amplitudes and compared the classic relation  $a_4/a_1 = 1$  with the newly found relation  $a_4/a_1 = 1.1$ . Results are shown in Fig. 4.7

These results show that we gain in highest achieved SNR with the new coefficients at the cost of losing in SNR at low amplitudes.

The second step in refining the proposed modulator consists of placing the complex conjugate pair of zeros at a frequency  $f_o$  near  $F_s/2$  and inside the signal band which minimizes the inband quantisation-noise power. The generalized NTF having a notch at frequency  $f_o$  is represented mathematically by:

$$NTF(z) = 1 + \delta z^{-1} + z^{-2} \quad (4.14)$$

which in the frequency domain is:

$$NTF(f) = NTF(z)|_{z=2\pi f/F_s} = 1 + \delta e^{-2\pi f/F_s} + e^{-4\pi f/F_s} \quad (4.15)$$

where  $\delta = 2\cos(2\pi f_o/F_s)$ . It is a low pass filter with a notch at frequency  $f_o$ . Note that using the traditional value of  $f_o$  at  $F_s/2$ , we get the standard NTF of second order HP modulator. To find the optimum value of  $\delta$  which results in the minimum inband quantization noise, and thus the maximum signal to quantization noise ratio (SQNR), we have to find the minimum of the function relating the inband noise power to the notch frequency  $f_o$ . Under the additive white noise model, the power of the quantization noise is  $\Delta^2/12$ , and is uniformly distributed in the sampling bandwidth. Therefore, the power spectral density of the shaped quantization noise is:

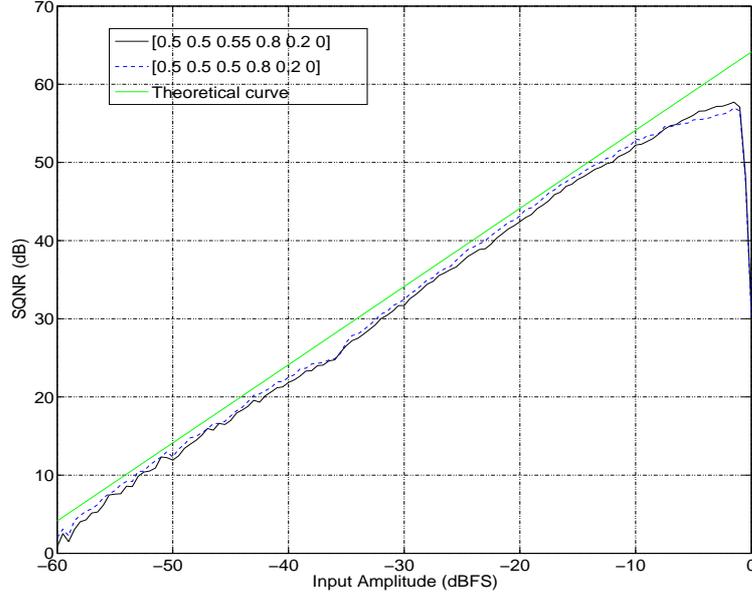


Figure 4.7: Comparison of proposed architecture performance at two different sets of coefficients

$$S_e(f) = \frac{P_e}{F_s} = \frac{\Delta^2}{12} \frac{1}{F_s}, \quad -\frac{F_s}{2} < f < \frac{F_s}{2} \quad (4.16)$$

Note that this spectral density is constant throughout the sampling bandwidth and is inversely proportional to the sampling frequency. Now using the generalized NTF of Eqn. 4.15, the spectral density of the shaped quantization noise is:

$$S_Q(f) = |NTF(f)|^2 S_e(f) = |1 + \delta e^{-2\pi f/F_s} + e^{-4\pi f/F_s}|^2 \frac{\Delta^2}{12} \frac{1}{F_s} \quad (4.17)$$

Now the inband quantization noise power is found by integrating the power spectral density  $S_Q(f)$  throughout the signal band:

$$P_Q(f_o) = \int_{-f_b}^{f_b} S_Q(f) \quad (4.18)$$

The value of  $f_o$  which minimizes this function and hence maximises the SNR is calculated by optimising this function, is approximately given by:

$$f_o = F_s - \frac{f_b}{\sqrt{3}} \quad (4.19)$$

The pole-zero plot of the NTF with standard and optimum zeros is shown in Fig. 4.8

To materialize this optimum NTF, we introduce a local feedback loop around the proposed modulator, thus making a resonator as shown in Fig. 4.9:

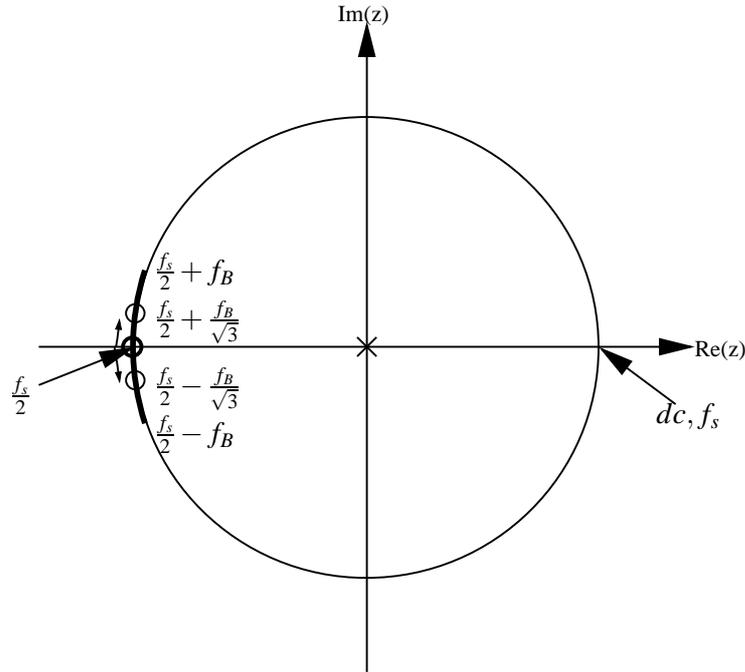


Figure 4.8: Pole Zero Plot of NTF with Standard and Optimum Set of Zeros

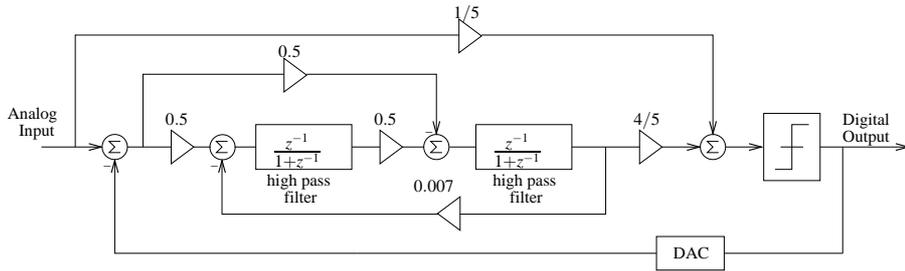


Figure 4.9: A new second-order low-distortion high-SNR HP modulator

The simulation result showing the modulator output spectrum indicative of zero-displacement by adding a local feedback path is shown in Fig. 4.10:

This zero-optimization of the NTF gives us an SQNR improvement of 3.5dB [10] and is presented in simulation result in Fig. 4.11:

#### 4.4 Comparative Analysis of Single-Loop HP Modulators

We presented various second-order HP  $\Delta\Sigma$  architectures and discussed their pros and cons theoretically in the preceding sections. In this section, we present a more in-depth analysis backed with simulation results to analyse these architectures critically. We compare the four architectures (Boser-based, Silva-based, Oberst-based, Proposed) on the basis of 1)

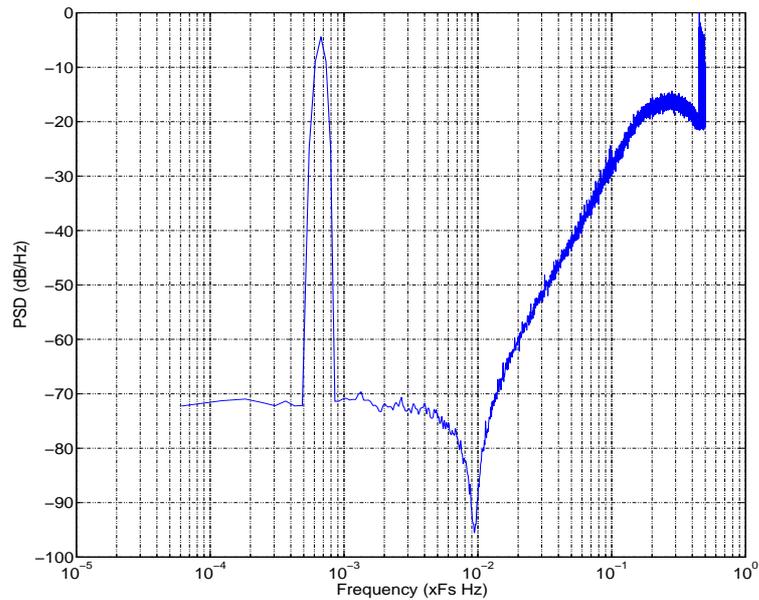


Figure 4.10: Displaced Zero of the High Pass  $\Delta\Sigma$  Modulator as a Result of Local Feedback

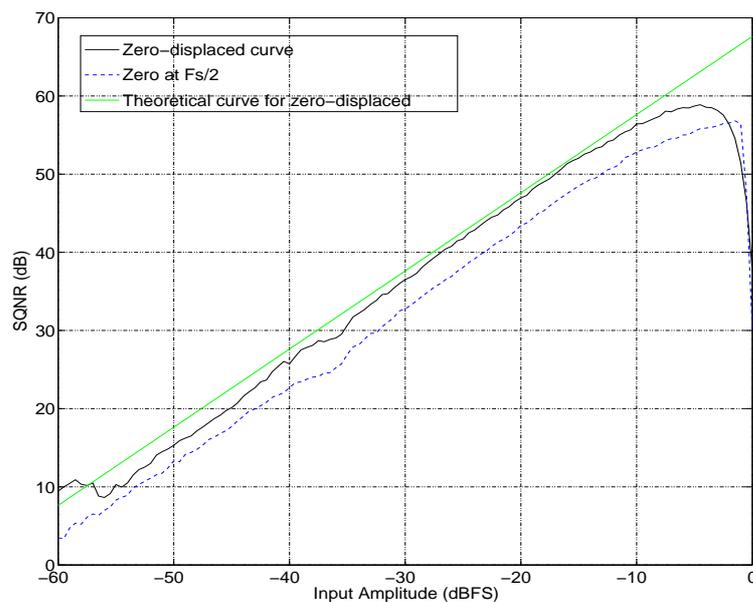


Figure 4.11: Performance improvement of Proposed Architecture by adding a Local Feedback Loop

High-Pass Filter Output Excursions 2) Op-Amp Non-Idealities Effect. Excursions of the high pass filters are an important parameter for comparison because they are directly related to the voltage swing of the op-amps implementing the high-pass filters. We want

to keep these excursions to a minimal level to simplify the design of the op-amps. Other op-amp non-idealities i.e finite dc-gain, finite unity-gain bandwidth and finite slew-rate effect depend on the modulator architecture and the signal flow in the topology. The more immune the architecture is towards these non-idealities, the better the architecture.

The four modulator architectures with their coefficient values, used for comparison analysis are shown in Fig. 4.12:

Note that local feedback loop for zero-optimization has been removed from the proposed architecture so that it becomes comparable with other structures.

#### 4.4.1 High-Pass Filter Output Excursion

System level simulations have been carried out using matlab to study the output excursions of high-pass filters of different HP modulator schemes. The best scheme is one which has minimum output range since it necessitates an opamp with the least voltage swing. The design of an opamp becomes fairly easy, if the constraint of voltage swing is relaxed and it allows us to design opamp with good values of other performance parameters like gain, bandwidth and consumption. On the other hand, if a filter has an output range which exceeds the quantization step, it will overload the comparator and render the system unstable. Another phenomena which makes excessive output excursions undesirable is voltage clipping at the output of op-amp; if the output voltage exceeds opamp's output voltage swing, the clipping occurs which also renders the system unstable. Thus output excursion is an important parameter to compare the various modulator architectures.

Like in the previous chapter, for each structure, ten sets of  $1.1 \times 2^{14} = 18022$  point simulations with each set at a random high-pass filter initial state, have been carried out. The first 1638 points have been truncated to remove the transient effects. The ten sets of histograms have been averaged for final results. The input signal is a sinusoid with an amplitude of 0.4 normalized with respect to quantization step i.e -8dBFS (dB with reference to full scale). The system level simulations have been performed with sampling frequency normalized to one and input signal frequency of  $F_s/2 - 6.7139e - 04 = 0.4993$ .

The histograms showing the output excursions of two high-pass filters in the four competing topologies are presented in Fig. 4.13

The results presented in Fig. 4.13 show that the Boser-based structure has the highest excursions in the first filter, which is expected since it processes both the useful signal and the quantization noise. All the other structures have the same excursions for first high-pass filter since they all process just the shaped quantization noise. These excursions are well inside the range  $-V_{ref} \leftrightarrow V_{ref}$  i.e the quantization step and are easily implementable. The saturations voltage of operational amplifier is normally set by quantization step i.e the voltage range  $-V_{ref} \leftrightarrow V_{ref}$ , but since Boser-based structure's excursion exceeds this range, we have to design opamps with higher voltage swings, thus increase the power consumption, which can become significant in low-voltage technologies.

The second high-pass filter's excursion is very less for Silva-based structure, the second in the run is the Proposed architecture, then the Oberst-based and Boser-based structures. But all of them are well inside the quantization step and are thus easily realized.

From another point of view, we have performed simulations by modelling the op-amp

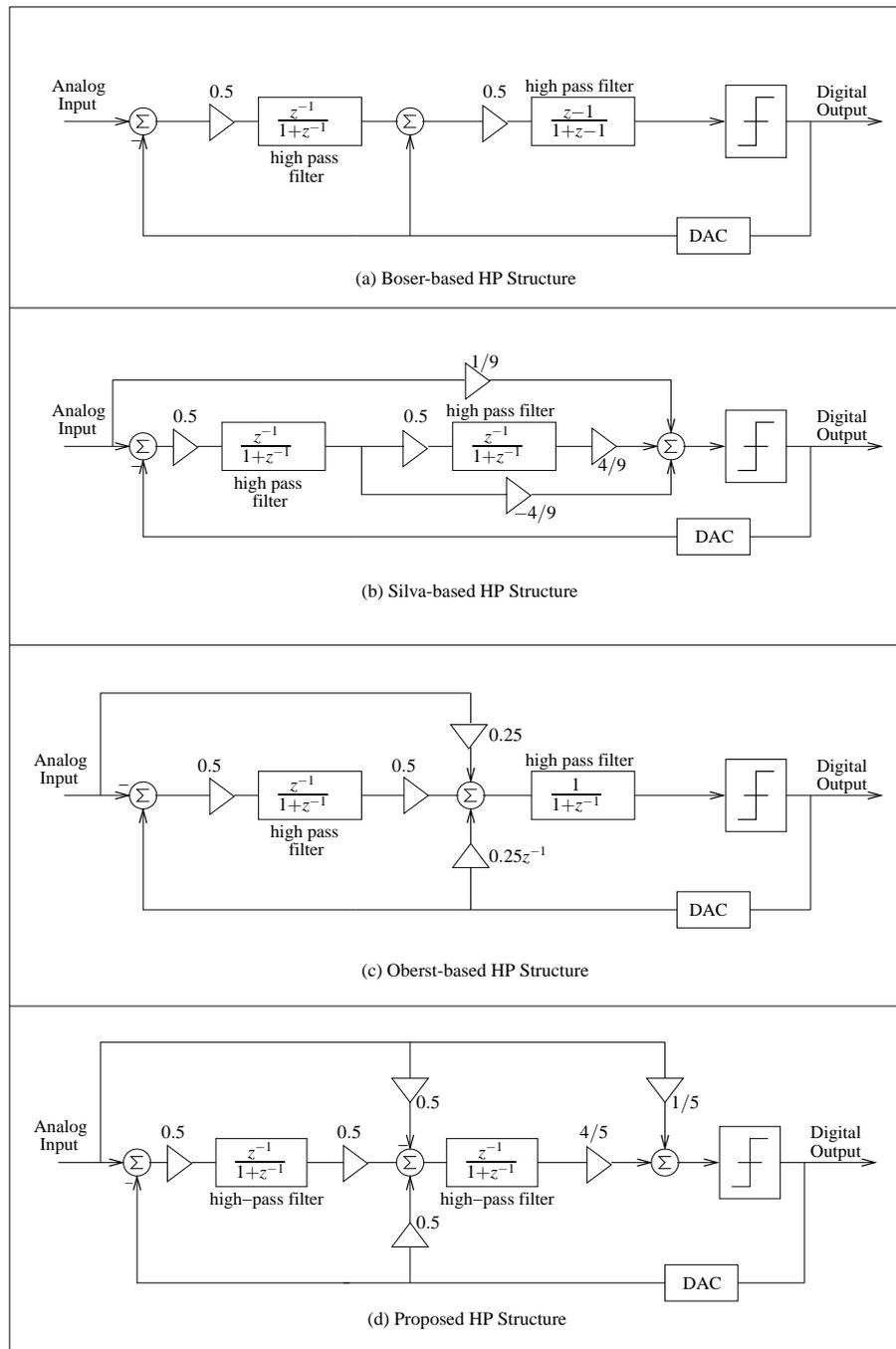


Figure 4.12: Four Structure used for comparative analysis

saturation by clipping the high pass filter output at  $\pm V_{ref}$ . That is any output greater than  $V_{ref}$  has been forced to be at  $V_{ref}$  and any output less than  $-V_{ref}$  has been forced to be at  $-V_{ref}$ . The resulting simulation result is shown in Fig. 4.14:

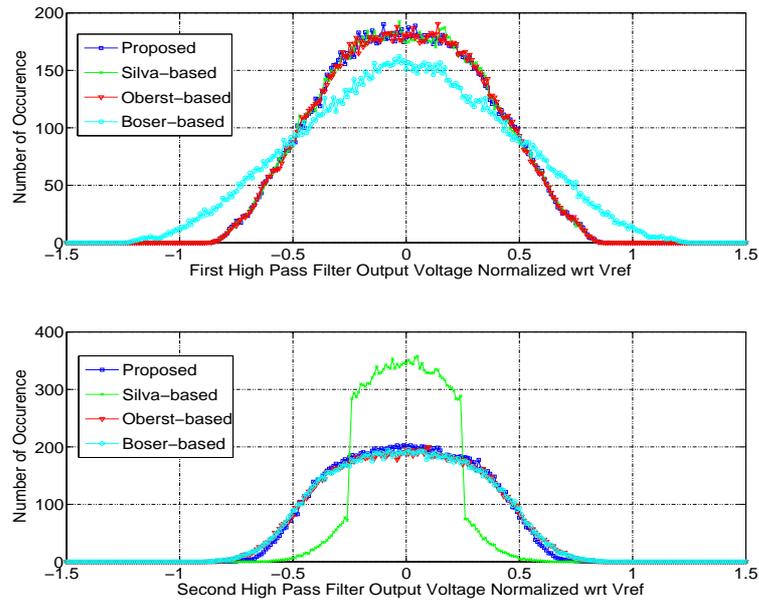


Figure 4.13: Comparison of High-Pass Filters' Output Excursion at  $V_{in}=-8\text{dBFS}$

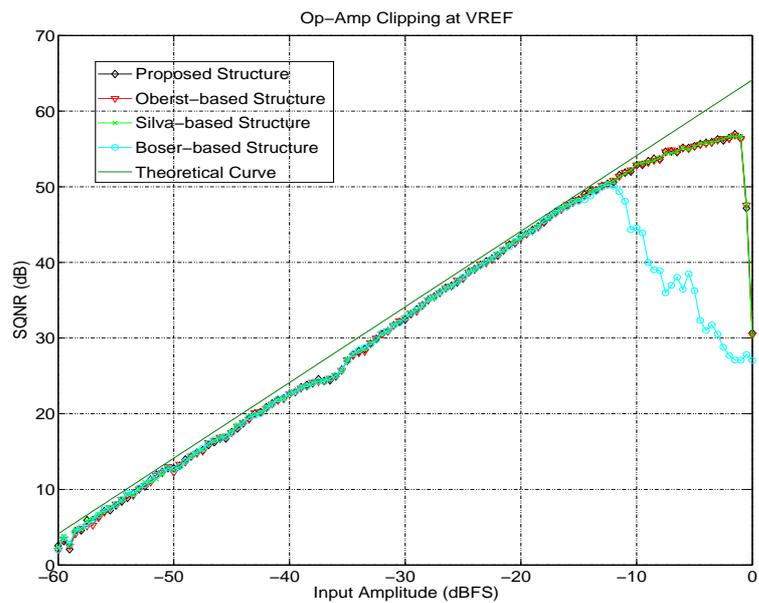


Figure 4.14: Plot of SNR Vs Input Signal in the presence of filter clipping at  $\pm V_{ref}$

As expected, the Boser-based structure is most affected by output clipping since it has the largest excursions. As we increase the input sinusoid amplitude, the output excursion becomes larger and larger and at one point becomes unstable because of clipping.

### 4.4.2 Op-Amp Non-Idealities Effect

Analogous to the role of integrator in the traditional low-pass  $\Delta\Sigma$  modulators is the role of high-pass filter in HP  $\Delta\Sigma$  modulator i.e it is its major building block. The performance of high-pass filter is directly related to the performance provided by its op-amp. Operational amplifiers' non-idealities including finite and nonlinear dc-gain, finite gain-bandwidth product (GBW) and finite slew rate (SR) cause incomplete transfer of charge in the switched-capacitor (SC) implementation of high-pass filter which is a major cause of performance degradation of HP  $\Delta\Sigma$  modulators. Several articles in the literature have discussed these effects and established their behavioural models to study their effect on integrators [80, 78, 81], which form the basis of traditional low-pass (LP)  $\Delta\Sigma$  modulators. Here, we discuss the op-amp nonidealities effect on a high-pass-filter and compare the different architectures discussed in the preceding sections with respect to their immunity to these non-idealities. We will discuss each non-ideality separately in the following sections.

#### 4.4.2.1 Finite DC-Gain

An ideal delayed high-pass filter with a coefficient  $b$  is described by  $z$ -domain transfer function:

$$H_{ideal}(z) = b \frac{z^{-1}}{1 + z^{-1}} \quad (4.20)$$

Although delay-less filters can be used to realize the desirable NTF, most often delayed-integrators are used in the first stage of the modulators as they are easily implemented in SC design. The operational amplifier finite open-loop dc-gain  $A_O$  introduces errors in this ideal transfer function. This effect can be represented mathematically by:

$$H_{practical}(z) = b \frac{\alpha z^{-1}}{1 + \beta z^{-1}} \quad (4.21)$$

where  $\alpha$  and  $\beta$  are less-than-unity quantities and represent gain degradation and filter leakage (or gain and pole location perturbation) respectively. Gain degradation results in only a fraction of the input signal being added to the output and filter leakage results in only a fraction of the last output being subtracted from the input. Since both the terms of subtraction are reduced, the output of high pass filter is less affected due to finite op-amp dc-gain. This is why, the high-pass filter is less prone to performance degradation due to finite op-amp dc-gain than an integrator.

To work out the values of  $\alpha$  and  $\beta$ , let us take the standard SC implementation of first high-pass filter of the second-order HP  $\Delta\Sigma$  modulators discussed previously. This implementation is illustrated in Fig. 4.15.

Where  $C_p$  represents the input parasitic capacitance of the op-amp, parasitic capacitance of the switches connected to the negative input of the op-amp and parasitic capacitance associated with the plates of capacitors connected to the negative input of the op-amp. Solving charge-transfer equations for this filter, keeping in view the charge-conservation law, the practical transfer function in terms of capacitances and op-amp dc-gain  $A_0$  is given by:



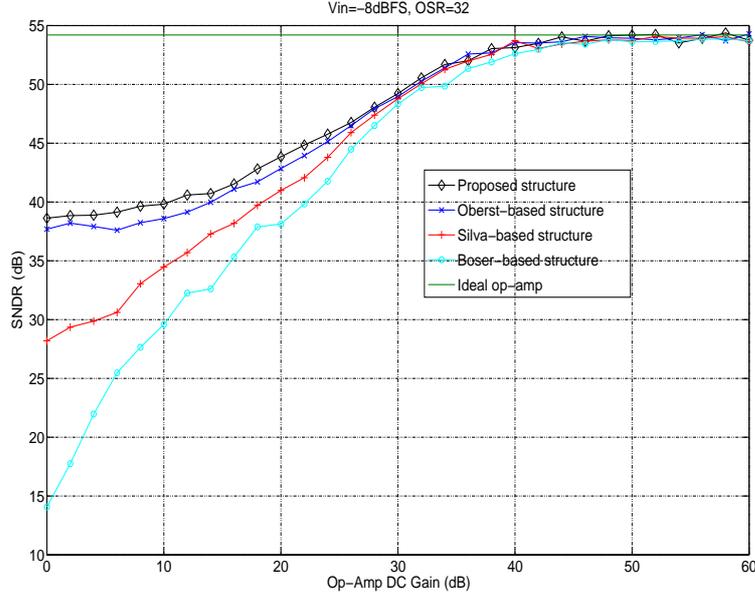


Figure 4.16: SNR Vs Op-Amp DC-Gain

#### 4.4.2.2 Finite Gain-Bandwidth Product and Slew Rate

With the assumption of a single-pole model for the op-amp, the output transient of the high-pass filter during  $n$ th integration phase is represented by:

$$v_{out}(t) = v_{out}(nT_s - T_s) + (-(1 + \beta)v_{out}(nT_s - T_s) + b\alpha v_{in}) \times \left(1 - e^{-\frac{t}{\tau}}\right), \quad 0 < t < \frac{T_s}{2} \quad (4.26)$$

where  $v_{out}$  is the output of the filter,  $T_s = 1/F_s$  is the sampling period,  $v_{in}$  is the input of the filter and  $\tau = (3 + b)/2\pi GBW$  is the time constant of the op-amp comprising the filter. The value of the time-constant  $\tau$  is derived in the Annex. B. If this high-pass filter represents the first high-pass filter of a second-order modulator,  $v_{in}$  is given by:

$$v_{in} = x(nT_s - T_s/2) - y(nT_s - T_s) \quad (4.27)$$

where  $x$  is the input of the modulator and  $y$  is the output of the modulator. In case of infinite GBW of the op-amp,  $\tau$  falls to zero and Eqn. 4.26 reduces to Eqn. 4.21, while the values of  $\alpha$  and  $\beta$  are given by Eqn. 4.25. Finite GBW on the other hand, reduces the gain of the filter which in turn reduces the value of the new input to be added to the output and also diminishes the value of the signal stored in the feedback capacitor which has to be added to the output during the integration phase.

A theoretical description of the op-amp slew rate is provided in the preceding chapter. In this chapter, we use those concepts to figure out the charge-transfer transient of high-pass filter in the presence of finite SR op-amp. SR demand on the op-amp is characterised

by maximum slope of the curve drawn by charge transfer eqn. 4.26. This curve finds its maximum slope at  $t = 0$ , given by:

$$SR_d = \frac{d}{dt}v_{out}(t)|_{max} = \frac{-(1 + \beta)v_{out}(nT_s - T_s) + b\alpha v_{in}}{\tau} \quad (4.28)$$

The charge transfer transient can now be represented by Eqns:

$$v_{out}(t) = v_{out}(nT_s - T_s) + SR_s t, \quad t \leq t_0 \quad (4.29)$$

$$v_{out}(t) = v_{out}(nT_s - T_s) + (-1 + \beta)v_{out}(nT_s - T_s) + b\alpha v_{in} - SR_s t_0 \times \left(1 - e^{-\frac{t-t_0}{\tau}}\right), \quad t > t_0 \quad (4.30)$$

where  $SR_s t_0$  is the value reached by  $v_{out}(t)$  at  $t = t_0$  where the limitation of SR ends i.e.  $SR_d$  equals  $SR_s$ .

Imposing the condition for the continuity of the derivatives of Eqns. 4.29-4.30 in  $t_0$ , we obtain:

$$t_0 = \frac{-(1 + \beta)v_{out}(nT_s - T_s) + b\alpha v_{in}}{SR_s} - \tau \quad (4.31)$$

If  $t_0 > T_s/2$  Eqn. 4.29 holds for the whole clock period. Otherwise, using the value of  $t_0$  from Eqn. 4.31 in Eqn. 4.30, we obtain:

$$v_{out}(t) = v_{out}(nT_s - T_s) + V_s - \text{sgn}(V_s)SR_s \tau e^{-\left(\frac{T_s}{2\tau} - \frac{|V_s|}{SR_s \tau} + 1\right)} \quad (4.32)$$

where  $V_s$  is given by:

$$V_s = -(1 + \beta)v_{out}(nT_s - T_s) + b\alpha v_{in}(nT_s - T_s/2) \quad (4.33)$$

Finite SR supplied by the op-amp results in changing the gain of the high-pass filter in a non-linear fashion and produces harmonics in the output degrading the SNDR. We have performed simulations of the different architectures by varying the values of  $SR_s$  and observed the output SNDR. This procedure is repeated for two different values of op-amp GBW. The results are illustrated in Fig. 4.17:

The results show that at least a  $SR_s$  of  $4F_s(V/sec)$  is needed for feedforward structures to establish the required performance, while for Boser-based structure a  $SR_s$  of  $8.5F_s(V/sec)$  is necessary to guarantee the optimum SNDR at GBW of  $5F_s$ . All the feedforward architectures perform equally good and better than Boser-based structure.

## 4.5 Multi-Stage HP $\Delta\Sigma$ Modulator Structures

At low values of over-sampling ratio (OSR), it is not possible to obtain high SNR values in a single-quantizer HP modulator simply by raising the order of the loop filter, since stability considerations limit the permissible input signal amplitude for higher-order loops, which counteracts the improved noise suppression. The SNR can still be increased by using more

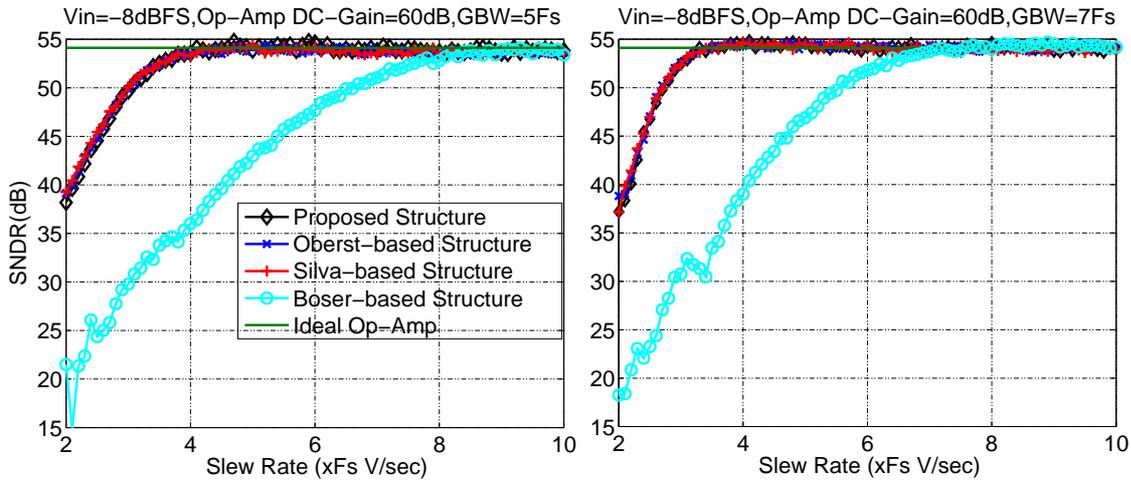


Figure 4.17: SNDR degradation for different architectures as a function of op-amp SR

bits in the internal quantizer, but this requires a multi-bit ADC and also means to insure the in-band linearity of the internal DAC [60]. As a result, the complexity of the quantizer grows exponentially with the number of bits used in it. Hence, this number can seldom be higher than 4 or 5 bits. A different strategy, which relies on the cancellation rather than the filtering of the quantization noise, is to use a multi-stage or MASH (for Multi-stage noise-Shaping) structure for the modulator. It is also called Cascade structure. Here, each stage is realized by a different  $\Delta\Sigma$  modulator. The quantization error of one stage is fed as an input to the next stage. The output of the next stage is then an approximation of this quantization error. The digital filters  $H1(z)$  and  $H2(z)$  are designed so as to cancel the quantization errors of all but the last stage in the output.

#### 4.5.1 Cascade 2-1 HP Delta Sigma Modulator Structure

In order to concisely differentiate between the various cascade combinations, cascaded modulator topologies are referred to by a sequence of numbers corresponding to the order of the differential noise shaping provided by each stage in the cascade. The first number corresponds to the first stage, the second to the second stage, and so on.

We use necessarily a  $2^{nd}$  order  $\Delta\Sigma$  Modulator as the first-stage of MASH Modulators, because it achieves stable, high-order performance without the strict matching requirements that characterize cascades of first-order stages [62]. Furthermore, the use of second-order noise-shaping in the first stage of a cascade avoids the potential presence of discrete noise tones in the output of the overall cascade. Fig. 4.18 shows a generic, cascade 2-1 HP  $\Delta\Sigma$  architecture based on Proposed Structure,

Where  $G1$  is the estimate of quantizer gain of first-stage. The quantization error of one stage is fed as an input to the next stage. The output of the next stage is then an approximation of this quantization error. The digital filters  $H1(z)$  and  $H2(z)$  are designed so as to cancel the quantization error of first stage in the output.

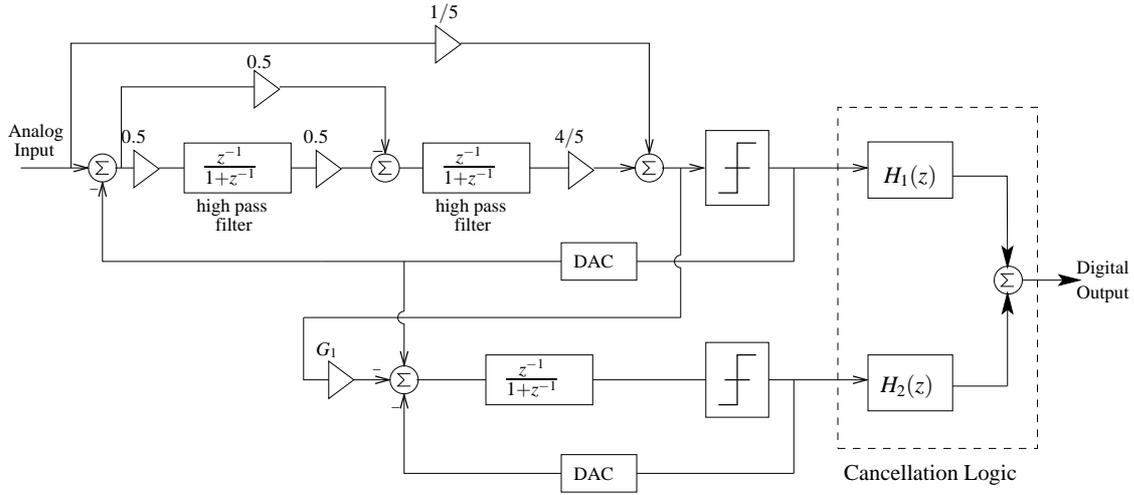


Figure 4.18: Generic architecture of cascade HP  $\Delta\Sigma$  modulator based on Proposed Structure

#### 4.5.2 Quantizer Linear Model and Quantizer Gain Calculation

The linear model of the quantizer, shown in Fig. 3.5 on Page 69 is very important in our design of cascaded  $\Delta\Sigma$  modulator structure. This model approximates the non-linear quantizer by a gain  $G$  called ‘quantizer gain’ in series with an additive gaussian noise source. This approximation which is valid when the quantization step is small as compared to the signal amplitude, is also used for low-resolution quantizers where it is not verified.

The gain of the linear model for multi-bit quantizer is naturally determined by the ratio of the step size to the distance between adjacent thresholds. However, the gain of a binary quantizer is not defined so easily because a binary quantizer has only one threshold [60]. If the statistical properties of quantizer input are known, an obvious optimality criterion for gain  $G$  is to minimize the average power of the error sequence  $e$ . This is defined as the expected (or mean) value of  $e^2$ .

$$\sigma_e^2 = \frac{1}{N} \sum_{n=0}^N e(n)^2$$

Since  $e = v - Gy$ , where  $v$  is quantizer output,  $y$  is quantizer input and  $G$  is quantizer gain, the average power of  $e$  can be written as,

$$\sigma_e^2 = \frac{1}{N} \sum_{n=0}^N (v(n) - G \cdot y(n))^2$$

This is minimized for,

$$G = \frac{\frac{1}{N} \sum_{n=0}^N v(n)y(n)}{\frac{1}{N} \sum_{n=0}^N y(n)^2} \quad (4.34)$$

When a system containing a binary quantizer is replaced by its linear model, the estimate of the quantizer gain  $G$  is found from numerical simulation [86]. Since, we are using binary quantizers in our structure, we find the quantizer gains  $G1$  and  $G2$  of the first-stage and second-stage quantizers respectively using simulation data and Eqn. 4.34. The evolution of  $G1$  and  $G2$  with input signal amplitude is shown in Fig. 4.19. Note that  $G1$  is constant at 3, and  $G2$  is constant at 1 for most part of the input signal range; but they decline at higher values of input signal amplitude due to the saturation of quantizer.

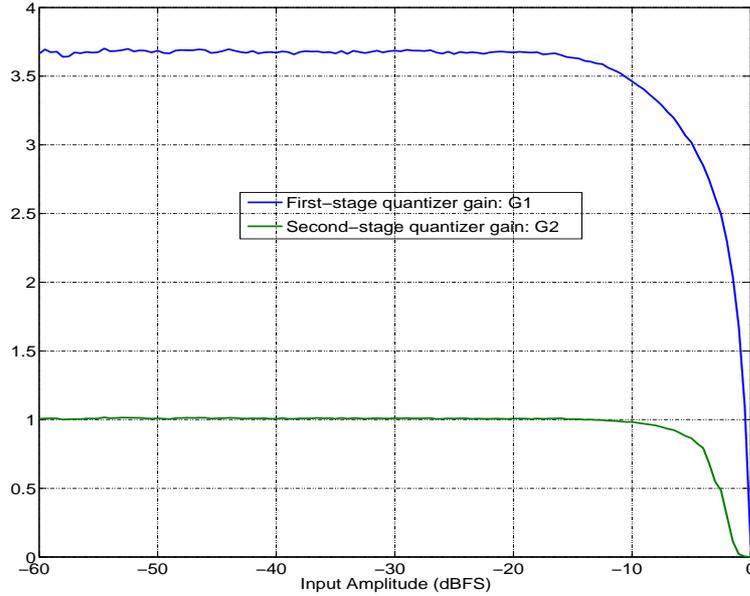


Figure 4.19: First and second-stage quantizer gains as a function of input signal amplitude

### 4.5.3 Quantization Noise Cancellation Filters' Designing

Digital Filters i.e  $H1$  and  $H2$  are designed to achieve two major objectives,

- To cancel the effect of first-stage quantization noise in the output
- To provide third-order HP noise shaping to the second-stage quantization noise in the output

From Fig. 4.18, using linear model of the quantizer presented in Section. 4.5.2, the output of first-stage modulator is,

$$Y1 = \frac{0.2G1}{D(z^{-1})}X + \frac{(1 + z^{-1})^2}{D(z^{-1})}E1 \quad (4.35)$$

where  $G1$  is the first-stage quantizer gain and,

$$D(z^{-1}) = 1 + (2 - 0.4G1)z^{-1} + (1 - 0.2G1)z^{-2}$$

and similarly the output of second-stage modulator is,

$$Y2 = \frac{G2z^{-1}}{1 + (1 - G2)z^{-1}}E1 + \frac{1 + z^{-1}}{1 + (1 - G2)z^{-1}}E2 \quad (4.36)$$

where  $E1$  is the quantization noise of first-stage and is the input of the second-stage, and  $G2$  is the quantizer gain of second-stage.

#### 4.5.3.1 Second-Stage Quantizer Gain $G2$

Simulation result presented in Fig. 4.19 suggests that  $G2$  is almost equal to 1 for most part of the signal range. Putting this value in Eq. 4.36, we get a nice expression for  $Y2$ ,

$$Y2 = z^{-1}E1 + (1 + z^{-1})E2 \quad (4.37)$$

#### 4.5.3.2 First-Stage Quantizer Gain $G1$

Assumption of a value for  $G1$  plays a major role in determination of digital filters. We define three models based on assumption of three different values for  $G1$ :

- In the hypothetical model, we assume  $G1$  to be equal to 5, which is not in accordance with simulation data presented in Fig. 4.19. Nevertheless, this assumption results in a nice expression for  $Y1$ ,

$$Y1 = X + (1 + z^{-1})^2E1$$

Now solving the equation,

$$Y1 \cdot H1 + Y2 \cdot H2 = -z^{-1}X + (1 + z^{-1})^3E2 \quad (4.38)$$

leads to very simple digital filters,

$$H1 = -z^{-1}$$

and,

$$H2 = (1 + z^{-1})^2$$

- In this model, which we call ‘Proposal 1’, we assume  $G1$  to be equal to 3.7, which is true as shown in Fig. 4.19 for most part of the input signal range. Putting this assumed value of  $G1$  in Eqn. 4.35 leads us to,

$$Y1 = \frac{0.74}{1 + 0.52z^{-1} + 0.26z^{-2}}X + \frac{(1 + z^{-1})^2}{1 + 0.52z^{-1} + 0.26z^{-2}}E1 \quad (4.39)$$

Now solving the set of Eqns. 4.37, 4.38 and 4.39 leads to the digital filters,

$$H1 = -z^{-1} - 0.52z^{-2} - 0.26z^{-3}$$

and,

$$H2 = (1 + z^{-1})^2$$

- As shown in Fig. 4.19, the value of  $G1$  varies between 3 and 0.5. We have tested the system performance at multiple values of  $G1$  in this range. As we decrease the value of  $G1$ , the dynamic range increases but the SNR decreases. We find that taking  $G1$  to be equal to 3 gives the best compromise between dynamic range and SNR. Therefore, the third model, which we call 'Proposal 2', consists of assuming  $G1$  to be equal to 3. Working on the same pattern as the previous model, we find the first-stage output as,

$$Y1 = \frac{0.6z^{-2}}{1 + 0.8z^{-1} + 0.4z^{-2}}X + \frac{(1 + z^{-1})^2}{1 + 0.8z^{-1} + 0.4z^{-2}}E1 \quad (4.40)$$

Solution of the set of Eqns. 4.37, 4.38 and 4.40 now gives us the digital filters to be,

$$H1 = -z^{-1} - 0.8z^{-2} - 0.4z^{-3}$$

and,

$$H2 = (1 + z^{-1})^2$$

So, three different assumptions for  $G1$  result in three different values for  $H1$ .  $H2$  remains constant. When we fill these three sets of values in Fig. 4.18, we get three models.

We have simulated these three set of values for an over-sampling ratio (OSR) of 32. Simulation results are presented in Fig. 4.20. In this plot, we have added the SNR curve of the theoretical third-order  $\Delta\Sigma$  modulator for reference.

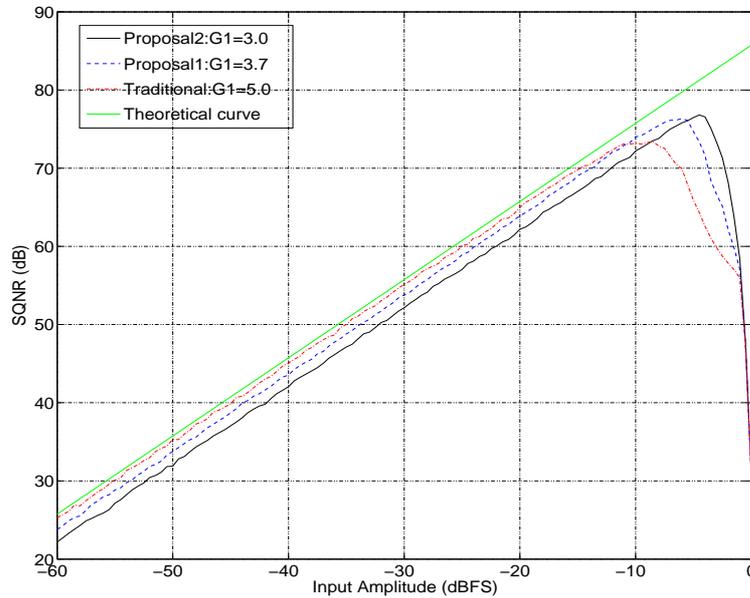


Figure 4.20: Plot of SNR Vs Input Signal for three cascaded HP  $\Delta\Sigma$  structures based on Proposed structure

Results presented in Fig. 4.20 show that the three models perform almost equally good in low-signal range. It is in the high-signal range that our proposals give a superior performance than the classical architecture. This improved performance is due to more accurate and systematic approximation for quantizer gain  $G_1$ .

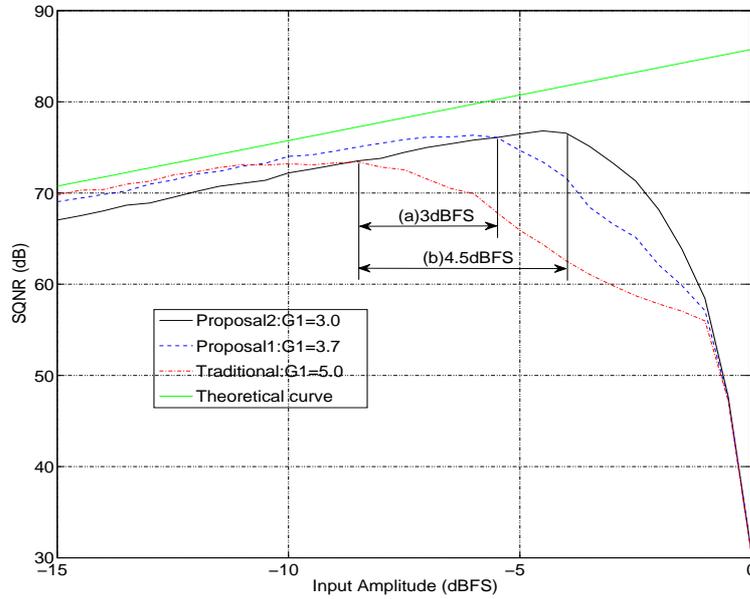


Figure 4.21: SNR vs. High Input Signal for three cascaded HP  $\Delta\Sigma$  models, (a) Increase in dynamic range achieved by Proposal 1 over Classic Architecture (b) Increase in dynamic range achieved by Proposal 2 over Classic Architecture

Figure. 4.21 shows the SNR curves of three models for only the higher values of input signal to highlight the improvement achieved by two proposals over Classic Architecture. It shows that Proposal 1 and Proposal 2 give 3 dB and 4.5 dB increase, respectively, in dynamic range over Classic Architecture. Thus, Proposal 2 gives the best performance with the highest dynamic range.

Input	-20	-15	-10	-5	-4	-2
Classical	65	69.8	73.2	65.9	62.5	57.8
Proposal 1	63.8	69.1	74.0	74.7	71.6	62.1
Proposal 2	62.2	67.0	72.2	76.5	76.6	68.2

Table 4.1: SNRs(dB) for three models at different values of input(dB)

Table. 4.1 gives SNRs for three modulators at different values of input signal amplitude to pinpoint the improvement achieved at higher values of input signal. Note that upto -10dB input signal, the three models give almost equal performance with the maximum difference of only 3dB; but at -4dB input signal, Proposal 2 gives an SNR which is almost

15dB and 5dB more than the SNRs given by classic architecture and Proposal 1 respectively. Proposal 1 gives better results than Classic Model with an improvement of 3dB in highest achieved SNR and an improvement of 3dB in dynamic range; Proposal 2 provides even better results with an improvement of 4dB in maximum attained SNR and an improvement of 4.5dB in dynamic range.

The problem associated with MASH structures is that there is a high level of matching needed between analog coefficients and digital filters. In case of any mismatch, the SNDR performance is degraded. From fabrication point of view, digital filters are quite precise while there is a degree of inaccuracy involved in analog coefficients implementation. To give an idea of performance degradation, we perform monte-carlo simulation of the proposed cascade structure (i-e Proposal 2) by varying the analog coefficients and fixing the digital filters. The 8192 points monte-carlo simulation has been carried out by varying all the coefficients with an standard deviation of .1%. The input signal is set at -8dBFS. The histogram of the resulting output is shown in Fig. 4.22, it has a mean of 72.9dB and an standard deviation of 0.31dB.

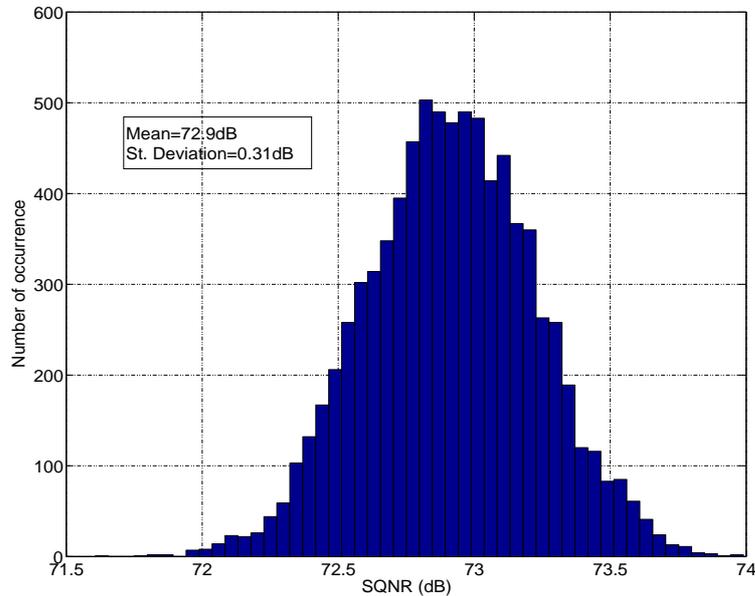


Figure 4.22: Proposed cascaded architecture's sensibility to analog and digital components' mismatches

Analog coefficients' inaccuracy is a direct consequence of the capacitor ratio mismatch in the circuit. Other analog imperfections that change the NTF and STF of individual MASH stages and consequently result in leakage of the quantization noise due to the mismatch of digital filters with analog circuits are finite dc-gain, finite GBW product and finite SR of the amplifiers. Adaptive digital correction of these analog errors is a widely investigated area. This adaptive calibration can be carried out off-line [18], on-line [19, 20, 21, 22, 23] or by test-signal injection [24]. All of these techniques come at the price of increased circuit complexity and power consumption.

#### 4.5.4 Generalized Multi Stage Close Loop

The problem of mismatch between analog components and digital filters in traditional MASH structures due to nonidealities has led to the new generation of MASH structures which are free from quantization noise cancellation filters. In this way, we reduce the circuit complexity and also increase the circuit robustness by eliminating sensitivity to circuit imperfections. The first cascade architecture of this nature is presented in [25]. This structure is called multi-stage closed loop (MSCL). Every stage in this structure is a single-order modulator and a global feedback is introduced from the output, which is the sum of the output of all comparators. An enhanced version of this structure is Generalized multi-stage closed loop (GMSCL). This is basically a cascade 2-2 structure, with each stage implemented as a feedforward structure, and a global feedback is used from the output. We have developed two implementations and compared. First by implementing each stage as a Silva-based high pass structure shown in Fig. 4.23:

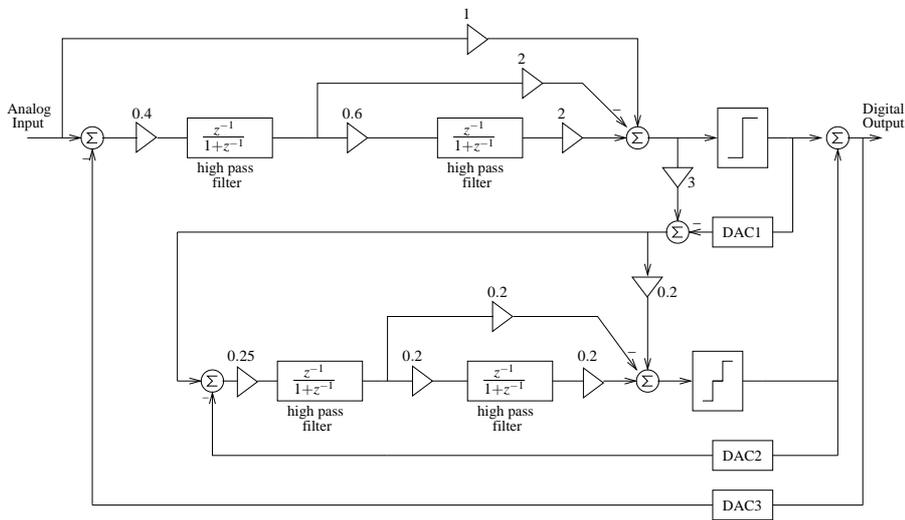


Figure 4.23: GMSCL HP Structure based on Silva-structure

and second by implementing each stage by proposed high pass structure shown in Fig. 4.24:

The coefficients have been chosen to derive the maximum performance out of each structure. The first-stage quantizer is a comparator, while the second-stage quantizer has three output levels, thus 1.5 bits of resolution. Three output levels of quantizer do not increase the non-linearity of the DAC (if implemented in a special fashion) while increase the SNR in comparison to a comparator. DAC1 has two output levels, DAC2 has three output levels while DAC3 has 5 output levels. While DAC1 and DAC2 do not have any non-linearity problems since they are single bit and one-and-a-half bits DACs respectively, DAC3 inherits non-linearity because of being multi-bit in nature. Its non-linearity has to be less than the highest non-linearity of the rest of the system, if we want that it does not degrade the system performance considerably. It has to be noted that the adder before



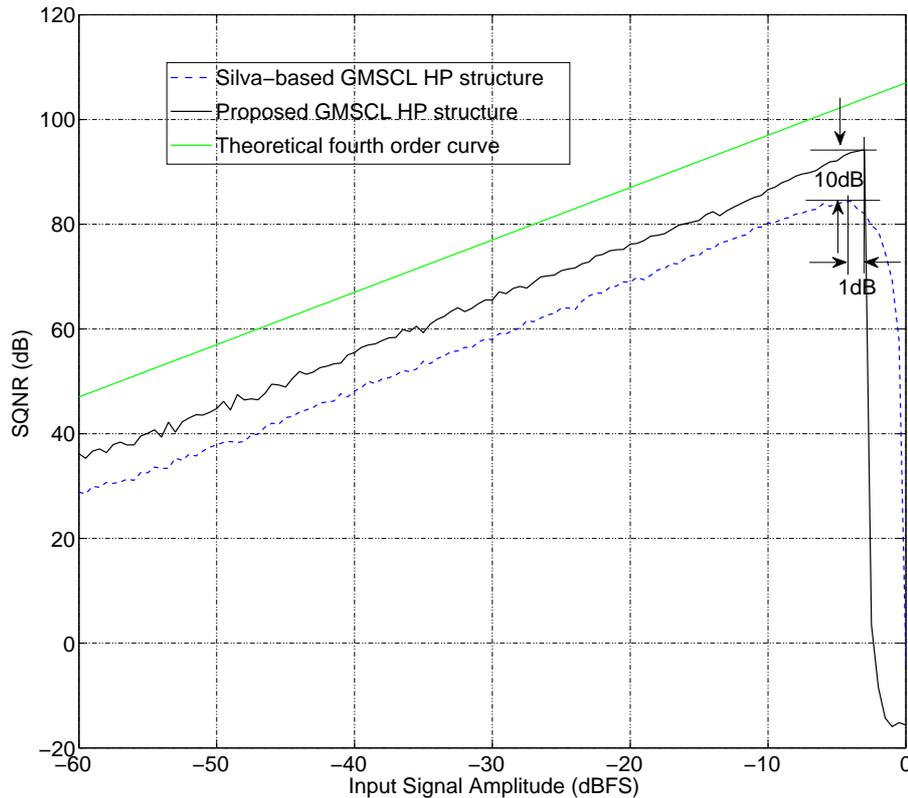


Figure 4.25: Performance comparison of two GMSCl HP structures

DACs. The resulting modulator configuration is shown in Fig. 4.27

Since the quantization noise of main quantizer is fed to the auxiliary and more aggressive quantizer, the output of which is injected back into the main loop, it allows the modulator to process the signals beyond the full-scale (FS) range of the main quantizer; thus the increased DR of the system and hence the increased SNDR performance. The other major advantage of this system comes from the fact that the auxiliary quantizer only processes the quantization noise of the main stage, thus its output is pseudorandom and it mixes up the non-linearities associated with itself. In the frequency domain, the peaks associated with the nonlinearities are flattened out across the frequency band ( $0 \rightarrow F_s$ ) and thus reduced by a factor of OSR. Thus, no tones are produced by this nonlinear DAC as it processes only the quantization noise. The sum of two DACs associated with the first-stage and second-stage comparators is a three level signal i.e  $V_{ref,0}$  and  $-V_{ref}$  and is inherently linear. Thus the total signal being fed back by the DACs is linear, rendering the overall system less sensitive to DAC nonlinearities and avoiding the costly techniques like DEM. To show the efficacy of the proposed architecture, behavioural simulations have been performed in matlab. The first simulation consists of ideal DACs i.e with no nonlinearities to show that the proposed architecture achieves extended DR. To compare the equivalent architectures, the second-stage quantizer of the traditional topology has been

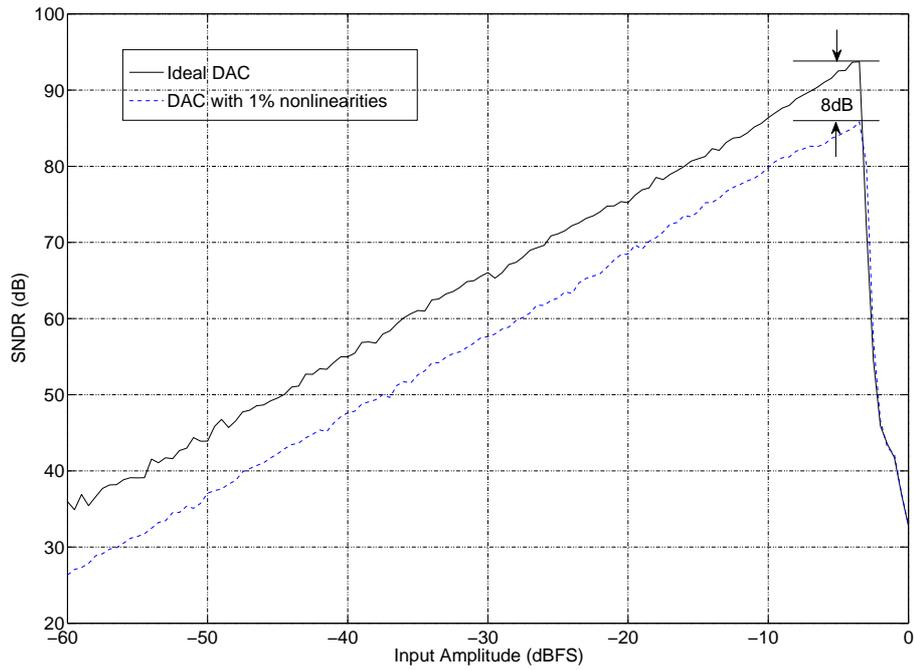


Figure 4.26: Performance degradation due to nonlinear DAC

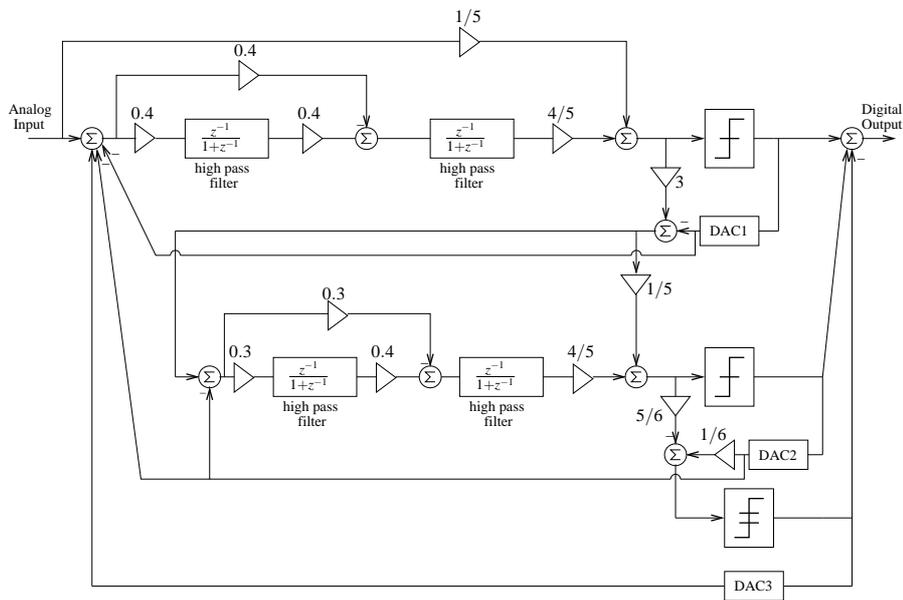


Figure 4.27: Proposed GMSCL HP architecture with extended DR

made 5-level so that it uses four comparators. The proposed architecture has a comparator and an auxiliary 4-level quantizer in the second-stage and thus four comparators. As

shown in the simulation result in Fig. 4.28, we achieve an improvement of 3.5dB in DR and 1dB in SNDR.

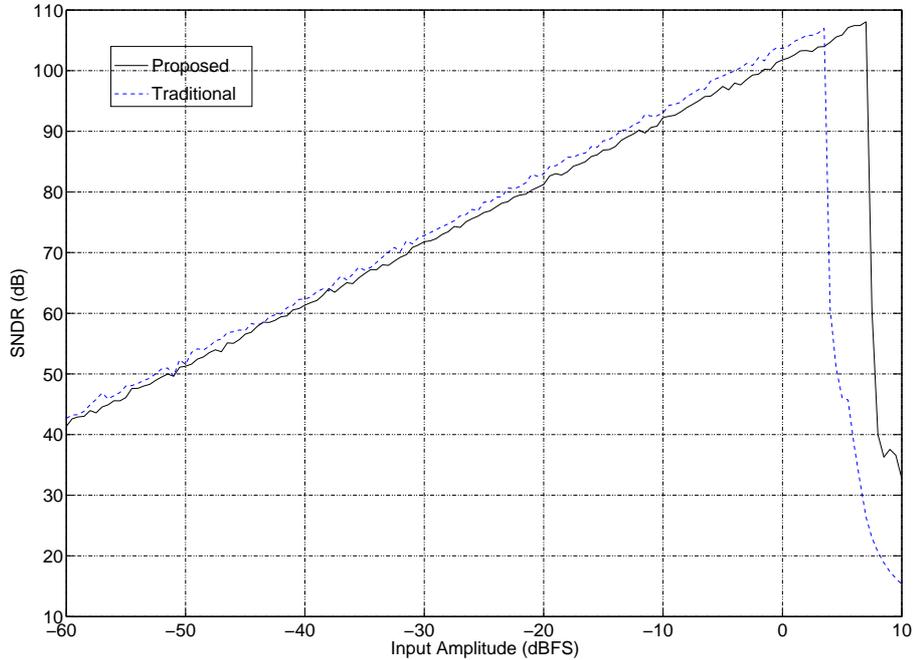


Figure 4.28: Extended DR obtained by auxiliary quantizer and ideal DACs

The real advantage of the proposed structure becomes evident in the presence of DAC nonlinearities since it is very robust against them in contrast to the traditional structure. Next, the modeling of DAC nonlinearities with mean 0 and variance 1% has been introduced in these two structures. The simulation result presented in Fig. 4.29 shows that the traditional modulator loses 10dB of peak SNDR, while the proposed structure only loses 4dB. Thus, eventually, in the presence of DAC nonlinearities, the proposed structure provides a 7dB better performance than the traditional one from the peak SNDR standpoint and 4dB performance improvement from the DR standpoint.

At -20dBFS input signal, the spectrum of the output signal of two modulators has been captured and exposed in Fig. 4.30.

It shows that the noise floor of the traditional topology is more elevated than the proposed one, because of its sensitivity to DAC nonlinearities. There are no signal distortions in both cases because these are multi-stage systems and multi-bit quantizers only process the quantization noise of first stage. So any DAC nonlinearities only result in noise floor elevation, which is more in the case of traditional scheme than the proposed one.

## 4.6 Conclusion

In this chapter, the principle of high-pass  $\Delta\Sigma$  modulator has been presented. Ideal performance of a high-pass  $\Delta\Sigma$  modulator is equivalent to that of the corresponding low-pass

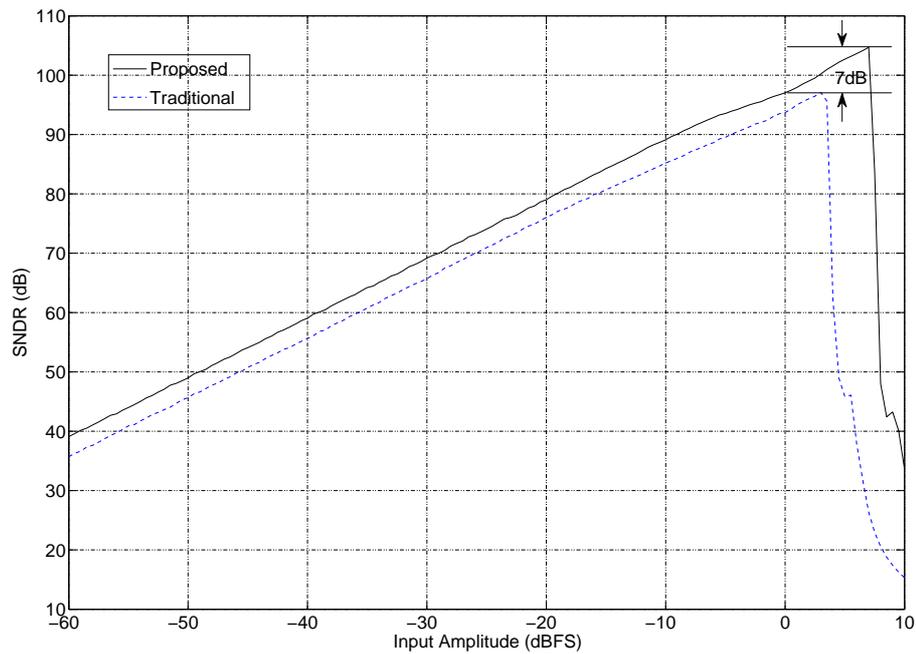


Figure 4.29: Performance comparison of two GMSCl HP structures with 1% DAC nonlinearities

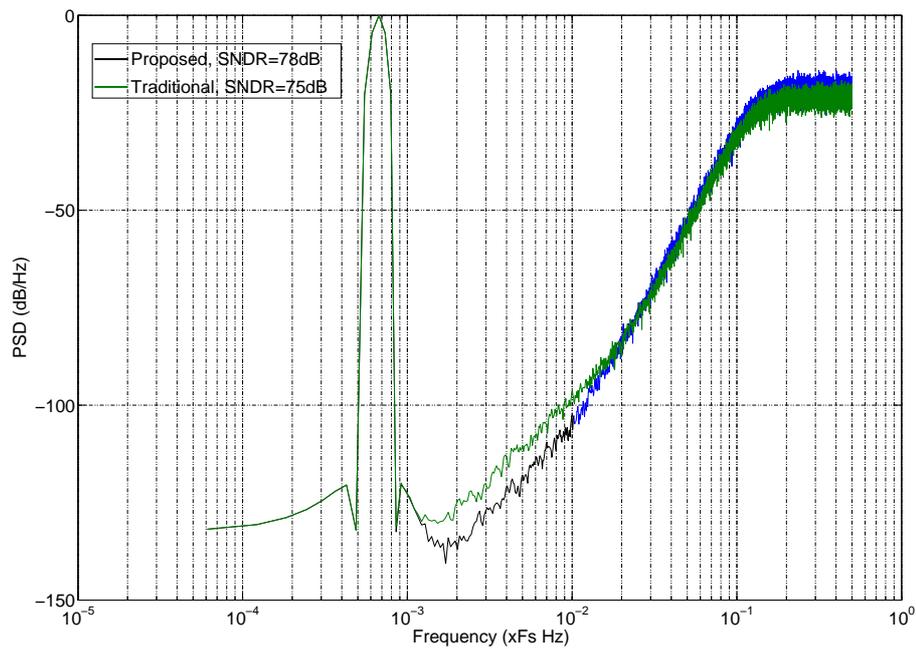


Figure 4.30: Output spectrum of two GMSCl topologies showing the high DAC nonlinearity immunity of the Proposed scheme

modulator. But in the presence of low-frequency noise, high-pass modulator performs much better since it eliminates completely the low frequency noise. Traditional architecture of high-pass modulator has been presented, followed by two more state-of-the-art feedforward topologies. A new feedforward topology has been proposed which results in the simplified design since it eliminates the need of a summing amplifier and performs better in the presence of op-amp non-idealities as shown in simulation results. A new MASH structure for high-pass  $\Delta\Sigma$  modulator has also been presented which increases the input dynamic range by and highest-achieved SNDR significantly. Finally an enhanced version of MSCL called GMSCL has been elaborated which is free from digital cancellation filters and reduces the circuit complexity. A new architecture of GMSCL has been presented which is based on the proposed second-order feedforward topology. This new GMSCL high-pass modulator achieves 10dB of SNDR over already established GMSCL structure and reduces the circuit complexity and power consumption.

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## Chapter 5

# High-Pass Filter Implementation

### 5.1 Introduction

High Pass filter is a major building block of HP  $\Delta\Sigma$  modulator. It enjoys the same importance in an HP modulator as an integrator enjoys in an LP modulator. The transfer function for the HP filter is realised by applying the transformation,  $z \rightarrow -z$ , to a SC integrator:

$$H_{LP}(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (5.1)$$

resulting in:

$$H_{HP}(z) = \frac{-z^{-1}}{1 + z^{-1}} \quad (5.2)$$

This filter has a zero at dc in contrast to a zero at  $F_s/2$  for the SC integrator. This transfer function can be described such that, each output sample is the negative of the sum of the previous input and the previous output. HP filter design has been a major bottle neck in the development of HP modulators. In the absence of an efficient HP filter little progress could be made in HP modulators. But recently, some interesting designs have been proposed. This chapter presents three state of the art of HP filters namely integrator-based filter, chopper-based filter and improved filter. The integrator-based filter is realized by introducing a feedback loop around the integrator by using a capacitor which is twice the size of the integrating capacitor. The chopper-based filter on the other is based on chopping the input signal and output signal of the integrator thus performing the signal processing in baseband. The improved structure, combines the advantages of both filters and rejects their shortcomings. The brief review of each filter is followed by detailed theoretical analysis. In the end the theoretical claims are proved by SPECTRE-simulation results.

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## 5.2 Integrator-based Structure

The first HP filter implementation shown in Fig. 5.1 was presented in [27] for band-pass  $\Delta\Sigma$  modulator implementation.

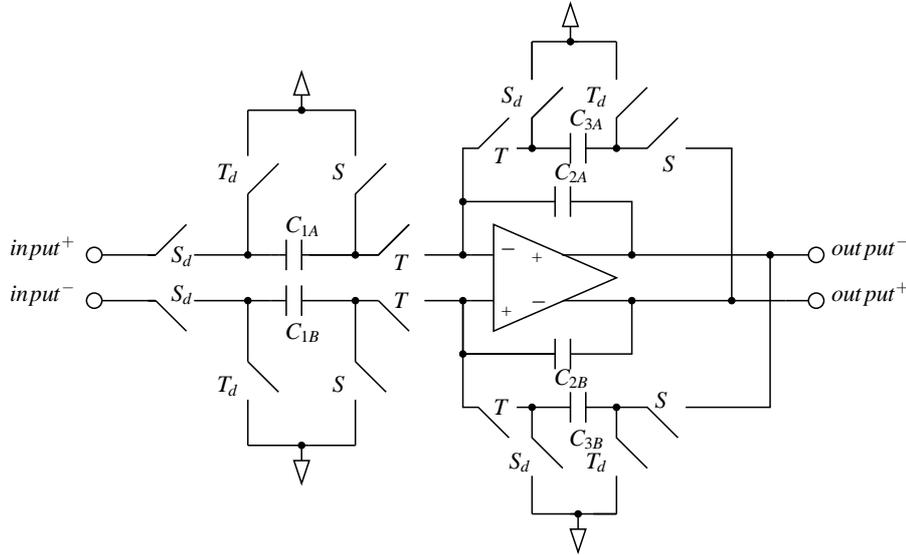


Figure 5.1: HP filter made by a feedback loop around integrator

It is designed by introducing an extra feed-back loop around the integrator, such that the transfer function for the HP filter is realised. This implementation suffers from various drawbacks which are listed as:

1. It has increased sensitivity to noise in the amplifier [28], as the extra feed-back loop results in the amplifier noise being sampled by both the integrating capacitor and the extra feed-back capacitor
2. The switches thermal noise level contribution to the output is augmented
3. The extra feedback capacitors significantly increase the capacitive loading of the amplifier, increasing the power consumption [27]

However, this implementation offers many advantages when compared to a band-pass solution, allowing the specifications for the amplifier design to be relaxed significantly [87].

### 5.2.1 Switch Noise

Two noise sources intrinsic to the MOS switches, thermal noise and flicker or  $1/f$  noise, can potentially corrupt the filter output. Thermal noise is caused by the random motion of charge carriers in the channel of the device. This results in random fluctuation of the drain current.  $1/f$  noise is generated by trapping and release of charge carriers during their

movement in the channel. It is associated with flow of direct current in the device. In the analysis of switch noise below,  $1/f$  noise is considered negligible because the current flow in these switches consists of short pulses occurring at the clock rate and hence there is no continuous flow of charge. The thermal noise contributed by the MOS switches in this HP filter can be estimated by modeling each switch path with the sample-and-hold circuit shown in Fig. 5.2.

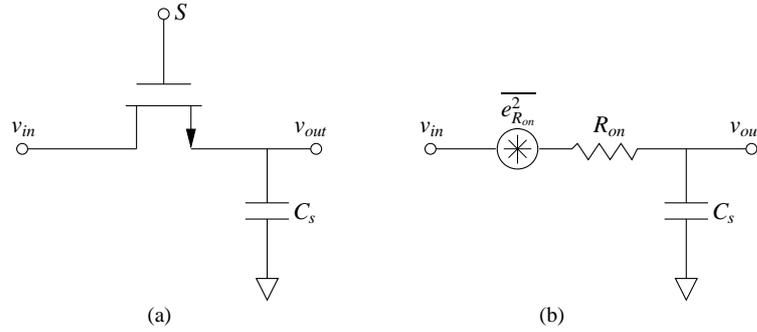


Figure 5.2: (a)MOS sample-and-hold circuit, (b)its equivalent noisy circuit when  $S$  is high

When  $S$  is high and the MOS switch is on, the channel is modeled as a noiseless resistor,  $R_{on}$ , in series with a noise source,  $e_{R_{on}}$ , that has a power spectral density:

$$S_R(f) = 4kTR_{on} \left[ \frac{V^2}{Hz} \right], \quad 0 < f < \infty \quad (5.3)$$

where  $k$  is Boltzmann's constant and  $T$  is absolute temperature. The mean square value of the noise sampled onto capacitor  $C_S$  is determined by integrating the noise power spectral density,  $S_R(f)$ , shaped by  $|H(f)|^2$ , where  $H(f)$  is the transfer function of the low-pass filter made by  $R_{on}$  and  $C_S$ :

$$\overline{e_{out}^2} = \int_0^\infty \frac{4kTR_{ON}}{1 + (2\pi f R_{ON} C_S)^2} df = \frac{kT}{C_S} [V^2], \quad 0 < f < \infty \quad (5.4)$$

Since the sampling frequency,  $F_s$ , is much lower than the circuit bandwidth set by  $R_{on}$  and  $C_S$ , it can be shown that the process of sampling the switch noise results in the distribution of the total noise power  $kT/C_S$  into the sampling bandwidth,  $-F_s/2$  to  $F_s/2$  in a uniform fashion due to aliasing [82]. In this HP filter, it can be seen in Fig. 5.1 that during the sampling phase, switch noise is sampled onto capacitors  $C_{1A}$ ,  $C_{1B}$ ,  $C_{3A}$ , and  $C_{3B}$ . During the charge-transfer phase, additional noise is sampled when the charge from capacitors  $C_{1A}$ ,  $C_{1B}$ ,  $C_{3A}$ , and  $C_{3B}$  is transferred to the integration capacitors,  $C_{2A}$  and  $C_{2B}$ . Since the noise sources are uncorrelated, their powers add. Therefore, the total power of the switch noise referred to the filter input is:

$$\overline{e_{switch}^2} = kT \left( \frac{2}{C_{1A}} + \frac{2}{C_{1B}} + \frac{2}{C_{3A}} + \frac{2}{C_{3B}} \right) \quad (5.5)$$

In this expression, the factor of 2 accounts for the fact that noise is sampled during both the sampling and charge-transfer phases, and it has been assumed that the noise sampled during both phases is bandlimited by the switch resistance and the sampling capacitor. This assumption results in an overestimate of the noise contribution during the charge-transfer phase because the charge-transfer process is actually bandlimited by the operational amplifier, not by the switch network. Sampling capacitances are  $C_{1A} = C_{1B} = C_S$ , and for an HP filter gain of 0.5, feed-back capacitances are  $C_{3A} = C_{3B} = 4 \times C_S$  to achieve the HP filter transfer function. With these values, the total noise power due to switches simplifies to:

$$\overline{e_{switch,filter}^2} = \frac{5kT}{C_S} \quad (5.6)$$

### 5.3 Op-Amp Noise

In addition to  $kT/C$  noise from the switches, noise from the op-amp also degrades the performance of the filter. In the following analysis, it is presumed that all noise sources within the amplifier can be referred to a source at the amplifier's non-inverting input, denoted  $e_{amp}$  in Fig. 5.3.

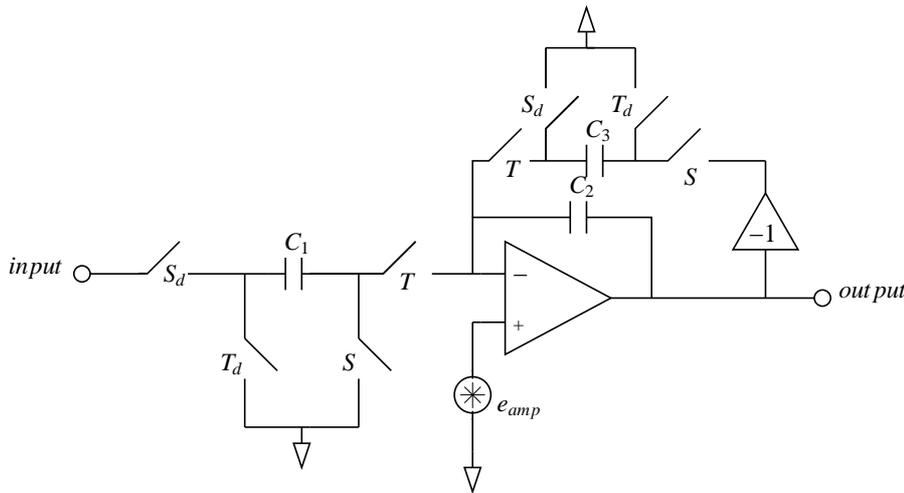


Figure 5.3: Single-ended integrator-based HP filter with op-amp noise

The analysis is simplified by using a single-ended representation of the filter, but no error is inherent in this simplification because  $e_{amp}$  is defined to equal the input-referred noise of the actual amplifier used in the fully-differential filter. Capacitor  $C_3$  is chosen to be  $2 \times C_2$  to yield the desired HP transfer function. The input-referred amplifier noise spectral density,  $S_{amp}(f)$ , typically consists of a white noise component, which is characterized by a power spectral density that is constant with frequency, and a  $1/f$  noise component that is inversely proportional to frequency. In this HP filter,  $1/f$  noise can be neglected because it is concentrated in a narrow region around dc, whereas the signal is centered at one-half of

the sampling frequency,  $F_s/2$ . The input-referred amplifier noise power,  $\overline{e_{amp}^2}$ , is limited by the overall closed-loop bandwidth of the filter, which is largest during the sampling phase. Then, as in the case of switch noise, it can be reasonably assumed that sampling the amplifier noise,  $e_{amp}$  distributes it uniformly across the filter sampling bandwidth,  $-F_s/2$  to  $F_s/2$ . To study the impact of the op-amp's noise on the performance of the filter, charge-transfer equations have been solved resulting in the time-domain difference equation describing the filter operation:

$$v_o[n] + v_o[n - 1] = \frac{C_1}{C_2}v_{in}[n - 1] + \left(2 + \frac{C_1}{C_2}\right)e_{amp}[n - \frac{1}{2}] + e_{amp}[n] - e_{amp}[n - 1] \quad (5.7)$$

This expression reveals that the filter operation amplifies the opamp noise power in two ways. First, Eqn. 5.7 indicates that the power of the noise term  $e_{amp}[n - 1/2]$  is magnified by  $(1 + 2C_2/C_1)^2$  with respect to the power of the input signal. This noise amplification factor can be large if the filter gain ( $C_1/C_2$ ) is less than one, as in the design of this modulator. A second effect is that a first-order differencing of  $e_{amp}$  is also referred to the input of the filter. In the frequency domain, a first-order differencing is equivalent to a first-order highpass shaping function that has a zero at dc and a maximum at one-half of the filter sampling frequency,  $F_s/2$ . This shaping is beneficial if the input signal is located near dc, as in a lowpass modulator. Unfortunately, in the HP modulator, the signal passband is centered precisely at  $F_s/2$ , where the shaping function applied to the amplifier noise has its maximum amplitude. In other words, the amplifier noise is shaped to have a maximum spectral density in the desired passband. The preceding discussion provides a qualitative feel for the noise behavior of the integrator-based HP filter with respect to the amplifier. However, it is difficult to quantitatively assess the impact of amplifier noise,  $e_{amp}$ , on the performance of the proposed modulator by only considering the stand-alone filter. This effect is not evident from a consideration of the HP filter alone but that of the complete modulator incorporating this filter. The effect of amplifier noise by using this type of HP filter in the proposed modulator is assessed by analyzing the modulator with two independent amplifier noise sources,  $e_{amp1}$  and  $e_{amp2}$ . A block diagram of the noisy HP modulator is shown in Fig. 5.4.

Once again, a single-ended representation is used for simplicity, and it is recognized that the -1 buffers represent the interchange of terminals in the fully-differential circuit. Modeling the quantizer in Fig. 5.4 as a gain,  $G$ , with an additive noise source,  $E(z)$ , it can be shown that the output of the highpass modulator is described in the z-domain by:

$$Y(z) = \frac{0.2G \cdot X(z) + (1 + z^{-1})^2 E(z)}{1 + (2 - 0.4G) \cdot z^{-1} + (1 - 0.2G) \cdot z^{-2}} + NTF_{amp1}(z) \cdot e_{amp1}(z) + NTF_{amp2}(z) \cdot e_{amp2}(z) \quad (5.8)$$

where the noise transfer functions for  $e_{amp1}$  and  $e_{amp2}$  are respectively,

$$NTF_{amp1}(z) = \frac{0.4G \cdot z^{-1} \cdot (1 + 2.5z^{-1/2} - z^{-1})}{1 + (2 - 0.4G)z^{-1} + (1 - 0.2G)z^{-2}} \quad (5.9)$$

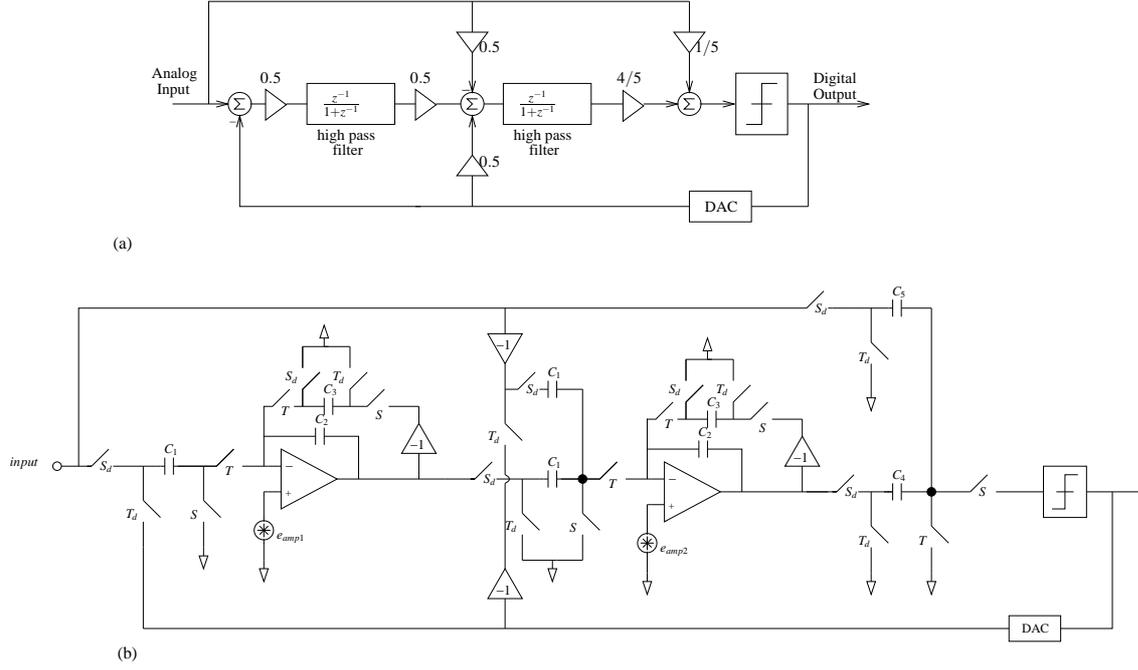


Figure 5.4: (a)Block diagram, (b)single-ended SC realization of the proposed HP modulator using integrator-based filter with associated opamp noise sources

and

$$NTF_{amp2}(z) = \frac{0.8G \cdot (1 + z^{-1}) \cdot (1 + 3z^{-1/2} - z^{-1})}{1 + (2 - 0.4G)z^{-1} + (1 - 0.2G)z^{-2}} \quad (5.10)$$

Recall that  $z^{-1}$  is interpreted as a single delay with respect to the sampling rate. Eqns. 5.8, 5.9, and 5.10 can be simplified by setting the gain of the quantizer,  $G$ , to 5. This yields:

$$NTF_{amp1}(z) = 2 \cdot z^{-1} \cdot (1 + 2.5z^{-1/2} - z^{-1}) \quad (5.11)$$

and

$$NTF_{amp2}(z) = 4 \cdot (1 + z^{-1}) \cdot (1 + 3z^{-1/2} - z^{-1}) \quad (5.12)$$

which, in the frequency domain, can be written as:

$$NTF_{amp1}(f) = 2 \cdot e^{-j2\pi fT_s} (1 + 2.5e^{-j2\pi fT_s/2} - e^{-j2\pi fT_s}) \quad (5.13)$$

and

$$NTF_{amp2}(f) = 4 \cdot (1 + e^{-j2\pi fT_s}) \cdot (1 + 3e^{-j2\pi fT_s/2} - e^{-j2\pi fT_s}) \quad (5.14)$$

where  $T_s$  is the sampling period. If  $\overline{e_{amp1}^2}$  is the input-referred noise power of the first-stage amplifier, then the spectral density of the shaped noise from  $e_{amp1}$  is:

$$S_{amp1,out}(f) = |NTF_{amp1}(f)|^2 \times \frac{\overline{e_{amp1}^2}}{F_s}, \quad -\frac{F_s}{2} < f < \frac{F_s}{2} \quad (5.15)$$

Similarly, the spectral density of the shaped noise from  $e_{amp2}$  is:

$$S_{amp2,out}(f) = |NTF_{amp2}(f)|^2 \times \frac{\overline{e_{amp2}^2}}{F_s}, \quad -\frac{F_s}{2} < f < \frac{F_s}{2} \quad (5.16)$$

given that  $\overline{e_{amp2}^2}$  is the input-referred noise power of the second-stage amplifier. Next, it is noted that the signal passband is centered at  $\pm F_s/2$ , and the passband bandwidth is assumed to be much less than  $F_s$ . Therefore, in the passband, the spectral density of the shaped noise from  $e_{amp1}$  and  $e_{amp2}$  can be approximated as:

$$\begin{aligned} S_{amp1,inband}(f) &\approx S_{amp1,out}(f)|_{f=F_s/2} \\ &= |NTF_{amp1}(f)|_{f=F_s/2}^2 \times \frac{\overline{e_{amp1}^2}}{F_s} \\ &= 41 \times \frac{\overline{e_{amp1}^2}}{F_s} \end{aligned} \quad (5.17)$$

and,

$$\begin{aligned} S_{amp2,inband}(f) &\approx S_{amp2,out}(f)|_{f=F_s/2} \\ &= |NTF_{amp2}(f)|_{f=F_s/2}^2 \times \frac{\overline{e_{amp2}^2}}{F_s} \\ &= 0 \times \frac{\overline{e_{amp2}^2}}{F_s} = 0 \end{aligned} \quad (5.18)$$

The important and disturbing implication of Eqn. 5.17 is that within the passband, noise power from the first amplifier is amplified by a factor of 41 at the output of the proposed modulator. Fortunately, Eqn. 5.18 indicates that the inband noise contribution from the second amplifier is negligible because the noise shaping function  $NTF_{amp2}(f)$  has a zero at  $F_s/2$ . From Eqns. 5.17 and 5.18, the power of the amplifier noise present in the signal band is approximately:

$$\begin{aligned} \overline{e_{amp,inband}^2} &\approx [S_{amp1,inband}(f) + S_{amp2,inband}(f)] \times B \\ &= 41 \times \frac{\overline{e_{amp1}^2}}{F_s} \times B \end{aligned} \quad (5.19)$$

where  $B$  is the width of the passband.

### 5.3.1 Parasitic Capacitances

Parasitic capacitance is the unavoidable and usually unwanted capacitance that exists between the parts of an electronic component or circuit because of their proximity to each other. All actual circuit elements such as inductors, diodes, and transistors have internal capacitance, which can cause their behavior to depart from that of 'ideal' circuit elements. In addition, parasitic capacitance can exist between closely spaced conductors, such as wires or printed circuit board traces. In CMOS processes, multiple parasitic capacitances disturb the normal operations of transistors. They are  $C_{gs}$ ,  $C_{gd}$ ,  $C_{sb}$  and  $C_{db}$  as illustrated for an NMOS in Fig. 5.5.

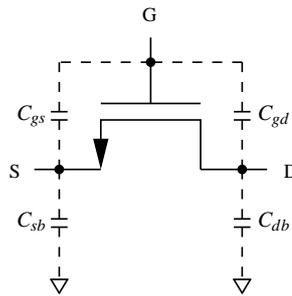


Figure 5.5: NMOS with parasitic capacitances

The parasitic capacitances in CMOS technologies also arise due to coupling between capacitor plates and the substrate. The impact of these parasitic capacitances can be analysed for a particular SC filter by solving its charge transfer equations and studying the output. Fig. 5.5 shows the integrator-based filter with the switch and capacitor plates parasitics. For switches,  $C_{sb}$  and  $C_{db}$  have been taken into account, while  $C_{gs}$  and  $C_{gd}$  have been ignored to facilitate the analysis.

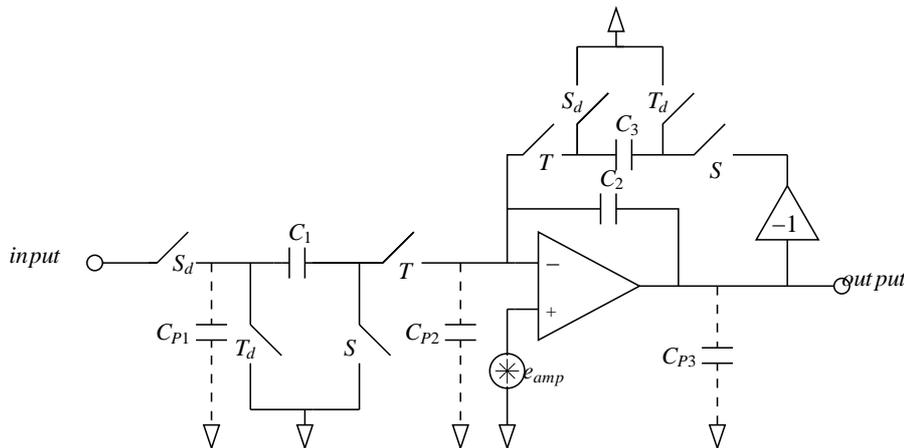


Figure 5.6: Single-ended integrator-based HP filter in the presence of opamp noise and parasitic capacitances

To further understand the working of this circuit, it has been broken into its constituent phases  $S$  and  $T$  in Fig. 5.7. Intuitive analysis suggests that parasitic  $C_{P3}$  has no influence on the output since it just charged by the opamp and not discharged.

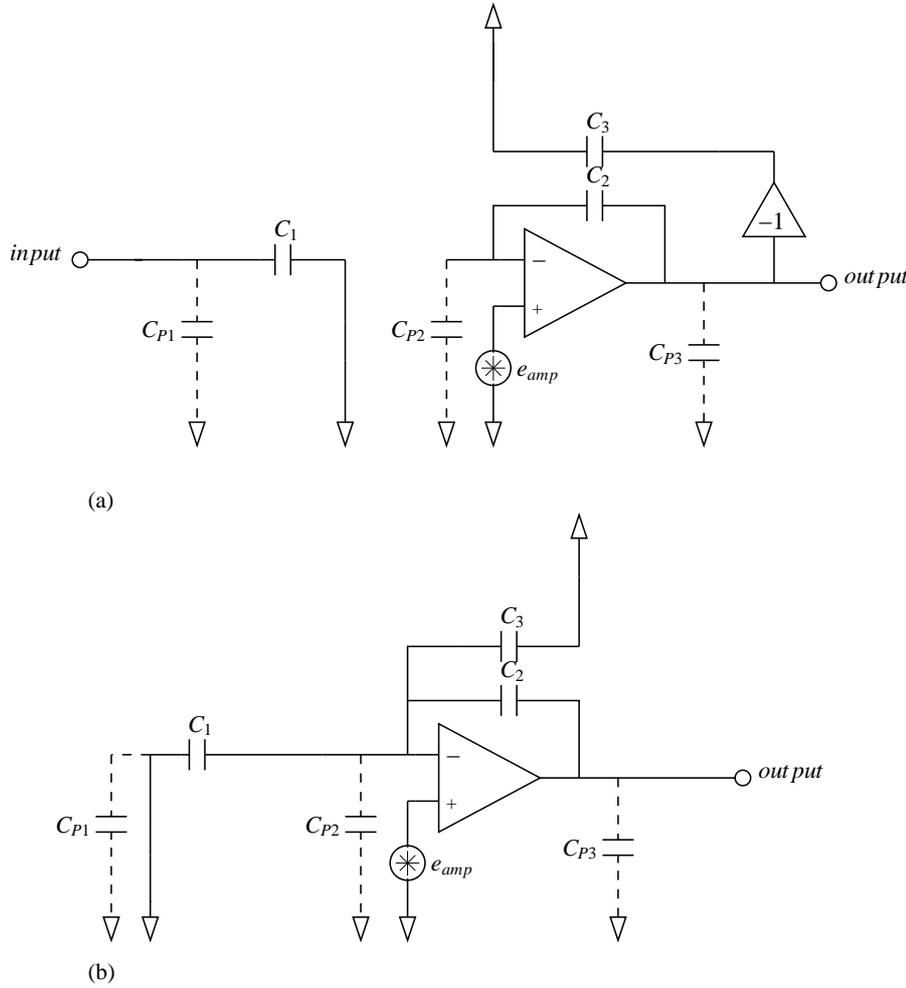


Figure 5.7: (a) Circuit configuration in phase  $S$ , (b) phase  $T$

The parasitic capacitance  $C_{P1}$  is charged to the input signal voltage in phase  $S$ . And during the charge-transfer phase  $T$ , this parasitic is discharged to the ground without affecting the output. The effect of  $C_{P2}$  is tricky since the voltage across it changes in two phases with opamp noise  $e_{amp}$  and the difference is discharged into  $C_2$ . The solution of charge transfer equation provides the result:

$$v_o[n] + v_o[n-1] = \frac{C_1}{C_2} v_{in}[n-1] + \left(2 + \frac{C_1}{C_2}\right) e_{amp}\left[n - \frac{1}{2}\right] + \left(1 + \frac{C_{P2}}{C_2}\right) e_{amp}[n] - \left(1 + \frac{C_{P2}}{C_2}\right) e_{amp}[n-1] \quad (5.20)$$



op-amp. Solving charge-transfer equations for this filter, keeping in view the charge-conservation law, the practical transfer function in terms of capacitances and op-amp dc-gain  $A_0$  is given by:

$$H_{practical}(z) = \frac{C_s}{C_i} \frac{\frac{A_0}{\frac{C_s}{C_i} + \frac{C_p}{C_i} + A_0 + 3} z^{-1}}{1 + \frac{\frac{C_p}{C_i} + A_0 - 1}{\frac{C_s}{C_i} + \frac{C_p}{C_i} + A_0 + 3} z^{-1}} \quad (5.23)$$

where  $\frac{C_s}{C_i} = b$  is the gain of the filter and  $\frac{C_p}{C_i} = p$  is the gain of the parasitic voltage. Replacing these values in Eqn. 5.23:

$$H_{practical}(z) = b \frac{\frac{A_0}{b+p+A_0+3} z^{-1}}{1 + \frac{p+A_0-1}{b+p+A_0+3} z^{-1}} \quad (5.24)$$

The value of  $b$  for the first HP filter in the proposed modulator is 0.5, assuming a reasonable value of 0.01 for  $p$ , the exact transfer function of this filter turns out to be:

$$H_{practical}(z) = 0.5 \frac{\frac{A_0}{A_0+3.51} z^{-1}}{1 + \frac{A_0-0.99}{A_0+3.51} z^{-1}} \quad (5.25)$$

Therefore the values of  $\alpha$  and  $\beta$  are given by:

$$\alpha = \frac{A_0}{A_0 + 3.51}, \quad \beta = \frac{A_0 - 0.99}{A_0 + 3.51} \quad (5.26)$$

Using Eqn. 5.25 as the transfer function for the first HP filter of the proposed modulator, it is simulated at a range of values of  $A_0$  to analyse the effect of this non-ideality. The input signal is a sinusoid at an amplitude of 0.4 normalized with respect to quantization step i-e -8dBFS at frequency of  $0.4993F_s$ . The simulation result is shown in Fig. 5.9:

This figure shows that the integrator-based filter used in proposed architecture requires the minimum op-amp dc gain of 45dB to acquire the ideal signal to quantization noise ratio (SQNR) for the fixed input amplitude.

### 5.3.2.2 Finite Gain-Bandwidth Product and Slew Rate

Finite Gain Bandwidth Product (GBW) and Slew Rate (SR) are responsible for incomplete or inaccurate charge transfer in SC circuits. With the assumption of a single-pole model for the op-amp, the output transient of this high-pass filter during  $n$ th integration phase is represented by:

$$v_{out}(t) = v_{out}(nT_s - T_s) + (-(1 + \beta)v_{out}(nT_s - T_s) + b\alpha v_{in}) \times (1 - e^{-\frac{t}{\tau}}), \quad 0 < t < \frac{T_s}{2} \quad (5.27)$$

where  $v_{out}$  is the output of the filter,  $T_s = 1/F_s$  is the sampling period,  $v_{in}$  is the input of the filter and  $\tau = (3 + b)/2\pi GBW$  is the time constant of the op-amp comprising the filter. In this equation, the term  $-2\beta v_{out}(nT_s - T_s)$  represents the discharge of the feedback

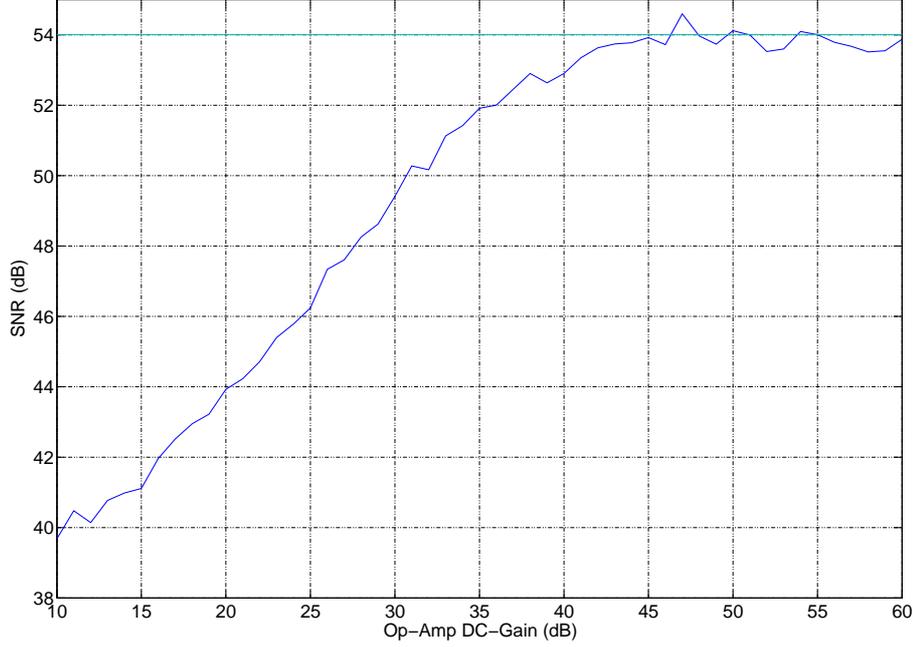


Figure 5.9: SNR vs. Op-Amp DC-Gain

capacitor  $C_3$ , and the term  $b\alpha v_{in}$  reflects the discharge of the sampling capacitor  $C_1$ ; both of them discharge into the integrating capacitor  $C_2$ . If this high-pass filter represents the first high-pass filter of a second order modulator,  $v_{in}$  is given by:

$$v_{in} = x(nT_s - T_s/2) - y(nT_s - T_s) \quad (5.28)$$

where  $x$  is the input of the modulator and  $y$  is the output of the modulator.

Slew rate of an op-amp is the maximum rate of voltage change that it can provide at its output. Unfortunately it is practically a finite quantity that is dependant on the bias current of the op-amp and its load capacitance. With this nonideality of the opamp, the output transient of this HP filter turns out to be:

$$v_{out}(t) = v_{out}(nT_s - T_s) + V_s - \text{sgn}(V_s)SR_s\tau e^{-\left(\frac{T_s}{2\tau} - \frac{|V_s|}{SR_s\tau} + 1\right)} \quad (5.29)$$

where  $V_s$  is given by:

$$V_s = -(1 + \beta)v_{out}(nT_s - T_s) + b\alpha v_{in} \quad (5.30)$$

Finite SR supplied by the op-amp results in changing the gain of the HP filter in a non-linear fashion and produces harmonics in the output degrading the SNDR.

Two simulations are performed by fixing the GBW of the opamp and varying the values of  $SR_s$  and observing the output SNDR. The result is illustrated in Fig. 5.10:

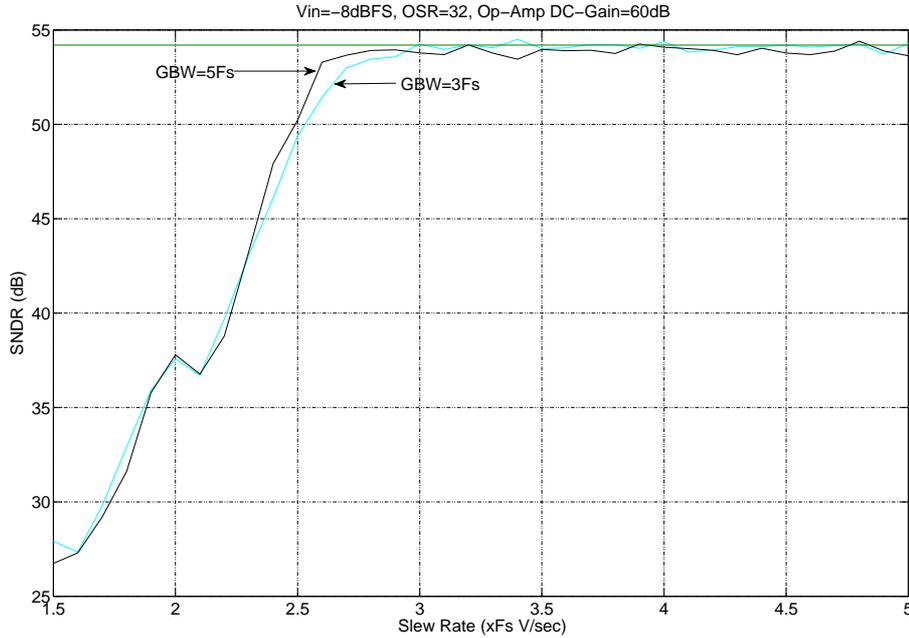


Figure 5.10: SNDR vs. SR for proposed modulator implemented with integrator-based HP filter at fixed input amplitude, opamp DC-gain and GBW

The result shows that atleast a  $SR_s$  of  $4.2 \times F_s (V/sec)$  at a GBW of  $5F_s$  is needed for the proposed modulator architecture with integrator-based filter to establish the required performance.

## 5.4 Chopper-based Structure

The second implementation as shown in Fig. 5.11, is based on the approach of modulating the input signal down to base band, where the signal is integrated by the SC integrator and then modulated back up to the IF frequency.

However, the signal processing still occurs at base band within the SC integrator. The benefits achieved by moving to an IF solution are lost once the signal is modulated back down to base band in the analog domain, reintroducing the need for chopper stabilization (CHS) and correlated double sampling (CDS).

### 5.4.1 Switch Noise

In this HP filter, switch noise is sampled onto capacitors  $C_{1A}$  and  $C_{1B}$  during sampling phase  $S$ . During the charge-transfer phase, additional noise is sampled when the charge from these capacitors is transferred to the capacitors,  $C_{2A}$  and  $C_{2B}$ . This gives the total power of the switch noise referred to the filter input as:

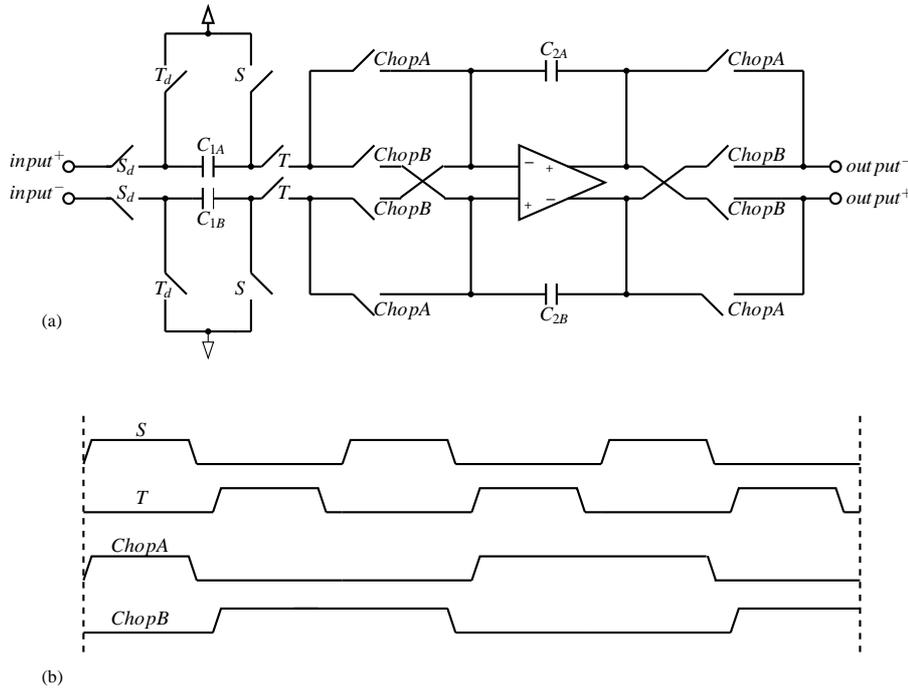


Figure 5.11: (a) HP filter made by chopping the input and output signal of integrator, (b) Its associated timing diagram

$$\overline{e_{switch}^2} = kT \left( \frac{2}{C_{1A}} + \frac{2}{C_{1B}} \right) \quad (5.31)$$

where the factor of 2 accounts for the noise sampling in both sampling and charge-transfer phases. With the sampling capacitances of  $C_{1A} = C_{1B} = C_S$ , the total input referred switch noise power is:

$$\overline{e_{switch,filter2}^2} = \frac{4kT}{C_S} \quad (5.32)$$

Thus, comparing Eqns. 5.6 and 5.32, it can be shown that chopper-based structure provides 1dB reduction in switch-noise over integrator-based structure.

### 5.4.2 Op-Amp Noise

To study the impact of op-amp noise on chopper-based HP filter, its single-ended version with op-amp noise is shown in Fig. 5.12:

In this filter, unlike the integrator-based filter,  $1/f$  noise of the op-amp cannot be neglected because the signal is chopped to low frequencies before being processed by the op-amp. Thus the low-frequency noises of op-amp directly corrupt the useful signal. However, to keep the analysis tractable, it is assumed that sampling the amplifier noise,  $e_{amp}$ , distributes it uniformly across the filter sampling bandwidth,  $-F_s/2$  to  $F_s/2$ . Solving the

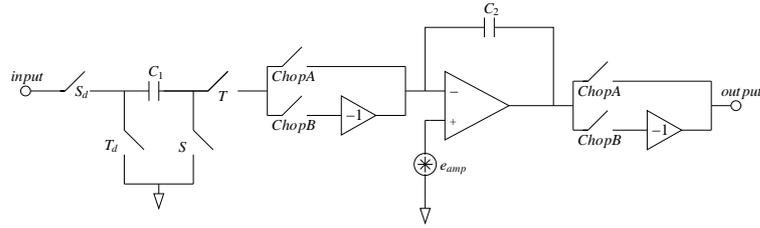


Figure 5.12: Single-ended chopper-based HP filter with op-amp noise

charge transfer equations of the filter, gives the time-domain equation describing the filter operation:

$$v_o[n] + v_o[n - 1] = \frac{C_1}{C_2} v_{in}[n - 1] + \left( \frac{C_1}{C_2} \right) e_{amp}[n - \frac{1}{2}] + e_{amp}[n] - e_{amp}[n - 1] \quad (5.33)$$

This result illustrates that the noise term  $e_{amp}[n - 1/2]$  experiences the same amplification as the input signal, in contrast to the integrator-based structure, where it undergoes increased amplification compared to the input signal as shown in Eqn. 5.7. On the other hand, like the integrator-based structure, first-order differencing of the opamp noise is referred to the input making the filtering of the noise in such a way that it has the highest level near the passband. To gain more insight into the noise performance of this filter, it is incorporated in the proposed second-order HP filter with its associated noise sources, as shown in Fig. 5.13.

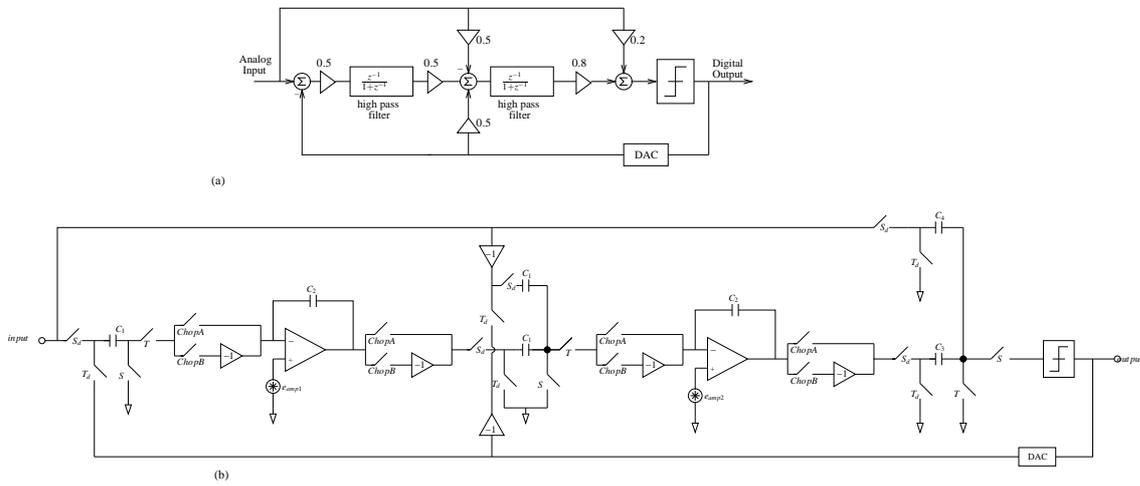


Figure 5.13: (a)Block diagram, (b)single-ended SC realization of the proposed HP modulator using chopper-based filter with associated opamp noise sources

Performing the necessary analysis, the output of this HP modulator in the z-domain turns out to be:

$$Y(z) = \frac{0.2G \cdot X(z) + (1 + z^{-1})^2 E(z)}{1 + (2 - 0.4G) \cdot z^{-1} + (1 - 0.2G) \cdot z^{-2}} + NTF_{amp1}(z) \cdot e_{amp1}(z) + NTF_{amp2}(z) \cdot e_{amp2}(z) \quad (5.34)$$

where the noise transfer functions for  $e_{amp1}$  and  $e_{amp2}$  are respectively,

$$NTF_{amp1}(z) = \frac{0.4G \cdot z^{-1} \cdot (1 + 0.5z^{-1/2} - z^{-1})}{1 + (2 - 0.4G)z^{-1} + (1 - 0.2G)z^{-2}} \quad (5.35)$$

and

$$NTF_{amp2}(z) = \frac{0.8G \cdot (1 + z^{-1}) \cdot (1 + z^{-1/2} - z^{-1})}{1 + (2 - 0.4G)z^{-1} + (1 - 0.2G)z^{-2}} \quad (5.36)$$

Simplifying Eqns. 5.34, 5.35, and 5.36 by setting the gain of the quantizer,  $G$ , to 5 yields:

$$NTF_{amp1}(z) = 2 \cdot z^{-1} \cdot (1 + 0.5z^{-1/2} - z^{-1}) \quad (5.37)$$

and

$$NTF_{amp2}(z) = 4 \cdot (1 + z^{-1}) \cdot (1 + z^{-1/2} - z^{-1}) \quad (5.38)$$

which, in the frequency domain, can be written as:

$$NTF_{amp1}(f) = 2 \cdot e^{-j2\pi f T_s} (1 + 0.5e^{-j2\pi f T_s/2} - e^{-j2\pi f T_s}) \quad (5.39)$$

and

$$NTF_{amp2}(f) = 4 \cdot (1 + e^{-j2\pi f T_s}) \cdot (1 + e^{-j2\pi f T_s/2} - e^{-j2\pi f T_s}) \quad (5.40)$$

where  $T_s$  is the sampling period. If  $\overline{e_{amp1}^2}$  is the input-referred noise power of the first amplifier, then the spectral density of the shaped noise from  $e_{amp1}$  is:

$$S_{amp1,out}(f) = |NTF_{amp1}(f)|^2 \times \frac{\overline{e_{amp1}^2}}{F_s}, \quad -\frac{F_s}{2} < f < \frac{F_s}{2} \quad (5.41)$$

Similarly, the spectral density of the shaped noise from  $e_{amp2}$  is:

$$S_{amp2,out}(f) = |NTF_{amp2}(f)|^2 \times \frac{\overline{e_{amp2}^2}}{F_s}, \quad -\frac{F_s}{2} < f < \frac{F_s}{2} \quad (5.42)$$

given that  $\overline{e_{amp2}^2}$  is the input-referred noise power of the second amplifier. Next, it is noted that the signal passband is centered at  $\pm F_s/2$ , and the passband bandwidth is assumed to be much less than  $F_s$ . Therefore, in the passband, the spectral density of the shaped noise from  $e_{amp1}$  and  $e_{amp2}$  can be approximated as:

---

$$\begin{aligned}
S_{amp1,inband}(f) &\approx S_{amp1,out}(f)|_{f=F_s/2} \\
&= |NTF_{amp1}(f)|_{f=F_s/2}^2 \times \frac{\overline{e_{amp1}^2}}{F_s} \\
&= 17 \times \frac{\overline{e_{amp1}^2}}{F_s}
\end{aligned} \tag{5.43}$$

and,

$$\begin{aligned}
S_{amp2,inband}(f) &\approx S_{amp2,out}(f)|_{f=f_s/2} \\
&= |NTF_{amp2}(f)|_{f=f_s/2}^2 \times \frac{\overline{e_{amp2}^2}}{f_s} \\
&= 0 \times \frac{\overline{e_{amp2}^2}}{f_s} = 0
\end{aligned} \tag{5.44}$$

With Eqn. 5.43, it can be deduced that near the useful signal, noise power from the first opamp is amplified 17 times at the output of the modulator. While, fortunately, the noise power of the second opamp is attenuated at the output because its shaping function  $NTF_{amp2}(f)$  has a zero at  $F_s/2$ . Using Eqns. 5.43 and 5.44, the power of the amplifier noise present in the signal band can be approximated by:

$$\begin{aligned}
\overline{e_{amp,inband}^2} &\approx [S_{amp1,inband}(f) + S_{amp2,inband}(f)] \times B \\
&= 17 \times \frac{\overline{e_{amp1}^2}}{F_s} \times B
\end{aligned} \tag{5.45}$$

where  $B$  is the width of the passband. The first look at Eqns. 5.45 and 5.19 suggests that chopper-based filter gives better performance than integrator-based filter as its opamp noise is multiplied by 17 in the output, as compared to 41 of the other. This result is misleading because the assumption of opamp noise as being white is not valid in the case of chopper-based filter; In this filter, the signal-processing is done at baseband, so the dc-offset and  $1/f$  noise of the opamp corrupt the useful signal. So Eqn. 5.45 fails to capture this corruption of the signal by the colored opamp noises and thus underestimates the total noise power in the signal band.

### 5.4.3 Parasitic Capacitances

Chopper-based filter in the presence of both opamp noise and parasitic capacitances (switch, capacitor plates and opamp) is shown in Fig. 5.14.

Performing analysis on this circuit gives the time-domain difference equation:

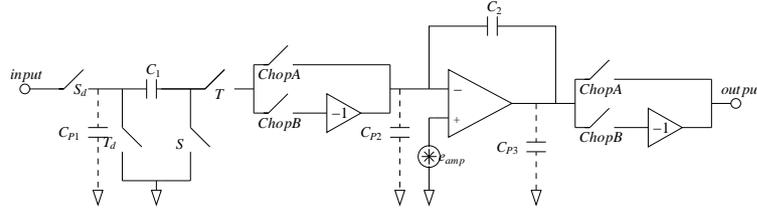


Figure 5.14: Single-ended chopper-based HP filter with parasitic capacitances

$$v_o[n] + v_o[n-1] = \frac{C_1}{C_2} v_{in}[n-1] + \left( \frac{C_1}{C_2} \right) e_{amp}\left[n - \frac{1}{2}\right] + \left( 1 + \frac{C_{P2}}{C_2} \right) e_{amp}[n] - \left( 1 + \frac{C_{P2}}{C_2} \right) e_{amp}[n-1] \quad (5.46)$$

This equation manifests the deterioratory effect of parasitic capacitance  $C_{P2}$  on the performance of the filter. It amplifies the opamp noise near the signal band i-e around  $F_s/2$ . Using  $C_{P2} = 0.1 \times C_2$  in this equation and putting it in the proposed HP modulator, as in the precedent section, gives the approximate power of the amplifier noise present in the signal band as:

$$\overline{e_{amp, inband}^2} \approx 20 \times \frac{\overline{e_{amp1}^2}}{F_s} \times B \quad (5.47)$$

This equation shows that with the inclusion of 10% parasitic capacitance, noise power in the signal band is increased by 17%, in contrast to 8% in the case of integrator-based HP filter.

#### 5.4.4 Op-Amp Non-Idealities

The consequences of opamp non-idealities on chopper-based structure are different than those of integrator-based structure. The fact that there is no feedback capacitor helps reduce the requirements on opamp performances, since it is less heavily loaded. In the next sections, finite dc-gain, GBW and slew rate of the opamp constituting chopper-based structure is discussed.

##### 5.4.4.1 Finite DC-Gain

The chopper-based structure built with a finite dc-gain opamp is shown in Fig. 5.15.

Where  $C_p$  represents the input parasitic capacitance of the op-amp, parasitic capacitance of the switches connected to the negative input of the op-amp and parasitic capacitance associated with the plates of capacitors connected to the negative input of the op-amp. Solving charge-transfer equations for this filter, keeping in view the charge-conservation law, the practical transfer function in terms of capacitances and op-amp dc-gain  $A_0$  is given by:

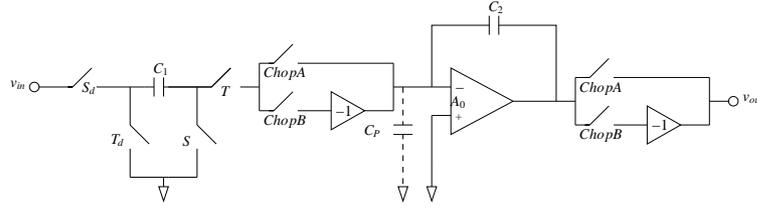


Figure 5.15: Chopper-based HP filter with finite opamp dc-gain

$$H_{practical}(z) = \frac{C_1}{C_2} \frac{\frac{A_0}{\frac{C_1}{C_2} + \frac{C_p}{C_2} + A_0 + 1} z^{-1}}{1 + \frac{\frac{C_p}{C_2} + A_0 + 1}{\frac{C_1}{C_2} + \frac{C_p}{C_2} + A_0 + 1} z^{-1}} \quad (5.48)$$

where  $\frac{C_1}{C_2} = b$  is the gain of the filter and  $\frac{C_p}{C_2} = p$  is the gain of the parasitic voltage stored on parasitic capacitance. Replacing these values in Eqn. 5.48:

$$H_{practical}(z) = b \frac{\frac{A_0}{b+p+A_0+1} z^{-1}}{1 + \frac{p+A_0+1}{b+p+A_0+1} z^{-1}} \quad (5.49)$$

The value of  $b$  for the first HP filter in the proposed modulator architecture is 0.5, assuming a reasonable value of 0.01 i-e  $C_p = 1\% \times C_2$  for  $p$ , the exact transfer function of this filter turns out to be:

$$H_{practical}(z) = 0.5 \frac{\frac{A_0}{A_0+1.51} z^{-1}}{1 + \frac{A_0+1.01}{A_0+1.51} z^{-1}} \quad (5.50)$$

Therefore the values of  $\alpha$  and  $\beta$  are given by:

$$\alpha = \frac{A_0}{A_0 + 1.51}, \quad \beta = \frac{A_0 + 1.01}{A_0 + 1.51} \quad (5.51)$$

Using Eqn. 5.50 as the transfer function for the first HP filter of the proposed modulator, it is simulated at a range of values of  $A_0$  to analyse the effect of this non-ideality. The input signal is a sinusoid at an amplitude of 0.4 normalized with respect to quantization step i-e -8dBFS at frequency of  $0.4993F_s$ . The simulation result is shown in Fig. 5.16:

This figure shows that the chopper-based structure planted in the proposed modulator architecture requires the minimum op-amp dc gain of 30dB (in contrast to 45dB for integrator-based structure) to acquire the ideal signal to quantization noise ratio (SQNR) for the fixed input amplitude.

#### 5.4.4.2 Finite Gain-Bandwidth Product and Slew Rate

The influence of finite GBW of the opamp constituting the chopper-based structure can be represented by:

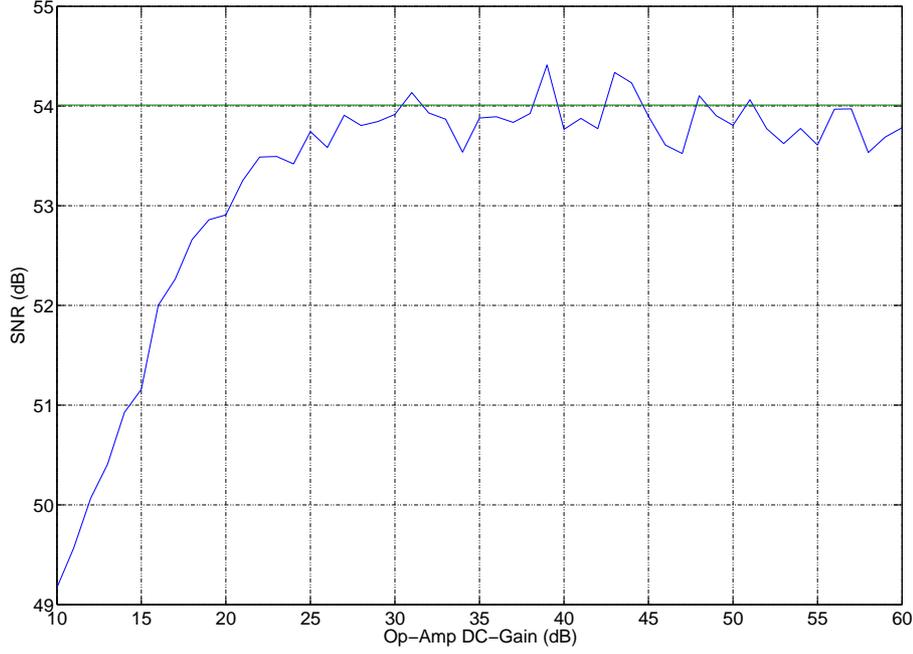


Figure 5.16: SNR vs. Op-Amp DC-Gain

$$v_{out}(t) = -\beta v_{out}(nT_s - T_s) + (b\alpha v_{in}) \times \left(1 - e^{-\frac{t}{\tau}}\right), \quad 0 < t < \frac{T_s}{2} \quad (5.52)$$

where  $v_{out}$  is the output of the filter,  $T_s = 1/F_s$  is the sampling period,  $v_{in}$  is the input of the filter and  $\tau = (1 + b)/2\pi GBW$  is the time constant of the op-amp comprising the filter as calculated in Annex. C. Note that in this equation, there is a single term for discharging transient i.e  $b\alpha v_{in}$  in contrast to two terms for integrator-based structure, as there is only one capacitor  $C_1$  which discharges into the output capacitor  $C_2$ . If this HP filter represents the first HP filter of the proposed second-order modulator,  $v_{in}$  is given by:

$$v_{in} = x(nT_s - T_s/2) - y(nT_s - T_s) \quad (5.53)$$

where  $x$  is the input of the modulator and  $y$  is the output of the modulator.

With the slew rate limitation of the op-amp, the output transient of this HP filter turns out to be:

$$v_{out}(t) = -\beta v_{out}(nT_s - T_s) + V_s - \text{sgn}(V_s)SR_s\tau e^{-\left(\frac{T_s}{2\tau} - \frac{|V_s|}{SR_s\tau} + 1\right)} \quad (5.54)$$

where  $V_s$  is given by:

$$V_s = b\alpha v_{in} \quad (5.55)$$

Simulation is performed by fixing opamp DC-gain, GBW and varying the values of  $SR_s$  and observing the output SNDR using the chopper-based structure. The result is illustrated in Fig. 5.17:

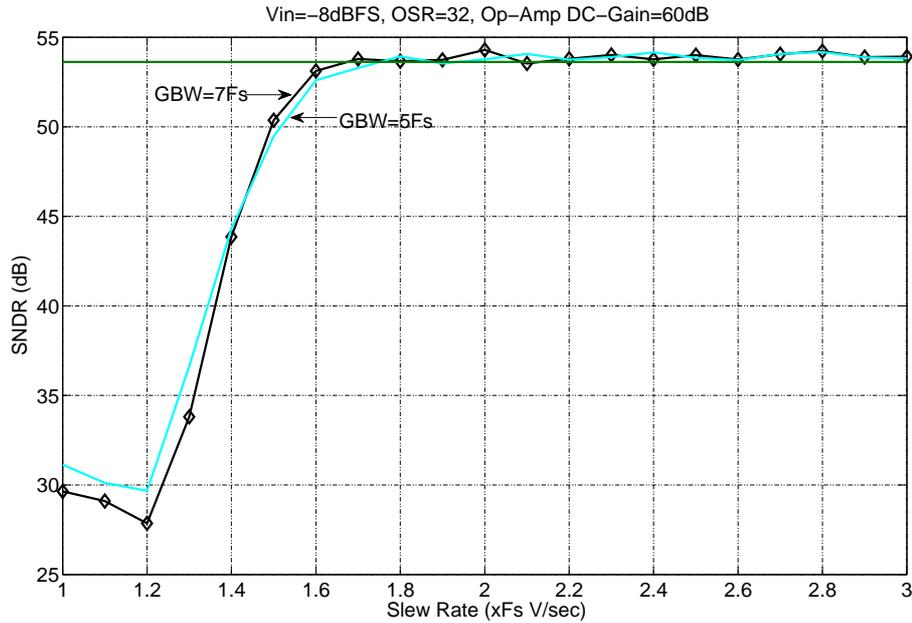


Figure 5.17: SNDR degradation of the proposed modulator implemented using chopper-based filter as a function of op-amp SR

The result shows that the minimum  $SR_s$  of  $1.8 \times F_s (V/sec)$  is needed for the proposed modulator architecture with chopper-based filter to establish the required performance, contrary to  $4.2 \times F_s (V/sec)$  for the integrator-based one.

## 5.5 Improved Structure

An improved implementation of HP filter is reported in [29] and is shown in Fig. 5.18. This implementation does not suffer from the disadvantages of the previous two implementations. The basic operation is such that the charge is sampled onto  $C_{1A}$ , during  $S$ . On  $T$  this charge is then transferred to  $C_{2A}$  on odd clock cycles and to  $C_{2B}$  on even clock cycles.  $C_{1B}$  functions in a similar manner.

This implementation is better than integrator-based filter because there is no extra feedback loop around integrator. This has various advantageous implications: it takes significantly less area, it reduces the capacitive loading on the opamp and consequently the power consumption, it improves the noise performance of the filter as derived analytically in the later sections and it improves the stability as it is no longer dependant on accurate capacitor matching. This structure also resolves the problem of low-frequency noises associated with chopper-based structure; all the signal processing is completed at IF frequency, thus dc offset or  $1/f$  noise no longer pollute the useful signal.

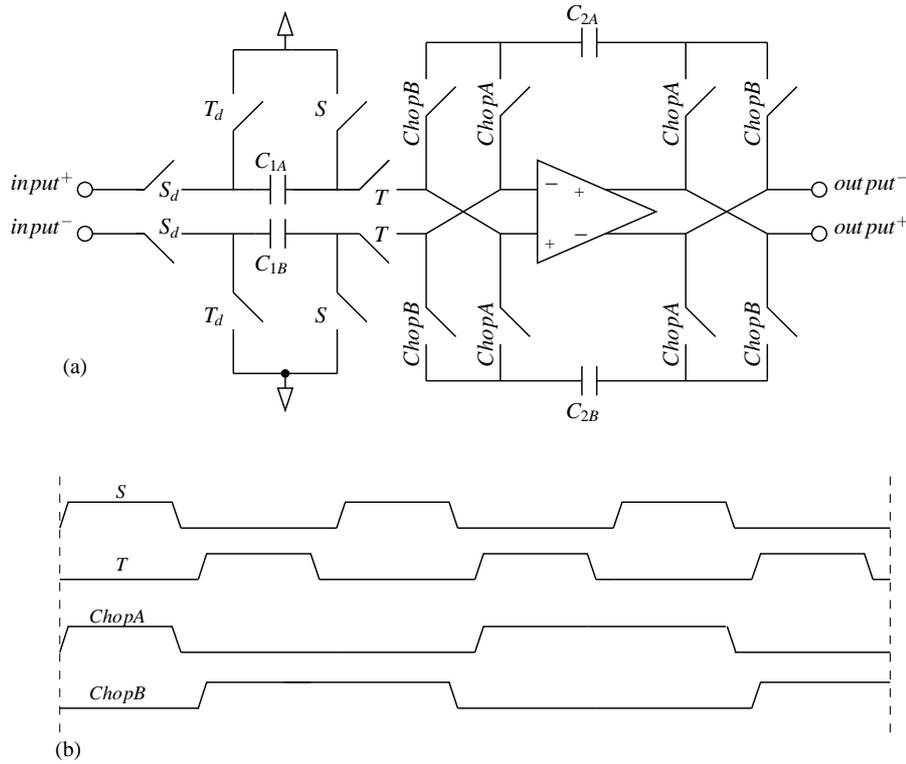


Figure 5.18: (a) Improved HP filter, (b) Its associated timing diagram

### 5.5.1 Switch Noise

The switch noise, in this HP filter shown in Fig. 5.18, is sampled onto capacitors  $C_{1A}$  and  $C_{1B}$  during sampling phase  $S$ . During the charge-transfer phase  $T$ , additional noise is sampled when the charge from these capacitors is transferred to the capacitors,  $C_{2A}$  and  $C_{2B}$ . This gives the total power of the switch noise referred to the filter input as:

$$\overline{e_{switch}^2} = kT \left( \frac{2}{C_{1A}} + \frac{2}{C_{1B}} \right) \quad (5.56)$$

where the factor of 2 accounts for the noise sampling in both sampling and charge-transfer phases. With the sampling capacitances of  $C_{1A} = C_{1B} = C_S$ , the total input referred switch noise power is:

$$\overline{e_{switch,filter2}^2} = \frac{4kT}{C_S} \quad (5.57)$$

Thus, comparing Eqns. 5.6, 5.32 and 5.57, it can be shown that improved-structure and chopper-based structure have the same input referred switch noise, while both of them provide 20% improvement in switch-noise over integrator-based structure.

### 5.5.2 Op-Amp Noise

Like the previous two structures, the single-ended version of the improved structure is used to study the influence of opamp noise on its performance. Its single-ended version with opamp noise is shown in Fig. 5.12:

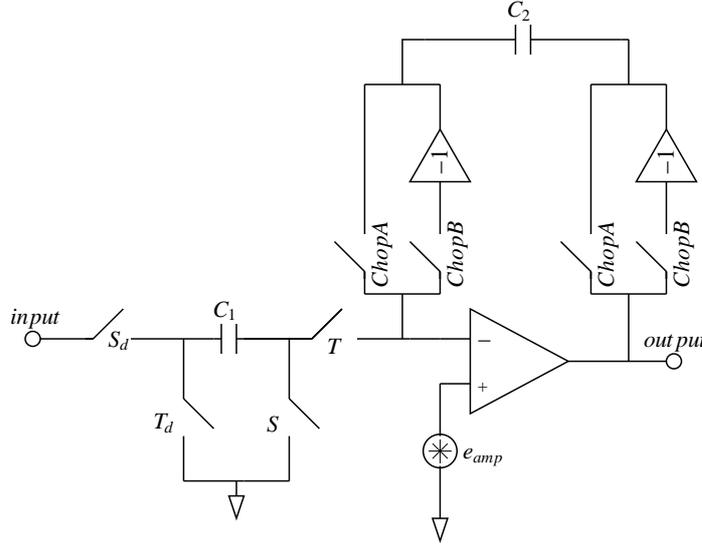


Figure 5.19: Single-ended improved HP filter with opamp noise

This figure shows that in this structure, unlike the chopper-based one, the signal is not chopped before being processed by the opamp, therefore the op-amp sees the signal placed near  $F_s/2$  and hence it is not corrupted by the dc offset and  $1/f$  noise of the opamp. For this reason, in the input-referred opamp noise  $e_{amp}$ ,  $1/f$  can be neglected and then it can be reasonably assumed that sampling the amplifier noise,  $e_{amp}$  distributes it uniformly across the filter sampling bandwidth,  $-F_s/2$  to  $F_s/2$ . Time-domain difference equation of the circuit shown in Fig. 5.19 is given by:

$$v_o[n] + v_o[n - 1] = \frac{C_1}{C_2} v_{in}[n - 1] + \left( \frac{C_1}{C_2} \right) e_{amp}[n - \frac{1}{2}] + e_{amp}[n] + e_{amp}[n - 1] \quad (5.58)$$

This result illustrates that the noise term  $e_{amp}[n - 1/2]$  experiences the same amplification as the input signal, in contrast to the integrator-based structure, where it undergoes increased amplification compared to the input signal as shown in Eqn. 5.7. On the other hand, unlike both integrator-based and chopper-based structures, no first-order differencing of the opamp noise is referred to the input; instead opamp noise is filtered by  $1 + z^{-1}$  function, which has a lowpass characteristic, thus diminishing the noise around the passband at  $F_s/2$ . To gain more insight into the noise performance of this filter, it is incorporated in the proposed second-order HP filter with its associated noise sources, as shown in Fig. 5.20.

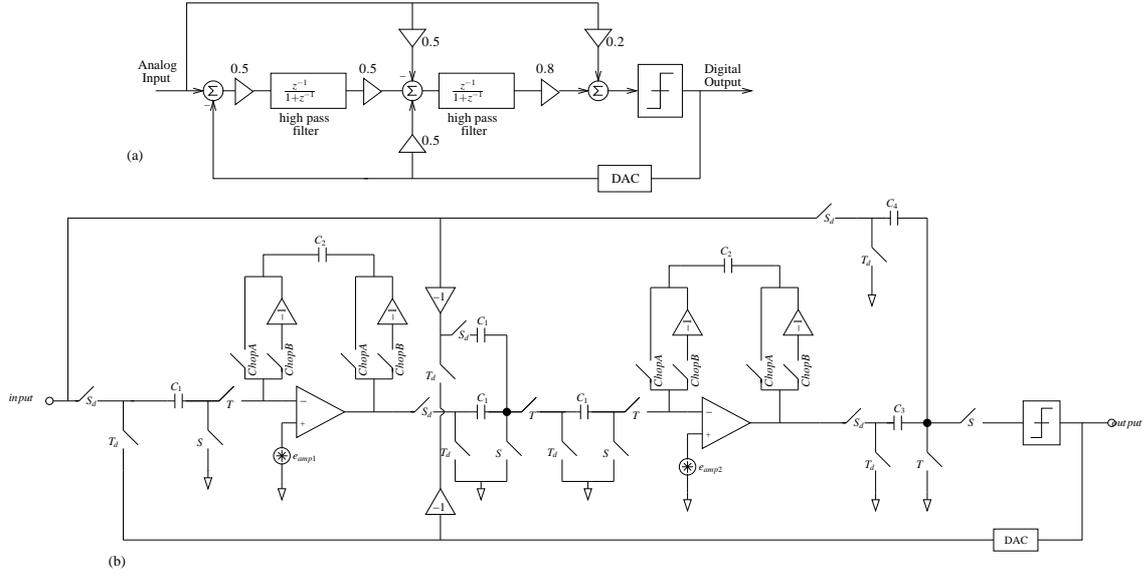


Figure 5.20: (a)Block diagram, (b)single-ended SC realization of the proposed HP modulator using improved filter with associated opamp noise sources

Performing the necessary analysis, the output of this HP modulator in the z-domain turns out to be:

$$Y(z) = \frac{0.2G \cdot X(z) + (1 + z^{-1})^2 E(z)}{1 + (2 - 0.4G) \cdot z^{-1} + (1 - 0.2G) \cdot z^{-2}} + NTF_{amp1}(z) \cdot e_{amp1}(z) + NTF_{amp2}(z) \cdot e_{amp2}(z) \quad (5.59)$$

where the noise transfer functions for  $e_{amp1}$  and  $e_{amp2}$  are respectively,

$$NTF_{amp1}(z) = \frac{0.4G \cdot z^{-1} \cdot (1 + 0.5z^{-1/2} + z^{-1})}{1 + (2 - 0.4G)z^{-1} + (1 - 0.2G)z^{-2}} \quad (5.60)$$

and

$$NTF_{amp2}(z) = \frac{0.8G \cdot (1 + z^{-1}) \cdot (1 + z^{-1/2} + z^{-1})}{1 + (2 - 0.4G)z^{-1} + (1 - 0.2G)z^{-2}} \quad (5.61)$$

Simplifying Eqns. 5.59, 5.60, and 5.61 by setting the gain of the quantizer,  $G$ , to 5 yields:

$$NTF_{amp1}(z) = 2 \cdot z^{-1} \cdot (1 + 0.5z^{-1/2} + z^{-1}) \quad (5.62)$$

and

$$NTF_{amp2}(z) = 4 \cdot (1 + z^{-1}) \cdot (1 + z^{-1/2} + z^{-1}) \quad (5.63)$$

which, in the frequency domain, can be written as:

$$NTF_{amp1}(f) = 2 \cdot e^{-j2\pi f T_s} \left( 1 + 0.5e^{-j2\pi f T_s/2} + e^{-j2\pi f T_s} \right) \quad (5.64)$$

and

$$NTF_{amp2}(f) = 4 \cdot \left( 1 + e^{-j2\pi f T_s} \right) \cdot \left( 1 + e^{-j2\pi f T_s/2} + e^{-j2\pi f T_s} \right) \quad (5.65)$$

where  $T_s$  is the sampling period. If  $\overline{e_{amp1}^2}$  is the input-referred noise power of the first amplifier, then the spectral density of the shaped noise from  $e_{amp1}$  is:

$$S_{amp1,out}(f) = |NTF_{amp1}(f)|^2 \times \frac{\overline{e_{amp1}^2}}{F_s}, \quad -\frac{F_s}{2} < f < \frac{F_s}{2} \quad (5.66)$$

Similarly, the spectral density of the shaped noise from  $e_{amp2}$  is:

$$S_{amp2,out}(f) = |NTF_{amp2}(f)|^2 \times \frac{\overline{e_{amp2}^2}}{F_s}, \quad -\frac{F_s}{2} < f < \frac{F_s}{2} \quad (5.67)$$

given that  $\overline{e_{amp2}^2}$  is the input-referred noise power of the second amplifier. Next, it is noted that the signal passband is centered at  $\pm F_s/2$ , and the passband bandwidth is assumed to be much less than  $F_s$ . Therefore, in the passband, the spectral density of the shaped noise from  $e_{amp1}$  and  $e_{amp2}$  can be approximated as:

$$\begin{aligned} S_{amp1,inband}(f) &\approx S_{amp1,out}(f)|_{f=F_s/2} \\ &= |NTF_{amp1}(f)|_{f=F_s/2}^2 \times \frac{\overline{e_{amp1}^2}}{F_s} \\ &= 1 \times \frac{\overline{e_{amp1}^2}}{F_s} \end{aligned} \quad (5.68)$$

and,

$$\begin{aligned} S_{amp2,inband}(f) &\approx S_{amp2,out}(f)|_{f=F_s/2} \\ &= |NTF_{amp2}(f)|_{f=F_s/2}^2 \times \frac{\overline{e_{amp2}^2}}{F_s} \\ &= 0 \times \frac{\overline{e_{amp2}^2}}{F_s} = 0 \end{aligned} \quad (5.69)$$

With Eqn. 5.68, it can be deduced that near the useful signal, noise power from the first opamp is not amplified at the output of the modulator, in contrast to the previous two implementations. While, like the previous implementations, the noise power of the second opamp is attenuated at the output because its shaping function  $NTF_{amp2}(f)$  has a zero at  $F_s/2$ . Using Eqns. 5.68 and 5.69, the power of the amplifier noise present in the signal band can be approximated by:

$$\begin{aligned} \overline{e_{amp,inband}^2} &\approx [S_{amp1,inband}(f) + S_{amp2,inband}(f)] \times B \\ &= 1 \times \frac{\overline{e_{amp1}^2}}{F_s} \times B \end{aligned} \quad (5.70)$$

where  $B$  is the width of the passband. Comparing Eqns. 5.19, 5.45 and 5.70, it becomes evident that the improved-filter has much better noise performance than the other two topologies, when used in the proposed HP modulator.

### 5.5.3 Parasitic Capacitances

To assess the deterioratory effect of parasitic capacitances (due to switches, capacitor plates and opamp) on the functioning of improved HP filter, they have been included (in addition to opamp noise) in this filter as illustrated in Fig. 5.21.

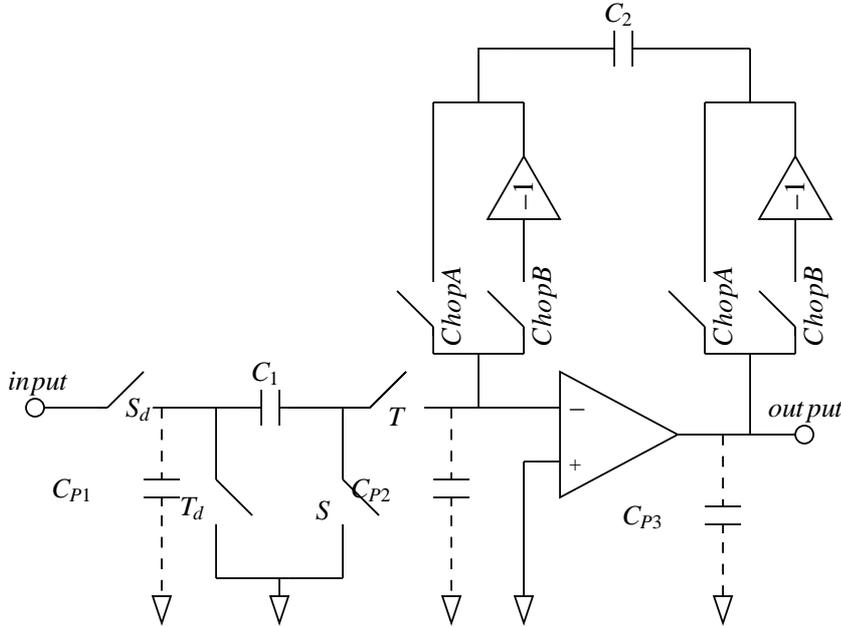


Figure 5.21: Single-ended improved HP filter with parasitic capacitances

Performing analysis on this circuit gives the time-domain difference equation:

$$v_o[n] + v_o[n-1] = \frac{C_1}{C_2} v_{in}[n-1] + \left(\frac{C_1}{C_2}\right) e_{amp}[n - \frac{1}{2}] + \left(1 + \frac{C_{P2}}{C_2}\right) e_{amp}[n] + \left(1 - \frac{C_{P2}}{C_2}\right) e_{amp}[n-1] \quad (5.71)$$

This equation manifests the deterioratory effect of parasitic capacitance  $C_{P2}$  on the performance of the filter. It amplifies the opamp noise near the signal band i-e around  $F_s/2$ . Using  $C_{P2} = 0.1 \times C_2$  in this equation and putting it in the proposed HP modulator,



op-amp. Solving charge-transfer equations for this filter, keeping in view the charge-conservation law, the practical transfer function in terms of capacitances and op-amp dc-gain  $A_0$  is given by:

$$H_{practical}(z) = \frac{C_1}{C_2} \frac{\frac{A_0}{\frac{C_1}{C_2} + \frac{C_p}{C_2} + A_0 + 1} z^{-1}}{1 + \frac{A_0 + 1 - \frac{C_p}{C_2}}{\frac{C_1}{C_2} + \frac{C_p}{C_2} + A_0 + 1} z^{-1}} \quad (5.73)$$

where  $\frac{C_1}{C_2} = b$  is the gain of the filter and  $\frac{C_p}{C_2} = p$  is the gain of the parasitic voltage stored on parasitic capacitance. Replacing these values in Eqn. 5.73:

$$H_{practical}(z) = b \frac{\frac{A_0}{A_0 + 1 + b + p} z^{-1}}{1 + \frac{A_0 + 1 - p}{A_0 + 1 + b + p} z^{-1}} \quad (5.74)$$

The value of  $b$  for the first HP filter in the proposed modulator architecture is 0.5, assuming a reasonable value of 0.01 i-e  $C_p = 1\% \times C_2$  for  $p$ , the exact transfer function of this filter turns out to be:

$$H_{practical}(z) = 0.5 \frac{\frac{A_0}{A_0 + 1.51} z^{-1}}{1 + \frac{A_0 + 0.99}{A_0 + 1.51} z^{-1}} \quad (5.75)$$

Therefore the values of  $\alpha$  and  $\beta$  are given by:

$$\alpha = \frac{A_0}{A_0 + 1.51}, \quad \beta = \frac{A_0 + 0.99}{A_0 + 1.51} \quad (5.76)$$

Using Eqn. 5.75 as the transfer function for the first HP filter of the proposed modulator, it is simulated at a range of values of  $A_0$  to analyse the effect of this non-ideality. The input signal is a sinusoid at an amplitude of 0.4 normalized with respect to quantization step i-e -8dBFS at frequency of  $0.4993F_s$ . The simulation result is shown in Fig. 5.23:

This figure shows that the improved structure used in the proposed modulator architecture requires the minimum op-amp dc gain of 30dB (like the chopper-based structure and in contrast to 45dB for integrator-based structure) to acquire the ideal signal to quantization noise ratio (SQNR) for the fixed input amplitude.

#### 5.5.4.2 Finite Gain-Bandwidth Product and Slew Rate

The influence of finite GBW of the opamp constituting the improved structure can be represented by:

$$v_{out}(t) = -\beta v_{out}(nT_s - T_s) + (b\alpha v_{in}) \times (1 - e^{-\frac{t}{\tau}}), \quad 0 < t < \frac{T_s}{2} \quad (5.77)$$

where  $v_{in}$  is the input and  $v_{out}$  is the output of the filter,  $T_s = 1/F_s$  is the sampling period and  $\tau = (1 + b)/2\pi GBW$  is the time constant of the op-amp comprising the filter. This expression for the time-constant is derived in Annex. D. Note that in this equation, there is a single term for discharging transient i-e  $b\alpha v_{in}$  in contrast to two terms for

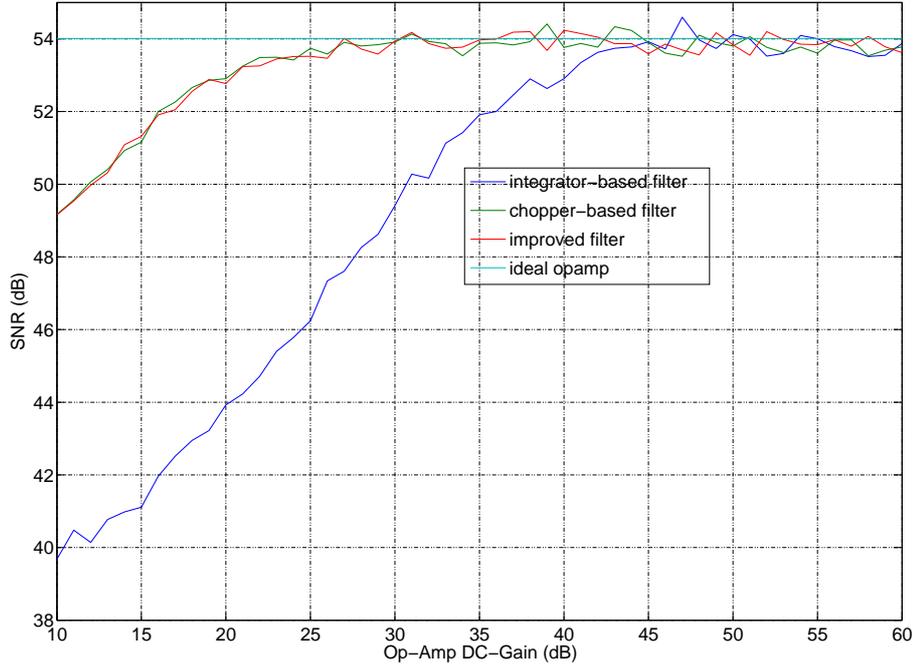


Figure 5.23: SNR vs. Op-Amp DC-Gain

integrator-based structure, as there is only one capacitor  $C_1$  which discharges into the output capacitor  $C_2$ . If this HP filter represents the first HP filter of the proposed second-order modulator,  $v_{in}$  is given by:

$$v_{in} = x(nT_s - T_s/2) - y(nT_s - T_s) \quad (5.78)$$

where  $x$  is the input of the modulator and  $y$  is the output of the modulator.

With the slew rate limitation of the op-amp, the output transient of this HP filter turns out to be:

$$v_{out}(t) = -\beta v_{out}(nT_s - T_s) + V_s - \text{sgn}(V_s)SR_s\tau e^{-(\frac{T_s}{2\tau} - \frac{|V_s|}{SR_s\tau} + 1)} \quad (5.79)$$

where  $V_s$  is given by:

$$V_s = b\alpha v_{in} \quad (5.80)$$

To gauge the impact of finite GBW and SR on the improved filter and to compare it with other two filter implementations, simulations are carried out by varying the values of  $SR_s$  at two different values of GBW and observing the output SNDR. The result is illustrated in Fig. 5.24:

The result shows that the minimum  $SR_s$  of  $1.8 \times F_s(V/sec)$  is needed for the proposed modulator architecture implemented with either the improved filter or the chopper-based filter to establish the required performance at the GBW of  $5F_s$ . On the other hand, the

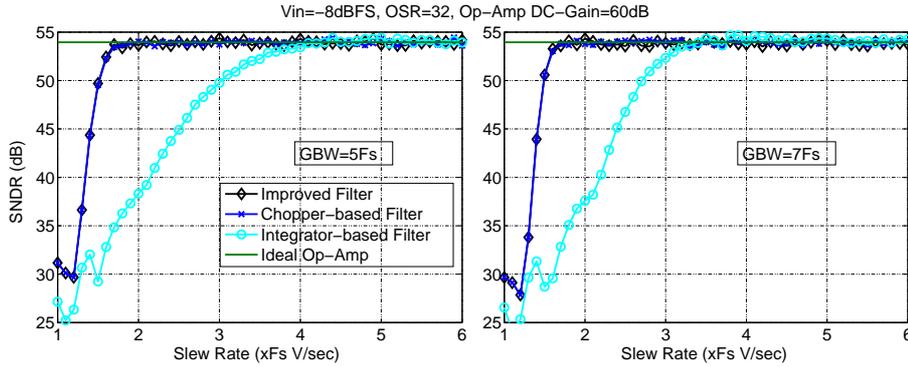


Figure 5.24: SNDR vs. op-amp SR for the proposed modulator architecture

minimum  $SR_s$  of  $4.2 \times F_s$  ( $V/sec$ ) is required at the GBW of  $5F_s$ , if the proposed architecture is built with integrator-based filter.

### 5.5.5 High Frequency Performance Analysis

The basic purpose of this design procedure is to find an architecture of the HP filter, which can convert large bandwidth while consuming the least amount of power. In other words, the filter which uses an opamp with least GBW and SR and operates at maximum sampling frequency. The simulation results in the previous sections reflect that chopper-based and improved structure fall in this category since their GBW and SR is the least multiple of sampling frequency  $F_s$ . In this section, this analysis is carried one step further by carrying it out in realistic simulator SPECTRE by CADENCE. For this purpose, macro-models of the building blocks are used.

The switches used are macro-models having  $R_{on} = 10\Omega$  and  $R_{off} = 10M\Omega$ . The capacitances used are  $C_1 = 1pF$ ,  $C_2 = 2pF$  and  $C_3 = 4pF$ . The op-amps used are single-pole macro-models having  $R_{out} = 10k\Omega$  and  $Gm = 10mS$  thus a dc-open-loop-gain of 40dB. The GBW of op-amp depends on the feedback loop or load across opamp during the charge transfer phase:

$$f_T = \frac{Gm}{2\pi C_L} \quad (5.81)$$

The capacitive load on chopper-based and improved filter is the same and is smaller than integrator-based filter which has an additional load because of feedback loop around the integrator. This loop makes the major part of the load around the op-amp because it is twice the value of integrating capacitor. Thus the op-amp with the same dimensions will give small GBW for integrator-based filter as compared to the other two implementations. In other words, to make the integrator-based filter work at high sampling frequencies, we have to make much aggressive op-amp compared to the other two implementations, resulting in high power consumption.

In this analysis, we measure the SNDR of the modulator by varying the sampling frequency for each type of filter while keeping the op-amp GBW constant.

This result is reflected in the simulation result shown in Fig. 5.25:

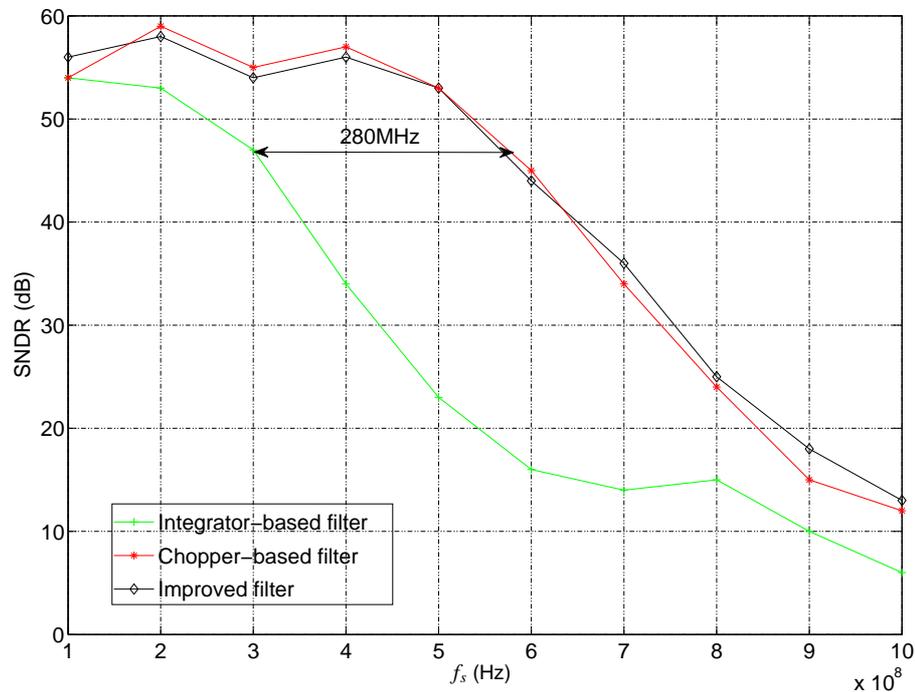


Figure 5.25: Performance of proposed HP modulator using three HP filters at high sampling frequencies

This shows that chopper-based and improved filter can work at sampling frequency which is 280MHz higher than highest possible sampling frequency for integrator-based filter using the same op-amp. In other words, at the same power consumption, modulator built with integrator-based filter can convert less bandwidth than the modulator constructed with the other two filter topologies.

### 5.5.6 Noise Analysis

Another important criteria that is used to compare the filters is op-amp noise rejection. Op-amp noise consists of thermal noise which has white spectrum over the frequency of interest and Flicker Noise, which has a spectrum proportional to  $1/f$ . In any op-amp configuration, at least four devices contribute to the noise: two input transistors and two load transistors. Since the op-amps used in the three filters are the same, we have reasonably assumed that their input referred noise is the same. Performance of the modulator in the presence of op-amp noise has already been analysed theoretically for each filter. In this section, the purpose is to validate the theoretical study by simulating the circuits in SPECTRE. Like in the previous section, macro-models of the building blocks have been used for this purpose.

### 5.5.6.1 Noise Generation

For the purposes of noise analysis, the input referred op-amp noise is generated in MATLAB which is the sum of dc-offset, thermal noise and flicker noise. Thermal noise consists of random values with normal distribution at mean 0 and variance equal to the power required of the noise source. This is easily achieved in MATLAB. The time interval between two samples has been set at  $T_s/10$  which enables to model the noise as a continuous time source [88]. On performing fast fourier transform of this random sequence, it is observed that the power spectral density is not considerably smooth. To counter this problem, averaging of ten sets of data is performed, which gives considerably smooth spectrum [88].

Flicker noise (1/f noise), on the other hand, is generated in MATLAB by passing white noise through a filter with a transfer function [89]:

$$H_f(z) = \frac{1}{(1 - z^{-1})^{\alpha/2}} \quad (5.82)$$

where  $\alpha$  is a real number between 0 and 2. Using the power series expansion, only the denominator of Eqn. 5.82 is expanded and the transfer function of infinite impulse response (IIR) filter and its coefficients are:

$$H_f(z) = \frac{1}{h_0 + h_1 z^{-1} + h_2 z^{-2} + \dots} \quad (5.83)$$

$$h_0 = 1, h_k = (k - 1 - \frac{\alpha}{2}) \frac{h_{k-1}}{k} \quad (5.84)$$

From the above equations, it is clear that for the perfect 1/f noise modeling, the required IIR filter order (i.e. the number of taps) is infinite, which is impractical. Therefore, 1/f noise is generated using 100 coefficients in Eqn. 5.84. To obtain the total noise, dc-offset (i.e constant voltage sequence), thermal noise and flicker noise sequences are added. The power spectral density of this combined noise is shown in Fig. 5.26:

### 5.5.6.2 Noise Injection in Circuit

Input referred noise of the op-amp which has been generated in the MATLAB is injected in the circuit by adding a voltage source at each input of the op-amp. The values of this voltage source are read from MATLAB. The circuit for proposed HP modulator, built with improved filter topology including op-amp noise sources is illustrated in Fig. 5.27.

$e_{amp}^+$  and  $e_{amp}^-$  are the noise sources generated in MATLAB and read directly in SPECTRE. The simulation result of noise-injection in three filters is shown in Fig. 5.28.

This figure shows that the integrator-based and improved filters succeed in avoiding the low frequency-Flicker noise, while in chopper-based filter, the Flicker noise corrupts the signal band and results in reduction of SNR. At OSR of 32, improved, integrator-based and chopper-based filters give an SNDR of 55dB, 52dB and 21dB respectively. Thus, 3dB of SNR is lost due to disadvantageous high-frequency op-amp noise shaping in integrator-based structure and 34dB are wasted due to op-amp noise shaping and low-frequency noise corruption of the useful signal in chopper-based structure.

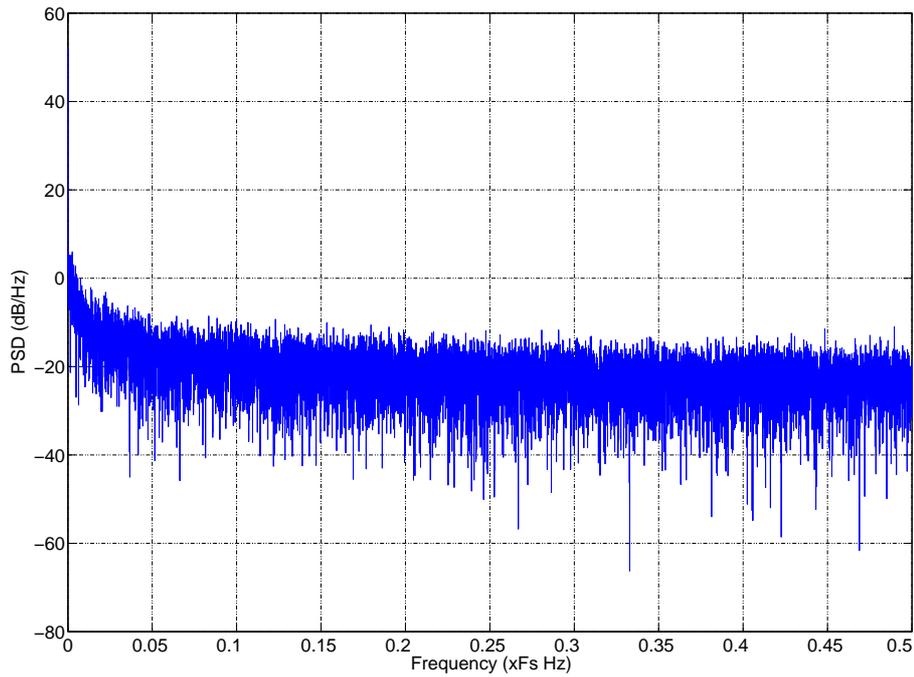


Figure 5.26: Input Referred Op-Amp Noise Spectrum

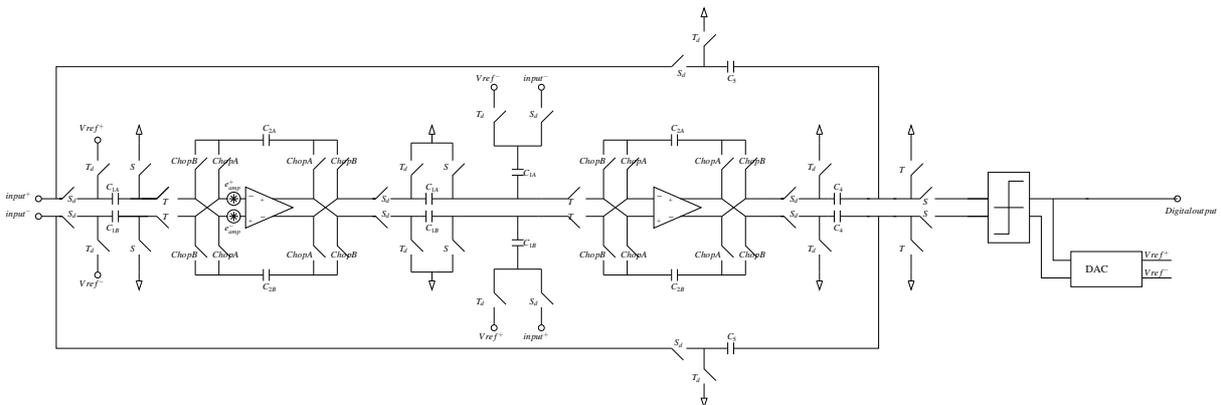


Figure 5.27: Noise injection in the modulator

## 5.6 Comparative Analysis between Low-Pass and High-Pass $\Delta\Sigma$ Modulators

The development of a High-Pass  $\Delta\Sigma$  modulator for a radio receiver necessitates a comparative analysis between High-Pass and the traditional Low-Pass modulator to justify the choice. Besides the important advantage of immunity to low-frequency noises, the improved HP filter, as explained in the chapter, eliminates the traditional shortcomings of HP modulator i.e increased op-amp requirements of dc-gain and slew-rate. In this section,

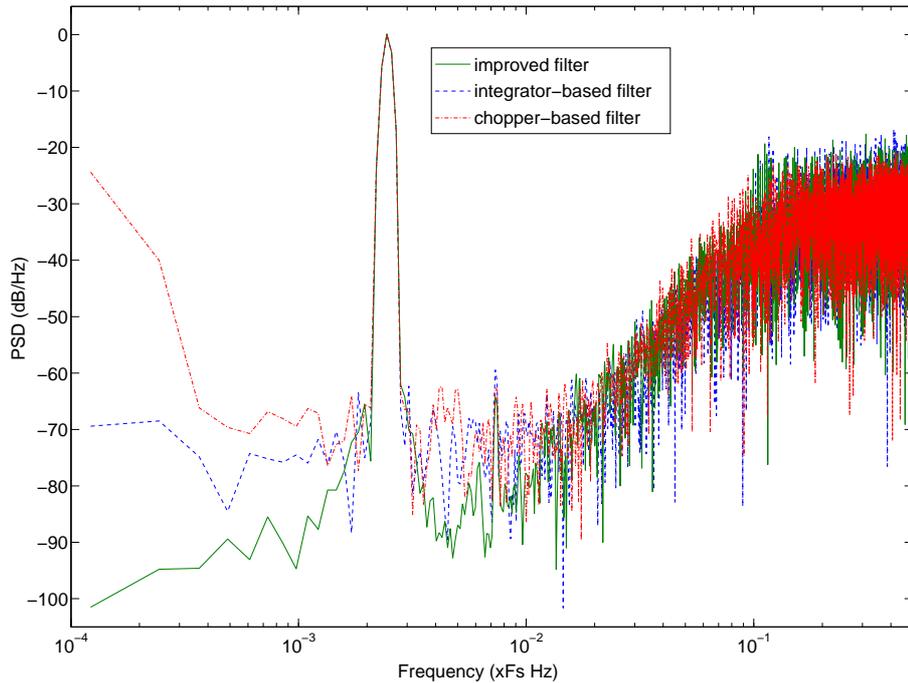


Figure 5.28: Modulator output spectrum in the presence of op-amp noise for three filters

a detailed comparative analysis between different architectures of HP and LP modulators is performed to study the trade-offs in designing a HP modulator.

### 5.6.1 Clipping

Op-amp clipping or saturation is a practical reality which happens due to limited voltage-swing available at the op-amp output. Feedforward structures perform better in comparison to feedback structures in the face of this nonideality because they process lesser amount of signal. The simulation result showing both LP and HP versions of different modulator architectures is presented in Fig. 5.29.

This shows that both LP and HP structures perform equally good with reference to the parameter of op-amp saturation. The feedback structures demonstrate instability at the early stages of input signal level, while the feedforward structures which do not process useful signal in the integrators/mirrored-integrators, remain stable throughout the input signal level even at low op-amp saturation levels.

### 5.6.2 Op-Amp DC-Gain

The DC-Gain of the op-amps employed in building the integrators/mirrored-integrators is an expensive parameter which needs to be reduced as much as possible to relax the requirements on the op-amp design and to increase the speed of the op-amp at a reasonable power consumption. Finite DC-Gain of the op-amps introduces static errors in the charge-

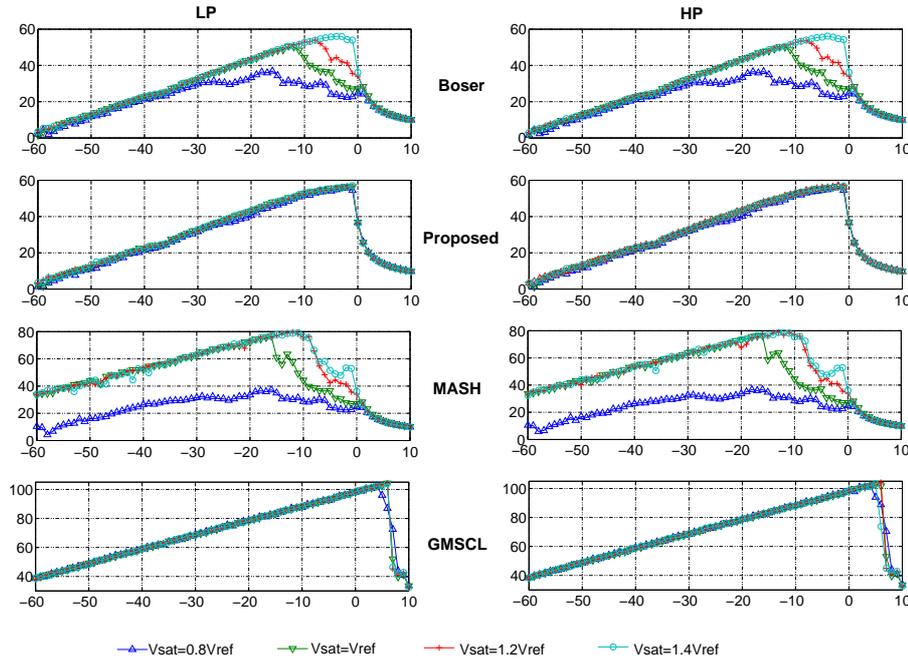


Figure 5.29: Effect of op-amp clipping on various architectures of LP and HP Modulators

transfer transient. To keep these errors below an acceptable level, a lower-level of the DC-Gain has to be determined. The minimum levels of op-amp DC-Gains have been determined through a system-level simulation and presented in Fig. 5.30

This result shows that there is no remarkable difference between the LP and HP modulators for requirement of op-amp DC-Gain in all the modulator architectures simulated.

### 5.6.3 Op-Amp GBW and SR

Op-amp gain-bandwidth product (GBW) and slew-rate (SR) are related parameters which come at the expense of power consumption. Finite GBW and SR introduce dynamic charge transfer errors which need to be kept below a maximum level to guarantee a minimum signal-to-noise ratio. A simulation has been performed to compare the requirements of GBW and SR for LP and HP (using improved HP filter) modulators. Its result is illustrated in Fig. 5.31.

It shows that the requirements of GBW and SR are the same for both LP and HP versions of all architectures. The GMSCL structure turns out to be the best choice in terms of SR required. For an op-amp GBW of  $5 \times F_s$ , the minimum SR required is just  $0.7 \times F_s$  in contrast to the MASH structure which requires  $1.5 \times F_s$ .

### 5.6.4 Clock Jitter

Clock jitter is the random fluctuation in the clock's rising and falling edges instants. Clock jitter at the point of input signal sampling injects white noise in the output signal spectrum

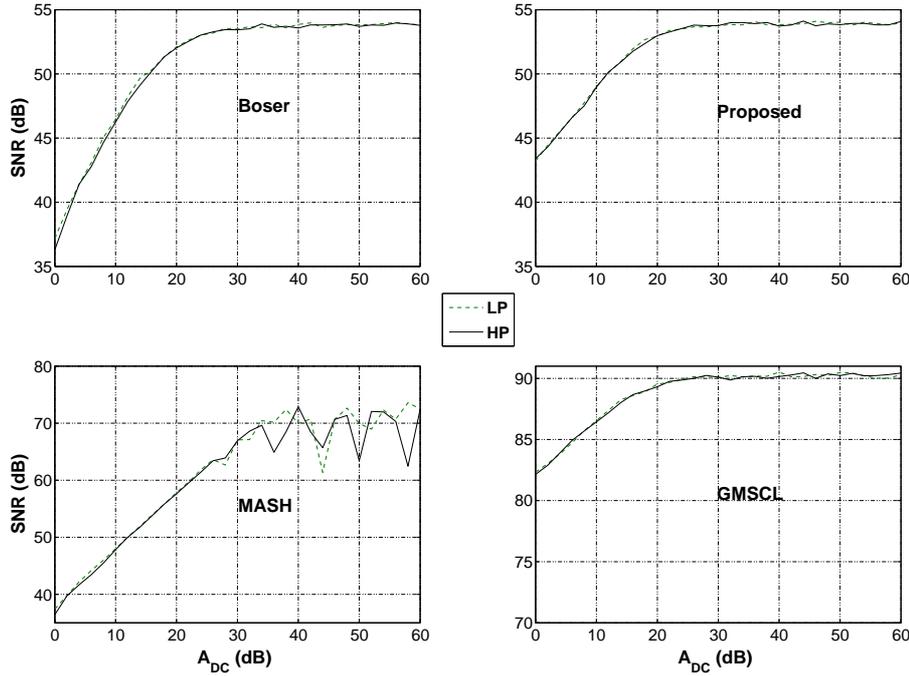


Figure 5.30: Relative performance degradation of LP and HP architecture due to finite dc-gain of op-amp

which is proportional to the frequency of the signal being sampled. Thus, naturally HP modulator is more prone to this type of non-ideality as the signal is at IF in contrast to baseband in LP modulators. The impact of clock-jitter on different modulators is shown in Fig. 5.32

This figure proves that clock-jitter is detrimental for HP modulators while its impact on LP modulators is negligible. For HP modulators, jitter is more harmful for higher-order cascade structures as the slope of the fall is steeper than single-loop second-order structures.

### 5.6.5 Comparator Hysteresis

Comparator hysteresis is another important non-ideality that needs to be studied and its impact analysed. It can be defined as the comparator's inability to change its state when its input signal is below a minimum signal. It is due to the fact that the comparator has a memory of the previous state, so an overdrive is necessary to make it commute to the correct state. The deterioration of the performance of various modulator schemes (both LP and HP versions) due to hysteresis is shown in Fig. 5.33.

It can be inferred that HP versions of all the modulators are highly resistant to hysteresis. But the LP versions of all the modulators are affected by hysteresis. The feedback structures are less influenced by hysteresis than feedforward architectures as the signal passes through the integrators/mirrored-integrators before attacking the comparator.

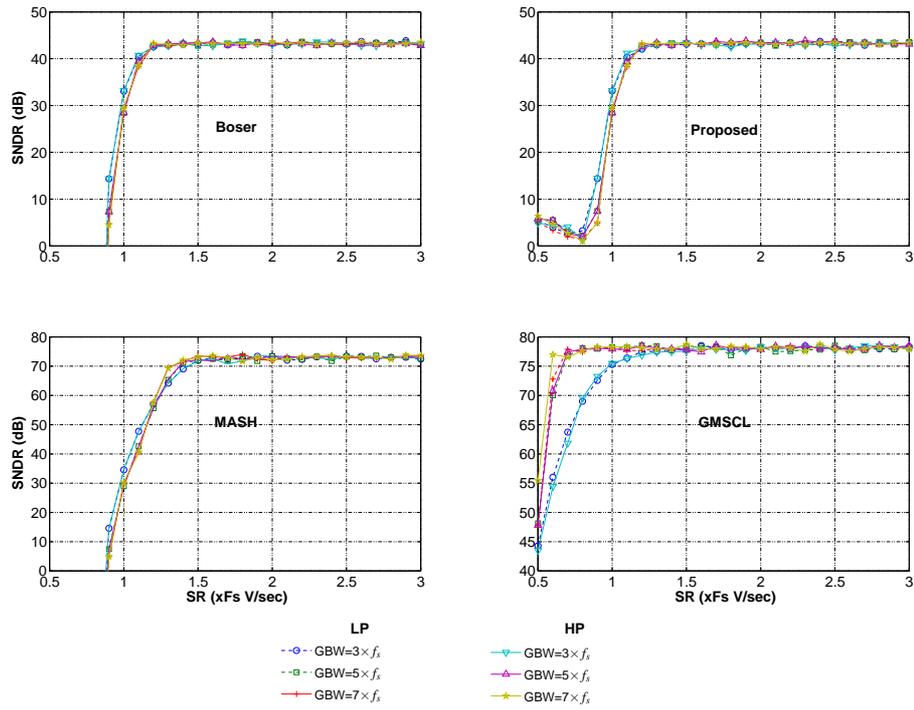


Figure 5.31: Impact of finite op-amp GBW and SR

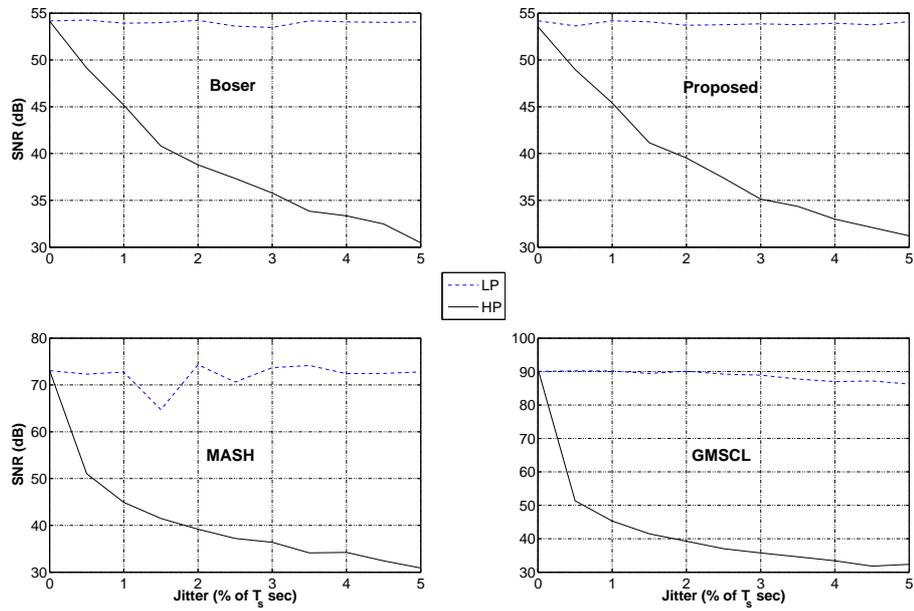


Figure 5.32: Clock jitter impact on modulator performance

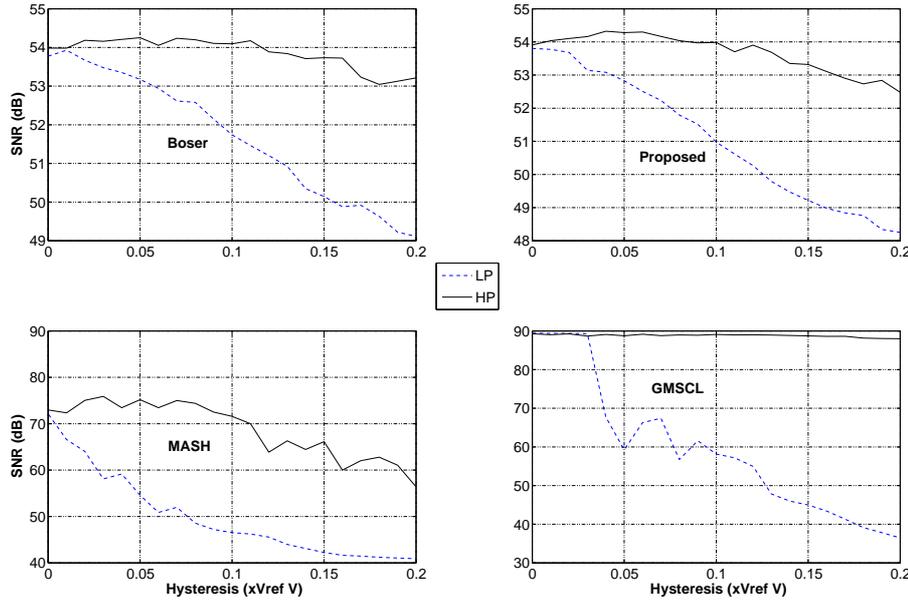


Figure 5.33: Hysteresis

## 5.7 Conclusion

After carrying out different theoretical analyses and experimental tests over the three types of HP Filters, it can be easily concluded that the improved filter is the best of the three structures. It is least effected by the switch noise, opamp noise, parasitic capacitances and consumes the least amount of power. It results in low distortion at high sampling frequencies because of low capacitive load on the op-amp. Thus it can work at high sampling frequencies, which is essential in wide band converters. It keeps low frequency noises away from the signal throughout the signal processing and filters white noise in a low-pass fashion, thus diminishing its power in the signal band near  $F_s/2$ . These characteristics make the improved filter an ideal choice for high-speed and high-resolution at reduced power solution.

With the comparative analysis between LP and HP modulators, it can be concluded that the requirements on the performance of op-amp for both HP and LP modulators are the same provided the improved version of HP filter is used. Clock jitter is detrimental to the performance of HP modulator since the useful signal is in a high frequency region and a slight jitter in the clock introduces enormous errors in the sampled signal. Comparator hysteresis on the other hand hits only the LP versions of the modulators except GMSL which has resistance against the hysteresis till 3% of  $V_{ref}$ . All the architectures of HP modulators are inherently robust in the face of comparator hysteresis.

## Chapter 6

# Design in 65nm CMOS

### 6.1 Introduction

The objective of this chapter is to provide the transistor level design of ADC which is developed on system-level in the earlier chapters. This ADC is designed to satisfy the performance requirements of the standards specified in Table. 6.1:

Looking at the diversity in performance requirements, it becomes evident that the ADC has to be reconfigurable. The reconfigurability is provided by changing sampling frequency ( $f_s$ ) and modulator order ( $M$ ). In the GSM/EDGE mode, since the signal-bandwidth is small, 28.57MHz of  $f_s$  ( $OSR = \frac{28.57MHz}{2 \times 135KHz} \approx 105$ ) and 2nd order noise-shaping with single bit quantizer is operated. Thus the second-stage of high-pass GMSCL structure is turned off in GSM/EDGE mode resulting in power saving. In the UMTS/WLAN mode of operation, the sampling frequency is elevated to 228.57MHz and the modulator order is increased to 4 plus an additional stage of auxiliary quantizer. In this chapter, the op-amp system-level specifications are presented which provide a guide line for designing the transistor-level op-amp. This is followed by the presentation of global single-ended circuit in both GSM/EDGE and UMTS/WLAN modes of operation. Then, the individual building blocks of the global circuit, including OTA, Comparator, DAC etc are exposed. Finally the simulation results are presented followed by the concluding remarks.

Standard	GSM/EDGE	UMTS	WLAN
Conversion Rate	270KHz	3.84MHz	25MHz
Signal Bandwidth	135kHz	1.92MHz	12.5MHz
Sampling Frequency ( $f_s$ )	28.57MHz	228.57MHz	228.57MHz
Modulator Order ( $P$ )	2	4+aux. quantizer	4+aux. quantizer
SNR	80dB	80dB	52dB

Table 6.1: ADC Specification

## 6.2 System level specifications

The system-level specifications for the op-amp are derived in the previous chapter using MATLAB. Based on the recommendations of the previous chapter, improved HP filter has been selected for 65nm CMOS implementations. The specifications of the op-amp (dc-gain, gain-bandwidth product and slew rate) are presented in Fig. 6.1 based on the results of the previous chapter.

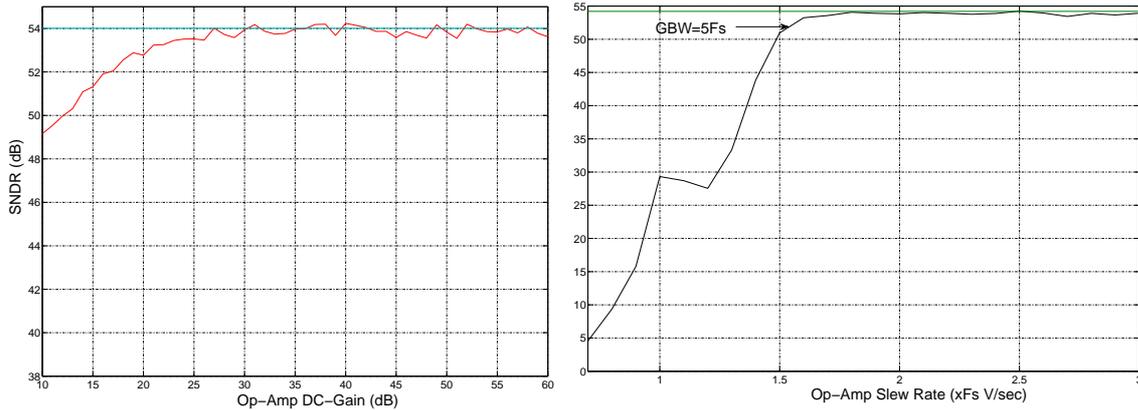


Figure 6.1: DC Gain, GBW and SR specifications of the Op-Amp

As shown in this figure, the proposed modulator built with improved filter attains the desired SNDR performance with an op-amp which has the minimum DC-gain of 30-dB, GBW of  $5 \times f_s$  and SR of  $1.8 \times f_s$ .

## 6.3 Global Circuit Schematic

The schematic of the modulator in the GSM mode is shown in its single-ended version for simplicity in Fig. 6.2. Input switch of the modulator is bootstrapped to fulfill the linearity requirements. The other switches are designed with CMOS transistors. The sampling capacitance at the input of the modulator is chosen equal to 600fF to meet thermal noise specifications.

The modulator used is of 2nd order with the architecture proposed in Chapter:5 and a 1 bit quantizer. This modulator provides the required SNDR performance at an OSR of 84 as presented in the simulation results section. The size of the capacitors decreases with the signal flow because of increased noise shaping along the signal path.

The single-ended modulator schematic in the ULAN mode is shown in Fig. 6.3. It is the proposed-GMSCL structure with improved dynamic range by adding an auxiliary quantizer in the last stage as described in Chapter 4.

The reference voltages used in the circuit are given in Table: 6.8.

The OTA used in the first two high-pass filters has Miller configuration as shown in Fig. 6.4. This OTA was originally designed for the ADC published in [90]. It is a two-stage amplifier, with the first-stage providing the major portion of gain and the second-stage

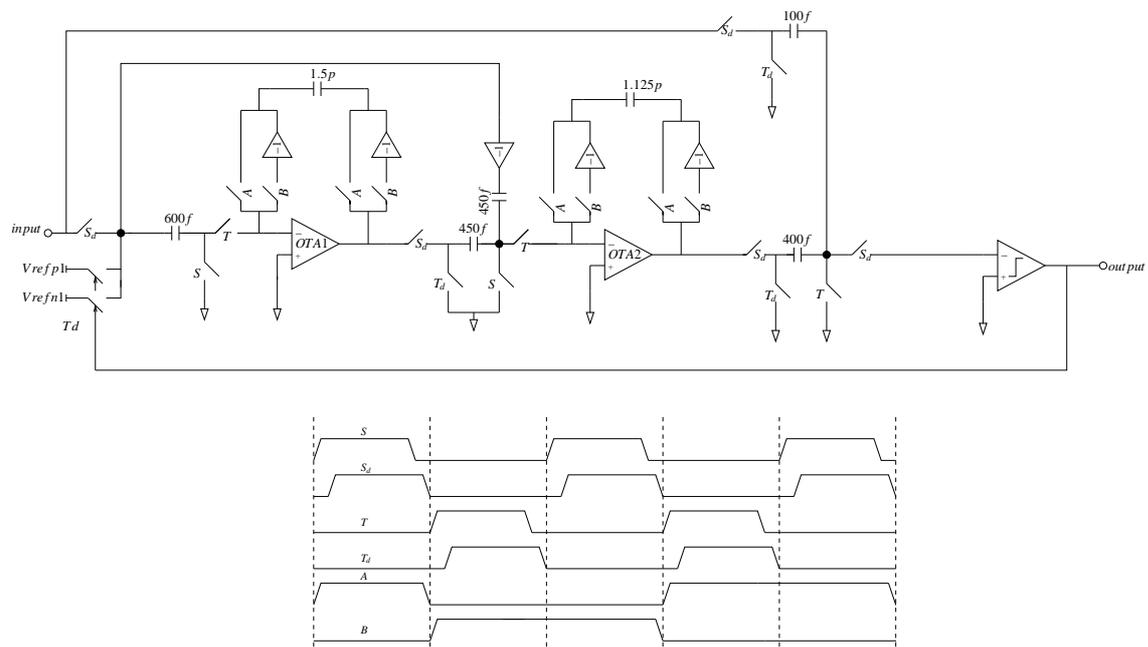


Figure 6.2: Single-ended global modulator in the GSM mode with its associated timing diagram

acting as a buffer and providing voltage-swing. It is not a very power-efficient solution since both the stages need to be biased with currents. The other drawback is that being two-stage amplifier, it needs capacitive compensation. But it provides reasonable performance for Noise, DC-Gain, GBW and voltage-swing.

The OTA1 performance parameters are listed in Table. 6.2.

These parameters are obtained by using the component sizes mentioned in Tables. 6.3 and 6.3. For the input differential pair, NMOS devices have been used. Such a configuration provides a higher gain than the PMOS-input pair because of greater mobility of NMOS devices [48]. The use of minimum-length transistors has been avoided in the input pair and in the current mirrors to limit  $1/f$  noise and mismatching.

The common-mode feedback (CMFB) signal is provided by the switched-capacitor circuit [91] shown in Fig. 6.5 which consumes negligible power.

Since the voltage-swing requirements are less stringent in the 3rd and 4th high-pass filters, gain-boosted Telescopic-Cascode OTA topology is the most-suitable for them. It has the advantages of less power consumption, high speed and high DC-Gain and the disadvantage of low-voltage swing, which is not detrimental for the performance of these filters. This OTA topology is shown in Fig. 6.6.

The performance of this OTA configuration is summarized in Table. 6.5.

Like the previous OTA, the gain-boosted Telescopic OTA was also basically designed for the low-pass  $\Delta\Sigma$  ADC published in [90].

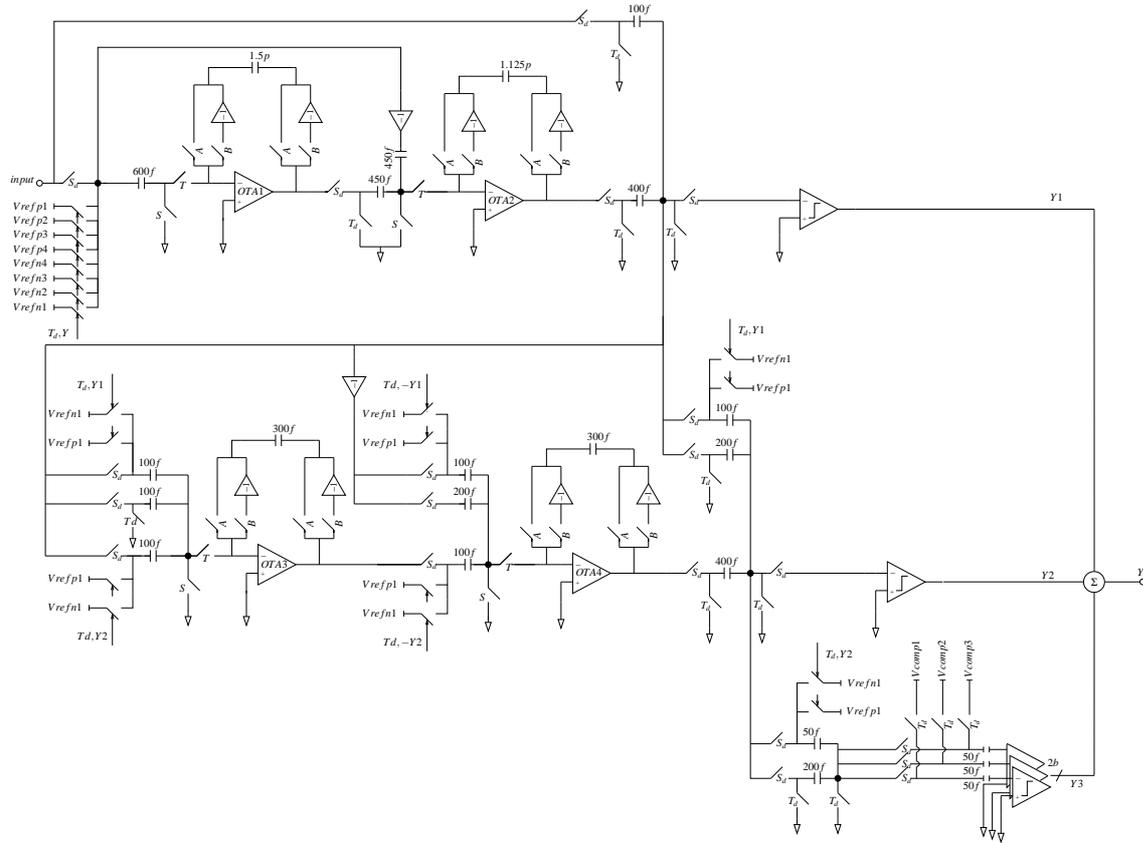


Figure 6.3: Single-ended global modulator in the UMTS/WLAN mode

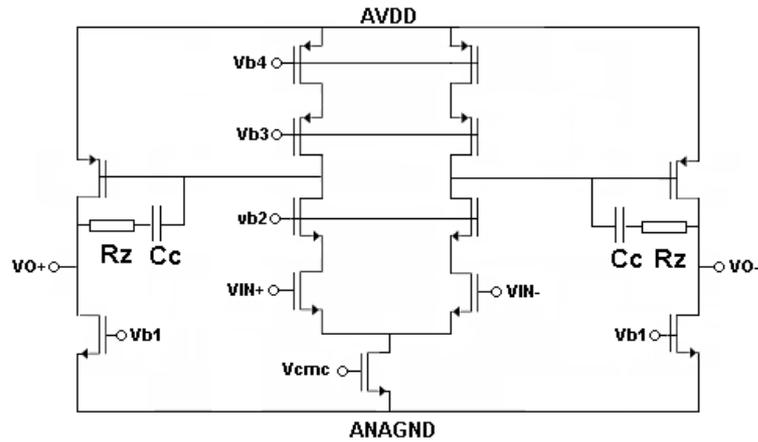


Figure 6.4: OTA1 & OTA2 Configuration

### 6.4 Passive Adder

One of the principal advantages of using the proposed unity-STF structures is that it reduces the constraints on the final adder before the quantizer and which can be implemented

OTA Parameters	Value
Input/Output common mode	600mV
Input Voltage Swing	0.85Vpp
Output Voltage Swing	+/- 350mV
DC Gain	41.3dB
Open Loop GBW	1049MHz
Phase Margin	64.6°
Input Noise	36.7 $\mu$ Vrms
Slew Rate	800V/ $\mu$ Sec
Systematic Input Referred Offset	3mV
Current consumption	8.2mA
Area	180 $\mu$ m $\times$ 100 $\mu$ m
Power Supply	1.2V
Process	CMOS 65nm

Table 6.2: OTA1 Characteristics in integrating phase:  $C_s=0.6$ pF,  $C_{int}=1.25$ pF

Transistors	Size		Unit
	Width	Length	
$M_{1p}, M_{1n}$	48	0.4	$\mu$ m
$M_{2p}, M_{2n}$	20	0.35	$\mu$ m
$M_{3p}, M_{3n}$	144	0.2	$\mu$ m
$M_{4p}, M_{4n}$	300	0.2	$\mu$ m
$M_{casp}, M_{casn}$	20	0.2	$\mu$ m
$M_{bias}$	480	1	$\mu$ m

Table 6.3: Active components sizes in OTA1

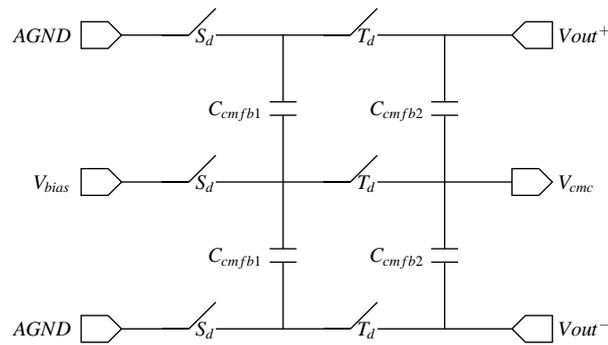


Figure 6.5: CMFB Circuit

passively. The schematic of the passive adder is shown in Fig. 6.7.

The expression for the output voltage  $V_s$  in case of null load capacitor,  $C_L = 0$ , can be

Components	Value	Unit
$R_{zp}, R_{zn}$	250	$\Omega$
$C_{Mp}, C_{Mn}$	320	fF
$C_{cmfb1}$	110	fF
$C_{cmfb2}$	55	fF

Table 6.4: Passive components values' in OTA1

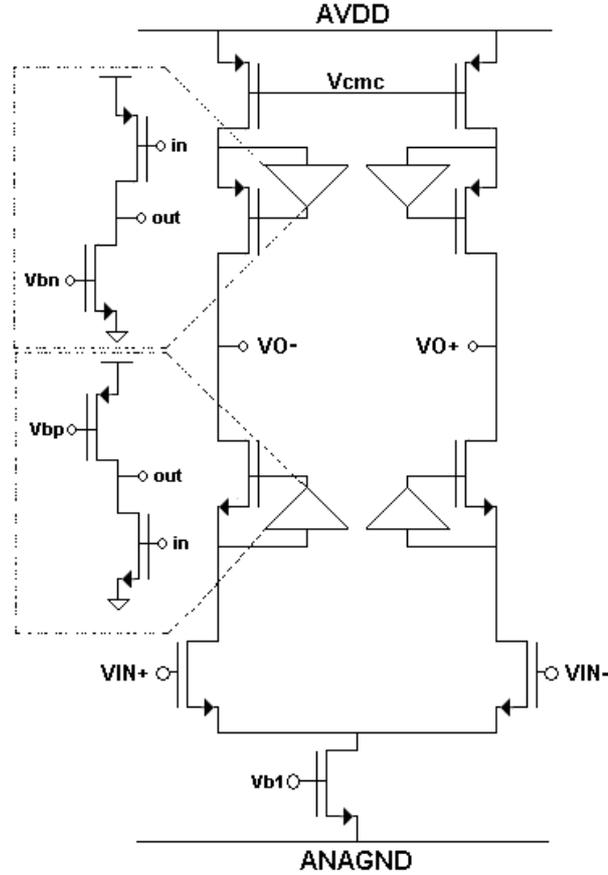


Figure 6.6: OTA3 &amp; OTA4 Configuration

written as:

$$V_s = \frac{\sum_{n=0}^2 C_{an} V_{an}}{\sum_{n=0}^2 C_{an}} = \frac{\sum_{n=0}^2 a_n C_u V_{an}}{\sum_{n=0}^2 a_n C_u} \quad (6.1)$$

where  $V_{an}$  and  $C_{an}$  are the input signal and capacitance of each branch respectively. The capacitance of each branch is proportional to the relative coefficient associated with it i-e  $a_n$ . For the symmetry purposes, unit capacitances  $C_u$  are used to implement  $C_{an}$ .

OTA Parameters	Value
DC Gain	51dB
Open Loop GBW	1.1GHz
Phase Margin	65°
Input Noise	46 $\mu$ Vrms
Current consumption	1.1mA
Power Supply	1.2V
Process	CMOS 65nm

Table 6.5: OTA3 Characteristics

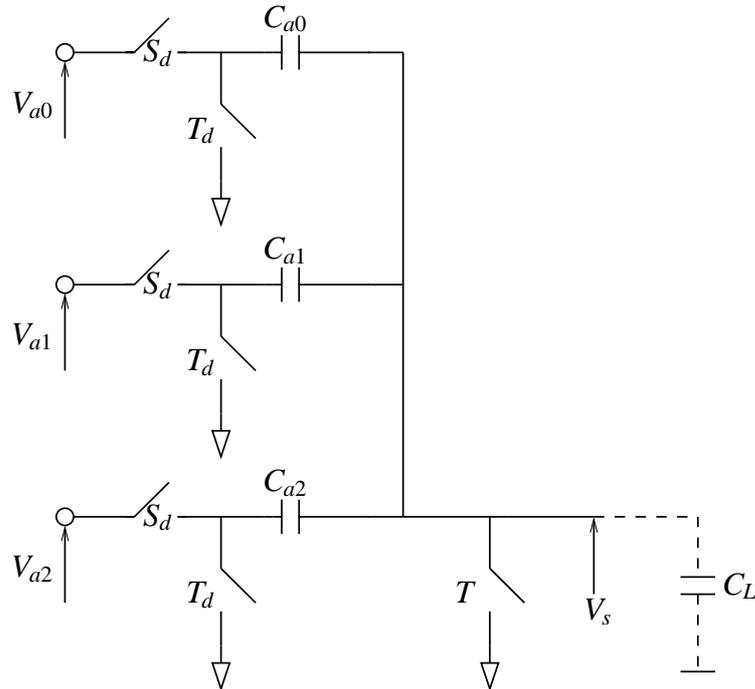


Figure 6.7: Passive Adder

From the Eqn. 6.1, it can be deduced that the sum signal is attenuated by the factor of:

$$Attenuation = \frac{1}{\sum_{n=0}^2 a_n} \quad (6.2)$$

In the presence of a load capacitance  $C_L$  which is charged by the passive adder, the effective attenuation factor becomes:

$$Attenuation_{eff} = \frac{1}{\sum_{n=0}^2 a_n + \frac{C_L}{C_u}} \quad (6.3)$$

The Eqn. 6.3 shows that by choosing a higher unity capacitor, the adder-output-signal

attenuation due to load capacitance is reduced. In the modulator circuit implemented as shown in Fig. 6.3, there is one passive adder in GSM mode and three passive adders in UMTS/ULAN mode. Since the output signal of the passive adders is fed to quantizers, the attenuation factor plays a role in defining the comparison reference voltages of the quantizer. The quantizer reference voltages are divided by the attenuation factors as well. In the light of the attenuation factor associated with its passive adder, the four-level quantizers' comparison reference voltages are given in Table. 6.6.

Voltage Reference	Adder Attenuation	Value
Vcomp1	6	$\frac{VREF}{4 \times 6}$
Vcomp2	6	$\frac{VREF}{2 \times 6}$
Vcomp3	6	$\frac{3 \times VREF}{4 \times 6}$

Table 6.6: Four-Level Quantizer Voltage References

## 6.5 Quantizer

The four-level quantizer is used in the third stage of the modulator to achieve the required resolution. As discussed in Chapter:5, the multi-level quantizer at this stage introduces negligible distortions. The four levels ADC is implemented as a flash quantizer with three comparators in parallel as shown in Fig. 6.8.

The schematic of one individual comparator is shown in Fig. 6.5. A dynamic latch is chosen to save power since it consumes power only when performing latching function i.e during one-half of the clock cycle. A wideband preamplifier improves latch sensitivity and isolates comparator input from kick-back noise. As the comparator should take a decision within the non-overlap period between the clock phases, the latch must be very fast. For a dynamic current of  $140\mu A$  the latch delay is less than 500ps which is the worst case (clock=208MHz).

The values of different performance parameters of the comparator are compiled in Table. 6.5.

## 6.6 DAC

The global digital-to-analog-converter (DAC) is chosen depending on the value of the control bit: ULAN as shown in Fig. 6.10. If the modulator is operating in GSM mode, the DAC operates on the single bit signal generated by the first-stage ADC. This DAC feeds back either one of the reference voltages:  $Vrefp1$ , and  $Vrefn1$ . And, in UMTS/WLAN (ULAN) mode, the global DAC consists of the sum of three local DACs each of which converts the signal of its respective stage ADC.

Global DAC voltage references in both GSM and UMTS/ULAN modes of operation are mentioned in Table. 6.8 as the proportions of maximum DAC voltage-reference called  $Vref$ .

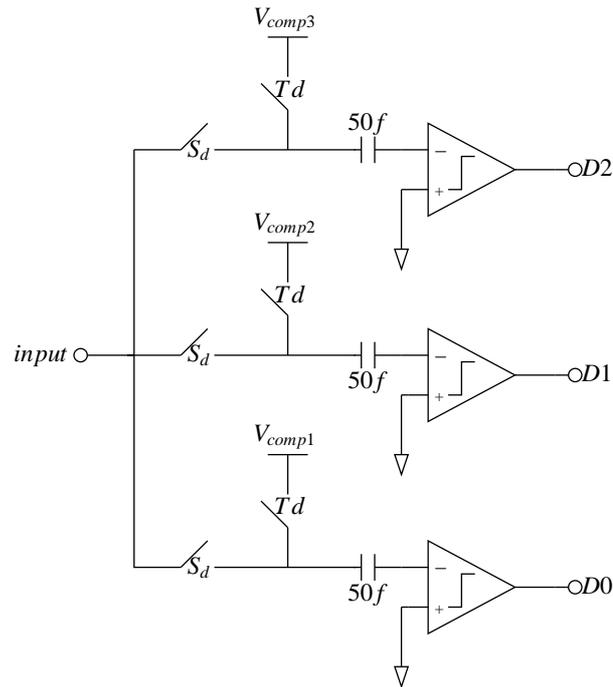


Figure 6.8: Four-level quantizer schematic

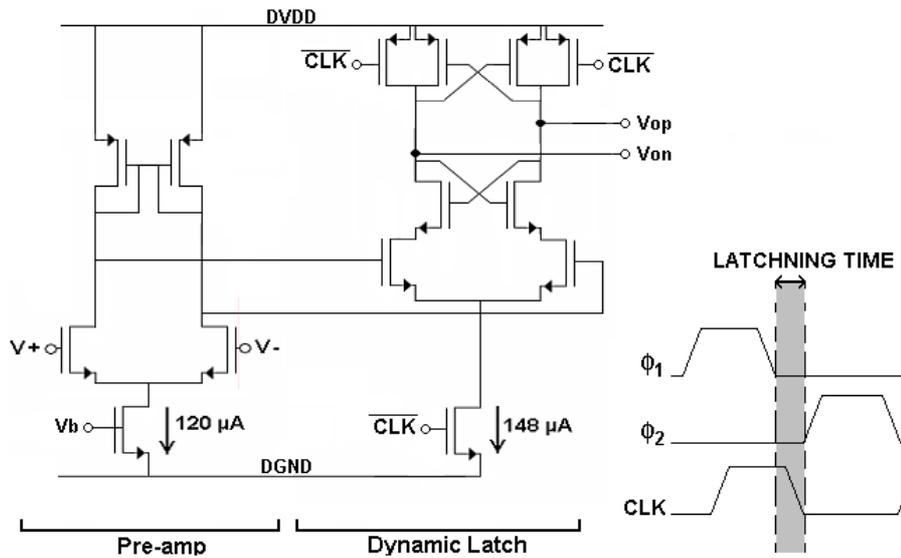


Figure 6.9: Comparator Configuration

## 6.7 Simulation results

The electrical simulation with real OTA (and associated CMFB circuit), quantizer, DAC is successfully performed for GSM mode. The output spectrum at full scale input is shown

Parameter	Value	Unit
PREAMPLIFIER DC gain	6.5	dB
PREAMPLIFIER GBW	7.8	GHz
INPUT REFFERED NOISE	142	$\mu V_{rms}$
SYSTEMATIC INPUT REFFERED OFFSET	6	mV
LATCH CLOCK	28.57-228.57	MHz
LATCH DELAY	120	ps
LOW STATE VOLTAGE VALUE	0	V
HIGH STATE VOLTAGE VALUE	1.2	V
Input common mode reference voltage	0.6	V
Analog ground voltage	0	V
Power supply voltage	1.2	V
Power consumption	258	$\mu A$

Table 6.7: Comparator performance characteristics

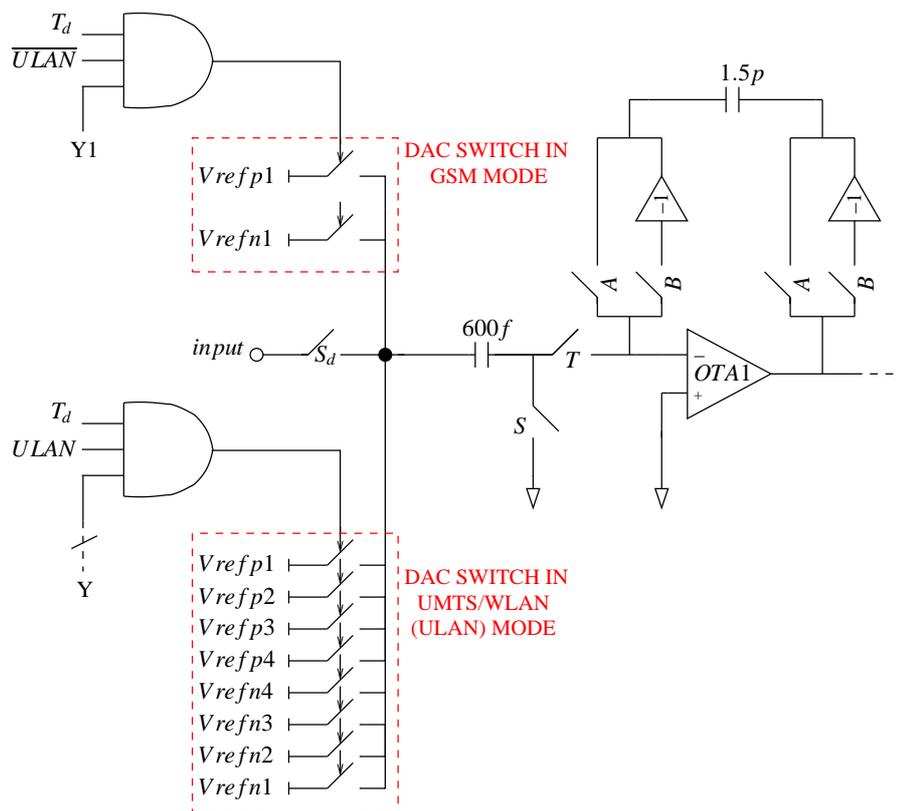


Figure 6.10: Global DAC configuration

Voltage Reference	GSM	UMTS/WLAN
Vref1=Vrefp1-Vrefn1	Vref	Vref
Vref2=Vrefp2-Vrefn2	-	$\frac{3V_{ref}}{4}$
Vref3=Vrefp3-Vrefn3	-	$\frac{V_{ref}}{2}$
Vref4=Vrefp4-Vrefn4	-	$\frac{V_{ref}}{4}$

Table 6.8: Global-DAC Voltage References

in Fig. 6.11. As presented in the figure, the resolution of 80-dB is achieved at the minimum OSR of 84 with the sampling frequency of 28.57MHz. Thus achieving the required specification of GSM mode.

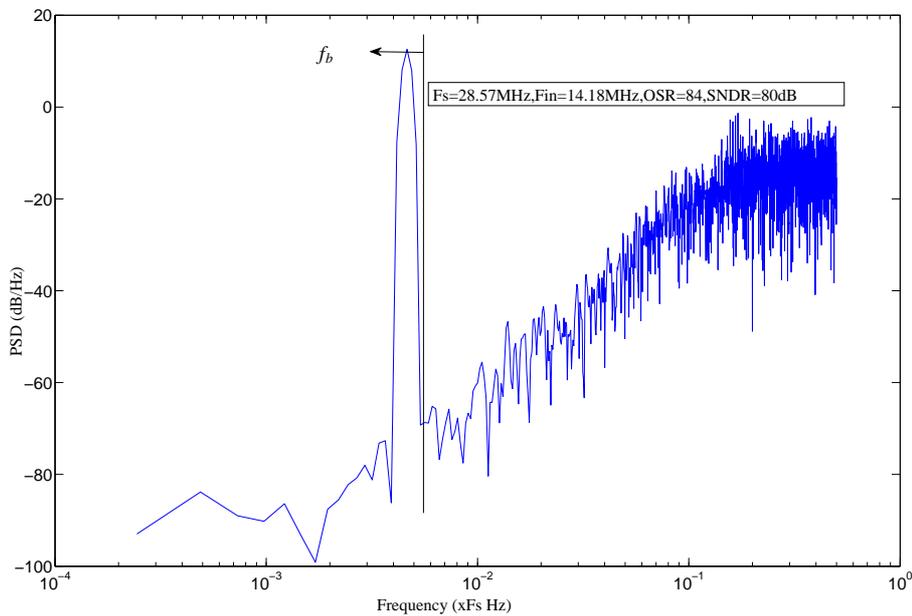


Figure 6.11: GSM mode simulation result

For the UMTS/WiFi modes of operation, an important distortion is observed in the signal band. The clean simulation result of these modes is expected to be present in a possible extension of this research.

## 6.8 Conclusion

The transistor-level implementation of a multi-mode ADC working on the principle of high-pass delta-sigma modulation is presented. The ADC has two modes of operation namely GSM/EDGE and UMTS/WLAN. This reconfigurability results in significant power saving. The implementation of key building blocks is presented in detail and their performance parameters are tabled. The simulation result of GSM mode is presented with the specified

objectives achieved; while for the UMTS/WiFi modes, the clean simulation result with the required linearity is still awaited and will be included in the future extensions of this research work.

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## Chapter 7

# Conclusion and Perspectives

### 7.1 Summary

The first part of this thesis presented the prominent radio receiver architectures which are interesting for today's wireless communication systems from the view point of reconfigurability, integrability and power consumption. An important step ahead towards the implementation of the concept of SDR is RF sampling receivers which use subsampling to bring down the signal from RF to IF. This way, the discrete time signal processing is introduced from the beginning, which is highly integrable. By using subsampling, the speed requirements on the following blocks are relaxed. The challenge in this scenario is anti-alias filtering to minimize the corruption of the signal by in-band and out-of-band interferers. This is accomplished by passive switched-capacitor filters. The state-of-the-art receiver uses a two-stage downconversion, each stage using subsampling, to achieve an acceptable compromise between downconverted signal frequency and anti-alias filtering. Though, with the increase in performance of ADCs, it has become feasible to use single-stage downconversion to decrease the component count. The downsampling is carried out in such a way that the signal is placed at  $F_s/2$  to enjoy the advantages of both zero-IF and low-IF architectures. In this scenario, the natural candidate for ADC is HP  $\Delta\Sigma$  modulator.

The second part of this thesis reviewed the state-of-the-art of  $\Delta\Sigma$  modulators. Starting from the classical feed-back architectures, the recent state-of-the-art feed-forward architectures are discussed alongwith their pros and cons. Higher-order single-loop and multi-stage modulators are also exposed which are inevitable for applications requiring high resolution. System-level modeling of the classical second-order Boser modulator is carried out to demonstrate the requirements on op-amp for this topology.

The third part was related to the study of HP  $\Delta\Sigma$  modulator. The HP  $\Delta\Sigma$  modulator shapes the quantization noise to low frequency. The signal band is located around one-half of the sampling frequency, therefore it is compatible with  $F_s/2$  IF discrete-time receiver and, in addition, completely immune to dc-offsets and flicker noise. Various existing topologies of LP  $\Delta\Sigma$  modulator are presented after adapting them for HP operation, and a new unity-STF single-loop second-order architecture is proposed. It alleviates the problems associated with traditional feedforward architecture by removing the need for an active summer. A

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novel technique to design cascaded or MASH structures is also proposed which increases the input dynamic range of the modulator. This technique is based on the systematic study of the first-stage quantizer gain and the adaptation of digital cancellation filters with this quantizer gain. An state-of-the-art architecture of multi-stage  $\Delta\Sigma$  modulator which is free from digital cancellation filters called Generalized-Multi-Stage-Closed-Loop (GMSCL) is adapted for HP operation while incorporating the proposed unity-STF single-loop architecture as its individual stage. Finally an auxiliary quantizer is added in the second-stage to increase the input dynamic range and to diminish the effect of the nonlinearities of global feedback DAC. A study on the comparison between HP and LP  $\Delta\Sigma$  modulators is also carried out, which reveals that the HP modulators are more sensitive to clock jitter thereby increasing the constraints on the clock generation circuitry. LP modulators on the other hand are increasingly sensitive to the hysteresis in the comparator necessitating an scheme to reduce the requirements on the comparator.

The fourth part of this research was aimed at selecting the best architecture of HP filter, which is the basic building block of HP  $\Delta\Sigma$  modulator. After a thorough comparative analysis of three competing topologies, the one which is recently introduced and based on alternating capacitor positions is selected. Its advantages of reduced consumption and noise are proved analytically and through simulations.

Finally a multi-standard, multi-mode ADC implementation in 65nm CMOS process is presented. It has three modes of operation namely GSM, UMTS and WiFi/WiMax. In GSM mode, the proposed second-order HP  $\Delta\Sigma$  modulator is used; while in UMTS and WiFi/WiMax modes, the double-loop, fourth-order, HP  $\Delta\Sigma$  GMSCL structure with an auxiliary quantizer is used for conversion.

## 7.2 Perspectives

The idea of a single-stage subsampling-based downconversion receiver coupled with a powerful high-pass  $\Delta\Sigma$  modulator needs to be rigorously studied and simulated. The challenge in this context is the design of an efficient anti-aliasing filter, since there is only one stage of anti-aliasing which should also perform sufficient channel filtering. The alias rejection of these filters needs to be augmented to achieve this objective. Since these subsampling circuits are implemented as SC circuits, they usually involve lot of high value capacitors. They occupy significant surface area, increase power consumption and do not scale with new CMOS technologies. Thus, an innovative RF subsampling receiver architecture is necessary to reduce the capacitors count and size involved. Another problem associated with these receiver architectures is the generation of high frequency clocks. New and innovative methods of clock synthesization, which bring accuracy to the clock signals and minimize the clock jitter noise, are to be developed.

For the GMSCL HP  $\Delta\Sigma$  modulator, much better results in terms of power consumption and surface area can be obtained by using a feedback single-loop architecture in the second stage. The reason is that much power is consumed in charging the capacitors for feedforward architectures which is not necessary because the second-stage only processes the quantization noise of the first stage. A detailed system-level study is necessary to

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design a GMSCL structure with feedforward structure in the first stage and a feedback structure in the second stage.

Finally a multi-level comparator, digital adder and multi-level feedback DAC need to be designed to properly exploit the idea of auxiliary quantizer which serves to minimize the nonlinearities generated by multi-level DAC. This way, even a larger spectrum of wireless protocols could be addressed with the ADC proposed.

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## Appendix A

# Charge-Transfer Transient in Integrator

In this annex, the charge transfer-transient of SC integrator is calculated. The influence of op-amp finite DC-Gain and finite gain-bandwidth product is taken into account. The implementation of integrator in SC circuit along with its associated clocks is shown in Fig. A.1. It has to be noted that the charge-transfer occurs in the integration  $T$  phase.

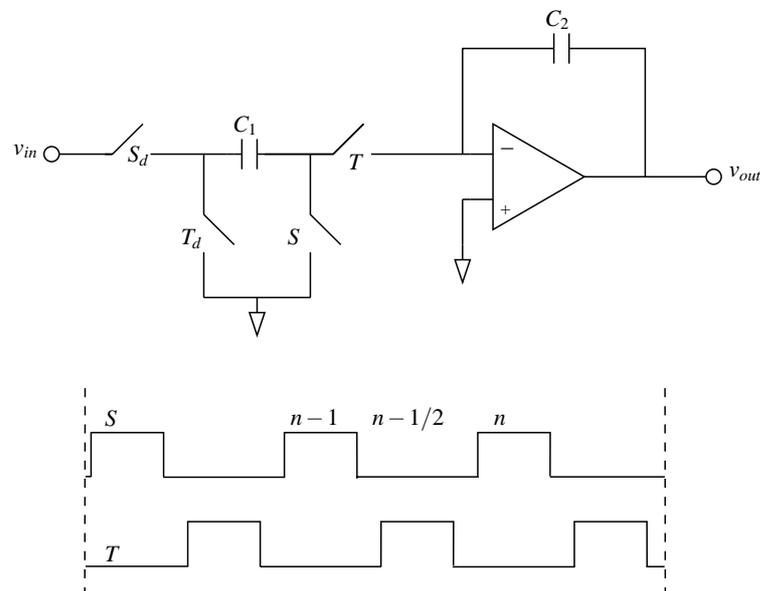


Figure A.1: Integrator implementation in a SC circuit

### A.0.1 Phase S<sub>n</sub>

In the sampling phase, the circuit configuration becomes as illustrated in Fig. A.2.  $\varepsilon$  is the voltage on the negative terminal of the op-amp and is non-zero due to the non-ideal nature of the op-amp i-e having finite DC-Gain and GBW.  $\varepsilon$  is constant during the sampling phase and is equal to its value at the end of the preceding integration phase.

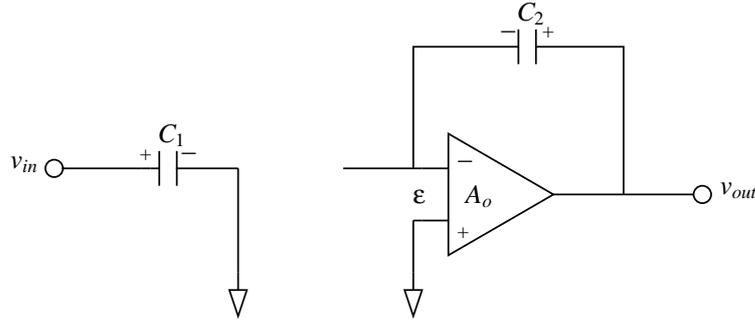


Figure A.2: Circuit configuration in sampling phase

$$Q_{C_1} = C_1 v_{in}(nT)$$

$$Q_{C_2} = C_2(v_{out} - \varepsilon)(nT)$$

### A.0.2 Phase T<sub>n-1/2</sub>

The circuit topology in the integration phase changes to as shown in Fig. A.3. The objective of this section is to find the charge transfer transient in this phase i-e to find the evolution of output voltage with time  $v_{out}(t)$  as a function of the known parameters.

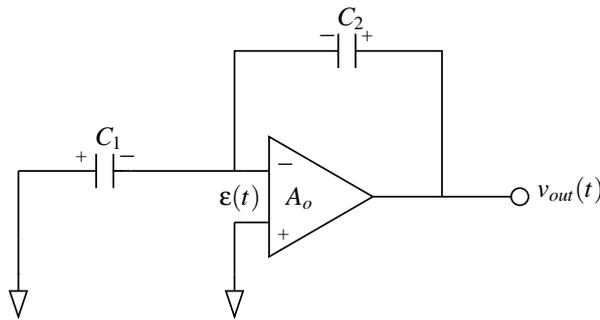


Figure A.3: Circuit configuration in charge-transfer phase

$$Q_{C_1}(t) = -C_1 \varepsilon(t)$$

$$Q_{C_2}(t) = C_2 (v_{out}(t) - \varepsilon(t))$$

By the law of conservation of charge:

$$\begin{aligned} Q_{C_1}(t) + Q_{C_2}(t) &= Q_{C_1}(n-1)T + Q_{C_2}(n-1)T \\ -C_1\varepsilon(t) + C_2(v_{out}(t) - \varepsilon(t)) &= C_1v_{in}(n-1)T + C_2(v_{out} - \varepsilon)(n-1)T \\ v_{out}(t) &= \frac{C_1}{C_2}\varepsilon(t) + \varepsilon(t) + \frac{C_1}{C_2}v_{in}(n-1) - \varepsilon(n-1) \\ &= \left(1 + \frac{C_1}{C_2}\right)\varepsilon(t) + \frac{C_1}{C_2}v_{in}(n-1) + v_{out}(n-1) - \varepsilon(n-1) \end{aligned}$$

Assuming the single-pole op-amp model, and the relation of its input evolution  $\varepsilon(t)$  with its output  $v_{out}(t)$ , as presented in [92]:

$$\varepsilon(t) = -\frac{1}{A_o}v_{out}(t) - \frac{1}{A_o\sigma_o} \frac{dv_{out}(t)}{dt}$$

where  $A_o$  is the DC-Gain,  $\sigma_o$  is the pole radian frequency and  $A_o\sigma_o$  is the unity-gain radian frequency  $GBW$  of the op-amp. And also using the following approximation:

$$\varepsilon(n-1) \approx -\frac{v_{out}(n-1)}{A_o}$$

we get:

$$\begin{aligned} v_{out}(t) &= \frac{-(C_2 + C_1)}{\sigma_o(A_oC_2 + C_2 + C_1)} \frac{dv_{out}(t)}{dt} + \frac{A_oC_2}{A_oC_2 + C_2 + C_1} \frac{C_1}{C_2} v_{in}(n-1) + \frac{A_oC_2 + C_2}{A_oC_2 + C_2 + C_1} v_{out}(n-1) \\ &= \frac{-(1+b)}{\sigma_o(A_o + 1 + b)} \frac{dv_{out}(t)}{dt} + \frac{A_o}{A_o + 1 + b} \cdot b \cdot v_{in}(n-1) + \frac{A_o + 1}{A_o + 1 + b} \cdot v_{out}(n-1) \end{aligned}$$

where  $b = C_1/C_2$  is the integrator gain. Using the approximation  $A_o + 1 + b \simeq A_o$ , we get:

$$v_{out}(t) = \frac{-(1+b)}{\sigma_o A_o} \frac{dv_{out}(t)}{dt} + \frac{A_o}{A_o + 1 + b} \cdot b \cdot v_{in}(n-1) + \frac{A_o + 1}{A_o + 1 + b} \cdot v_{out}(n-1)$$

Solving the differential equation, we get:

$$v_{out}(t) = K \cdot e^{-\left(\frac{\sigma_o A_o}{1+b}\right)t} + \alpha \cdot b \cdot v_{in}(n-1) + \beta \cdot v_{out}(n-1) \quad (\text{A.1})$$

where:

$$\alpha = \frac{A_o}{A_o + 1 + b}$$

and:

$$\beta = \frac{A_o + 1}{A_o + 1 + b}$$

In Eqn. A.1  $K$  is the constant which has to be found by the initial condition:

$$\begin{aligned} v_{out}(0) &= v_{out}(n-1) = K + \alpha \cdot b \cdot v_{in}(n-1) + \beta \cdot v_{out}(n-1) \\ \Rightarrow K &= v_{out}(n-1) - \beta \cdot v_{out}(n-1) - \alpha \cdot b \cdot v_{in}(n-1) \\ \Rightarrow K &\approx -\alpha \cdot b \cdot v_{in}(n-1) \end{aligned}$$

Using this approximation in the Eqn. A.1, we have

$$\begin{aligned} v_{out}(t) &= \beta \cdot v_{out}(n-1) + \alpha \cdot b \cdot v_{in}(n-1) \left( 1 - e^{-\left(\frac{\sigma_o A_o}{1+b}\right)t} \right) \\ &= \beta \cdot v_{out}(n-1) + \alpha \cdot b \cdot v_{in}(n-1) \left( 1 - e^{-\left(\frac{2\pi GBW}{1+b}\right)t} \right) \end{aligned} \quad (\text{A.2})$$

Equation A.2 reveals that the time-constant of the integrator is:

$$\tau = \frac{1+b}{2\pi GBW} \quad (\text{A.3})$$

## Appendix B

# Charge-Transfer Transient in Integrator-based HP Filter

In this annex, the charge transfer-transient of SC integrator-based HP filter is calculated. The influence of op-amp finite DC-Gain and finite gain-bandwidth product is taken into account. The implementation of integrator in SC circuit along with its associated clocks is shown in Fig. B.1. It has to be noted that the charge-transfer occurs in the transfer  $T$  phase.

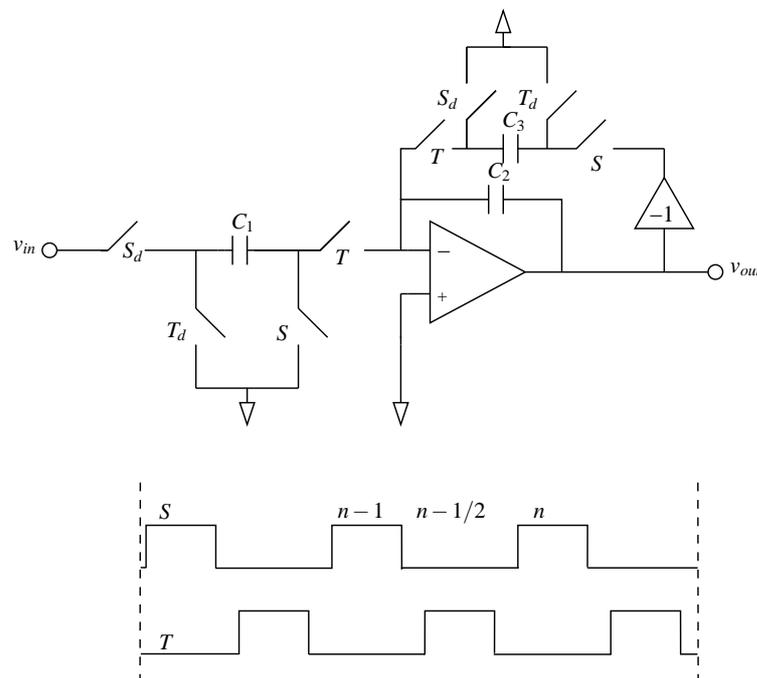


Figure B.1: Integrator-based HP filter implementation

### B.0.3 Phase S,n

In the sampling phase, the circuit configuration becomes as illustrated in Fig. B.2.  $\varepsilon$  is the voltage on the negative terminal of the op-amp and is non-zero due to the non-ideal nature of the op-amp i-e having finite DC-Gain and GBW.  $\varepsilon$  is constant during the sampling phase and is equal to its value at the end of the preceding integration phase.

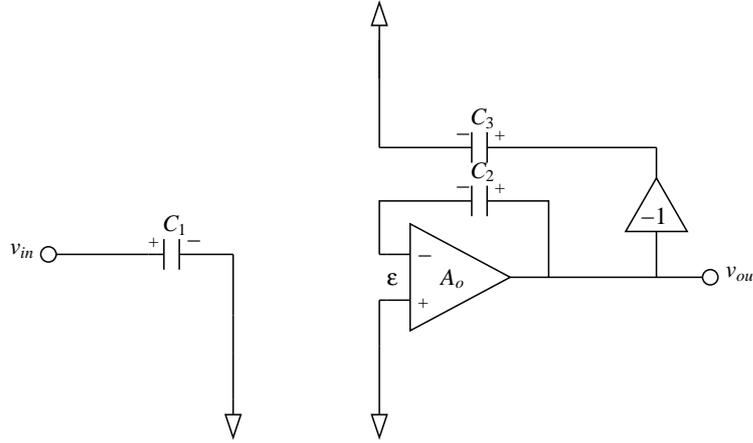


Figure B.2: Circuit configuration in the sampling phase

$$Q_{C_1} = C_1 v_{in}(nT)$$

$$Q_{C_2} = C_2 (v_{out} - \varepsilon)(nT)$$

$$Q_{C_2} = -C_3 v_{out}(nT)$$

### B.0.4 Phase T,n-1/2

The circuit topology in the charge-transfer phase changes to as shown in Fig. B.3. The objective of this section is to find the charge transfer transient in this phase i-e to find the evolution of output voltage with time  $v_{out}(t)$  as a function of the known parameters.

$$Q_{C_1}(t) = -C_1 \varepsilon(t)$$

$$Q_{C_2}(t) = C_2 (v_{out}(t) - \varepsilon(t))$$

$$Q_{C_3}(t) = -C_3 \varepsilon(t)$$

By the law of conservation of charge:

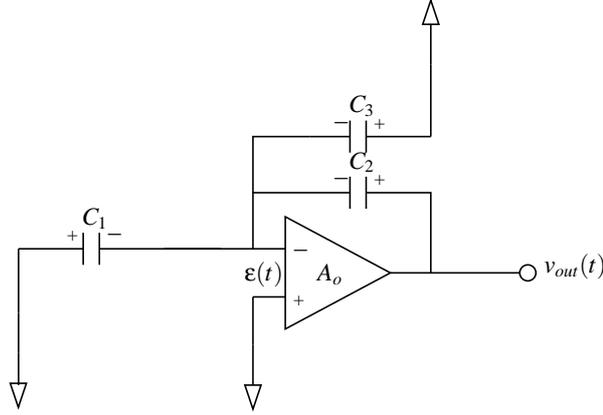


Figure B.3: Circuit configuration in charge-transfer phase

$$\begin{aligned} Q_{C_1}(t) + Q_{C_2}(t) + Q_{C_3}(t) &= Q_{C_1}(n-1)T + Q_{C_2}(n-1)T + Q_{C_3}(n-1)T \\ -C_1\varepsilon(t) + C_2(v_{out}(t) - \varepsilon(t)) - C_3\varepsilon(t) &= C_1v_{in}(n-1)T + C_2(v_{out} - \varepsilon)(n-1)T - C_3v_{out}(n-1)T \end{aligned}$$

Assuming the single-pole op-amp model, and the relation of its input evolution  $\varepsilon(t)$  with its output  $v_{out}(t)$ , as presented in [92]:

$$\varepsilon(t) = -\frac{1}{A_o}v_{out}(t) - \frac{1}{A_o\sigma_o} \frac{dv_{out}(t)}{dt}$$

where  $A_o$  is the DC-Gain,  $\sigma_o$  is the pole radian frequency and  $A_o\sigma_o$  is the unity-gain radian frequency  $GBW$  of the op-amp; and also using the following approximation:

$$\varepsilon(n-1) \approx -\frac{v_{out}(n-1)}{A_o}$$

and solving the equation for  $v_{out}(t)$ , we get:

$$\begin{aligned} v_{out}(t) &= \frac{-(C_1 + C_2 + C_3)A_o}{A_o\sigma_o(C_1 + C_2 + C_3 + A_oC_2)} \frac{dv_{out}(t)}{dt} + \frac{A_oC_1}{C_1 + C_2 + C_3 + A_oC_2} v_{in}(n-1) \\ &\quad + \frac{C_2 + A_oC_2 - A_oC_3}{A_o} v_{out}(n-1) \\ &= \frac{-(3+b)A_o}{A_o\sigma_o(A_o + 3 + b)} \frac{dv_{out}(t)}{dt} + \frac{A_o}{A_o + 3 + b} \cdot b \cdot v_{in}(n-1) + \frac{1 - A_o}{A_o + 3 + b} \cdot v_{out}(n-1) \end{aligned}$$

where  $b = C_1/C_2$  is the high-pass filter gain and  $C_3/C_2 = 2$ . Using the approximation  $A_o + 3 + b \simeq A_o$ , we get:

$$v_{out}(t) = \frac{-(3+b)}{\sigma_o A_o} \frac{dv_{out}(t)}{dt} + \frac{A_o}{A_o + 3 + b} \cdot b \cdot v_{in}(n-1) + \frac{1 - A_o}{A_o + 3 + b} \cdot v_{out}(n-1)$$

Using :

$$\frac{A_o}{A_o + 3 + b} = \alpha \quad \text{and} \quad \frac{A_o - 1}{A_o + 3 + b} = \beta$$

and solving the differential equation, we get:

$$v_{out}(t) = K \cdot e^{-\left(\frac{\sigma_o A_o}{3 + b}\right)t} + \alpha \cdot b \cdot v_{in}(n - 1) - \beta \cdot v_{out}(n - 1) \quad (\text{B.1})$$

In Eqn. B.1  $K$  is the constant which has to be found by the initial condition:

$$\begin{aligned} v_{out}(0) &= v_{out}(n - 1) = K + \alpha \cdot b \cdot v_{in}(n - 1) - \beta \cdot v_{out}(n - 1) \\ \Rightarrow K &= v_{out}(n - 1) + \beta \cdot v_{out}(n - 1) - \alpha \cdot b \cdot v_{in}(n - 1) \\ \Rightarrow K &= (1 + \beta)v_{out}(n - 1) - \alpha \cdot b \cdot v_{in}(n - 1) \end{aligned}$$

Using this result in the Eqn. B.1, we have

$$\begin{aligned} v_{out}(t) &= v_{out}(n - 1) + \{-(1 + \beta)v_{out}(n - 1) + \alpha \cdot b \cdot V_i(n - 1)\} \left(1 - e^{-\left(\frac{\sigma_o A_o}{3 + b}\right)t}\right) \\ &= v_{out}(n - 1) + \{-(1 + \beta)v_{out}(n - 1) + \alpha \cdot b \cdot V_i(n - 1)\} \left(1 - e^{-\left(\frac{2\pi GBW}{3 + b}\right)t}\right) \end{aligned}$$

This equation shows that the time-constant of the integrator-based HP filter is:

$$\tau = \frac{3 + b}{2\pi GBW} \quad (\text{B.2})$$

---

## Appendix C

# Charge-Transfer Transient in Chopper-based HP Filter

In this annex, the charge transfer-transient of SC improved HP filter is derived. The influence of op-amp finite DC-Gain and finite gain-bandwidth product is taken into account. The single-ended implementation of improved HP filter along with its associated clocks is shown in Fig. C.1. It has to be noted that the charge-transfer occurs in the phase  $T$ .

### C.0.5 Phase S,Chop A,n

In the sampling phase, the circuit configuration becomes as illustrated in Fig. C.2.  $\varepsilon$  is the voltage on the negative terminal of the op-amp and is non-zero due to the non-ideal nature of the op-amp i-e having finite DC-Gain and GBW.  $\varepsilon$  is constant during the sampling phase and is equal to its value at the end of the preceding integration phase.

$$Q_{C_1}(nT) = C_1 v_{in}(nT)$$

$$Q_{C_2}(nT) = C_2(v_{out} - \varepsilon)(nT)$$

### C.0.6 Phase T,Chop A,n-1/2

The circuit topology in the charge-transfer phase, when the clock  $ChopA$  is on, changes to Fig. C.3. The objective of this section is to find the charge transfer transient in this phase i-e to find the evolution of output voltage with time  $v_{out}(t)$  as a function of the known parameters i-e capacitor ratios, op-amp DC-Gain  $A_o$  and unity-gain frequency  $GBW$ .

$$Q_{C_1}(t) = -C_1 \varepsilon(t)$$

$$Q_{C_2}(t) = C_2 (v_{out}(t) - \varepsilon(t))$$

By the law of charge conservation:

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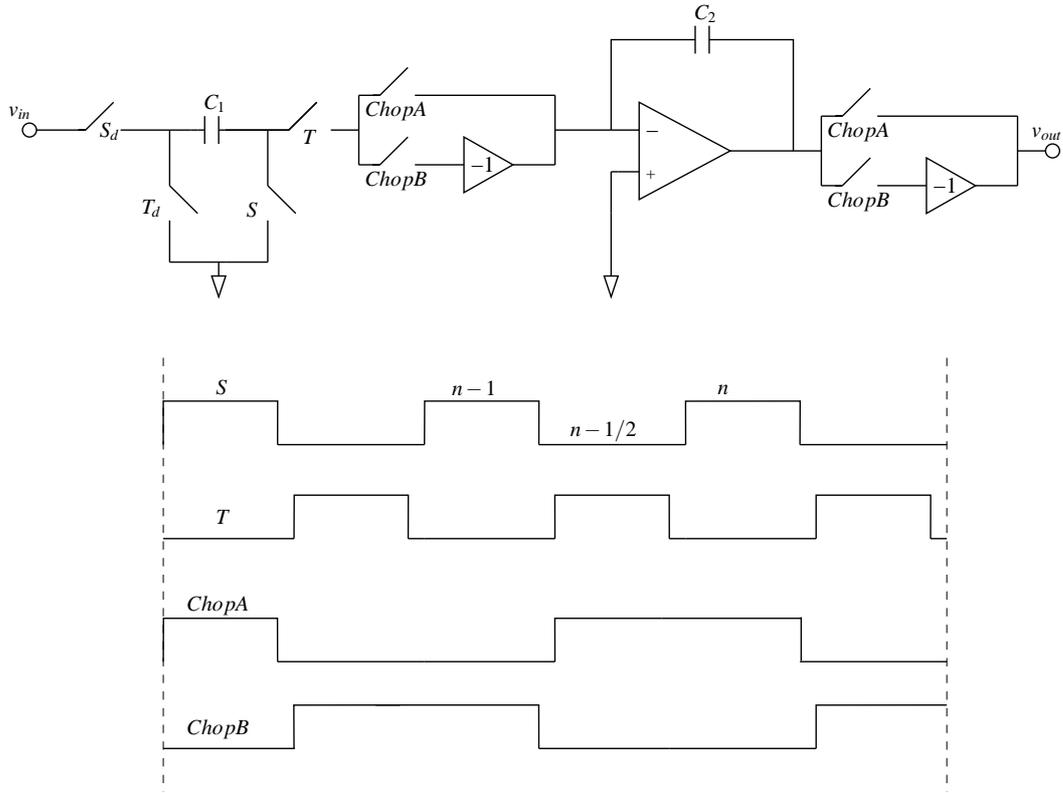


Figure C.1: Improved HP filter implementation

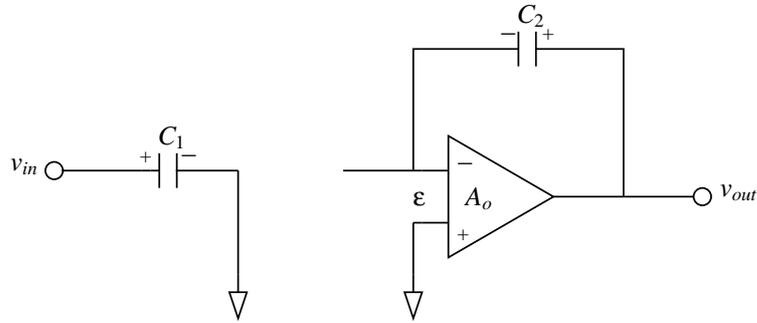
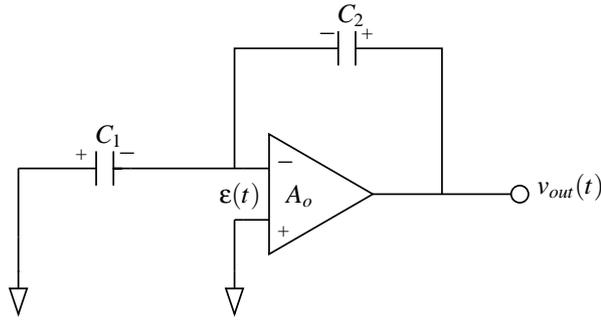
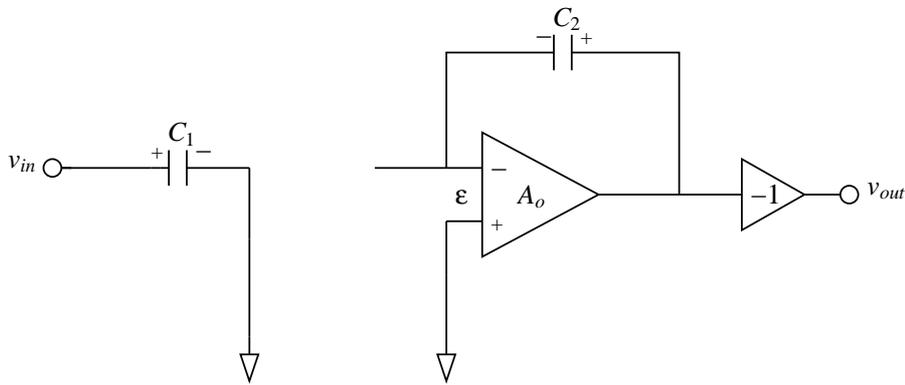


Figure C.2: Circuit configuration in the sampling phase, with *ChopA* clock on

$$Q_{C_1}(t) + Q_{C_2}(t) = Q_{C_1}(n - 1)T + Q_{C_2}(n - 1)T \tag{C.1}$$

To find the charges stored in the capacitors during the phase  $S, n - 1, ChopB$ , please refer to the Fig. C.4.

Looking at this figure, the charges stored at the end of  $(n - 1)$ th phase are evaluated as:

Figure C.3: Circuit configuration in charge-transfer phase, with *ChopA* clock onFigure C.4: Circuit configuration in the sampling phase, with *ChopB* clock on

$$Q_{C_1}(n-1)T = C_1 v_{in}(n-1)T$$

$$Q_{C_2}(n-1)T = C_2(-v_{out} - \varepsilon)(n-1)T$$

Putting these values in the charge-conservation Eqn. C.1, we get:

$$-C_1 \varepsilon(t) + C_2 (v_{out}(t) - \varepsilon(t)) = C_1 v_{in}(n-1)T + C_2 (-v_{out} - \varepsilon)(n-1)T$$

Assuming the single-pole op-amp model, and the relation of its input evolution  $\varepsilon(t)$  with its output  $v_{out}(t)$ , as presented in [92]:

$$\varepsilon(t) = -\frac{1}{A_o} v_{out}(t) - \frac{1}{A_o \sigma_o} \frac{dv_{out}(t)}{dt}$$

where  $A_o$  is the DC-Gain,  $\sigma_o$  is the pole radian frequency and  $A_o \sigma_o$  is the unity-gain radian frequency *GBW* of the op-amp; and also using the following approximation:

$$\varepsilon(n-1) \approx \frac{v_{out}(n-1)}{A_o}$$

and solving the equation for  $v_{out}(t)$ , we get:

$$\begin{aligned} v_{out}(t) &= \frac{-(C_1 + C_2)A_o}{A_o\sigma_o(C_1 + C_2 + A_oC_2)} \frac{dv_{out}(t)}{dt} + \frac{A_oC_1}{C_1 + C_2 + A_oC_2} v_{in}(n-1) - \frac{A_oC_2 + C_2}{A_o} v_{out}(n-1) \\ &= \frac{-(1+b)A_o}{A_o\sigma_o(A_o + 1 + b)} \cdot \frac{dv_{out}(t)}{dt} + \frac{A_o}{A_o + 1 + b} \cdot b \cdot v_{in}(n-1) - \frac{A_o + 1}{A_o + 1 + b} \cdot v_{out}(n-1) \end{aligned}$$

where  $b = C_1/C_2$  is the HP filter gain. Using the approximation  $A_o + 1 + b \simeq A_o$ , we get:

$$v_{out}(t) = \frac{-(1+b)}{\sigma_o A_o} \frac{dv_{out}(t)}{dt} + \frac{A_o}{A_o + 1 + b} \cdot b \cdot v_{in}(n-1) - \frac{A_o + 1}{A_o + 1 + b} \cdot v_{out}(n-1)$$

Using :

$$\frac{A_o}{A_o + 1 + b} = \alpha \quad \text{and} \quad \frac{A_o + 1}{A_o + 1 + b} = \beta$$

and solving the differential equation, we get:

$$v_{out}(t) = K \cdot e^{-\left(\frac{\sigma_o A_o}{1+b}\right)t} + \alpha \cdot b \cdot v_{in}(n-1) - \beta \cdot v_{out}(n-1) \quad (\text{C.2})$$

where  $K$  is the constant which has to be found by the initial condition:

$$\begin{aligned} v_{out}(0) &= -v_{out}(n-1) = K + \alpha \cdot b \cdot v_{in}(n-1) - \beta \cdot v_{out}(n-1) \\ \Rightarrow K &= -v_{out}(n-1) + \beta \cdot v_{out}(n-1) - \alpha \cdot b \cdot v_{in}(n-1) \\ \Rightarrow K &\approx -\alpha \cdot b \cdot v_{in}(n-1) \end{aligned}$$

Using this approximation in the Eqn. C.2, we have

$$\begin{aligned} v_{out}(t) &= -\beta \cdot v_{out}(n-1) + \alpha \cdot b \cdot v_{in}(n-1) \left( 1 - e^{-\left(\frac{\sigma_o A_o}{1+b}\right)t} \right) \\ &= -\beta \cdot v_{out}(n-1) + \alpha \cdot b \cdot v_{in}(n-1) \left( 1 - e^{-\left(\frac{2\pi GBW}{1+b}\right)t} \right) \end{aligned}$$

This equation shows that the time-constant of the Chopper-based HP filter is:

$$\tau = \frac{1+b}{2\pi GBW} \quad (\text{C.3})$$

---

## Appendix D

# Charge-Transfer Transient in Improved HP Filter

In this annex, the charge transfer-transient of SC improved HP filter is derived. The influence of op-amp finite DC-Gain and finite gain-bandwidth product is taken into account. The single-ended implementation of improved HP filter along with its associated clocks is shown in Fig. D.1. It has to be noted that the charge-transfer occurs in the phase  $T$ .

### D.0.7 Phase S,A,n

In the sampling phase, the circuit configuration becomes as illustrated in Fig. D.2.  $\varepsilon$  is the voltage on the negative terminal of the op-amp and is non-zero due to the non-ideal nature of the op-amp i-e having finite DC-Gain and GBW.  $\varepsilon$  is constant during the sampling phase and is equal to its value at the end of the preceding integration phase.

$$Q_{C_1}(nT) = C_1 v_{in}(nT)$$

$$Q_{C_2}(nT) = C_2(v_{out} - \varepsilon)(nT)$$

### D.0.8 Phase T,Chop A,n-1/2

The circuit topology in the charge-transfer phase, when the clock  $ChopA$  is on, changes to Fig. B.3. The objective of this section is to find the charge transfer transient in this phase i-e to find the evolution of output voltage with time  $v_{out}(t)$  as a function of the known parameters i-e capacitor ratios, op-amp DC-Gain  $A_o$  and unity-gain frequency  $GBW$ .

$$Q_{C_1}(t) = -C_1 \varepsilon(t)$$

$$Q_{C_2}(t) = C_2(v_{out}(t) - \varepsilon(t))$$

By the law of charge conservation:

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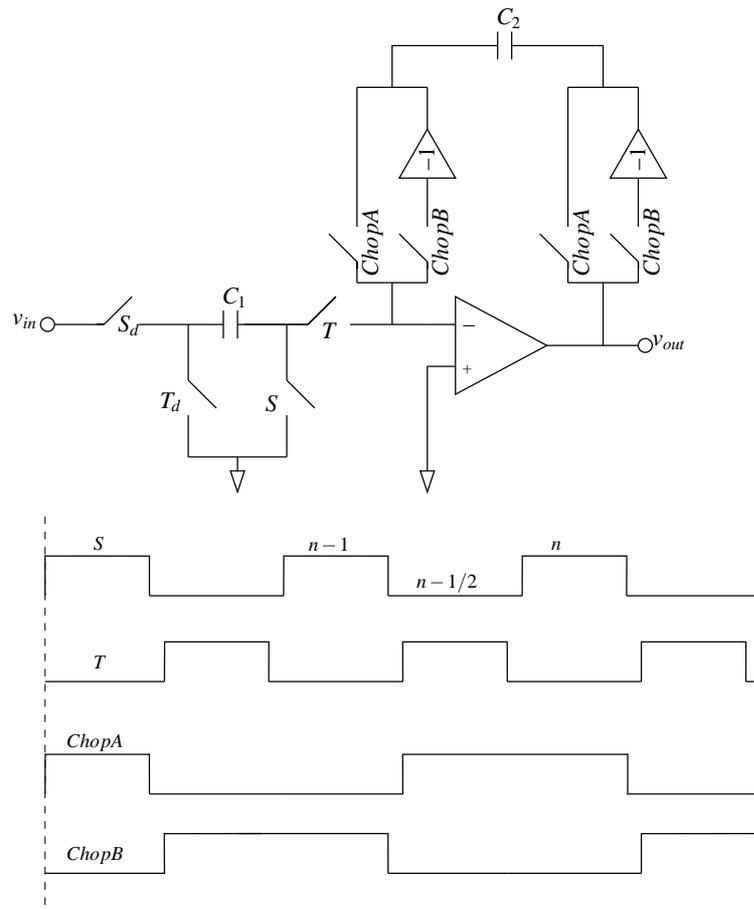


Figure D.1: Improved HP filter implementation

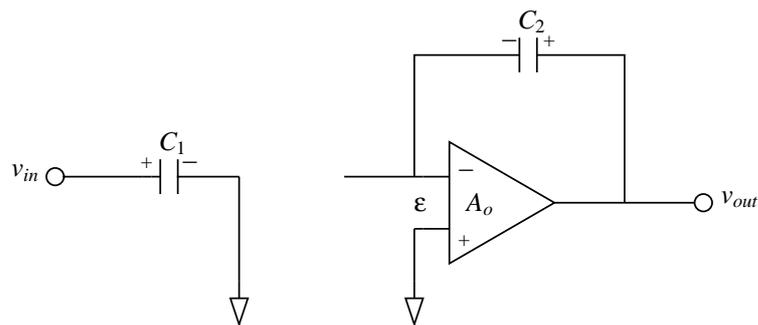


Figure D.2: Circuit configuration in the sampling phase, with *ChopA* clock on

$$Q_{C_1}(t) + Q_{C_2}(t) = Q_{C_1}(n-1)T + Q_{C_2}(n-1)T \tag{D.1}$$

To find the charges stored in the capacitors during the phase  $S, n-1, ChopB$ , please

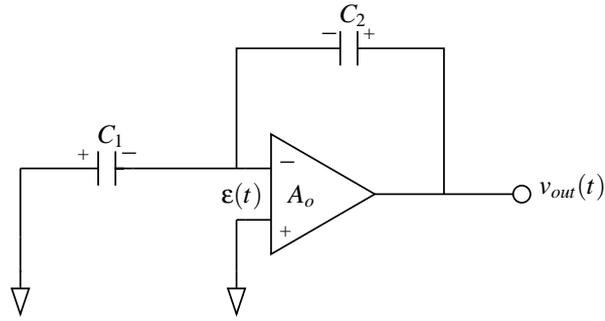


Figure D.3: Circuit configuration in charge-transfer phase, with *ChopA* clock on

refer to the Fig. D.4.

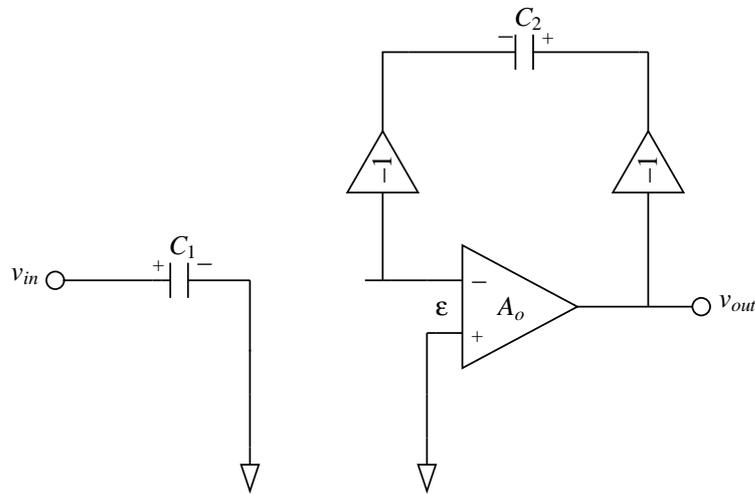


Figure D.4: Circuit configuration in the sampling phase, with *ChopB* clock on

Looking at this figure, the charges stored at the end of  $(n - 1)$ th phase are evaluated as:

$$Q_{C_1}(n - 1)T = C_1 v_{in}(n - 1)T$$

$$Q_{C_2}(n - 1)T = C_2(-v_{out} + \varepsilon)(n - 1)T$$

Putting these values in the charge-conservation Eqn. D.1, we get:

$$-C_1\varepsilon(t) + C_2(v_{out}(t) - \varepsilon(t)) = C_1 v_{in}(n - 1)T + C_2(-v_{out} + \varepsilon)(n - 1)T$$

Assuming the single-pole op-amp model, and the relation of its input evolution  $\varepsilon(t)$  with its output  $v_{out}(t)$ , as presented in [92]:

$$\varepsilon(t) = -\frac{1}{A_o}v_{out}(t) - \frac{1}{A_o\sigma_o} \frac{dv_{out}(t)}{dt}$$

where  $A_o$  is the DC-Gain,  $\sigma_o$  is the pole radian frequency and  $A_o\sigma_o$  is the unity-gain radian frequency  $GBW$  of the op-amp; and also using the following approximation:

$$\varepsilon(n-1) \approx -\frac{v_{out}(n-1)}{A_o}$$

and solving the equation for  $v_{out}(t)$ , we get:

$$\begin{aligned} v_{out}(t) &= \frac{-(C_1 + C_2)A_o}{A_o\sigma_o(C_1 + C_2 + A_oC_2)} \frac{dv_{out}(t)}{dt} + \frac{A_oC_1}{C_1 + C_2 + A_oC_2} v_{in}(n-1) - \frac{A_oC_2 + C_2}{A_o} v_{out}(n-1) \\ &= \frac{-(1+b)A_o}{A_o\sigma_o(A_o + 1 + b)} \frac{dv_{out}(t)}{dt} + \frac{A_o}{A_o + 1 + b} \cdot b \cdot v_{in}(n-1) - \frac{A_o + 1}{A_o + 1 + b} \cdot v_{out}(n-1) \end{aligned}$$

where  $b = C_1/C_2$  is the HP filter gain. Using the approximation  $A_o + 1 + b \simeq A_o$ , we get:

$$v_{out}(t) = \frac{-(1+b)}{\sigma_o A_o} \frac{dv_{out}(t)}{dt} + \frac{A_o}{A_o + 1 + b} \cdot b \cdot v_{in}(n-1) - \frac{A_o - 1}{A_o + 1 + b} \cdot v_{out}(n-1)$$

Using :

$$\frac{A_o}{A_o + 1 + b} = \alpha \quad \text{and} \quad \beta = \frac{A_o - 1}{A_o + 1 + b}$$

and solving the differential equation, we get:

$$v_{out}(t) = K \cdot e^{-\left(\frac{\sigma_o A_o}{1+b}\right)t} + \alpha \cdot b \cdot v_{in}(n-1) - \beta \cdot v_{out}(n-1) \quad (D.2)$$

where  $K$  is the constant which has to be found by the initial condition:

$$\begin{aligned} v_{out}(0) &= -v_{out}(n-1) = K + \alpha \cdot b \cdot v_{in}(n-1) - \beta \cdot v_{out}(n-1) \\ \Rightarrow K &= -v_{out}(n-1) + \beta \cdot v_{out}(n-1) - \alpha \cdot b \cdot v_{in}(n-1) \\ \Rightarrow K &\approx -\alpha \cdot b \cdot v_{in}(n-1) \end{aligned}$$

Using this approximation in the Eqn. D.2, we have

$$\begin{aligned} v_{out}(t) &= -\beta \cdot v_{out}(n-1) + \alpha \cdot b \cdot v_{in}(n-1) \left( 1 - e^{-\left(\frac{\sigma_o A_o}{1+b}\right)t} \right) \\ &= -\beta \cdot v_{out}(n-1) + \alpha \cdot b \cdot v_{in}(n-1) \left( 1 - e^{-\left(\frac{2\pi GBW}{1+b}\right)t} \right) \end{aligned}$$

This equation shows that the time-constant of the improved HP filter is:

$$\tau = \frac{1 + b}{2\pi GBW} \quad (\text{D.3})$$



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