Portable design of ADPLL for TV applications

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Conception portable d'une ADPLL pour des applications TV

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Résumé

Dans un système radio communication pour les applications hautes fréquences (>300 MHz), la partie frontal RF est généralement analogique et alors moins compatible avec la partie numérique bande de base. La consommation d'énergie, la surface et le coût de la partie analogique sont importants par rapport à la partie numérique. La migration vers des systèmes numériques apporte plusieurs avantages des conceptions numériques comme la possibilité d'utiliser des outils de CAD *Computer Aided Design*, de plus les circuits numériques sont plus faciles à tester, plus petit en surface et leur temps de conception est plus court contrairement aux circuits analogiques qui demande plusieurs itérations de fabrication avant leur commercialisation.

Le synthétiseur de fréquence est un élément clé. On veut un temps d'accrochage réduit pour permettre les sauts de fréquence (changement de canal), un signal stable, précis et avec moins de surface de circuit et moins de consommation d'énergie. Une PLL est un composant dont les signaux sont analogiques ou mixtes. Alors qu'une ADPLL est une boucle dont tous les signaux d'entrées/sorties sont numériques. Une ADPLL est plus facilement intégrée sur un SoC qu'une boucle analogique et plus robuste au bruit qui vient de la partie numérique bande de base.

Dans ce mémoire on propose dans le premier chapitre un modèle comportemental de l'ADPLL pour les applications radio autour de 2GHz comme le GSM et le Bluetooth. Le modèle Linéaire Variant en Temps (LTV) du bruit de phase de l'oscillateur est intégré dans un modèle haut niveau de l'ADPLL en utilisant VHDL-AMS. Dans le deuxième chapitre on propose une conception portable de l'ADPLL pour les applications TV. L'ADPLL conçue contient un oscillateur en anneau interpolateur contrôlé numériquement et un Convertisseur Temps en Numérique TDC basé sur le DCO pour une réduction de la consommation de puissance.

Chapitre 1

Modélisation comportementale du bruit de phase de l'ADPLL

Plusieurs architectures des boucles à verrouillage de phase numériques sont présentées dans la littérature, [1, 2, 3, 4] pour les applications hautes fréquences. Les éléments clés dans la conception de la boucle numérique sont : le calcul de dephasage entre la phase de la référence et la phase variable, la structure du filtre de la boucle, l'existence ou non d'un convertisseur analogique numérique pour le control numérique de l'oscillateur et la topologie de l'oscillateur. En plus, dans une ADPLL tous les signaux d'entrée/sortie sont numériques. On opte pour l'architecture de l'ADPLL proposé par [3] qui a été développée progressivement pour les applications GSM et Bluetooth en utilisant les processus 130nm, 90nm, et 65nm car elle constitue un bon démonstrateur pour notre objectif de modélisation.

Le schéma de l'ADPLL de [3] est montrée dans la figure 1.1. Cette boucle contient un oscillateur contrôlé numériquement DCO, deux accumulateurs de phase dont un pour la phase de la référence et le deuxième est pour la phase variable. Elle contient aussi un comparateur de phases numériques, un filtre numérique et un TDC. Cette boucle est conçue pour

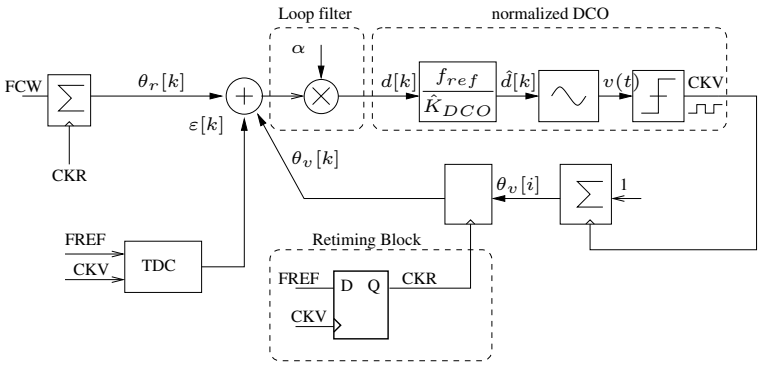

FIG. 1.1 – La boucle à vérrouillage de phase numérique de [3]

les applications GSM et Bluetooth et son bruit de phase est égal à -124 dBc/Hz@600kHz de la fréquence de porteuse (2.4GHz).

1.1 Phase de référence et phase variable

On appelle T_v la période instantanée du DCO, CKV le signal de la sortie du DCO, Fref est le signal de référence, T_R est sa période. On suppose que $T_R >> T_v$. Dans les applications radio fréquences le signal de référence est un signal de fréquence entre 10MHz et 40MHz, alors que le signal du DCO est de quelques GHz.
On suppose aussi pour simplifier les équations qu'en régime stable les périodes instantanées T_R et T_v sont invariantes en temps. Ainsi, Les instants de passage par zéro des deux signaux sont donnés par les équations

$$t_v = i.T_v \tag{1.1}$$

$$t_r = k.T_R + t_0 \tag{1.2}$$

Où i = 1,2,...et k = 1,2,... sont les indices de passage par zéro pour les signaux CKV et Fref et t_0 est l'offset initial entre les deux signaux. On normalise les deux équations en les divisant par T_v et on définie les phases instantanées et normalisées θ_v et θ_r, la phase variable et la phase de référence respectivement, et on a

$$\theta_v = t_v/T_v = i \tag{1.3}$$

$$\theta_r = t_r/T_v = kN + \theta_0 \tag{1.4}$$

Où N est le rapport entre la période de référence et la période RF désirée. Alors, la phase variable θ_v est une accumulation du nombre 1 à chaque front montant (ou descendant) du signal CKV. La phase de la référence est une accumulation du nombre N connu à priori comme le FCW à chaque front montant (ou descendant) du signal référence. Alors, on a les deux équations suivantes

$$\theta_v = \sum_{l=1}^{i} l \tag{1.5}$$

$$\theta_r = \sum_{l=1}^{k} FCW \tag{1.6}$$

Le mot numérique de commande de la fréquence RF désirée est FCW et c'est le rapport entre la valeur estimée de la fréquence variable de CKV et la fréquence de référence Fref et c'est donné par l'équation 1.7. N_i et N_f sont les parties entières et fractionnaires de FCW respectivement.

$$FCW = \frac{\varepsilon(f_v)}{f_R} = \frac{T_R}{\varepsilon(T_v)} = N_i + N_f \tag{1.7}$$

Dans le régime d'accrochage de la boucle, la différence de phase ϕ_E entre le signal de référence et le signal CKV est constante ou zéro. Mais la non synchronisation entre les instants t_v et t_r pose un problème de métastabilité. En mathématique, les deux signaux t_v et t_r sont discrets et non synchrones alors on ne peut pas les comparer sans faire une interpolation. D'où, on est obligé de faire un sur-échantillonage de la référence Fref par le signal CKV et on utilise le signal résultat CKR pour accumuler le mot FCW. La phase de la référence est ainsi modifié par une erreur $\varepsilon[k]$ et peut s'écrire sous la forme

$$\theta_r[k] = t_r/T_v = k.FCW + \theta_0 + \varepsilon[k] \tag{1.8}$$

La valeur de $\varepsilon[k]$ peut être calculée et corrigée et on explique la procedure dans la section du TDC.

1.2 Détecteur de phase

L'erreur de phase ϕ_E est la différence entre la phase de la référence θ_r et la phase variable θ_v comme le montre l'équation :

$$\phi_E[k] = \theta_r[k] - \theta_v[k] \tag{1.9}$$

L'équation 1.8 exprime $\theta_r[k]$ en fonction du mot de commande FCW et de $\varepsilon[k]$. La phase de la référence contient une partie entière $\theta_{ri}[k]$ et une partie fractionnaire $\theta_{rf}[k]$ et $\varepsilon[k]$. On peut écrire l'erreur de phase avec l'équation

$$\phi_E[k] = (\theta_{ri}[k] - \theta_v[k]) + (\theta_{rf}[k] + \varepsilon[k]) \tag{1.10}$$

Dans l'équation précédente on a séparé la partie entière $(\theta_{ri}[k], \theta_v[k])$ de la partie fractionnaire $(\theta_{rf}[k], \varepsilon[k])$. Le détecteur de phase est montré dans la fig.1.2. La partie entière est

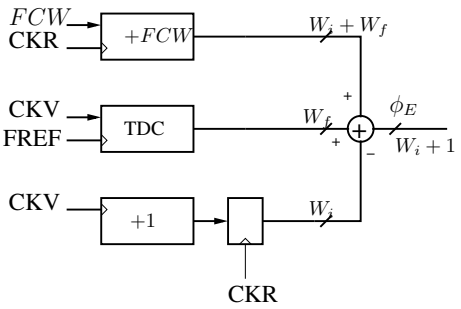

FIG. 1.2 – Le diagramme du détecteur de phase. CKR est le signal Fref après la synchronisation par CKV

codée sur W_i bits et la partie fractionnaire est codée sur W_f bits. Les valeurs de W_i et de W_f sont calculée dans 1.2

Dimensionnement du détecteur On veut écrire le modèle en VHDL pour les applications Bluetooth. Les contraintes du model sont montrées dans le tableau 1.1. On choisit la fréquence de la référence égale à 13MHz. On peut calculer le mot numérique de commande FCW à partir de l'équation 1.7. Les valeurs de la partie entière de FCW pour couvrir toute la bande donnée sont dans le tableau 1.1. On constate que N_i peut être codé sur 8 bits. La partie fractionnaire N_f est codée sur 15 bits. Le mot alors est codé comme le montre l'exemple .

Exemple On suppose qu'on veut générer la fréquence 2.4GHz et la référence est égale à 13MHz. Le mot numérique est calculé à partir de l'équation 1.7.

$$FCW = \frac{2.402GHz}{13MHz} = 184.76923 \simeq 184 + \frac{25206}{2^{15}} \tag{1.11}$$

D'où $N_i = 184$ et $N_f = 25206$. L'erreur dans le calcul de N_f introduit une erreur dans le calcule de la fréquence f_{out} par rapport à la valeur désirée. Cette erreur de fréquence est calculé comme le montre l'équation 1.12. L'erreur est égale à 61Hz, alors le codage de N_f sur 15 bits est suffisant.

$$\Delta f_{out} = f_{out} - f_{ref} * (184 + 2^{-15} * 25206)) = 61Hz \tag{1.12}$$

	Fréquence	$N_i(8bits)$	$N_f(15bits)$
minimale	2.402GHz	184	25206
maximale	2.49GHz	191	17644
centrale	2.44GHz	187	22685

Tab. 1.1 – Les fréquences Bluetooth

1.3 Convertisseur temps en numérique *TDC*

A cause de la synchronisation des compteurs sur les fronts du DCO, la précision de la phase variable est égale à $\pm T_v/2$. Pour les applications télécoms on a besoin de plus de précision sur la phase variable. Cette erreur de quantification peut être calculée et mesurée en utilisant un TDC. Le TDC va calculer le retard des fronts montants et descendants du signal CKV par rapport à FREF avec une précision égale au délai nominal d'un inverseur CMOS de la technologie $0.13\mu m$. L'architecture du TDC est montrée dans la fig.1.4. Le TDC va calculer le retard du front montant t_r et le retard t_f du front descendant par rapport à FREF comme le montre la fig.1.3, puis il calcule la période instantanée T_v. On voit à partir de la figure que la période est calculée à partir de t_r et t_f selon l'équation 1.13.

$$T_v = 2.|t_r - t_f| \tag{1.13}$$

En pratique, il est préférable de calculer la période T_v précisément. La période moyenne $\overline{T_v}$ est plus précise dans ce cas. La période est un nombre entier (en fonction du délai d'inverseur) et en calculant la période moyenne sur un nombre N on ajoute plus de bit dans la partie fractionnaire avec des opérations plus lentes. La période moyenne $\overline{T_v}$ est donnée par l'équation 1.14.

$$\overline{T_v} = \frac{1}{N}\sum_{n=1}^{N} T_v(n) \tag{1.14}$$

Le TDC calcule le retard des fronts montants et descendants de CKV par rapport à FREF

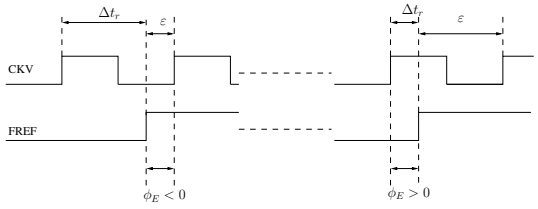

Fig. 1.3 – Le retard ε en fonction de t_r et t_f

et l'erreur $\varepsilon[k]$ peut être calculer à partir de l'équation suivante :

$$\varepsilon[k] = 1 - \frac{t_r}{T_v} \tag{1.15}$$

Architecture du TDC Le TDC est composé d'une ligne de retard faite d'inverseurs qui produit un certain nombre d'horloges retardées $D(i)$ égale au nombre d'inverseurs L. La sortie de chaque inverseur est synchronisée par la référence FREF et on obtient à la sortie un vecteur Q de même longueur L. Son architecture est illustrée dans la fig.1.4. Le

nombre d'inverseurs L peut être calculé à partir de l'équation 1.16.

$$L \geq \frac{max(T_v)}{min(t_{inv})} \tag{1.16}$$

La fréquence minimale à la sortie de l'ADPLL est équivalente à la période maximale qu'on

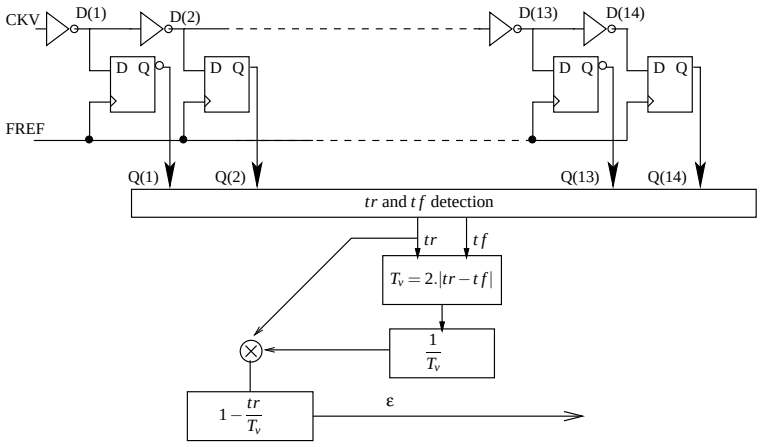

FIG. 1.4 – architecture du TDC

veut avoir, voir tableau 1.1. Cette période est égale à $416.3ps$ et le nombre d'inverseurs nécessaire pour couvrir cette période est égale à 14, le temps de retard minimum de l'inverseur est égal à $t_{inv} = 30ps$ pour la technologie considérée [5]. La lecture du vecteur TDC_Q permet de mesurer le retard de FREF sur les derniers fronts montants et descendants de CKV. Le passage de la valeur '1' à '0' détecte le front descendant t_f et le passage de '0' à '1' indique la valeur t_r, voir l'exemple de la fig.1.5. Dans cet exemple la période est égale à $(8.t_{inv})$. On voit que $t_r = 6$ et $t_f = 2$. Ainsi, la période est égale à 8 dans cet exemple.

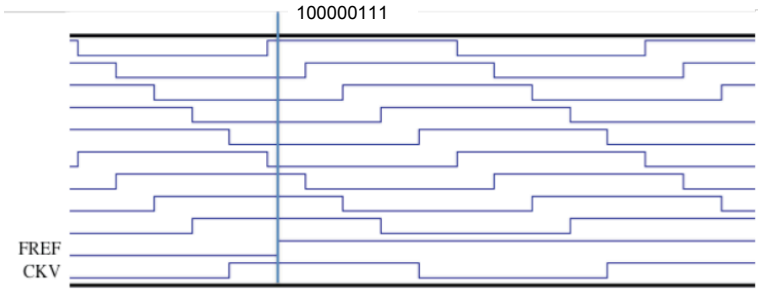

FIG. 1.5 – Le calcule de t_r et t_f par le TDC

1.4 Modèle comportemental temporel du DCO

Le DCO est contrôlée par le mot numérique et le signal de sortie v(t) est analogique et peut être écrit sous la forme :

$$v(t) = Acos(\omega_0 t + \varphi(t)) = Acos(\int_0^t (2\pi f_{out} dt) + \varphi(t)) \tag{1.17}$$

Où φ est le bruit de phase du DCO et f_{out} est la fréquence de sortie. Le bruit de phase est modélisé par le modèle linéaire variant en temps LTV qui se base sur la fonction impulsionnelle de sensibilité de l'oscillateur.

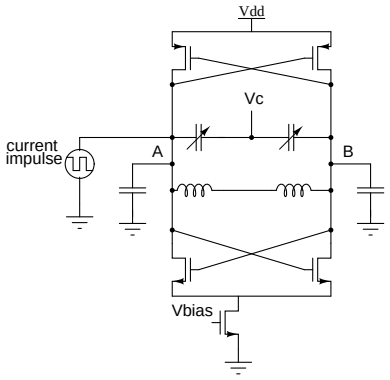

Fig. 1.6 – Un oscillateur LC

Le gain du DCO est le changement de la fréquence de sortie qui répond à un changement du mot numérique à son entrée. Un gain linéaire est recherché. Dans ce cas la fréquence de sortie peut être écrite comme l'équation 1.18.

$$f_{out} = f_c + \Delta f = f_c + K_{DCO}.\hat{d[k]} \tag{1.18}$$

Où f_c est la fréquence centrale, K_{DCO} est le gain du DCO et c'est par définition le changement δf de la fréquence f_{out} pour un changement du mot numérique égale à 1LSB. K_{DCO} est donné par l'équation 1.19.

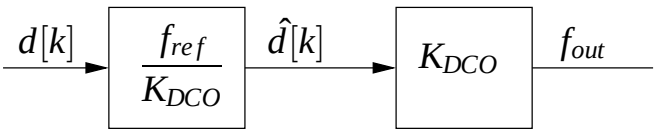

Fig. 1.7 – Modèle temporel du DCO

$$K_{DCO} = \frac{\delta f}{1LSB} \tag{1.19}$$

L'erreur de phase Δf est exprimée en fonction de la fréquence de la référence f_r à la sortie du comparateur de phase d'une part et en fonction de K_{DCO} d'autre part. Un block de normalisation est ajouté comme on voit dans la figure 1.7. Le premier bloc fait la normalisation et le deuxième calcule et génère le signal périodique CKV de fréquence f_{out}.

1.4.1 Modèle du bruit du DCO

On considère un oscillateur LC illustré dans la figure 1.6. Les sources de bruit dans le DCO sont le bruit blanc d'origine thermique produit par les résistances parasites et le bruit en $1/f$ des transistors CMOS. Un résultat de simulation Spectre du bruit du circuit est montré dans la figure 1.8. On voit dans cette figure les deux régions de bruit, en $1/f$ et le bruit blanc. Le point $\omega_{1/f}$ est vue 3MHz.

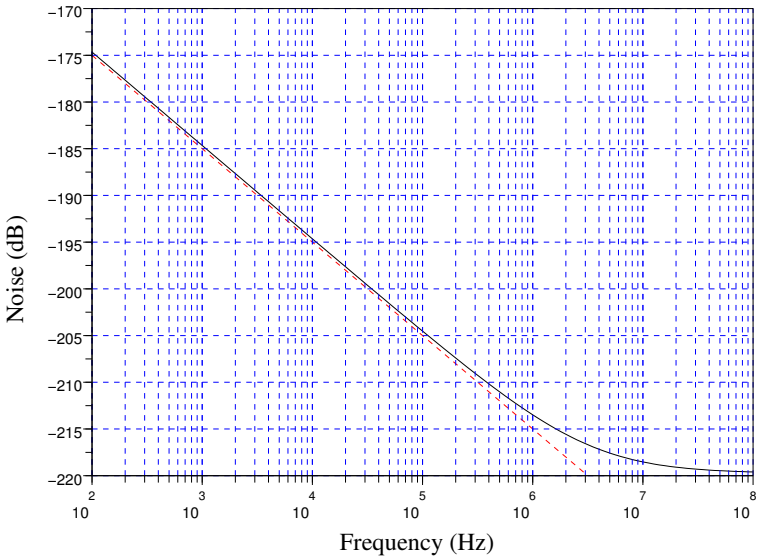

FIG. 1.8 – Le bruit CMOS de l'oscillateur LC. C'est le résultat de l'analyse noise de Spectre

Générateur de bruit en 1/f Le bruit en $1/f$ est modélisée en VHDL-AMS par la somme de bruits blancs de distribution Gaussienne N(0,1) filtrés par des filtres passe-bas comme on voit dans le figure 1.9, [6]. Les filtres h_k ont des réponses impulsionnelles qui peut être écrite par

$$y_k[i] = (1 - a_k)y_k[i-1] + a_k A^{-(k-1)}x[i] \tag{1.20}$$

Où k est le numéro du filtre, $x[i]$ est le bruit blanc de distribution normale N(0,1) modélisée

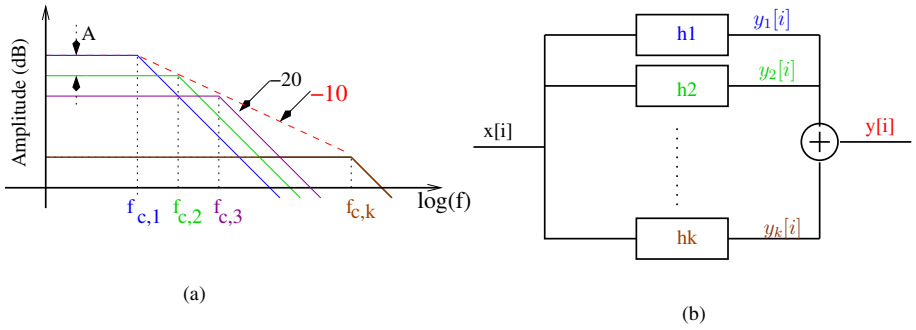

FIG. 1.9 – (a) : La composition de la pente -10dB à partir de la somme de bruit blanc filtré passe bas -20dB. (b) : Schéma block du générateur de bruit en $1/f$.

par la méthode de Box-Muler, a_k est calculé à partir de l'équation 1.21 et A est l'atténuation linéaire du filtre et il est donné par l'équation 1.22.

$$a_k = 2\pi \frac{f_{c,k}}{f_s} \tag{1.21}$$

Où f_s est la fréquence d'échantillonnage. Chaque filtre forme une zone différente du spectre et la somme des sorties des filtres forme le bruit en $1/f$ désiré.

$$slope = \frac{A_{dB}}{r} \tag{1.22}$$

A_{dB} est l' atténuation en dB des filtres. Chaque filtre a une fréquence de coupure différente $f_{c,k}$ et r le rapport de deux fréquences voisines comme montre l'équation suivante :

$$r = \frac{f_{c,k+1}}{f_{c,k}} \tag{1.23}$$

La réponse fréquentielle de chaque filtre a une pente égale à -20 dB/décade. La somme des signaux $y_k[i]$ à la sortie des filtres construit le signal $y[i]$ avec une densité spectrale de pente égale à -10 dB/décade.

Dans la simulation, le générateur simule le bruit du circuit de la fig.1.6. Le point $\omega_{1/f}$ est repéré à 3 MHz avec Spectre, voir fig.1.8. Dans notre modèle, ce générateur est composé de cinq filtres dont les fréquences de coupure sont $f_{c,1} = 300\ Hz$, $f_{c,2} = 3\ kHz$, $f_{c,3} = 30\ kHz$, $f_{c,4} = 300\ kHz$ et $f_{c,5} = 3\ MHz$. La fréquence d'échantillonnage f_s est égale à 300 MHz. Celui-ci est ajouté à l'entrée du modèle du VCO. Le bruit de phase du VCO est modélisé comme présenté dans 1.4.2.

1.4.2 Modélisation du bruit de phase de l'oscillateur

Le modèle proposé par Hajimiri considère que le bruit de phase est dépendant du temps τ de l'injection. Il dépend de la fonction de la sensibilité ISF de l'oscillateur et il prédit le bruit de phase de l'oscillateur et déplacement du point $\omega_{1/f}$ vers un nouveau point ω_{1/f^3} qui dépend de la conception. La fonction ISF est périodique, on peut la décomposer en série de Fourier comme le montre l'équation 1.24.

$$\Gamma(\omega_{out}\tau) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n cos\left(n\omega_{out}\tau + \theta_n\right) \tag{1.24}$$

Où $\Gamma(\omega_{out}\tau)$ est la fonction ISF, τ est l'instant d'injection. La phase instantanée de l'oscillateur peut s'écrire en fonction de l'ISF comme :

$$\varphi(t) = \frac{1}{q_{max}}.[\frac{C_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} C_n \int_{-\infty}^{t} i(\tau)\, cos(n\omega_0\tau)\, d\tau] \tag{1.25}$$

Où $i(t)$ est le courant d'injection sur le noeud de sortie de l'oscillateur et q_{max} est la charge maximale qui se déplace à cause de l'injection. Finalement, le signal de l'oscillateur est obtenu directement par la relation 1.17. Un bloc diagramme du modèle est montré dans la fig.1.10. Le comportement en sortie du modèle de bruit de phase est en $1/f^2$ si la source de bruit à l'entrée est un générateur de bruit blanc. Par contre, si la source de bruit a une densité spectrale en $1/f$, la sortie du modèle est un bruit de phase en $1/f^3$.

1.4.3 La détermination de l'ISF

Plusieurs méthodes approximatives de détermination de l'ISF sont présentées dans la littérature [7] et la méthode la plus exacte propose d'injecter une impulsion $i(t)$ à un instant τ de la période T et de simuler l'oscillateur pour quelques périodes après la période de l'injection. En calculant la déviation Δt de l'instant de passage par zéro, on peut en déduire le déphasage $\Delta\varphi = 2\pi\Delta t/T$, produit par l'injection. On change l'instant d'injection τ afin de déterminer l'ISF sur une période complète. Une implémentation automatisée de la procédure est développée. Scilab [8] est utilisé comme interface entre le simulateur Spectre et le concepteur et comme un environnement de calcul arithmétique. L'oscillateur de la

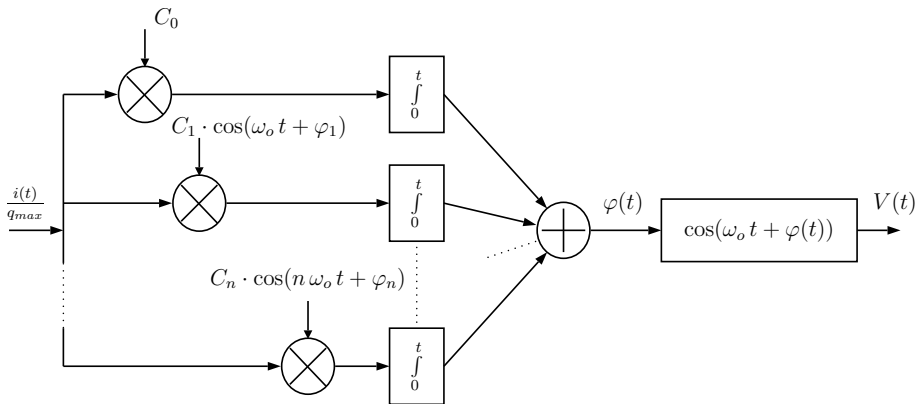

FIG. 1.10 – Les blocs du modèle de VCO

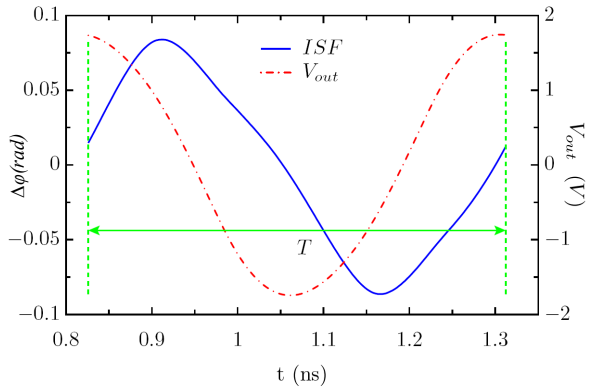

FIG. 1.11 – Les variations de l'ISF en fonction du temps et de la phase du signal oscillant

fig.1.6 est conçue en CMOS 90nm. La source $i(t)$ est injectée sur le noeud de la sortie de l'oscillateur. La quantité de charge injectée est choisie telle qu'elle ne change pas la linéarité de la réponse du bruit de phase. Dans notre mesure, le paramètre de temps d'injection est augmenté par pas de 1 ps afin de couvrir une période $T_0 = 1/f_0 = 1/2\ GHz \simeq 0.5ns$. Le nombre total de points de la fonction ISF est 500 points par période. Un processeur puissant est utilisé pour les simulations, Intel Xeon CPU 3.20 GHz. Le temps de simulation est égal à 30mn pour 500 points/période.

Les résultats de la simulation sont montrés dans la fig.1.11. On observe dans cette figure que la fonction ISF atteint son maximum quand le signal oscillant passe par zéro. Cette méthode de détermination de l'ISF est très utile dans le développement du modèle du VCO avec le bruit de phase.

1.5 Les résultats de simulation du modèle VHDL-AMS de l'ADPLL

Le modèle complet de l'ADPLL est implémenté en VHDL-AMS. Le détecteur de phase contient l'accumulateur du mot de controle numérique FCW, le compteur de CKV, et le TDC. Le filtre de la boucle est un filtre numérique d'ordre zéro et d'atténuation α. La

boucle est du premier ordre. L' influence de la valeur de α est présentée dans **??**. Comme les signaux d'entrées/sorties des blocs sont numériques, le détecteur de phase peut être modélisé en VHDL. D'autre part l'utilisation de VHDL-AMS permet la portabilité du modèle et la rapidité de l'exécution.

On s'intéresse dans la simulation du modèle aux performances de l'ADPLL en terme de bruit de phase en présence du DCO et du TDC. Le paramètres génériques sont : les coefficients de Fourier de l'ISF, le gain du DCO. Le modèle de l'ADPLL est simulé pour les applications radio autour de 2.4GHz (ex :Bluetooth). La fréquence centrale du DCO est égale à 2.44GHz et il couvre la bande [2.4,2.49]GHz. La fréquence de la référence est égale à 13MHz. La longueur de la chaîne d'inverseur du TDC est égale à 14 et le temps de délai des inverseurs est égal à 30ps. Le modèle du bruit de phase du DCO est calculé à partir de la simulation transitoire où le signal de sortie est un signal continu déterminé à partir de l'équation 1.17. Ce signal est échantillonné et les instants de passage par zéro des fronts montants et des fronts descendants sont calculés par interpolation de premier ordre. La période moyenne est calculée comme montre l'équation suivante :

$$T_{out} = \frac{1}{N} \cdot \sum_{i=0}^{N} (t(i+1) - t(i)) \tag{1.26}$$

Le jitter périodique est obtenue à partir de l'équation :

$$e_j = t(i) - i \times T_{out} \tag{1.27}$$

L'erreur de phase est alors calculée à partir de la conversion temps en phase comme le montre l'équation suivante :

$$e_\phi = 2\pi \frac{e_j}{T_{out}} \tag{1.28}$$

La densité spectrale de puissance de e_Φ est calculée par la fonction *cspect* de Scilab avec 2^{19} points et le résultat est illustré dans la figure 1.12.

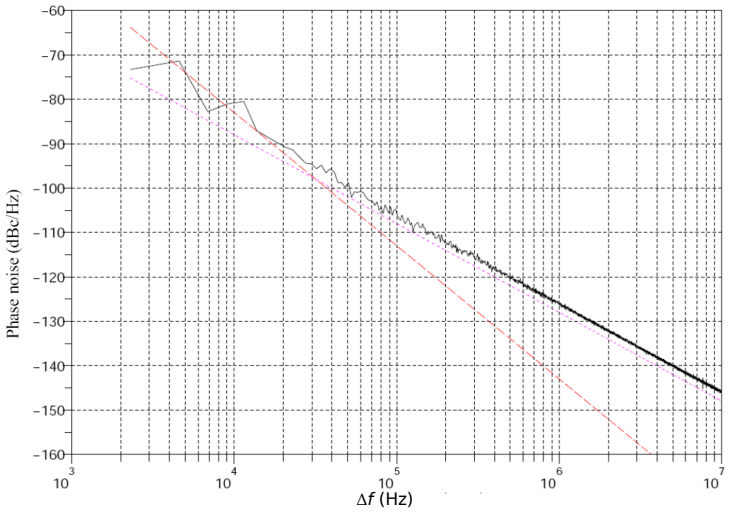

Fig. 1.12 – La densité spectrale de puissance du DCO. Le point ω_{1/f^3} est vu à 30kHz

1.6 Conclusion

Le bruit de phase constitue un obstacle dans la conception et la modélisation de l'ADPLL. Dans ce chapitre on propose un modèle comportemental de l'ADPLL avec le modèle LTV de bruit de phase de l'oscillateur. La fonction ISF décrit la réponse de l'oscillateur à une injection de bruit. Les coefficients de Fourier de l'ISF sont des paramètres génériques du modèle. En conséquent, pour un autre oscillateur seuls les coefficients de Fourier doivent être changés. Le bruit de quantification du TDC est aussi traité. Le modèle est portable pour une autre application et une autre technologie car il est générique. L'utilisation de VHDL-AMS ajoute une rapidité de la simulation en comparant avec les simulateurs électriques et donc une possibilité d'intégrer ce modèle dans un système plus complexe comme les récepteurs radio.

Chapitre 2

Conception de l'ADPLL pour les applications TV

Récemment, l'augmentation de l'intérêt de voir la télé dans un environnement mobile favorise la nécessité d'intégrer la bande TV sur un appareil portable. Les architectures classiques des oscillateurs locaux qui sont performants en terme de bruit de phase sont soit larges comme les circuits LC ou très consommateurs de puissance comme les oscillateurs en anneaux à base d'inverseurs. Ils sont donc inappropriés dans ce cas de figure. L'utilisation d'une ADPLL forme une alternative attractive pour ces exigences.

Dans ce chapitre on présente une conception de l'ADPLL conçue pour les applications TV. On considère que les contributions principales dans cette partie du travail sont la conception du DCO interpolateur et l'architecture fusionnée des DCO et TDC. Par contre, les autres blocs de la boucle sont détaillés dans le mémoire. Dans 2 on présente l'architecture de la boucle et les spécifications des applications TV. Puis, on présente l'architecture du DCO interpolateur à base de cellule NOR conçue pour un minimum de bruit de phase. Dans la section 1.3 on présente L'architecture du TDC fusionnée avec le DCO et son bruit de quantification.

Architecture de l'ADPLL L' architecture de l'ADPLL conçue pour les applications TV est illustrée dans la figure 2.1. La boucle contient un oscillateur en anneau contrôlé numériquement, un comparateur de phase numérique, un compteur numérique pour déterminer la phase variable du signal RF, un accumulateur du mot FCW pour déterminer la phase de la référence, un tableau de données où on trouve les mots numériques de contrôle, et le TDC. La boucle est divisée en deux parties. La première partie fonctionne à la fréquence de la référence comme le comparateur de phase. Cette partie est programmée sur un FPGA. La deuxième partie fonctionne à la fréquence radio comme l'oscillateur. Cette partie est réalisée en technologie CMOS 65nm.

Spécifications des applications TV Les spécifications des applications TV en terme de plage de fréquence couvre la bande VHF de 174 à 230 MHz et la bande UHF de 470 à 862MHz pour les applications DVB-T. Le bruit de phase est égal à -115dBc/Hz@5MHz de la porteuse et -128dBc/Hz@8MHz de la porteuse.

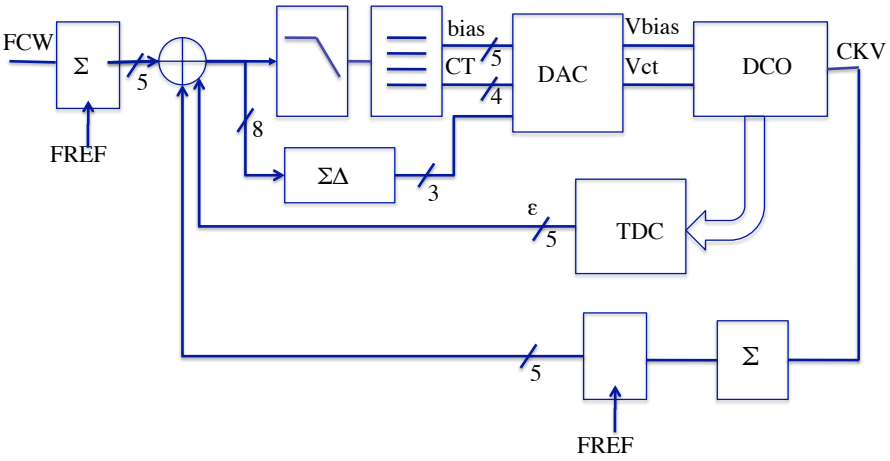

Fig. 2.1 – L'architecture proposée de l'ADPLL conçue pour les applications TV

2.1 Implémentation de l'ADPLL

La fréquence maximale à la sortie de l'oscillateur est égale à 800 MHz, la fréquence de la référence f_{ref} =26 MHz, et le mot de contrôle de fréquence FCW est définie par :

$$FCW = \frac{f_{max}}{f_{ref}} = 30.769 \tag{2.1}$$

Où f_{max} est la fréquence maximale à la sortie de l'oscillateur. La partie entière du mot

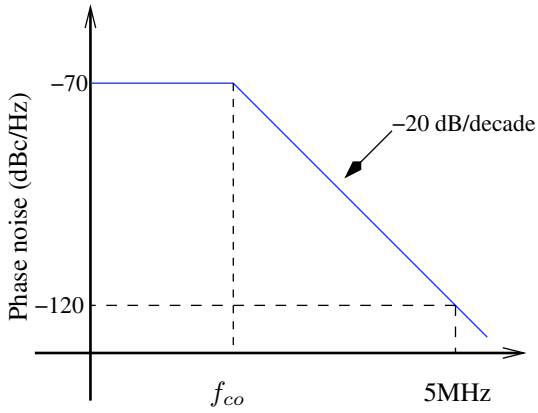

Fig. 2.2 – Le bruit de phase de l'ADPLL de premier ordre

de contrôle est dimensionnée à partir de la fréquence maximale atteinte par le DCO et la partie fractionnaire est dimensionnée pour atteindre une résolution égale à 100 kHz. Par conséquent, le nombre de bit de la partie entière de FCW est égal à 5 et le nombre de bit de la partie fractionnaire est égal à 8. La résolution est donnée par l'équation :

$$\delta f_{min} = \frac{800MHz}{2^5.2^8} = 97.656kHz \tag{2.2}$$

La boucle est de premier ordre et la bande passante est calculée à partir de l'équation :

$$f_{co} = \frac{\delta f_{min}}{2\pi} \tag{2.3}$$

La bande passante de la boucle est égale à 16kHz. Afin de pouvoir répondre aux spécifications des applications TV, le bruit de phase du DCO doit être inférieur à -120dBc/Hz@5MHz de la porteuse. En général, le bruit de phase a une pente -20dB/décade pour les fréquences supérieures à f_{co}, et le bruit a -70dBc/Hz@f_{co} de la porteuse, voir figure 2.2. Ce bruit résulte du bruit du DCO seulement, et le bruit du TDC est un bruit thermique, et il ne doit pas dépasser -70dBc/Hz.

2.2 Conception de l'oscillateur

L'oscillateur choisi est un oscillateur en anneaux interpolateur dont l'architecture est montrée dans la figure 2.3. Les raisons pour lesquelles ce choix a été pris sont détaillées dans le mémoire complet avec une comparaison synthétique entre l'architecture choisie et les oscillateurs en anneaux à cellules inverseuses. En résumé, ce type d'oscillateur permet

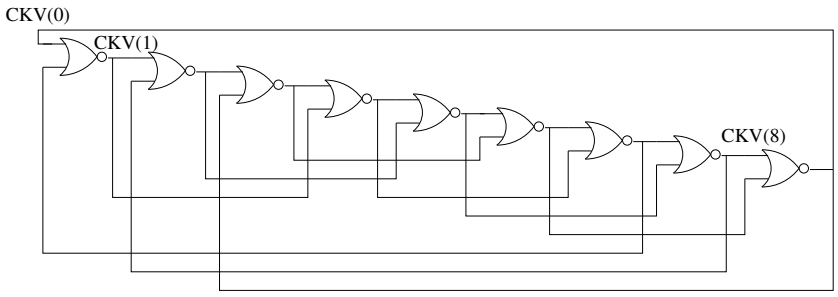

FIG. 2.3 – Un oscillateur interpolateur (9,7) en anneau à cellule NOR de deux ports

d'augmenter la plage de fréquences couverte par l'oscillateur et d'augmenter aussi sa fréquence centrale sans détériorer le bruit de phase. La cellule de base de l'anneau est une porte NOR à deux entrées. La cellule NOR est montrée dans la figure 2.4. C'est grâce à la tension CT qu'on peut régler l'interpolation de deux fréquences de deux anneaux, une fréquence qui résulte par le retard des portes du chemin direct et une deuxième fréquence qui est produit par la somme des signaux des anneaux plus courts, voir figure 2.3 et donc qu'on peut élargir sa plage de fréquence.

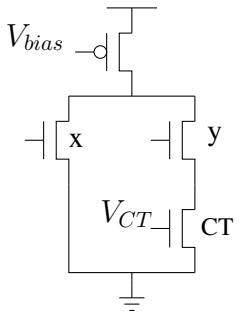

FIG. 2.4 – Une cellule NOR

En général, dans un oscillateur en anneau, la fréquence d'oscillation f_0 à la sortie du DCO est donnée par l'équation suivante :

$$f_0 = \frac{1}{2Nt_d} \tag{2.4}$$

Où N est le nombre d'étage de l'anneau et t_d est le temps de délai par étage.

Les éléments bruyants dans l' anneau sont les transistors PMOS et NMOS. Ils ont deux zones du bruit : en $1/f$, et du bruit blanc, avec un point d' intersection des deux zones appelé $\omega_{1/f}$. Afin de diminuer le bruit de phase de l'oscillateur on choisit le modèle Linéaire Variant en Temps du bruit de phase développé par Hajimiri [7]. Ce modèle est présenté dans le chapitre 1. Le dimensionnement de l'oscillateur est basé sur le modèle LTV et la fonction ISF de l'oscillateur comme présenté dans la section 2.2.1.

2.2.1 Stratégie du dimensionnement

Le dimensionnement des oscillateurs en anneaux est largement présenté dans la littérature [11, 12, 13]. Les concepteurs augmentent le rapport W/L des transistors pour minimiser la conversion du bruit en 1/f vers les hautes fréquences sans dépasser le budget de consommation de puissance. En plus, le bruit de phase de l'oscillateur ne dépend pas de nombre d'étages, et donc un grand nombre d'étages est généralement utilisé. Ce principe reste valide pour un minimum de bruit de phase due au bruit thermique [13, 9].

L'architecture de l'oscillateur interpolateur est constituée des port NOR, voir figure 2.3. Les variables de la conception sont les dimensions des transistors (W, L), ce qui fait huit dimensions par étage dans l'anneau. On utilise l'ISF pour évaluer la sensibilité de l'oscillateur à l'injection du bruit en deux étapes :

1. La variation de l'ISF en fonction de L pour une valeur fixe de W_p/W_n.
2. La variation de l'ISF en fonction de W_p/W_n pour une valeur fixe de L.

La détérmination de l'ISF est présenté dans la section 1.4.3.

La variation de l'ISF en fonction de L L'influence de la longueur L de la grille sur l'ISF est vue dans la figure 2.5. Dans cette figure L prend quatre valeurs (65nm, 120nm, 130nm, 250nm) et le rapport W/L est constant pour la même fréquence[1]. L'oscillateur est conçu en CMOS 65nm et l'ISF est déterminée automatiquement en utilisant Scilab et Spectre comme on décrit dans la deuxième partie du mémoire. Les résultats de simulation sont illustrés dans la figure 2.5 et on constate que la valeur RMS de l'ISF et donc le bruit de phase diminuent en augmentant L.

La variation de l'ISF en fonction de W_p/W_n La symétrie du signal oscillant (temps de montée et temps de descente) est un indice d'amélioration du bruit de phase,[14]. Cette propriété dépend du rapport W_p/W_n. On détermine le rapport W_p/W_n qui diminue l'ISF et améliore le bruit de phase. Dans la figure 2.6 on montre la fonction ISF pour l'oscillateur interpolateur pour un rapport $W_p/W_n = 1, 2, 3$ et $W_n = L = 250nm$. On remarque que la valeur de l'ISF est diminuée pour un rapport égal à trois. Pour $W_p/W_n > 3$ la puissance consommée augmente sans améliorer le bruit de phase de façon significative.

Finalement, les dimensions des transistors sont montrés dans le tableau 2.1. Wp est la largeur du transistor PMOS et Wx,Wy,Wct sont les largeurs des transistors X, Y, CT respectivement. L est la longueur de tous les transistors. L'analyse Pnoise de l'oscillateur montre le bruit de phase de l'oscillateur à une fréquence de porteuse égale à 462MHz dans

[1] Les résultats de simulation de la figure 2.5 ont été effectués pour la fréquence 2GHz. Ces résultats sont portables pour d'autre bande de fréquences. Pour les applications autour de 500MHz, Ces résultats sont rafinés avec Spectre(Pnoise et Trans) afin de couvrir les spécifications des applications TV.

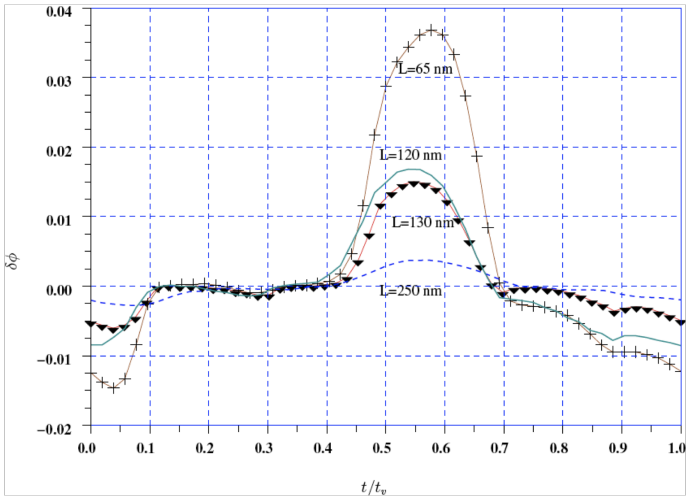

FIG. 2.5 – La fonction ISF de l'oscillateur interpolateur pour L= (65nm,120nm,130nm,250nm)

la figure 2.7. Le bruit de phase est égal à -120dBc/Hz@5MHz. La puissance consommée est 1.6mA -1.2V et la plage de fréquence est de 400MHz à 800MHz.

Wp (μm)	Wx (μm)	Wy (μm)	Wct (μm)	L (μm)
15	5	2.5	2.5	0.5

TAB. 2.1 – Les dimensions de la cellule NOR pour minimizer le bruit de phase

2.3 Le TDC

Le TDC est utilisé pour calculer le retard ε entre un front montant du signal oscillant CKV et le front montant de la référence FREF, voir fig.2.8, dans une boucle à verrouillage de phase numérique ADPLL, comme le montre l'équation suivante :

$$\varepsilon = \phi_{FREF} - \phi_{CKV} \tag{2.5}$$

où ϕ_{FREF} et ϕ_{CKV} sont les instants des fronts montants de FREF et de CKV respectivement. L'oscillateur de la boucle est un oscillateur en anneau montré dans la figure 2.3 . Il contient neufs étages dont le retard de chaque étage est appelé t_d et dont les signaux d'entrées-sorties sont appelés S(0),S(1),...,S(8).

Le principe de fonctionnement du TDC est de relever l'état de l'anneau et de le stocker dans un registre en utilisant des bascules synchronisées aux fronts montants de FREF comme montre la figure 2.8. Puis, la valeur dans le registre va être codée selon le tableau 2.2 pour déterminer ε.

Un état de l'anneau est défini donc sur neuf bits et cela est équivalent à dire que la période $T_{CKV}/2 = 9t_d$. Il s'agit de 18 états différents comme le montre le tableau 2.2. A partir de chaque état on peut déterminer la position du front qui se propage sur la chaîne à l'arrivée d'un front montant de FREF. Quand un front montant ou descendant se propage sur la chaîne, le signal S(0) est égal à '1' ou à '0' respectivement, et la valeur de ε varie de $9t_d$ à $17t_d$ ou de 0 à $8t_d$ respectivement selon la position des fronts.

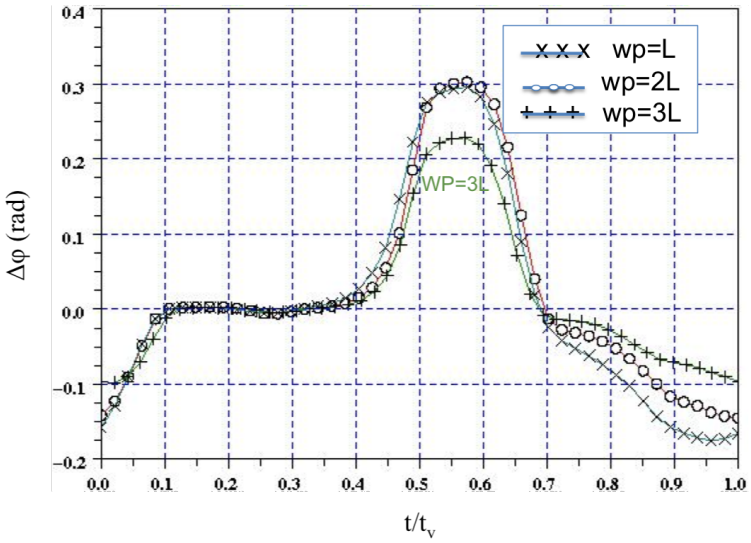

Fig. 2.6 – La fonction ISF de l'oscillateur interpolateur

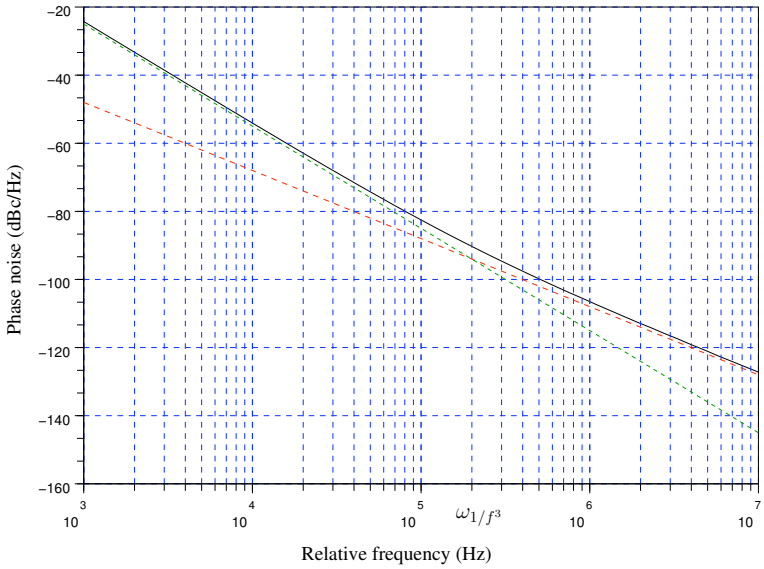

Fig. 2.7 – Les résultats de la simulation Pnoise du DCO

2.4 Conclusion

Une conception de l'ADPLL pour les applications TV a été présentée. Le DCO de la boucle est un oscillateur en anneau interpolateur a base des cellules NOR de neuf étages. Cette architecture est choisie pour sa plage de fréquence qui est plus large que celle des architectures classiques des oscillateurs en anneaux à base des cellules inverseuses. Une comparaison en simulation a été effectuée afin de choisir la bonne architecture du DCO et une stratégie de dimensionnement dépendant de l'ISF a été implémentée. Ceci permet d'optimiser le bruit de phase et la consommation de l'oscillateur. Une architecture fusionnée du DCO et du TDC est conçue afin de réduire la surface et la consommation du circuit.

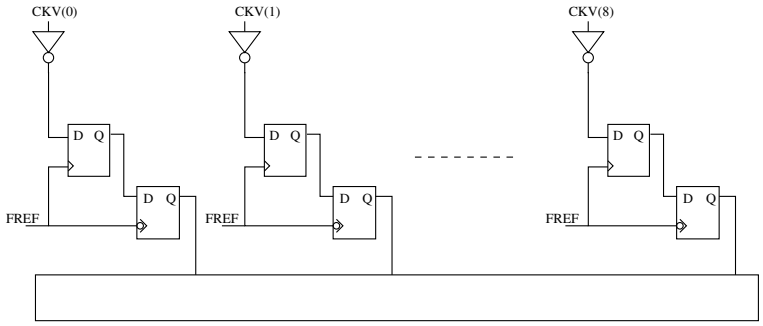

FIG. 2.8 – Le schéma bloc du TDC

[0]	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	ε
0	1	0	1	0	1	0	1	0	0
0	1	0	1	0	1	0	1	1	1
0	1	0	1	0	1	0	0	1	2
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	1	0	1	0	1	1	0	11
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	1	1	0	1	0	1	0	15
1	0	0	1	0	1	0	1	0	16
1	1	0	1	0	1	0	1	0	17

TAB. 2.2 – Les 18 états de l'anneau et la valeur de ε correspondante

Les résultats de simulation du DCO montre un niveau de bruit de phase égale à -120dBc/Hz@5MHz de la porteuse pour une fréquence de 450MHz. Le bruit du TDC est uniformément distribué de densité spectrale égale à -94DBc/Hz. La partie de la boucle qui fonctionne à la fréquence de la porteuse est programmée sur un FPGA et la partie RF comme le DCO et le TDC est réalisé sur un circuit intégré en technologie CMOS 65nm. Les résultats de mesure de la boucle sont présentés dans le chapitre suivant.

Chapitre 3

Résultats de mesure

L'ADPLL est conçue pour les applications TV pour un minimum de bruit de phase. Dans ce chapitre on présente les résultats de mesure de la boucle ouverte. On montre les performances du DCO et du TDC. Les tests de la boucle fermée n'ont pas été effectués par manque de temps.

3.1 La carte de test de la boucle ouverte

Un schéma bloc de la carte de test est illustré dans la figure 3.1. Le circuit est placé dans le centre de la carte et les signaux de contrôle sont connectés aux interupteurs et le signal de sortie du DCO est connecté à l'analyseur de spectre afin de mesurer le bruit de phase Le circuit complet consomme 7mA-1.2V.

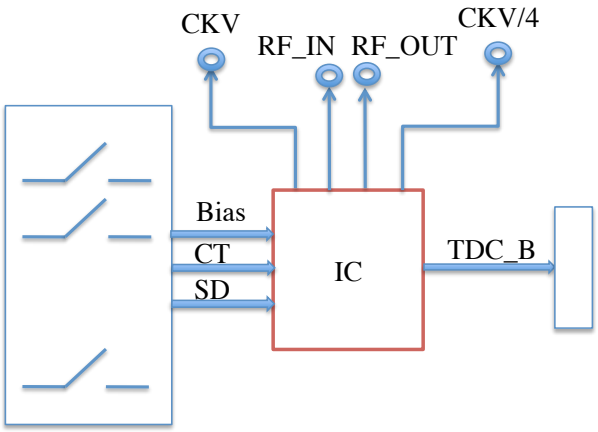

FIG. 3.1 – Schéma bloc de la carte de test de la boucle ouverte

3.2 Les performances du DCO

Dans cette section on présente les performances du DCO en termes d'amplitude du signal, de plage de fréquence, de consommation de puissance et de bruit de phase. On compare les résultats obtenus par simulation avec les résultats mesurés. On présente aussi une comparaison en terme de facteur de mérite avec autre architecture présentée dans l'état de l'art.

Les caractéristique du DCO Les bits de contrôle CT et Bias sont commutés pour avoir la plus basse fréquence (CT=15, Bias=1). Le signal CKV est connecté à l'oscilloscope TDS754D et le signal vu est illustré dans la figure 3.2. Où on voit que l'amplitude de CKV

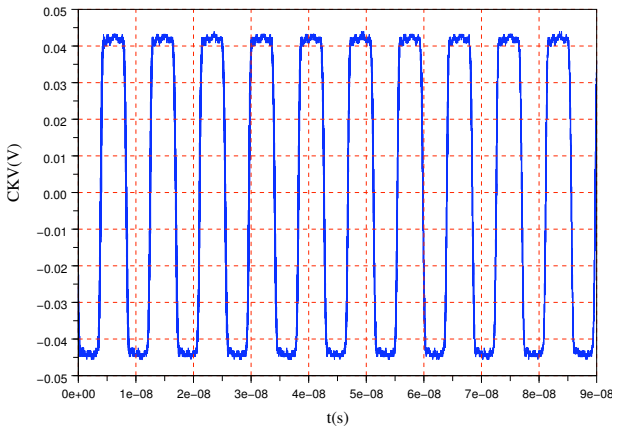

Fig. 3.2 – Le signal CKV mesuré pour (CT=15, Bias=1)

est égale à 94 mV P-P et la fréquence est égale à 122 MHz. La simulation montre que cette amplitude est égale à 400mV P-P en utilisant une résistance pull-up égale à 100Ω. On utilise 475Ω dans la carte de mesure.

La fréquence maximale obtenue est égale à 470MHz (CT=1,Bias=31). Dans la figure 3.3

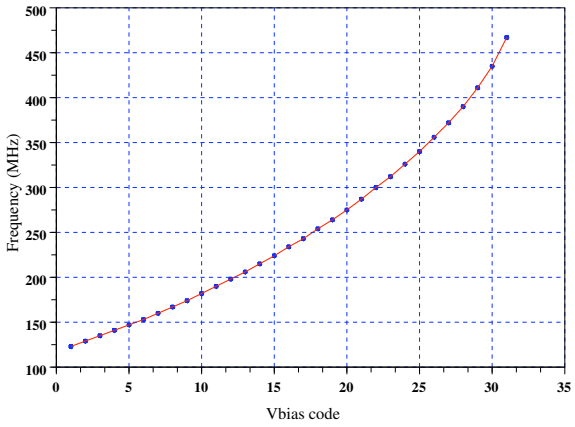

Fig. 3.3 – La plage de fréquences couverte par le DCO en fonction du mot bias pour CT=1

on voit la variation de la fréquence de CKV en fonction de Bias code. La plage de fréquence obtenue est de 122MHz à 470MHz et il est diffèrent de celui obtenu par simulation (400MHz à 800MHz).

Le bruit de phase de CKV dans la boucle ouverte est mesuré pour toute la plage de 100kHz à 10MHz de la porteuse. La fréquence de la porteuse est égale à 470MHz et le bruit de phase mesuré est illustré dans la figure 3.4. Il atteint -117dBc/Hz à 5MHz. Cette valeur est 3dB plus grand que celle obtenue par simulation.

Dans le tableau 3.1, on compare les résultats de simulation avec les résultats de mesure. L'amplitude et la consommation de puissance sont validés mais la plage de fréquence est

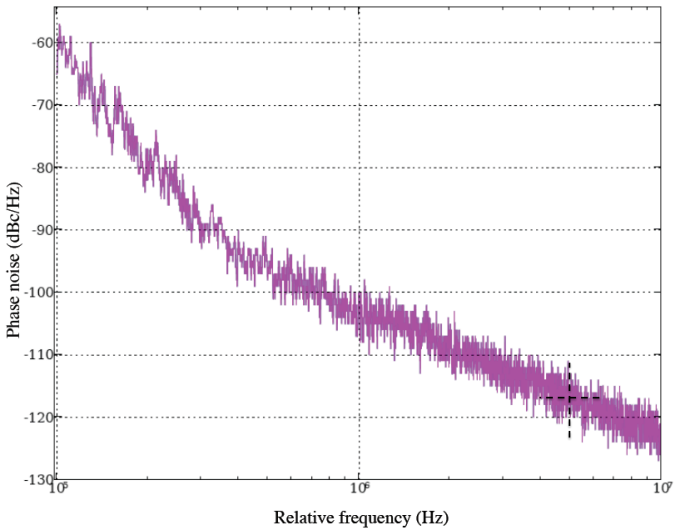

FIG. 3.4 – Le bruit de phase mesuré de CKV f_{CKV}=470MHz

différente que celle obtenue en simulation. Cette déviation peut être due aux tensions de

TAB. 3.1 – Tableau de comparaison entre les résultats de simulation et les résultats de mesure

DCO	Phase noise	Power consumption	Tuning range	Amplitude
Simulation	-120dBc/Hz	1mA	400MHz - 800MHz	94mV
Measurements	-117dBc/Hz	$<$1mA	122MHz - 470MHz	110mV

controle (V_{bias} and V_{CT}) qui insuffisantes pour générer la bonne fréquence.

Facteur de mérit du DCO Une définition de facteur de merite est proposée dans [15] :

$$FM = 10\log\left(\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{@\Delta f\}P}\right) \tag{3.1}$$

Où P est la puissance consommée de l'oscillateur seul (sans le buffer de sortie).

Selon l'équation 3.1, le FOM du DCO est égale à 160.

Le tableau 3.2 contient une comparaison entre le DCO conçu avec d'autre oscillateurs en anneau en terme de facteur de mérite.

Pour la même plage de fréquence, Le DCO proposé est amélioré en terme de bruit de phase et de consommation de puissance.

3.3 Les performances du TDC

Les bits du registre du TDC définissent l'état du DCO et il sont nommés TDC(0),TDC(1),...,TDC(8). En pratique, en absence de métastabilité, on a 18 états équiprobables de l'anneau. On teste l'absence d'états interdits et l'équiprobabilité des états dans la figure 3.5. Dans cette figure on illustre un histogramme des états du DCO pour FREF=25MHz sur 8000 échantillons.

Tab. 3.2 – Comparaison entre les performances du DCO interpolateur et d'autres architectures présentées dans l'état de l'art

Ref.	TR (GHz)	$L(\Delta f)(dBc/Hz)$	Δf (MHz)	FOM	Power(mW)	Tech
[16]-2002	9.8-11.5	-98	2	153	75	0.5μm
[17]-2003	0.1-3.5	-106	4	152	16	0.18μm
[18]-2004	3.1-6.3	-101.4	1	155	157	0.18μm
[19]-2009	1.7-5.5	-120.2	4	162	81	0.18μm
This DCO	**0.1-0.5**	**-120**	**5**	**160**	**1.2**	**65nm**

Dedans on observe l'absence des états interdits mais les états ne sont pas équiprobables. Ceci peut être due à deux raisons : premièrement, le TDC contient des buffers à la sortie de chaque étage du DCO pour déterminer l'état high/low de l'étage et chaque buffer a un seuil diffèrent. Deuxièmement, la dispersion statistique de temps de délai des portes NOR.

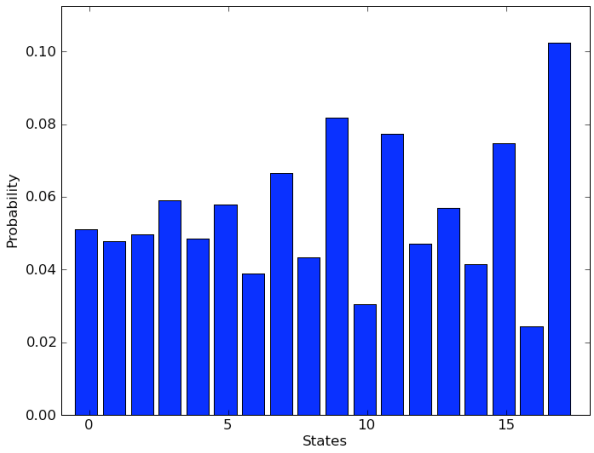

Fig. 3.5 – Histogram d'état de l'anneau. Le nombre des échantillons est égale à 8000

3.4 Conclusion

Ce chapitre contient les résultats de mesure du DCO et du TDC. D'autres mesures sur le DCO ont été effectuées et sont présentées dans le mémoire complet. La boucle est conçue pour les applications TV de 400MHz à 800MHz. Le DCO couvre une plage de fréquence de 100MHz à 500MHz. Il consomme 1.2mW comme prévue en simulation. Le bruit de phase du DCO est égal à -117dBc/Hz@5MHz de la porteuse qui a 400MHz de fréquence. Les résultats de mesure du DCO sont compatibles avec les simulations sauf la plage de fréquence. Ceci peut être due à une valeur insuffisante des tensions de contrôle V_{CT} et V_{bias}.

Ce travail est le premier pas dans la conception des ADPLL pour les applications TV.

Comme travail de future on propose de tester les performances de la boucle fermée pour valider les performances de la boucle en terme de bruit de phase et de consommation de puissance. On propose aussi d'améliorer les DAC qui génèrent les tensions de contrôle de DCO au niveau architecture et dimensionnement. On propose aussi d'implémenter un modulateur $\Sigma\Delta$ pour améliorer la résolution de la boucle.

Finalement, une implémentation de la boucle complète sur un circuit intégré est intéressante à cause de la surface réduite de la conception.

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By

Wissam ALTABBAN

Portable Design of ADPLL for TV Applications

Defended on December 4, 2009

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Abstract

Local Oscillators are key buildings in radio communication system. They are considered as intensively analog blocks and then more sensitive to internal noise than digital blocks. This noise is up-converted to phase noise around the carrier frequency at the output of the oscillator. High performance of LO in terms of low phase noise is paid by high surface circuit or by high power consumption. One solution, proposed in the literature, is the All Digital Phase Locked Loops ADPLL. Within, digital blocks replace the analog blocks, such as the phase comparator and the loop filter. In addition, the oscillator of the ADPLL is a digitally controlled oscillator (DCO), and a Time to Digital Converter (TDC) is used to determine the time difference between the rising edges of the reference signal and the oscillator signal. This solution reduces the circuit area, but the used DCO is LC based oscillator, which occupies a large surface whatever the technology is. As for TDC, many architectures are proposed in the literature, and they suffer from limited resolution, design complexity, and power consumption.

In this thesis, down to top behavior model of ADPLL is developed using VHDL-AMS. This model includes oscillator phase noise and TDC quantification noise. The modeling of the DCO is based on the Linear Time Variant LTV model of phase noise that is based on the Impulse Sensitivity Function ISF of the oscillator. We are interested in this work by the design and modeling of the DCO and of the TDC because of their noisy behavior. For the DCO, LC oscillators are generally opted for their low phase noise and low power consumption performances compared to ring oscillators. However, they have low tuning range, they are not scalable with technology progress, and they occupy very large area in the communication system. For these reasons, we are interested in this work in the design of digital controlled ring oscillator. We opt for nine-stage ring interpolative oscillator made by NOR cells for its larger tuning range than inverter based ring oscillators. It contains nine NOR main gates that interpolate in phase with seven NOR gates. Two voltages that are digitally controlled weight this interpolation to produce a wider tuning range with low jitter and low power consumption. We propose an ISF based design strategy that can optimize the design variables of ring oscillators for minimum phase noise. In order to minimize the circuit area and the power consumption, we propose to merge DCO and TDC architectures. TDC uses the ring status to determinate the position of the rising or the falling edge of the oscillator waveform that is propagating in the ring at the rising edge of the reference. The resolution of this TDC is equal to 1/18 of the oscillation period and it has very low power consumption and a small surface compared to other TDC architectures. The ADPLL circuit is divided into two parts: High frequency operation part (DCO, TDC)

that is designed and fabricated in 65nm CMOS process, and low frequency operation part (phase comparator) that are programmed on FPGA.

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Introduction

Motivation and aim of research

Local Oscillators are key building blocks in radio communication system. They are considered as intensively analog blocks and then more sensitive to internal noise than digital blocks. This noise is up-converted to phase noise around the carrier frequency at the output of the oscillator. High performance of LO in terms of low phase noise is paid by high surface circuit or by high power consumption. One solution, proposed in the literature, is the All Digital Phase Locked Loops ADPLL. Within, digital blocks replace the analog blocks, such as the phase comparator and the loop filter. In addition, the oscillator of the ADPLL is a digitally controlled oscillator (DCO), and a Time to Digital Converter (TDC) is used to determine the time difference between the rising edges of the reference signal and the oscillator signal. This solution reduces the circuit area, but the used DCO is LC based oscillator, which occupies a large surface whatever the technology. As for TDC, many design are proposed in the literature, and they suffer from limited resolution, design complexity, and power consumption. In addition to its low surface compared to classic PLL, ADPLL contains digital blocks that are scalable with technology progress. The advantage of scalability is the short time of design of future generations in future technologies. But the design and optimization of an ADPLL in order to obtain a pure signal with low power and low area remains a significant challenge. Two main noise sources exist in the ADPLL, the DCO and the TDC. In spite of the digital control of the oscillator, it is analog core block. It is designed and optimized generally using electrical simulators like Spectre. Besides the mathematical models of oscillator basic elements (transistors, capacitors, inductors and resistors), these simulators contain analysis of circuit behavior in respect to variations of time and frequency. In addition, it contains predictive models of noise, phase noise that are powerful in case of relatively small circuits such as a DCO. For more complicated systems such as ADPLL, these tools are no more helpful since simulation time explodes with the complexity of the design. In this case, other modeling types are needed.

In this thesis we are interested by the performance of ADPLL in terms of phase noise. We propose to model ADPLL using the Impulse Sensitivity Function (ISF) of the oscillator. This function describes carefully the sensitivity of an oscillator to any impulse current injection in any node of the circuit. The TDC noise is due to quantification error and it is modeled as well. The resulting model predicts rigorously the ADPLL behavior in the presence of DCO and TDC noise. This model is programmed in VHDL-AMS for its

compatibility with the digital, analog and mixed blocks in the ADPLL. In addition, we present a z-domain model of the ADPLL. In which, we present the influence of the closed loop transfer function on the TDC and DCO noises. This model is descriptive and it could be used in system more complex such as radio receivers.

We propose also a design strategy of DCO ring oscillator using the ISF. We opt for nine-stage ring interpolative oscillator made by NOR cells for its larger tuning range than inverter based ring oscillators. It contains nine NOR main gates that interpolate in phase with seven NOR gates. Two voltages that are digitally controlled weight this interpolation to produce a wider tuning range with low jitter and low power consumption. We propose an ISF based design strategy that could optimize the design variables of ring oscillators for minimum phase noise. In order to minimize the circuit area and the power consumption, we propose merged DCO and TDC architecture. It uses the ring status to determinate the position of the rising or the falling edge of the oscillator waveform that is propagating in the ring at the rising edge of the reference. The resolution of this TDC is equal to 1/18 of the oscillation period and it has very low power consumption and a small surface compared to other TDC architectures. The ADPLL circuit is divided into two parts: High frequency operation part (DCO, TDC) that is designed and fabricated in 65nm CMOS process, and low frequency operation part (phase comparator) that is programmed on FPGA.

Organization of the thesis

The thesis is organized as follows. The first chapter contains a historical review on PLL, starting from analog PLL to finally arriving to ADPLL, the architectures are progressively modified. We review also a state of the art of the two main noisy elements in ADPLL, the DCO and the TDC. Two principal models of oscillator phase noise, Linear Time Invariant and Linear Time Variant, are also presented in this chapter. Next, in chapter 2 we develop our ADPLL model based on the LTV model of phase noise. In chapter 3 we present our design of ADPLL for TV applications. Within, a design strategy for minimum phase noise based on the LTV model is also presented. Then, in chapter 4 we present a comparison between simulation and measurement results.

Major contribution

- An implementation of LTV model of DCO phase noise in ADPLL behavior model using VHDL-AMS
- A design strategy of digital controlled ring interpolative oscillator bases on the ISF
- Merged DCO and TDC architecture for low power, low surface applications.

Chapter 1

Analog and Digital PLL review

1.1 Historical review on frequency synthesis

Frequency synthesizers are used to generate periodic signals whose frequencies are equal to multiple of the frequency of reference signal. Historically, the earliest description of what is now known as a Phase Locked Loop (PLL) is proposed by H. de Bellescize in 1932[1],[11]. He proposed a Local Oscillator (LO) whose frequency is precisely the same of the incoming carrier and whose phase is locked to that of the carrier in *direct-conversion* receiver. First PLLs were not intensively used because of the high cost of complete circuit. Then, from 1970s with the advancement of IC technology, the PLL becomes one of the indispensable elements of any communication system. In the first generation of PLL, the output frequency is equal to integer multiple of the reference frequency, then, fractional PLLs that generate radio signals of frequencies equal to fractional multiple of reference frequency are used. The major difference between the two architectures is the frequency resolution. In integer PLL, the frequency resolution is equal to the reference frequency, which is selected generally to be the same as the channel spacing. Whereas, in fractional PLL, the output frequency can be incremented by a fractional part of reference frequency. This allows high reference frequency, then, an improved loop dynamic and attenuation of the oscillator noise, [12]. Details on integer and fractional PLL are viewed in section 1.2. For the reference oscillator, a crystal oscillator is generally used because of its accurate and stable frequency signal. The other blocks of classical PLL can be viewed in figure 1.1: the Phase Detector (PD), the Voltage Controlled Oscillator (VCO), and the Low Pass Filter (LPF). The phase detector compares the reference phase with the phase of the VCO and it generates a signal error that will be filtered by the low pass filter. The output voltage of the filter controls the VCO that generates a signal with a frequency corresponding to the input voltage. The closed loop form the named LO. Figure 1.1 shows a general block diagram of integer frequency synthesizer. In the first frequency synthesizers, all the PLL blocks were analog. Then, with technology progress, logic and digital blocks are used in PLL, like the phase detector block [13], these are named Digital Phase Locked Loops DPLL. Recently, an All Digital Phase Locked Loop ADPLL is presented by [14] for wireless

[1] "La réception Synchrone,"L'onde Electrique,v.11,June 1932,pp.230-40

applications. Within, all inter-blocks signals are digital and the oscillator of the loop is digitally controlled.

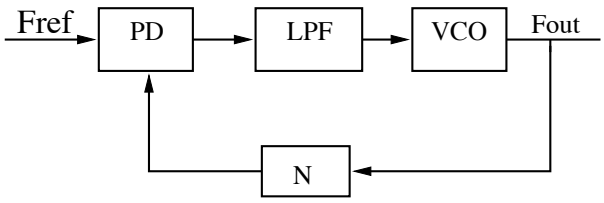


Figure 1.1: Integer frequency synthesizer

In the PLL, the PD can be divided into three categories: analog phase detectors such as the mixer [15], digital phase detectors based on logic gates [16] that are generally named phase/frequency detectors in Digital PLL (DPLL), and digital phase detectors with a Time to Digital Converter (TDC) are used in the ADPLL [14]. The loop filter is an analog device element in the PLL and a digital one in the ADPLL. The VCO is replaced by the Digital Controlled Oscillator (DCO) in the ADPLL. Since the oscillator is the most noisy element in the loop, we present afterwards the main architectures of VCO in section 1.4 and some DCO architectures in section 1.10.

In spite of its different architecture, ADPLL has the same trade-off than analog PLL. In order to understand the trade-off between noise and loop bandwidth we present a first order linear model of first order of PLL in section 1.3.

1.2 Integer and fractional PLL

Integer PLLs are used to generate an output frequency that is an integer multiple of the reference frequency. Within, the frequency resolution is equal to the reference frequency, which is selected generally to be the same as the channel spacing. Whereas, in fractional PLL, the output frequency can be incremented by a fractional part of reference frequency. This allows high reference frequency, then, an improved loop dynamic and attenuation of the oscillator noise.

Fractional PLL can be realized using static or dither moduli. In static moduli, the reference frequency is divided by an integer N and the output frequency is divided by another integer M. Thus, the generated output frequency Fout is related to Fref by the following equation:

$$Fout = \frac{M}{N}\, Fref \tag{1.1}$$

In this case, Fref/N is considered as the frequency resolution and the phase detector output is updated at this rate. Because of the need to suppress the control voltage ripple, the PLL bandwidth is smaller than Fref/N. However, to obtain the maximum benefit from the low noise reference, the PLL have to track that reference over a wide bandwidth as possible. Additionally, wider loop bandwidth would speed the settling time. These conflict requires

other architectures for fractional PLL. One of these architectures is obtained by dividing the output frequency by another integer P as the following equation

$$Fout = \frac{M}{NP}\, Fref \tag{1.2}$$

In this PLL, updating of the phase comparator is done at the same rate of the previous architecture, but the resolution is equal to Fref/NP. Another type of fractional PLL that is widely used employs the dual modulus prescaler. Wherein, the average fractional value is obtained by switching between two integer division ratios. It is used in order to increase the resolution of output signal whatever the reference frequency is high without deteriorating the phase noise performance [15]. The fractional synthesizer uses a digital accumulator producing a sequence of K cycle at its carry output. This signal controls a $(N+1)/N$ divider to divide by $N+1$ during K and by N during $(2^k - K)$ cycle. The average division number is then given by the equation

$$N_{frac} = \frac{(2^k - K).N + K.(N+1)}{2^k} = N + \frac{K}{2^k} \tag{1.3}$$

The spectrum of the output signal contains spurious signals resulting from the periodical $(N, N+1)$ switching. A $\Sigma\Delta$ modulator replaces the accumulator and its flux of bits control the divider. Noise shaping of the modulator provides the elimination of low frequency quantification noise and the rest of the noise is eliminated by the filtering behavior of the loop. It was the excellent choice of full integration of CMOS frequency synthesizer [11, 15] until the arrival of CMOS ADPLL of [17].

1.3 First order PLL

The first order PLL is the one in which the loop filter has a zero order. Then, it is simply a scalar with units of volts per radian. Besides of its simplicity compared to PLL of second order and more, its main attribute is the obtained large phase margins. However, bandwidth and steady-state phase error are strongly coupled in this type of loop. To evaluate quantitatively the limitations of this loop we study a linear model of first order loop of the figure 1.2.

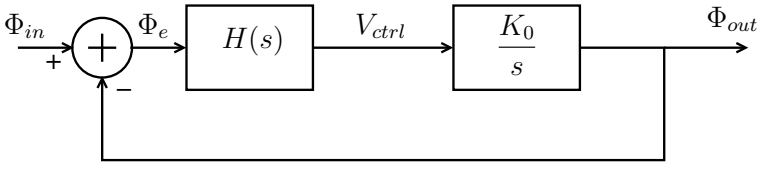


Figure 1.2: First order PLL

The input and the output of the model are respectively the phases Φ_{in} and Φ_{out} . The loop filter attenuation is equal to 1, the phase comparator gain is named K_d, the VCO output frequency depends on the control voltage V_{ctrl}. The VCO gain is named K_0 and

it is expressed in radian/second/volts. Since the VCO is an integrator, then its transfer function is equal to $\frac{K_0}{s}$. The input-output phase transfer function is given by the equation

$$\frac{\Phi_{out}}{\Phi_{in}} = \frac{K_0 K_d}{s + K_0 K_d} \tag{1.4}$$

The closed loop bandwidth ω_h is therefore

$$\omega_h = K_0 K_d \tag{1.5}$$

To verify the relation between the phase error Φ_e and the loop bandwidth, let us consider the phase error-input transfer function that is expressed in the equation:

$$\frac{\Phi_e(s)}{\Phi_{in}(s)} = \frac{s}{s + K_0 K_d} \tag{1.6}$$

The input frequency is, in general, a sinusoidal signal of fixed frequency ω_i, then, the Laplace representation of the input signal is [11]:

$$\Phi_{in}(s) = \frac{\omega_i}{s^2} \tag{1.7}$$

so that

$$\Phi_e(s) = \frac{\omega_i}{s(s + K_0 K_d)} \tag{1.8}$$

The steady-state error is therefore

$$\lim_{s \to 0} s\Phi_e(s) = \frac{\omega_i}{K_0 K_d} = \frac{\omega_i}{\omega_h} \tag{1.9}$$

Then, the steady-state phase error is the ratio of the input frequency to the loop bandwidth. Therefore, a small steady-state phase error requires a large loop bandwidth. To decouple the steady-state error from the loop bandwidth we can use a LPF of first order and we obtain a second order PLL.

1.4 Voltage Controlled Oscillators

Oscillators are an integral part of many electronic systems. Applications range from clock generation in microprocessors to frequency synthesis in wireless communication system and require different oscillator topology and performance parameters. Robust, small, low power, oscillator design in CMOS technology continues to make challenges. The VCO is characterized by its surface, power consumption, tuning range, resolution, and phase noise. Many architectures are presented in the literature, the most stable one is the crystal oscillator. This oscillator has some tens of MHz frequency, and it is used as a reference in the PLL. Two other fundamental types of oscillators are generally used in PLLs, LC and ring oscillators.

Design recommendations differ from application to another. For example, GSM and UMTS recommendations on phase noise are not the same as Bluetooth or TV application.

LC oscillator is generally opted in high frequency applications [18, 19, 20, 21, 22, 23] for its relatively good phase noise performance compared to ring oscillators. Whereas, ring oscillators are used in wide tuning range applications [24, 25, 26]. Single ended or differential VCO, the two architectures offer the flexibility to obtain one output signal or two signals in quadrature for any communication system needs.

1.4.1 LC oscillators

A general block of cross coupled LC oscillator is viewed in figure 1.3. Wherein, the cross-coupled transistors form a positive feedback loop to provide negative resistances to cancel the LC-tank loss that sustains the oscillation. Generally, the greater the oscillator core bias current is used, the better phase noise performance is obtained. For the CMOS technology,

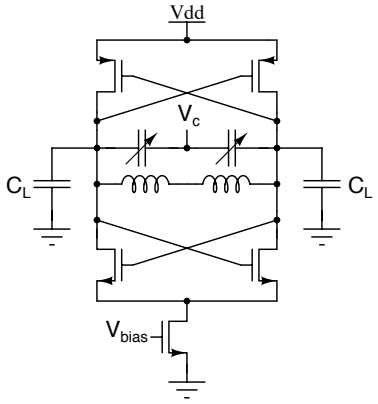


Figure 1.3: A cross coupled LC oscillator

noise factor depends on the bias current. In addition, compared to a PMOS transistor, an NMOS transistor could have a lower noise at one bias condition while having a higher noise at another bias condition. Thus, the complementary cross-coupled structure is used to average the 1/f noise contribution between NMOS and PMOS transistors at different bias conditions. Moreover, the complementary structure has the advantage of producing more transconductance g_m with the same amount of current, thus reducing the overall power consumption, [27].

The output frequency f_0 of the oscillator is related to the LC resonator as can be viewed in the equation 1.10.

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{1.10}$$

Where L and C are the inductor and varactor values. In the LC VCO, the value of L is fixe while the value of C is modified in responding to the input control voltage. This response depends on the technology of fabrication (MIM, MOS, junction-diod varactor,...,etc) and affects directly, by its quality factor and C_{max}/C_{min} ratio, the VCO gain. The quality factor Q of any circuit is generally defined by the ratio of the stored energy to the dissipated

energy, and for an ideal LC oscillator is can be written as [28]:

$$Q = \frac{R}{\omega_0 L} \tag{1.11}$$

Where R is the tank resistor, L is the inductor value, ω_0 is the carrier pulsation. This relation expresses the explicit dependence of Q on R and L. The value of Q affects directly the phase noise performance of an LC oscillator, as can be viewed in the following equation [29]

$$L\{\Delta\omega\} = 10.log\left[\frac{2FkT}{P_{sig}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{1.12}$$

where L is the power spectral density of the phase noise at the oscillator output, $\Delta\omega = 2\pi.\Delta f$ is the offset from the carrier frequency, F is the noise factor, k is the Boltzmann constant, T is the temperature, Q is the quality factor of the LC oscillator and $\Delta\omega_{1/f^3}$ is the frequency of intersection between the two regions $1/f^3$ and $1/f^2$ of phase noise, see section 1.6. From equation 1.12 we can see that for higher Q values, better phase noise performance is obtained.

Design strategy of LC oscillator to enhance its phase noise performance is largely developed in the literature [18, 19, 21, 30, 31, 32]. In the annex A a method of design strategy based on the noise to signal ratio presented in [18] is opted for the LC oscillator used in our model of DCO. Square, circular, hexagonal, filled, hollow,..., whatever the form is, inductors are generally very large compared to ring oscillators area. The limitation of the use of LC oscillators is their surface, then cost. Since the necessary inductor value for an output frequency is the same whatever the technology of fabrication, LC oscillators are not scalable with technology progress.

In section 1.10 we present the method presented in the literature to control the LC oscillator frequency digitally.

1.4.2 Ring oscillators

Due to their speed and ease of integration, ring oscillators are increasingly being used as VCO in jitter sensitive applications. Applications benefit from the cost and size advantages of fully integrated oscillators, like clock recovery PLL [33, 34], clock frequency multiplication [35, 36], and oversampling analog-to-digital converter [37]. The design complexity of ring oscillator depends on the design of one stage of the ring and of total ring. Performances of ring VCO in terms of phase noise is not so easy to be predicted since most of phase noise prediction models [29, 38, 39] are expressed in function of the quality factor of the oscillator as we see in section 1.6. Then, in ring oscillators, jitter is generally determined to predict the noise contribution on the oscillation period.

In case of ring oscillators, phase noise is expressed in function of cycle jitter as we see in the following equation [24].

$$S_\Phi = \frac{f_0^3 \Delta T_c^2}{(f-f_0)^2} \tag{1.13}$$

where f_0 is the carrier frequency and ΔT_c is the cycle jitter and it is defined in section 1.7.

Design of ring oscillator has two main steps: the first one is the number of stages in the ring and the second one is the design of one stage of the ring. The tuning range of simple architectures such as single ended inverter based ring is equal to 50%, while it could reach 74% for other architectures [40, 10]. Oscillation period T_0 is related to stages number N

Figure 1.4: Ring oscillator based on inverter gates

and to delay time t_d of each stage as can be seen in the following equation:

$$T_0 = 2Nt_d \tag{1.14}$$

A comprehensive overview of phase noise in CMOS ring oscillators is given in [41, 42]. In [41] the author discusses achievable phase noise as function of oscillator topology and the number of stages in the ring. It also includes measured phase noise results on a number of experimental inverter-chain-ring-oscillators using both simple inverter cells and current starved inverter cells. A symmetry in rising and falling edge of the oscillator waveform is said to lower the $1/f^3$ corner frequency and to decrease phase noise. Single ended ring oscillators are said to be best in terms of phase noise but worse in terms of susceptibility to supply noise. In [42] a modified linear model for the additive noise sources in a ring oscillator is developed and the model is used to calculate an effective quality factor that can be expressed entirely in technology parameters and supply voltage. It predicts that a more advanced CMOS technology will produce lower phase noise.

1.5 Noise sources

Noise sources in any oscillator are thermal noise and flicker noise. Thermal noise is white noise whatever the frequency of oscillation. Its power spectral density is given by the equation:

$$S_v(f) = 4kTRe(Z) \qquad S_i(f) = 4kTRe(Y) \tag{1.15}$$

Where Re(Z) and Re(Y) are respectively the impedance and the admittance of the equivalent noise sources, T is the temperature in Kelvin and k is the Boltzmann constant. For LC oscillators, such of figure 1.5, thermal noise sources are the parasitic resistances of the inductor, of the varactor, and of the MOS transistors. Thermal noise of the inductor whose model is viewed in figure 1.5.(b) is given by the following equation, [20]:

$$S_i(f) = 8kT[\frac{1}{R_p} + \frac{1}{(L\omega_0)^2/R_s}] \tag{1.16}$$

Where R_p and R_s are the parasitic serial and parallel resistors of the inductor, ω_0 is the oscillation pulse.

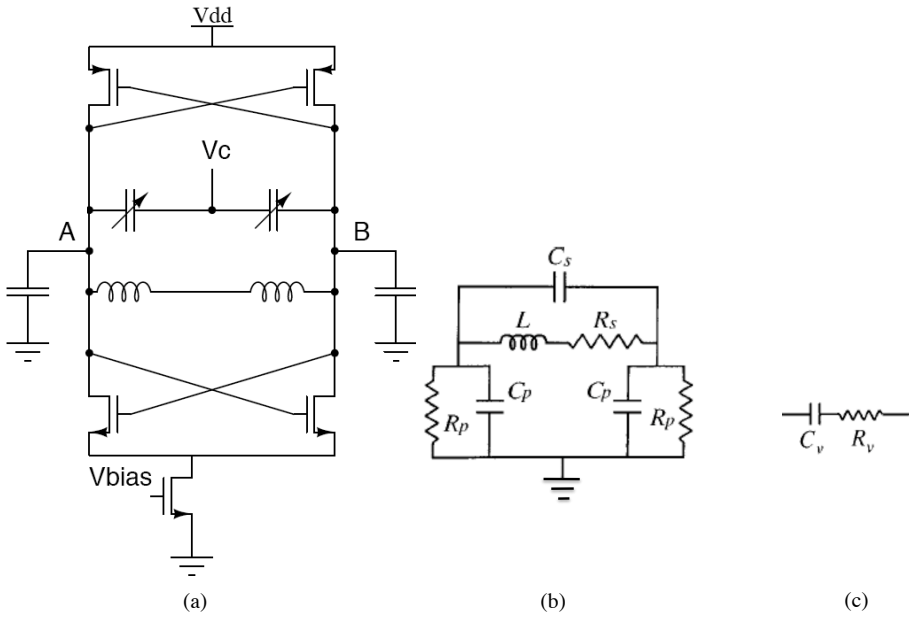


Figure 1.5: (a) Cross coupled LC VCO. (b) Inductor model. (c) varactor model

Thermal noise of the varactor whose model is viewed in figure 1.5.(c), is presented in the equation 1.17.

$$S_i(f) = \frac{8kTC_v\omega_0}{Q_v} \tag{1.17}$$

Where C_v is the capacitor of the varactor and Q_v is the quality factor.

MOS transistors have two sources of thermal noise, one between the drain and the source, the other is between the grille and the source. The power spectral density of the drain/source noise is:

$$S_i(f) = \frac{4kT\gamma I_{bias}}{E_{sat}L} \tag{1.18}$$

Where $\gamma = 2$ in the case of short channel, I_{bias} is the drain/source current of MOS transistor, L is the channel length, and E_{sat} is the electromagnetic field defined by:

$$E_{sat} = 2\frac{v_{sat}}{\mu} \tag{1.19}$$

with v_{sat} is the speed of saturation in the material, μ is the mobility in the channel.

The power spectral density of grille/source noise is expressed in the equation:

$$S_v(f) = \frac{4kT\delta W^2 C_{gs}E_{sat}L}{5I_{bias}} \tag{1.20}$$

where $\delta = 2$ in case of short channel MOS, C_{gs} is the grille/source capacitor.

Flicker noise has $1/f$ behavior and this contributes to an increase in oscillator phase noise at small offset frequencies.

In MOS transistor $1/f$ noise is given by the following equation:

$$S_i(f) = \frac{k}{f}\frac{\mu^2 E_{sat}^2 W}{4L} \tag{1.21}$$

Where W and L are transistor dimensions, k is the constant of Boltzmann, μ is the mobility and E_{sat} is the electromagnetic field defined by the equation 1.19.

1.6 Theoretical reviews of phase noise models

Phase noise is the up-conversion of noise sources in the oscillator circuit around the carrier frequency, thus generating a phase modulation of the oscillation signal. These fluctuations around the carrier frequency are named phase noise in spectral domain and jitter in time domain. In order to show the influence of the phase noise on radio communication system, we consider the receiver side of an RF transceiver. Just after the antenna, the RF signal passes through RF filter, then through Low Noise Amplifier LNA, then it is down converted by the mixer. The second signal of the mixer is the LO signal. The phase noise of this oscillator affects the quality of the received signal in terms of signal to noise ratio as can be viewed in figure 1.6. Wherein, because of the LO phase noise, the power of the neighbor signal is found in-band of the received signal after the downconversion.

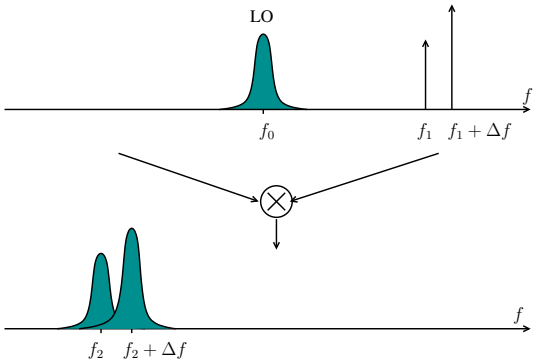


Figure 1.6: Effects of the phase noise behavior of LO on the received signal

Several phase noise models are already developed, [29, 43, 38]. The first one was the Linear Time Invariant model of Leeson which is reviewed in the next paragraph. The Linear Time Variant model of phase noise was developed later. Other numerical methods were also developed, such as the Spectre analysis model *Pnoise*. These models are more complex than the two models explained in this chapter.

1.6.1 The LTI phase noise model of Leeson

A Linear Time Invariant (LTI) model of phase noise was first proposed by Leeson [29]. The phase noise spectrum is divided into three regions, see figure 1.7. The first region is the $1/f^3$ region; it is considered as a close-in phase noise. The second region is the $1/f^2$

phase noise region and the third region corresponds to the noise floor and it is generally far from the carrier frequency. We ignore the phase noise in the noise floor region because it is

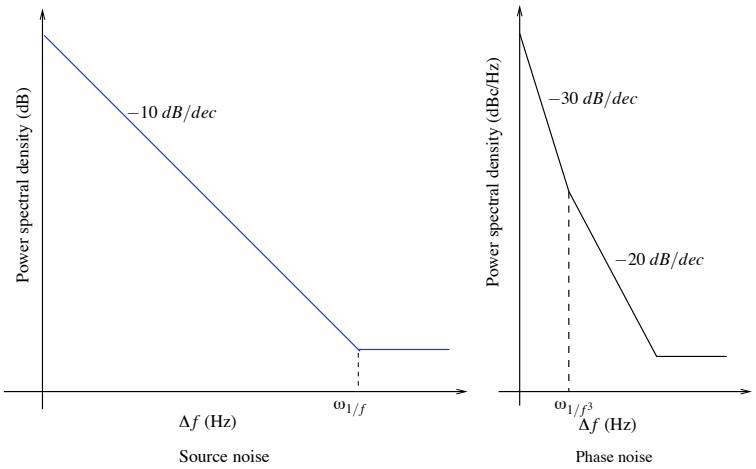


Figure 1.7: The up conversion of sources noise around carrier frequency

quite far from carrier frequency and can be eliminated by simple filtering operations. We will be interested in our model by the $1/f^3$ and $1/f^2$ phase noise regions. In equation 1.22 we find the expression of the LTI model of phase noise proposed by Leeson:

$$L\{\Delta\omega\} = 10.log\left[\frac{2FkT}{P_{sig}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{1.22}$$

where L is the power spectral density of the phase noise at the oscillator output, $\Delta\omega = 2\pi.\Delta f$ is the offset from the carrier frequency, F is the noise factor (empirical), k is the Boltzmann constant, T is the temperature, ω_0 is the carrier pulsation, Q is the quality factor of the LC oscillator and $\Delta\omega_{1/f^3}$ is the frequency of intersection between the two regions $1/f^3$ and $1/f^2$.

Leeson's model of phase noise is linear time invariant and it depends on the empirical noise factor F that must be determined from measurements and simulations of the oscillator circuit behavior in the linear part of the oscillation period. However, oscillators are completely non linear devices. The Hajimiri LTV phase noise model verifies the time variance behavior of phase noise in oscillators. The key point of the LTV model is that the response of the oscillator output to any impulse injection is time dependent. This dependence can be measured by the ISF that will be described in section 1.6.2.

1.6.2 LTV phase noise model

The LTV model of phase noise proposed by Hajimiri depends on the ISF of the oscillator. This function is, by definition, independent of the oscillation amplitude and the oscillation frequency in the tuning range of the oscillator [38]. It depends on the injection time $t = \tau$. Let's consider the LC cross coupled oscillator of figure 1.3. The noise sources in the circuit

are the parasitic resistances of the inductor and of the varactor and the drain current of the NMOS and PMOS transistors. As mentioned above, the response to any current source injection is time dependent. Then, if the injection occurs when the signal attains

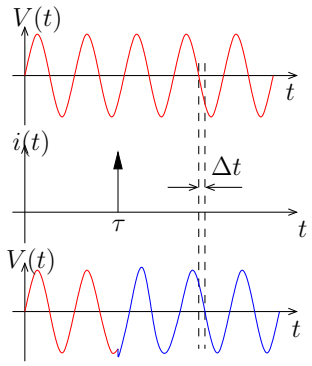


Figure 1.8: The response of an oscillator to current injection is time dependant

its maximum, the signal amplitude increases by an amount $\Delta V = \Delta q/C$ but the new waveform remains in-phase with the one before perturbation occurs, i.e. the time of zero crossing does not change. On the other hand, if the injection happens when the signal crosses zero, its phase changes and its amplitude remains constant. So, an injection at any time of the oscillation period will affect both amplitude and phase at once. Hence, there is a time dependant phase response to any impulse injection.

The phase response $h_\varphi(t,\tau)$ to an impulse injection current $i(t)$ can then be written as [38]:

$$h_\varphi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau) \tag{1.23}$$

where $u(t)$ is the unit function, $\Gamma(\omega_0\tau)$ is the ISF and it is measured in (Rad.C) units, and q_{max} is the maximum charge displacement at the VCO output node. $\Gamma(\omega_0\tau)$ determines the sensitivity of the oscillator to an injection at phase $\omega_0\tau$ of oscillation. It is periodic and it can be represented in function of its Fourier transform coefficients C_n as we see in the following equation:

$$\Gamma(\omega_0\tau) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n cos\left(n\omega_0\tau + \theta_n\right) \tag{1.24}$$

where $\Gamma(\omega_0\tau)$ is the ISF function, τ is the injection time. Analytical methods used for the determination of the ISF values are described in [38], but the most accurate method is the direct determination of the ISF by simulation which is described in the next section.

The LTV phase noise model developed by Hajimiri in the $1/f^2$ region depends on the Fourier transform coefficients C_n of the ISF function and it can be written as:

$$L(\Delta\omega) = 10.log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}.\sum_{n=0}^{\infty} C_n^2}{4q_{max}^2\Delta\omega^2}\right) \tag{1.25}$$

where $\overline{i_n^2}/\Delta f$ is the power spectral density of the noise current source, q_{max} is the maximum charge displacement on the node, and $\Delta\omega$ is the offset from the carrier frequency.

Phase noise in the $1/f^3$ region is given by the equation

$$L(\Delta\omega) = 10.log\left(\frac{C_0^2}{q_{max}^2}.\frac{\overline{i_n^2}/\Delta f}{8.\Delta\omega^2}.\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{1.26}$$

In Leeson's model, the intersection point $\omega_{1/f}$ between the $1/f$ noise region and white noise region is identical to the point ω_{1/f^3} of intersection between $1/f^3$ and $1/f^2$ phase noise regions. Whereas, in the LTV model of Hajimiri the conversion of noise sources into phase noise around the carrier frequency will not retain this point. The ω_{1/f^3} point depends on the Fourier transform coefficients of the oscillator's ISF function and it can be expressed as:

$$\omega_{1/f^3} = \omega_{1/f}.\left(\frac{C_0}{2\Gamma_{rms}}\right)^2 \simeq \omega_{1/f}.\frac{1}{2}\left(\frac{C_0}{C_1}\right)^2 \tag{1.27}$$

where Γ_{rms} is the rms value of $\Gamma(\omega_0\tau)$.

We see from this equation that the point ω_{1/f^3} is not identical to $\omega_{1/f}$ but it is reduced by a factor of $(C_0/2\Gamma_{rms})^2$. The coefficient C_0 depends on the waveform and can be reduced if the oscillation waveform has more symmetrical properties. This property is considered in the design of LC oscillator (used in ADPLL model) and ring oscillator (used in the realized ADPLL).

1.7 Jitter definitions

In the time domain, jitter is defined as perturbations of zero crossing instants of the periodic signal. In real oscillator, in the presence of noise sources, the n^{th} period of output signal of an oscillator is not constant as can be viewed in figure 1.9. It has a Gaussian distribution. If T_0 is the average period of the signal, we define the difference $\Delta T_n(t)$ between the real n^{th} period $T_n(t)$ and the average period. If $\Delta T_n(t)$ is different from zero, jitter exists.

$$\Delta T_n(t) = T_n(t) - T_0 \tag{1.28}$$

The distribution has a standard deviation, which we will define in equation 1.31 as the cycle-to-cycle jitter. The absolute jitter is defined by $\Delta T_{abs}(N)$ [44],

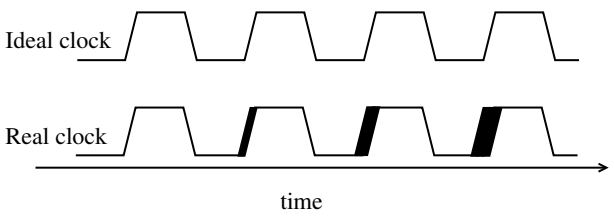


Figure 1.9: The jitter in periodic signal

$$\Delta T_{abs}(N) = \sum_{n=1}^{N} \Delta T_n \tag{1.29}$$

The cycle jitter is defined as rms value of the timing error ΔT_n as expressed in the equation

$$\Delta T_c = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} \Delta T_n^2} \tag{1.30}$$

Cycle jitter describes the magnitude of the period fluctuations, but it contains no information about the dynamics.

The cycle to cycle jitter is the rms difference between two consecutive periods like the equation [44]

$$\Delta T_{cc} = \lim_{N\to\infty} \sqrt{\frac{1}{N}\sum_{n=1}^{N} (T_{n+1} - T_n)^2} \tag{1.31}$$

1.8 Relation between jitter and phase noise

In the absence of 1/f noise in a region where the phase noise displays a -20 dBc/Hz slope, the cycle-to-cycle jitter can be related to the phase noise by the following equation [44]:

$$S_\Phi = \frac{(\omega_0^3/4\pi)\ \Delta T_{cc}^2}{(\omega - \omega_0)^2 + (\omega_0^3/8\pi)^2 \Delta T_{cc}^4} \tag{1.32}$$

In the presence of 1/f noise, absolute jitter can be calculated from an arbitrary phase noise response from different equations that are published in the literature [41, 45, 46]. Since no equation was compared to measurements we chose the equation presented by [41] within the phase noise is modeled using the LTV model (see section 1.26). This equation is written as 1.33.

$$\Delta T_{abs}^2(t) = 4 \int_{-\infty}^{\infty} S_\Phi(f)\ \sin^2(\pi f t)\ df \tag{1.33}$$

1.9 State of the art of ADPLL

A number of digital PLLs have been described in the literature [1, 2, 3, 4], with target application ranging from microprocessors to cellular telephone chipsets. Key DPLL design issues include how the phase error between reference and feedback clock is quantified, the structure of the loop filter, whether an analog (via digital-to-analog conversion of the filter output) or direct digital control of the VCO is used, and the choice of oscillator topology. On the other side, in ADPLL, all input output signals between blocks are digital, then, it is less sensitive to noise. The migration to digital blocks brings many advantages such as the fast design flow using Computer Aided Design tools. In addition, digital circuits are easily scalable with the technology development, while analog circuit parameters vary strongly with technology advancement.

One architecture of integer frequency synthesis composed of discrete elements is proposed by [1]. Wherein, the reference is replaced by *Read-Only Memory ROM*. Since the reference frequency is constant, the phase is a linear function of time. The phase values are stored in the ROM and they are used at sampling instants. The phase detector is a digi-

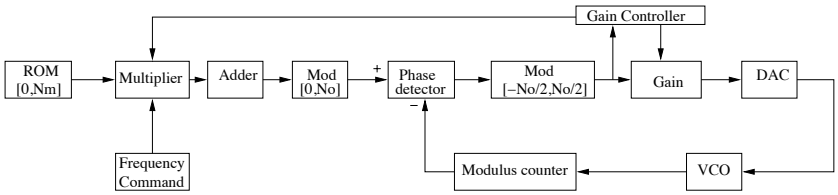


Figure 1.10: Integer digital frequency synthesizer [1]

tal subtractor. The reference phase and the variable phase are calculated using modulus counter. The oscillator is controlled by the error signal via a Digital to Analog Converter DAC. No loop filter in this loop, this is then, a first order ADPLL. This ADPLL is tested for application around 80MHz and it is composed of DSP's except the oscillator.

One chip of digital fractional synthesizer is then proposed in [2], it is viewed in figure 1.11. The DCO control word has 16 bits. Arithmetically incrementing or decrementing the DCO control word modulates DCO frequency and phase. The adder and subtracter provide the updates to the DCO control register. Also, the anchor circuit, which contains a

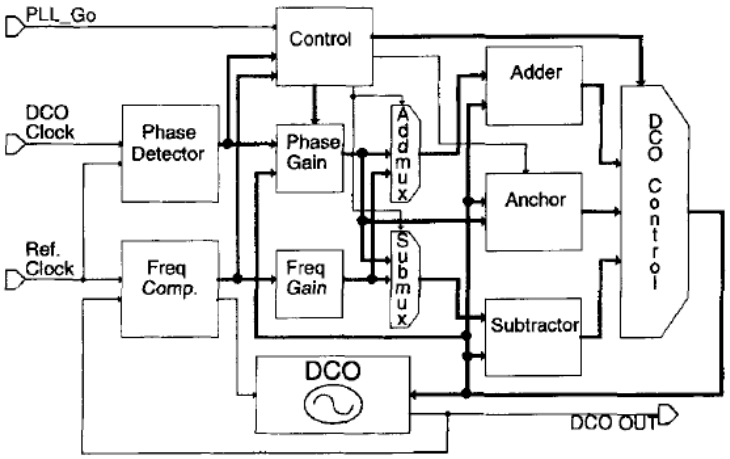


Figure 1.11: ADPLL architecture of fractional frequency synthesis proposed by [2]

register and an adder, updates the DCO control register in frequency maintenance mode. The frequency-gain register and phase-gain register provide operands to the adder and subtracter via the add mux and subtract mux. In addition, the phase-gain register provides data to the anchor circuit. The ADPLL uses four loosely coupled modes of operation: frequency acquisition, phase acquisition, phase maintenance, and frequency maintenance.

The phase-lock process is separated into frequency acquisition and phase acquisition, which reduces the phase-lock time penalty.

The ADPLL has 6000 transistors and 1100 mm^2 in a TLM 0.5μm CMOS process. It consumes 12 mA from a 3.3 V supply (DCO@100 MHz). At 200 MHz, the ADPLL has a peak-to-peak jitter under 125 ps. The DCO is ring oscillator based on inverter gates and it operates from 50 to 550MHz. It is described in section 1.10.

The first architecture of fractional synthesis for RF wireless application is proposed by [3] for Bluetooth applications. It is viewed in figure.1.12. It contains a Digital Controlled Oscillator (DCO) that allows the loop to be controlled in a digital manner. This DCO has an LC resonator but the varactor is replaced by an array of capacitors that could be switched individually into a high or low capacitance mode by a two-level digital control voltage bus, thus giving a coarse tuning for the high significant bits (MSBs) and less coarse for the low significant bits (LSBs) [47]. The ADPLL contains also two digital phase accumulators to calculate both the reference phase and the variable phase of the DCO output. A retiming reference clock is used to calculate the two phases in synchronous instants. This clock is obtained by over-sampling the reference signal by the DCO output signal. A Time to Digital Converter (TDC) is used to correct the fractional phase error with precision of one inverter delay. A $\Sigma\Delta$ modulator is used to dither the LSB bits of frequency control word generated by the loop filter in order to increase its frequency resolution. This modulator is used to push the residual quantization noise into higher frequencies, which are then rejected by the low pass characteristic of the ADPLL closed loop transfer function.

This ADPLL is considered as the first generation of Digital Radio Frequency Processor (DRFP) implementing a single-chip full Bluetooth radio. It is realized in 130nm CMOS technology. An enhancement on the RF circuit performances of the DRFP is proposed in [17] using 90nm CMOS process for more challenging application like GSM.

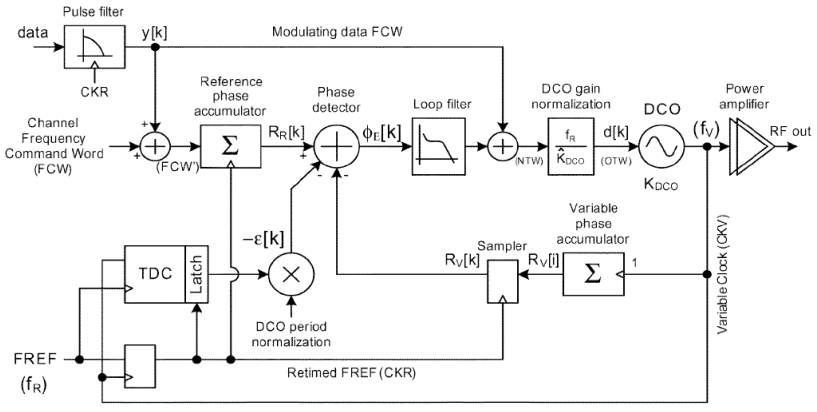


Figure 1.12: ADPLL frequency synthesizer for Bluetooth/GSM applications, [3]

Recently, an all static CMOS ADPLL fabricated in 65nm is proposed in [4]. Figure 1.13 shows the top level diagram of the ADPLL. Wherein, a bang-bang phase and fre-

quency detector (PFD) is used to compare the arrival times of the reference and divided clock edges. The resulting early/late information is filtered through a digital proportional-differential-integral filter operating at the divided frequency. The output of the filter is divided into most significant bits (MSB), which are sent directly to the DCO, and the least significant bits (LSB), which are sent to a third-order $\Sigma\Delta$ modulator to enhance the frequency resolution of the DCO. The output of the DCO is divided down in two stages. The first stage is used to generate a local clock that goes to all of the digital logic, while the second stage is used to generate a clock gating signal that further reduces the effective clock frequency, and is used by the loop filter and the PFD. A duty cycle correction buffer (DCC) at the output of the DCO is used to compensate for asymmetries of the DCO output drivers. The DCO is a three stage, inverter based ring oscillator. It is described in section 1.10.

The measured phase noise of the ADPLL is -112dBc/Hz@1 MHz offset from 4GHz output frequency. Period jitter for this design was measured to be 0.7 ps RMS for a 4GHz output frequency. Power consumption was measured to be 17.2mW from a 0.9 V supply at a 4 GHz output frequency.

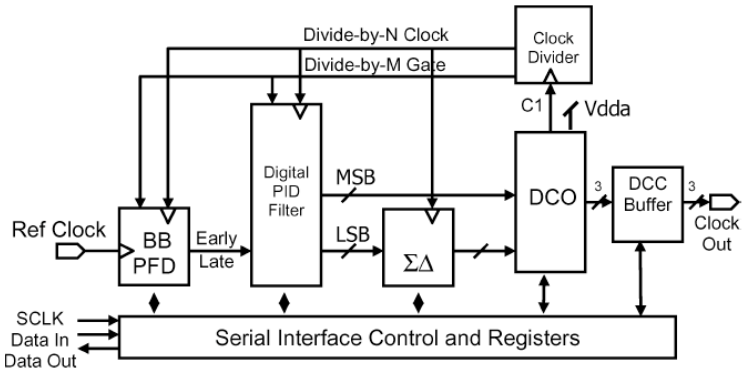


Figure 1.13: The ADPLL architecture proposed in [4] for 4GHz applicayions

A summary of performances of the presented ADPLL is viewed in the illustrative table 1.1. Wherein, the presented architectures of ADPLL cover various radio frequency applications. The design requirements are different from application to another. We find that no one is proposed for TV application. Within, phase noise requirements are challenging as we will see in chapter 3.

1.10 State of the art of DCO

The design of DCO is considered as the most challenging work in the design of ADPLL. It determines most of the performances of the LO such as the tuning range, the power consumption, the surface, and the phase noise. As we said before, oscillators has generally an LC or a ring resonator circuit. Therefore, DCO is an LC or ring oscillator that is digitally controlled. Comparison between LC and ring oscillator is presented in section

Table 1.1: ADPLL state of the art

ADPLL	[1]	[2]	[3]	[4]
Phase noise/Jitter		<125ps pp		-112dBc/Hz@1 MHz
Frequency	80MHz	50-550MHz	2.4GHz	0.5-8GHz
Area		1100mm^2	3mm^2	200μm×150μm
Power consumption		12mA-3.3V	37mA-1.5V	8mW/GHz-1.2 V

1.4. Here we are interested by the way the oscillator frequency is controlled.

Two main realized DCOs are presented in the literature [27, 47, 4, 5]. The first one is named hybrid digital control and it is viewed in figure 1.14. It consists of a digital to analog converter and a VCO. This approach has a significant advantage in that it enables the immediate use of well known and understood VCO and DAC structures with minimal redesign. The disadvantage of this architecture is that performances depend on the

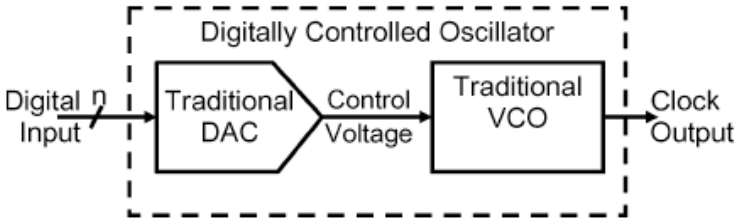


Figure 1.14: DCO formed by DAC and VCO

analog behavior of both components that may limit the benefit of implementing ADPLL architecture. Furthermore, the analog dependence of this design style makes portability to newer or different technologies less direct, leading to extensive manual intervention if a remap is required.

The second approach, shown in figure 1.15, is to digitize the mechanism for varying the frequency as presented in [27] for an LC-tank based DCO and in [4] for an inverter based ring oscillator. This approach demands a much larger oscillator than that of the hybrid approach.

The first architecture of cross coupled LC DCO is presented for Bluetooth applications, [27] . The proposed solution to control the oscillating frequency could generally be summarized as follows. The varactor of the resonator circuit is replaced by an array of varactors that could be switched individually into a high or low capacitance mode by a two-level digital control voltage bus, thus giving a very coarse step control for the more-significant bits, and less coarse step control for the less-significant bits, see figure 1.16. In order to achieve a very fine frequency resolution, the LSB digital control bit (or multiple bits) are dithered using a $\Sigma\Delta$ modulator.

The proposed idea of high-rate dithering of LSB capacitors is illustrated in figure 1.17.

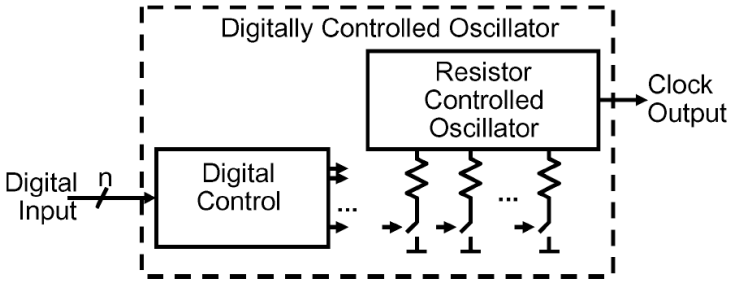


Figure 1.15: The direct digital approach of DCO control

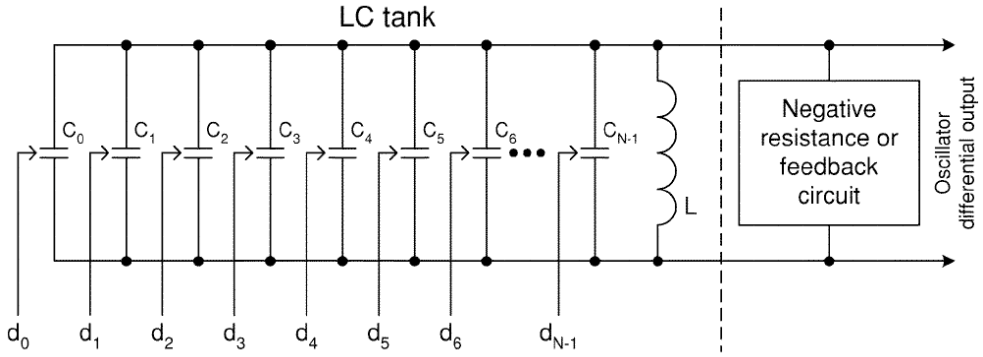


Figure 1.16: LC-tank-based oscillator with switchable capacitors

Instead of applying a constant input that would select capacitance C_1 or C_2, where $C_2 = C_1 + \Delta C$ with ΔC being an LSB capacitor, during the entire reference cycle, the selection alternates between C_1 and C_2 several times during the cycle. Figure 1.17 shows an example of the dithering method, within, C_2 is chosen one-eighth of the time and C_1 is chosen the remaining seven-eighths. The average capacitance value, therefore, will be one-eighth of the $C_2 - C_1$ distance over C_1. The resolution of the time-averaged value relies on the

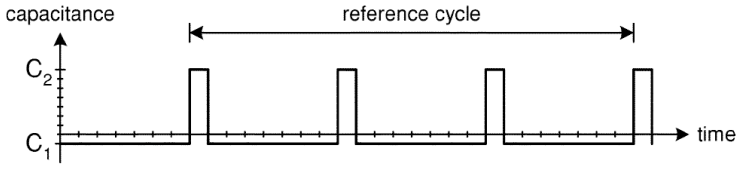


Figure 1.17: DCO dithering by changing the discrete capacitance at high rate

dithering speed. Without any feedback that would result in a supercycle, the dithering rate has to be higher than the reference cycle rate times the integer value of the resolution inverse (eight in this case). Therefore, there is a proportional relationship between the frequency resolution improvement and the dithering rate. The oscillator frequency is then

controlled by the digital bits d_k and equation 1.10 of the output frequency becomes:

$$f = \frac{1}{2\pi\sqrt{L\sum_{k=0}^{N-1} C_k}} \tag{1.34}$$

Where C_k value is given by the following equation

$$C_k = C_{0,k} + \overline{d_k}.\Delta C_k \tag{1.35}$$

A complementary cross-coupled LC structure is used in this DCO to average the noise contribution between NMOS and PMOS transistors at different bias conditions. On the other hand, the transistors were sized so that each NMOS and PMOS pairs generates about one-half of the total thermal noise. Consequently, the overall thermal noise is lower than the one attained when using only an NMOS pair.

The DCO [27] has been fabricated in a digital 0.13μm CMOS process together with a digital signal processor to investigate noise coupling. The 2.4-GHz DCO core consumes 2.3 mA from a 1.5-V supply and has a tuning range of 500MHz. The phase noise is -112 dBc/Hz@500-kHz. An enhancement on the DCO phase noise performances is proposed for GSM applications [47] and for 3G applications [48] using 90nm CMOS process.

In [4], the inverters that comprise the ring are divided into addressable component structures and the effective strength of the composite inverters adjusted by increasing or decreasing the number of enabled transistors that form each stage of the ring. As a drawback, this approach demands a much larger oscillator than that of the hybrid approach. Figure 1.18 shows the structure of the DCO used in the ADPLL of [4]. Each stage of this three-stage ring oscillator comprises 271 tri-state CMOS inverters connected in parallel, yielding a total of 813 inverters. As more inverters in each stage are turned on by the control blocks of the DCO, the current driving strength of the stage increases while its capacitive load remains essentially constant, resulting in an increase in the output frequency.

The tri-state inverters are arranged in an array of 17 rows by 48 columns, yielding a total of 816 inverters. The first 16 rows of the inverter array are turned on/off by a row/column pseudo-thermometer control. On the periphery of the array, a set of column control latches determines which inverters in the partially turned on row are on, and which are off. A set of row control latches divides the rows into fully turned on, partially turned on, and fully turned off. When the loop filter requests an increase in the output frequency, the column control latches are shifted, turning on one more inverter in the partially turned on row as long as such an inverter is available. When the current row is fully turned on, the row control is shifted, so that the next available row becomes the partially turned on row. Likewise, when the loop filter requests that the frequency be reduced, the column and row controls are shifted in the reverse direction. To avoid having to flip all of the latches in the column control every time a change in which row is partially on occurs, adjacent rows are controlled by opposite polarities of the column control. When neither a decrease nor an increase are requested, a clock gating signal is generated to reduce the power dissipation generated by the row/column control.

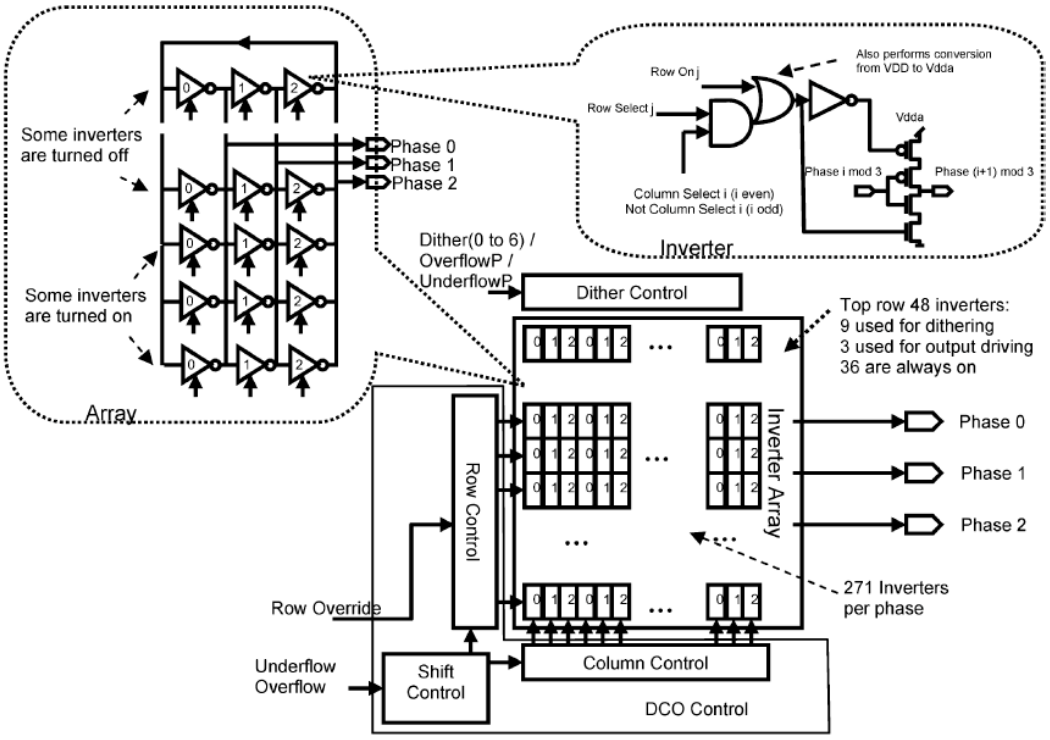


Figure 1.18: Tri-state inverter based DCO proposed in [4]

A $\Sigma\Delta$ modulator was implemented using a programmable, third order, MASH architecture. It can be configured to operate as a first, second, or third order element, or can be altogether turned off by using clock gating on each of the sections of the modulator. The modulator is used to encode the fractional frequency generated by the loop filter into dithering signals for the DCO, effectively increasing its frequency resolution. Higher order sigma delta modulators are used to push the residual quantization noise into higher frequencies which are then rejected by the low pass characteristic of the ADPLL closed loop transfer function.

This DCO has been fabricated in a 65nm CMOS process. It consumes 4.5mW/GHz from 1.2V power supply and the digital part consumes 3.9mW/GHz. It has a tuning range from 4 to 7.7GHz. The measured phase noise is -112dBc/Hz@1MHz offset from 4GHz carrier frequency.

Another ring DCO based on adjustable resistor is presented in [5]. The DCO circuit is viewed in figure 1.19. The ring is composed of a coarse delay chain and a fine delay chain to have wide lock range and fine resolution. The coarse delay chain consists of a coarse cell with tuning codes of 4 bits, three replica coarse cells with fixed tuning codes and a 4-to-1 mux for tuning codes of 2 bits to have wide lock-in frequency range. The coarse cell has tuning codes of 2 bits with PMOS array and 2 bits with NMOS array in the form of thermometer code. It has monotonous increase of delay according to increase

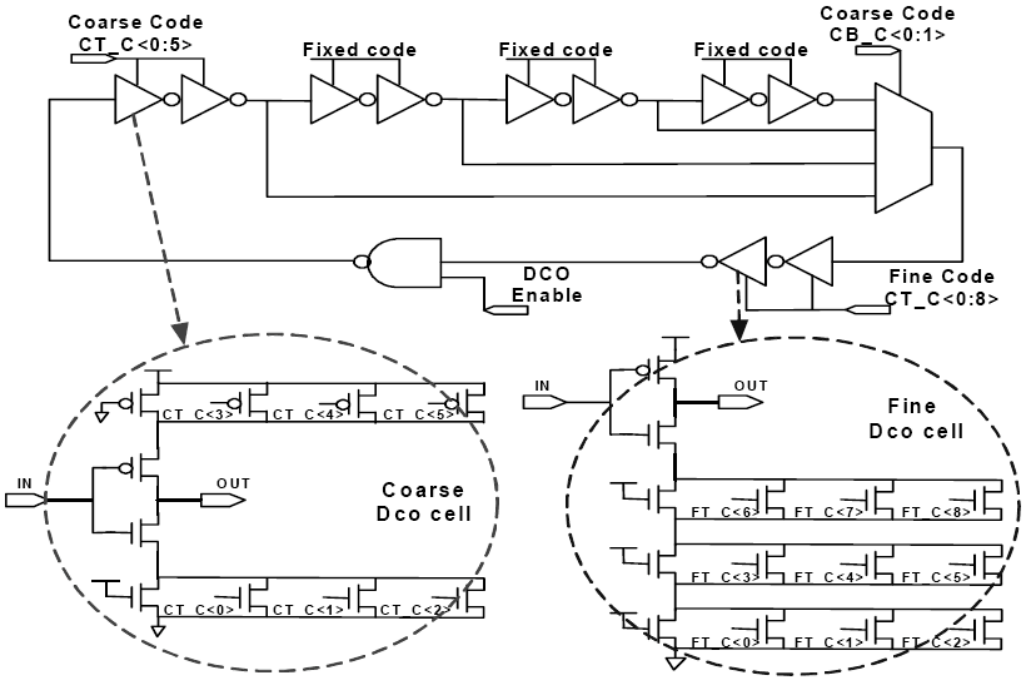


Figure 1.19: Ring DCO circuit of [5]

of tuning codes. Meanwhile, the fine delay chain consists of only a fine cell with tuning codes of 6 bits. The fine cell has tuning codes of 6 bits by only NMOS array in the form of thermometer code.

This DCO is implemented in an ADPLL chip that is fabricated using a 0.18μm CMOS technology. The ADPLL has operation range between 520MHz and 1.5GHz and has 76ps peak-to-peak jitter at 668MHz.

The presented ring DCO architectures use a thermometer code tuning word. This coding type can minimize the jitters since only one transistor has transition at the update of tuning codes and this code type has less DAC circuit size than binary weighted codes. Binary type of coding for the DCO control word is presented in [2]. Wherein, the DCO is inverter based ring oscillator. In order to have a larger tuning range, the number of ring stages can be switched form 4 to 8 according to the enable bit at the input of NAND gate as can be viewed in figure 1.20.

In the DCO of figure 1.20, the binary code word controls every stage of the ring as can viewed in figure 1.21. In this figure we see that the sizing ratio of the control devices is a power of two, achieving binarily weighted control. The most significant control-word bit (15) corresponds to the largest control device. Thus, when control bit 15 asserts, the largest device (256×1.2μm) is on in each DCO cell.

A stand-alone, 4-cell test DCO was fabricated using 0.5μm CMOS and it operates with a supply voltage of only 0.7 V and runs up to 900 MHz with a supply voltage of 3.3 V. Its tuning range is from 50 to 550 MHz.

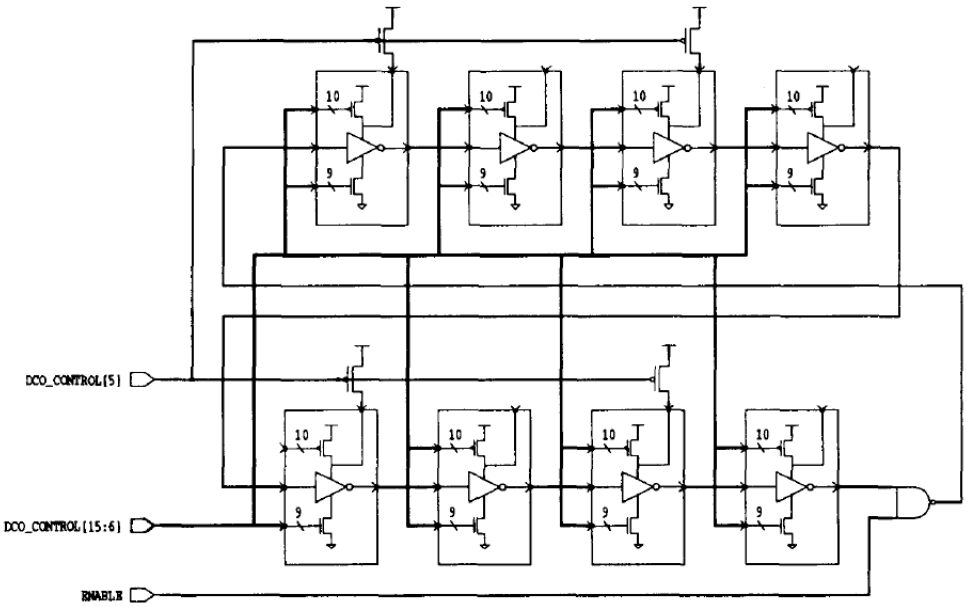


Figure 1.20: The DCO proposed by [2]

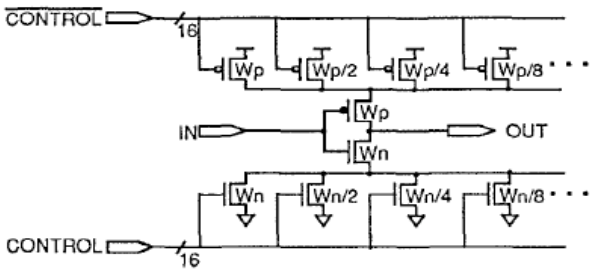


Figure 1.21: The digital control word is binary coded in the DCO of [2]

We summaries the presented state of the art by the table of performances of the DCO in terms of technology of fabrication, frequency range, phase noise/jitter and power consumption.

1.11 State of the art of TDC

For many applications various TDC architectures are proposed in the literature, starting from analog intensive solution that is presented in [49] to the CMOS digital solutions [50, 51, 52, 53, 54, 55]. For the analog intensive TDC, the form factor was less important than achieving high-resolution and accuracy. As a result, many of the best TDC solutions in terms of resolution are large, consume significant power, and require complex tuning or calibration. Unlike these designs, TDC constructed with digital CMOS technology have

Table 1.2: A summary table of DCO performances

DCO	Technology	Frequency range	Phase noise (dBc/Hz)	power consupmtion
LC-[27]	130 nm	central=2.4GHz range=500MHz	-112@500kHz	2.3mA-1.5V
LC-[47]	90 nm	central f=3.6GHz range=900MHz	-165@20MHz	18mA-1.4V
Ring-[4]	65 nm	4-7.7GHz	-112@1MHz	11.2mW
Ring-[5]	0.18 μm	520MHz-1.5GHz	76ps p-p	26.8mW
Ring-[2]	0.5 μm	50-550MHz	NA	NA

benefited greatly from process feature scaling, since a more advanced process results in not only compact and fully-integrated solutions, but also smaller CMOS gate delays and the accompanying improvement in resolution.

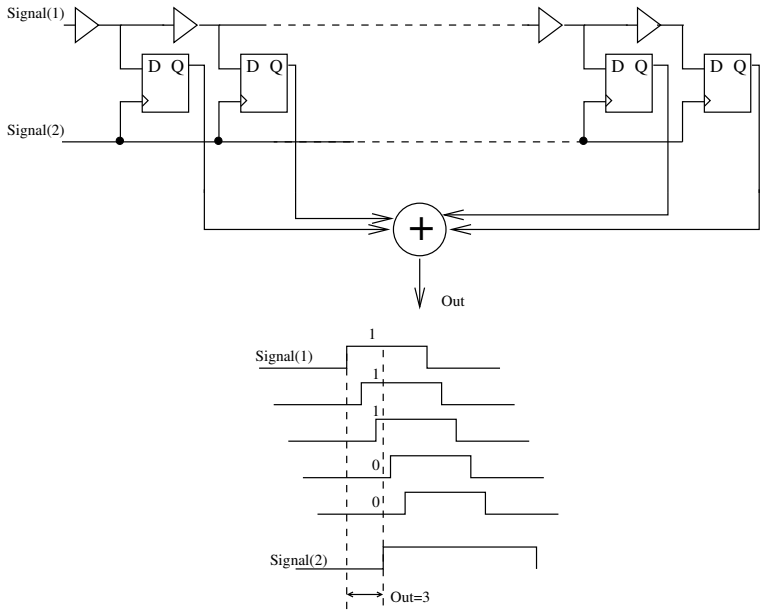


Figure 1.22: TDC delay line architecture

The classical digital solution is the chain-delay line based TDC, [56, 57]. It is shown in figure 1.22 and effectively works by counting the number of sequential inverter delays that occur between two rising edges of signal(1) and signal(2). One very attractive feature of this architecture can be seen immediately in that the TDC can be constructed entirely from standard digital gates, or it could be programmed on FPGA. The compact and digital architecture offers a moderate performance, and has been proved to be commercially viable

for some digital PLL applications in the wireless industry [58].

To explain its operation, consider a rising edge of signal(1), which represents the first event. It is successively delayed by a series of gates, each with delay t_d. The outputs from each of these inverters are input to a register, which is clocked with the rising edge of signal(2) representing the second event. A thermometer code is then generated at the register output, which corresponds to the number of delay elements that have transitioned within the measurement interval. The TDC output named Out is then calculated as the sum of the thermometer code.

Although the delay-chain architecture offers a simple TDC with moderate performance, an important limitation to consider is the high cost for increasing its range. Increasing the dynamic range of the delay-chain TDC requires a linear increase in the number of delay elements, which similarly increases the power consumption and decreases the maximum sampling rate.

An alternative solution to the delay line TDC is the parallel delay gates presented in [6]. The signal(1) traverse parallel delay elements as can be viewed in figure 1.23. The delay time of the first inverter is t_d, that of the second is $2t_d$, ...,and the last delay gate is Nt_d. Then, at the arrival of the rising edge of signal(2), the output signal of the registers are

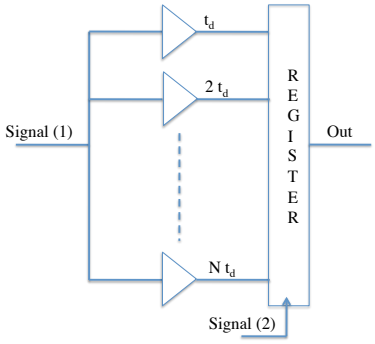


Figure 1.23: TDC architecture formed by parallel delay gates [6]

read and the TDC output signal Out is determined. The different delays of the different branches are made via load capacitors. This load increases the design mismatch and limits the TDC performance.

The Vernier delay technique [7] is one of the older techniques for time digitization that has been adopted for improving the resolution of digital CMOS TDC [52]. As shown in Figure 1.24, the concept is to effectively retard the two signals using two delay-chains each of different time delay (T_{DEL1} and T_{DEL2}). The resolution in this case is not the absolute rate of transitions, but the relative rate of transitions. As a result, the effective resolution of the Vernier TDC is found to be the difference of the two delays, $T_{DEL1} - T_{DEL2}$.

An enhancement to the resolution of the delay line TDC of [59] has been recently proposed in [60]. This TDC employs two stage conversion by a delay line based TDC. The time residue after the first stage is amplified by a Time Amplifier TA and then processed by a second stage. It improves the resolution by a factor of almost 20, [61]. The main disadvantage of this TDC is its large area and relatively complex design, which leads to

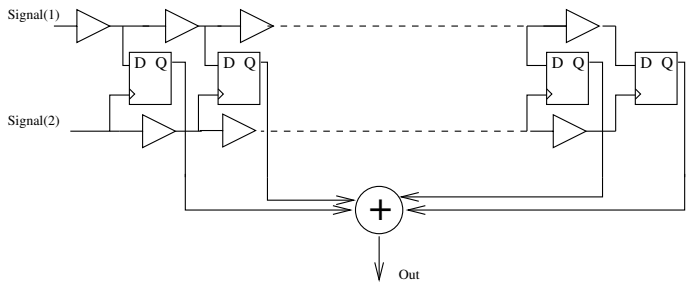


Figure 1.24: Vernier TDC of [7]

nontrivial scaling as the process shrinks. Given that the time measurement is done by a delay line, a calibration is necessary in this case as well.

All these TDCs suffer from many problems, starting by the limited resolution of the delay line, to the high mismatching of the parallel buffers, to the complex design of the vernier TDC, to the large area, high power consumption, and complexity of TA TDC. For many applications very high resolution TDC is indispensable like nuclear experiments to locate single-shot events [62]. For applications of wireless communication systems such as GSM or Bluetooth a good resolution might be sufficient [57]. In chapter 3 we will present our merged DCO TDC design circuit for TV applications. Compared to the presented architectures, this TDC is considered as low power, low surface, scalable with technology advancement with minimum efforts.

1.12 Conclusion

This chapter presents a chronological progress of frequency synthesizer from classical PLL to ADPLL. Wherein, the internal blocks become digital like the phase comparator and the loop filter or digitally controlled like the DCO. The state of the art of ADPLL architectures is also presented. The comparison between the presented ADPLL in terms of tuning range, phase noise performance, area, and power consumption is viewed. Unlike the other presented ADPLL, the ADPLL architecture of [3] is developed progressively to cover Bluetooth,GSM, and 3G applications by architectural and circuit enhancements improving the modulation capability. The oscillator of this ADPLL has an LC resonator circuit which is not scalable with technology progress.

In this work, many point are taken into consideration:

- A precise model of ADPLL that takes into account the linear time variance of the DCO phase noise is required.
- A design of small, economic, portable with technology progress, and low phase noise oscillator is challenging.
- TDC noise exists whatever the architecture, but the complexity of the state of the art of these TDC is important. So, a design of simple, economical and portable TDC is interesting.

Chapter 2

Modeling of ADPLL

Local oscillators are key building blocks in modern communication systems. The needs for smaller cellular phones have created an increase in radio frequency integrated circuits. ADPLL are proposed to replace the analog PLL because of their low area. In addition, ADPLL contains more digital blocks that are scalable with technology progress. The design and optimization of an ADPLL in order to obtain a pure signal with low power and low area is a significant challenge. Two noise sources exist in the ADPLL, they come from the DCO and the TDC. In spite of the digital control of the oscillator, it is an analog core block designed and optimized generally using electrical simulators at transistor level like Spectre[1]. Besides the mathematical models of oscillator basic elements (transistors, capacitors, inductors and resistors), these simulators allow analysis of circuit behavior in respect to variations of time and frequency. In addition, it contains predictive models of noise, phase noise that are powerful in the design of DCOs. For more complicated systems such as ADPLL, these tools are no more helpful since simulation time explodes with the complexity of the design. In this case, other modeling types are needed.

Macromodel based simulation is used in ADPLL designs, wherein, full circuit simulation is replaced by the use of small, simple behavioral models to approximate the loop responses [63] and phase noise [64], resulting in great simulation time saving. The time domain model of DCO presented in [64] models the oscillator jitter, wander, and flicker noise. These noises are described mathematically as additive random variables that are added to the ideal rising edges instants of the oscillation waveform. In another ADPLL model presented by [63], DCO macromodel is represented as a simple linear integrator that converts input oscillation control word to output period. This is an oversimplification and as a result, this model does not predict the impact of the DCO phase noise on the ADPLL total phase noise. These macromodels do not deal with the time variance behavior of oscillator phase noise that is presented in [38].

In this chapter we present a behavioral model of ADPLL with phase noise using VHDL-AMS modeling language. We model the ADPLL architecture of [3] that is presented in fig.2.1. Within the ADPLL, the DCO is modeled by a Linear Time Varying (LTV) model of phase noise, [38]. The LTV model of phase noise is based on the Impulse Sensitivity

[1] http://www.cadence.com/products/rf/spectre_circuit/pages/default.aspx

Function (ISF) of the oscillator, which describes carefully the sensitivity of an oscillator to any impulse current injection in any node of the circuit. The TDC noise is due to quantification error and it is modeled as well. The resulting model contains informations about noise at the transistor level, then, it predicts rigorously the ADPLL behavior in the presence of DCO and TDC noise. In addition, we present a z-domain model of the ADPLL. In which, we present the influence of the closed loop transfer function on the TDC and DCO noises. This model is descriptive and it could be used in system more complex such as radio receivers.

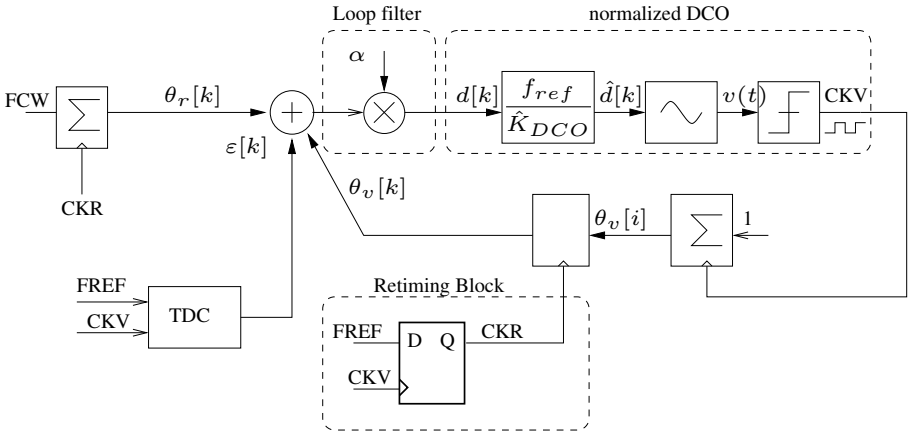


Figure 2.1: The block diagram of our ADPLL model

The model is programmed using VHDL-AMS modeling language. VHDL-AMS is a super set of the hardware description language VHDL (IEEE standard 1076-1993). It includes analog and mixed-signal extensions (AMS) in order to define the behavior of analog and mixed-signal systems (IEEE 1076.1-1999). The VHDL-AMS standard was created to enable designers of analog and mixed signal systems and integrated circuits to create and use modules that encapsulate high-level behavioral descriptions as well as structural descriptions of systems and components,[65, 66]. It is an industry standard modeling language for mixed signal circuits. It provides both continuous-time and event-driven modeling semantics, and so is suitable for analog, digital, and mixed analog/digital circuits. It is particularly well suited for verification of very complex analog, mixed-signal and radio frequency integrated circuits such as ADPLL. By using VHDL-AMS language we ensure the portability of the model and the fast time of execution.

2.1 Reference phase and variable phase

The oscillation period T_v is the instantaneous period of the DCO output signal CKV. FREF is the reference signal and T_R is its period. We assumes that $T_R >> T_v$. We suppose also that T_v and T_R are deterministic and then the zero crossing instants of each

one is given by the equations 2.1 and 2.2 respectively.

$$t_v = i.T_v \tag{2.1}$$
$$t_r = k.T_R + t_0 \tag{2.2}$$

where i = 1,2,...and k = 1,2,... are the zero crossing indexes of CKV and FREF signals and t_0 is the initial offset of the two signals. The two equations are normalized by T_v, then we define θ_v and θ_r as the variable phase and reference phase respectively as the following equations:

$$\theta_v = t_v/T_v = i \tag{2.3}$$
$$\theta_r = t_r/T_v = kN + \theta_0 \tag{2.4}$$

Where N is equal to T_R/T_v the number of CKV periods in FREF period.

Then, the variable phase is determined by counting the rising edges of CKV signal, and the reference phase is determined by accumulating N at every rising edge of FREF. N is known as the Frequency Control Word FCW. The reference and variable phases are then written as:

$$\theta_v = \sum_{l=1}^{i} 1 \tag{2.5}$$
$$\theta_r = \sum_{l=1}^{k} FCW \tag{2.6}$$

The FCW word is a digital word that contains an integer part N_i and a fractional part N_f like:

$$FCW = \frac{E(f_v)}{f_R} = \frac{T_R}{E(T_v)} = N_i + N_f \tag{2.7}$$

Where $E(f_v)$ and $E(T_v)$ are the estimated frequency and period of CKV respectively.

When the loop is locked, the phase difference ϕ_E is constant or zero. But, the zero crossing instants t_v and t_r are not synchronous so a metastability problem can occur. One solution is to retime the reference signal FREF by CKV, see section 2.3. Then, the reference phase is given by the following equation:

$$\theta_r[k] = t_r/T_v = k.FCW + \theta_0 + \varepsilon[k] \tag{2.8}$$

Where $\varepsilon[k]$ is the retiming error and it will be determined by the TDC. From equation 2.7, FCW has an integer part and a fractional part, then $\theta_r[k]$ has the same property and could now be divided into integer and fractional parts $\theta_{ri}[k]$ and $\theta_{rf}[k]$ as the equation:

$$\theta_r[k] = \theta_{ri}[k] + \theta_{rf}[k] + \epsilon \tag{2.9}$$

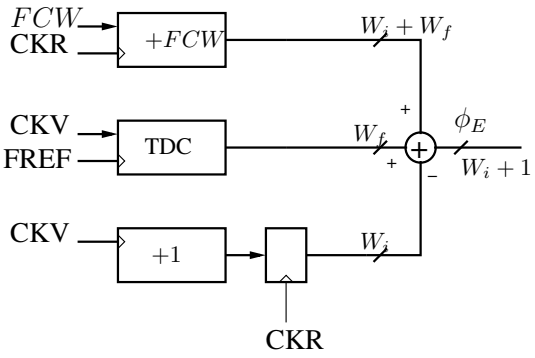


Figure 2.2: The phase detector diagram. CKR is the retimed reference clock

2.2 The phase detector

The phase error ϕ_E is the difference between θ_r and θ_v as viewed in the equation:

$$\phi_E[k] = \theta_r[k] - \theta_v[k] \tag{2.10}$$

By replacing $\theta_r[k]$ by the equation 2.9, we obtain the following expression of $\phi_E[k]$ in function of the integer part θ_{ri} and fractional part θ_{rf} of the reference phase and of $\varepsilon[k]$.

$$\phi_E[k] = (\theta_{ri}[k] - \theta_v[k]) + (\theta_{rf}[k] + \varepsilon[k]) \tag{2.11}$$

In the previous equation we arrange the integer parts together $(\theta_{ri}[k], \theta_v[k])$ and the fractional parts together $(\theta_{rf}[k], \varepsilon[k])$. Then the phase detector is presented in fig. 2.2.

2.2.1 The arithmetic modulus of reference and variable phases

We see in equations 2.5 and 2.8 that the variable and reference phases are the accumulation of digital numbers, this could saturate the registers. In order to prevent registers from saturation we use the arithmetic modulus. Then, the phases could be obtained by the following equations:

$$\theta_v[k] = mod(\theta_v[k-1] + 1, 2^{W_i}) \tag{2.12}$$

$$\theta_{ri}[k] = mod(\theta_{ri}[k-1] + N_i, 2^{W_i}) \tag{2.13}$$

$$\theta_{rf}[k] = mod(\theta_{rf}[k-1] + N_f, 2^{W_f}) \tag{2.14}$$

Finally, the integer parts of $\theta_r[k]$ and $\theta_v[k]$ are coded on W_i bits while the fractional part of $\theta_r[k]$ and ε are coded on W_f bits. The phase error $\phi_E[k]$ is a signed word and it is coded on $(W_i + W_f + 1)$ bits.

2.2.2 The design of the phase detector

As an example of application, we consider Bluetooth applications. Frequencies of this application range from 2.402GHz to 2.49GHz as presented in table 2.1. The reference

frequency is equal to 13MHz and according to equation 2.7, the integer parts N_i of the maximum and minimum FCW are coded on 8 bits. The fractional part N_f is coded on 10 bits in order to have a precision of 10^3 in the fractional part of FCW.

	Frequency	N_i
minimale	2.402GHz	184
maximale	2.49GHz	191
centrale	2.44GHz	187

Table 2.1: Bluetooth maximum and minimum frequencies and the integer part of FCW in case of 13MHz reference frequency

2.3 The retiming

The determinations of the variable phase and the reference phase have to be done at the same instants. This is done using the retimed reference clock CKR. CKR is obtained by oversampling FREF by CKV. This operation introduces an error in the calculation of the phase difference as can be viewed in fig.2.3. This error is named ε. In the absence of perturbations (noise, ...), ε is periodic as we can view in fig.2.4, and its value is determined by the TDC.

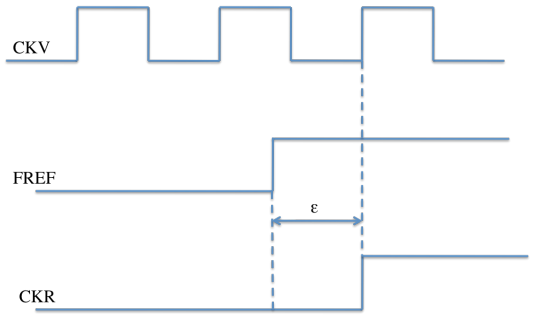


Figure 2.3: The retiming error

In fig. 2.4 we see FREF, CKV, CKR and the retiming error values ε. FREF period is equal to 22.5 ns, CKV period is equal to 10 ns, Then, $FCW = 2\frac{1}{4}$. The value of ε is observed at every rising edge of CKR ($\varepsilon = 0, 1/4, 1/2, 3/4$).

In case of positive and negative phase error the retiming error is given by the equation 2.15 , as can be viewed in fig.2.5.

$$\varepsilon = 1 - \frac{\Delta tr}{T_v} \tag{2.15}$$

Where Δtr is the time difference of the rising edges instants of FREF and CKV.

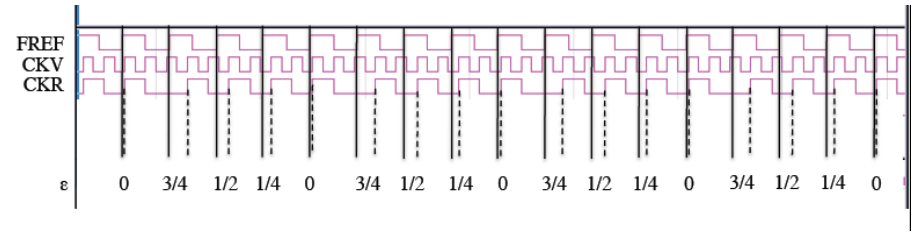


Figure 2.4: The retiming error is periodic

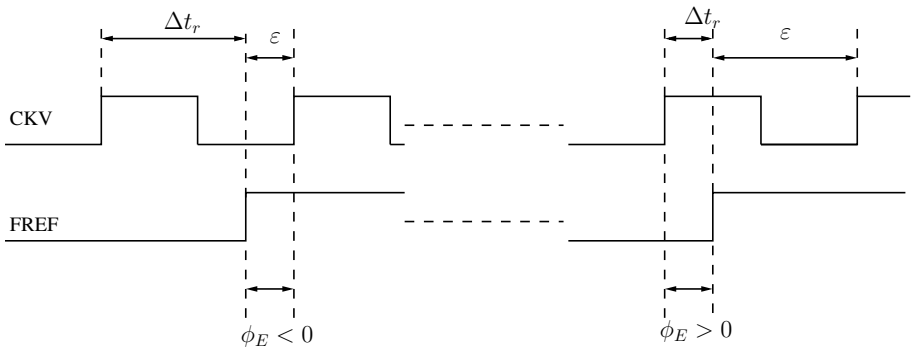


Figure 2.5: The expression of ε in positive and negative phase error

2.4 TDC model

Since the variable phase is the counting of the DCO signal periods between two FREF rising edges, as described in section 2.2, this operation limits the phase error quantification resolution to $Tv/2$. In wireless applications, this precision is not sufficient and best resolution is recommended. One good resolution architecture proposed by [57], is presented in fig.2.6. We implement this architecture in the ADPLL model for its simplicity regarding the other architectures, see section 1.11. The resolution of such TDC is equal to one inverter delay time t_d and the value of t_d that ensures a good resolution for GSM and Bluetooth application is equal to 40ps, [57].

2.4.1 TDC architecture

In this TDC the signal CKV is delayed successively by inverter gates, each one has the delay time t_d. The output of each inverter is the input of a register which is clocked at the rising edge of FREF. A thermometer code is then obtained at the register output. From this code, the distances between FREF rising edge and the rising and the falling edges of CKV are determined, then the instantaneous period T_v of CKV is calculated from the equation:

$$T_v = 2.|tr - tf| \tag{2.16}$$

where tr and tf are the rising and falling instants of CKV. This period is an integer number of t_d. The value of ε in function of tr and T_v is given by the equation:

$$\varepsilon[k] = 1 - \frac{tr}{T_v} \tag{2.17}$$

From equation 2.17, we see that the maximum value of ε is equal to 1. Then, the necessary

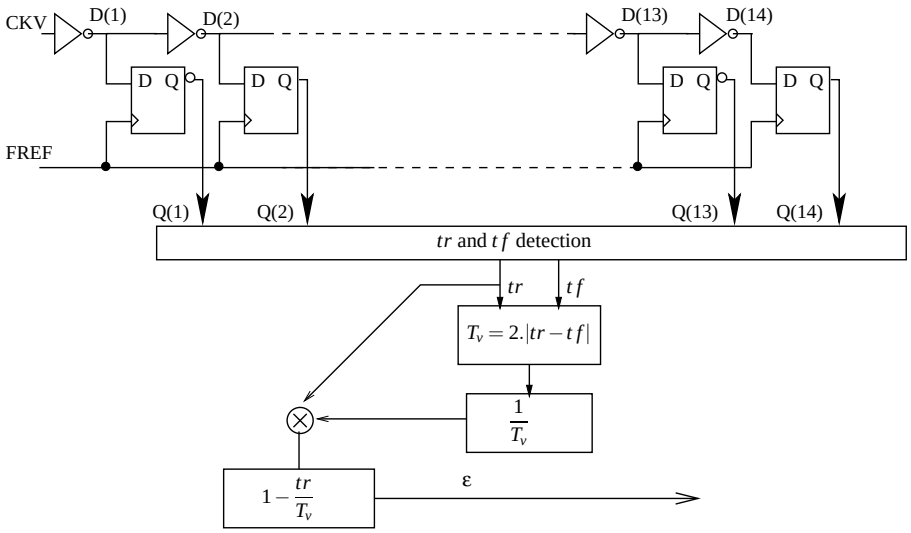


Figure 2.6: The TDC model of [3]

number of inverters in the TDC is determined from ratio of the maximum period that is covered by the ADPLL to one inverter delay t_d like the following equation:

$$L = \frac{max(T_v)}{t_d} \tag{2.18}$$

where $max(T_v)$ is the maximum output frequency of the ADPLL and t_d is the delay of inverter gate. From table 2.1, we see that the maximum period is $401.6ps$ and we take $t_d = 30ps$ for 90nm CMOS process, then, L is equal to 14.

By reading the thermometer code Q, we determine the value of tr and tf. If there is a transition from '1' to '0', we detect the rising edge tr, and if there is a transition from '0' to '1' we detect the falling edge tf as it is shown in the example of figure 2.7 . In this example, tr = 1 and tf = 6, then, from equation 2.16 we have $T_v = 10$, and from equation 2.17 we determine $\varepsilon = 9/10$.

2.4.2 TDC resolution

The phase detector output $\Phi_E[k]$ could be interpreted as the estimation of the deviation of the CKV frequency from the central frequency $\widehat{\Delta f_{out}}$ in one reference period. This could be written as

$$\widehat{\Delta f_{out}} = \Phi_E f_{ref} \tag{2.19}$$

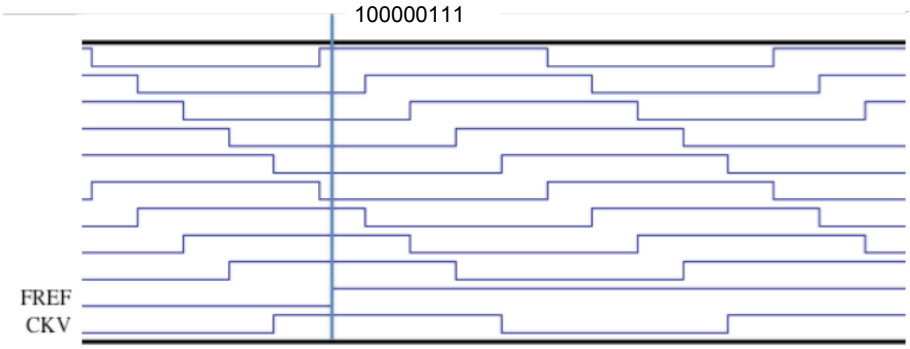


Figure 2.7: The functionality of the TDC model of [3]

In addition, phase detector resolution is equal to TDC resolution and it is defined in function of CKV period and time delay of one inverter gate as t_d/T_v. By replacing it in the previous equation we obtain the effect of the TDC resolution on the frequency resolution as can be viewed in the following equation:

$$\Delta f_{out,res} = \frac{t_d}{T_v}.f_{ref} \tag{2.20}$$

In our model, $t_d = 30ps$ and $f_{ref} = 13MHz$. For example, for Bluetooth applications, we take the output frequency 2.4GHz, then we have a frequency resolution $\Delta fout, res = 936kHz$.

2.4.3 TDC phase noise

The resolution of the used TDC is equal to the inverter delay time t_d and this affects the closed loop phase noise performance. The variance σ_t of this error is given by $\sigma_t^2 = t_d^2/12$, and the phase error then can be obtained from $\sigma_\phi = 2\pi\sigma_t/T_v$.

The TDC phase noise is uniformly distributed over the frequency band from dc to reference frequency f_{ref}, and it can be written as:

$$L(\Delta\omega) = \frac{\sigma_\phi^2}{f_{ref}} = \frac{(2\pi)^2}{12}\left(\frac{t_d}{T_v}\right)^2 \frac{1}{f_{ref}} \tag{2.21}$$

This phase noise depends on the reference frequency and it is filtered by the closed loop. In our TDC, this resolution is equal to 30ps, the frequency oscillation is equal to 2GHz, and the reference frequency is equal to 13MHz. Therefore, the power spectral density of phase noise is equal to $-90dBc/Hz$. This noise is low pass filtered by the closed loop transfer function as we will see in section 2.7.2.2.

2.5 The DCO model

Although a digital control word is applied, the oscillator output signal is always continuous and can be written as

$$v(t) = A\cos(\int_0^t \Phi(t)dt) = A\,cos(\int_0^t (2\pi f_{out})dt + \varphi(t)) \tag{2.22}$$

where $\Phi(t)$ is the instantaneous phase of the oscillator waveform, f_{out} is its output frequency, and $\varphi(t)$ is its phase noise and it is supposed to be linear time variant. The phase

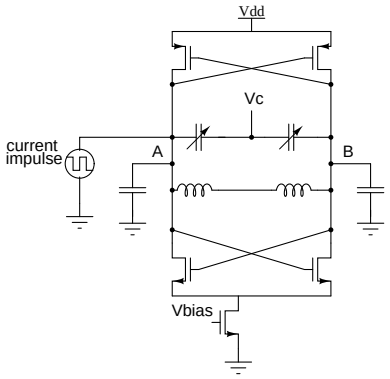


Figure 2.8: The LC oscillator of the ADPLL

$\varphi(t)$ will be expressed in function of the impulse sensitivity function ISF of the oscillator, see section 2.5 and f_{out} varies with the variation of the digital tuning word $\hat{d}[k]$ according to the following equation

$$f_{out} = f_c + \Delta f = f_c + K_{DCO}.\hat{d}[k] \tag{2.23}$$

where f_c is the central frequency, and the DCO gain K_{DCO} is defined by the frequency variation Δf responding to a variation of one LSB of its input the Oscillator Tuning Word OTW. The phase error $\phi_E[k]$ is expressed relatively to the reference frequency f_{ref}, while the oscillation tuning word $\hat{d[k]}$ is calculated in units of the DCO gain K_{DCO}. So a normalization block f_{ref}/K_{DCO} is added in order to represent the phase error $\hat{d}[k]$ in units of K_{DCO}, see fig.2.9.

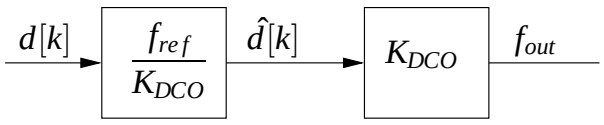


Figure 2.9: The block diagram of the DCO model

2.5.1 Noise modeling

Two types of noise sources exist in LC oscillators. The first one is the thermal noise that comes from the parasitic resistances of the inductor and transistors and this noise is white. The second type of noise is the flicker noise that comes from the NMOS and PMOS transistors and this noise has 1/f behavior, see fig.2.10. In this figure, we see the result of noise analysis of the LC oscillator. The corner $\omega_{1/f}$ is viewed at frequency 3MHz.

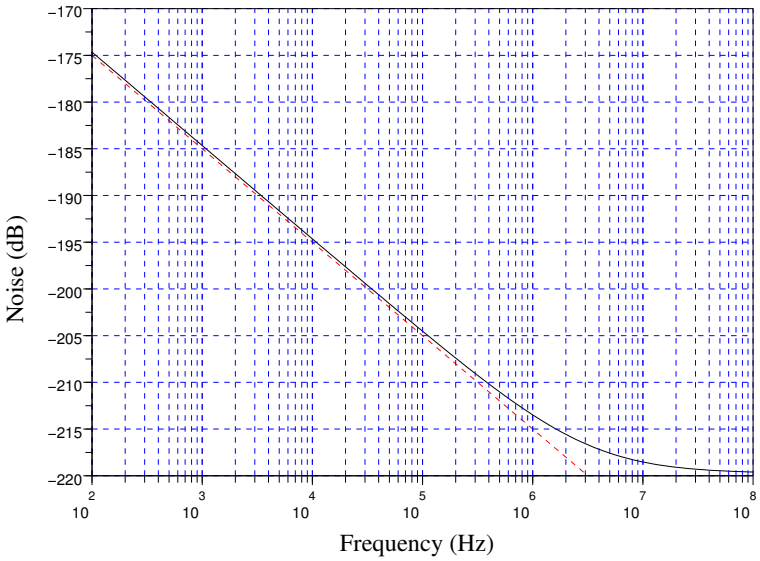


Figure 2.10: The CMOS noise of the LC oscillator. This is the result of Spectre analysis

2.5.1.1 The white noise generator

Thermal noise is modeled by a pseudo random number generator with uniform spectral density and Gaussian distribution (0,σ^2). In VHDL-AMS we used the function *uniform* in the IEEE.math_real.all library. This function generates random numbers of uniform distribution in]0,1[. Thus, by applying the Box Muller method [67] we generate random numbers of Gaussian distribution from random numbers of uniform distribution]0,1[by using the equation

$$Z = \sqrt{-2.\sigma^2.ln(Y_1)}cos(2\pi Y_2) \tag{2.24}$$

where (Y_1, Y_2) are random numbers uniformly distributed in]0,1[, and Z is the random number generated with Gaussian distribution $(0, \sigma^2)$.

To adjust the value of σ^2 we consider the Pnoise[2] simulation results in the $1/f^2$ phase noise region. We can choose any point in this spectrum region to compare it with our VCO model results of phase noise at the same point. We choose the phase noise at 600 kHz from carrier frequency because it is considered as a requirement point in GSM standard.

[2]http://www.cadence.com/Community/blogs/rf/archive/2009/05/01/enhanced-pnoise-algorithm-to-compute-phase-noise-for-vcos-with-bandgap-voltage-reference.aspx

According to *Pnoise* the phase noise at this point is equal to -121 dBc/Hz. We compare this value with the value obtained from the phase noise of our DCO model. We executed many iterations for different values of σ^2 to achieve this phase noise level.

2.5.1.2 The flicker 1/f noise generator

The $1/f$ noise region is modeled by the sum of several signals issued by the filtering of white noise, which is filtered by first order low-pass filters [64], see fig.2.11. Each IIR filter h_k has an infinite impulse response which is defined by the equation 2.25.

$$y_k[i] = (1 - a_k)y_k[i-1] + a_k A^{-(k-1)}x[i] \tag{2.25}$$

where k is the filter index, $x[i]$ is the white noise with normal distribution N(0,1) and it

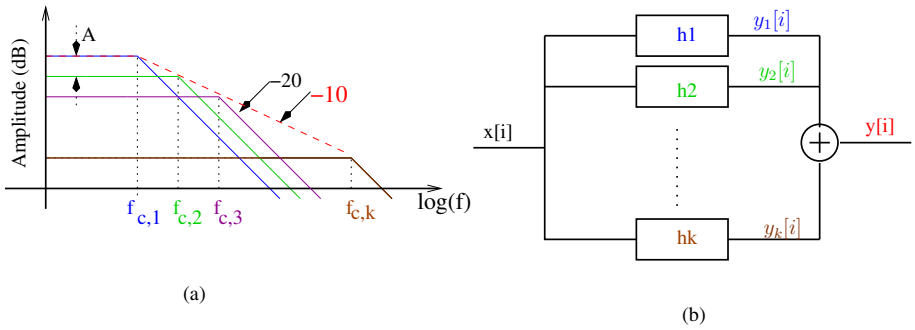


Figure 2.11: (a): Composition of -10 dB slope from low-pass responses of -20 dB slopes. (b): The generated 1/f noise signal from the sum of low-pass filtered white noise signals

is modeled by Box-Muler method that is described previously in section 2.5.1.1, a_k can be calculated from equation 2.26 and A is the linear attenuation of each filter that can be calculated from equation 2.27.

$$a_k = 2\pi \frac{f_{c,k}}{f_s} \tag{2.26}$$

The value f_s is the common sampling frequency. Each filter shapes a different region of the noise spectrum to provide a composite output having the desired 1/f response of slope -10 dB/decade.

$$slope = \frac{A_{dB}}{r} \tag{2.27}$$

A_{dB} is the attenuation in dB of all filters. Each filter has a cutoff frequency $f_{c,k}$ and r is the ratio of two neighboring frequencies as viewed in the next equation:

$$r = \frac{f_{c,k+1}}{f_{c,k}} \tag{2.28}$$

In our implementation the sampling frequency f_s is equal to 300 MHz and we have five filters of 3-dB cutoff frequencies at $f_{c,1}$=300 Hz, $f_{c,2}$=3 kHz, $f_{c,3}$=30 kHz, $f_{c,4}$=300 kHz, and $f_{c,5}$=3 MHz. The obtained noise spectrum has a $1/f$ behavior from 300 Hz to 3 MHz,

so the $\omega_{1/f}$ corner point is viewed at 3 MHz. After this point the noise spectrum has a $1/f^2$ behavior, and peaks are viewed at the sampling frequency f_s. In [64], the authors propose to implement an anti-aliasing filter at the output of the filters in order to eliminate the peaks viewed at multiples of sampling frequency. In our implementation we are not interested in frequencies superior to 10 MHz in phase noise spectrum, so for simplicity reasons we have f_s equal to 30 MHz and we do not use the anti-aliasing filter.

2.5.2 Phase noise modeling

The Linear Time Variant model of phase noise that is presented by Hajimiri and Lee [38] is used in a DCO behavioral model. This model of phase noise depends on the Impulse Sensitivity Function ISF of the oscillator and predicts the phase noise in the close-in phase noise region and $1/f^2$ region. In addition, it predicts the displacement of the $1/f$ corner to a new $1/f^3$ corner which depends on the ISF function. This function is periodic, and then it can be described by its Fourier transform coefficients C_n like in the following equation:

$$\Gamma(\omega_{out}\tau) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n cos\left(n\omega_{out}\tau + \theta_n\right) \tag{2.29}$$

where $\Gamma(\omega_{out}\tau)$ is the ISF function, τ is the injection time. Using the expression of $\Gamma(\omega_{out}\tau)$ we can write the phase $\varphi(t)$ with the equation

$$\begin{aligned}\varphi(t) =& \frac{1}{q_{max}}.[\frac{C_0}{2}\int_0^t i(\tau)d\tau + \\ & \sum_{n=1}^{\infty} C_n \int_0^t i(\tau)\, cos(n\omega_{out}\tau)\, d\tau]\end{aligned} \tag{2.30}$$

where $i(t)$ is the noise source that is injected at the output node of the oscillator.

As we mentioned above, the modelled oscillator has a cross coupled LC resonating circuit, so the noise sources in the circuit are the parasitic resistances and the CMOS transistors. The noise power spectral density has two regions, 1/f noise that comes from active elements and white noise. The corner point is named $\omega_{1/f}$ as mentioned before. This noise source $i(t)$ can be modelled by the sum of $1/f$ noise source and white noise source.

Once the phase $\varphi(t)$ have been calculated, the DCO output signal can be easily determined from equation 2.22. The $v(t)$ signal in this model carries all the information on the phase noise of the oscillator. Then, the digital CKV signal can be obtained by passing the continuous $v(t)$ signal through a comparator. Thus, the complete model is presented in fig.2.1.

2.5.3 Determination of the ISF

For the DCO model we chose the LC oscillator of fig.2.8. This oscillator is designed in 90 nm CMOS process and it is optimized to have -121dBc/Hz@600kHz phase noise. Its

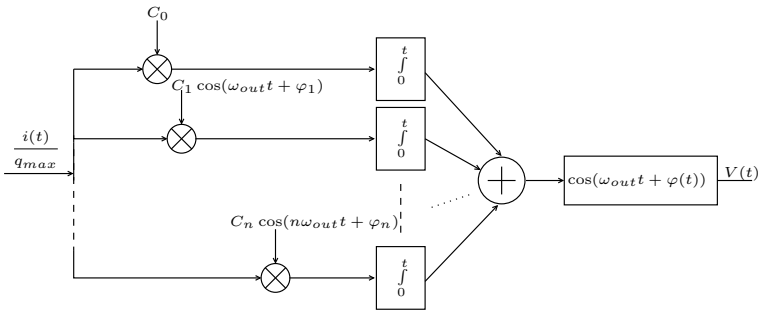


Figure 2.12: The DCO phase noise model

design strategy is presented in the appendix A for reading convenience. In section 2.5.4 we present the Pnoise behavior for this oscillator.

Exact analytical derivations of the ISF are usually not obtainable for any but the simplest oscillators. Various approximation methods are outlined in [38] and [68], but the more accurate method is generally the direct evaluation of the time-varying impulse response. In this direct method, an impulse is injected at different relative phase of the oscillation period and the oscillator is simulated for a few periods afterwards, see figure 2.13. By measuring the time shift Δt of the zero crossing of oscillation signal caused by the injection we can calculate the phase shift $\Delta\varphi$ results by the injection $\Delta\varphi = 2\pi\Delta t/T$, where T is the oscillation period. By sweeping this procedure on one oscillation period, we measure the phase shift resulting from an injection at every time of oscillation period.

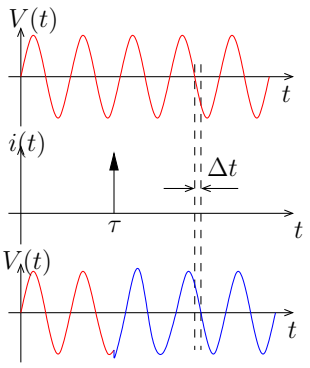


Figure 2.13: An impulse is injected at time τ and the resulting shift Δt of zero-crossing is calculated few periods afterwards

An implementation with Scilab[3] is used to sweep the waveform automatically, see figure 2.14. SciLab is used to make an interface command between the designer and the electrical simulator Spectre and it is a good environment for numerical calculations. The simulated oscillator is the cross coupled LC oscillator of the fig.2.8. The netlist of the oscillator is

[3] http://www.scilab.org/

first created under the Cadence[4] environment. In this netlist, we define the source current parameters that are the amplitude and the injection time. The impulse current source is injected at the output node of the oscillator. The total amount of injected charge is 0.1pC

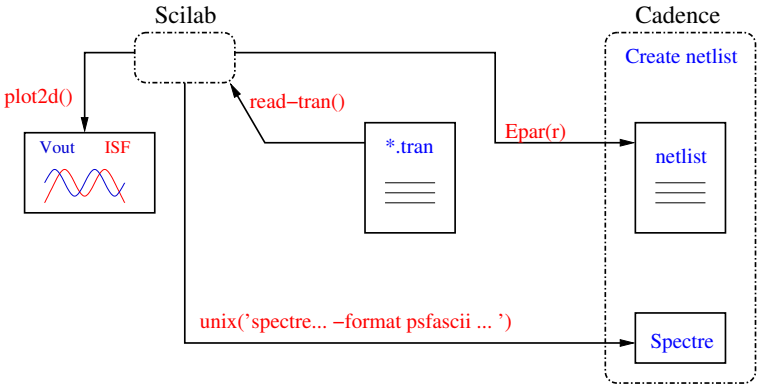


Figure 2.14: The automatic implementation of the ISF between Spectre and Scilab

corresponding to $\Delta V = 50mV$. Anyway, the charge displacement on the output node caused by the injection depends on the current source amplitude but it would not change the linearity of the phase noise response. We know that the excess phase response to charge injection is linear if the quantity of charge injection on the node is less than 10% of the total charge on the effective capacitance of the node of interest [38]. The oscillation period is known in Scilab and then Scilab controls the execution of the transient analysis by Spectre. The injection time parameter is increased before every transient analysis by a step to cover one oscillation period. Then, we determine the time shift of the zero crossing point few periods afterwards and we measure the resulting phase shift. Since we measure the phase shift a few periods after the injection period, the simulation time for one injection point is the time that Spectre takes to finish its transient analysis. So, the time spent to measure the ISF values depends on the number of injection points within a period; the increase of the number of injection points increases the number of iterations and then the simulation time. In our simulation the impulse current injection time parameter is increased by 1ps to cover the period $T_{out} = 1/f_{out} = 1/2GHz = 0.5ns$. The total number of points for the ISF function is 500 points per period.

The result of the simulation is shown in fig. 2.15. We see in this figure the oscillation period with the ISF values. In addition, it can be viewed that the maximum phase variations, i.e. the maximum ISF values are near the zero crossing values of the oscillation waveform.

The Fourier transform coefficient values of this ISF are listed in table 2.2 and we discus in next section the phase noise behavior of this oscillator. We list in this table the first four coefficients because the remained ones are negligibles.

[4]http://www.cadence.com/us/pages/default.aspx

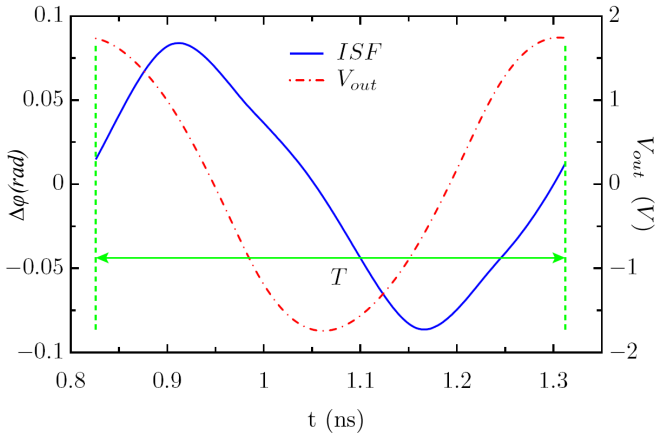


Figure 2.15: The ISF function of the LC oscillator

Table 2.2: The Fourier transform coefficients of the LC oscillator designed in 90nm

C_0	C_1	C_2	C_3
6.99e-3	5.7e-2	6.04e-3	6.04e-3

2.5.4 Comparison between Spectre and LTV model

The LTV equations of phase noise model in the $1/f^2$ and $1/f^3$ regions and the position of ω_{1/f^3} corner in the frequency spectrum are respectively repeated for reading convenience:

$$L(\Delta\omega) = 10.\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}.\sum_{n=0}^{\infty} C_n^2}{4q_{max}^2\Delta\omega^2}\right) \tag{2.31}$$

$$L(\Delta\omega) = 10.\log\left(\frac{C_0^2}{q_{max}^2}.\frac{\overline{i_n^2}/\Delta f}{8.\Delta\omega^2}.\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2.32}$$

$$\omega_{1/f^3} = \omega_{1/f}.\left(\frac{C_0}{2\Gamma_{rms}}\right)^2 \simeq \omega_{1/f}.\frac{1}{2}\left(\frac{C_0}{C_1}\right)^2 \tag{2.33}$$

Since the ISF has been determined, its Fourier transform coefficients C_n are calculated and the LTV model is ploted from the equations that are listed before. In addition, the ω_{1/f^3} corner is determined at $30kHz$. The noise analysis result of the DCO circuit is viewed in fig.2.10. Wherein, the noise corner $\omega_{1/f}$ is viewed at 3MHz. On the other side, Pnoise analysis result of figure 2.16 shows that ω_{1/f^3} is observed at $30kHz$ thus a reduction factor of 100.

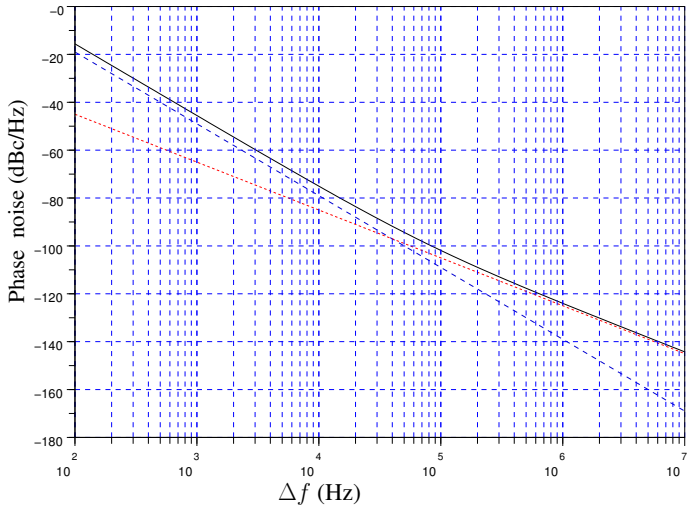


Figure 2.16: Simulation results of Pnoise analysis in solid line. The $1/f^2$ and $1/f^3$ phase noise estimation by the LTV model in dash lines. The ω_{1/f^3} corner is viewed at 30kHz.

According to table 2.2 and to equation 2.33, the prediction of displacement of ω_{1/f^3} corner in the LTV model is in conformity with Spectre analysis.

2.6 VHDL-AMS simulation results

The complete model of the ADPLL is implemented using VHDL-AMS. The phase detector block is composed of the FCW accumulator, the CKV clock counter and the TDC block. We use a digital filter of zero order in the loop with gain α. Then, this is a model of a first order ADPLL. The influence of the value of α on the closed loop time response is viewed in section 2.6.1. Because of the digital nature of the input and output signals in the phase detector it can be implemented using VHDL language. On the other hand, the DCO has a continuous waveform according to equation 2.22. The use of VHDL-AMS language ensures the portability of our model, and the rapidity in execution.

This simulation main objective is the validation of the ADPLL phase noise performance in the presence of TDC and DCO noise. The generic parameters of the model are the ISF Fourier transform coefficients C_n, the DCO gain $K_{DCO} = 23kHz$, the delay time of one inverter and the frequency control word FCW. The ADPLL model is simulated for a RF application that has a carrier frequency around 2.4 GHz (ex: Bluetooth). The DCO has a central frequency of 2.44 GHz, and a linear tuning range in [2.4,2.49] GHz. The reference frequency is equal to 13 MHz. In the TDC block, the inverter propagation delay is equal to 30 ps and the number of needed inverters is equal to 14.

2.6.1 ADPLL transient simulation

The results of the transient analysis of the ADPLL model is presented in figure 2.17. The low pass filter of the loop is zero order and its attenuation $\alpha = 1/10$ for this simulation. The desired frequency is 2.45 GHz and it is reached after $5\mu s$. This time varies with α as can be seen in figure 2.18.

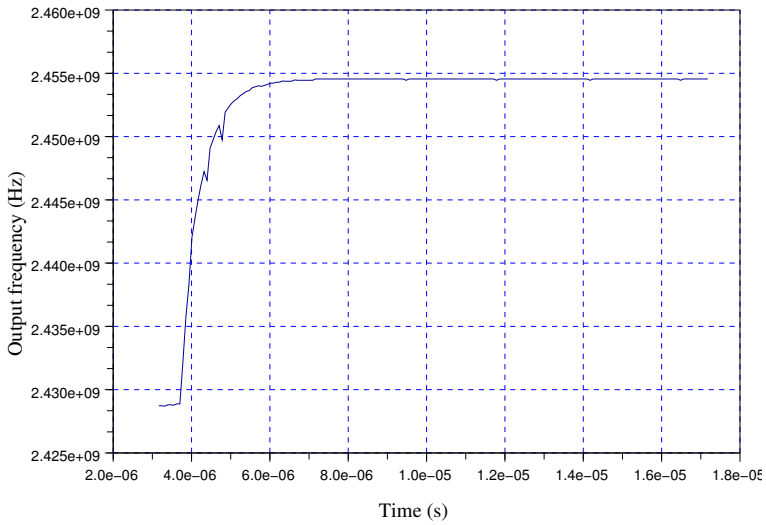


Figure 2.17: Transient simulation of the VHDL-AMS model of ADPLL. The lock time is equal to $5\mu s$

In this figure the ADPLL is simulated with three different values of α (1/2, 1/4, 1/10). The x axis is the simulation time and the y axis is the phase difference ϕ_E. We see in this figure that the lock is faster with the great value of α. Therefore, it is interesting to begin the simulation with a great value of α (1/2 for example) then decrease it to obtain a fine resolution output frequency. In section 2.7.1 we see the influence of α on the bandwidth of the ADPLL.

2.6.2 DCO phase noise performance

The modeled DCO phase noise is calculated from the transient simulation where the output result is the continuous time signal of equation 2.22. This signal $v(t)$ is high frequency sampled and the zero crossing instants of the rising edges are obtained by an interpolation of first order. Then, the mean period T_{out} is calculated from the equation:

$$T_{out} = \frac{1}{N}.\sum_{i=0}^{N}(t(i+1) - t(i)) \tag{2.34}$$

The periodic jitter is then obtained as the error on T_{out} by:

$$e_j = t(i) - i \times T_{out} \tag{2.35}$$

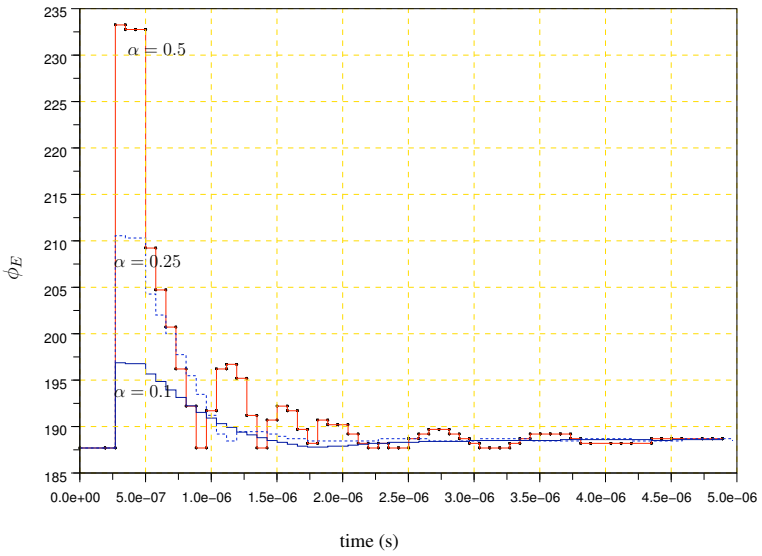


Figure 2.18: Variations of the ADPLL time response with the attenuation α

The resulting phase error from this jitter is obtained from the general time to phase conversion equation:

$$e_\phi = 2\pi \frac{e_j}{T_{out}} \tag{2.36}$$

The power spectral density of e_ϕ is then calculated by Scilab function *cspect* with 2^{19} points and the result is viewed in 2.19. The DCO phase noise has two regions $1/f^2$ and $1/f^3$ regions. The corner ω_{1/f^3} is viewed at 30 kHz. This result is in agreement with Pnoise result presented in figure 2.16.

The main contribution of the use of the LTV model while Pnoise gives us the same phase noise performance of the oscillator, is the simulation time. For the LC oscillator of figure 2.8, simulation time of transient analysis with Spectre is equal to 1 s for five periods against 10ms with our VHDL-AMS model. This time will be highly augmented if we simulate a more complex system such as ADPLL

2.7 ADPLL frequency response

Since the input/output signals of the ADPLL blocks are discrete time samples, a discrete z model of the ADPLL is significant. In this section we develop a z-model of ADPLL, and we determinate the noise contributions in the ADPLL phase noise. Concerning the noise, the VHDL-AMS model that is previously presented is a predictive model of ADPLL while the following model is a descriptive one.

2.7.1 z-domain model response

The phase information is normalized to the clock period T_v, then the reference phase $\Theta_r(z)$ is calculated from accumulating the FCW at the reference clock rising edge, and

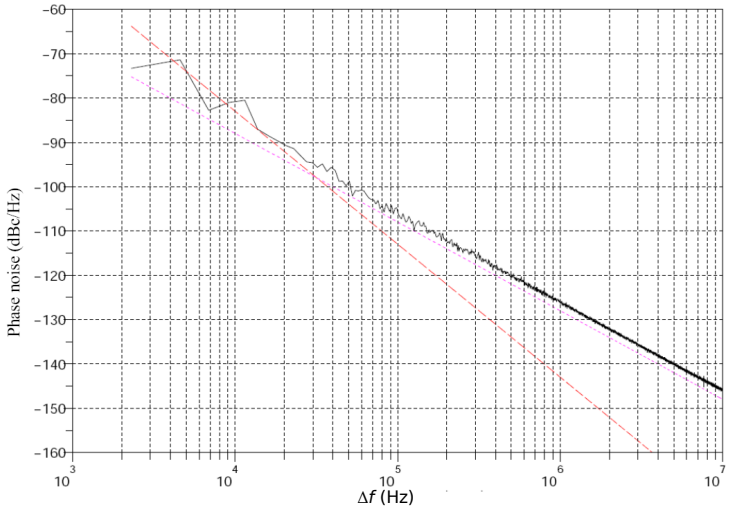


Figure 2.19: The power spectral density of DCO phase noise. The ω_{1/f^3} point is observed at 30kHz

the variable phase $\Theta_v(z)$ is calculated by accumulating one at the CKV rising edge. In the real ADPLL the phase comparator operates at the reference clock. Thus, during one reference period T_r, the variable phase accumulates the actual ratio $\frac{T_r}{T_v}$. The digital loop filter has a gain factor α and the phase error is expressed in reference frequency units so it is multiplied by f_{ref}/K_{DCO}. The output frequency is expressed in function of the DCO gain as in the equation 2.23. If the output frequency is superior to the central frequency, then its period is inferior to the central period as we can see in the following equations:

$$f_{out} = f_c + \Delta f \tag{2.37}$$

$$T_{out} = T_c - \Delta T = \frac{1}{f_c + \Delta f} = T_c \frac{1}{1 + \Delta f / f_c} = T_c(1 - \Delta f / f_c) \tag{2.38}$$

$$\Delta T = T_c^2 \Delta f \tag{2.39}$$

ΔT is the offset of the output signal period from central signal period and Δf is the offset of the output frequency from central frequency and it can be expressed in function of the K_{DCO} as can be seen in the equation:

$$\Delta f = K_{DCO} \hat{d}[k] \tag{2.40}$$

The time offset ΔT is then expressed in function of K_{DCO} and T_c^2 as

$$\Delta T = K_{DCO}.T_c^2.\hat{d}[k] \tag{2.41}$$

We normalize by the instantaneous period T_v:

$$\frac{\Delta T}{T_v} = \frac{1}{T_v} K_{DCO} T_c^2 \hat{d}[k] \tag{2.42}$$

Finally, the model can be viewed in fig.2.20, and the open loop transfer function is given by the following equation:

$$H_{ol}(z) = \frac{\Theta_v}{\Theta_r} = \alpha.\frac{f_{ref}}{K_{DCO}}.\frac{1}{T_v}.K_{DCO}T_c^2.\frac{T_r}{T_v}\frac{1}{1-z^{-1}} \tag{2.43}$$

Thus, the open loop transfer function can be written as:

$$H_{ol}(z) = \alpha.\frac{T_c^2}{T_v^2}.\frac{1}{1-z^{-1}} \tag{2.44}$$

and the closed loop transfer function is:

$$H_{cl}(z) = \frac{H_{ol}}{1+H_{ol}} = \frac{\alpha.T_c^2/T_v^2}{1-z^{-1}+\alpha T_c^2/T_v^2} \tag{2.45}$$

We define z as $z = e^{j\omega T_r}$ and T_r is the reference period. For low frequencies, where $f \ll f_{ref}$, $z^{-1} = e^{-j\omega T_r}$ can be simplified:

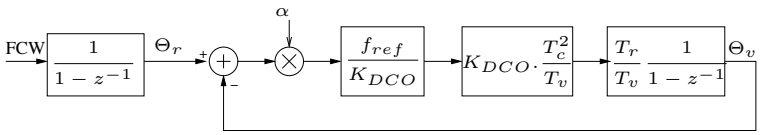


Figure 2.20: The linear Z model of first order ADPLL

$$z^{-1} = e^{-j\omega T_r} \approx 1 - j\omega T_r \tag{2.46}$$

By replacing z^{-1} in the closed loop transfer function and rearranging it, we can obtain the frequency transfer function:

$$H_{cl}(f) = \frac{\alpha.T_c^2/T_v^2}{\alpha T_c^2/T_v^2 + j\omega T_r} \tag{2.47}$$

The closed loop transfer function is a low-pass filter with 3-dB cutoff frequency f_{co} which is given by:

$$f_{co} = \frac{\alpha.f_{ref}}{2\pi}\frac{T_c^2}{T_v^2} \tag{2.48}$$

We can notice that the loop bandwidth depends on the loop filter gain α, and then it will be reduced when $\alpha < 1$. This model will be completed afterwards by the noise sources in the loop.

2.7.2 Noise sources and contributions

There are two internal noise sources in the ADPLL. The TDC and the DCO. We name the former $\phi_{n,TDC}$ and the later is named $\phi_{n,DCO}$. The z-time loop model with noise sources can be viewed in the fig.2.21.

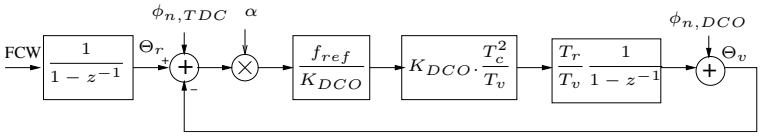


Figure 2.21: The ADPLL model with noise

2.7.2.1 The DCO noise

This noise $\phi_{n,DCO}$ comes from the oscillator itself and it depends on the oscillation circuit design. It undergoes a high-pass filtering of equations 2.49 and 2.50 with 3-dB cutoff frequency f_c that is given by equation 2.48.

$$H_{cl,DCO}(z) = \frac{1}{1+H_{ol}(z)} = \frac{1-z^{-1}}{1-z^{-1}+\alpha.T_c^2/T_v^2} \tag{2.49}$$

$$H_{cl,DCO}(f) = \frac{j\omega T_r}{\alpha.T_c^2/T_v^2+j\omega T_r} = \frac{1}{1-j\frac{\alpha.T_c^2/T_v^2}{\omega T_r}} \tag{2.50}$$

Considering only the tracking mode of the ADPLL, $\alpha = 1$, $f_{ref} = 13\ MHz$, $T_v = 409.165\ ps$ and $T_c = 409.836\ ps$, the cut-off frequency is about 2 MHz while corner point ω_{1/f^3} for the same DCO is observed at 300 KHz (Pnoise results of Spectre). In figure 2.22 the DCO phase noise in the $1/f^3$ and $1/f^2$ regions is plotted with dot line, ω_{1/f^3} is the $1/f^3$ corner. The high-pass filter is plotted with dash line, and the phase noise at the output of the ADPLL in the presence of the DCO phase noise is plotted with solid line. It contains three regions, $1/f$ region, plate region, and $1/f^2$ region.

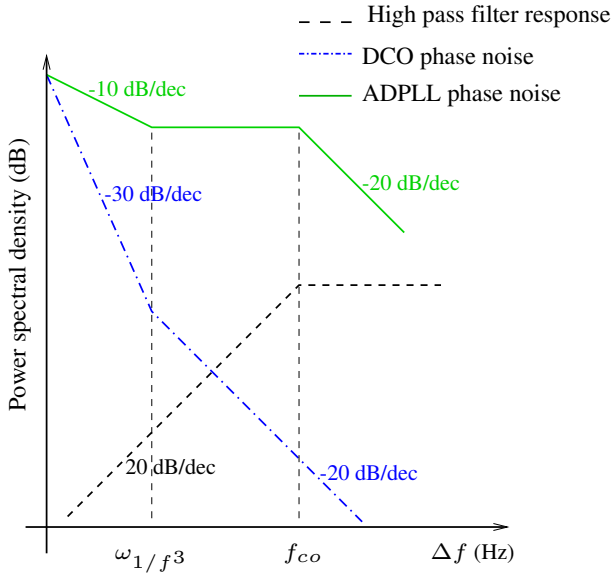


Figure 2.22: The ADPLL phase noise transfer function of DCO noise

2.7.2.2 The TDC noise

TDC noise $\phi_{n,TDC}$ is derived in section 2.4.3. It has a uniform spectrum level that is equal to -100 dBc/Hz. This noise is low-pass filtered by the closed loop transfer function given by equation 2.51. The cut-off frequency of the filter is the same f_{co} given by equation 2.48.

$$H_{cl}(f) = \frac{1}{1 + j\omega T_r / \left(\alpha T_c^2 / T_v^2\right)} \tag{2.51}$$

2.7.3 ADPLL phase noise performance

According to equation 2.48, the cut-off frequency f_c of the ADPLL is near 2 MHz. The ω_{1/f^3} corner is around 30 kHz (see figure 2.19). Then the three regions of the expected phase noise of the ADPLL are plotted in figure 2.23 with dash line. The phase noise at the ADPLL model output is calculated from the steady state regime by the same method used in section 2.6.2 and it is plotted also in figure 2.23. We see in this figure that ADPLL phase noise has respectively the asymptotic $1/f$, flat, and $1/f^2$ behavior. We view in fig.2.19

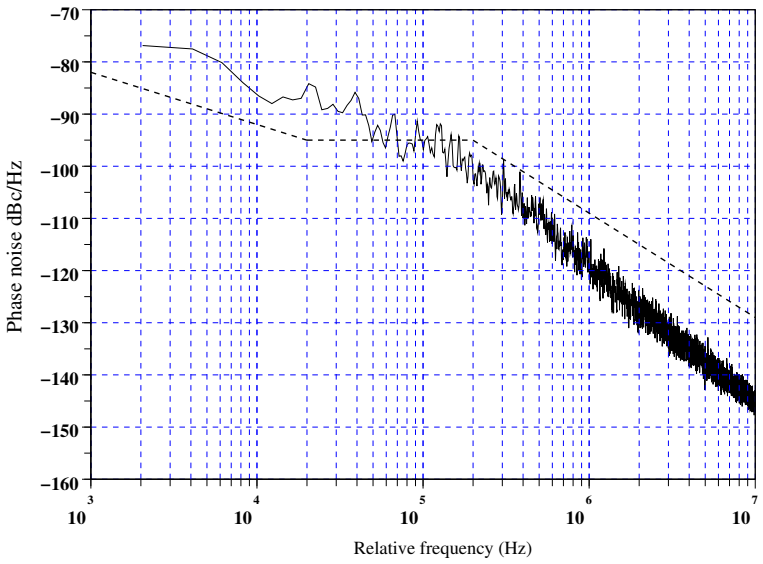


Figure 2.23: The power spectral density of RF output signal of the ADPLL

and fig.2.23 that the number of points in the close-in phase noise is not enough to observe clearly the level of the phase noise spectrum, and increasing this number is not possible since it exceeds the memory of the employed machine.

In summary, the presented model predicts the phase noise behavior of the ADPLL in the existence of DCO and TDC noises. These noise sources are treated separately in the model. The DCO model based on the ISF Fourier transform coefficients of the DCO. Taking into account the linear time variations of DCO phase noise, the resulting model is considered as accurate as electrical simulators such as Spectre. The main contribution of this model is the simulation time. It is 100 times faster than Spectre transient analysis.

The DCO model is valid for all DCO architectures since the Fourier transform coefficients are generic parameters of the model and they could be replaced for other DCO designs. The TDC quantification noise is also treated in the model. It depends on the delay time of inverter gate that is treated as generic parameter of the model. This delay time depends on the technology of fabrication and it is decreased with technology progress.

2.8 Summary

Phase noise constitutes a real obstacle in ADPLL modeling. In this chapter we propose a behavioral model of ADPLL with phase noise. Within, we presented the implementation of the LTV model of oscillator's phase noise in the ADPLL model. The LTV model of phase noise is based on the ISF function of the oscillator. The ISF describe rigorously the oscillator response to noise injection. The Fourier transform coefficients of the ISF are generic parameters in the model. So, for another DCO design, just these coefficients have to be replaced by that of the new design. The model is portable to any application and to any technology process since the generic parameters could be simply modified. The TDC quantification noise is also treated in the model. It depends on the delay time of inverter gate that is treated as generic parameter of the model. This delay time depends on the technology of fabrication and it decreased with technology progress. Therefore, the ADPLL model simulates precisely the DCO and the TDC noise contributions in the ADPLL phase noise performance. The use of VHDL-AMS provides the rapidity of execution time. We said in 2.6.2 that the run time of the behavioral model of the DCO is 100 time faster than Spectre transient analysis. Regarding this difference of speed of execution time, the total model of the ADPLL is also faster than electrical simulators. In addition, the variation of the lock time in function of the attenuation constant of the loop filter is viewed. We presented also the noise contributions in the ADPLL phase noise in a z-transform model. This model is descriptive and it could be used in models of more complex system such as the radio receiver.

Chapter 3

ADPLL design for TV applications

Recently, the increasing interest in watching TV in a mobile environment makes it necessary to integrate TV on a hand-held device. The traditional RF front-end blocks of TV receiver are not appropriate for a mobile device, because of their high power consumption and large components area. Thus, in order to integrate TV receiver into a mobile device, power consumption and size should be reduced dramatically. The System on Chip (SoC) technology, which integrates all of the functional blocks including the digital part on a single chip, can be the best solution for those requirements.

One of the main blocks of TV receiver is the LO. It is presented in the literature as intensively analog block (classic PLL) that occupies large area and is less integrable on SoC. The ADPLL on the other hand can provide the good solution that guaranties total integrability of the LO in the radio receiver chip with low area and low power consumption. The challenge of the design of the ADPLL for TV application is achieving a wide frequency range (from 400 MHz to 800 MHz), while ensuring low phase noise.

Here we propose to design an ADPLL with DCO ring oscillator for its large tuning range, low area, scalability with technology advancement. To overcome the general poor phase noise performance of ring oscillators we propose to use the interpolative oscillator with a design strategy based on the ISF function for minimum phase noise with low area and low power consumption. Merged DCO and TDC architecture is also proposed which reduces the ADPLL area and power consumption.

In this chapter we present top-down ADPLL design for TV applications. We start by presenting the ADPLL architecture in section 3.1, next we present the DCO architecture and design strategy in section 3.2. Wherein, the NOR interpolative oscillator is presented. The Digital to Voltage converter is presented in section 3.3. The proposed merged DCO and TDC architecture is presented in section 3.4. The FPGA blocks that operate at FREF rate are presented in section 3.6. The summary of the ADPLL simulated results is presented in section 4.1.

3.1 Architecture and specifications

We present in this section the architecture of ADPLL designed for TV applications. The comparison between different architectures of ADPLL in terms of tuning range, phase noise performance, area, and power consumption is viewed in chapter 1. We saw that unlike the other presented ADPLL, the ADPLL architecture of [3] is able to cover Bluetooth,GSM, and 3G applications by architectural and circuit enhancements improving the modulation capability. Thus, we opt for this architecture in our TV application.

3.1.1 ADPLL architecture

The proposed ADPLL is based on the ADPLL proposed by [3] and its block diagram is viewed in figure 3.1. Unlike the ADPLL of [3], the proposed one has a DCO ring oscillator and a merged DCO and TDC architecture. However, it contains a digital phase comparator, a digital counter for the variable phase, digital accumulator of FCW. A look-up table containing the control words of the DCO is used. The ADPLL is divided into two parts: the first one operates at radio frequencies and it is integrated on CMOS 65nm circuit, and the second part operates at reference frequency and it is programmed on FPGA. The $\Sigma\Delta$ modulator is used to increase the frequency resolution of the ADPLL.

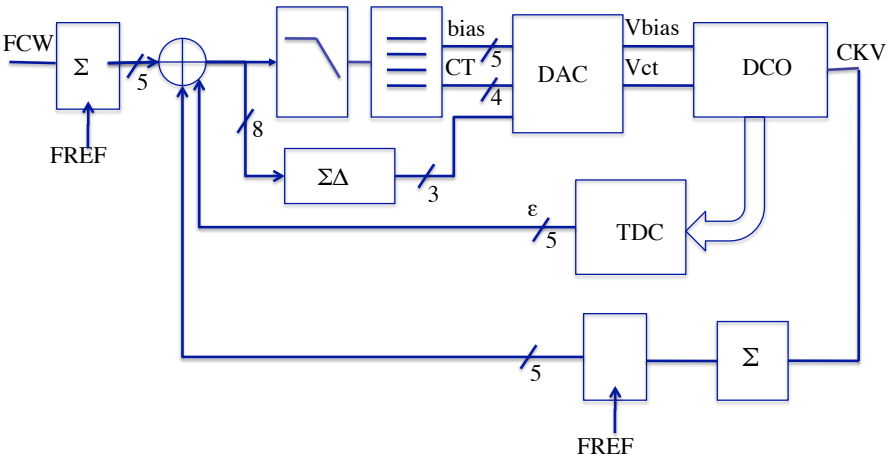


Figure 3.1: The proposed architecture of ADPLL designed for TV applications

3.1.2 TV application specifications

The designed LO is placed in the TV receiver as can be seen in figure 3.2[1]. Wherein, the RF front-end of the TV receiver consists of Low Noise Amplifier LNA, mixer, Low Pass Filter, amplifier and then Analog to Digital Converter. The RF signal arrives from

[1]Yann Le Guillou, RF synthesizers specifications for TV receiver. NXP semiconductors, Caen, France, 2007

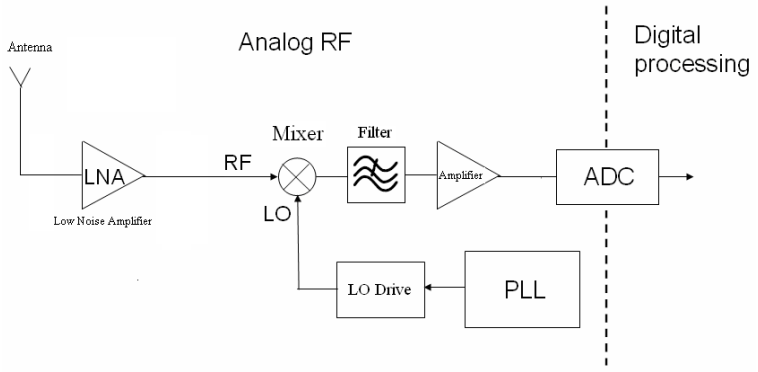


Figure 3.2: RF front-end of TV receiver

antenna with frequency ranges from 174MHz to 230MHz (VHF band) and from 470MHz to 862MHz (UHF band) for Digital Video Broadcasting terrestrial TV (DVB-T) application.

It has -115dBc/Hz at 5 MHz offset from carrier frequency and -128dBc/Hz at 8 MHz from carrier[2]. Since DCO phase noise has a slop equal to -20dB/decade at this offset from carrier frequency (in general ω_{1/f^3}<1MHz). This means that the oscillator have to be designed to have <-115dBc/Hz at 5MHz offset.

3.1.3 ADPLL circuit implementation

The maximum frequency of the oscillator output is equal to 800MHz, and the reference frequency is f_{ref} =26 MHz, Then, the maximum value of the Frequency Control Word FCW_{max} is given by the equation:

$$FCW_{max} = \frac{f_{max}}{f_{ref}} = 30.769 \tag{3.1}$$

Where f_{max} is the maximum frequency of the DCO output. The integer part of FCW is then coded over 5 bits and the fractional part is designed for 100kHz frequency resolution and it is coded over 8 bits. The resolution is then calculated like the following equation

$$\delta f_{min} = \frac{800MHz}{2^5.2^8} = 97.656kHz \tag{3.2}$$

The designed ADPLL has a zero order low pass filter, thus it is a first order ADPLL. We see in section 2.7.1 that the ADPLL bandwidth is determined by the cut-off frequency given by the equation:

$$f_{co} = \frac{\delta f_{min}}{2\pi} \tag{3.3}$$

According to this equation, the ADPLL bandwidth is around f_{co}=16 kHz. Since the DCO phase noise has to have -120dBc/Hz@5MHz from carrier frequency and the ADPLL phase

[2]Yann Le Guillou, RF synthesizers specifications for TV receiver. NXP semiconductors, Caen, France, 2007

noise has -20dB/decade for frequencies higher than f_{co}, we obtain the phase noise level of -70dBc/Hz@f_{co} from carrier. This phase noise is the result of the DCO noise only. We said that TDC phase noise is white then the designed TDC has to have a power spectral density of phase noise less than -70dBc/Hz. Therefore, the ADPLL has the phase noise behavior illustrated in figure 3.3.

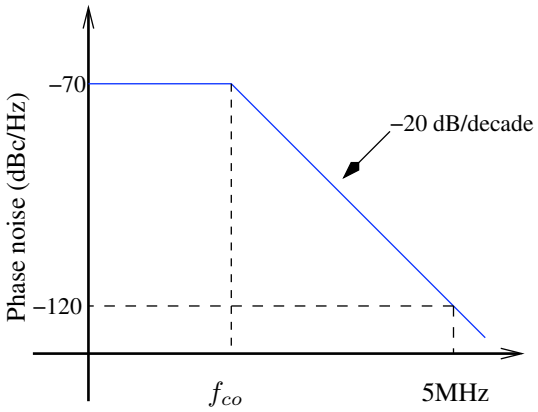


Figure 3.3: Phase noise behavior of first order ADPLL designed for TV application

ADPLL high frequency blocks are fabricated using 65 nm CMOS technology and the low frequency blocks are implemented on Stratix II EP2S60 FPGA. The integrated circuit parts are the DCO, the TDC, the digital counter, the frequency divider, and the output buffer (see figure 3.4). We describe afterwards the design strategy of each block and we describe in section 3.6 the phase comparison part programmed on the FPGA.

The bloc diagram of the circuit is illustrated in figure 3.4. The input signals of the circuit are the DCO control bits (CT and Bias) and FREF. They are all clocked at FREF rising edges for preventing any metastability problem. The output signals are the DCO state register (TDC), the variable phase vector (RV), CKR, CKV and CKV/4.

3.2 DCO Design

We presented in chapter 1 a state of the art of DCO. In this study, we concluded that two main approaches exist in the literature, the hybrid digital control (DAC+VCO) approach like [69] and direct digital control approach like [27, 4]. We opt for the hybrid approach for its significant advantage in that it enables the immediate use of well known and understood VCO and DAC structures with minimal redesign.

In this section we present the followed steps of our choice of interpolative ring oscillator based on NOR cells in 3.2.1. Then, we details the characteristics of this architecture and its benefits for large band TV applications in 3.2.2 and 3.2.3. A design strategy based on the ISF function is presented in 3.2.4. Finally, we summaries the characteristics of the designed oscillator in 3.2.5.

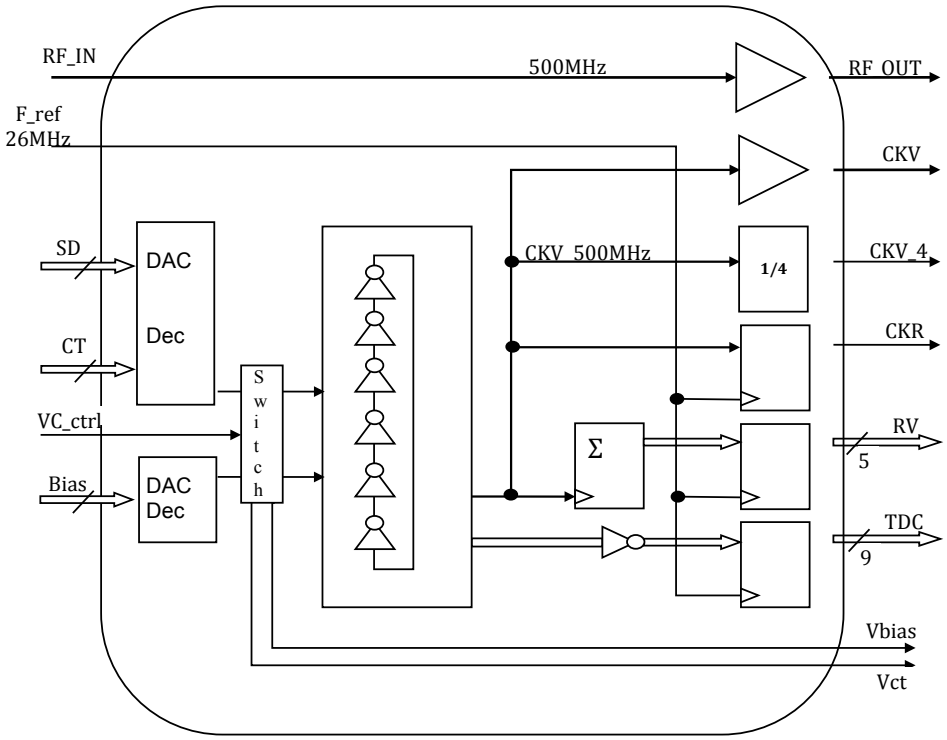


Figure 3.4: Block diagram of the CMOS 65nm part of the ADPLL

3.2.1 Choice of DCO architecture

The tradeoff between LC and ring oscillators is exposed quantitatively by [70]. Within, the author considered only the white noise because the PLL suppresses the flicker noise. He concludes that for the same phase noise performance, 3-stages ring oscillator consumes 450 $\times$ the power consumed by LC oscillator. He added that this comparison is unfair since it considered a very optimized inductor with high quality factor. In addition, it is more and more difficult to design high quality factor inductor with technology progress.

In order to choose the DCO architecture, we compare 4 architectures of VCO: the LC oscillator we designed in the previous chapter see section 2.5, the 5-stages and 15-stages ring oscillator based on inverter gates and NOR interpolative oscillator (see figure 3.9) for frequencies around 2GHz. The comparison is made for two purposes: Firstly, we are interested by comparison between LC and different ring architectures. Secondly, we detail a comparison between ring architectures in terms of: stage design, stages number and its influence on ring performances. The LC oscillator is designed in CMOS 90nm for the ADPLL model presented in chapter 2 according to the design strategy described in the annex A. As for ring oscillators based on inverter gates, see figure 3.6, they are designed by parametrical analysis of Spectre [3] in CMOS 65nm technology following the design strategy presented in 3.2.1.1.

[3] http://www.cadence.com/products/rf/spectre_circuit/pages/default.aspx

3.2.1.1 Design of inverter based ring oscillators

The oscillation period of ring oscillator is generally defined by the time it takes for a transition to propagate twice in the ring. In N stages ring oscillator based on inverter gates, see figure 3.6,this involves N pulldowns by the NMOS and N pullups by the PMOS, resulting in the oscillation frequency f_0 that is given by [70]:

$$f_0 = \frac{1}{N(t_{dN} + t_{dP})} \simeq \frac{2}{NCV_{dd}} \left(\frac{1}{I_N} + \frac{1}{I_P} \right)^{-1} \simeq \frac{I/C}{NV_{dd}} \tag{3.4}$$

where I is the bias current, V_{dd} is the supply voltage, C is the load capacitor of each stage, (t_{dN}, t_{dP}) are the delay times of NMOS and PMOS respectively. The delay time is defined as the time difference between the time when the input crosses the switching threshold of the inverter and the time when its output crosses the middle point V_M of the next inverter as wee see in figure 3.5. In this figure, we see the delay time when the input is an ideal step (figure 3.5). However, the input waveforms in a practical logic chain are not ideal steps but have a finite slope. This slope is the same in the case of a chain of identical stages and in case of CMOS inverters with equal pull-up and pulldown. This led to a refinement

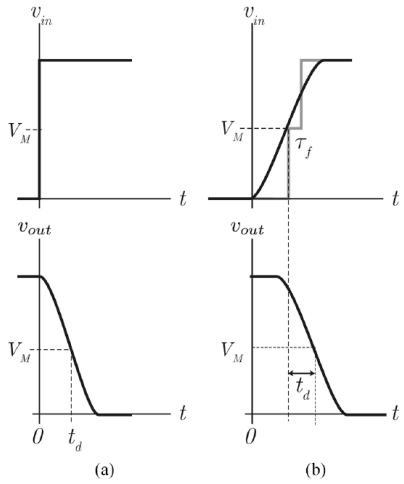


Figure 3.5: Delay times in case of: (a) Ideal step input. (b) Real step input

of the calculation based on step response delay to one which takes into account the finite slope of the input ramp, see figure 3.5.b. In general, for large fanouts, a longer propagation delay is obtained. Yet better estimations of propagation delay continue to be published [71] providing complicated but complete analytical expression for delay, under the assumption that the circuit contains only one NFET, one PFET, and one capacitor. The complexity of these analyses forces designers to continue to use simple estimate based on RC delay for hand calculation, which are refined on timing simulators (see section 3.2.3).

The design variables in the ring oscillator are the NMOS and PMOS dimensions and the design guidelines use the phase noise model of [70] because the measured phase noise is identical to the predicted one for white noise. In this model, phase noise due to white

noise is expressed as

$$L(f) = \frac{2kT}{I}\left(\frac{1}{V_{dd} - V_t}(\gamma_N + \gamma_P) + \frac{1}{V_{dd}}\right)\left(\frac{f_0}{f}\right)^2 \tag{3.5}$$

where k is the Boltzman constant, T is the temperature, I is the bias current, V_{dd} is the supply voltage. V_t, γ_N, and γ_P are technological parameters.

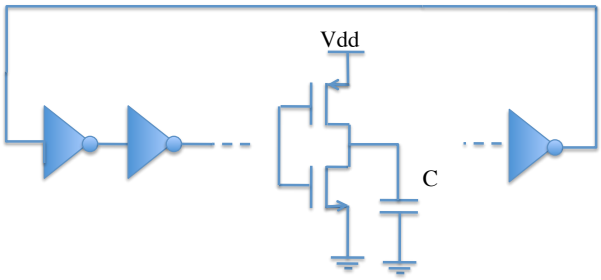


Figure 3.6: ring oscillator based on inverter gates

Based on equation 3.5 of phase noise of inverter based ring oscillator we obtain the first design guideline:

- Use of maximum large W/L (maximum I) for each transistor to minimize phase noise due to white noise

Flicker noise is also predicted in [70] and it is expressed as the following equation:

$$L(f) = \frac{C_{ox}}{8NI}\left(\frac{\mu_N K_{fN}}{L_N^2} + \frac{\mu_P K_{fP}}{L_P^2}\right)\left(\frac{f_0}{f}\right)^3 \tag{3.6}$$

Where C_{ox} is the capacitance of the oxide layer, K_{fP} and K_{fN} are empirical coefficients ($\approx 10^{-24}$), and μ_N and μ_P are the charge-carrier effective mobilities in the NMOS and PMOS respectively.

The phase noise induced by flicker noise of equation 3.6 gives us the following design guidelines:

- Use of maximum large W/L (maximum I) for each transistor to minimize phase noise due to flicker noise.
- Use of maximum L for the same reason.
- Larger the number of stages is, lower the phase noise due to flicker noise is.

3.2.1.2 DCO architectures comparison

These design guidelines are used to design two inverters based ring oscillators (5 stages and 15 stages) in 65nm CMOS for frequencies around 2GHz. Table 3.1 summaries their performances and compares it to LC performances obtained in section 2.6. We remind

that the used inductor is not optimized to have very high quality factor (Q=6). These performances are simulation results of Spectre analysis[4] (trans, PSS, and Pnoise). We see in table 3.1, that phase noise of 15 stages ring oscillators based on inverter gates is much worse than LC oscillator although its power consumption is 12 times higher. This result leads us to think about other architectures of ring oscillators as the interpolative oscillator presented by [10].

Table 3.1: Simulation results of LC and ring oscillators

Osc type	PN@600kHz	TR	PC (1.2V)
LC	-120 dBc/Hz	22%	5mA
5-stages	-91 dBc/Hz	35%	25mA
15-stages	-96 dBc/Hz	35%	60mA

The special architecture of this oscillator has a direct impact on its performances in terms of power consumption and tuning range as we will see in section 3.2.2. It consists of 5-stages NOR gates that interpolate with 3-stages of the ring, see figure 3.9(b). We design this oscillator for frequencies around 2GHz to compare it to the previously designed oscillators and following the same guidelines of inverter based ring oscillator. The ring is designed in 65nm CMOS and its performances are presented in table 3.2. This oscillator has larger tuning range than inverter ring oscillators and lower power consumption. Its phase noise is higher than LC phase noise but its power consumption is of same order.

Table 3.2: Simulation results of LC, inverter based rings, and NOR interpolative ring oscillators

Osc type	PN@600kHz	TR	PC (1.2V)
LC	-120 dBc/Hz	22%	5mA
5-stages	-91 dBc/Hz	35%	25mA
15-stages	-96 dBc/Hz	35%	60mA
5-3 stages [10]	-88 dBc/Hz	66%	6mA

As a summary, we opt for the design and optimization of interpolative oscillator responding to TV application requirements concerning phase noise with low power and low area.

3.2.2 The interpolative oscillator

The comparison between different ring oscillator architectures presented in table 3.2 leads us to choose interpolative oscillator design. We found that its power consumption is relatively lower than other ring architectures and its tuning range is higher. Many topologies

[4] http://www.cadence.com/products/rf/spectre_circuit/pages/default.aspx

of interpolative circuits that vary only by the method in which they sum their input signals are presented in the literature. One well known implementation, the inverter interpolator, is shown in figure 3.7 [8, 9]; it contains two inverters with competing outputs. In this circuit, inverters a and b are fed by two slightly out-of-phase inputs, labeled x and y. When the inputs are in phase, the interpolator acts as a series of two inverters, (a and b in parallel, in series with c). However, when the signals are out of phase, contention forms

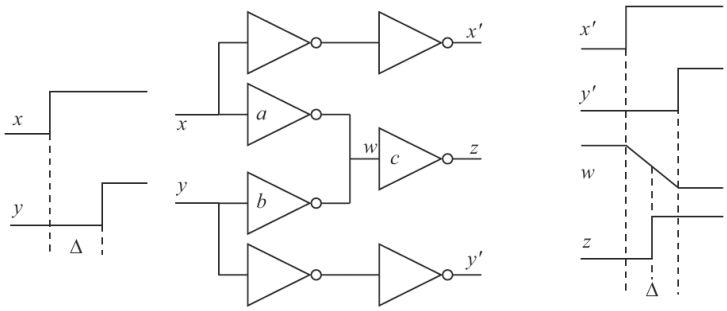


Figure 3.7: The inverter interpolator of [8, 9]

on node w, causing the voltage at w to fall nearly linearly over a time delay Δ. Assuming inverter c has a trip point at middle voltage ($V_{dd}/2$), the output at z temporally bisects the input signals $\acute{x}$ and $\acute{y}$. This assumes that the inverters are of equal strength, which may not be the case. If the inverters do not have equal strength, interpolation is shifted

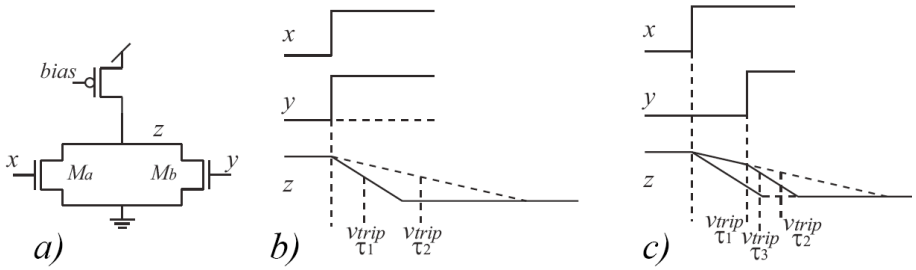
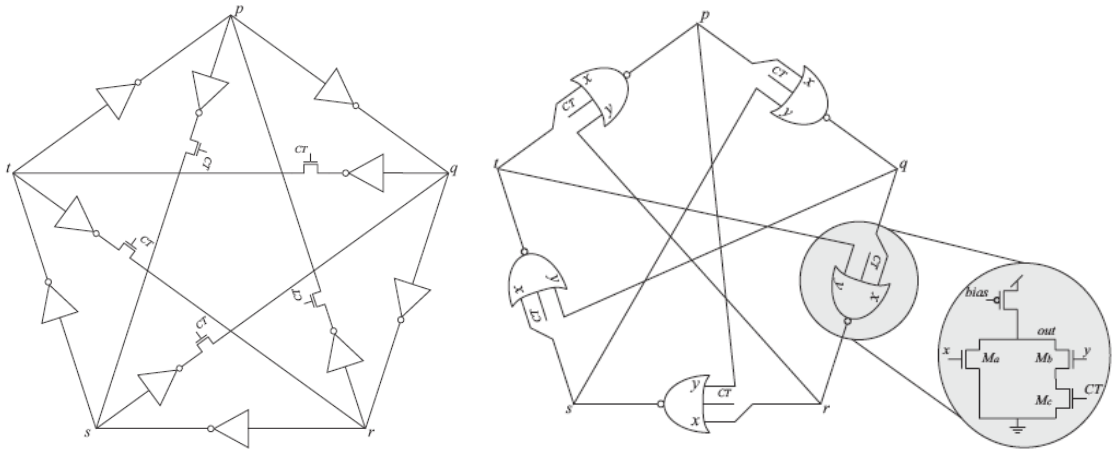


Figure 3.8: A modified digital interpolator, its timing diagram with b) equal time inputs, and c) unequal time inputs, [10]

more towards $\acute{x}$ or $\acute{y}$. Note that the unlabeled inverters are placed in this circuit strictly for convenience in timing and are not required for operation.

3.2.2.1 5-3 Interpolative oscillator

Another class of interpolator, proposed in [10], is a modification of the inverter based interpolator and it is called the NOR interpolator, see figure 3.8.a. This circuit interpolates between the rise/fall delay times with a single pull-down or a double pull-down device.



(a) 5-3 inverter based interpolative oscillator of

(b) 5-3 NOR interpolative oscillator of [10]

Figure 3.9: Two implementations of balanced 5-3 interpolative oscillator

Figure 3.8.b shows x and y arriving in phase and only x arriving, thus showing the two extremes of the interpolation. V_{trip} can be moved to any point between the time points τ_1 and τ_2 in figure3.8.b by adjusting the delay between x and y. Figure 3.8.c illustrates two signals arriving out of phase. In this case, the output node z begins its pull-down when x is high. In this state, the slope is relatively small and would take a longer time to reach ground, but when y becomes high, the z node is pulled low with a much steeper slope. As expected, the result is a trip point that lies between τ_1 and τ_2.

Figure 3.9 shows the circuit implementation of a traditional fully balanced 5-3 digital interpolative VCO using inverter interpolators [72, 73, 74], where the internal inverters interpolate in phase with the main inverters of the ring. The control voltage, CT, is used to weight the interpolation of the delay between a 5 and 3 stage ring.

We simulate in section 3.2.1.2 5-3 NOR interpolative oscillator for frequencies around 2GHz. For TV applications where frequencies range from 400MHz to 800MHz we propose 9-7 NOR interpolative oscillator. This architecture allows us to make use of the larger number of stages to increase the TDC resolution as we will see in section 3.4.2.

3.2.2.2 9-7 NOR interpolative oscillator

We present our 9-7 NOR interpolating oscillator in figure 3.10. This figure shows the circuit implementation of a 9-7 digital interpolative VCO using NOR interpolators, where nine delay cells interpolate in phase with seven delay cells of the ring. The NOR gate is viewed in figure 3.11, wherein, the control voltage, CT, is used to weight the interpolation of the delay between 9-stages and 7-stages rings.

The NOR gate implementation has high rejection of supply noise because the PMOS device acts as a quality current source. A second advantage is that fewer devices are in the signal path, implying less circuit noise (in most cases). Third, the NOR gate circuit

can be expanded to include more summations, allowing the interpolation of more than two signals with little overhead. This property is essential to facilitate high performance oscillators as it will be seen in section 3.2.5. Fourth, the circuit can be formed into a differential equivalent allowing multi phase outputs (in-phase and opposite phase). Fifth,

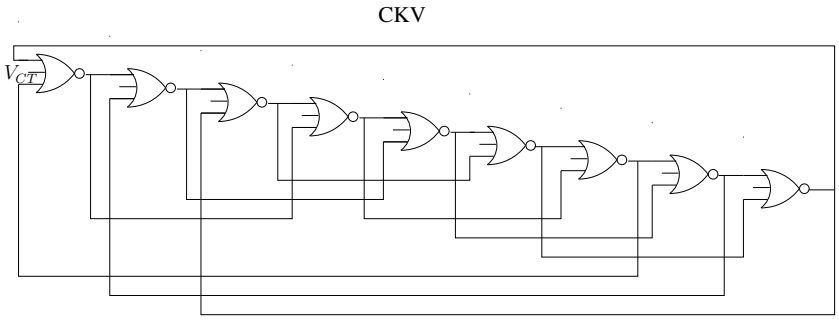


Figure 3.10: The interpolative oscillator (9,7) based on two ports NOR gates

the NOR gate structure inherently presents less input and output capacitance due to the limited use of PMOS devices in the signal path. Lastly, the frequency response is improved by reduced output swing. Since an interpolation causes contention at the output of the circuit, the pull-up and pull-down networks never completely shut off. This reduces the time required to activate the pull-down networks, allowing the oscillators to operate at higher frequencies.

The designed DCO is controlled by the control voltage CT that allows the interpolation of two frequencies: the first one comes from 9 stages ring and the second one comes from 7 stages as can be viewed in figure 3.10. In general, in case of equal delay time in NMOS and PMOS (this is a simple case and not a general case), the output frequency f_{out} of the ring oscillator of figure 3.6 is given by the equation:

$$f_0 = \frac{1}{2Nt_d} \tag{3.7}$$

Where N is the delay stages number and t_d is the delay time in each stage and in case of CMOS inverter, it is given by the equation [75]:

$$t_d = \frac{V_{dd} + v_n}{(I/C)} \tag{3.8}$$

where v_n is the resulting voltage of the integration of the noise current on the load capacitor C over t_d as expressed in the following equation:

$$v_n = \frac{1}{C} \int_0^{t_d} i_n(t)\, dt \tag{3.9}$$

3.2.3 The NOR cell

In the designed DCO, the NOR cell of figure 3.11 has in general (with no optimization

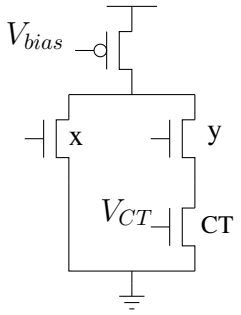


Figure 3.11: NOR gate

for low phase noise performance) no equal delay times of NMOS and PMOS, as we see in figure 3.12. Then, we define a new time delay as the average of two delay times t_{d1} and t_{d2}. t_{d1} is the delay time of the rising edge while t_{d2} is the delay time of the falling edge. The delay time of one stage is then given by the equation 3.10:

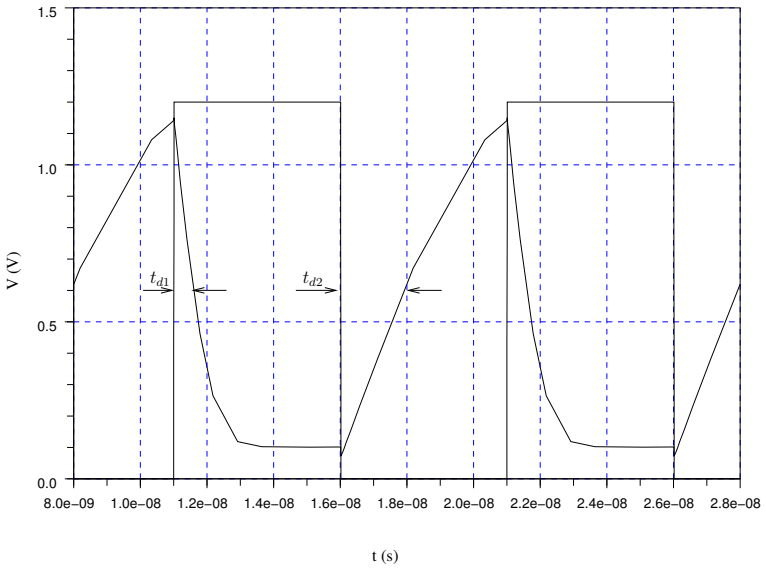


Figure 3.12: Delay times of rising and falling edges of NOR cell

$$t_d = \frac{t_{d1} + t_{d2}}{2} \tag{3.10}$$

If t_{d1} and t_{d2} are equal, the oscillation frequency doesn't change, but the output signal has best performance in terms of phase noise (this will be discussed in design strategy section 3.2.4). The simulated delay times t_{d1} and t_{d2} of figure 3.12 are less than the real ones because of the ideal step input with infinite slope, as we explained in figure 3.5. To simulate more precisely the delay time of one gate, the ideal input signal flows through three NOR stages whose inputs are shorted. The delay times t_{d1} and t_{d2} of the second

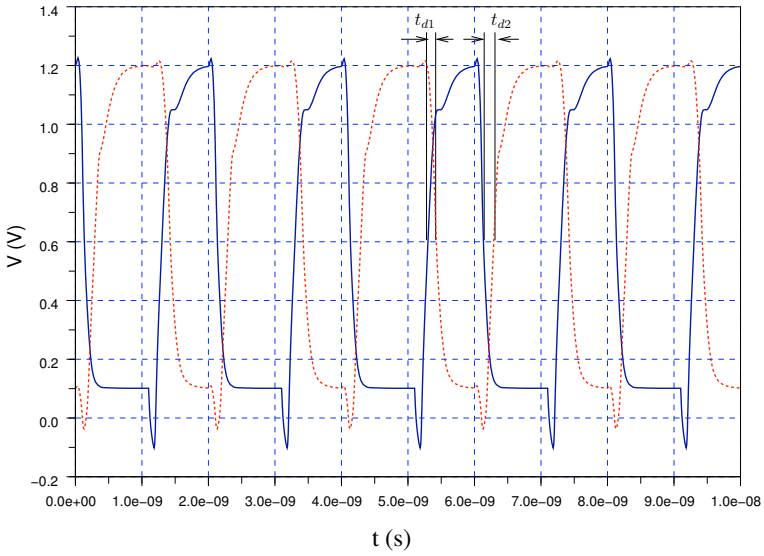


Figure 3.13: Delay times of rising and falling edges of the NOR gate

stage are then determined relatively to the first stage output and the third stage is used as the load capacitor of the NOR gate. Delay times t_{d1} and t_{d2} are equal to 120ps and 130ps respectively as presented in figure 3.13. This figure contains the transient analysis of Spectre[5] for 65nm CMOS process. Using equations 3.10 and 3.7, for 9 stages ring, the output frequency is around 450MHz.

Performance of ring oscillator in terms of power consumption is expressed by its maximum consumption given by the following equation:

$$P_{max} = N_{max} I_{bias\_max} V_{dd} \tag{3.11}$$

Where V_{dd} is the power supply voltage and I_{bias_max} is the maximum bias current.

The noisy elements in the ring are the NMOS and PMOS transistors. They have two noise types, $1/f$ flicker noise, and thermal noise with the corner point $\omega_{1/f}$. These noises are converted to phase noise around the carrier frequency at the oscillator output. We present in the next section a design strategy based on the ISF function of the ring oscillator to minimize the phase noise.

3.2.4 Design strategy using the ISF function

Design strategy of ring oscillator for minimum phase noise is largely presented in the literature [25, 76, 41]. It generally rolls in the use of high W/L for lower flicker noise upconversion with high L. In addition, phase noise doesn't depend on stages number, then, large number of stages is used. These guidelines are valid for lower phase noise due to white noise [41, 70].

[5] http://www.cadence.com/products/rf/spectre_circuit/pages/default.aspx

Design variables are NMOS and PMOS dimensions (W, L) of each stage. The channel widths of NMOS and PMOS are named Wn and Wp respectively. Therefore, we have 8 variables in each stage. The ISF is used to determine the sensitivity of the oscillator to noise injection in function of the design variables in two steps:

1. The variation of the ISF in function of L for fixed Wp/Wn.
2. The variation of the ISF in function of Wp/Wn ratio for fixed L.

In the first step we verify the variation of the sensitivity of the oscillator to noise injection with L and in the second step we verify the impact of the symmetrical properties of the oscillation waveform on the ISF.

Determination of the ISF

A current pulse is injected at the output of one stage of the ring (amplitude = 0.05mA, rise time = fall time = 0.5ps, pulse width=1ps) at the instant time τ of the oscillation period, then, its impact on the zero crossing instants is viewed a few periods after the injection period. The injected charge is $Q = I.dt = 0.1fC$. This charge is small in order to keep the linearity of the oscillator response. After that, τ is increased linearly by fixed steps to cover one oscillation period. Thus, the ISF is determined in any point of the oscillation period.

ISF variation with L: The influence of the transistors length L on the ISF can be viewed in figure 3.14. Wherein, four values of L are tested (65nm, 120nm, 130nm, 250nm)

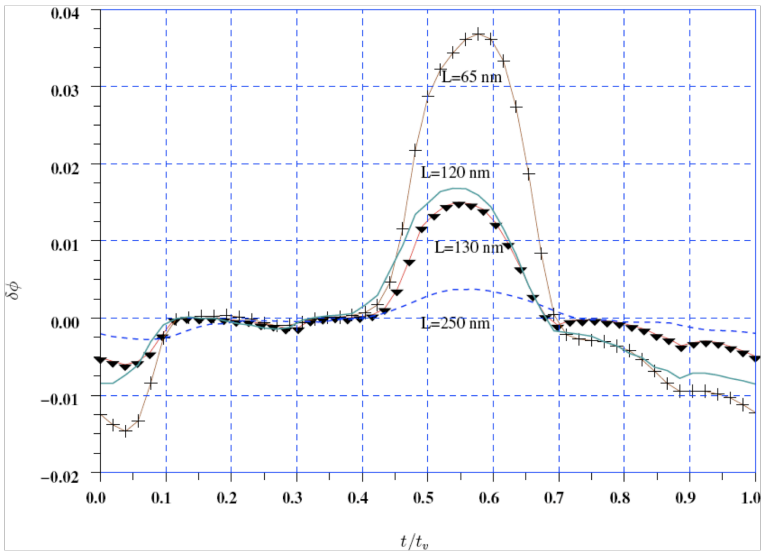


Figure 3.14: The ISF function for the ring oscillator interpolator for L= (65nm, 120nm, 130nm, 250nm)

with a fixed ratio Wn/Wp and with fixed frequency[6]. The oscillators are designed using 65nm CMOS and the ISF is extracted automaticaly using Spectre and Scilab tools as presented in section 2.5.3. The simulation result is viewed in figure 3.14 where we see that the ISF values decrease for increased L.

ISF variation with W_p/W_n: The symmetrical properties of the oscillation waveform is defined by the rising and falling times of the oscillation waveform. This property depends on the widths ratio W_p/W_n of the NMOS and PMOS transistors and it influences the position of the new corner ω_{1/f^3} as predicted by the LTV model of phase noise (see section 1.6.2),[18]. We determine by simulation the ratio that decreases the ISF for minimum

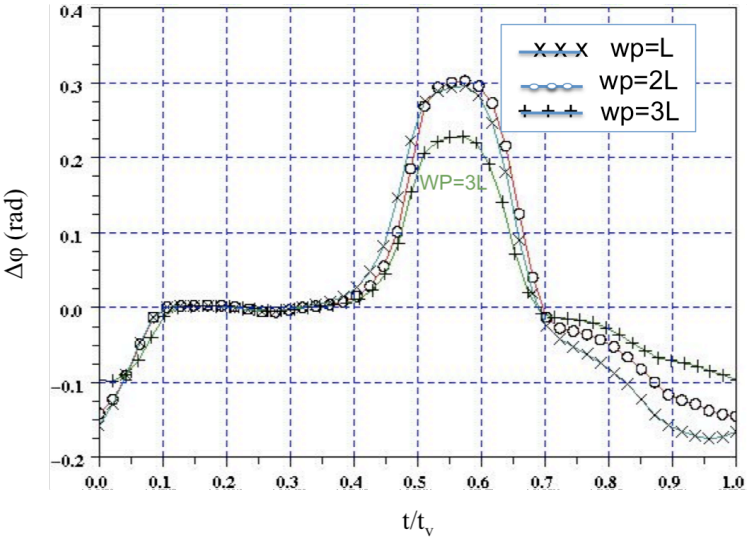


Figure 3.15: The ISF function of the interpolative oscillator in function of W_p/W_n for the W_n=L=250nm

power consumption. We take L=250nm because it has the minimum ISF values in the previous simulation. We choose $W_n = L$ to reduce the parameters in the simulation and we vary the ratio W_p/W_n. In figure 3.15 we present the ISF function for $W_p/W_n = 1, 2, 3$. For $W_p/W_n > 3$ the power consumption increased with no significant enhancement on the ISF function.

Finally, the transistors have the dimensions that are presented in table 3.3. Wherein, Wp,Wx,Wy,Wct are the widths of the PMOS, X, Y, CT transistors respectively. L is their length. The layout view is presented in figure 3.16. Pnoise analysis result shows that the phase noise of this oscillator at 462MHz carrier frequency is equal to -120dBc/Hz@5MHz, see Fig. 3.19. The oscillator consumes 1.6 mA from 1.2 V power supply and its tuning

[6]The simulation curves of figures 3.14 and 3.15 are done for 2GHz frequencies. But the results are scalable to all frequency bands. For our application (500MHz), these results are refined by Spectre analysis (Pnoise and trans) to reach TV specification presented in section 3.1.2.

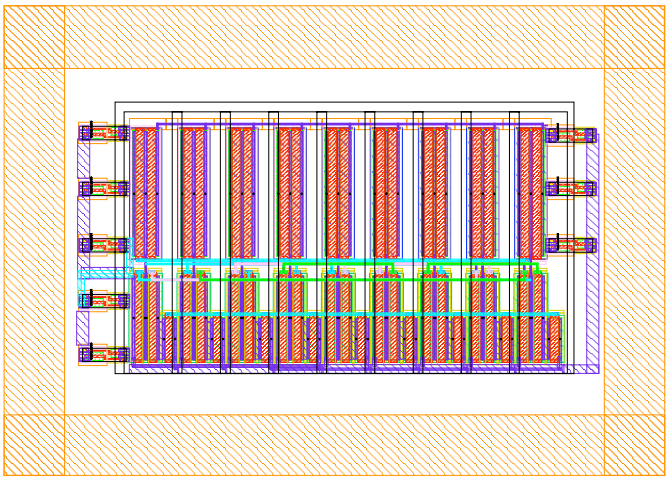


Figure 3.16: Layout view of nine interpolative DCO

range is from 400MHz to 800 MHz.

Wp (μm)	Wx (μm)	Wy (μm)	Wct (μm)	L (μm)
15	5	5	2.5	0.5

Table 3.3: The dimensions of the NOR port for minimum phase noise

3.2.5 DCO simulated characteristics

The DCO performances are determined using Spectre analysis. Transient analysis of the interpolative oscillator of figure 3.10 is presented in figure 3.17. CKV excursion is equal to 1 V. The presented signal is taken before the buffer stage. The influence of the buffer will be mentioned in section 3.5.2.

The DCO tuning range is from 200 MHz to 850 MHz, see figure 3.18. In this figure we present the DCO tuning range in function of the control voltages V_{bias} and V_{CT}. V_{bias} voltage is generated from 5 bits digital control word and V_{CT} is generated from 4 bits digital control word. We verify the monotony of the DCO frequency versus V_{bias} and V_{CT} variations. 5 curves are viewed in figure 3.18. Each one for different V_{bias}. The abscise axis is V_{CT} and the coordinate is the DCO frequency.

Pnoise analysis shows phase noise behavior of the DCO. We see in figure 3.19 the corner ω_{1/f^3} that is spotted at 200kHz offset from carrier frequency. The phase noise constraints that are presented in section 3.1.2 are respected for 5MHz offset from carrier frequency. The DCO has -120dBc/Hz@5MHz.

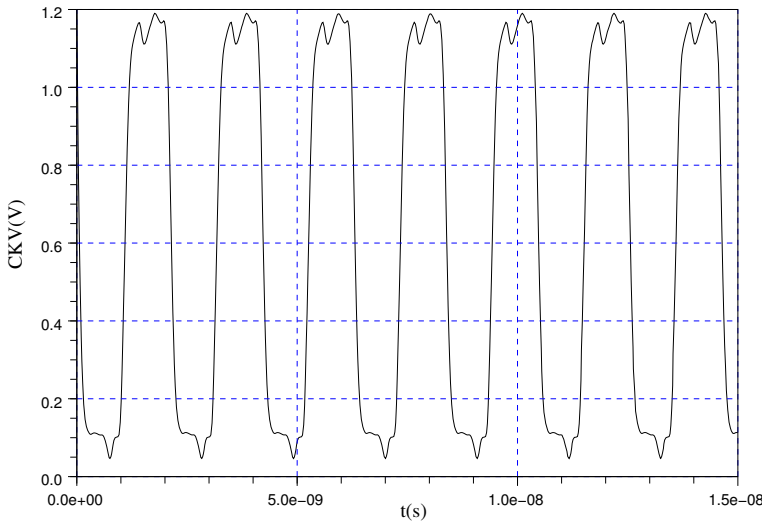


Figure 3.17: The CKV signal before the buffer stage. Its frequency is equal to 427.320 MHz and the digital control words are CT=7 and Bias = 15

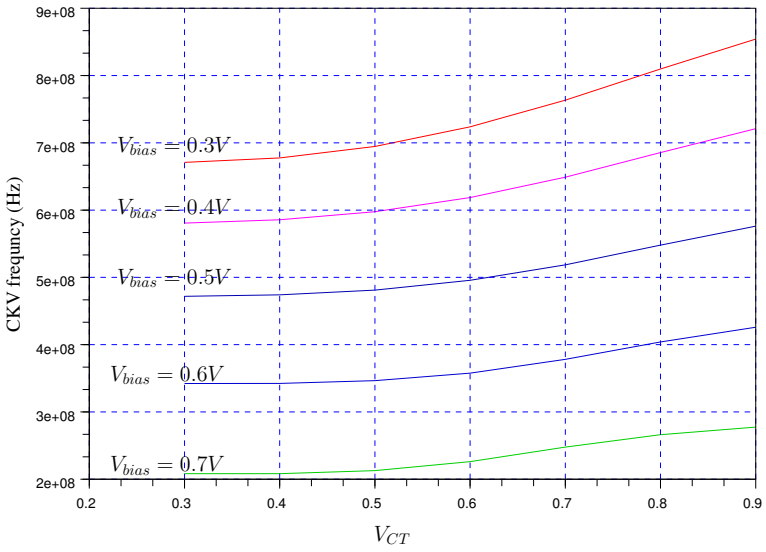


Figure 3.18: DCO tuning range in function of V_{bias} and V_{CT}

The oscillator has 1.2V power supply and it consumes 1.6mA for 460MHz carrier frequency and has $28 \times 39\mu m^2$ area. Table 4.1 shows the performances of this oscillator. These characteristics are simulated before extraction of the parasitics.

In next section we present the Digital to Voltage Converter used to generate both V_{bias} and V_{Ct} to cover the TV band.

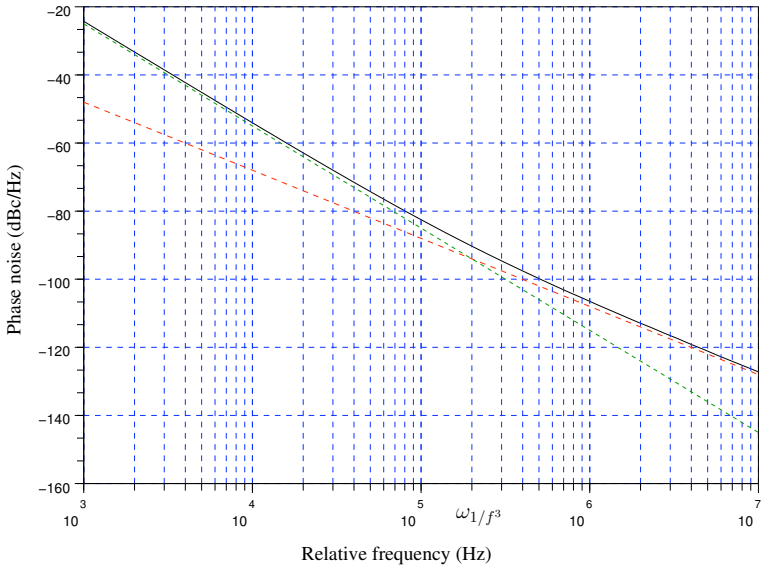


Figure 3.19: The Pnoise simulation results of the ring DCO

3.3 The Digital to Voltage Converter design

The most common types of electronic DACs are the pulse width modulator used in power converters [77], the oversampling DACs or interpolating DACs such as the delta-sigma DAC used in digital audio (ISDN) and HDTV applications [78], the binary weighted DAC [2], the R-2R ladder DAC [79], the thermometer coded DAC [5]. The difference between these DACs is measured in terms of resolution, maximum sampling frequency, monotonicity, and dynamic range.

The sampling frequency in our ADPLL is the reference frequency and it is equal to 26MHz. Two DACs are necessary in this design, for generating V_{bias} and V_{CT}. The monotonicity is the only requirement we impose in our application. Then, we use in our design thermometer code Digital to Voltage Converter for its simplicity, rapidity, and monotonicity.

3.3.1 Architecture and operation principle

A simplified diagram of the selected DAC architecture is viewed in figure 3.20. Wherein, the DAC inputs are the thermometer coded bits b_i that are updated at f_{ref} rate and the output signal is V_{out}. At f_{ref} rising edge, the charge Q_i of the bit b_i is stored. Q_i is activated/desactivated for high/low logic states respectively. The i-th current is then generated. Sum of all branches currents are added at the V_{out} node. Current to voltage conversion is performed across the resistor R:

$$V_{out} = R \times I_{total} = R.\sum_{i=0}^{n-1} I_i b_i \tag{3.12}$$

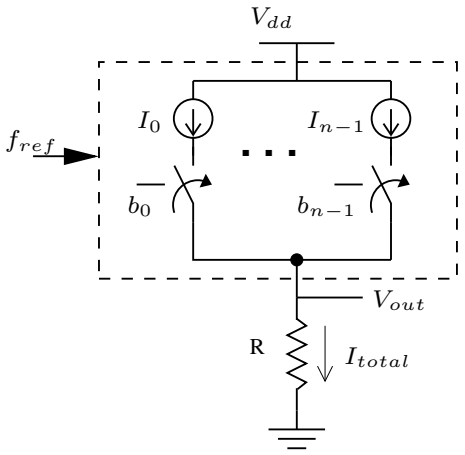


Figure 3.20: Digital-to-Voltage block diagram

In thermometer DAC, when the input binary bits are increased by x, x additional current sources of same size in the array are turned on, thus ensuring monotonicity and relaxed matching requirements on the current sources. As for binary weighted DAC, this is done by switching current sources of different size introducing more mismatching problems.

3.3.2 Binary to thermometer coding

A combinatory code to translate binary code into thermometrical code is written using VHDL language. Two encoders are necessary for the ADPLL. The first one has 5 bits input and 2^5 bits output for generating V_{bias}. The second one is 4 bits decoder. It has 2^4 bits output to generate V_{CT}. These bits arrive at f_{ref} rate, then two arrays of D flip-flop (5 bits, 4bits) are added at the arrival of the binary bits. The resulting bloc diagram of the DAC is the viewed in figure 3.21

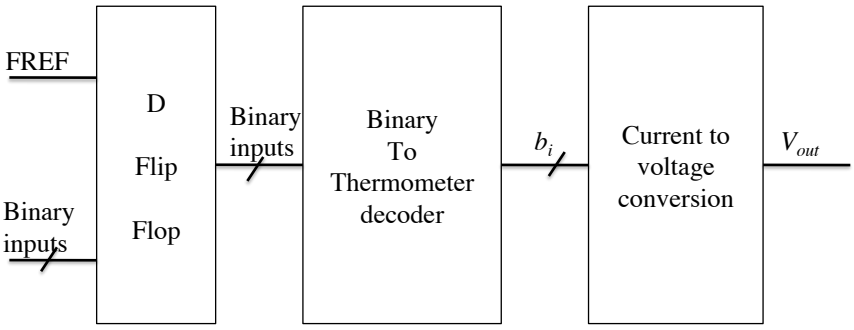


Figure 3.21: Block diagram of Digital-to-voltage converter synchronized with FREF

3.3.3 Implementation and simulated characteristics

In practical implementation, current sources are PMOS transistors and they are identical. They are activated or not according to the control bit b_i providing the elementary current I_i. The resistor is replaced by an NMOS transistor in order to guarantee the portability of the design. In this converter , the drain-source voltage of the basic transistors that provide I_i depends on V_{out}. Ideally, when these transistors are biased in saturation region, the value of I_i is independent of V_{out}. In practice, due to channel-length modulation [80], the basic current sources have a finite output impedance and I_i depends on V_{out}, limiting the linearity of the Digital-to-Voltage Conversion DVC. Here, this linearity is not questioned for simplicity reasons. The only criteria that is required is the monotonicity of the DVC.

For stable control bits b_i, the total drain-source current of the NMOS transistor is given by the following equation :

$$I_{total} = \sum_{i=0}^{n-1} I_i b_i = I_i \times OCW \tag{3.13}$$

where OCW is the oscillation control word and it ranges from 0 to 31 for V_{bias} and from

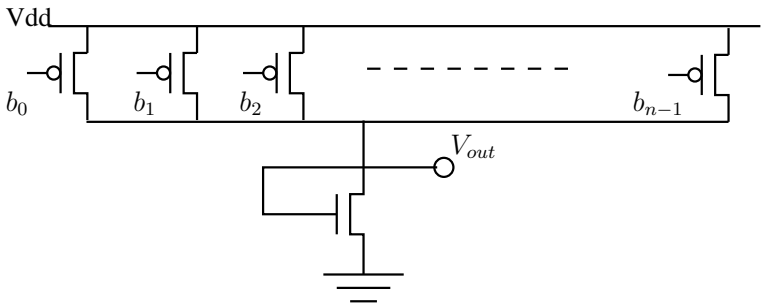


Figure 3.22: The Digital to Voltage Converter

0 to 15 for V_{CT}.

On the other hand, in the saturation region this current is given by

$$I_{total} = \frac{K_n}{2}\left(\frac{W}{L}\right)_{nmos}(V_{gs} - V_t)^2 \tag{3.14}$$

where $K_n = \mu_n C_{ox}$, being μ_n the mobility of electrons and C_{ox} the gate capacitance per unit area. (W, L) are transistor width and length, V_t is the voltage threshold of the channel, V_{gs} and V_{ds} are respectively the grid-source and drain-source voltages. Since V_{gs} and V_{ds} are equal to V_{out}, the drain-source current becomes:

$$I_{total} = \frac{K_n}{2}\left(\frac{W}{L}\right)_{nmos}(V_{out} - V_t)^2 \tag{3.15}$$

For the individual current I_i, the PMOS transistor is supposed to function in saturation region, then its drain-source current is given by the equation:

$$I_i = \frac{K_p}{2}\frac{W}{L}(V_{dd} - V_{tp})^2 \tag{3.16}$$

where $K_p = \mu_p C_{ox}$, μ_p is the electron mobility and V_{tp} is the threshold voltage of the channel in the PMOS transistor. Then, from equations 3.13, 3.15 , and 3.16 we find

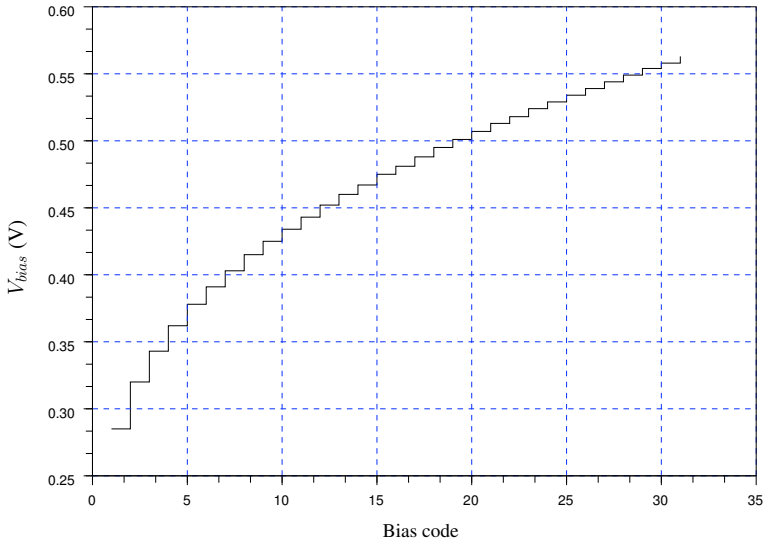


Figure 3.23: Simulation result of 31 bit DAC shows the variation of V_{bias} in function of Bias code

$$K_n \left(\frac{W}{L}\right)_{nmos} (V_{out} - V_t)^2 = OCW \times K_p \left(\frac{W}{L}\right)_{pmos} (V_{dd} - V_{tp})^2 \tag{3.17}$$

This equation is derived from first order approximation of I_{total} in function of NMOS dimensions (equation 3.14). More simplifications can be performed on equation 3.17 (for example: $K_n = K_p$) just to have a simple idea of the ratio between the NMOS and PMOS transistors (OCW).In addition, V_{out} range is known from the DCO gain K_{DCO} in function of two control voltages V_{bias} and V_{CT}. V_{bias} ranges from 0.3V to 0.6V while V_{CT} varies from 0.5V to 0.8V.

Figure 3.23 illustrates the variation of V_{bias} in function of Bias code using spectre analysis and figure 3.24 presents the variation of V_{CT} in function of CT code.

3.4 TDC design

The TDC is used to determine the delay ε between the rising edges of the reference signal FREF and the oscillator signal CKV in the ADPLL of figure. 3.1, as can be viewed in the equation:

$$\varepsilon = \phi_{FREF} - \phi_{CKV} \tag{3.18}$$

where ϕ_{FREF} and ϕ_{CKV} are the rising edges instants of FREF and CKV respectively.

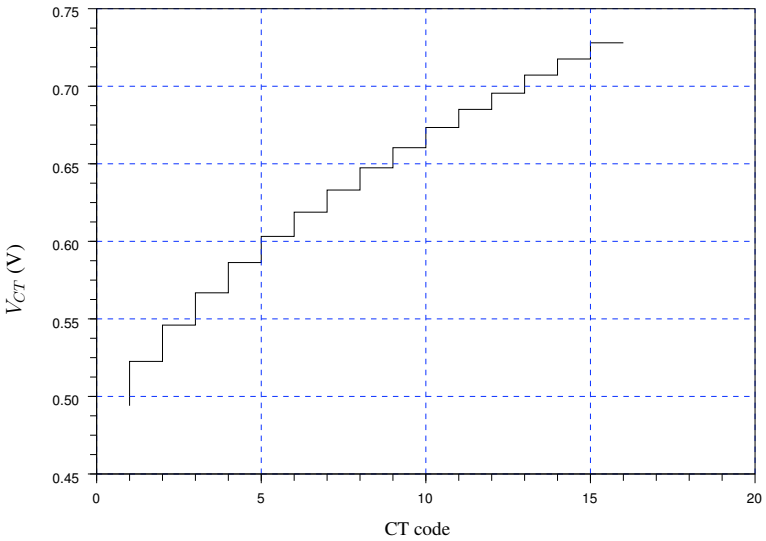


Figure 3.24: Simulation result of 16 bit DAC shows the variation of V_{CT} in function of CT code

3.4.1 Architecture and operation principle

We use the ring oscillator that contains nine stages NOR gates each one has t_d delay time. The input/output signals of the ports are named CKV(0),CKV(1),...,CKV(8).

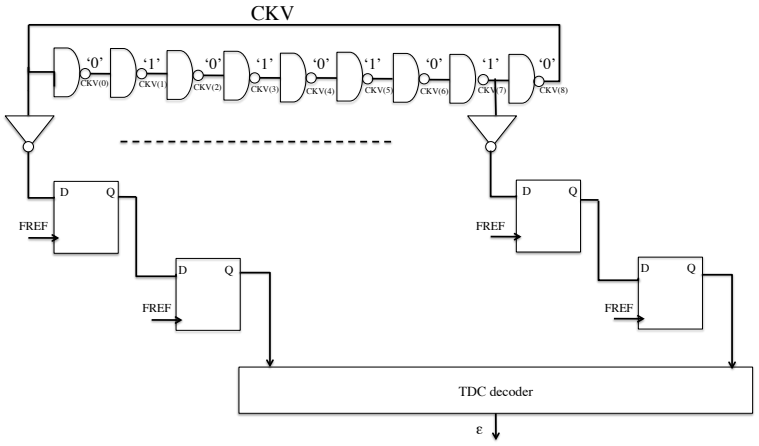


Figure 3.25: The TDC reads the output of each stage of the ring at the rising edge of the FREF. This state is then decoded to determine ε

The functionality of the TDC is based on the read of the state of the ring at the rising edge of the reference FREF. Then, this state is registered, and decoded according to table 3.4 to determine the position of the rising or falling edge that is propagating in the ring, and thus determinates ε.

An example of the functionality of the proposed TDC is viewed in figure 3.26. Wherein, the oscillator has five stages, thus the TDC register contains 5 bits. The oscillator period $T_{CKV}/2 = 5t_d$. Therefore, the normalized period (by t_d) is equal to 10. In figure 3.26 we

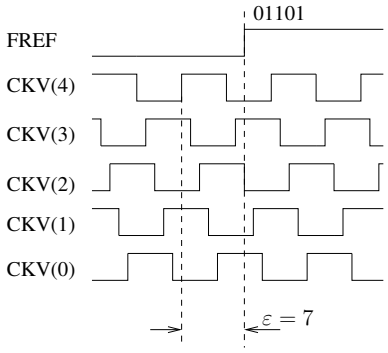


Figure 3.26: Ring status example for 5 stages ring oscillator

see that the ring state at the rising edge of FREF is 01101. This means that the falling edge is observed at 3/10 and ε is equal to 7/10.

In our TDC, the ring state is defined by the output bits of the nine stages of the ring. The oscillator normalized period is then equal to 18 ($T_{CKV}/2 = 9t_d$). Then, we can define 18 states of the ring, see Table 3.4. From each one we can know if there is a rising or falling edge in the ring and then we can determine its position relatively to the rising edge of FREF. When a rising or falling edge propagates in the ring the signal CKV(0) is equal to '1' or '0' respectively, and the value of ε varies from 0 to $8t_d$ or from $9t_d$ to $17t_d$ respectively.

Table 3.4: The ring has 18 states, and each one corresponds to a different value of ε

[0]	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	ε
0	0	1	0	1	0	1	0	1	17/18
0	1	1	0	1	0	1	0	1	16/18
0	1	0	0	1	0	1	0	1	15/18
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	0	1	0	1	0	1	0	9/18
1	1	0	1	0	1	0	1	0	8/18
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	1	0	1	0	1	1	0	2/18
1	0	1	0	1	0	1	0	0	1/18
1	0	1	0	1	0	1	0	1	0

The main advantages of this architecture is its low area and economical power consumption compared to TDC delay line based and TDC vernier presented in section 1.11. It consists of only 9 digital buffers and 18 D flip-flop (65nm digital cells library). The

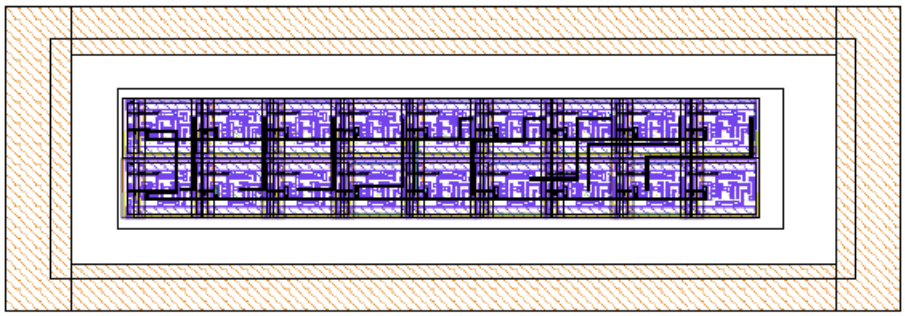


Figure 3.27: Layout view of the TDC register

layout view of this TDC is presented in figure 3.27. Next we determine the phase noise performance of the proposed TDC.

3.4.2 TDC phase noise

The resolution of the proposed TDC is equal to $T_{CKV}/18$ and it corresponds to t_d. The quantization error affects the closed loop phase noise. The variance σ_t of this error is given by $\sigma_t^2 = t_d^2/12$, and the phase error then can be obtained from $\sigma_\phi = 2\pi\sigma_t/T_{CKV}$. The TDC phase noise is uniformly distributed over the frequency band from dc to reference frequency f_{ref}, and it can be written as

$$L(\Delta\omega) = \frac{\sigma_\phi^2}{f_{ref}} = \frac{(2\pi)^2}{12}\left(\frac{t_d}{T_v}\right)^2 \frac{1}{f_{ref}} \tag{3.19}$$

This phase noise depends on the reference frequency and it is filtered by the closed loop as we said in section 2.7. In our TDC, this resolution is equal to $T_{CKV}/18$. If the frequency oscillation is equal to 500MHz and the reference frequency is equal to 26MHz, the power spectral density of phase noise is equal to $-94dBc/Hz$. This noise is low pass filtered by the loop at the cut-off frequency f_{co}=16kHz (see section 3.1.3) . Therefore, this phase noise is about -144dBc/Hz@5MHz from carrier frequency which is 24dB less than DCO phase noise (-120dBc/Hz@5MHz).

3.4.3 Modeling and simulation

The TDC part that calculates ε is programmed using VHDL. We define the input-output signals S(0), S(1),...,S(8) of the DCO stages as the input vector of the TDC. DCO output is S(8). The S vector is then decoded according to the table 3.4 into thermometer code that represents ε. This TDC is programed on FPGA.

Modelsim[7] simulation result is viewed in figure 3.28. In this simulation, the period T_{CKV} is equal to 2 ns ($t_d = 222ps$) and the reference period is equal to 38 ns. We could verify the correspondence between the value of ε and the time delay between the rising

[7] www.mentor.com/products/fv/modelsim/

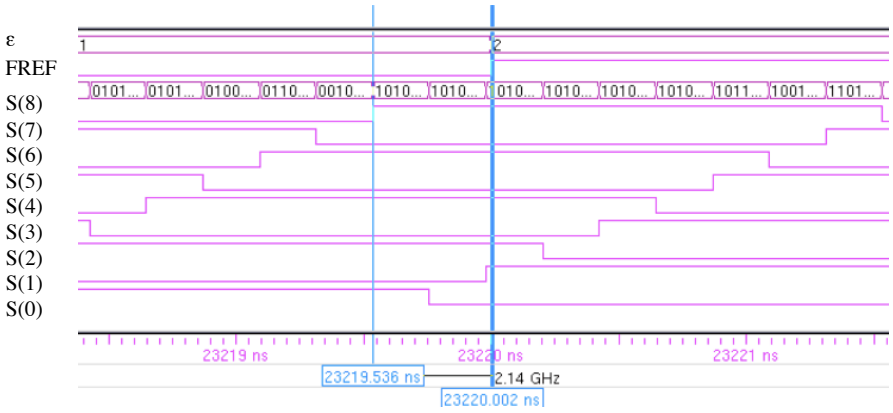


Figure 3.28: The simulation results of the TDC. ε is the delay time between the rising edges of FREF and CKV.

edges of FREF and CKV. In this figure, the delay between FREF and S(8) is equal to 466 ps and it is equivalent to $\varepsilon = 2$. The relative error in this calculation is $\frac{466ps - \varepsilon.t_d}{\varepsilon.t_d} = 4.8\%$.

3.5 Other high frequency blocks design

In addition to the DCO, the two DACs, and TDC register, the integrated circuit part of the ADPLL contains a digital counter to calculate the variable phase Rv, an output buffer for CKV signal, and a frequency divider to obtain the CKV/4 signal. Each of these blocks are designed as follows.

3.5.1 CKV counter

The variable phase can be calculated by incrementing by one at every rising edge of CKV. This block is designed using VHDL synthesis. Where in Rv is defined as followed:

```
Rv : unsigned ( 4 downto 0 ) ;
```

Then, the arithmetic modulo is done as the following equation:

$$Rv[k] = (1 + Rv[k-1]) \mod 2^5 \tag{3.20}$$

The counter is described as an accumulator of 1 (modulo 2^5) at each CKV rising edge as follows:

```
accum: process (ckv)
variable compte1 : unsigned ( 4 downto 0 ) := (others => '0');
begin
    if ckv = '1' then compte1 := ( 1 + compte1 ) mod 2^5 ;
```

```
    else compte1 := compte1 ;
    end if ;
    Rv1 <= transport compte1 ;
end process ;
```

The value RV1 is then observed at the rising edge of FREF as described below:

```
sync: process (fref)
variable Rv2 : unsigned ( 4 downto 0 ) := (others => '0');
begin
    if fref ='1' then Rv2 := Rv1 ;
    else Rv2 := Rv2 ;
    end if ;
    Rv <= transport Rv2 ;
end process ;
```

Modelsim simulation of the presented model of digital counter is illustrated in figure 3.29. It contains FREF signal of period 38ns, CKV signal whose period is about 2ns and R_v. This model is synthesized and the digital counter circuit is implemented in the 65nm circuit.

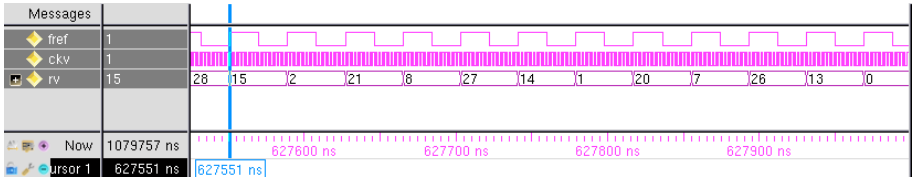


Figure 3.29: Modelsim result of digital counter model.

3.5.2 Buffer Design

A buffer is used to bring CKV signal to the phase noise measurement device without deteriorating its phase noise performance. The buffer is an NMOS open drain amplifier that is presented in figure 3.30 . It is preceded by two inverters that have smaller gate width in order not to charge the DCO output.

This buffer is designed following these steps:

1. Design of the transistor without the inverters by adjusting the transistor width for a symmetrical signal with no amplitude excess.

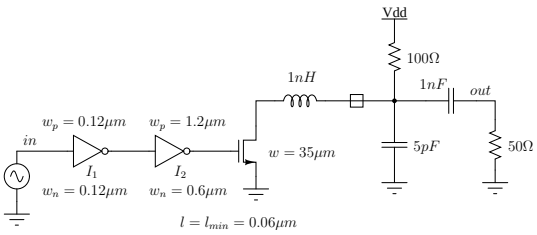


Figure 3.30: The ouput buffer

2. Insertion of two inverters of minimum dimensions.

3. Refinement of the second inverter in order to have a symmetrical waveform on CKV.

4. Verification of the DCO performance in phase noise with the buffer.

Buffer performances

The buffer is designed according to the design steps presented in section 3.5.2. The final dimensions of the NMOS transistor are W/L=35/0.5 and the layout view is shown in figure 3.31. Inverter's dimensions are presnted in figure 3.30. In the simulation we take

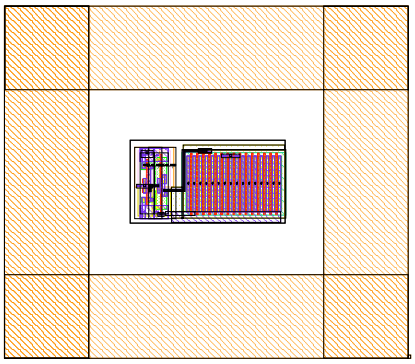


Figure 3.31: Layout view of the buffer

into account the inductive effects of the packaging, a load resistance 50Ω, and the coupling capacitors at the input of measurement device. The pull-up resistance is implemented on the test bench circuit.

The results of the transient analysis is illustrated in figure 3.32. The amplitude of CKV is about 400mV P-P.

Pnoise analysis result is presented in figure 3.33. DCO phase noise is conserved and it equal to -120dBc/Hz@5MHz from 480MHz frequency.

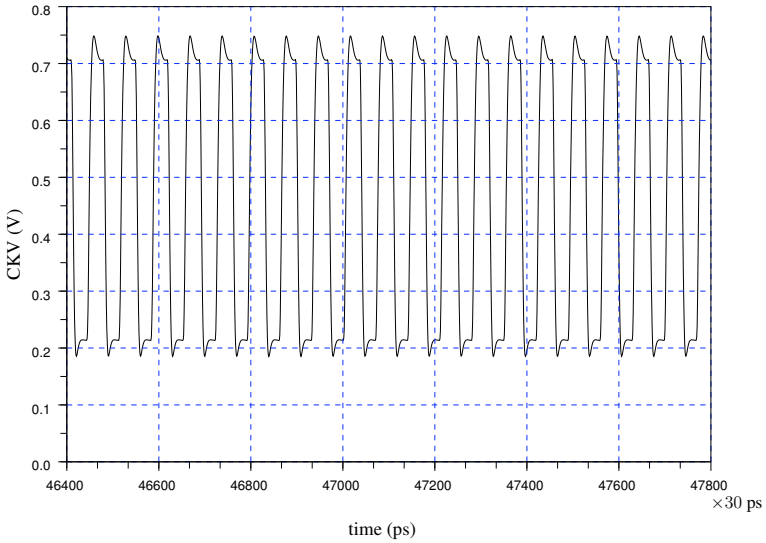


Figure 3.32: Transient analysis results of the buffer

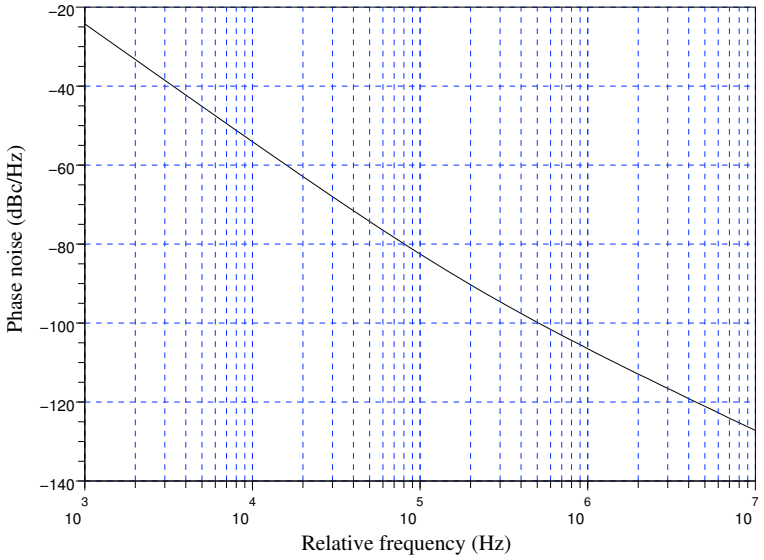


Figure 3.33: Pnoise analysis results with the buffer

3.5.3 The frequency divider

We use a frequency divider to generate a signal CKV/4 that has quarter of CKV frequency. The generated clock is used in the $\Sigma\Delta$ modulator of the ADPLL that will be designed in future work. The LSB bits of the control word of the DCO will be dithered in order to have better resolution on the CKV signal. The block diagram of this divider is presented in figure 3.34. The D flip-flops used in the design are standard elements of the library. This divider is followed by the same buffer of section 3.5.2 and the output signal is connected

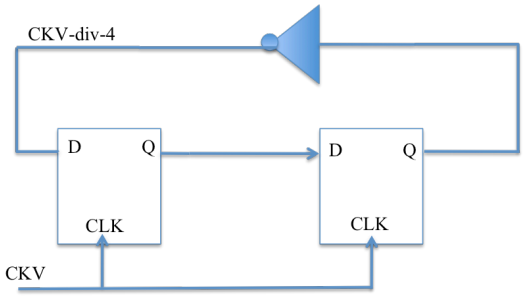


Figure 3.34: Block diagram of the frequency divider

to the FPGA.

Performances We verify the functionality of the frequency divider by transient analysis of Spectre. In figure 3.35. we see CKV and CKV/4 signals whose frequencies are equal to

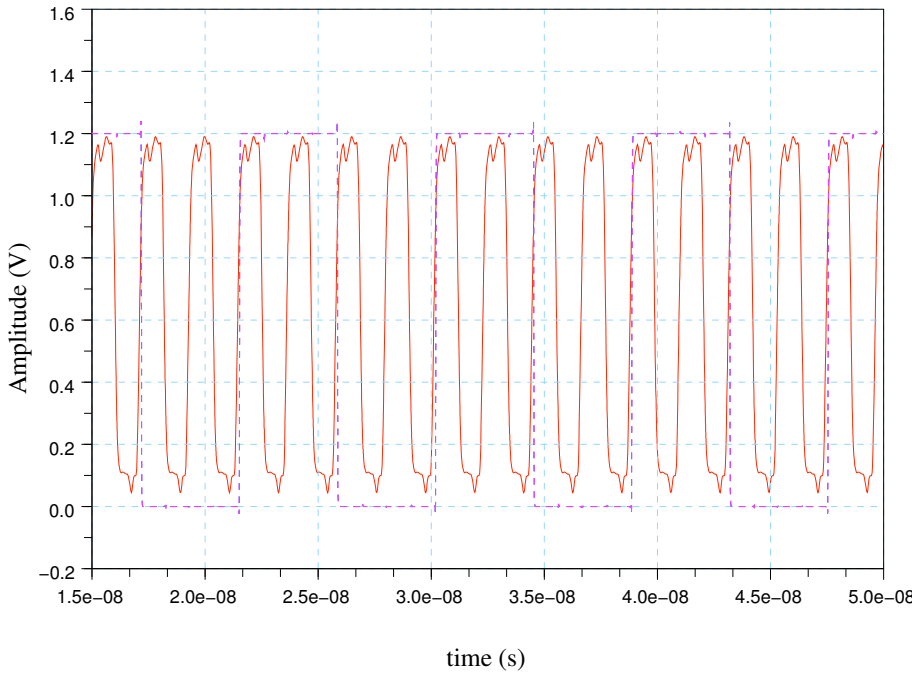


Figure 3.35: CKV and CKV/4 signals have respectively 427.320MHz and 106.791MHz frequencies (CT=7, bias=15).

427.320MHz and 106.791MHz respectively.

3.6 Phase comparison implementation in FPGA

Some parts of the ADPLL operate at the reference frequency f_{ref}. These blocks are programmed on FPGA. The block diagram of these blocks is viewed in figure 3.36. This

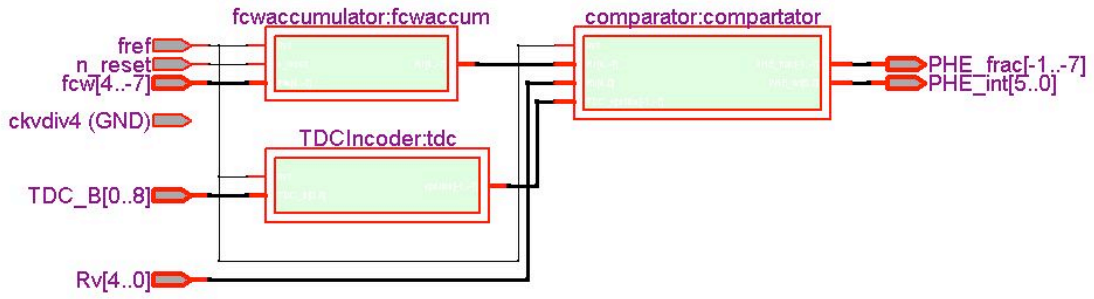


Figure 3.36: The phase detector block diagram implemented on FPGA

figure contains the FCW accumulator for the reference phase, the TDC encoder and the phase comparator.

3.6.1 Reference phase

The reference phase is calculated by accumulating the FCW word at the rising edges of FREF. FCW is defined as an unresolved fixed point *ufixed* signal in VHDL. This type of signal is proposed in the library **floatfixlib** designed by VHDL-93 compilers synthesis tools according to IEEE Standards Department Activities. Two packages are defined in this library: the first one is **fixed_pkg** that allows to make the most popular mathematical operations (like '+','-','div','mod','*' ,'abs',..etc) and comparison operations between signed/unsigned fixed point numbers (named sfixed/ufixed respectively) and the other signal types (like integer and natural), and the second one is **math_utility_pkg** that contains the statements of the types.

The accumulator inputs are FREF signal and reset bit to initialize the register. FCW and reference phase Rr words are defined as ufixed signals as follows :

FCW : in ufixed (4 downto -7) ;

Rr : out ufixed (4 downto -7) ;

This means that FCW and Rr are unsigned numbers and their integer parts are defined on five bits (4 down to 0) while their fractional parts are defined on 7 bits (from -1 down to -7). The accumulation is done at FREF rising edges according to the following equation:

$$Rr[k] = (Rr[k-1] + FCW) \mod 2^5 \tag{3.21}$$

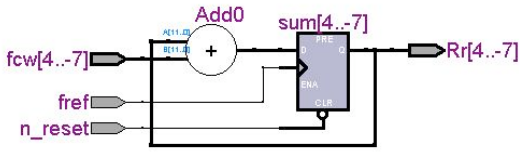


Figure 3.37: An accumulator of the frequency control word

Observing the block diagram of FCW accumulator in figure 3.37, we notice that the critical time is the propagation time Δ in the D flip-flop. The D flip-flop is required to avoid unstable data at the following comparator input (see figure 3.36) and to prevent any metastability problem. So, the comparator is in charge to deliver the phase difference. The delay time Δ depends on the used FPGA. We use the Stratix II EP2S60F1020C3 DSP development board[8].

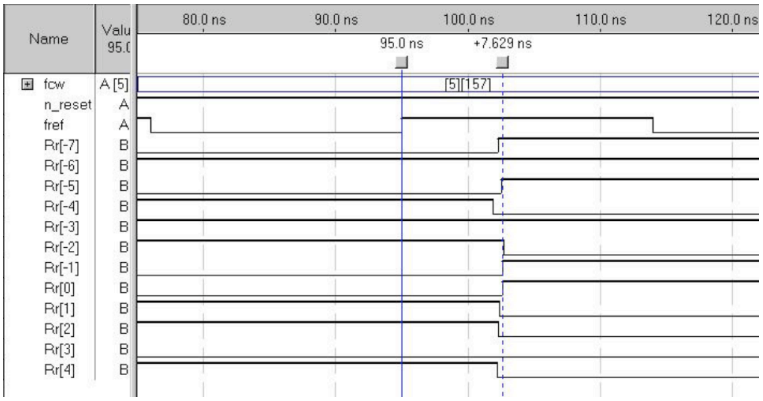


Figure 3.38: Delay time of FCW accumulator is around 7ns

Simulation result of the FCW accumulator are presented in figure 3.38. Wherein, FCW is equal to 11.226 (N_i=01011, N_f=0011101). The time delay Δ between the rising edge of FREF and the last stable output bit in Rr is observed to be around 7ns. We can note that this value is inferior to half of FREF period (FREF = 26MHz).

$$\Delta_{FCWaccum} < \frac{T_{ref}}{2} \tag{3.22}$$

3.6.2 TDC encoder

The TDC encoder transforms the received state of the ring to ε according to table 3.4. DCO state is presented as std_logic vector as follows:

[8] http://www.altera.com/products/devkits/altera/kit-dsp-2S60.html

TDC_B : in std_logic vector (0 to 8) ;

The output block is ε and it is defined as the fractional part of a real number as follows:

epsilon : out ufixed (-1 downto -7) ;

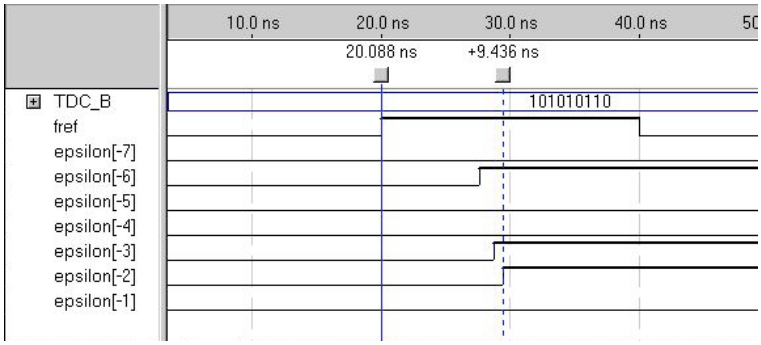


Figure 3.39: Simulation result of the TDC encoder. Delay time is around 10ns

Propagation delay is also simulated and presented in figure 3.39. Its value is around 9.5ns. In this example, the value of propagation time is inferior to half of FREF period. This result have been validated for all TDC_B possibilities (18 cases of table 3.4) and it is inferior to 10ns and we can rewrite:

$$\Delta_{TDCencoder} < \frac{T_{ref}}{2} \tag{3.23}$$

The schematic block diagram of the TDC encoder is viewed in the annex C.

3.6.3 The phase comparator

The phase comparator block has four input signals and two output signals as we see in figure 3.36. Rr, Rv, TDC_epsilon, are the input words of the comparator and FREF is the clock. Rv comes from the integrated circuit see figure 3.4 while Rr and TDC_epsilon are calculated in the FPGA.

We noted before that the propagation delays Δ of the FCW accumulator and the TDC encoder don't exceed half of the FREF period (see equations 3.22 and 3.23).

Propagation delay Δ of this block is also critical, because the output phase difference have to be available before the arrival of the next event. This time is simulated and it is presented in figure 3.40. In worst case, this time doesn't exceed half of FREF period and we write again:

$$\Delta_{phase\ comparator} < \frac{T_{ref}}{2} \tag{3.24}$$

This equation guarantees the stability of the outputs PHE_int and PHE_frac at the input of the integrated circuit before the arriving rising edge of FREF.

In conclusion, the phase is sampled at the rising edge of FREF. Then, we can calculate R_r and ε during the first half period of the next FREF period and the phase comparator is activated at the next falling edge of FREF. Finally, the DCO command is updated within 1 FREF period.

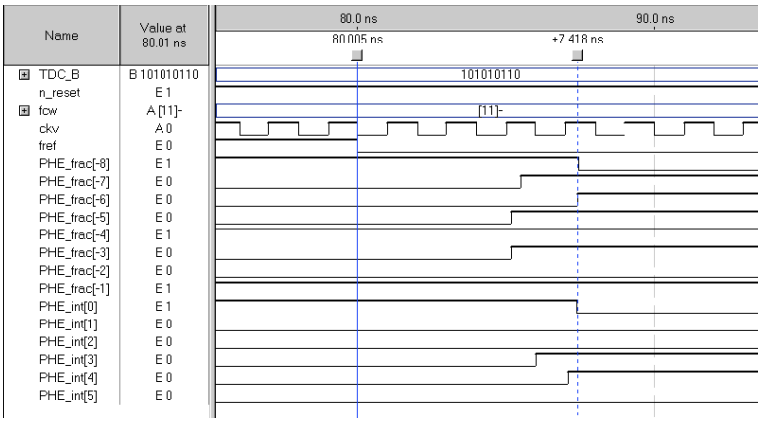


Figure 3.40: Delay time of the phase comparator block in the FPGA is around 9ns

3.7 Conclusion

A design of ADPLL for TV application is presented in this chapter. Wherein, design strategy of the DCO ring interpolator for low surface and low phase noise is presented. The proposed DCO is based on hybrid DCO approach that is opted for its smaller surface, lower power consumption, and simpler implementation of well know oscillators and DACs architectures than the direct DCO approach. One of the main benefits of the DCO ring oscillator is the possibility of determination of the position of the propagating edge in the ring from FREF rising edge, thus determination of ε without increasing the power consumption. Therefore, the DCO and TDC architectures are merged lowering the surface and the power consumption of the total ADPLL.

Simulation results of the DCO shows a low phase noise behavior of the designed oscillator. It has -120dBc/Hz at 5MHz from 450MHz carrier frequency. TDC phase noise has uniformly distributed power spectral density of -94dBc/Hz. The low frequency parts of the ADPLL are designed and simulated on FPGA. The propagation time of each block is inferior to half of FREF period. Thus, this allows the phase comparison to be synchronized with the falling edge of FREF.

Measurement results of the ADPLL in terms of phase noise, power consumption, and frequency range are presented in chapter 4.

Chapter 4

Measurement results

The ADPLL is designed for TV applications for minimum phase noise. Chapter 3 describes the design of the high frequency part implemented on 65nm circuit and of the low frequency part programmed on FPGA. The characteristics of the ADPLL blocks are also presented.

In this chapter we compare the measurement results to simulation results. Therefore, we present the open loop behavior and its performances in terms of phase noise, power consumption and tuning range. We compare the predicted DCO performances to the measured ones. Performances of the TDC, the frequency divider, the digital counter are verified as well.

This chapter is organized as follows: A summary of the ADPLL simulated performances is presented in section 4.1. Next, the open loop test card is viewed in section 4.2. Within, we present the performances of the DCO in section 4.2.1, of the TDC in section 4.2.2. Then the test of the digital counter is presented in section 4.3, and the frequency divider in section 4.4. Finally, we conclude this work in section 4.5 with some perspectives.

4.1 Simulated performances of the ADPLL blocks

4.1.1 Level of the simulation done

High frequency part of the ADPLL is designed in 65nm CMOS technology and performances of its blocks are simulated using spectre analysis. The presented performances are results of schematic analysis and post layout analysis (with parasitic capacitors) are performed to ensure the required characteristics. Phase noise of the DCO has not been deteriorated in the presence of parasitic capacitors. As for FPGA blocks, we presented the simulation results of each block separately. The complete ADPLL is not simulated at physical level but it can be modeled by the ADPLL model developed in chapter 2 as it will be described afterward. However, the DCO is designed using the ISF function and the ADPLL phase noise model presented in chapter 2 is based on the ISF as well. The differences between the ADPLL model and of the designed ADPLL are:

1. The ADPLL model simulates the performances of the ADPLL for frequencies around 2GHz. However, this application is chosen as an example and the model is generic

from this point of view.

2. The DCO of the designed circuit is a ring oscillator while it is an LC in the ADPLL model. Whereas, the DCO model in the ADPLL depends on its ISF Fourier transform coefficients independently on the DCO architecture.

3. The TDC architecture in the ADPLL model is a delay line while it is merged with the DCO in the designed circuit. The phase noise behavior of each architecture is presented.

The ADPLL can be simulated using the ADPLL model developed in chapter 2 by modifying the generic parameters of the model following these steps:

1. The integer part of FCW is defined on 5 bits and the fractional part is defined on 8 bits.

2. The central frequency is a generic parameter and it can be modified to correspond to TV applications (660MHz).

3. The normalization block f_{ref}/K_{DCO} in the DCO model has a new value because of the new K_{DCO} that corresponds to the 9-7 ring interpolative oscillator.

4. 1/f noise sources are not the same in LC and ring oscillator and then the 1/f source has to be modified (a_k values to be determined).

5. The ISF Fourier transform coefficients C_n of the LC oscillator have to be replaced by the ISF coefficients of the 9-7 ring DCO.

6. The TDC noise due to quantification error can be modeled by added white noise to the instantaneous phase $\phi(t)$ in the model

This model is currently under test and simulation results will be provided in the presentation.

4.1.2 Summary of the simulated results

In terms of required performances, phase noise behavior of the DCO has -120dBc/Hz@5MHz at carrier frequency being in the band 400MHz to 800MHz. The TDC has uniform white noise of density -94dBc/Hz. The following table summaries the simulation results of the implemented circuit in terms of power consumption, phase noise, area, and signal excursion. Signal dynamic of CKV is deteriorated by the buffer but phase noise and tuning range are conserved. As for FPGA part of the ADPLL, its blocks are simulated using Stratix II EP2S60 transient analysis and delay time in each block is determined.

	Power consumption	Phase noise @5MHz	area μm^2	Excursion
DCO	1.6 mA - 1.2V	-120dBc/Hz	28×39	1V
Buffer	7mA -1.2V	-120dBc/Hz	17×15	400mV
TDC	–	-94dBc/Hz	17×46	–
DAC (CT)	–	–	16×21	–
DAC (V_{bias})	–	–	17.8×20.5	–

Table 4.1: Summary table of the high frequency parts of the ADPLL that are implemented in CMOS 65nm process.

4.2 Open loop test card

Tests of open loop ADPLL are done using the card which block diagram is illustrated in figure 4.1. Wherein, the circuit is placed in the card center. RF outputs (CKV and CKV/4) are connected to oscilloscope and spectrum analyzer while digital output pins are connected to logic analyzer. IC input signals are controlled using switches allowing

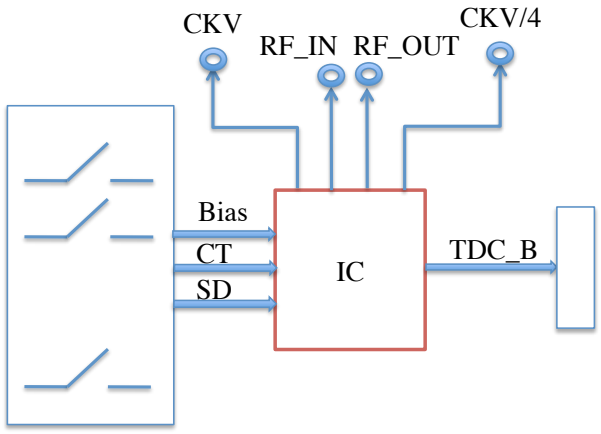


Figure 4.1: Block diagram of open loop test card

high/low bit states for Bias, CT, and SD bits. The total circuit consumes 7 mA from 1.2V power supply.

4.2.1 DCO performances

In this section we present the DCO performances in terms of signal amplitude, tuning range, power consumption, and phase noise and we compare it to simulation results of the DCO presented in section 3.2.5. The power spectral density of CKV with its harmonics is also viewed. In addition we present the variation of the output frequency as a function of Bias code and power supply in section 4.2.1.2. A comparative table in terms of figure of merit with the state of the art of ring oscillators is presented in section 4.2.1.3.

4.2.1.1 DCO main characteristics

The input bits of the DCO are switched to have the lowest output frequency (CT=15, Bias=1). CKV is directly connected to TDS754D oscilloscope and the viewed signal is illustrated in figure 4.2. Wherein, we see that the CKV has an amplitude of 94 mV P-P

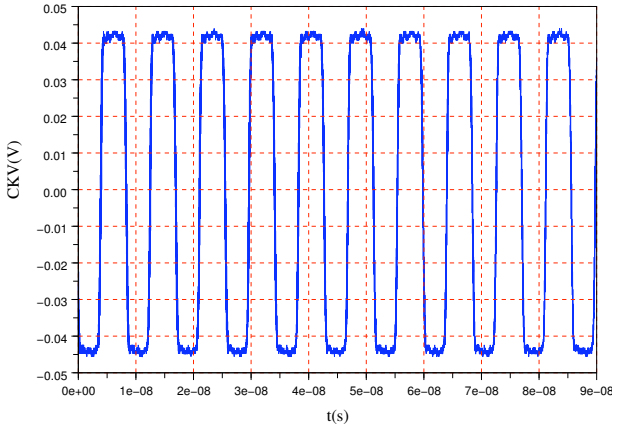


Figure 4.2: The measured signal CKV

and a frequency of 122 MHz. The simulation result presented in section 3.2.5 shows that this amplitude is about 400mV P-P. This value is obtained using a 100Ω pull-up resistor while it is equal to 475Ω in the measurement card. Simulation of the buffer using 470Ω resistor gives 110mV P-P.

The highest CKV frequency obtained using this card is around 470MHz (CT=1,Bias=31). In figure 4.3 we see the variation of CKV frequency as a function of Bias code. The ob-

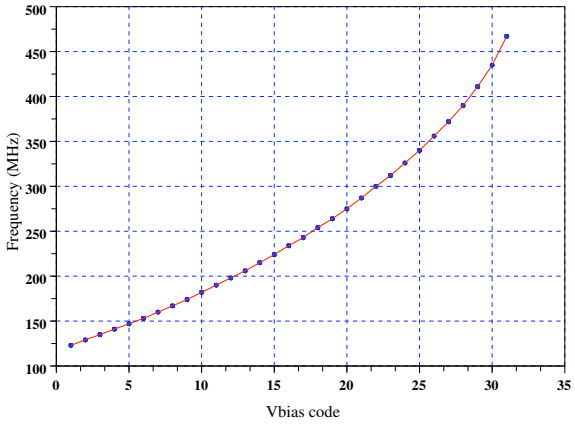


Figure 4.3: The DCO tuning range in function of the bias word with CT=1

tained range is from 122MHz to 470MHz and it is different from the predicted one (from

400MHz to 800MHz).

CKV phase noise in the open loop is measured at frequency offset ranges from 100kHz to 10MHz from 470MHz carrier frequency and it is illustrated in figure 4.4. Phase noise at 5 MHz from 470MHz carrier frequency is equal to -117dBc/Hz and reaches -125dBc/Hz at 8MHz. These values are 3dB above the predicted value presented in section 4.1.2.

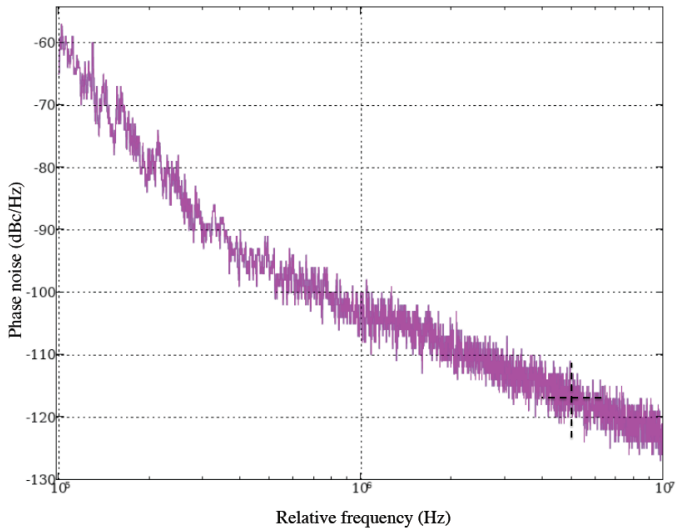


Figure 4.4: Measured phase noise of CKV for f_{CKV}=470MHz

The DCO is considered as the sensitive block of the circuit, it could be perturbed by other blocks (victim) and it perturbs the other blocks because of its high frequency operating (provocative). One way to minimize the interaction between the DCO and the other blocks in the circuit is to feed the DCO separately. Thus, we use three different power supply pins to feed the integrated circuit. One for the DCO core (named V_{dda}), one for the buffer (named V_{ddRF}), and the third one is for the other blocks of the circuit (named V_{ddd}). This way, the power consumption of the DCO core could be measured. The DCO consumes 1mA from 1.2V.

Table 4.2 compares simulation results to measurements. The amplitude and the power consumption are validated while the phase noise behavior is 3dB above the predicted one and a large difference between the predicted tuning range and the measured one is obtained. This shift may be due to insufficient control voltage (V_{bias} and V_{CT}). This means, the DACs

Table 4.2: Comparison between simulated results and measured results

DCO	Phase noise	Power consumption	Tuning range	Amplitude
Simulation	-120dBc/Hz	1mA	400MHz - 800MHz	94mV
Measurements	-117dBc/Hz	$<$1mA	122MHz - 470MHz	110mV

don't provide the correct voltages that allow high frequency operation. We presented in

section 3.2.5 the tuning range of the DCO as a function of V_{bias} and V_{CT}. We viewed in figure 3.18 that high frequency operation of the DCO (f_{CKV}>600MHz) corresponds to V_{bias} <0.4V and V_{CT}>0.5V. For example, for f_{CKV}=650MHz we have V_{bias}= 0.4V and V_{CT}= 0.7V). If one of the DACs can not provide the necessary voltage (if V_{bias}> 0.4V or V_{CT}< 0.7V) lower frequency is obtained.

CKV harmonics are viewed in figure 4.5. Wherein, CKV has a peak at 263MHz and an amplitude of -16dBm under 50Ω and the second harmonic is 32 dB below the carrier. This figure is picked up in the absence of FREF.

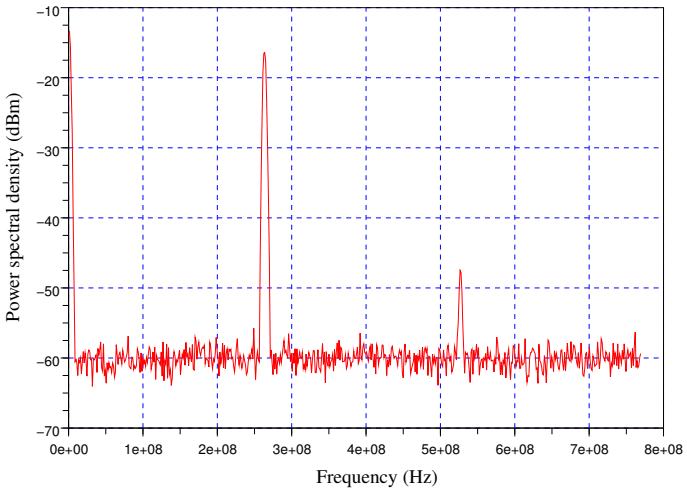


Figure 4.5: Measured CKV power spectral density. CKV has a peak at 263MHz and an amplitude of -16dBm

Figure 4.6 contains CKV power spectral density trace in the presence of FREF. CKV has a frequency of f_{CKV}=473MHz and an amplitude of -15dBm. We see in this figure spurious at $\pm(f_{ref}, 2f_{ref}, ..., etc)$ offsets from the carrier f_{CKV}. The amplitude at $f_{CKV} \pm f_{ref}$ is about -50dBm. Thus, it is 35 dB less than the carrier amplitude.

4.2.1.2 Variations of oscillator frequency with Vdd

The variations of CKV frequency in respect to power supply are illustrated in figure 4.7. Frequencies are measured as a function of the input code Bias with CT is equal 15. The power supply of the DCO core is varied from 0.8V to 1.3 V. We see in figure 4.7 that the DCO has higher frequency tuning range for higher Vdd.

V_{dda} feeds both the DCO and the DACs so the increase of CKV frequency is due to both a faster DCO and a higher Bias and CT commands.

4.2.1.3 DCO figure of merit

It is not easy to compare the performance of different oscillators. The oscillator design space inculdes phase noise, power consumption, and oscillation frequency, and to a lesser extent,

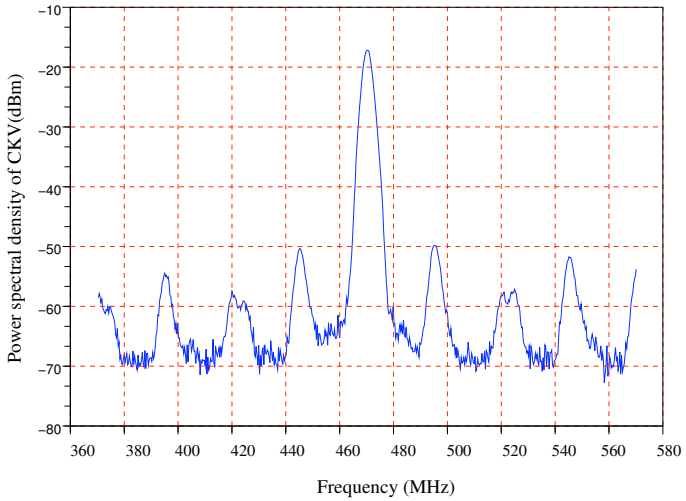


Figure 4.6: Power spectral density of CKV in the presence of FREF

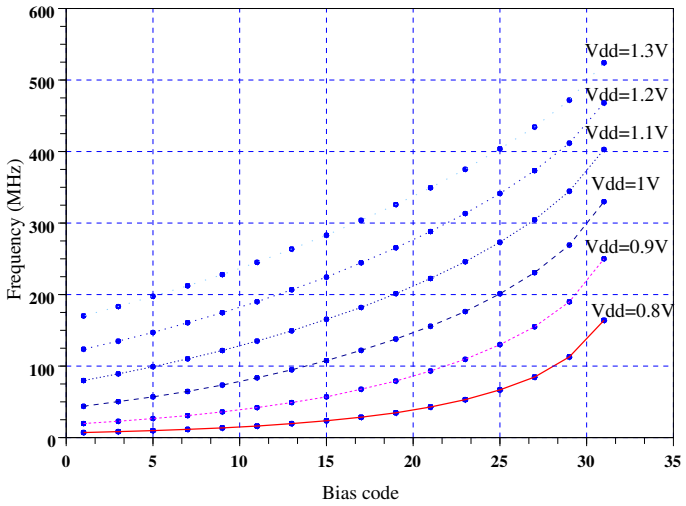


Figure 4.7: Variation of the tuning range of the DCO as a function of DCO supply V_{dda}

tuning range. Comparison of simulation results is easier. For example, we presented in section 3.2.1 the table 3.2 that contains comparison between simulation results of different architectures of ring oscillators designed in 65nm technology. Their center frequencies are around 2GHz. The performances of these oscillator in terms of phase noise are compared at the same offset frequency. Whereas, comparison of measurement results could not be done by the same way. The oscillators have generally been fabricated with different technologies and they are characterized for phase noise performances $L(\Delta f)$ at different frequency offsets Δf from different center frequencies f_0. Thus, the best way to compare these oscillator is the figure of merit.

One definition of a normalized figure of merit (FOM) is proposed in [81]

$$FM = 10\log\left(\left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{L\{@\Delta f\}P}\right) \tag{4.1}$$

Where P is the power consumption for the oscillator core alone and does not include the output buffer.

According to equation 4.1, FOM of the realized DCO is equal to 168.

Related works We present in table 4.3 a comparison between our designed DCO and other ring oscillators in terms of figure of merit presented in equation 4.1.

Table 4.3: Comparison of measured performances of ring oscillators

Ref.	TR (GHz)	$L(\Delta f)(dBc/Hz)$	Δf (MHz)	FOM	Power(mW)	Tech
[82]-2002	9.8-11.5	-98	2	153	75	0.5μm
[83]-2003	0.1-3.5	-106	4	152	16	0.18μm
[84]-2004	3.1-6.3	-101.4	1	155	157	0.18μm
[85]-2009	1.7-5.5	-120.2	4	162	81	0.18μm
This DCO	**0.1-0.5**	**-120**	**5**	**168**	**1.2**	**65nm**

For the same tuning range, the proposed DCO has better phase noise and lower power consumption compared to the ring oscillator of [83]. The main factor in the reduction of the phase noise is the design strategy based on the reduction of the ISF in order to have symmetrical rising and falling edges reducing thus the up-conversion of the ω_{1/f^3} corner. Another reason for the high FOM of the DCO is its low power consumption compared to other ring architectures that is due to the oscillator architecture.

4.2.2 TDC performances

The TDC register bits are the DCO states and they are named TDC(0),TDC(1),...,TDC(8). In practice, in the absence of metastability problem and of undefined states, we have 18 possible equiprobable states of the ring. Here we test the absence of prohibited states and the equiprobability of the 18 states.

In figure 4.8 we illustrate the histogram of DCO states for FREF=25MHz and with 50% duty cycle performed on 8000 samples. Wherein, we see that there is no prohibited states, however, states are not equiprobable. This problem has two reasons: Firstly, the TDC contains buffers at the output of each stage of the ring to determine the high/low state of the stage (cf. figure 3.25). If the buffers have different thresholds for rising and falling edges (different from 0.5 V), this causes a worse decision on the state and produces non equiprobable states. Secondly, the statistical dispersion of the delay time of DCO stages is in favor of non equiprobable states.

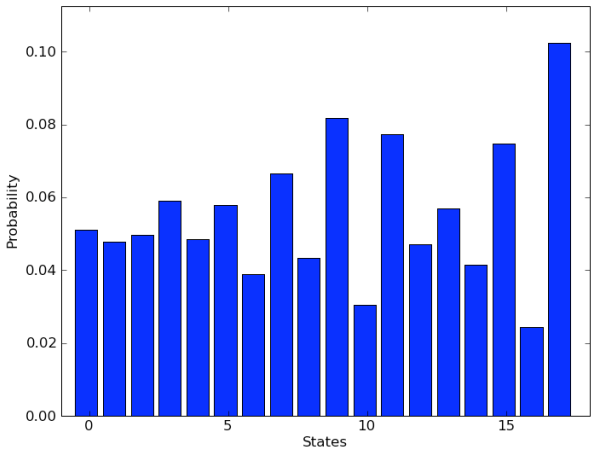


Figure 4.8: Histogram of ring states measured over 8000 samples

4.3 The digital counter

As we say in section 3.5.1, the digital counter is made by VHDL synthesis. Modelsim simulation is also presented and it shows the desired functionality of digital counter.

However, measurements shows the non functionality of the digital counter. Unfortunately, the counter is not simulated at electrical level. In order to diagnose the problem, we use Quartus to synthesize this counter and we obtain the block diagram illustrated in figure 4.9. In fact, because of the interpretation of the code presented in section 3.5.1, the used synthesized tool doesn't provide the desired block diagram viewed in figure 4.9 and thus a bad functionality of the digital counter is observed.

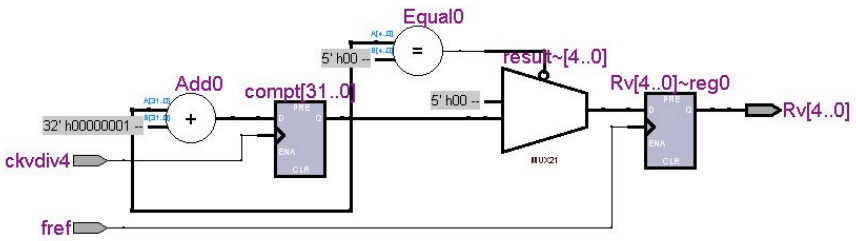


Figure 4.9: Block diagram of the digital counter implemented on the FPGA

4.4 The frequency divider

CKV/4 is viewed in figure 4.10. Its amplitude is 1V P-P under 50Ω load. We note that the frequency divider is followed by the same output buffer designed in section 3.5.2. This buffer has a pull-up resistor equal to 200Ω.

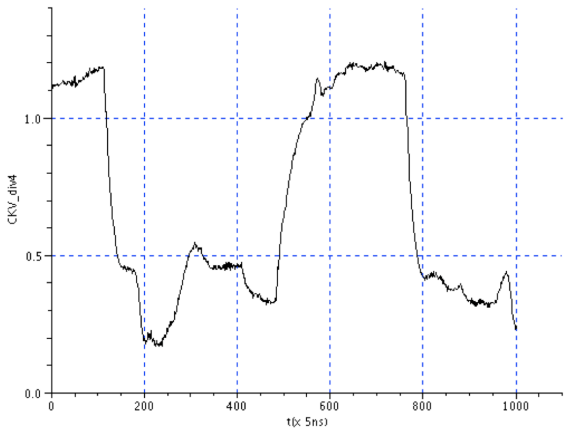


Figure 4.10: The measured CKV/4 signal

Phase noise measurements of CKV/4 signal is performed and it is illustrated in figure 4.11. It has -125dBc/Hz@5MHz from 118MHz carrier frequency.

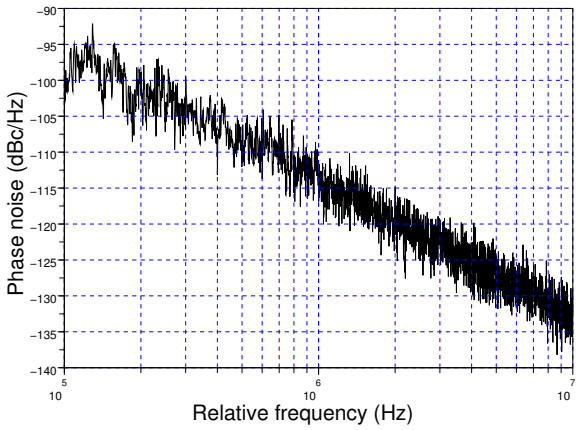


Figure 4.11: The measured phase noise of $CKV/4$ signal. CKV frequency is equal to 472MHz

4.5 Conclusion and perspectives

This chapter presents a comparison of designed and measured characteristics of the ADPLL blocks designed for TV applications. The DCO performances in terms of phase noise and power consumption are validated and the FOM of the DCO is 6dB more than that presented in [85]. Measured power consumption of the designed buffer is equal to simulation results. Measurements of the ADPLL closed loop can not by done because the digital counter is not functional.

This work can be considered as a first step in the design of portable ADPLL for TV application. As a first perspective we propose to test the closed loop behavior in low power conditions. For lower power supply, the DCO provides lower frequencies as we presented in section 4.2.1.2. Therefore, for frequencies around 250MHz (V_{dda}=0.7V), the digital counter can be implemented on the FPGA that allows tests of closed loop performances.

Secondly, enhancements on the DAC architecture to cover the TV band application can be performed.

Thirdly, the design of $\Sigma\Delta$ modulator to dither the LSB bits of the DCO control word CT is necessary to have fine resolution signal.

Finally, an implementation of the complete ADPLL on the same integrated circuit reduces the huge area occupied by the digital input/output pins used to interconnect the circuit part with the FPGA part.

Conclusion

The design of ADPLL continues to make a challenge. Digitizing most of its blocks becomes more interesting and benefiting. Within, the DCO and the TDC continue to be the noisiest elements. A state of the art of the ADPLL, the DCO, and the TDC are presented in the first chapter. We started from the ADPLL architecture of [3] that is developed progressively to cover Bluetooth,GSM, and 3G applications. Modeling of this ADPLL taking into account the linear time variance of phase noise is not yet presented. The state of the art of DCO leads us to decide to use the hybrid approach in the design of our DCO for TV applications. Some of TDC architectures are also reviewed and compared. Most of them are precise but they all of them are complex, occupy large area, high power consumers.

In this work we propose to carry the electrical characteristics of the DCO that are considered as low level modeling results to higher level. Within, the ISF is determined and used in the DCO phase noise modeling. Then, the linear time variance of phase noise of the DCO is implemented in the ADPLL model. Thus resulting a rigorous and generic model of phase noise. The proposed solution is independent of the DCO architecture, of the technology, and of the application. An implementation of the model is proposed for 2GHz application with LC oscillator. The ISF carries the characteristics of the DCO phase noise and the LTV model based on the ISF conserves it fairly providing a complete model of phase noise in the two regions $1/f^2$ and $1/f^3$ and the position of the corner ω_{1/f^3}. The model is simulated using VHDL-AMS language for its portability and capability to describe analog, digital and mixed signals. Finally, the ADPLL model is fast, predictive, and generic .

A design of ADPLL for TV applications is also presented. Wherein, the DCO is designed using the ISF function for low noise and low power consumption. The used DCO is hybrid and contains a VCO core controlled digitally by DACs. It is a NOR interpolative ring oscillator. It has a nine stages ring that interpolates with seven stages ring producing a larger tuning range than inverter based ring oscillator. Benefiting from the ring architecture, we propose to merge the DCO and TDC architecture. The DCO state is read at the rising edge of FREF and then the distance of the propagated edge in the ring from the FREF rising edge is deduced. The merged TDC/DCO architecture reduces the area, the power consumption, and the complexity of the ADPLL.

Comparison between the realized DCO and other ring oscillators that are published is performed in terms of figure of merit. TDC results validate the concept of merged DCO/TDC architecture concept allowing lower area and lower power consumption of the ADPLL.

Perspectives

This work can be considered as a first step in the design of portable ADPLL.

As a first perspective of this work we propose to develop a complete model of ADPLL taking into consideration the different locking modes (calibration, fast lock, fine lock). Implementation of different order $\Delta\Sigma$ modulators can be performed to simulate the effect of LSB bits dithering on the resolution of the synthesized frequency.

In addition, an automatization of the extraction of the ISF is performed in this work and it can be completed to an automatization of the design of ADPLL. Within, the presented design strategy determines the design variables, then ,Scilab and Spectre provide together the ISF, then, Scilab functions determine the Fourier transform coefficients necessary for the ADPLL model that can simulate the phase noise and the time response of the loop.

The target application of this work was TV application but the ADPLL model is generic and the DCO oscillator has large tuning range and low power consumption. Therefore, it would be interesting to focus on other applications such as RF multi-standard, wide-band applications.

Appendix A

Design strategy of LC oscillator for minimum phase noise

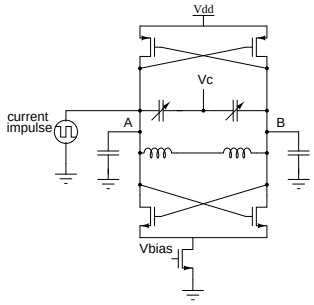


Figure A.1: The cross coupled LC oscillator

The LC oscillator is presented in figure A.1. Design constraints are the phase noise, the tuning range, the power consumption and the central frequency. The simulated circuit is developed using CMOS 90 nm technology.

The first step in our design was the choice of the inductor L. In our simulator environment we have to choose between seven inductor models. The inductors are not optimized to have very high quality factor (Q=7). However, they have different values L and different parasitic conductances g_L. We included in our model the inductor which realizes the minimum Noise/Carrier Ratio (NCR). This NCR is proportional to the value of Lg_L^2 [18] and is thus minimized if we take the inductor of the minimum Lg_L^2 value. Then, the minimum start-up condition α_{min} is defined by the following equation

$$\alpha_{min} = g_{active}/g_{tank,max} \tag{A.1}$$

where g_{active} is the effective conductance of the active circuit, and $g_{tank,max}$ is the maximum resonator conductance. In our design $\alpha_{min} = 2.5$. The maximum phase displacement occurs when the VCO signal crosses zero. This is why we expect to have the most symmetrical properties of the circuit at this operation point. This symmetric property can

be achieved if the transconductances of the transistors are equal ($g_{mn} = g_{mp}$) at the zero crossing point. In this case, the PMOS canal width is proportional to the NMOS canal width. The NMOS canal width can be calculated from the start-up condition and the value of g_L. The value of the varactor is determined from the tuning range we impose in the design constraints.

Finally, the oscillator has a relative tuning range equal to 22%, a phase noise equal to -121 dBc/Hz@600kHz from the carrier frequency, a maximum output voltage $V_{max} = 1\ V$, a power supply of 1.2 V and a bias current I_{bias} of 5 mA.

Appendix B

Scilab code for the calculation of DCO phase noise

```
clear all;
xbasc(0:1);

ckv=fscanfMat('crossing2.txt');
ckv=ckv(2000:$,1);
npts=length(ckv);
printf('data length: %d\n',npts);
T=mean(ckv(2:npts)-ckv(1:npts-1));
ckv=ckv(2:npts)-ckv(1);
cki=T*(1:npts-1);
ej=ckv(:)-cki(:);
decfactor=10;
ej=intdec(ej,1/decfactor);
npts=length(ej);
printf('vector length after decimation by %d: %d\n',decfactor,npts);
scf(0);plot2d2(ej);

ephi=2*%pi*ej/T;
Fdco=1/T;
Fdec=Fdco/decfactor;
pxx=cspect(int(npts/100),int(npts/4),'tr',ephi);
smsize=int(length(pxx)/2);
pxx=pxx(1:smsize);
fr=Fdec*(1:smsize)/(2*smsize);
pdb=10*log10(pxx)-10*log10(Fdec); // psd dB/Hz
scf(1);plot2d(fr,pdb,logflag='ln');xgrid(2)
```

Appendix C

Block diagram of TDC encoder programmed on FPGA

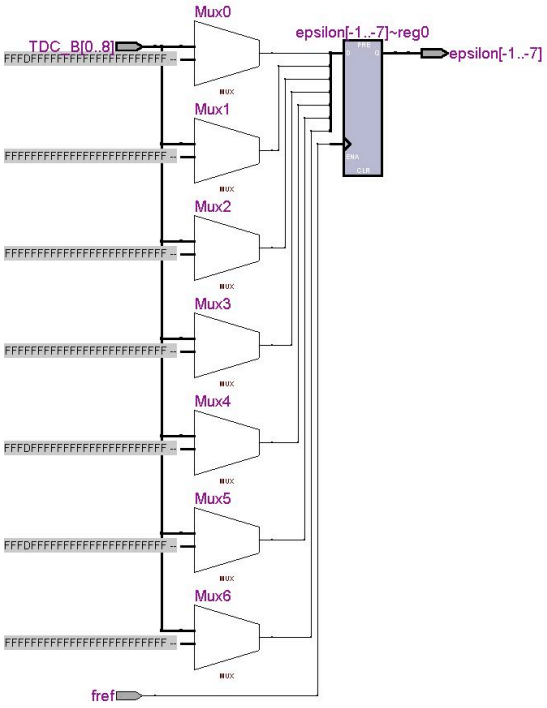


Figure C.1: The block diagram of the TDC encoder synthesized by Quartus and programmed on Stratix II

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