Chapter 4

Fabrication of a porous stack for one-dimensional nanostructure growth

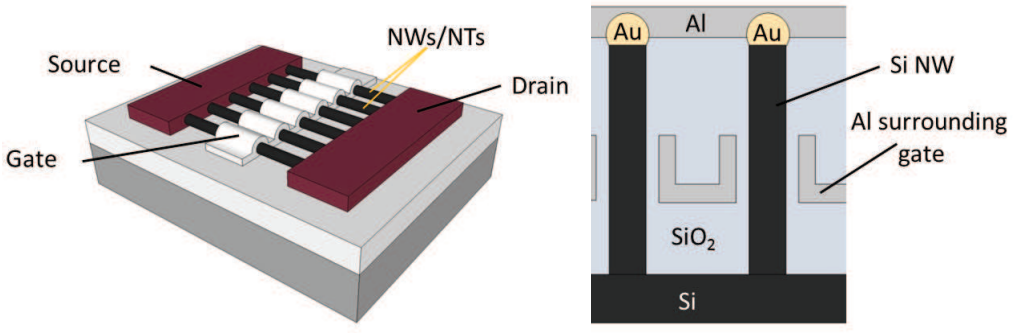
In this chapter, the first section is dedicated to a brief introduction for a sum-up about what has been reported concerning NW/NT-based FET so far in the literature. Then we present our attempts and investigations to realize a porous structure that is able to receive NWs or NTs, but also that provides the features required to connect these nanostructures in three different places. Indeed, we have seen in the previous chapter that SiNWs could electrically link the top of the PAA to the underlying silicon substrate, which is a two-electrode connection. Of course, to make a FET, a third electrode is required to realize a gate effect, and a way has therefore to be found to connect the NWs at a third point. The method we chose consists in a porous stack, realized on the basis of a PAA template that will help to realize vertical straight pores inside several thin layers. This will be discussed in the second section of this chapter, after the introductory first section. In a third section, we will develop our experiments carried out for the CVD growth of nanostructures inside a porous stack, and the techniques we used to treat the samples so as to perform a selective growth in predefined patterns.

4.1 Introduction

4.1.1 1D nanostructure-based FETs: a state of the art

Historically, the first electrical characterization of 1D nanostructures was performed on CNTs in the late 90s, and led to many publications. Particularly, essential articles come from McEuen's, Dekker's, Avouris' and Thess' teams ([1], [2], [3], [4], [5], [6], [7]). The transport measurements performed by Bockrath [1] or by Tans [3] were very promising for the CNT integration into active electrical components, and convincing improvement have been brought by Avouris et al. [7], as far as getting performances better than for state-of the-art planar bulk devices, and fabricating logic circuits. However, the use of

CNTs in nanoelectronics comes up against the fact that the selectivity between semiconducting and metallic CNTs, which depends on their helicity, is not totally controllable yet. Besides, the controlled doping, which is essential for electrical devices, is not achievable in nanotubes. Therefore, a few years later, research about transport properties in intrinsically semi-conducting nanowires has been performed and brought interesting results, notably concerning key device parameters extracted from measurements performed on NW-based FET. The most memorable progresses have been done by Lieber's group, which carried out electrical transport measurement in semi-conducting NWs, and used them as building blocks for fabricating a wide variety of nanoscale electronic devices such as diodes, bipolar transistors and inverters [8], LEDs and FETs [9], logic gates [10]... The NWs were synthesized by the laser ablation technique (see chapter 3), SiH_4 being used as a reactant for Si or Ge NWs synthesis [11], and special targets containing both the material of interest and catalyst for other types of NWs (III-V compounds...) [12]. p- and n-doping have been achieved by adding B_2H_6 and in the reactant flow and using a phosphorous-doped target, respectively. Once synthesized, the NWs are collected onto an oxidized Si substrate, and then contacted thanks to a set of electrodes defined by e-beam lithography. To carry out gate-dependent measurements, the Si substrate was used as the third electrode in a back-gate configuration, insulated from the NWs by the oxide layer. Nevertheless, though fabricating demonstrators is a great stride, the manipulation and assembling techniques used to connect two or more NWs remain quite complex, and are not transferable for collective, rapid and high-density integration. Besides, the conventional planar configuration adopted in most studies leads to a partial gate coupling, which is not optimal regarding power losses and global consumption ([13], [14]). Some solutions have been proposed a few years ago to improve this gate coupling, using multiple-gate structures (triple-gate [15], also known as Π-gate [16], [13], [17]), semi gate-around structure [18]...), or completely surrounding-gate structure on vertically-oriented SiNWs [19], [20], [21], [22] or ZnO NWs [23]. A drawing of the planar, semi gate-around and the vertical, gate-all-around (GAA) structure is visible in Figure 4.1.



(a) (b)

Figure 4.1: (a) Planar configuration and (b) vertical configuration of NW-based FETs, as described in [24] and [20], respectively.

The so-called GAA structure contributed for example to reach a subthreshold slope as low as 50 mV/decade, in a vertical SiNW FET [25].

4.1.2 The concept of the vertical FET

The ingenuity of the structure that we want to use so as to fabricate our vertical FET is that it can resolve several problems by itself all in the same time, including those mentioned above. Before going further, let's have a look on the 3D diagram represented in Figure 4.2. The structure consists in a porous stack, where one can recognize the already-known PAA (white). Parallel, straight and vertical pores cross all the stack from the PAA down to the substrate, and are fabricated in order to receive one 1D nanostructure each. The source electrode can be realized from any metal deposit, like Au, Pt or Al, commonly used for creating metallic contacts. The gate electrode is necessarily in Al, since it comes from the non-anodized Al layer used for the PAA synthesis. Finally, the drain electrode can be either a conductive layer deposited on an insulating substrate, or directly the substrate, provided it's conductive. The source and gate electrodes, and the gate and drain electrodes are separated one from each other by the PAA and by an SiO_2 layer, respectively. The fabrication process is as follows: highly-doped (10^{16}-10^{17}.cm^{-3}) p-type Si wafers are thermally oxidized in order to create a 100 nm-thick SiO_2 layer on its surface. This step is made by the substrate manufacturer, so we receive the substrates already oxidized and clean. Then, a high-purity Al layer (several hundreds of nm, up to 1 µm) is evaporated in an e-beam evaporation chamber, under the same conditions as described in chapter 1 for PAA fabrication. The stack "Al/SiO_2/Si" thus constitutes

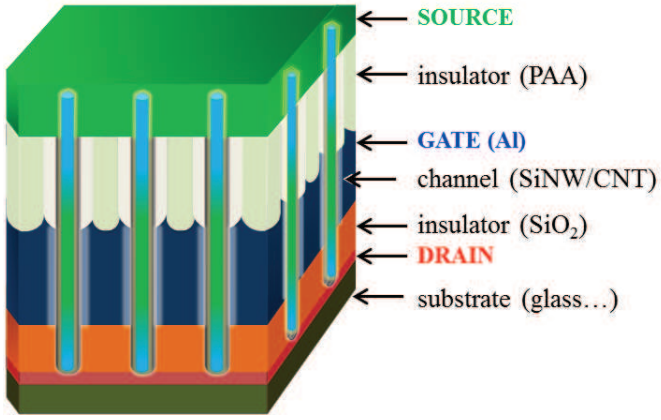


Figure 4.2: 3D diagram of the porous stack. The 1D nanostructures (light-blue) grow in the vertical pores that provide the gate contact (Al, dark blue) and insulating layers between the source and drain electrodes.

the "gate/insulator/drain (or source)" structure. Here comes one of the particularity of the process. The Al layer is subsequently partially anodized to form a PAA layer, which will be used afterwards as a hard mask for successive anisotropic etchings. Thus, the pore length can be extended through the whole stack and therefore form vertical

pores crossing the non-anodized Al and the SiO_2 underlying layers. The vertical porous template is ready to receive 1D nanostructures, which growth will be discussed in the next section of this chapter, as well as the preliminary catalyst electrodeposition. Once the growth is achieved, a metal deposition is planned to contact the top of the protruding nanostructures and thus create the source (or drain) electrode to complete the FET.

This stack thus provides the surrounding gate structure that ensures the best gate coupling, as discussed earlier. Fabricated in this way, this template enables the fabrication of a single FET per pore, which, knowing the potential ultra-high pore density of PAA (up to 10^{11} per cm^2), is very interesting. Since Al and SiO_2 pores were born from the PAA, all inherent advantages of the latter are consequently transferred to the whole porous stack. Thus, the pores are the same diameter, which leads to nanostructures identical in diameter, the dimensions are adjustable to the needs, and no costly lithographic techniques is required to obtain the good ordering of the pores. As mentioned in chapter 3 for simple PAA, collective organization, orientation and connection is also possible with this stack structure, while the location of NWs or NTs is controlled by the pore arrangement itself. This process is fully-CMOS compatible since no high thermal budget is required for the template fabrication, nor for the nanostructure growth (growth can be performed below 500°C). Besides, the as-obtained structure acts as a passive template for controlling the nanostructure growth, but also as active element for the device.

In the following are described in details the different steps to fabricate the porous stack, and the experimental results we obtained from our attempts to fabricate it.

4.2 The porous stack fabrication

Since the PAA fabrication has already been detailed in chapter 1 and doesn't differ much here, we will focus on the two successive etchings steps, that is the etching of the Al layer, and the etching of the SiO_2 layer. Both are achieved using an inductively-coupled plasma (ICP) reactor, which principle is presented hereafter with other uses of plasma in microelectronics. Finally, the experiments carried out to efficiently etch Al and SiO_2 will be presented in details.

4.2.1 Plasma processing in microelectronics

Plasma deposition

We have already mentioned PECVD in chapter 3, that uses the energy of a plasma to create radicals for subsequent film growth, which allows to decrease the temperature of the CVD process. Another plasma-based deposition technique is called sputtering. Very basically, it consists in accelerating heavy ions (typically Ar^+) generated in a plasma, towards a metallic target. This target, composed of the material one wants to deposit, is thus partially pulverized (by a simple transfer of momentum), and atoms can deposit forming a thin film. Oppositely, plasma can be used in direct contact with the sample to process, like in plasma-assisted etching. This specific use of plasma will be more detailed

since it constitutes the heart of the processing of our porous sample described in the previous section.

Plasma etching

Plasma etching is a general term used to designate any material removal achieved thanks to a plasma. It requires a plasma source, which species will react with the sample giving volatile products. The elimination (by pumping) of these by-products leads the etching of the sample. Since the reactions occurring during this process mostly involve the ions of the plasma, this process is usually called reactive ion etching (RIE). RIE is a very widely spread technique in the domain of microfabrication. Inside a vacuum chamber, a plasma is generated from a particular gas mixture by an electromagnetic discharge, and reacts chemically, physically, or both with the sample positioned in the chamber. Figure 4.4(a) shows a typical RIE reactor, with the two (bottom and top) electrodes necessary for the plasma ignition. This set-up is called "capacitively coupled" plasma, because of the parallel electrodes configuration. Once the chosen gases are introduced inside the chamber, a strong RF (radio-frequency, typically 13.56 MHz) electrical discharge is applied between these two electrodes, provoking the ionization of the gaseous species, and thus creating the plasma (typical density of $\approx 10^{15}$-10^{16} m^{-3}). A plasma consists in a mixture of cations and electrons, coming from the gas molecules that have been ionized. The impacts between these species lead to several events: electrons and ions can recombine into neutral atoms or molecules, which is a radiative event and is responsible of the plasma glow (the color is characteristic of the species concerned). The electrons can also hit atoms or molecules and ionize them, thus contributing to the generation and the stability of the plasma.

Self-bias and plasma sheath

Contrary to plasmas existing in outer space, plasmas created in laboratories have boundaries, played by the chamber walls themselves. The presence of these walls induces some capital local properties to the plasma that are worth to be mentioned. Usually the top electrode is grounded and the bottom one supports the wafer to etch. Every half-period of the RF signal, the electric field direction changes and the electrons, very light and fast, are therefore accelerated up and down following the field direction. If they hit the top electrode on their way up, or even the chamber wall, nothing special happens since both are ground-connected, and they only vanish in the electrical circuit. On the reverse, if they hit the bottom electrode, which is insulated from DC component (by a capacitor), they will accumulate and create a negative charge on the bottom electrode. This negative charge creates what is called the "self-bias", and a negative potential is therefore created in the bottom electrode (typically a few volts up to hundreds volts). The cations, due to their much greater mass, can't follow the field variations. Nevertheless, the self-bias strongly attracts them, which leads to their displacement towards the bottom electrode, and particularly towards the wafer, which lies on it. An ionic bombardment is therefore observed, which is responsible of the physical etching of the sample. The cations also form

a layer of positive charges, that exactly compensates the negative self-bias. This thin layer (typically a few tenth of mm, depending notably on the electrons concentration) is commonly called "sheath" (or Debye sheath) and is considered as being the transition between a plasma and a solid surface (or vacuum). During one RF cycle, the structure of the sheath varies, contracting and expanding with the RF variations. Its potential also changes: the amplitude of this variation is called "peak-to-peak voltage", and is important, as well as the self-bias, for monitoring the plasma. Figure 4.3 represents a general situation for a plasma near an electrode insulated from DC component.

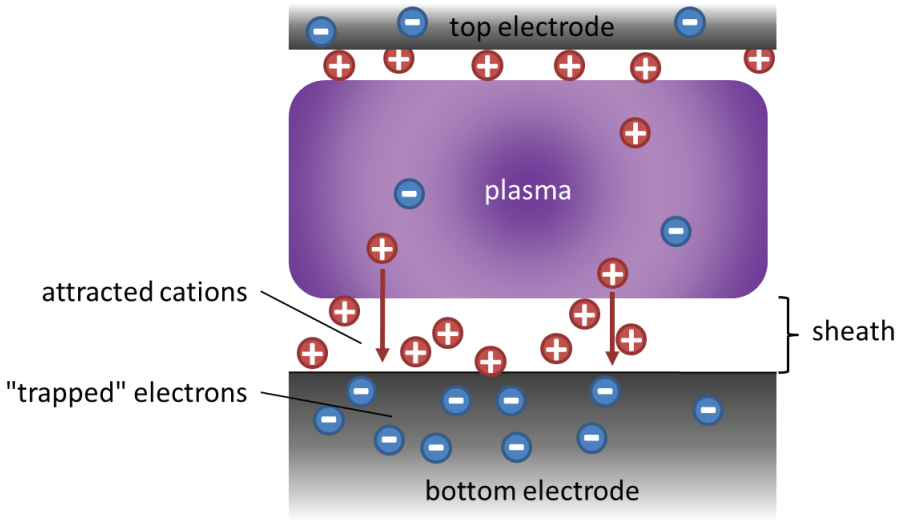
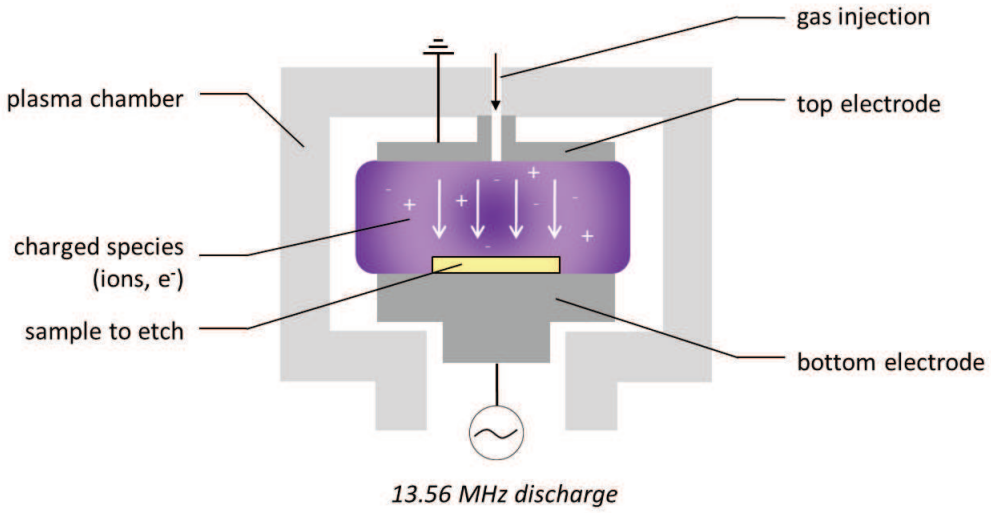


Figure 4.3: Schematic diagram of the formation of a plasma sheath close to the electrodes. Electrons accumulate in the electrode because of DC field isolation, and thus attract positive ions.

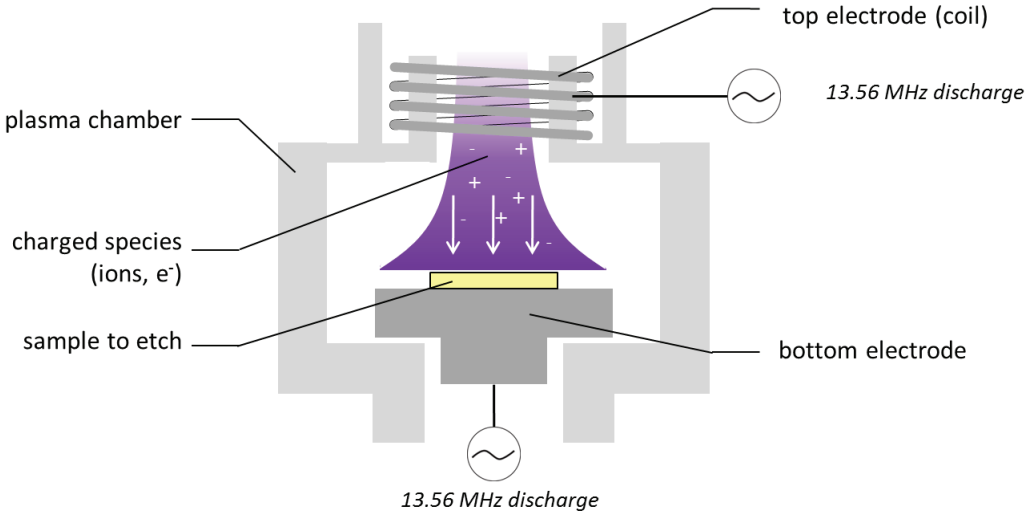
Chemical etching versus physical etching

If the gaseous species are chosen so that cations can chemically react with the wafer material, then a second type of etching, simultaneous to the physical etching, is possible. However, cations are not very chemically reactive because of their lack of electrons. The efficient chemical reaction occurs provided they catch some local trapped electrons from the wafer/bottom electrode and recombine into reactive species. These two different etching modes are very useful to adjust an etching profile, since one of the two can be favoured by playing on the multiple conditions that are the gas nature, the ratio between the species, but also the pressure and the RF signal power. Indeed, a stronger chemical etching will lead to a more isotropic etching, whereas the bombarding effect can be promoted using inert gas plasma, and/or applying a higher power between on the bottom electrode. A high bombardment would normally lead to more anisotropic etching, since the ions follows the field lines, that are perpendicular to the electrodes. Thus, a clever balance between the two etching modes theoretically enables to control

the angle between the surface of the wafer and the side walls of the etched area.



(a)



(b)

Figure 4.4: (a) Classic parallel plates RIE reactor and (b) ICP RIE reactor.

Deep etching

Other types of RIE reactors exist: the electron cyclotron resonance (ECR) plasma reactor uses ECR (created under specific conditions, i.e. the superimposition of a magnetic field and a high frequency electromagnetic field) to generate a plasma, that is then extracted towards the sample thanks to a magnetic field. Inductively coupled plasma (ICP) is a

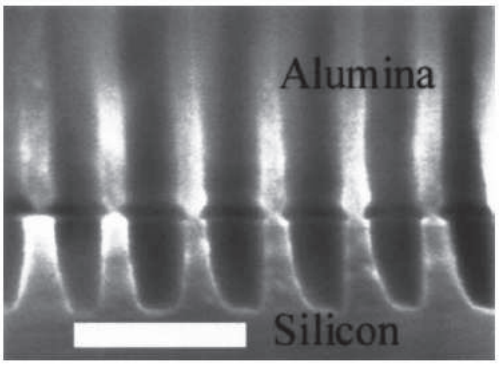


Figure 4.5: SEM cross-section of a Si substrate etched with a PAA layer as a mask, from [32]. Scale bar is 200 nm.

spin-off of the simple RIE described above. In an ICP reactor (see Figure 4.4(b)), the plasma is generated by a discharge provoked by a high variable magnetic field, induced by an RF current circulating through the coil located on the top of the chamber. It is then extracted towards the other part of the chamber thanks to a second electrode (usually called "platen") that is biased as in classical RIE (13.56 MHz). The interest of this configuration is that the electrode responsible of the plasma generation is away from the reaction chamber, and thus remains clean from any contaminant. It also allows to control the ion flux (controlled by the coil) and the ion energy independently, since the separate bottom electrode is independently biased for the extraction of the plasma. Besides, the ICP is known to provide a plasma with a higher density ($\approx 10^{16}$-10^{18} m^{-3}) than the classical RIE configuration. The sample is generally set perpendicular to the electric field direction, on a substrate holder located on the platten.

When combined with ion bombardment (i.e. physical etching), chemical reactions can lead to high anisotropy etching, and therefore to high aspect ratio structures. This is why RIE is a tool of choice for realizing vertical pores. It is commonly used for MEMS (Micro Electro-Mechanical Systems) [26], RAM fabrication, photonic crystals [27], [28] and to dig deep trenches in integrated circuits for 3D technology (Through Silicon Vias). Instead of using costly means like lithography to define patterns in photo-resist, the self-organized porous structure of PAA has been used as an etching mask so as to realize vertical pores in semiconductor substrates. In 1998, Nakao et al. [29] placed a PAA membrane onto GaAs or InP substrates and performed RIE to transfer the porous pattern of the PAA to these III-V compounds. More recently, nanohole arrays with diameter as low as 30 nm have been fabricated in GaAs using basically the same technique [30]. Let's cite Cheng and Moskovits, who used this process to deposit Au quantum dots at the bottom of GaAs nanopores [31]. Similar results have been obtained in silicon (see Figure 4.5), without the complex step of the PAA transfer onto the substrate [32]. We remind the reader that this PAA masking technique is the method we used to realize vertical pores in stacked layers. In order to understand the etching conditions we selected in our process, it is necessary to have a few words about the deep RIE (DRIE). To fabricate trenches with high aspect

ratio in a substrate, a more complex process is required to prevent the degradation of the sample. Indeed, we have already seen that a balanced ratio of chemical etching (which is isotropic) and physical etching (more anisotropic) has to be found. However, even long after the etch has begun, the chemicals keep on reacting with the top of the trench, leading to its progressive degradation. Some solutions have therefore to be found to limit this isotropic etching while the rest of the trench is being etched. One of them is called the cryogenic process, where the sample is cooled down to freezing temperatures (-110°C) in order to limit the chemical reactions while allowing the physical bombardment to be performed. Another one has been patented in 1996 by the German company Bosch, and therefore holds its name. The Bosch process is based on a continuous protection of the as-etched walls of the trench, which prevents the chemical species from reacting with them. Besides the etching gases, another gas (typically CHF_3 or C_4F_8 for silicon etching) is inserted in the reaction chamber in order to deposit a passivation layer on the side walls. This mechanism is drawn in Figure 4.6. Carbon-based gases are often used as they form carbon-based polymers (Teflon-like, CF_xH_y when associated with fluor [33]), that efficiently protect side walls against etching. To control the thickness of this passivation layer, and thus to prevent the clogging of the holes, a last gas (typically O_2) is used to partially sputtering it off. The ratio between these two gases has therefore to be carefully controlled, to allow the third gas to preferentially etch the bottom of the trench. Similar conditions have been widely used in the literature ([34], [28], [35]).

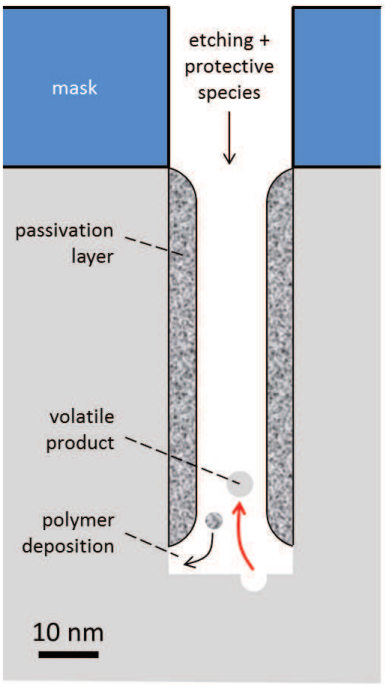


Figure 4.6: Schematic diagram of the Bosch process. The bottom of the trench, which can be as small as 20 nm large in our case, is etched while the side walls are protected by the passivation layer. The passivation layer thickness is not to scale.

The following section presents the experiments we carried out to etch successively Al and SiO_2 through a PAA mask.

4.2.2 Results: the pore etching through Al and SiO_2

We will first describe the different equipments necessary to realize the anisotropic etchings we have talked about in the previous section, then we will show some successful results with straight pores crossing the multilayer, and finally we will introduce an alternative way to fabricate a porous stack, which deserve to be considered.

Description of the equipments

All the anisotropic etchings we performed for the pores fabrication have been achieved using an ICP reactor. For the sake of keeping the plasma chambers clean, the Al and the SiO_2 etchings were performed in dedicated equipments, since the species used in each case could contaminate the chamber walls for the other, despite a regular cleaning. Both reactors were Multiplex, fabricated by the company STS. We use the one dedicated to metal etching to etch Al and the other one to etch SiO_2. Both are equipped with a laser interferometry end point detection system, that allows to control the etching in real time by monitoring the interference signals from two interfaces. Thus, we can detect the moment when a particular layer is completely etched, that is when the laser intensity variations stop or abruptly change. The samples are introduced inside the chamber via a load-lock, that transfers the sample holder (a 6" ceramic disc) on the platen. During the etching, the wafer often heats because of permanent ion bombardment, therefore a liquid helium-based system is mounted right underneath the platen so as to cool down the wafer. The sample is usually fixed on the sample holder using vacuum grease, that allows good thermal transfer. The vacuum has to be carefully and homogeneously spread on the back of the sample to avoid local heating, and thus inhomogeneous etching. The etching parameters that are the total pressure, platen and coil powers, gas flow rates, and the etching time are of course controlled through a computer-assisted interface, which also allows to visualize the self-bias and the peak-to-peak voltage.

Al etching through PAA

It is well-known that chlorinated gases react with aluminium and that aluminium can be etched this way [36], [36]. Different gases can be used, such as $SiCl_4$, BCl_3, Cl_2... In our case, we used Cl_2 to etch Al, which can be modelized by this reaction:

$$2\,Al_{(s)} + 3\,Cl_{2(g)} \longrightarrow Al_2Cl_{6(g)}$$

$Al_2Cl_{6(g)}$ being a volatile product, it is easy to evacuate with the pumping system of the RIE reactor. Some secondary reactions may occur, but this one must be the predominant one here. As already discussed earlier, we need a balanced ratio between the latter chemical reaction and the physical bombardment. Indeed, the isotropicity of 4.2.2 wouldn't lead to vertical pores; we therefore added some argon in the plasma in order to

$Ar:Cl_2$ ratio	Pressure	Platen power	Coil power
8:4 sccm	3 mTorr	240 W	95 W

Table 4.1: Optimized conditions for Al etching through a PAA mask in our ICP reactor.

enhance the anisotropy of the etching. The ratio between Ar and Cl_2 had already been optimized by Marquardt [37], and set to $Ar:Cl_2$=8:4 sccm in some specific conditions to provide a proper etching of the Al through the PAA mask. As an illustration, Figure 4.7, extracted from [37], show the results for several $Ar:Cl_2$ ratios. We notice that a higher Cl_2 flow leads to deeper pores, but with damaged walls due to the predominance of the isotropic etching. A too small amount of Cl_2 does etch Al pores, but with a quite lower etch rate; it has been then decided to use the 8:4 ratio, which gives satisfactory results, that is straight and intact pore walls, and an etch rate sufficiently high to keep the PAA mask intact (this will be discussed deeper later on).

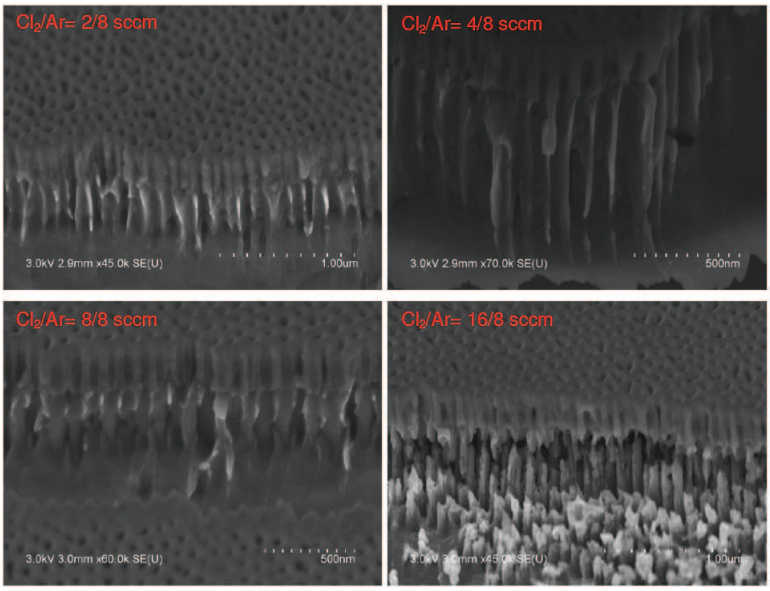


Figure 4.7: SEM cross-sections of PAA on an Al layer after an Al etching with different $Ar:Cl_2$ ratios. From [37].

The choices of the other etching parameters we used (electrode power, pressure...) are explained in [37], and have been used as a basis for further investigations. They are gathered in Table 4.1.

Despite a good selectivity of the Cl-based chemical etching regarding Al and Al_2O_3, we observe a clear decrease in the PAA thickness during the etching, very probably due to the ion bombardment. In order to anticipate the behaviour of the PAA mask during the Al etching, a calibration graph has been established, exhibiting the thickness of the PAA and the depth of the Al pores as a function of the etching time, for the conditions mentioned in Table 4.1. After anodizing an Al layer for 7'45 in sulfuric acid and etching

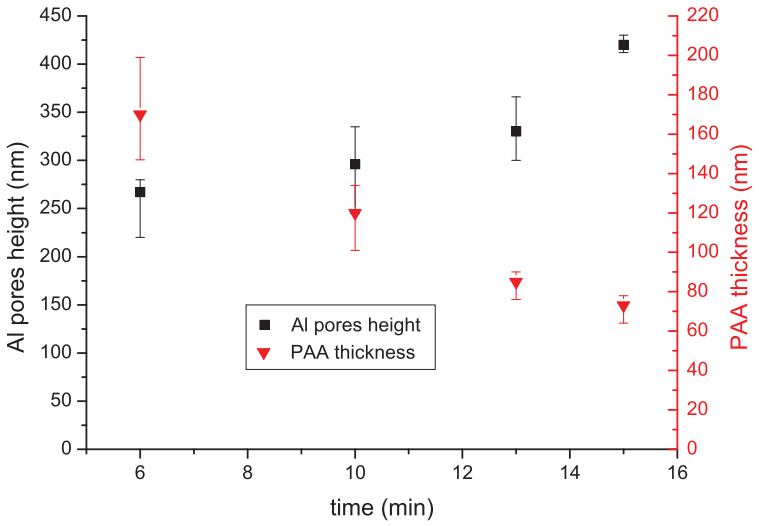


Figure 4.8: Al (black squares) and PAA (red triangles) thickness as a function of etching duration.

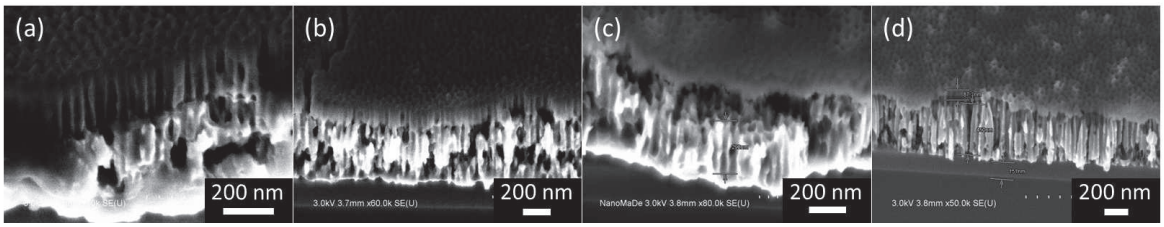


Figure 4.9: SEM cross-sections of PAA after (a) 6 min, (b) 10 min, (c) 13 min and (d) 15 min ICP etching of the Al layer.

the barrier layer for 15 min, several etchings have been performed for 6, 10, 13, and 15 minutes, respectively. One can notice both on the graph in Figure 4.8 and on the SEM pictures in Figure 4.9 that the pore height increases for increasing etching time, but also that the PAA thickness decreases, until it completely disappears (not shown here). For a proper etching duration, here 15 min, we notice that the Al is completely etched, that is the Al pores are open above the Si substrate. The bright, sheet-like Al layer visible right under the Al pores in Figure 4.9(a), (b) and (c), is not visible anymore. Once this step is reached, the underlying layer is not immediately etched thanks to the good selectivity of the etching species that doesn't react with it (in this specific case it is an SiO_2 layer). Nevertheless, one should carefully control the end of the Al etching, since an over-etching could damage the bottom of the Al pores, due to the reflection of the etching species against the bottom of the pores.

To succeed in these etchings, we performed a 15 min wet etching to remove the barrier layer (as explained in chapter 1). This step is essential to properly etch the Al layer,

since the barrier layer, made of alumina, is extremely resistant to plasma etching. As an illustration, we show in Figure 4.10 an SEM cross-section of a PAA template after a 4'30 Al etching. Visibly, the barrier layer etching was too short, since in this area of the sample, one can notice the remaining thin barrier layer. Some pores are visible in the Al anyway (white arrows), where the barrier layer was thin enough to be etched or completely removed by the wet etching. With this example we can feel the importance of homogeneity during all the steps that precede the Al etching, that is Al evaporation, anodization, barrier layer etching... since they inevitably impact its efficiency.

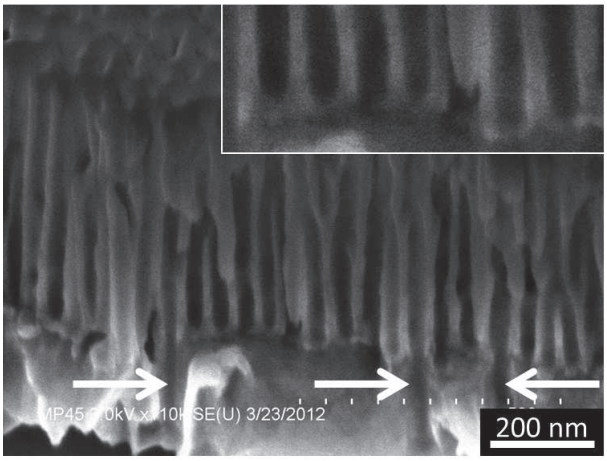


Figure 4.10: SEM cross-section of a PAA template after a 4'30 etching. White arrows indicate the places where Al has been etched, corresponding to places where barrier layer has been removed. The inset is a magnification of the central part of the picture.

Given the graph shown in Figure 4.8, we know the PAA thickness has to be carefully controlled if one doesn't want it to disappear, or to be too thin after the etching. In our case, it has to be sufficiently thick to put up with two successive plasma etchings (Al + SiO_2). We can notice that a porous structure in Al is achievable even with very thin PAA mask (see Figure 4.11). Indeed, once initiated thanks to the PAA mask, the porous structure is conserved even after the complete etching of the mask. However, in that case the Al is no longer protected and it is of course non-desirable to end up in this situation since the porous Al is destructed (from the top) as it is created (at the bottom). The inset in Figure 4.11(b) shows how Al is etched if the PAA mask is completely removed. The remaining nano-imprints on the surface of the Al layer lead to this needle-like structure

Straight pores, corresponding to the replica of a PAA mask, have been obtained in aluminium by ICP etching. In the context of the fabrication of our vertical 1D nanostructure FET, this means that the porous gate electrode has been fabricated over a large area, able to receive a large number of nanostructures. However, this structure has no interest as it is, and the next etching step, necessary to reach the underlying Si substrate remains to be done. This is the subject of the next section.

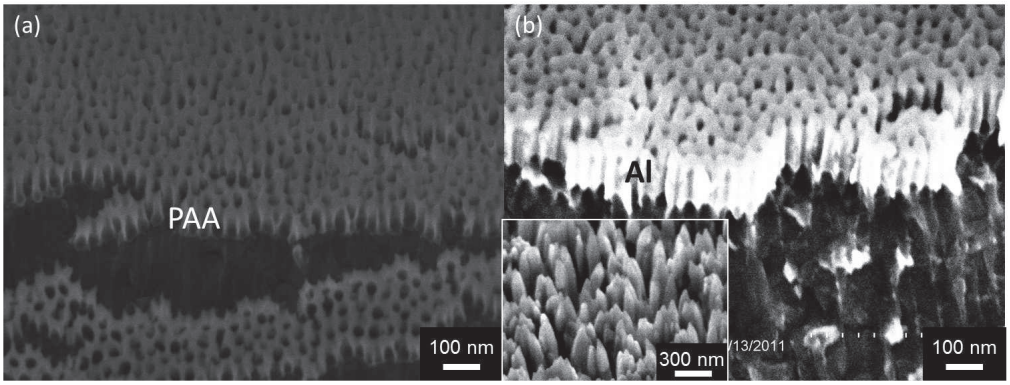


Figure 4.11: (a) Thin PAA ($\approx$ 85 nm thick) on an Al layer before the Al etching and (b) porous Al layer after a 2 min etching. The PAA has disappeared, leaving the porous Al ($\approx$ 170 nm thick) unprotected.

SiO_2 etching through PAA

This step has also been studied in [37], and SiO_2 etching in general has been widely studied. Nevertheless, the very specific conditions imposed by the porous structure prevent the use of classical recipes, and require more investigations. SiO_2 plasma etching generally uses fluor-based gases, like CHF_3, SF_6, C_4F_8, CF_4..., since fluor associates with Si to form SiF_4. The corresponding overall reactions are

$$3\,SiO_2 + 4\,CF_3 \longrightarrow 2\,CO + 2\,CO_2 + 3\,SiF_4 \text{ for fluorocarbon-gases, and}$$

$$SiO_2 + 2\,CHF_2 \longrightarrow 2\,CO + H_2 + SiF_4 \text{ for hydro-fluorocarbon-gases [38].}$$

Fluor-based molecules generally first dissociates and adsorbs on the SiO_2 surface before reacting, once their mechanical energy have weakened Si-O bonds. As an example, CHF_3 dissociates into CHF_2 + F, CHF_2^+ breaks Si-O bonds and dissociates by adsorbtion into C, H and 2F. F atoms finally react with silicon to form SF_4. Chlorine does react with silicon ($4\,Cl + Si \longrightarrow SiCl_4$), and could have been used to etch SiO_2, but etching rates are much lower than with aluminium, which wouldn't be suitable if one wants to etch SiO_2 without damaging the as-etched Al pores. Therefore, since it also provides a good selectivity regarding aluminium, fluor has been chosen. Our ICP reactor was equipped with many gas lines, including CHF_3 and SF_6 that we used combined to O_2 to make Bosch-like etchings (see p.113). Some investigations about etching SiO_2 through PAA and porous Al have been done in [37]. Basically, the electrodes powers have been varied so as they create a highly-directional plasma, that allows anisotropic etching without damaging the Al pores. A too low platen or coil power leads to a plasma in which the species are not directed enough, or to a plasma that is not dense enough to etch SiO_2, respectively. On the contrary, a too high coil power leads to such a high plasma density that even the PAA was etched. The as-found optimized conditions, reported in [37] are gathered in Table 4.2.

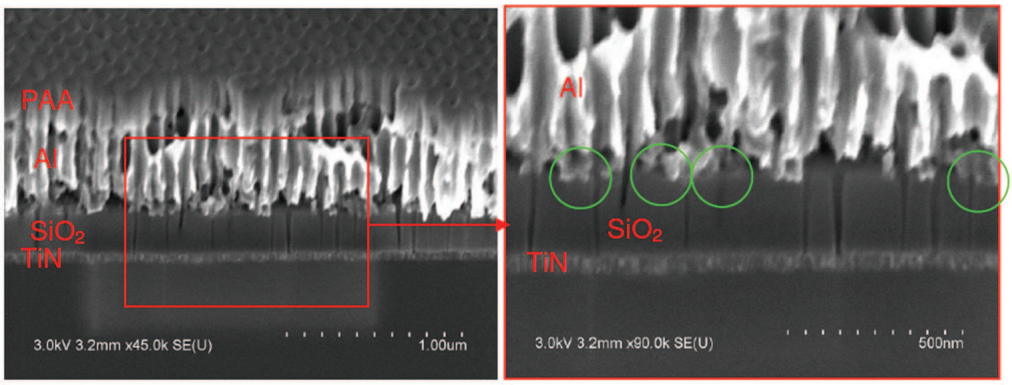


Figure 4.12: SEM cross-sections of a stack after an SiO_2 etching. Only a few pores go through the SiO_2 layer entirely. From [37].

CHF_3:SF_6:O_2 ratio	Pressure	Platen power	Coil power
100:5:2 sccm	4 mTorr	150 W	300 W

Table 4.2: Optimized conditions for SiO_2 etching through a PAA mask in our ICP reactor.

Despite these relevant optimizations, the pores couldn't be transferred in SiO_2 with a high efficiency, and some areas remain without any pore (Figure 4.12). The author supposed that a blocking Al layer, coming from a non-uniform deposition, could hinder the SiO_2 etching. Besides the potential non-uniformity of the Al layer, we supposed that a too thick PAA mask and porous Al layer could not be good for an efficient ion transfer until the SiO_2 layer, and that it could be useful to have dedicated reactors to perform Al etching on one hand and SiO_2 etching one the other. In order to get used to the SiO_2 etching process and to check by ourselves its feasibility, we chose to use a very simple structure, composed of a thin PAA mask realized directly on a 500 nm-thick SiO_2 layer. This configuration has the advantage to suppress the influence of the porous Al layer, and clearly shows whether the SiO_2 etching through a porous mask could be easily achieved. After optimizing the two steps of the anodization process, we found that a 2'30 first anodization followed by a $\approx$ 1'10 second anodization led to open pores on SiO_2, with the desired small thickness of 100 nm. In order to adjust the pore diameter to a higher value (the as-formed pores are $\approx$ 15-20 nm in diameter), we performed a 15 min pore widening (see chapter 1) in 0.3 M H_3PO_4, which led to an average pore diameter of 35 nm, which is supposed to be more appropriate for a first attempt of etching. Then, we performed a 30" ICP etching, in the conditions of Table 4.2. In spite of the dramatic current decrease observed at the end of the second anodization (as described in chapter 1), we found some alumina residues forming a thin barrier layer at the bottom of some pores (white arrows in Figure 4.13(a)). This may have hindered the SiO_2 etching, as shown in Figure 4.13(b): pores in SiO_2 are barely visible. Nevertheless, we can notice that the pores are now completely open on the SiO_2 layer (no remaining barrier layer), and we can even find some places where SiO_2 has clearly been etched. The white dotted

line in Figure 4.13(c) marks out the interface between Al and SiO_2, just to show how deep the SiO_2 has been etched, which is evaluated at 45 nm maximum.

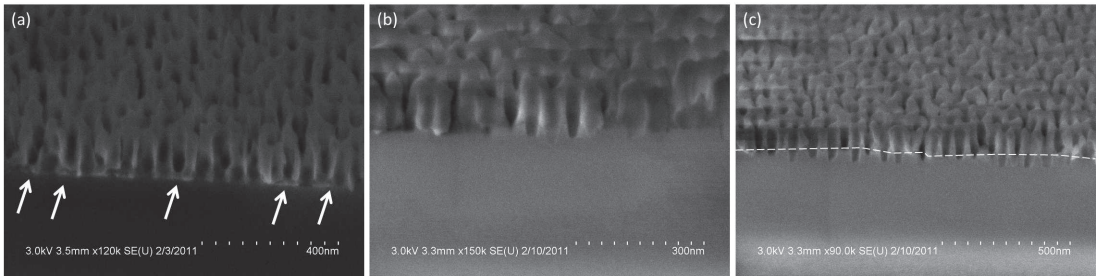


Figure 4.13: SEM cross-sections of 500 nm-thick SiO_2 layer with a PAA mask (a) before the SiO_2 etching, (b) and (c) after the 30 s SiO_2 etching. The white arrows in (a) indicate some places with remaining barrier layer, and the white dotted line in (c) marks the Al/SiO_2 interface.

It seems like these few seconds of etching have been useful to remove any obstacle (including the remaining barrier layer) for the etching, so we performed longer etchings, for 1 min, 2 min and 3 min, respectively. The results are visible in Figure 4.14

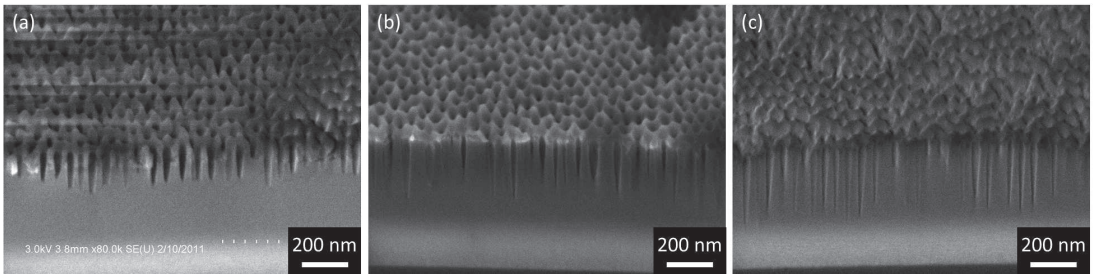


Figure 4.14: SEM cross-sections of 500 nm-thick SiO_2 layer etched through a PAA mask for (a) 1 min, (b) 2 min and (c) 3 min.

One can see that the SiO_2 layer is efficiently etched through the thin PAA mask, since long pores have been created. As expected and as already mentioned for the Al etching step, the longer the etching the deeper the SiO_2 pores and the thinner the PAA mask. The average pore diameter in the SiO_2 layer has been estimated at ≈ 20 nm, which is a bit smaller than the average pore diameter in PAA. The pores exhibit a conical shape, that is all the more visible for long etchings (Figure 4.14(c)). The maximum height of the pores in SiO_2 has been estimated to 109 nm, 217 nm, and 328 nm for 1 min, 2 min and 3 min etching, respectively, though a high disparity in height has been found. These height measurements, together with the corresponding PAA thicknesses and the sample shown in Figure 4.13 (30 s etching) are reported in the graph presented in Figure 4.15.

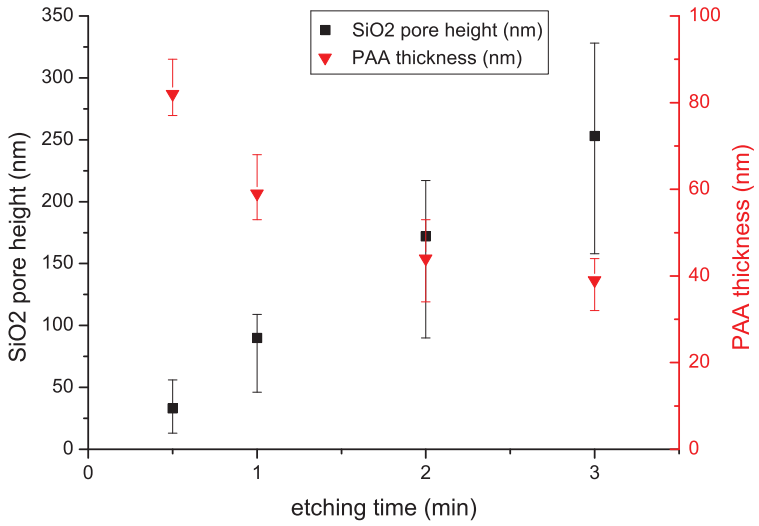
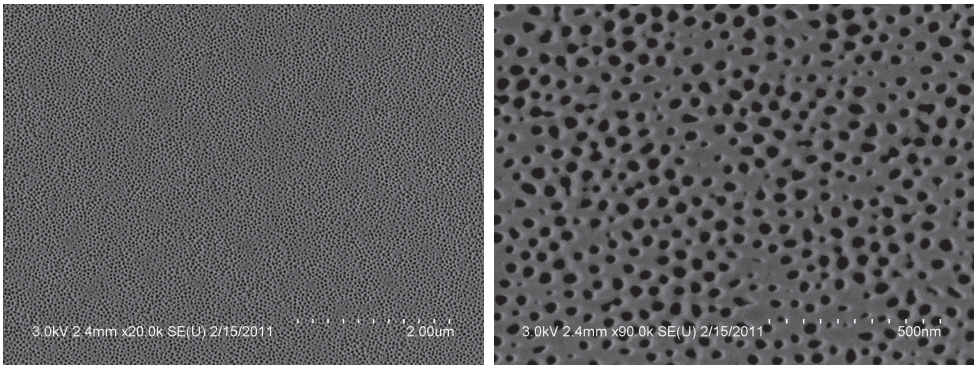


Figure 4.15: SiO_2 pore height (black squares) and PAA thickness (red triangles) as a function of etching duration.

It is interesting to notice that the etching time-dependence of the SiO_2 pore height is almost linear for the three first minutes of etching, with an etching rate of about 90 $nm.min^{-1}$. We haven't performed longer etching since we don't need to fabricate pores longer than the ones shown above. Indeed we planned to use 100 nm-thick SiO_2 layers in the following. As we could expect from the graph shown in Figure 4.15, a one-minute etching would be enough to get 100 nm-high SiO_2 pores, but we will see later that the thick PAA mask (necessary to bear two successive etchings) added to the porous Al layer will considerably decrease this etching rate.

SiO_2 pores are therefore easy to fabricate through a thin (100 nm) PAA mask. To better realize it, we completely removed the PAA mask by chemical etching (CrO_3 + H_3PO_4 as already described in the previous chapters). The SEM top views visible in Figure 4.16 correspond to the sample shown in Figure 4.14(c), that is after a 3 min etching. The density of the created pores in the SiO_2 layer is very high (estimated at 3.6 $10^{10}.cm^{-2}$), almost as high as the density in PAA since, as we can see, there is almost no place left without pore in the SiO_2 layer.

An alternative equipment has been used instead of the ICP reactor to achieve the SiO_2 etching, namely a simple RIE reactor, in order to compare the efficiency of each process. We went by an already-existing process, routinely used to realize deep trenches in silica through photo-resist masks. As the previous process, it involves three gases: here we used CF_4, C_4F_8 and O_2 (45, 15 and 10 sccm, respectively) under a pressure of 100 mTorr. The two first gases provide the fluor and the carbon for the etching and the polymer formation while O_2 is used as the polymer etchant (see p.113). The electrode power has been set to 200 W, and we performed two etchings for 8 min and 16 min.



(a) (b)

Figure 4.16: SEM top-view of the surface of a SiO_2 layer after a 3 min etching through a PAA mask and its subsequent removal. (a) is magnified 20 000 times and (b) is magnified 90 000 times.

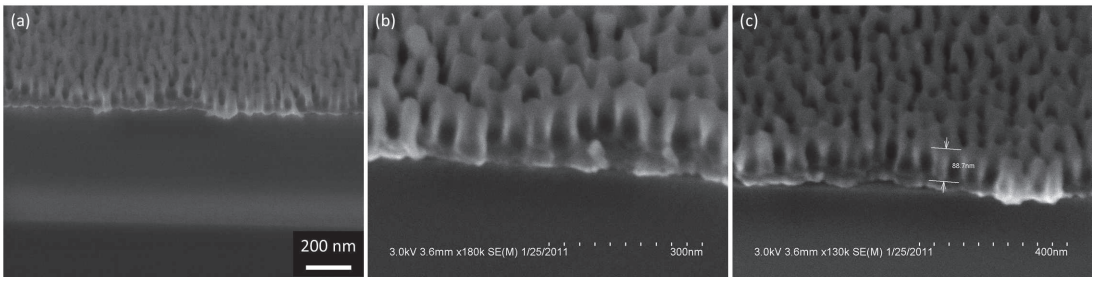


Figure 4.17: SEM cross-sections of an SiO_2 layer (a) before and (b), (c) after an RIE etching. (b): 8 min and (c): 16 min etching with CF_4:C_4F_8:O_2 = 45:15:10 sccm.

As shown in Figure 4.17(b) and (c), none of them gave satisfactory results. It is clearly visible that even a thin barrier layer remains under the PAA, proving that the etching had no impact on the structure. We therefore tried another existing recipe, replacing the C_4F_8 by SF_6 (5 sccm) and keeping the other parameters unchanged (see Table 4.3). After an 8 min etching, we could notice some very rare signs of etching at the bottom of the PAA pores, but no convincing evidence has been found (see Figure 4.18). Since the samples have been found to be similar before and after the etching (especially concerning the barrier layer), we assume that the barrier layer remains an obstacle for an efficient etching, that cannot be easily removed by RIE in these conditions. To support this assumption, we performed an very short ICP etching to remove this barrier layer (30 s, same conditions as in Table 4.1). Subsequently, we performed the same RIE etching as described right above, but for only 2 minutes. The first thing to be noticed is the efficiency of the first etching, performed in the ICP reactor, to remove the barrier layer (Figure 4.19(a)). Then we can see that much more pores are visible in the SiO_2 layer (white arrows in Figure 4.19(b)), and that they are deeper (as much as 104 nm, see Figure 4.19(a)), though the etching time has been four times shorter. Thus, the short

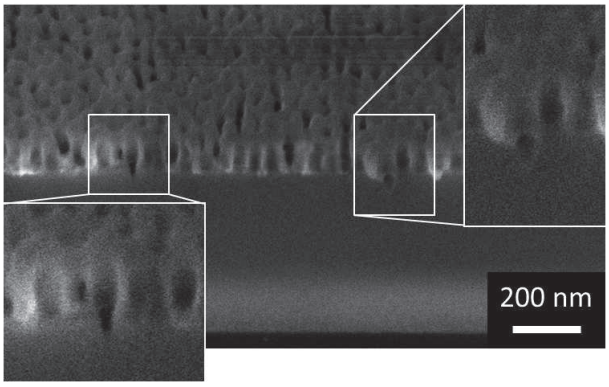


Figure 4.18: SEM cross-section of an SiO_2 layer under a PAA after an 8-min SiO_2 etching with CF_4:SF_6:O_2 = 45:5:10 sccm.

ICP etching performed before the SiO_2 etching is necessary if the latter is performed with RIE, in the particular conditions detailed. We couldn't investigate more deeply the simple RIE etching, but we assume that, like the ICP SiO_2 etching, optimized conditions could lead to a direct etching of the barrier layer and to the formation of pores. In particular, the high pressure (compared to the 3 or 4 mTorr used for ICP Al and SiO_2 etching) of 100 mTorr may be detrimental for an efficient etching, since a lot of collisions between ions must occur, which make them lose much energy before reaching the bottom of the pores. In the following, since it has been shown that pores could be easily fabricated in SiO_2, the optimized conditions detailed in Table 4.2 and the ICP RIE will be conserved.

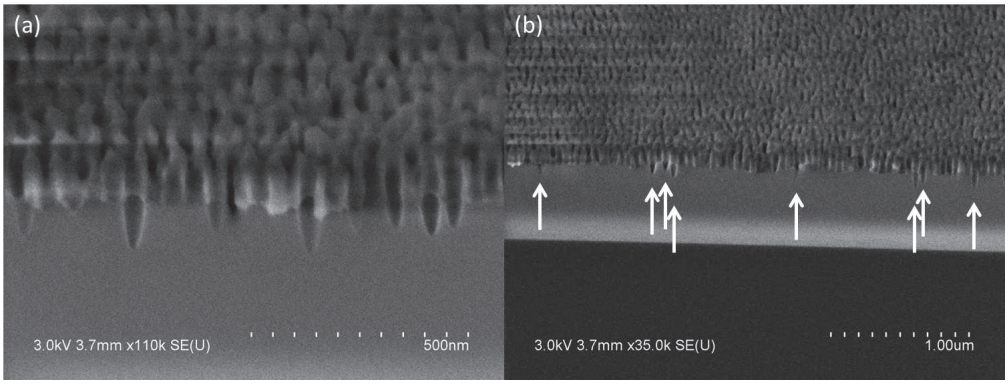


Figure 4.19: SEM cross-sections of an SiO_2 after a short barrier layer etching performed by ICP RIE, followed by a simple SiO_2 RIE.

The following table groups together all the RIE conditions of the experiments described above, with some comments about the results in each case.

Gases ratio	Pressure	Electrode power	Duration	Comments
CF_4:C_4F_8:O_2 = 45:15:10 sccm	100 mbar	200 W	8 min	no impact
CF_4:C_4F_8:O_2 = 45:15:10 sccm	100 mbar	200 W	16 min	no impact
CF_4:SF_6:O_2 = 45:5:10 sccm	100 mbar	200 W	8 min	A few holes are visible in the SiO_2
ICP RIE (Table 4.1) for 30 s + CF_4:SF_6:O_2 = 45:5:10 sccm	100 mbar	200 W	2 min	Barrier layer removed: etching more efficient.

Table 4.3: Summary table of the SiO_2 etchings performed in a simple RIE reactor.

SiO_2 etching through PAA and porous Al

We combined the good results that have been obtained concerning the Al etching and the SiO_2 etching in order to fabricate a complete porous stack. As explained above, one should anticipate the inevitable thinning of the PAA, therefore we deposited a 700 nm-thick Al layer on SiO_2/Si substrate (i.e. a Si substrate with a 100 nm-thick thermal SiO_2 layer). After several attempts, we found a good set of anodization durations, that is 8 minutes for the first anodization and 9 min for the second one. With a formation rate of ≈ 33 nm.min^{-1} (at 20 V, 5°C, in sulfuric acid), the second anodization led to a $\approx$ 300 nm-thick PAA layer, which leaves a 150-200 nm Al layer underneath. 300 nm have been found to be an appropriate thickness before Al and SiO_2 etchings if one expect a final 100 nm thickness after the etchings. These final thicknesses are believed to be a good compromise to make a sufficiently strong structure, without hindering the etchings because of too deep pores.

We used the conditions described in 4.2.2 to etch the Al layer, and found that 3 minutes were enough to create throughhole pores above the SiO_2 layer, which is rather consistent with the global trend of the Al pore height visible in Figure 4.8. Figure 4.20 shows a sample at this state of the process, where one can make out little holes in the SiO_2 layer, due to ion bombardment that continues even when the Al layer is completely etched. Contrary to the experiments shown in 4.2.2, the structure that lies on the SiO_2 layer is much more thick: 200 nm for the PAA mask (after the Al etching) and 200 nm for the porous Al layer, that is a 400 nm distance that should be covered by the etching species to the SiO_2 surface. As expected, this requires more time than with a very thin PAA mask, actually about twice the time predicted by the graph in Figure 4.15, since we performed a 2 minutes etching to see some pores cross through-and-through the SiO_2 (Figure 4.21(a)). This must be due to multiple collisions occurring between the etching species and the pore walls, which are potentially much more numerous inside long pores than short ones. Nevertheless, one can notice in Figure 4.21(b), which shows the SiO_2 surface after the PAA and Al removal, that all the pores have been transferred, at least partially.

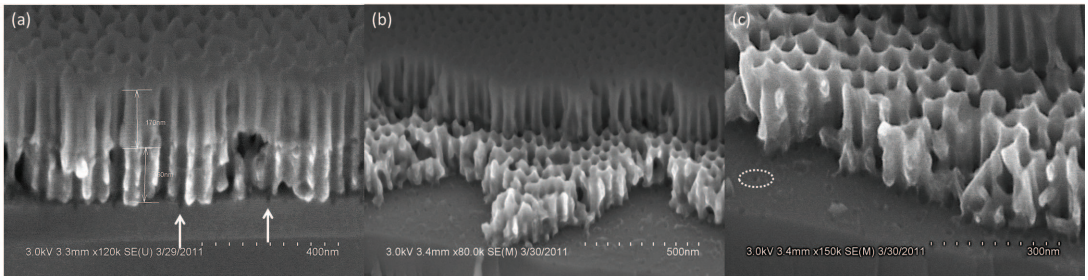
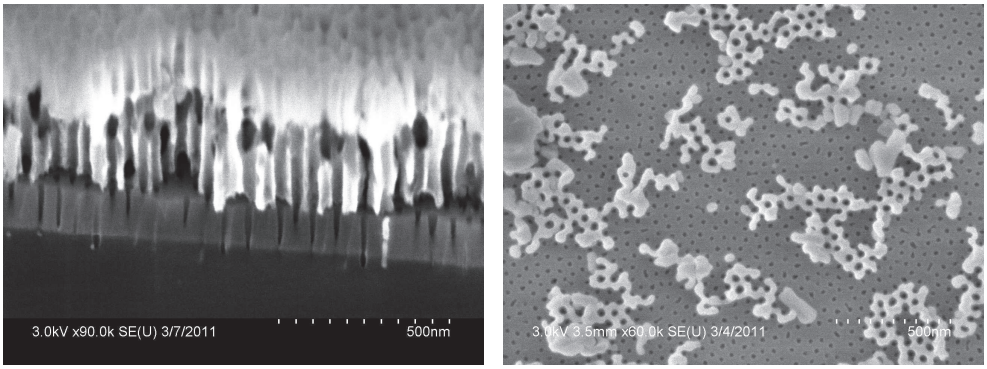


Figure 4.20: SEM cross-sections of a stack after a 3 minutes Al ICP etching. The white arrows and circle show some of the many little holes in the SiO_2 layer.



(a) (b)

Figure 4.21: (a) SEM cross-section of a porous stack after the 2 min SiO_2 etching and (b) same sample as after PAA and Al dissolution (some Al parts remain on the SiO_2 surface).

We therefore performed longer etchings, so as a maximum number of pores could open onto the underlying Si substrate. Three and four minutes etchings have been performed using the same conditions: the corresponding results are shown in Figure 4.22. Figure 4.22(a) is another picture of the sample shown in Figure 4.21(a) after the 2 minutes SiO_2 etching, and placed by pictures of samples etched for 3 and 4 minutes, respectively (Figure 4.22(b) and (c)). The difference between each other is remarkable: as expected, there are more open pores in SiO_2 for longer etchings. The pores are also wider (up to 18 nm in Figure 4.22(c)), and we notice that the etching becomes much more isotropic when the pores reach the Si substrate, as the ball-like shape indicates. This can be explained by the change in the etched material (SiO_2 –> Si), that would require a different gas combination to properly protect the side walls during the etching. A too long etching as shown in Figure 4.22(c) would not be very problematic, the most important being to get as many open pores as possible. For these very specific conditions, considered as optimized conditions, we nevertheless chose to perform 3'30 etchings for the following, in order to limit the thinning of the PAA. Anyway, a very high density of straight through-hole pores have been successfully realized in the SiO_2 layer, which hadn't been achieved so far in such a reproducible way, and with so thin pores (thanks to a low voltage during the anodization). Besides, these good results have been obtained on areas as large as 2 inches wafers, with a good uniformity thanks to a proper application of the vacuum grease on the back side of the wafer.

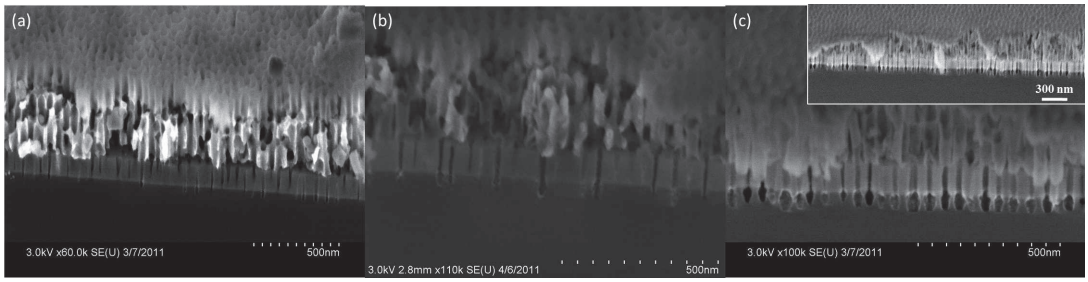


Figure 4.22: SEM cross-sections of a stack after (a) 2 min, (b) 3 min and (c) 4 min SiO_2 etching.

The as-obtained porous structure (a last example is shown in Figure 4.23 is therefore ready to act as the porous template that is supposed to receive metallic catalysts first, and then the nanostructures that will be grown to form the channel of many individual FETs. This will be studied in the next section (4.3), but beforehand we would like to talk about an alternative method which we have started to worked on, in order to fabricate a similar porous stack.

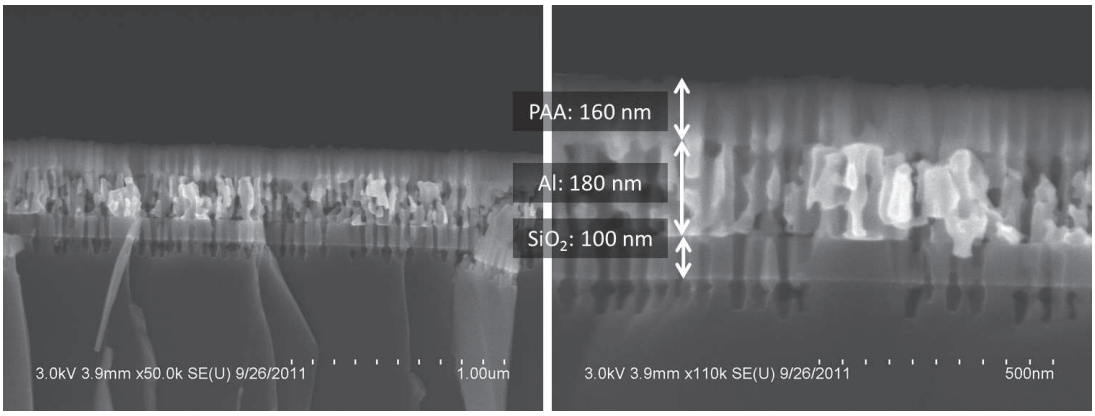


Figure 4.23: SEM cross-section of a stack realized on a 2 inches wafer. PAA, Al and SiO_2 layers are 160, 180 and 100 nm-thick, respectively.

We will now talk about the second part of the fabrication process of the vertical FET, the growth of the 1D channel. The first part deals with the catalyst electrodeposition, takes up the results obtained in chapter 2, and introduces some problems inherent to the porous stack. Then we will talk about the 1D nanostructures, in a part dedicated to CNT growth and in another part dedicated to SiNWs. The last section deals with the work we have done about electrical connection, with a view to connecting the tips of the nanowires or nanotubes on the top of the porous stack.

4.3 1D nanostructure growth inside the porous stack

4.3.1 Catalyst electrodeposition in the porous stack

Since our best results concerning homogeneity and reproducibility have been obtained with Ni, we first chose this metal for the electrodeposition inside the porous stack. A sample similar to the one we used has already been presented in Figure 4.21(a). The optimized conditions found in chapter 2 for Ni, that is one hundred -5.5 V pulses of 5 ms each, separated by a 90 ms resting time have been applied to this sample. Some cross-sections pictures are visible in Figure 4.24.

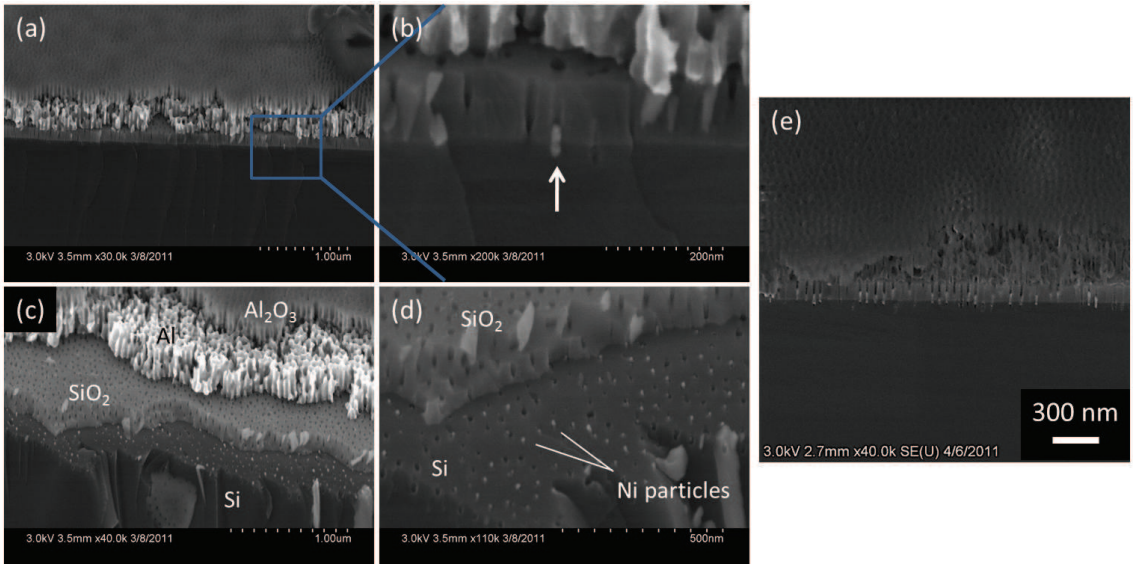


Figure 4.24: SEM cross-sections of a porous stack after Ni electrodeposition under optimized conditions.

Though only a few Ni particles are visible at the bottom of the pores in Figure 4.24(a) and (b), we realized that many particles have been deposited when we found an interesting point of view that revealed the silicon surface (Figure 4.24(c) and (d)). These pictures allow to visualize both edge and top surface of every single porous layer composing our stack. Figure 4.24(b), which is a magnification of (a), shows a Ni particle at the bottom of a pore. Nevertheless, the section plane can sometimes be non-perpendicular to the substrate, and therefore the SiO_2 pores don't show their entire length, nor a probable Ni particle, as in Figure 4.24(b). The tilted section plane (non-controllable) is thus a good opportunity to realize how many particles have been deposited. They appear in bright, little spots on the Si surface in Figure 4.24(d). When, like in most cases, the section plane of the sample is well perpendicular to the substrate, we can see that most pores contain a Ni particle (Figure 4.24(e)). This is the kind of result we were expecting for a subsequent CNT growth, that is as many Ni particles as possible inside a well ordered porous stack. We will therefore use this sample in the section devoted to CNT growth in the following.

Contrary to simple electrodeposition in PAA, the silver paste used to attach a sample to the sample holder has to be applied with particular precaution, so as it doesn't contact the edges of the sample. Indeed, it could create a short-circuit by contacting both the Al layer by the edge and the Si substrate at the back, making the Al layer the working electrode instead of the substrate. This, as expected, led to a localized reduction of the cations in the Al pores, which is absolutely undesired (see pictures in Figure 4.25).

With a view to growing SiNWs, we also wanted to deposit gold at the bottom of the stack pores. Like Ni, we also went by the results we got from chapter 2. However, we have never been able to get a proper deposition in a reproducible way. Due to the

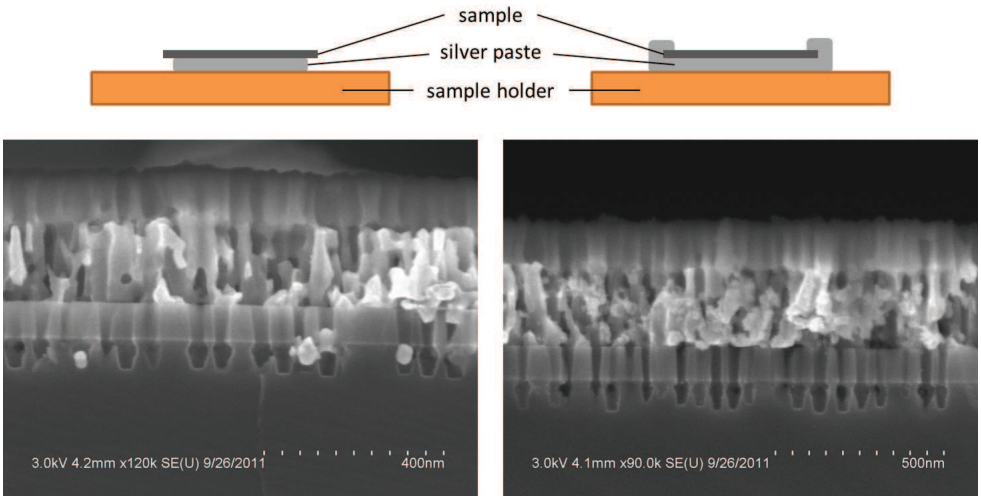


Figure 4.25: Illustration of the importance of the silver paste contact during the electrodeposition. On the left, a proper contact leads to a deposition at the bottom of the pores (though very limited here), whereas a contact on the edges (on the right) reduces cations in the Al pores.

high complexity of our porous structure, and despite our efforts to make it as uniform as possible, some places may have different properties than others and this could results in a non-homogeneous deposition. Besides, electrically speaking, the stack structure is not as simple as a PAA layer on a Si substrate: since it is composed of conductive and insulating layers, complex capacitive effects must occur, which modifies a lot the electrical behaviour of the electrolyte species. We couldn't identify why such problems has never happened with Ni deposition.

Au electrodeposition has been very difficult to control, but some optimizations have been done anyway. Concerning the number of sweeps, it appeared that 50 was a good compromise since, like in chapter 2, a higher number led too a spill all over the surface. However, in some cases, even a low number of sweeps led to a large amount of gold on the stack surface, which was not due to overspilling, as shown in Figure 4.26(c). However, we can see that Au has definitely been deposited at the bottom of the pores, and with a perfectly appropriate amount, though a rather low pore filling. This proves that the set of deposition conditions can be used, but that a problem emerges for unknown reasons with some stacks. Indeed, we managed to fabricate a similar sample with small Au particles at the bottom of the pores with no parasitic deposition on the PAA surface. Since the preparation of the porous stack and the electrodeposition conditions have been assumed to be strictly the same, we couldn't figure out how we obtained these good results, that are shown in Figure 4.27. We therefore took the opportunity to attempt some SiNW growths with the samples exhibiting such a good deposition.

Copper electrodeposition has also been very difficult to control, but has been performed to see how it would take place. Like in simple PAA, a bad homogeneity was the main problem. Cu particles are deposited at the bottom of the pores, but the areas where

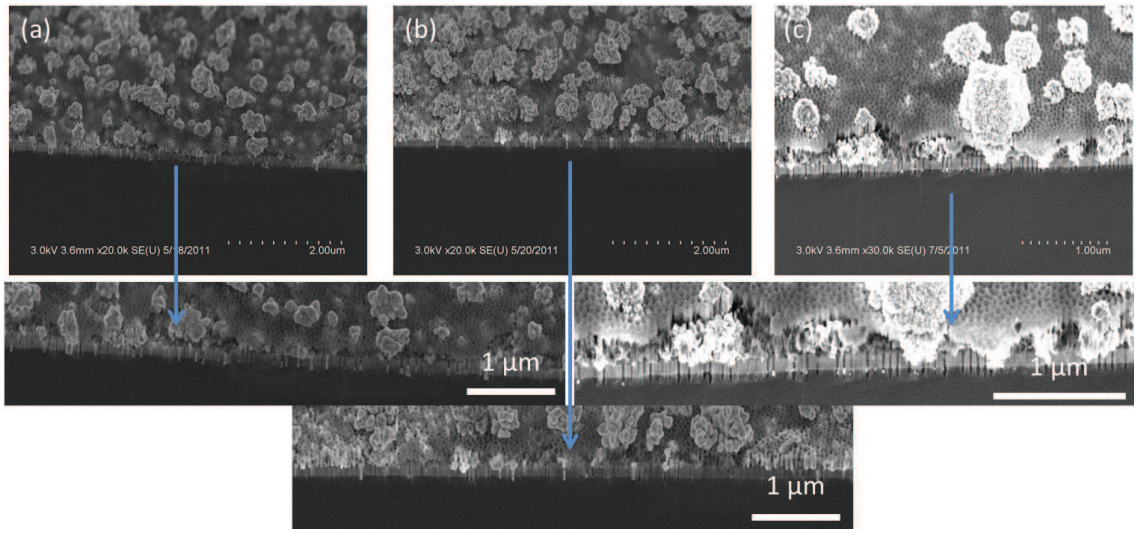
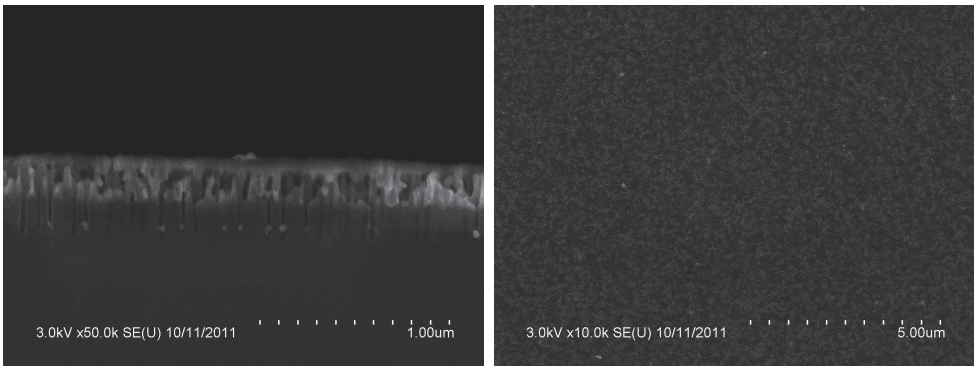


Figure 4.26: SEM cross-sections of a porous stack after Au electrodeposition under optimized conditions of chapter 2. (a) 1000 sweeps, (b) 50 sweeps and (c) 20 sweeps.



(a) (b)

Figure 4.27: (a) SEM cross-section and (b) top view of a porous stack after Au electrodeposition under optimized conditions of chapter 2. Au is properly deposited, with no deposition on the surface of the sample.

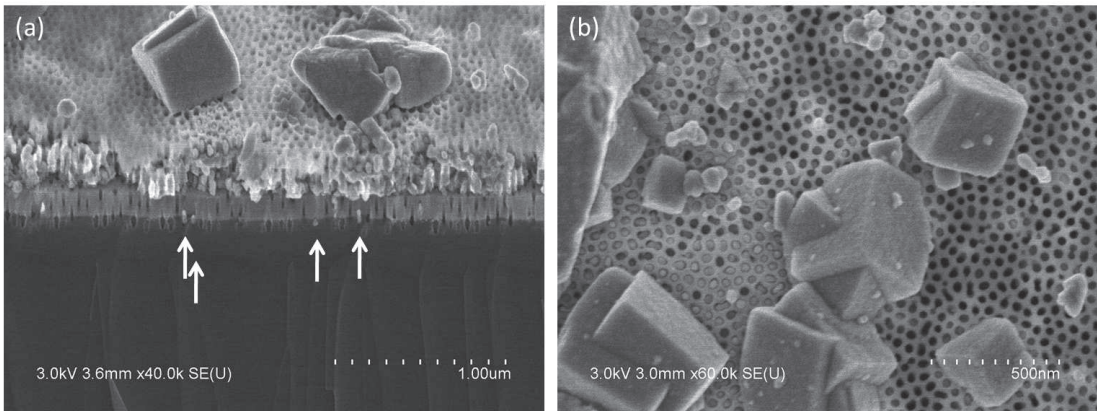


Figure 4.28: (a) SEM cross-section and (b) top view of a porous stack after Cu electrodeposition: 1000 sweeps of 5 ms, at -8.5 V. The white arrows in (a) indicates the few Cu particles visible at the bottom of the pores.

a high deposition rate takes place exhibit huge particles (compared to pore size) due to mater spill over the pores. A very typical example is shown in Figure 4.28, where we can clearly see both on (a) and (b) some long Cu wires forming big cubic structure once reaching the top of the pores. The pores filled with copper appear in bright in Figure 4.28(b) and the empty ones (or less filled) appear in black.

The substrates we have used so far have a resistivity between 1 and 10 Ω.cm, which forced us to adapt the voltage to values as high as -8.5 V in the case of Cu, so as the successive voltage drops don't hinder the cation reduction. Besides, the 100 nm-thick thermal SiO_2 (realized by the substrate manufacturer itself) has been realized on both sides of the wafers for obvious cost reasons. Therefore, an additional 100 nm-thick resistive layer is present between the Si substrate and the metallic back contact. In order to study whether a lower voltage could be beneficial to electrodeposition, we tried similar experiments on low resistivity substrates ($\rho < 0.005$ Ω.cm, obtained by a high boron doping: $N_A > 2.10^{19}.cm^{-3}$), from which the back SiO_2 layer had been removed by wet etching using hydrofluoric acid (HF). Figure 4.29 shows the three I(t) curves corresponding to a few pulses extracted from a typical Au electrodeposition, for the three different cases detailed on the graph. As expected, the current is higher when the back SiO_2 is etched away with HF, and even higher for low resistivity substrates without this SiO_2 layer, which indicated a more efficient deposition. Indeed, the pictures in Figure 4.30 show that the Au particles are very small, ball-like (a), as shown in Figure 4.27(a) when the back SiO_2 layer is not removed and with a 1-10 Ω.cm substrate. No big difference has been noticed when the SiO_2 layer has been removed, except a higher proportion of long particles, reaching the Al layer as pointed out by the white arrow in Figure 4.30(b). Low resistivity substrates have led to a higher deposition rate, due to the higher current as shown in Figure 4.29. Many Au particles reach the PAA layer and even higher, which leads to a lot of big Au particles on the top surface, as illustrated by the inset of Figure 4.30(c).

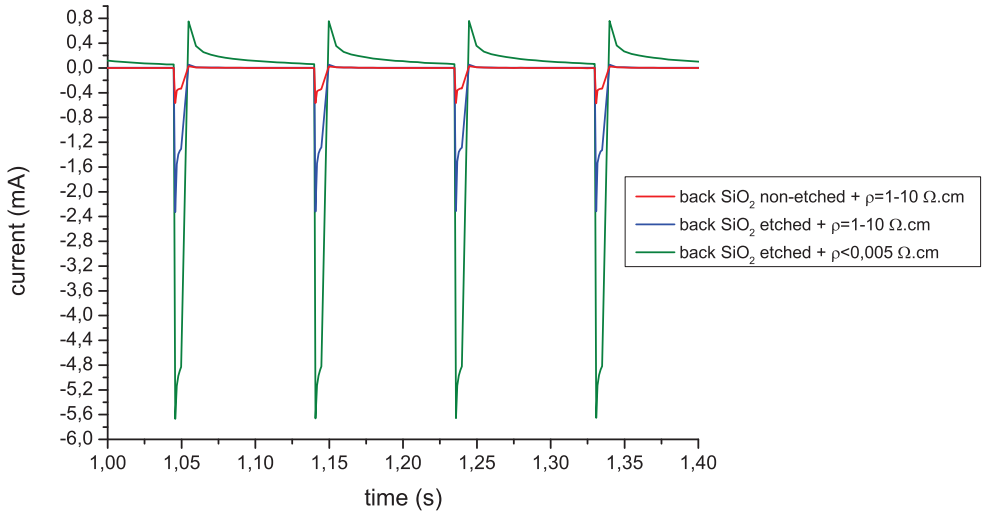


Figure 4.29: Partial I(t) curves from a typical Au electrodeposition on (red curve) 1-10 Ω.cm substrate with the back SiO_2, (blue curve) 1-10 Ω.cm substrate without the back SiO_2 and (green curve) $<$ 0.005 Ω.cm substrate without the back SiO_2.

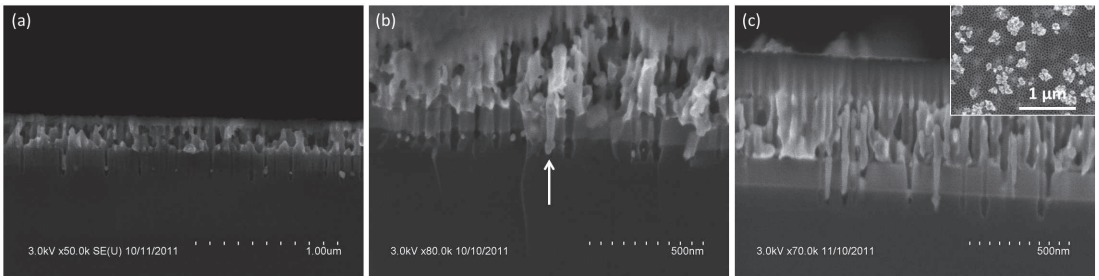


Figure 4.30: SEM cross-sections of a porous stack after a typical Au electrodeposition (50 sweeps at -5.5V) on a (a) 1-10 Ω.cm substrate with the back SiO_2, (b) 1-10 Ω.cm substrate without the back SiO_2 and (c) $<$ 0.005 Ω.cm substrate without the back SiO_2.

A different substrate resistivity requires an adjustment of both the applied voltage and the number of sweeps, so a series of experiments has been done in order to know if a proper deposition could be done with low resistivity substrates. We tried several voltages, from -3.5 V to -0.5 V. As shown in Figure 4.31, the current values are of course lower for lower voltages, and this have successfully led to smaller Au particles at the bottom of the pores. One can also notice the progressive disappearance of the Au particles from the surface on the top view pictures as the voltage decreases.

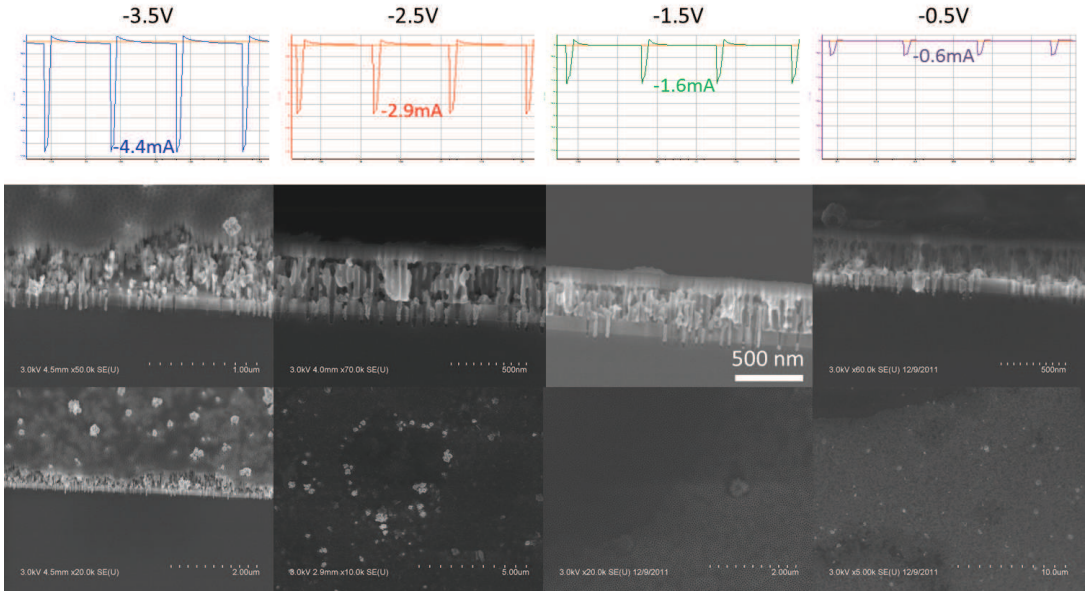


Figure 4.31: Four I(t) curve extracts, from Au electrodeposition at -3.5 V, -2.5 V, -1.5 V and -0.5 V. 50 sweeps have been applied in each case. Corresponding SEM pictures are visible under each I(t) curve.

Reducing the number of sweeps hasn't led to any improvement since we couldn't find any Au particle in the pores when applied 20 or 30 sweeps.

We also tried to find new operating conditions for Ni electrodeposition, and found after several experiments that a voltage of -1.5 V, with 100 sweeps led to pretty satisfactory results, that is a clean surface, a good homogeneity in length and a good filling ($>$ 75 %). The corresponding sample is shown in Figure 4.32 and shows that a small amount of Ni has been deposited in almost each pore. An interesting but expected thing is that the current we measured under these conditions is similar to the current we measured under optimized conditions with 1-10 Ω.cm substrates, that is between -15 and -20 mA. This would mean that, beyond the duration of the pulses and resting time, the value of the current is a capital parameter to control for a proper deposition. It is therefore hard to say whether electrodeposition is better with low resistivity substrates and lower voltages than with "high" resistivity and substrates and the conditions used in chapter 2. Indeed, the conditions that were found to lead to the most proper deposition correspond to a similar current value (around -1 mA for Au and -20 mA for Ni), no matter what the

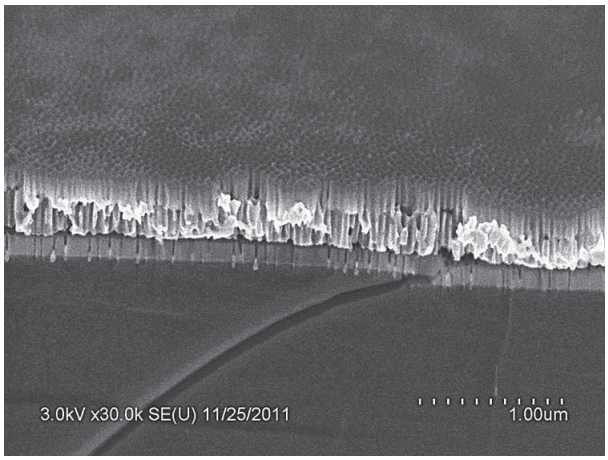


Figure 4.32: Cross-section of a sample after a Ni electrodeposition (-1.5 V, 100 sweeps) on low resistivity substrate.

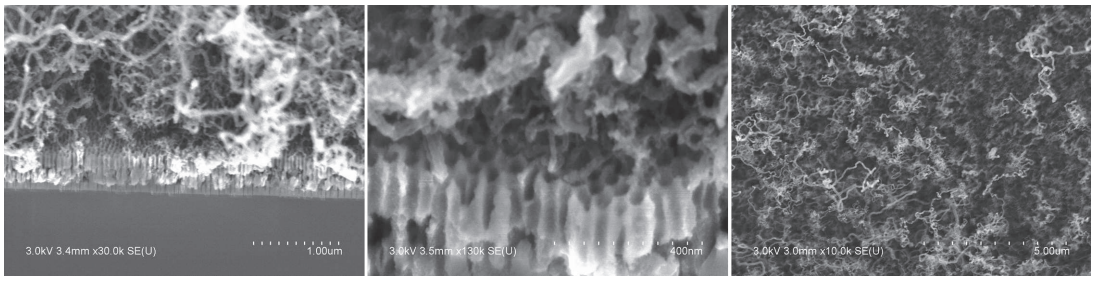
conditions were. Cu electrodeposition hasn't been studied enough with low resistivity substrate to present any result worthy of note here.

We have shown that we successfully deposited Au and Ni at the bottom of our porous stack, despite some irregularities with Au and and certain lack of reproducibility. These results are nevertheless very promising for the following of the FET fabrication, that is the 1D nanostucture growth in the porous stack. The two next sections, which are based on the use of the properly-filled samples, deal with CNT and SiNW CVD growth, respectively.

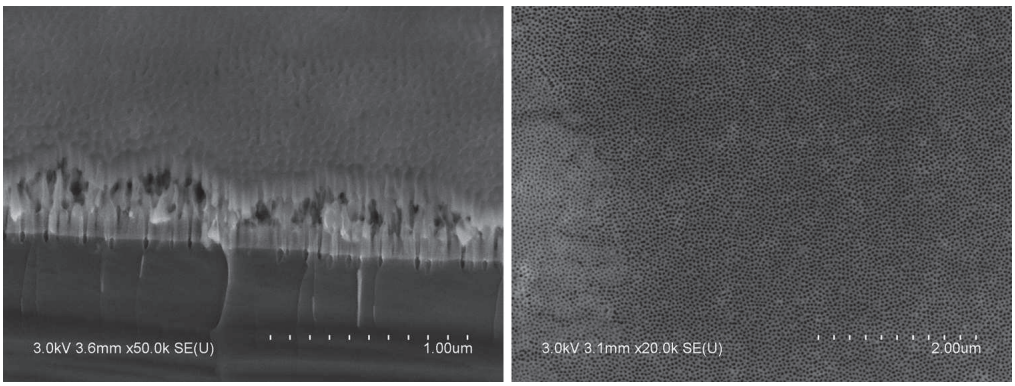
4.3.2 CNT growth

As in chapter 3, we used Ni as catalyst to grow CNTs by HWCVD technique and took up the samples shown in the very last section. We haven't really planned to use CNTs as the FET channel, since most of them must have a metallic behaviour (because they are multi-walled). Nevertheless, it is interesting to investigate their growth in the porous stack, were it only to bring another proof of concept.

The growth conditions differ from the optimized conditions detailed in chapter 3, and have been chosen so as to increase the growth rate. To do so, a higher pressure and temperature have been used ; the conditions are grouped in Table 4.4. Ni has been deposited at -5.5 V, since a 1-10 Ω.cm substrate has been used in this case. After a first 15-minute growth under the conditions of Table 4.4, we can see a lot of CNTs covering the surface of the stack (Figure 4.33(a)). Probably due to a too long growth, we almost can't see anything below this pile of CNTs. We nevertheless brought evidence that they grew from the Ni catalysts, since we couldn't see any CNT on a sample that had no Ni particles and which had been inserted in the reactor in the same time as a reference (Figure 4.33(b)).



(a)



(b)

Figure 4.33: (a) SEM pictures of a porous stack after a 15-minute CNT growth performed in the conditions described in Table 4.4. (b) Same sample as in (a) but without catalyst particle: no CNT is visible after the growth.

Reactor temperature	**Pressure**	**H_2:CH_4 ratio**	**H_2 hot wire power**	**CH_4 hot wire power**
600°C	95 mbar	50:50 sccm	180 W	180 W

Table 4.4: CVD growth conditions for CNT growth in the porous stack in our HW-CVD reactor.

The growth duration has been progressively decreased so as we are still able to see the surface of the PAA after the growth and thus observe a protruding CNT. 3'30, 2'20 and 1'00 growths have been performed for this purpose, and the corresponding SEM pictures are shown in Figure 4.34. We can clearly see the CNT density decrease as the growth duration decreases, which allows us to see the surface of the PAA. 3'30 and 2'20 growth have both led to a satisfactory result (CNTs have grown) but it appeared that one single minute was not enough to observe any CNT going out from the porous stack. It is therefore assumed that the duration of the incubation period (saturation of the catalyst,

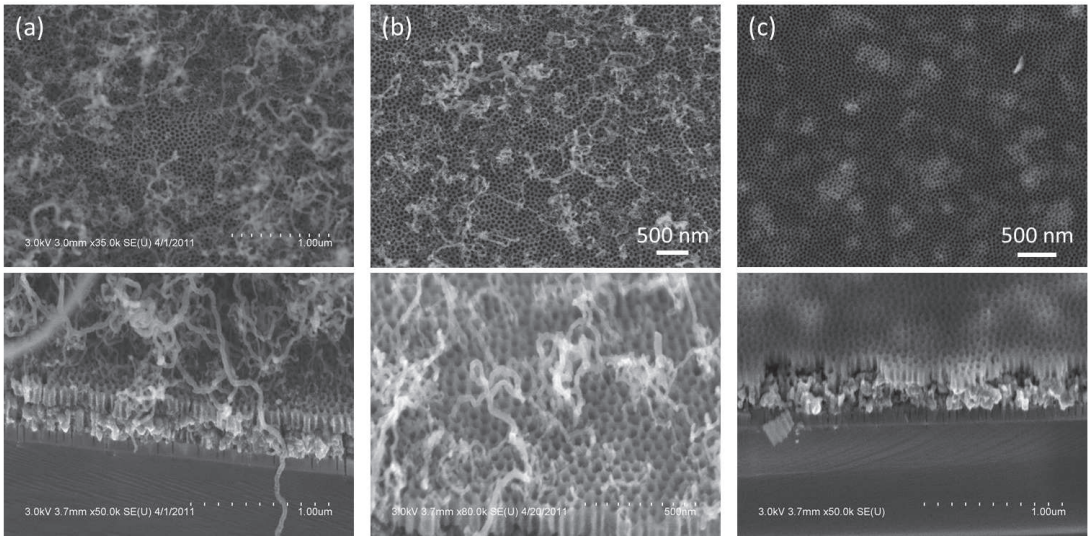


Figure 4.34: SEM top views (top) and cross-sections (bottom) or porous stacks after a (a) 3'30, (b) 2'20 and (c) 1'00 CNT growth.

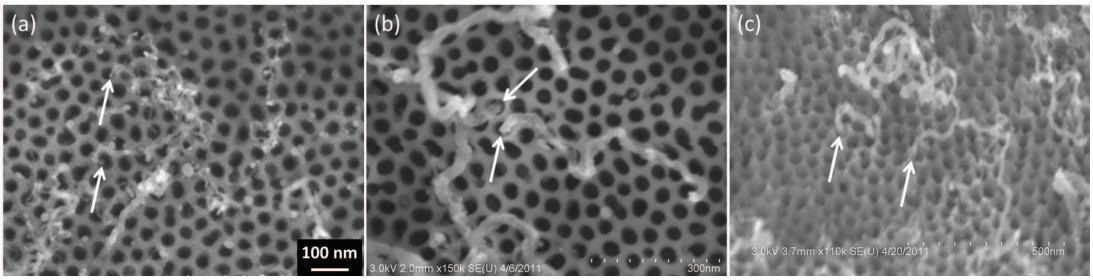


Figure 4.35: SEM pictures showing protruding CNTs after CNT growths. (a) and (b) have been taken after the 3'30 growth, and (c) after the 2'20 growth.

see chapter 3) and the growth along the pore is at least one minute. Some pictures of protruding CNTs, taken from the samples shown in Figure 4.34, are given in Figure 4.35. Pictures from Figure 4.33(b) to 4.35 confirm that the CNTs come from inside the stack, thanks to a catalytic growth. No further study has been done about CNT growth, since our only goal was to prove they could be grown in our stack.

4.3.3 SiNW growth

We only focus on Au-catalysed SiNW growth in this part. Of course it is essential to use a stack in which a proper electrodeposition has been done, since parasitic gold deposited on the surface would inevitably lead to a SiNW growth from the top of the porous structure, which is completely useless. Basing on the results detailed in chapter 3, we performed several growths modifying the key parameters that are temperature and gas ratio. The different growths, for a period of 30 min each, are summed up in Table 4.5. The total

pressure was set to 5 mbar during the growths and the filament power to 175 W.

		Growth temperature		
		450°C	470°C	500°C
SiH_4:H_2 (sccm)	5:95		×	
	10:100		×	×
	15:85		×	×
	20:100	×	×	

Table 4.5: Summary table of the SiNW growths carried on in the porous stack.

Four gas ratios have been tried at a temperature of 470°C, namely 5:95, 10:100, 15:85 and 20:100 sccm.

Even if we could see some Au particles coming out from the porous stack, no SiNW has been seen when SiH_4:H_2 equalled 5:95 sccm (Figure 4.36-top), which proves the difficulty to catalyse SiNW growth under these conditions. The very low number of SiNWs visible on the reference (5-nm Au particles on Si substrate) confirms that such a low gas ratio is not appropriate (Figure 4.36(a)-bottom).

By increasing the gas ratio to 10:100, we managed to grow some SiNWs out of the porous structure, as shown in Figure 4.36(b). No parasitic Au had been seen on the surface before the growth, so the SiNWs must have grown from the very bottom of the stack. Moreover, all the SiNWs have approximately the same diameter, that is a little more than the pore diameter itself ($\approx$ 30 nm). This confirms the intra-pore growth on one hand, but also indicates that a thin oxide layer must have formed on the side of the wires once out of the stack, on the other.

Another gas ratio, SiH_4:H_2 = 15:85 sccm, has been tried. Some SiNWs may come directly from the top of the surface, since we noticed a few Au particles deposited on the surface before the growth. Nevertheless, we could find some nanowires protruding from the inside of the stack, with a Au particle at their tip, indicating that these conditions are suitable for SiNW growth in the porous stack (top picture and inset in Figure 4.36(c)). This is confirmed by the rapid growth on the reference sample, shown in Figure 4.36(c)-bottom. One should remind that the low density of SiNWs is as much due to a low number of catalyst as to incongruous growth conditions. Furthermore, we noticed that some Au particles have remained at the bottom of the pores after the growth, which reduces again the number of SiNWs.

Finally, we performed a growth with 20 sccm of SiH_4, diluted in 100 sccm of H_2, which is close to the previous 15:85 ratio (0.20 and 0.18, respectively). The sample we used is the one we presented in Figure 4.27(a), as an example of a proper Au electrodeposition. The high flow rate dramatically increased the SiNW growth rate, as proved by the large number of SiNWs visible in Figure 4.36(d). The NW diameter is rather homogeneous, at least as much as the pore diameter dispersion. Despite the high flow rate of SiH_4, we can't see much amorphous silicon, which proves the efficiency of the hot wire in removing it. We can draw from these results that a relatively high silane ratio is required to grow SiNWs in the porous stack.

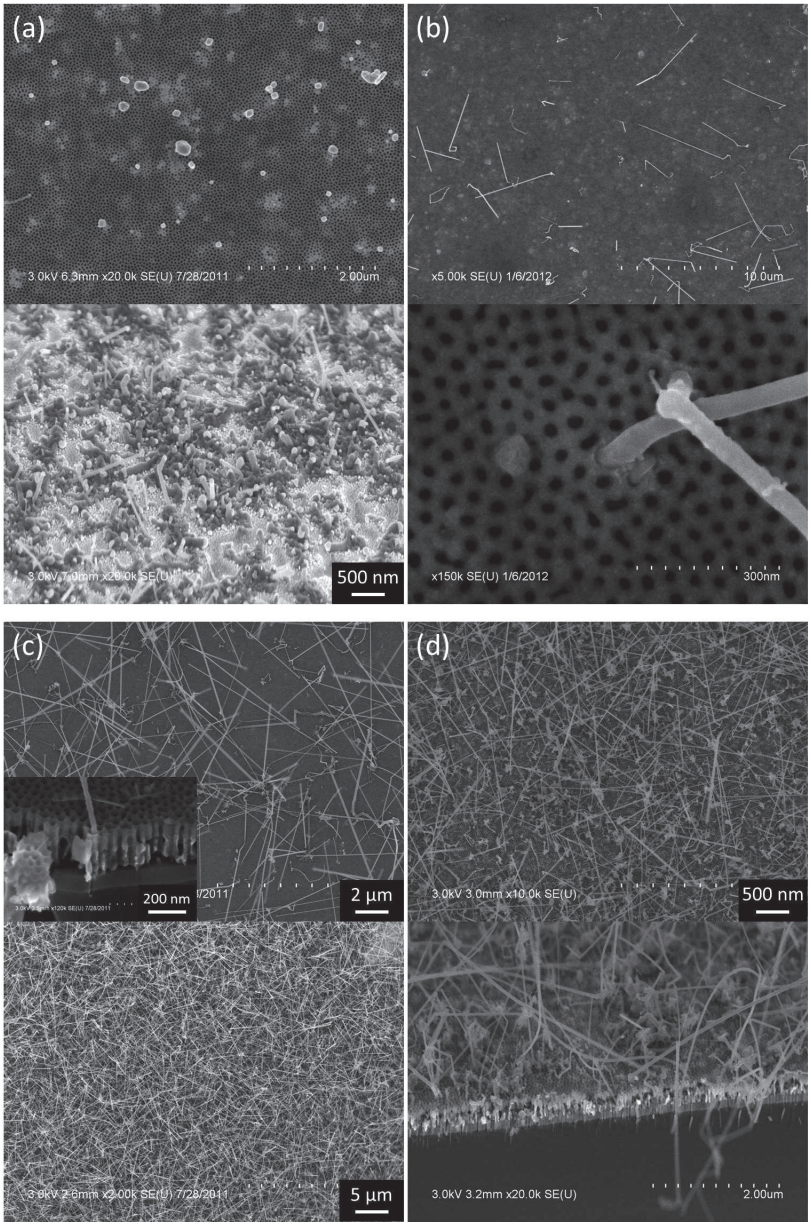


Figure 4.36: SEM pictures of the porous stack after a SiNW growth at 470°C for SiH_4:H_2 = (a) 5:95, (b) 10:100, (c) 15:85 and (d) 20:100 sccm. The bottom pictures in (a) and (c) correspond to reference samples (Au nano-particles on Si substrate)

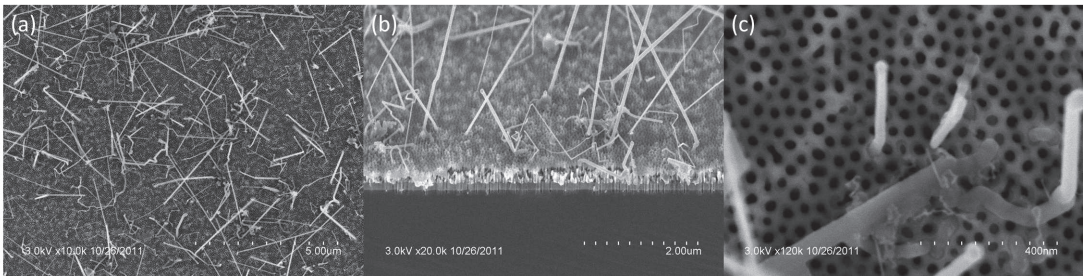


Figure 4.37: SEM pictures of the porous stack after a SiNW growth at 450°C for SiH_4:H_2 = 20:100 sccm.

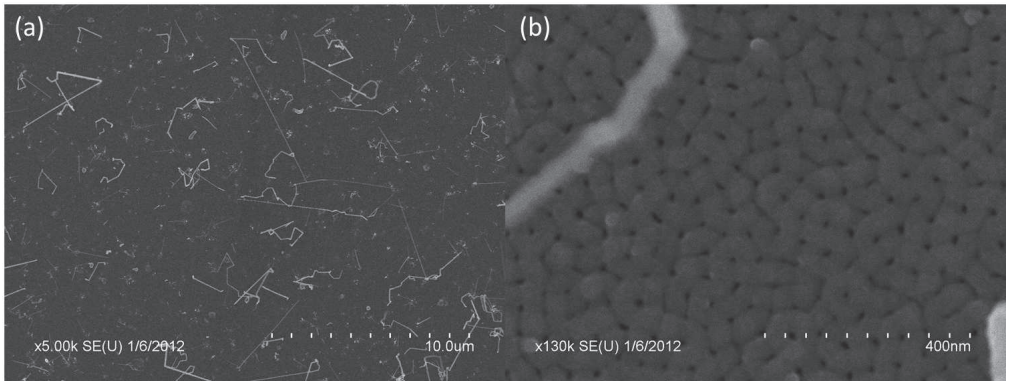


Figure 4.38: SEM pictures of the porous stack after a SiNW growth at 500°C for SiH_4:H_2 = 10:100 sccm.

The same conditions have been tried using a lower temperature, that is 450°C. The gas ratio we used was SiH_4:H_2 = 20:100 sccm, so this sample can be compared with the one shown in Figure 4.36(d). The temperature decrease seems to lead to a lower growth rate, as suggested by the pictures shown in Figure 4.37. Indeed, the surface of the stack is less covered with the SiNWs, and the cross-section in (b) exhibits shorter SiNWs than on the sample after a growth at 470°C (Figure 4.36(d)). Figure 4.37(c) gives an example of two SiNWs going out of the porous stack, with a Au particles at their tip.

Finally, we tried to perform some growths at higher temperatures. As expected, this leads to a higher formation of amorphous silicon on the surface of the stack and on the pore walls, which reduces the pore diameter. The example of a porous stack after a 30-min growth at 500°C is shown in Figure 4.38. The lower number of visible SiNWs could be explained by the smaller surface exchange between the Au particles and the silane, due to the progressive pore clogging.

This short study has allowed to identify some parameters compatible with the SiNW growth, that are different from those found in chapter 3. Indeed, we used a lower temperature (450-470°C) with a higher pressure and gas ratio. Basically, as far as we studied, the growth behaves according to what we found in chapter 3 regarding the temperature and the gas ratio, that is a higher growth rate with increasing temperature and gas ratio,

limited by the formation of amorphous silicon. For too low gas ratio, the SiNW growth couldn't be observed at 470°C (Figure 4.36(a)), whereas it has been achieved at 490°C in chapter 3.

Anyway, the objective set in the beginning of this chapter has been fulfilled: indeed, we successfully grew both CNTs and SiNWs in a vertical porous stack, that includes a conductive layer (Al) between two insulating layers (SiO_2 and alumina, respectively). However, the Al layer, embedded under the PAA, is inaccessible in this configuration and thus prevents any gate-controlled measurement. At the same time, one has to find a better way to contact the protruding SiNWs with the metallic probes than just putting them directly on the sample. The next section deals with both these problems: we developed a method to pattern the stack in order to leave some pure Al pads in the middle of the pores, and tried a simple and fast method to print metallic contact thanks to a silver-based ink.

4.3.4 The electrode printing and the patterned porous stack

First of all we focus on the contact printing. We will talk about the patterning of our porous stack in the second part of this section.

Electrode printing

An special ink-jet printer, available in our lab, has been used to realize electrical contacts by printing micrometre-sized conductive droplets on glass. The power of this device is that one can design any shape of electrode thanks to the computer assisted control, and that one can chose the distance between the droplets, as well as the droplet size the nozzle delivers. These parameters are controlled by the dispense frequency of the droplets and by the voltage applied on the nozzle, respectively. The higher the voltage the bigger the droplet. The thickness of the printed electrode can be adjusted by increasing the number of ink layers deposited with the nozzle.

We studied inter-droplet distances from 5 to 20 µm, and voltages from 12 to 18 V, as indicated in Table 4.6. These voltages correspond to droplet volumes around 10 pL, +/- 2 pL. The number of layers has been kept to two for every experiment.

Voltage	**Inter-droplet distance**
18 V	10 µm
16 V	20 µm
	15 µm
	10 µm
	5 µm
12 V	10 µm

Table 4.6: Summary table of the printing conditions we used to realize electrodes on a porous stack.

The ink we used is provided by *InkTec*, and is a none-particle-based ink, made of soluble silver complex. The use of this ink is based on sintering, which is reached by drying, typically for 30 min at $\approx$ 150°C after the printing. We printed rectangular electrodes (1 mm wide and 3 mm long) on a porous stack set on a platen heated to 60°C, and cleaved the samples through the as-printed electrodes to observe the cross-sections with the SEM. Some differences can be noticed depending on the printing conditions. As an example, one can notice the difference in morphology and thickness between the samples shown in Figure 4.39.

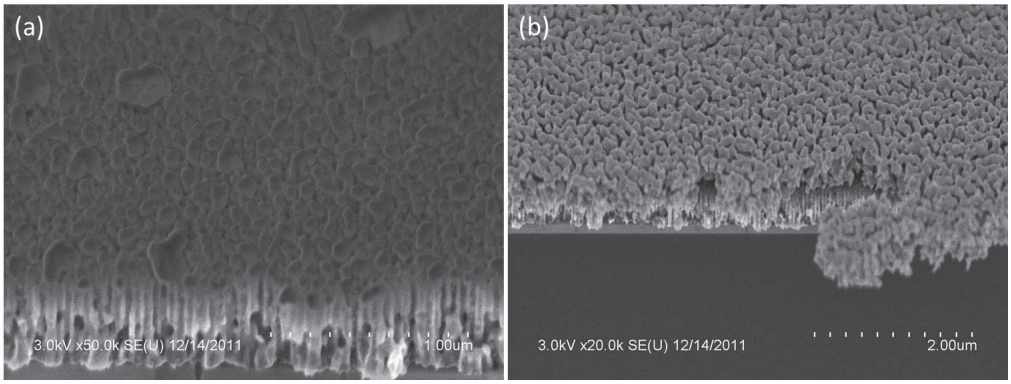


Figure 4.39: SEM cross-sections of a porous stack after the electrode printing at (a) 12 V and (b) 18 V.

Figure 4.39(a) corresponds to electrodes printed with a voltage of 12 V, whereas Figure 4.39(b) shows electrodes printed with a voltage of 18 V (that is bigger droplets). The inter-droplet distance has been set to 10 µm in both cases. The ink layer is clearly thinner in the first case, due to a lower amount of matter dispensed in each droplet. We haven't studied more thoroughly the influence of the printing conditions upon the morphology of the ink layer, since we realized that many particles penetrated inside the pores during the printing, no matter what the conditions were. This has to be avoided to prevent any short-circuit between the different layers of the porous stack.

As a potential solution, we tried to print the electrodes on a hotter sample, by heating it on a hot plate to 150°C, so as to evaporate the solvent as fast as possible and thus avoid an undesired penetration inside the pores. However, after performing the same experiments as described above, we unfortunately realized that particles have still penetrated inside the pores (Figure 4.40). Even if the pores are supposed to be filled with NWs, the pore filling has never reached 100 %, therefore a single pore filled with the conductive ink could potentially create a short-circuit.

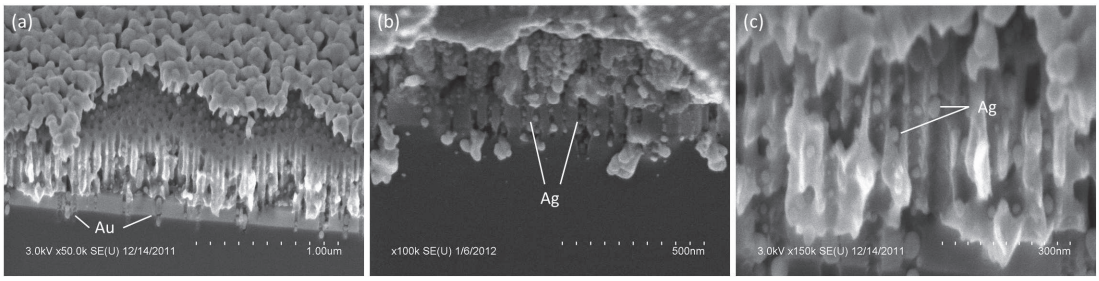


Figure 4.40: SEM cross-sections of a porous stack after the electrode printing on heated substrates. Small particles are visible inside the pores.

As said in the introduction, the second part of this section is dedicated to the patterning of a porous stack, with a view to preserving some Al areas during the whole fabrication process until the electrical measurements.

Localized porous stack

During the multi-stack fabrication process, because the peripheral part of the 2" wafers are outside the anodization area, an aluminium ring surface remains exposed to air. One could find it convenient to use it as a gate contact for subsequent electrical measurement, since this layer is necessarily in contact with SiNWs that grew inside the stack, at least for primary and basic measurements. It unfortunately turns out that this surface is exposed to all the "violent" treatments that make the process flow, especially plasma etchings, which leads to a very damaged surface, unusable for any electrical contact (Figure 4.41). Therefore, a protective layer must be present during all the process flow, keeping some areas of the Al layer away from bombardment and chemical attacks, until its removal that will reveal a clean, intact Al layer, suitable for an electrical contact.

A first basic, simple attempt has been carried out using Kapton tape applied on a part of the Al layer during the anodization. Nevertheless, a PAA layer formed anyway under the protective tape and, as we could expect, the removal of the tape after the anodization led to important damage on the sample.

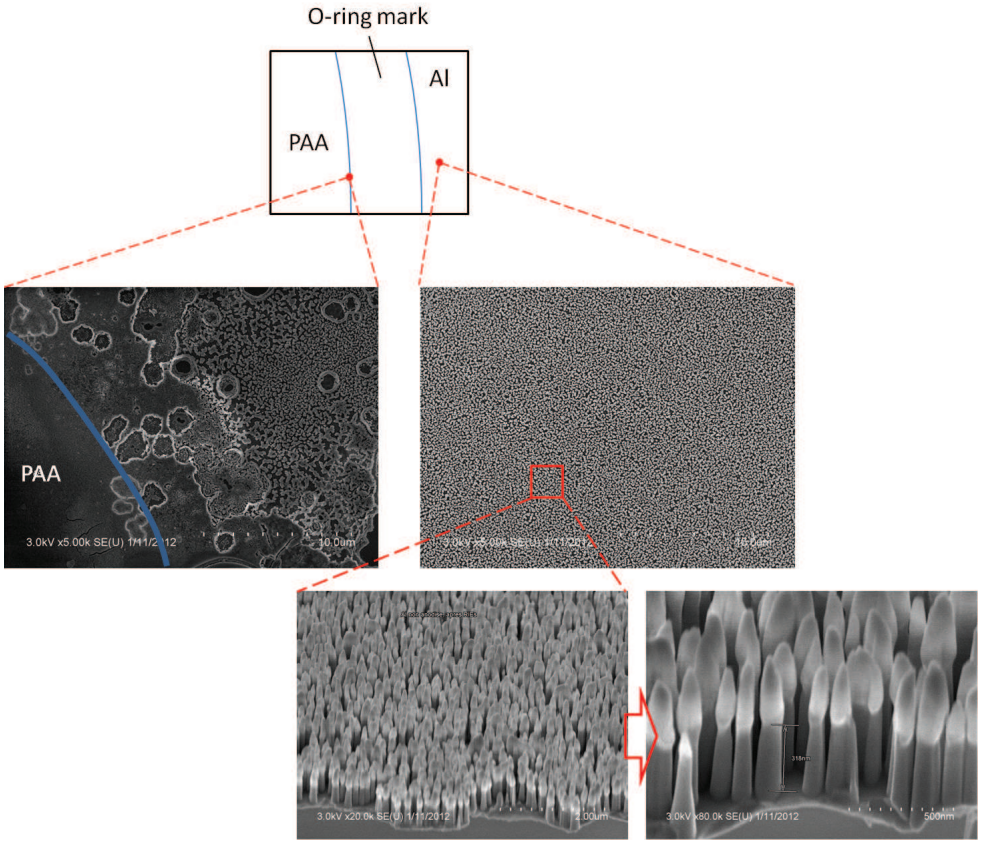


Figure 4.41: SEM pictures of the o-ring area (inside and beyond) after the anodization step and the Al RIE.

Patterning with a photoresist layer

A simple patterning method has been reported in 2009 by Juhász et al., [39], and is based (among others) on the use of a photoresist as a barrier layer to the anodization of an Al layer. They used positive photoresists with high thicknesses (> 2 µm) and classical photolithography to define some patterns in the photoresist layer that coated an Al layer (see the setup in Figure 4.42). After the anodization, it has been found that only the open areas were anodized and therefore porous, and that the resist-protected areas were still pure Al. The authors add that a high resist thickness has allowed to prevent pinhole defects and to limit the oxidation of the Al layer under the edges of the resist patterns.

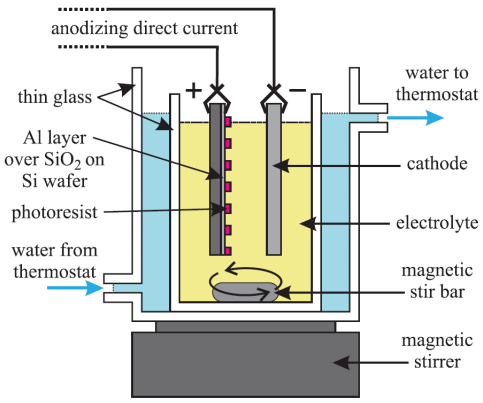


Figure 4.42: Experimental setup for selective anodization, as used in [39].

We carried out a similar experiment to realize local anodization of an Al layer. On a classical 2" Si wafer covered with an Al layer, we deposited a 1.2 µm-thick photoresist layer (we used SPR 700) with a spin coater at 4000 rpm for 30 s, which led to a 1.2 µm-thick resist layer. After a 5-min baking at 110°C (on a hot plate), the sample has been exposed to UV rays for 5 s, through a hard mask designed by our team. The UV rays make the exposed resist soluble in a specific chemical, called developer, and is therefore called positive resist (we speak about negative resist when the exposed parts become non-soluble, while the non-exposed parts are already soluble). The developer was MF 319, and the sample has been immersed in it for 25 s to reveal the unexposed parts of the resist. The sample was subsequently rinsed in deionized water for 3 min and dried under N_2. The global process is visible in Figure 4.43. The patterns mostly consist in basic shapes, like rectangles, squares or crosses, as well as more complex shapes that are the alignment crosses (see Figure 4.44(a)). As can be seen on Figure 4.44(b), the smallest patterns (10 µm crosses) are not well-defined After this patterning step, an anodization has been performed as usual. We used a 0.3 M sulfuric acid and a voltage of 20 V for 2 min to anodize the Al layer only in the openings defined in the resist layer. We didn't performed the two-step anodization described in chapter 1, since the only goal here is to check whether the resist acts as a good barrier. After the anodization, the photoresist is simply removed with acetone. We observed the sample with SEM and grouped the pictures in Figure 4.45. We noticed that the Al has been anodized in the exposed areas (Figure 4.45(a)), with an expected bad ordering due to a single anodization step. However, after a 9-min pore widening (performed in H_3PO_4), we realized that the top-view PAA appearance was rather comparable with samples anodized twice (Figure 4.45(b)). Interestingly, no pore has been found in the protected areas, as shown in Figure 4.45(c), which proves the efficiency of the 1.2-thick resist layer in preventing the oxidation of the Al layer, at least under this voltage (20 V) and for this duration (2 min). Nevertheless, a large transition zone ($\approx$ 20 µm wide) has been found on the former resist edges (Figure 4.46), and corresponding to a limited or partial anodization. As we move away from the anodization zone through this transition zone, the pore get smaller

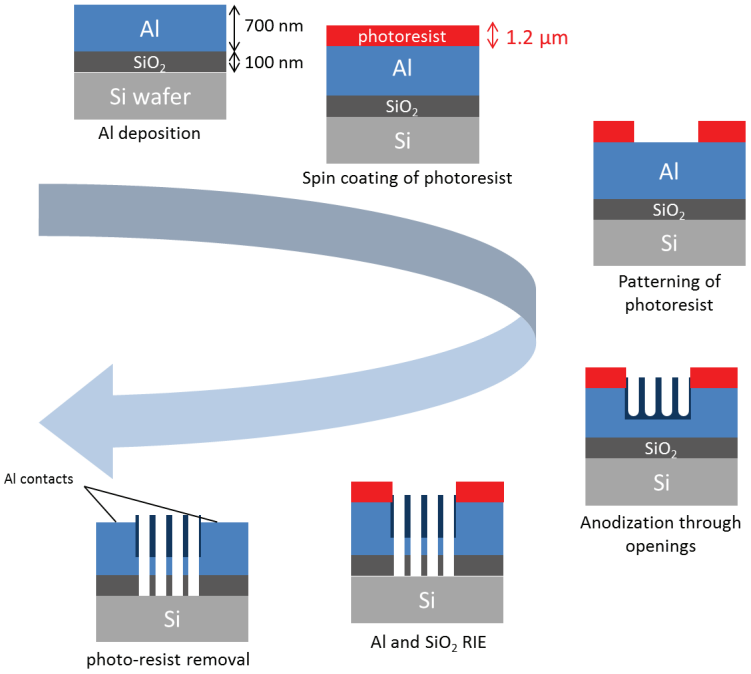
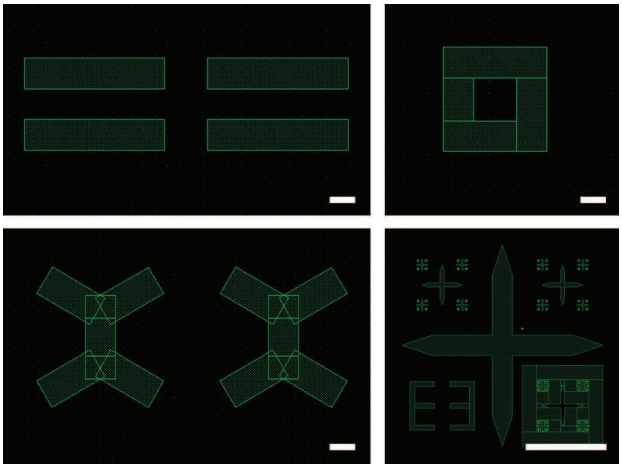
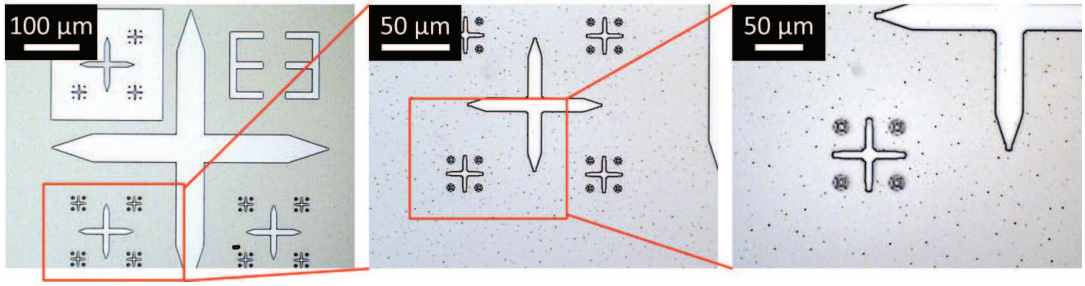


Figure 4.43: Global process of the localized formation of the porous stack using photoresist as a mask. Thicknesses are not to scale.

until they completely disappear (Figure 4.46) This result is very positive regarding the protected Al areas, that hasn't been anodized. However, the single anodization step may not provide a satisfactory ordering in the PAA. We therefore tried to perform the classical two-step anodization, which includes the step of PAA removal between the first and the second anodization, while the protective resist layer is still present. With a view to preventing a too irregular surface due to the PAA removal, one should perform a short first anodization, so that only a small thickness of Al is removed. The same 2-min anodization has therefore been performed before removing the as-formed PAA in our etching solution (H_3PO_4 + CrO_3, see details in chapter 1), followed by a 7-min anodization in order to form the final PAA. The first thing we noted is the unexpectedly high current observed during the second anodization (Figure 4.47). Indeed, while the first anodization current was limited to 0.16 mA, the second anodization current reaches values as high as 0.70 mA (more than 4 times higher) during the plateau, which has nothing to see with the higher value pointed out for second anodization in chapter 1, but is more characteristic of an entire 2" wafer anodization. This indicates that the whole surface of the Al layer has been anodized, which has been confirmed by observing the sample with the SEM. Indeed, we can see in Figure 4.48(a) that the surface that used to be under the resist layer has been perforated with multiple tiny holes because of alumina formation. Concerning the pore arrangement, we can see on Figure 4.48(b) that the pore ordering is conformal to what we usually get after a two-step anodization, but that no



(a)



(b)

Figure 4.44: Some examples of patterns we designed for the SiO_2 mask etching. (a) Design software views and (b) optical microscope pictures of the alignment crosses after the resist development. Scale bars in (a) are 200 nm.

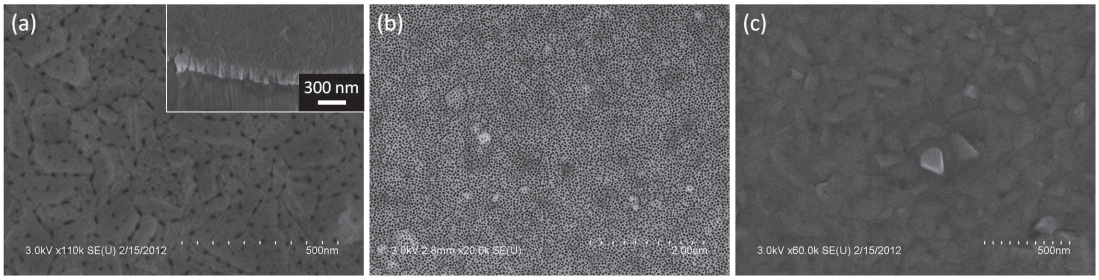


Figure 4.45: SEM top-views of (a) a PAA after a one-step anodization (cross-section in the inset), (b) a PAA after a one-step anodization and a 9-min pore widening (c) the Al surface formerly covered with photoresist.

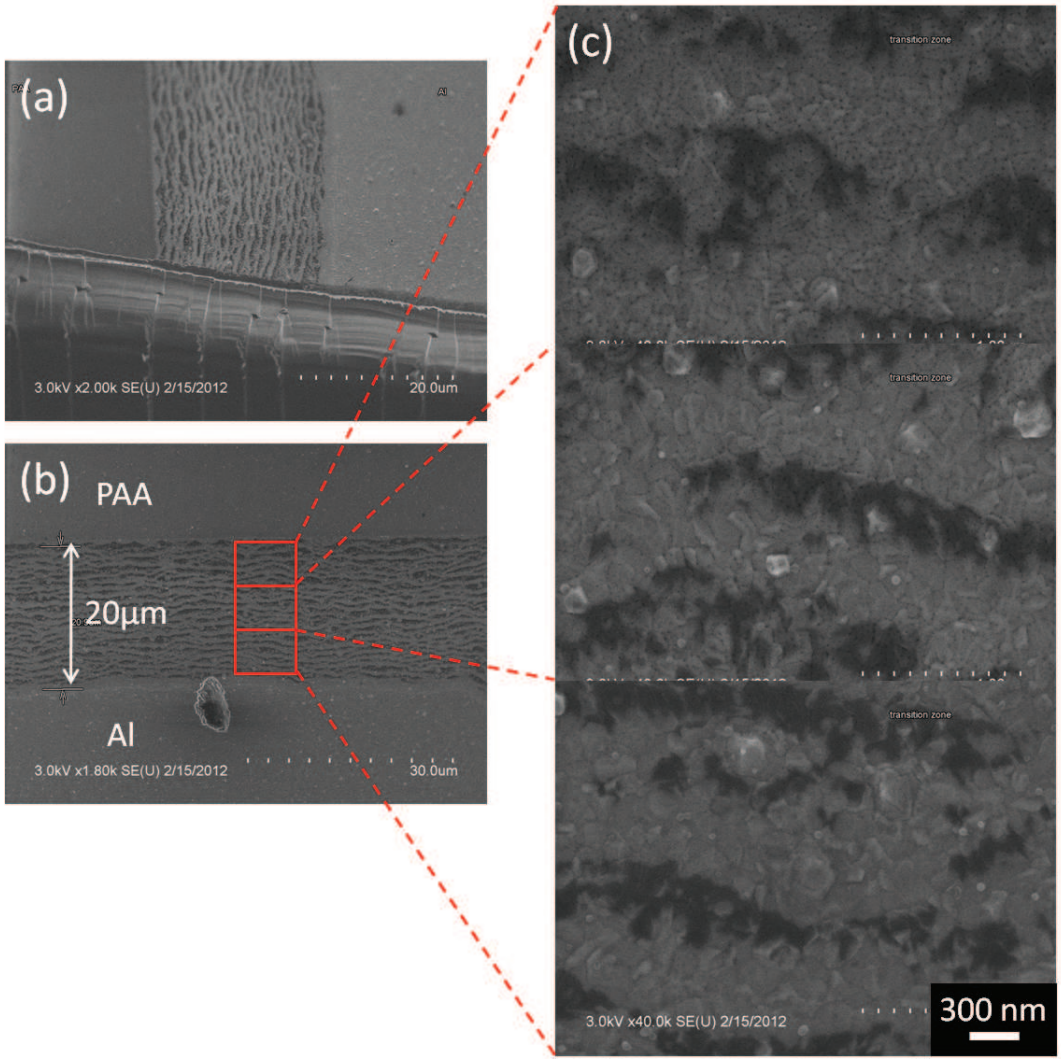


Figure 4.46: (a) Cross-section and (b) top-view of the transition zone between the PAA and the protected Al. (c) Magnifications of specific parts of the transition zone.

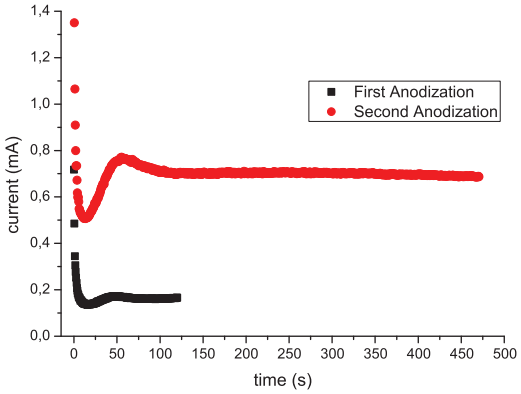


Figure 4.47: First anodization (FA) and second anodization (SA) I(t) curves corresponding to the PAA formation with photoresist as a barrier (the whole SA lasted about 8 min).

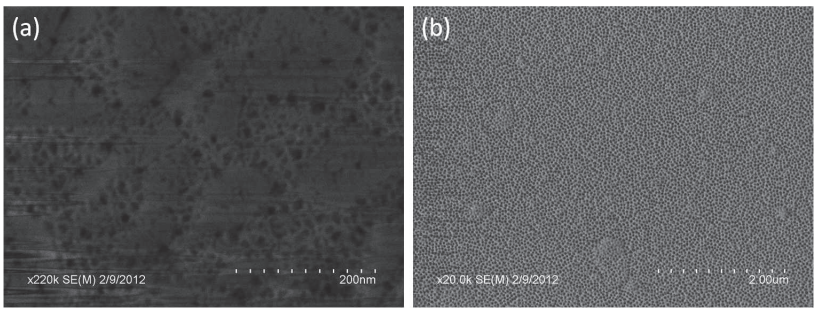
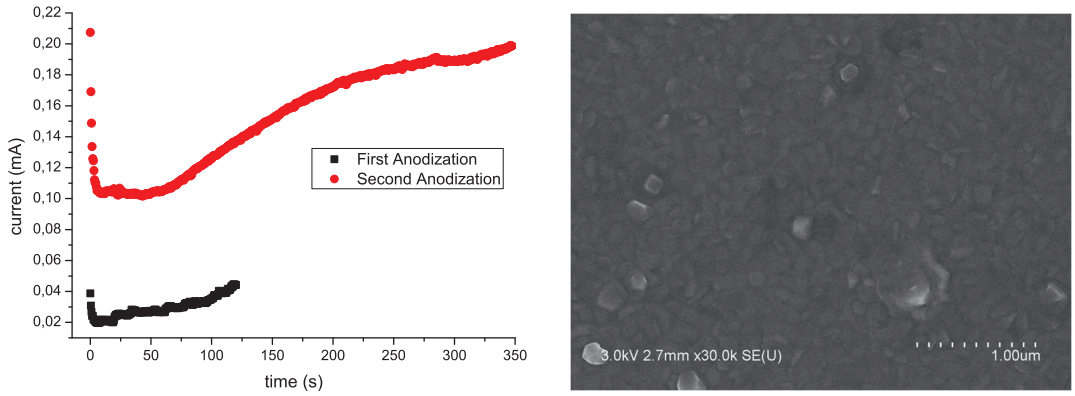


Figure 4.48: SEM top views of a sample after a two-step anodization of (a) the surface under the resist and (b) in the unprotected patterns.

big difference is visible with a single-step anodization.

Another experiment has been attempted by monitoring the second anodization current, and stopping the process as soon as the current reaches a too high value (that is an abnormal value regarding the limited surface exposed to the electrolyte). In this case, after a short plateau that lasted $\approx$ 40 s (with a current already much higher than during FA), the current started to increase rapidly, indicating the start of a leakage in the resist (see the graph in Figure 4.49(a)). When it reached $\approx$ 0.2 mA, we decided to stop the experiment, assuming that the resist was going to break down completely. It appeared that we did well since no pore has been seen on the protected surfaces after the resist removal (Figure 4.49(b)). A 20 µm-wide transition zone was also visible, in which the PAA thickness progressively decreases (Figure 4.50), showing that a lower electric field existed in this area. The two latter experiments showed that the two-step anodization was difficult using a photoresist layer as an insulating barrier, since it is very likely that leakages appear in the latter. For the moment, it is assumed that some damage form during the etching step between the first and the second anodization, and that the PAA



(a) (b)

Figure 4.49: (a) FA and SA I(t) curves corresponding to the PAA formation with photoresist as a barrier, with a shorter SA. (b) Al surface after two-step anodization and resist removal.

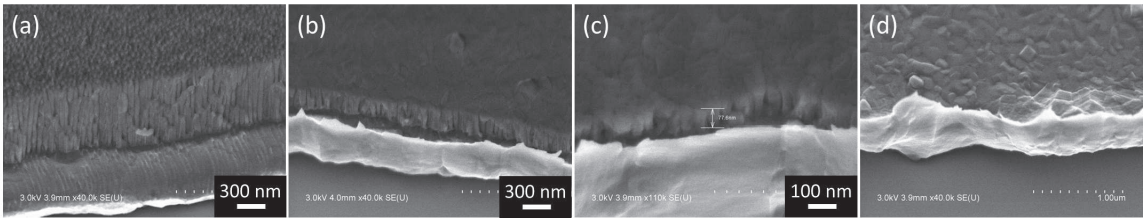


Figure 4.50: SEM cross-sections of a PAA in the transition area after a two-step anodization. (a) is in the unprotected area and (b), (c), and (d) correspond to what one can see as we head for the protected area. Note that third picture is magnified for the sake of visibility and that the scale is therefore different.

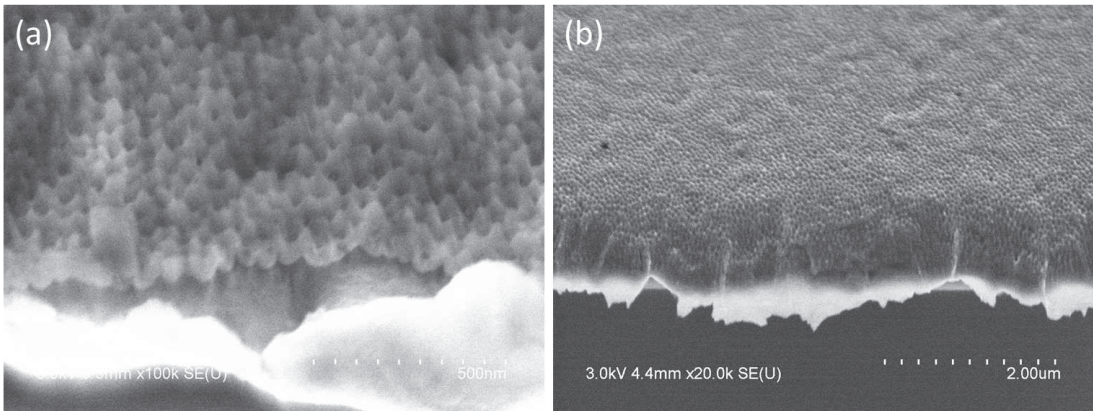


Figure 4.51: PAA formed under the resist, that has been deposited between the first and the second anodization to avoid PAA removal. The PAAs are very thin, especially in (b), where one can see it follow the curve of the underlying Al layer.

removal, added to the volume expansion of the Al during its anodization, could lead to the progressive formation of cracks and spaces under the resist layer, which would make the current increase. In order to remedy this problem, we imagined a preliminary first anodization all over the surface of the 2" sample, to realize the small imprints in the Al layer after the PAA removal. We called this step the "pre-patterning" of Al. Once this is achieved, we carried out the same process to deposit and pattern the photoresist onto the already marked Al layer. Thus, only the second anodization remains to be done without any etching step. Unfortunately, the second anodization current behaved exactly as described above, that is continuously increasing, indicating a leakage in the resist. This resulted in the formation of a very thin PAA even under the resist layer, as shown in Figure 4.51(a). The fact that we can see the pore bottom shape on the Al layer (Figure 4.51(b)) indicates that it must have been shortly anodized, thus making its observation so easy. Indeed, after a PAA removal, the pore prints in Al are normally unobservable. The Al pre-patterning doesn't seem to be an efficient method to get round the problem of anodization under the resist, which seems contradictory since the pre-patterned Al was supposed to behave just like a normal Al layer before a first anodization. We suppose that the pore prints might prevent a good contact between the resist and the Al layer, thus creating some leakages.

We kept to only one anodization step, without pre-patterning, but we rapidly found out that the problem of leakages wasn't only based on the fact that the anodization is performed in one or two steps, but also on the duration of these steps. Indeed, in order to fabricate a thick PAA, we performed an 8-min single anodization, and realized that the current started to increase from 2 min. After a few minutes, it stabilized at 0.21 mA, while the plateau was supposed to stay around 0.15 mA (see Figure 4.52). However, no pore was visible in the Al layer when we removed the resist, despite the current increase. We think that the current stabilization has occurred at a sufficiently low value not to form pores in the Al layer. Nevertheless, a greater increase could lead to the total break

down of the resist in a single anodization step, and thus lead the formation of pores under the latter. It is therefore thought that the combination of the PAA etching between the first and the second anodization step and a too long anodization inevitably leads to a flaw in the barrier role of the resist.

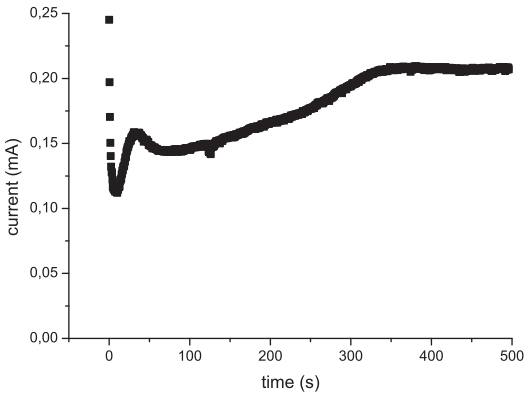


Figure 4.52: Single long anodization I(t) curve corresponding to the PAA formation with photoresist as a barrier.

An ICP etching has therefore been performed on a sample anodized in a single step, so as to etch the Al layer through the as-formed PAA. We realized that a well-ordered, proper PAA, and therefore formed by two-step anodization was actually required. Indeed, after a typical Al etching (described earlier in this chapter) we noticed irregularities in the etched layer. Some parts of the sample exhibited short through-hole pores in the Al, while other parts exhibited twice as long pores, still not open on the underlying SiO_2 layer (Figure 4.53). This shows that the PAA formed after a one-step anodization is not compatible with the subsequent Al plasma etching planned by our fabrication process, which can be explained by tilted pores or barrier layer thickness variation, obtained after a single-step anodization.

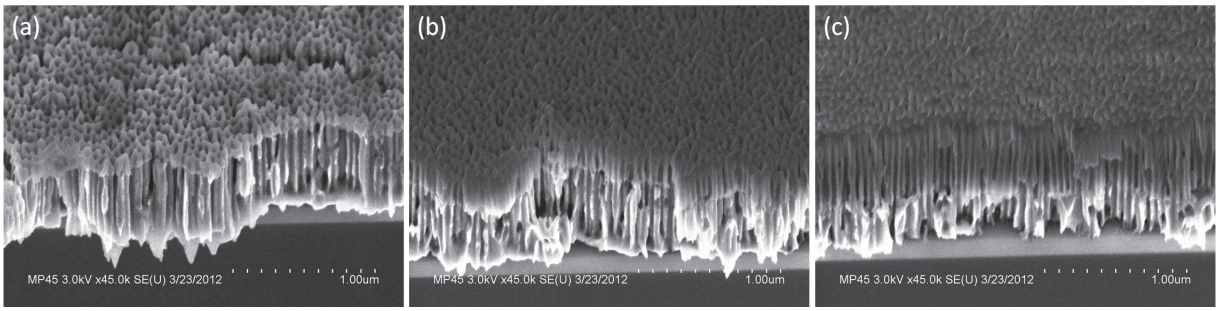


Figure 4.53: SEM cross-sections taken at different places of a sample after a one-step anodization and a 6 min Al etching. (a), (b) and (c) show some large thickness disparities in the PAA and the Al layer.

The photoresist layer may seem to be a convenient and simple way to realize a protective layer on the aluminium, but a more insulating, thick layer should be used to put up with a two-step anodization. Basing on two other articles where SiO_2 had been used as a mask ([40], [41]), we have tried to pattern a SiO_2 layer onto our Al layer in order to realize a patterned PAA, and then a patterned porous stack.

Patterning with an SiO_2 layer

Of course, using an SiO_2 layer requires more steps than using a simple photoresist layer, since the patterning of the SiO_2 itself requires the patterning of a photoresist layer, in between the SiO_2 deposition and its partial etching. A 500 nm thick SiO_2 layer has been realized in a Plasma-Enhanced Chemical Vapor Deposition (PECVD) reactor, that allows a low-temperature deposition (340°C) thanks to the plasma that provides energy to the gaseous species in the reactor. We used SiH_4 (40 sccm) and NO_2 (2000 sccm) at 500 mTorr, for 100 min. Once deposited, the SiO_2 layer has been covered with the same 1.2 µm-thick resist layer as above in which the same patterns have been defined. Thus, after the resist development, all the SiO_2 layer is covered with resist, except some small areas (typically less than a mm^2) that remain exposed to air. A plasma etching is then performed to remove the SiO_2 layer where the resist doesn't protect it. Some small openings are thus realized in the SiO_2 layer that will play the role of a mask for the subsequent anodization step. Beforehand of course the whole protective resist is removed with acetone. The process is presented in Figure 4.54.

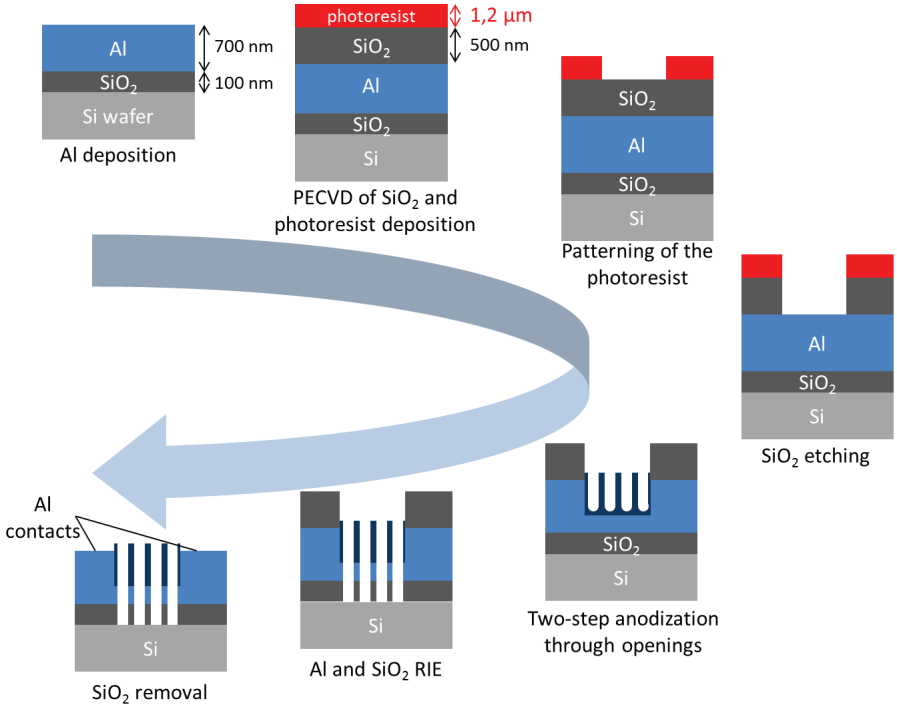


Figure 4.54: Global process of the localized formation of the porous stack using SiO_2 as a mask. Thicknesses are not to scale.

Four different recipes have been tried, including the one detailed in Table 4.2. The three other recipes have been chosen because they had been developed for silicon oxide deep etching, earlier by another team working on this equipment. Table 4.7 groups the conditions of these three recipes, and reminds the one used for the etching of pores in SiO_2 through PAA.

Gas ratio	Pressure	Platen power	Coil power
CHF_3:SF_6:O_2:He = 100:5:5:10 sccm	35 mTorr	150 W	100 W
CHF_3:SF_6:O_2:He = 100:5:5:10 sccm	15 mTorr	150 W	100 W
CHF_3:O_2 = 100:3 sccm	15 mTorr	150 W	100 W
CHF_3:SF_6:O_2 = 100:5:2 sccm	4 mTorr	150 W	300 W

Table 4.7: Summary table of the four recipes we tried to realize openings in the SiO_2 mask.

The three first ones basically led to similar results. Besides the fact that the patterns were rather badly defined in the SiO_2 layer, the Al layer was highly damaged after the SiO_2 etching (Figure 4.55). Despite the good selectivity of the gas mix we used regarding aluminium, and the the surface of the underlying aluminium has always presented the curly, round-shape structures after the etching shown in Figure 4.55(b).

We therefore decided to try the recipe we have always used for the realization of pores

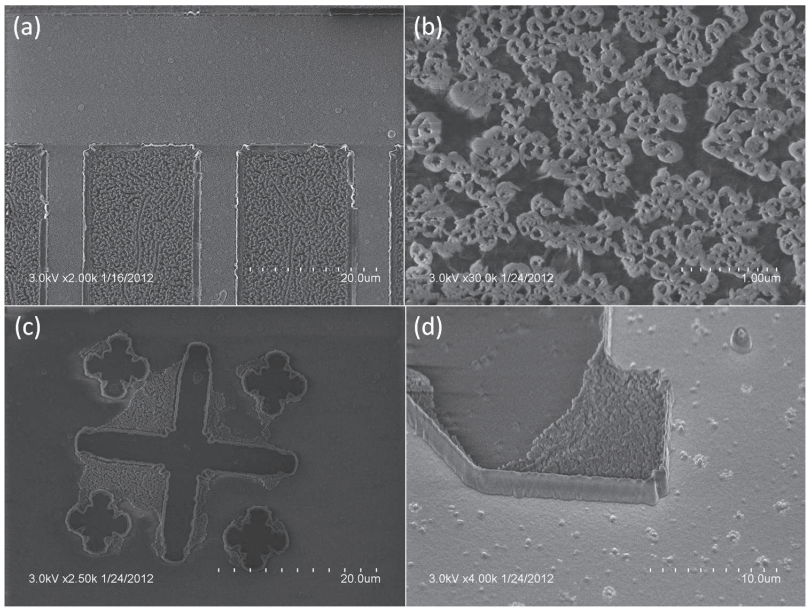


Figure 4.55: SEM pictures of some patterns realized in a SiO_2 layer. The SiO_2 etching recipe is the first one in Table 4.7, and similar results have been obtained with the second and third recipes. Badly defined etchings are particularly visible in (c), in the corners of the crosses.

in SiO_2. Interestingly, we immediately obtained much better results, since the Al surface looked intact, despite some impurities on its surface. We performed an 11 min etching, and stopped it when the end point detection curve started to stabilize. Figure 4.56(a) and (b) show that the patterns are better defined, especially in corners, but the edges are still very rough, as visible in Figure 4.56(b), (c) and (d). However, the goal wasn't to optimize the quality of the etching in the SiO_2 mask, but to realize some clean Al areas around a porous structure, which has been successfully achieved. Due to bombarding effect during the Al etching through the PAA, added to the bottom SiO_2 layer etching through PAA and Al, the SiO_2 mask needs to be very thick, even if the bottom SiO_2 layer is only 100-nm thick and that the Al etching chemistry is selective regarding SiO_2. Indeed, a 200-nm thick SiO_2 mask were not enough to put with both etchings, and disappeared before the end of the bottom SiO_2 layer. We therefore deposited a 500-nm thick SiO_2 mask (using PECVD), performed the two-anodization step, the Al etching and finally the SiO_2 etching.

We successfully carried out a two-step anodization using a thick SiO_2 mask, with stable currents during both anodization steps (Figure 4.57(a)). This led to a well-ordered PAA, with round-shaped pores before any pore widening (contrary to the sample shown in Figure 4.45). Figure 4.58 presents some pictures of the as-formed PAA. The pores are slightly tilted towards the neighbouring Al layer (4.58(b)), which indicates the electric field local direction near the boundary delimited by the SiO_2 mask. On Figure 4.58(c), we note that the edge of the SiO_2 mask is even thicker than the mask itself, probably

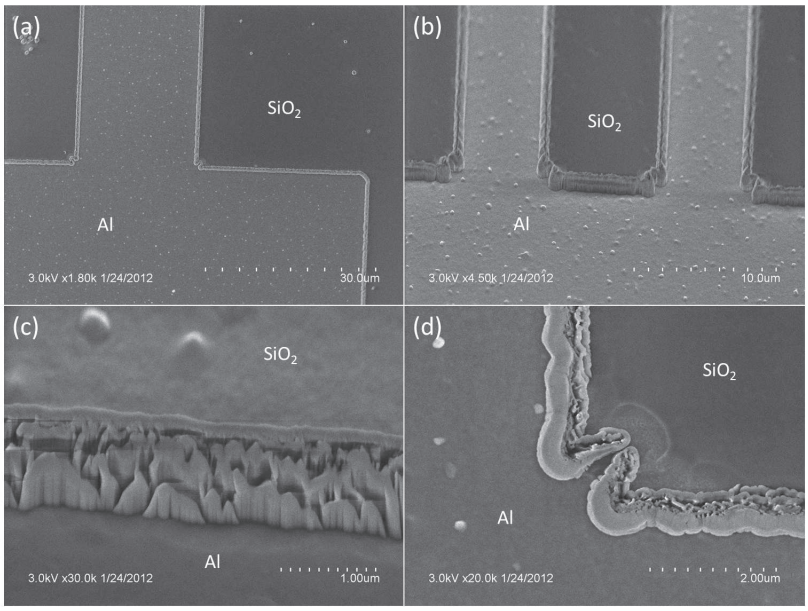
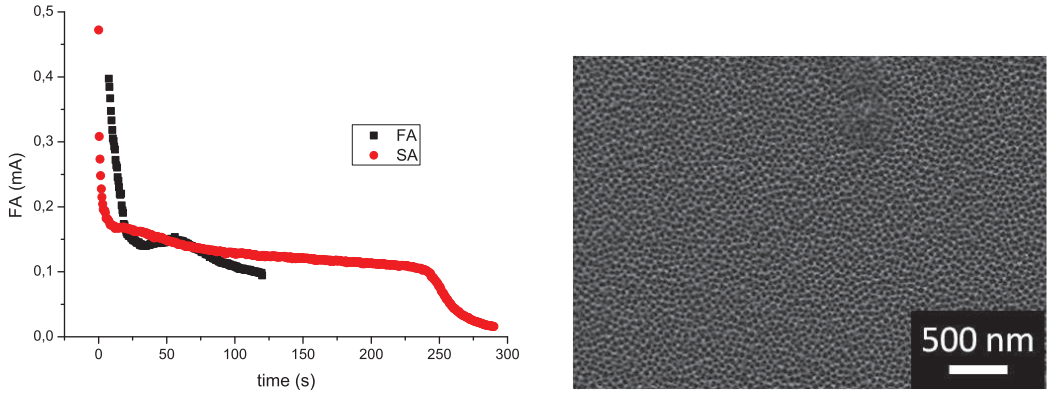


Figure 4.56: SEM pictures of some patterns realized in a SiO_2 layer, etched with the fourth recipe of Table 4.7. (c) and (d) show the edge of the SiO_2 mask in cross-section and top view, respectively.

due to the massive formation of carbon and fluor-based polymers during the Bosch-like etching. We have already pointed out these edges in Figure 4.56(d).

Subsequently, we performed the Al plasma etching to create vertical pores in the Al layer. We use the recipe detailed in Table 4.1 for 3 min (after a 14-min barrier layer wet etching) to dig this 200-nm thick Al layer. Thanks to the good ordering a good uniformity provided by the two-step anodization, the Al etching is properly done, and leads to straight, solid pores in the Al layer, that all open on the SiO_2 layer (Figure 4.59(a)). In this case, the remaining PAA thickness is evaluated to 300-350 nm, which is enough for perform the subsequent SiO_2 etching. The latter has been performed for 3'30 or 4'30, leading to through-hole pores in the SiO_2 layer, with a more or less big hole in the Si substrate depending on the etching duration (the sample shown in Figure 4.59(b) has been etched for 3'30). One can notice a last time the decreasing thickness of the PAA as the two etchings are carried out, to finally reach an optimized thickness of $\approx$ 100-150 nm. Figure 4.59(c) shows the boundary area, where porous and non-porous stack meet. We can see both Al and SiO_2 layers, protected under the thick SiO_2 mask. The white arrow points out the very last pores visible in the bottom SiO_2 layer.

As a conclusion to this part, we can say that many experiments have been done in order to realize a patterned porous stack, and that this has finally been achieved. Most problems came from the nature and the behaviour of the mask layer (photoresist, SiO_2) rather than from the etching processes, that were found to work as good as for non-patterned etchings. We finally found out that a SiO_2 layer was quite more appropriate than photoresist, in spite of the additional steps needed to realize it. Some improvements



(a) (b)

Figure 4.57: (a) First and second anodization I(t) curves of a sample anodized through a 500-nm thick SiO_2 mask. (b) SEM top view of the as-formed PAA after the SA.

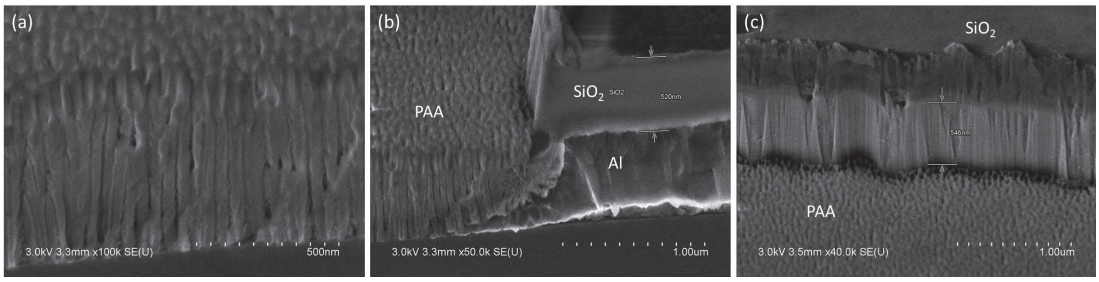


Figure 4.58: SEM cross-sections of a PAA realized through a 500-nm thick SiO_2 mask: (a) in the middle of a pattern, (b) and (c) near the boundary with the SiO_2 mask.

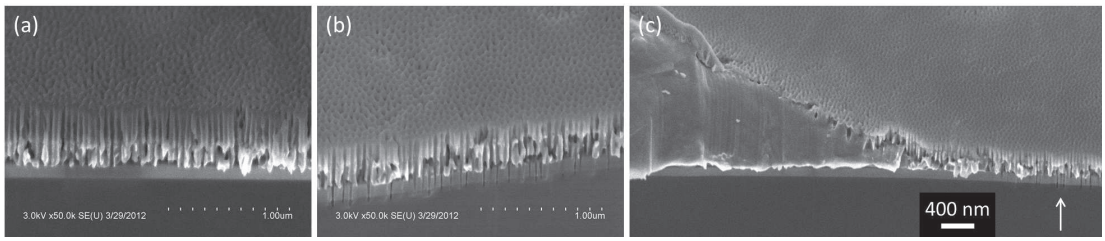


Figure 4.59: SEM cross-sections of a stack after (a) the two-step anodization and the Al etching, (b) the SiO_2 etching. (a) and (b) are in the middle of a pattern and (c) shows the boundary with the SiO_2 mask after Al and SiO_2 etchings. The white arrow points out the very last visible pores.

could be done concerning the edges of the SiO_2 mask, but are of less interest since it is planned to remove it completely for electrical measurements. This mask removal hasn't been studied yet, but it is planned to use a very simple RIE recipe to achieve a massive, fast etching, that doesn't need to be anisotropic. A pure SF_6 with a low platen power is thought to suit well so as not to over-etch the bottom SiO_2 layer. One should note that this mask etching step has to be performed before the nanostructure growth, since any etching step would remove (at least damage) the as-grown nanostructures.

	Photoresist	**SiO_2**
Can be used as a barrier layer	✓ but for short (< 2 min) anodization	✓
Compatible with two-step anodization	× must create cracks in resist during PAA removal	✓
Transition area	Wide (20 µm)	Small (< 1 µm)
Simplicity	Very convenient (only simple lithography is required)	Requires more fabrication steps (PECVD, RIE)
Underlying layers etchings	× tilted pores, barrier layer thickness	✓

Table 4.8: Comparative table of the two methods we tried to realize localized porous stack.

4.4 Conclusion

We successfully fabricated a nanoporous structure exhibiting straight, vertical and parallel pores able to receive individual 1D nanostructures, that is SiNWs or CNTs in our case. This complex porous stack has the particularity to incorporate a conductive layer that surrounds every single nanostructure, thus forming a collective surrounding gate electrode for every FET. The FET channels, i.e. the nanostructures, are easily and collectively organized, and completely similar in diameter thanks to the self-arrangement provided by the PAA. The vertical pores pass through three different layers, namely alumina, aluminium and silica (from the top to the bottom of the stack), and have been realized by two successive plasma etchings using the PAA as a hard mask.

Basing on the results obtained in chapter 2 and chapter 3, we studied Ni, Au and Cu electrodeposition, as well as CNT and SiNW growth in this porous stack, showing that both could be grown in it. Investigations have been carried out in order to optimize the thicknesses of the different layers, and to keep them intact so as electrodeposition and growths can be performed properly.

With a view to performing electrical measurements on these as-grown nanostructures, we developed a patterning method that allows their growth only on specific areas, leaving the rest of the sample available for the creation of a gate contact.

Though no electrical measurement showing a transistor behaviour has been made yet, a big step forward has been made by proving our ability to fabricate a complex and

nanometric porous stack, and to grow SiNWs and CNTs in it. Improvements could be brought for the electrodeposition, that appeared to be even trickier in the porous stack than in a simple PAA. This would require a better understanding of the stack behaviour regarding the applied signal. Given the aspect of the porous stack after SiNW growth, it is thought that the growth conditions found in this chapter are suitable and that the conditions to synthesize SiNWs with ultra-high density relies more on the efficiency of the electrodeposition.

No deep investigations have been carried out concerning the quality of the SiO_2 mask edges, that look quite rough after the realization of the openings in the mask. Even though it was not a problem for us since the patterns were millimeter-sized, a deeper work has to be done about this etching, using a more appropriate recipe if one wants to realize micrometer-sized openings.

Concerning a following source/drain contact, no work has been done except the electrode printing mentioned in the last section of this chapter. This method is very easy and convenient, but seems to be inappropriate for our porous surface, at least using the conditions mentioned in this chapter. Furthermore, the lower limit of the electrode size may limit the applications (a single ink droplet is several microns in diameter). Therefore, one ought to turn to classical evaporated deposits (evaporation, sputtering...) to realize the metallic contacts on the surface of the porous stack after the growth. Nevertheless, we fear that metal deposits inside the pores, just like we observed with the ink-jet method.

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Conclusion

This work has been realized in the framework of the use of nanostructures in microelectronics, which is the specificity of our team NanoMaDe in the lab. We focused on using 1D nanostructures that are CNTs or SiNWs as building blocks to fabricate a field effect transistor. For this purpose, an innovative method has been developed in our lab and has the advantage to collectively organize these nanostructures, which is one of the highest obstacle for people who try to manipulate them. Furthermore, this method doesn't require any costly equipment, since based on the self-organization of a particular structure, porous alumina.

During these three years and a half we improved several steps in the fabrication process and understood a lot of problems, which allowed to reach a well-advanced step of the global fabrication process of the FET. Indeed, we managed to grow both CNTs and SiNWs in vertical nanopores, composed of three different piled layers and providing the electrodes required for the electrical connections.

More precisely, here are the progresses achieved during this thesis:

- The PAA template fabrication has been studied with various conditions, making the customization of its different features possible, which was a prerequisite for a further use as an etching mask and as a well-ordered template. Calibration curves have been established, especially for anodization in sulfuric acid, which provides a good ordering with low voltage and thus lead to small pores. Besides, studies have been carried out to fabricate through-hole vertical pores of a desired length and diameter.

- We have extended the possibilities of electrodeposition to other metals, like Au and Cu, besides Ni, and have investigated several parameters to understand in what extent the electrodeposition could be controlled. We have successfully deposited Au, Cu and Ni, but a lack of uniformity has been found, especially for Au and Cu. We have proposed a promising method based on a plasma exposure to improve the filling efficiency of the catalyst particles. Though this method remains to be investigated more deeply, we explain the changes observed in the pore filling by a variation in the hydrophilicity of the pore walls, which could impact the penetration of the electrolyte in the pores.

- The combination of these results allowed to carry out a study about organized CNT and SiNW growth, using PAA as a porous template. We have showed that

the hot tungsten filament placed in our CVD reactor was useful to prevent the parasitic deposition of amorphous silicon on one hand (for SiNWs growth), and to make the methane molecules dissociation easier on the other (CNT growth). Optimized growth conditions have been found in order to successfully grow these 1D nanostructures vertically, parallel, and with a similar diameter thanks to the PAA. We have also discovered special structures, namely SiNTs, that probably form from the deposition of amorphous silicon on the pore walls under specific conditions. Basic electrical measurements has proved that SiNWs could connect the top of a PAA to the bottom, showing that this nanostructure could be used as a semiconducting channel for a vertical FET. A TEM investigation has been carried out to observe closer some SiNWs grown under different conditions, and we have shown that the NWs grown under some specific conditions were crystalline and presented a twinned structure.

- The biggest part of the work of this thesis must be the fabrication of a porous stack and the subsequent growth of nanostructures in it. Vertical nanopores with diameter as low as 20 nm have been realized in a stack composed of three different piled thin layers, using plasma etchings through a PAA template as a hard mask. Taking into account the thinning of the PAA due to the plasma etching, a global process has been developed to fabricate the porous stack with optimized thicknesses and in a reproducible way, on areas as large as 2" wafers. For the electrical measurements needs, we had to think about a method to protect some parts of the Al layer from all the steps of the fabrication process, and have therefore developed a masking technique using an SiO_2 layer. This has proved to be an efficient barrier for Al anodization and plasma etchings, though some improvements can be brought for the precision of the patterns in the SiO_2 mask.

For a better global uniformity and quality of our device, several ideas are proposed.

It has been reported that very highly-ordered PAAs have been fabricated by using ultra-long anodization (several hours) on high-purity Al sheets. To use them on top of our stack (Al + SiO_2), a tricky and delicate transfer step would be required, but this could eliminate the problems related to inhomogeneous anodization and etchings.

A systematic study of the impact of a water plasma on the PAA seems to be necessary, since some variable results have been obtained. In particular the exposure duration and the diffusion current are thought to be decisive regarding the subsequent behaviour of the sample.

An interesting research subject would be to investigate more deeply the SiNW crystalline structure dependence on the growth conditions, which has been started with the TEM studies presented in chapter 3. We know the crystalline structure of SiNWs is intimately linked to their electrical properties, and our studies have shown a wide variety of structures. It would be therefore very useful to be able to control the crystalline structure so easily.

In 2011, Intel has started the series production of its tri-gate transistor, which provides a better control over the channel, and thus exhibits a lowered power consumption and a

faster state switch. We propose to go further by using a surrounding gate and by adding the vertical dimension to the transistor configuration, without making the fabrication process heavy or expensive. Indeed, the vertical channel and the surrounding gate could lead to ultra-high density integration, with a theoretical better gate control. This is why it is worth to make some efforts to push ahead with this promising work.