Epitaxial growth of Si(Ge) materials on Si and GaAs by low temperature PECVD: towards tandem devices

Romain Cariou

Doctoral thesis in Physics / Material Science

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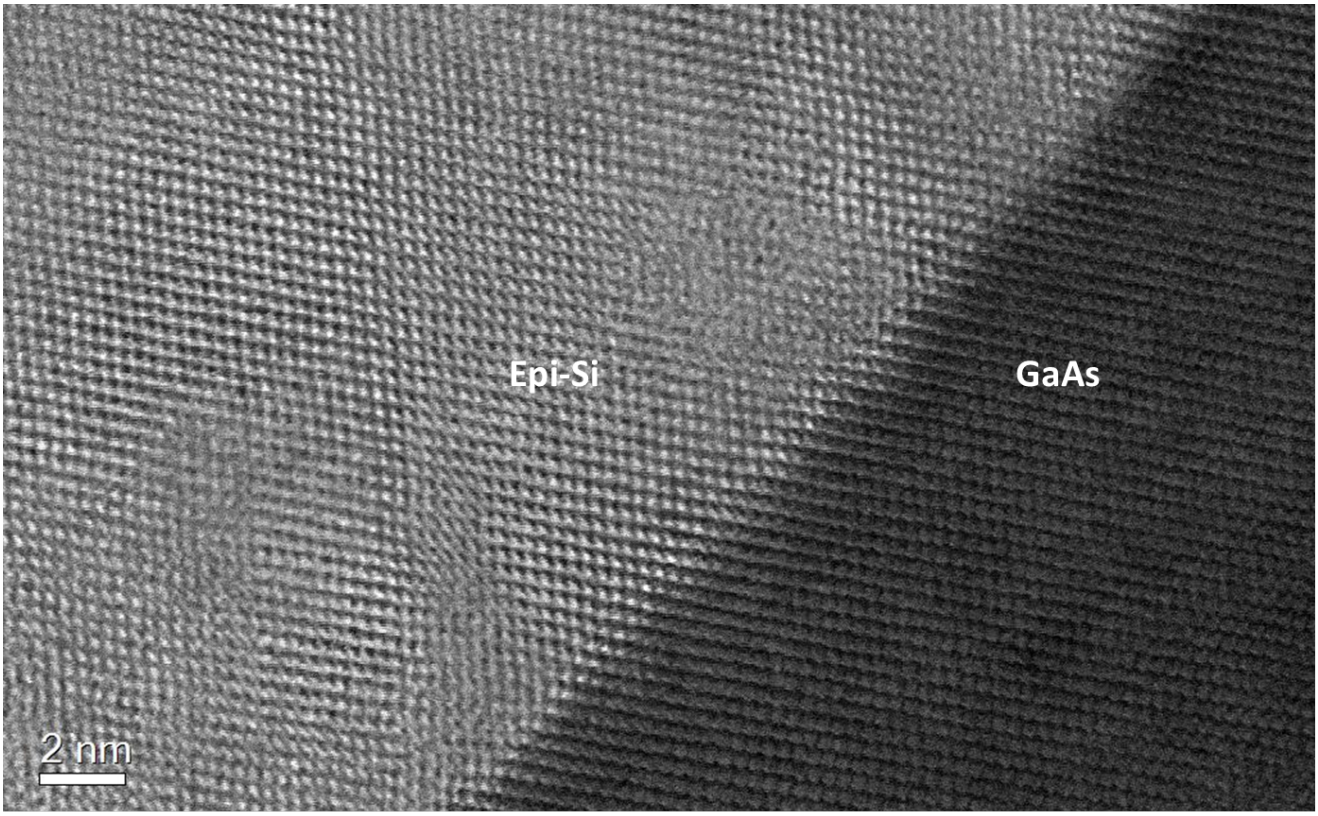

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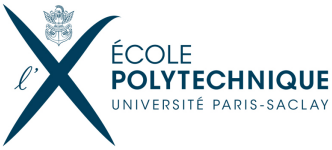

Thèse

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par

Romain Cariou

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Dr.	Jean-Louis Gentner	III-VLab	Supervisor
Prof.	Pere Roca i Cabarrocas	LPICM	Supervisor

In the deepest ocean
The bottom of the sea
Your eyes
They turn me

Why should I stay here?
Why should I stay?

I would be crazy not to follow
Follow where you lead
Your eyes
They turn me

Radiohead - Weird Fishes/Arpeggi

à ma belle Marion

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Contents

List of acronyms

Acronym	Unit	Definition
a-Si:H		Hydrogenated amorphous silicon
a-SiC:H		Hydogenated amorphous silicon carbide
BSF		Back Surface Field
c-Si		Monocrystalline Silicon
c-Ge		Monocrystalline Germanium
CVD		Chemical Vapor Deposition
$\mathbf{E}_F$	eV	Fermi level energy
$\mathbf{E}_g$	eV	optical bandgap energy
ε_i		Imaginary part of the pseudo dielectric function
epi-Ge		Epitaxial germanium
epi-Si		Epitaxial silicon
epi-SiGe		Epitaxial silicon germanium
FIB		Focused Ion Beam
FF	%	Fill factor
FWHM		Full Width at Half Maximum
HAADF		High-Angle Annular Dark-Field imaging
HF		Hydrofluoric acid
ITO		Indium Tin Oxide (Tin doped Indium Oxide)
$\mathbf{J}_{sc}$	$\mathrm{mA.cm^{-2}}$	Short-circuit current
LTE		Low Temperature Epitaxy (namely $\sim 200°\mathrm{C}$)
MBE		Molecular Beam Epitaxy
μ**c-Si:H**		Hydrogenated microcrystalline silicon
μ	$\mathrm{c^{-2}.V^{-1}.s^{-1}}$	Carrier mobility
PECVD		Plasma Enhanced Chemical Vapor Deposition
pm-Si:H		Hydrogenated polymorphous silicon
$\mathbf{R}_S$	$\Omega.\mathrm{cm^2}$	Series resistance
$\mathbf{R}_{Sh}$	$\Omega.\mathrm{cm^2}$	Shunt resistance
RTSE		Real Time Spectroscopic Ellipsometry
SEM		Scanning electron microscopy
SIMS		Secondary Ion Mass Spectrometry
sccm	$\mathrm{cm^3.min^{-1}}$	Standard cubic centimeter per minute
$\mathbf{S}_{rec}$	$\mathrm{cm^2.s^{-1}}$	Surface recombination velocity
STEM		Scanning Transmission Electron Microscopy
τ_{eff}	s	Effective lifetime
TEM		Transmission Electron Microscopy
TRMC		Time Resolved Microwave Conductivity
$\mathbf{V}_{oc}$	mV	Open-circuit voltage
XRD		X-ray Diffraction

Chapter 1

Photovoltaic energy outlook

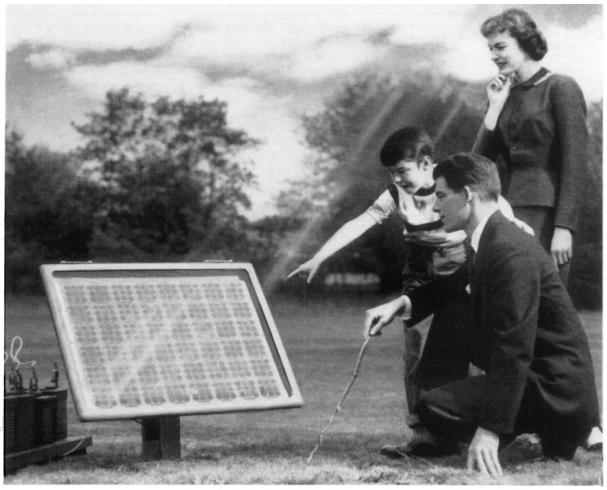
Contents

1.1 Introduction - context

"The ultimate answer to humanity's energy problems
rises every morning and sets every evening."[1]

"Ever since Archimedes, men have been searching for the secret of the sun. [...]The dream of ages has been brought closer by the Bell System Solar Battery. [...]The progress so far is like the opening of a door through which we can glimpse exciting new things for the future. Great benefits for the telephone users and for all mankind may come from this forward step in putting the energy of the sun to practical use". With those emphatic words, Bell Telephone Laboratories spread the news, in 1954[2], for their new invention: a device that can convert sun light into electricity (see Fig.1.1). Based on the photovoltaic effect, discovered in 1839 by Alexandre-Edmund Becquerel, this first solar panel, made of crystalline silicon p-n junction, had a 5-6% efficiency.

The sun is Earth's natural power source, driving the circulation of global wind and ocean currents, the cycle of water evaporation and condensation that creates rivers and lakes, and the biological cycles of photosynthesis and life. Indeed, the potential of solar energy, as underlined by the journal Nature in 2008[1], is tremendous: the total power received from the sun on earth exceeds by $\sim 10^4$ times the mean power consumed by Humanity. The solar energy, radiant light and heat from the sun, has been harnessed by humans since ancient times using a range of ever-evolving technologies. Three main solar energy conversion processes can be distinguished: i) the production of fuel (biomass), through natural and artificial photosynthesis. ii) The energy of the sun, concentrated or not, can also be used to produce heat for direct use or further conversion into electricity. iii) It is possible to convert directly solar energy into electricity, by creating electron-hole pairs in a photovoltaic cells. If we also take into account the secondary solar-powered resources (wind, wave power, hydroelectricity, etc.) the solar radiation account for most of the available renewable energy on earth. However only a minuscule fraction of the available solar energy is used.; solar's uses are mostly limited only by human ingenuity.



Something New Under the Sun. It's the Bell Solar Battery, made of thin discs of specially treated silicon, an ingredient of common sand. It converts the sun's rays directly into usable amounts of electricity. Simple and trouble-free. (The storage batteries beside the solar battery store up its electricity for night use.)

Bell System Solar Battery Converts Sun's Rays into Electricity!

Fig. 1.1 – "It's the Bell Laboratories Solar Battery, made of thin discs of specially treated silicon, an ingredient of common sand". Advertisement for the very first solar panel.[2]

The supply and demand of energy determine the course of global development in every sphere of human activity. Besides the energy from food necessary to sustain our body (∼2500 kCalories per day, corresponding to a 100 W light bulb), roughly 30 times more energy is used on average to make our life more comfortable. Sufficient supplies of clean energy are intimately linked with global stability, economic prosperity, and quality of life. Many of the global challenges humanity is facing today are driven by two factors: i) the continuing increase of the word population and ii) the growing energy demand from both the new developing and the developed countries. The evolution of the global population is represented in fig.1.2. The 7 billions threshold was reached roughly at the beginning of 2012, while 13 years earlier, there were only 6 billions people on the planet and 2 billions in 1927. This fast

[1]Editorial, Nature, 14th August 2008, A task of terawatts
[2]Science: Solar Batteries, Time magazine, 3 May 1954, Sun Electricity

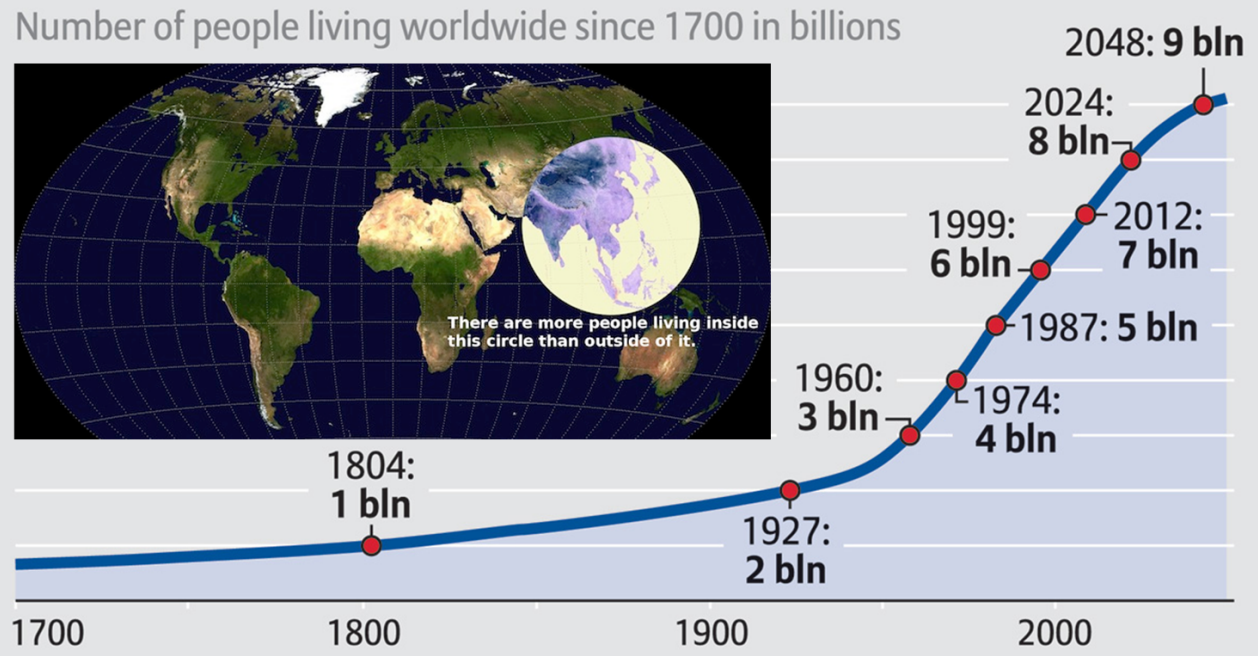


Fig. 1.2 – Evolution of the World population growth from the 18th century and foreseen trend. The population density is largely non-uniform as shown in the inset. Source: United Nations Population Prospects.

increase will most likely lead to an additional billion of people by 2024. Consequently, the world energy demand is projected to more than double (30 TW) by 2050, and more than triple (50 TW) by the end of this century. Covering 0.16% of the land on Earth with 10% efficient solar conversion systems would provide 20 TW of power, nearly twice the present world's consumption rate of fossil energy and the equivalent of 20 000 nuclear fission plants (1 GW). In comparison, the ultimate resources for oil, estimated at 3×10^{12} barrels represent the energy delivered by the Sun in one day and a half.

1.2 Photovoltaic market

Burning fossil fuels to produce energy is a short term solution that has long term negative impacts. From the accurate scientific understanding of the climate system (see IPCC report[1]), the influence of human activities on the climate system is clear. This is evident from the increasing greenhouse gas concentrations in the atmosphere, positive radiative forcing, observed warming of the atmosphere and oceans, reductions in snow and ice, global mean sea level rise, and changes in some climate extremes. For example, the atmospheric concentrations of carbon dioxide, methane, and nitrous oxide have increased to levels unprecedented in at least the last 800 000 years; carbon dioxide concentrations have increased by 40% since pre-industrial times, primarily from fossil fuel emissions and secondarily from net land use change emissions. Continued emissions of greenhouse gases will cause further warming and changes in all components of the climate system.

Today, oil, coal and gas account for nearly 80% of world final energy consumption, as shown in Fig.1.3. A diversification of energy sources is absolutely necessary in the current context of rarefaction of fossil resources, climate change and ever-growing energy prices. This shift to a new mode of production with better efficiency and less environmental impact becomes more obvious as we consider that global energy demand will more than double by 2050 and even more than treble by the end of century. Finding energy sources to satisfy the world's growing demand is one of society's foremost

[1]IPCC., Cambridge University Press, ISBN: 978–1–107–66182–0, 2013.

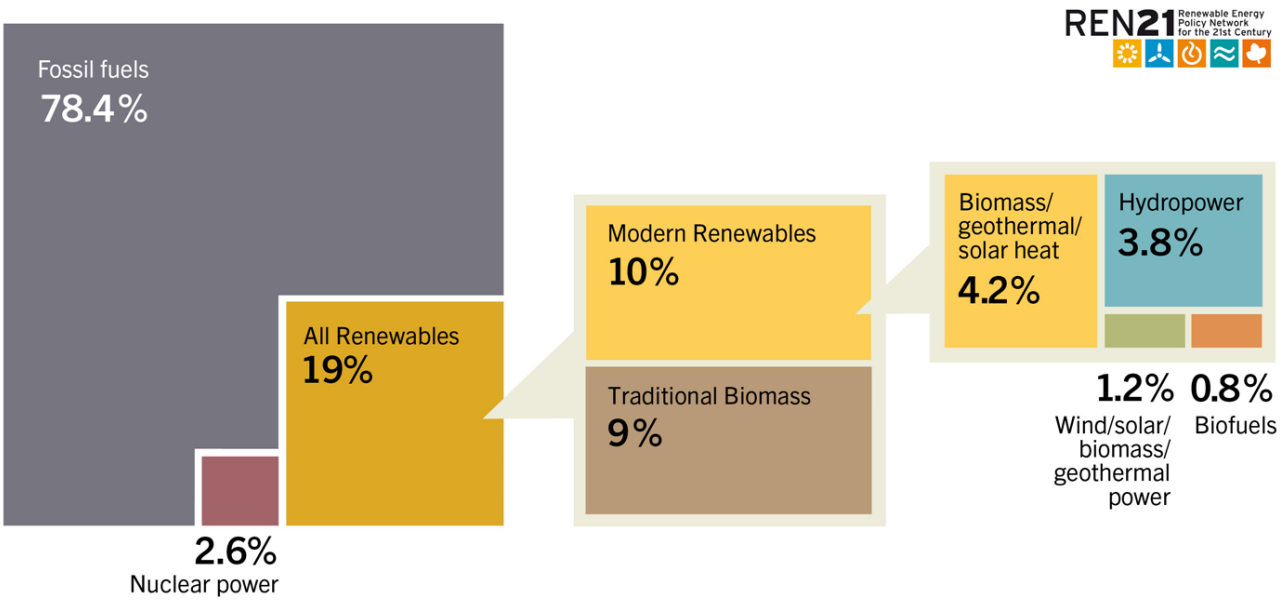


Fig. 1.3 – Estimated renewable energy share of global final energy consumption, in 2012[3].

challenges for this century. More particularly, the direct conversion of solar radiation into electricity with photovoltaic (PV) devices, is a very promising solution since the solar radiation is relatively well-distributed on Earth, there are no major geopolitical risks associated with this technology, and it can potentially cover a large fraction of today's an tomorrow's energy demand[2].

The fraction of renewable energy in the global final energy consumption in 2012 is estimated around 19%[3]. This value may seem important, however slightly less than half of it comes from traditional biomass, that is burning wood for cooking and heating, in developing countries. The share of modern renewable energies is thus only in the 10% range. Moreover, the wind/solar/geothermal energies sources represent only 1.2% of the global energy demand. Looking more specifically at electricity production, the share of photovoltaic technologies represent around 0.7%, while wind account for 2.9% and hydropower 16.4%.

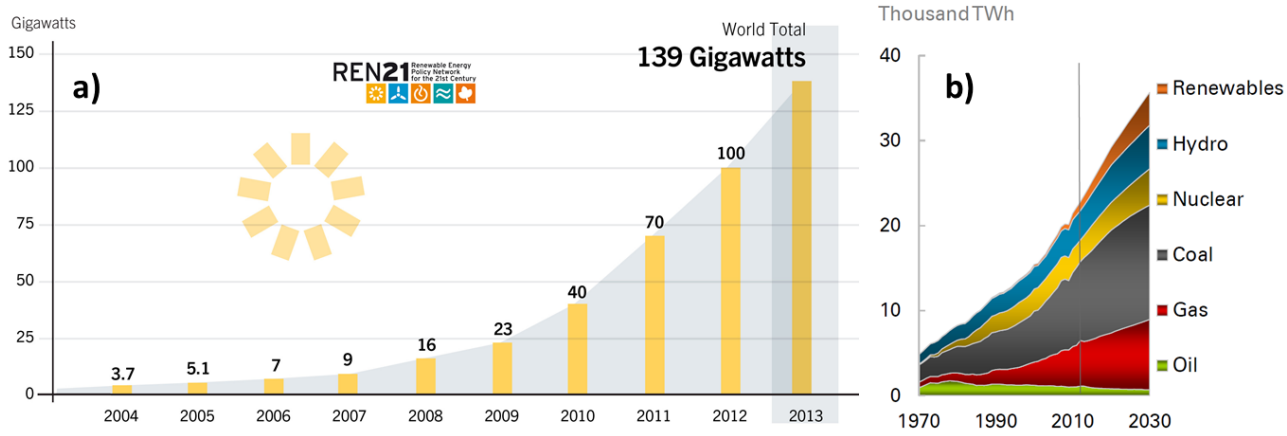


Fig. 1.4 – a) Total world solar PV capacity evolution from 2004 to 2013[3]. b) World electricity power generation in TWh[4].

[2] A. Slaoui et al., MRS Bulletin, **32**: 211–218, 2007.
[3] REN21., Renewables 2014 global status report, ISBN: 978–3–9815934–2–6, 2014.

However, despite contributing only to a tiny fraction of the energy mix, the photovoltaic market is growing fast, as shown in Fig.1.4-a): 39 GW of PV capacity were added in 2013 to the existing 100 GW of 2012. And, compared to 2013 level, almost half of the world PV capacity has been installed during the years 2011 and 2012. This two digit growth of the PV market has to be compared with the total electricity consumption increasing by roughly 2.5%[4] per year. Consequently the share of phovoltaic in global power electricity generation, and more generally the share of renewable, will increase in the coming years (see Fig.1.4-b)).

1.3 An intermittent energy

One of the major obstacles for extensive photovoltaic penetration into the grid, is the intermittency of this renewable power source (day/night alternation, daily/season weather fluctuation). While conventional electricity sources can produce at their nominal power more than 8000 hours per year, photovoltaic yields is estimated to produce an equivalent of about 1000 h/year at nominal power. It is indeed not acceptable for today's society to access electricity only when the wind is blowing and/or the sun shinning. So far, the intermittency of renewable sources has been balanced by back up peak power plants (gas, coal); this is of course mitigating the low carbon impact of renewable energies. To overcome this intermittency problem, several solutions have to be considered:

- The development of energy storage technology with low dissipation losses (pumped hydro, compressed air, fuel cells, batteries, etc.) can potentially smoothen the electricity production from renewables.
- Improving weather prediction and its correlation with electricity generation, on time scale spanning from minutes to days, is also crucial.
- Improving the grid interconnection between countries, e.g. at the European scale, can partially compensate the uncorrelated weather fluctuation at large scale.
- And finally, all this will require smart grids to adapt production, storage and consumption in an optimized way. Another option could be to implement local grid and decentralized storage.

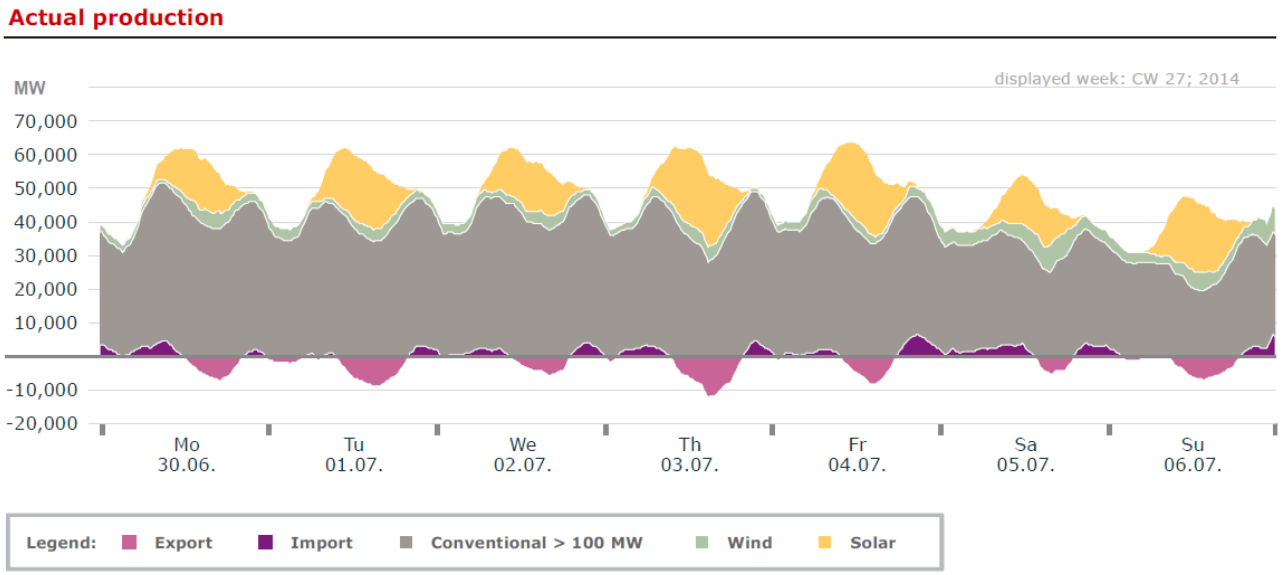


Fig. 1.5 – Electricity production (solar, wind and conventional sources) for the first week of July 2014 in Germany. From B. Burger[5].

[4] BP., Available online, www.bp.com/energyoutlook, 2014.

To illustrate the intermittent characteristic of solar photovoltaic energy, the electricity production in Germany, as presented by Fraunhofer ISE[5], during the first week of July 2014, is shown in Fig.1.5. On this graph, the share of PV electricity is represented in yellow. The peak of PV electricity production happens around noon, which corresponds also to the peak of electricity consumption; Germany even exports electricity during this peak production. More than 30% of the peak electricity consumption comes from solar PV panels. Of course this contribution can change a lot for less sunny weeks; in average, during the first 6 months of 2014, PV has contributed to 7% of German electricity mix. As a comparison, PV production in France, which features a higher sun irradiation, represented around 0.8% of the electricity mix in 2013.

1.4 Solar photovoltaic technologies

Much progress were made since the first solar panel from Bell Laboratories in 1954 (see Fig.1.1), reaching 5-6% efficiency. The record conversion efficiencies and their evolution, for laboratory scale solar cells, are reported in the NREL chart, in Fig.1.6. This chart includes all the PV technologies, and spans from 1975 to 2014, including the latest certified record cells[6]. Indeed, improving the photovoltaic power conversion efficiency has been driving research for years, since it has a major impact on electricity generation cost.

The highest conversion efficiencies, represented in purple in this graph, are achieved using semiconductors of the column III and V of the periodic table. The record certified efficiency to date is 44.7%[7] (and even 46% in december 2014), and these so-called III-V cells have still room for efficiency improvement. Such solar cells are based on complex multilayer architectures to collect and convert a large fraction of the incident solar energy. By concentrating the sunlight, the solar cell area (and thus the required material) can be reduced, while at the same time a logarithmic efficiency increase with the illumination is obtained, thus they are often used under concentrated light. However, these so-called III-V solar cells remain expensive and relatively scarce; consequently they are mainly used in space and terrestrial concentrator photovoltaic applications. This technology represents in fact a tiny fraction of the solar market.

Crystalline silicon (blue curves in Fig.1.6) is by far the most common material for PV panels. The best conversion efficiency achieved so far is 25.6%[6]. This technology now follows an asymptotic efficiency curve, because it is in fact getting very close to its theoretical upper limit. But this is one of the cheapest technologies, and as we will see in the next section, it is based on the abundant and non-toxic silicon material. If the cell efficiency has not changed much over the past 15 years for this technology, the module efficiency has improved a lot, and the gap between best cell and module efficiencies is now reduced to $\sim$ 2%; the cost has also strongly decreased. A new technology based on thin film crystalline silicon (see downward blue triangles) is progressively catching up with the efficiency level of standard crystalline silicon; using $\sim$3-4 times less materials compared to crystalline silicon, it can potentially further reduce the cost and thus replace the standard crystalline silicon technology at some point.

Another category of solar cell technologies, based on thin film, is getting close to the 25% value; they are represented in green on this graph. Indeed they differ from crystalline silicon because they have an active material thickness roughly 100 times smaller. The champion materials in this category are CdTe and CIGS solar cells, reaching respectively 21% and 21.7% efficiency[6]. While potentially low cost, the drawback of these technologies are material scarcity and/or toxicity issues. Finally, the category of emerging PV is represented in orange; it includes organic solar cells, CZTSe, Quantum dots, etc. Most of them are very recent, and some of them have a very high efficiency progression rate (e.g. Perovskite cells). However, they are facing many issues such toxicity, light degradation, etc.

[5] B. Burger., Available online, www.ise.fraunhofer.de, 2014.
[6] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **22**: 1–9, 2014.
[7] F. Dimroth et al., Progress in Photovoltaics: Research and Applications, **22**: 277–282, 2014.

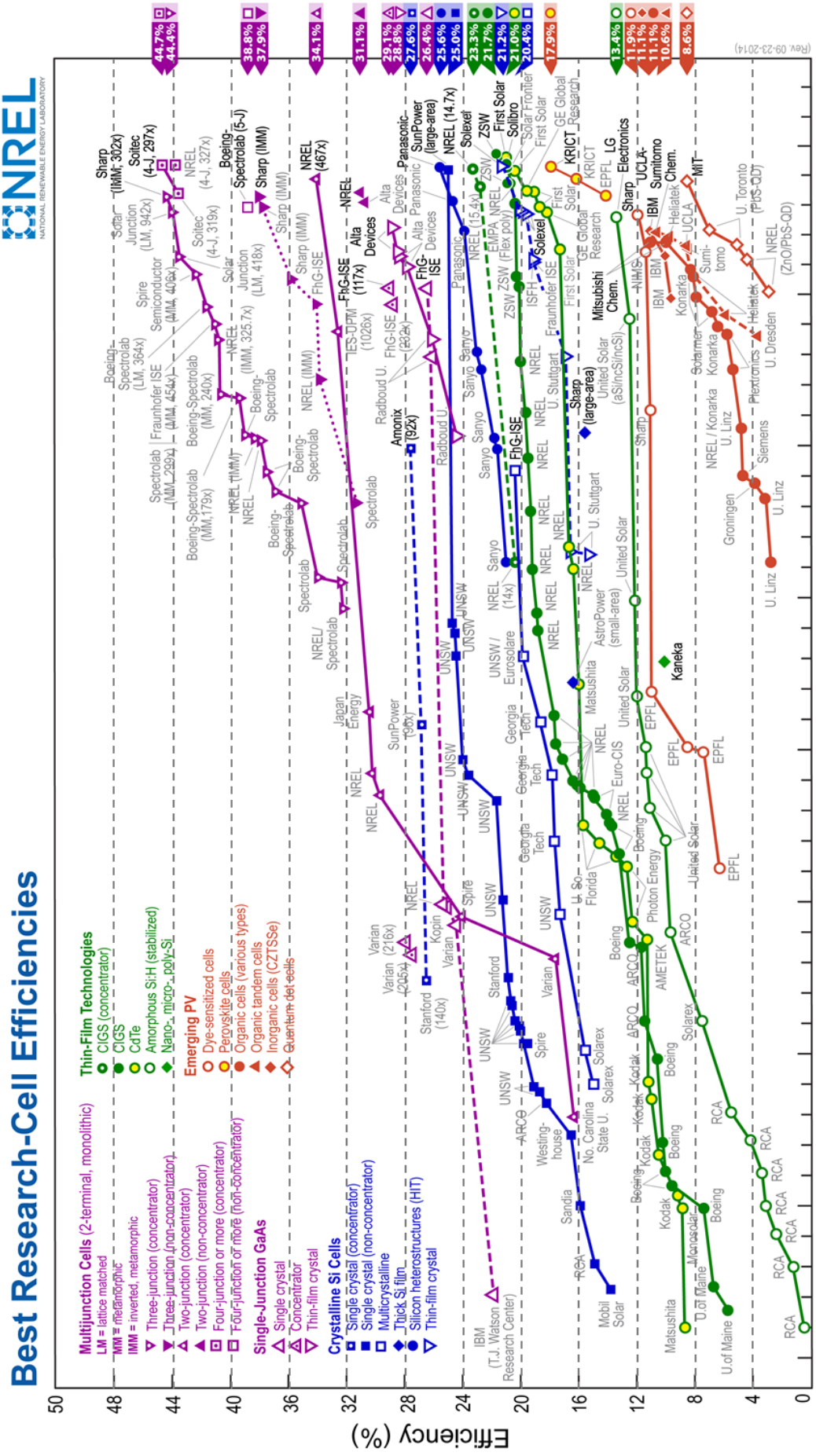


Fig. 1.6 – The yet famous NREL chart with best research cells efficiencies time evolution.

1.5 Material availability

From small size off-grid applications to industrial grid connected power plants, photovoltaics is a true multi-scale energy. Apart from specific small volume markets (space, etc.), the material availability is a crucial point in solar cell technologies. If photovoltaic energy is to become a noticeable source of electricity, then it has to reach the terawatt peak order of magnitude. As seen above several materials can be used in solar cells. In this large scale and long term production scenario, the question of chemical components abundance and ability to recycle materials by the end of product life is crucial for both economical and environmental points of view.

1.5.1 Chemical elements abundance

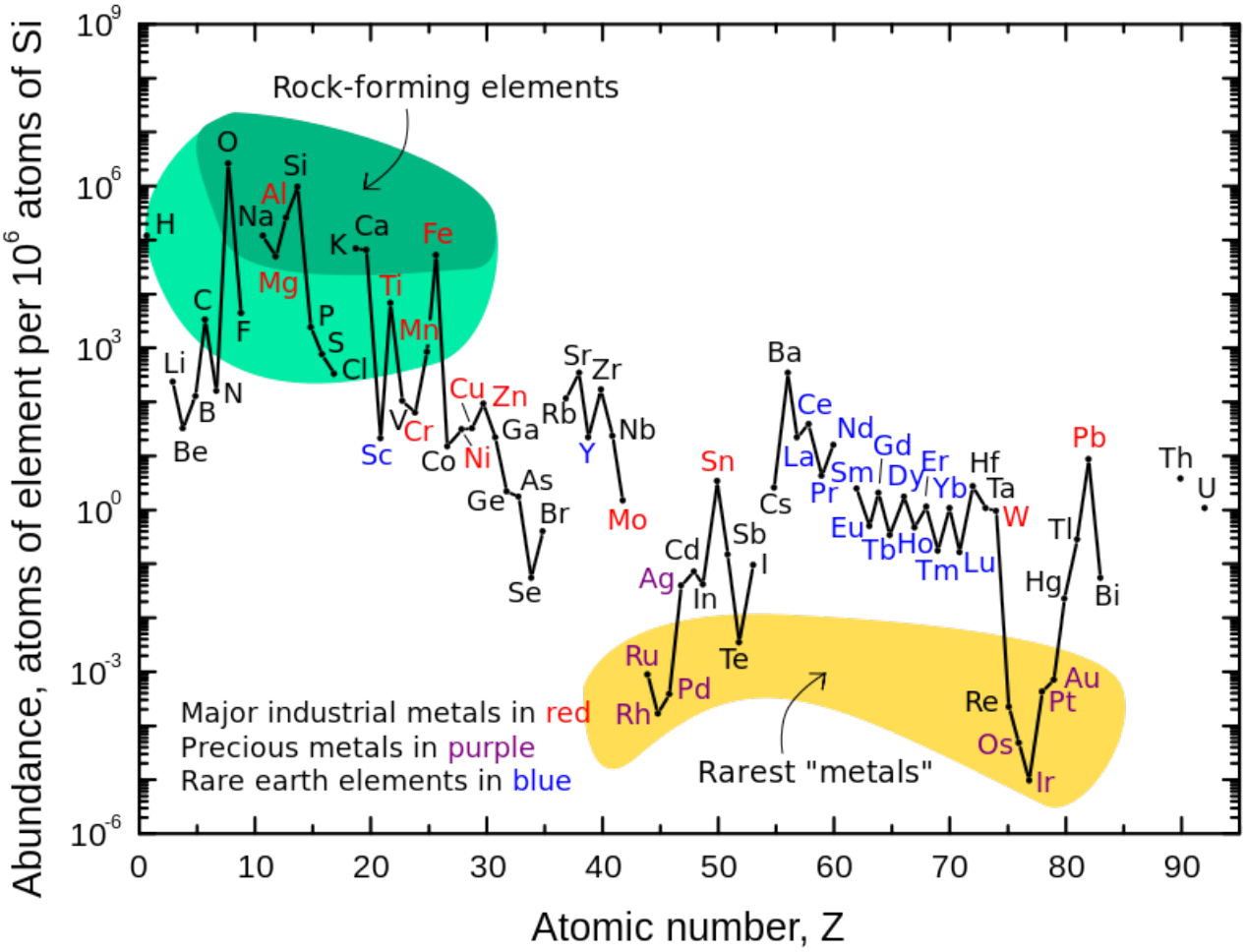


Fig. 1.7 – Abundance of chemical elements in Earth's upper continental crust as a function of atomic number. Graph from Wikipedia, data from United States Geological Survey - USGS[8].

Fig.1.7 shows chemical elements abundance, for a 10^6 silicon atoms quantity of matter, in Earth's upper continental crust as function of atomic number[8]. The Earth crust is typically composed of the 30 to 50 km outermost solid shell of our planet. Elements with small atomic number are the most abundant ones (Rock forming elements, highlighted in green), the top 8 in decreasing order, by weight %, being: O(∼47%), Si(∼28%), Al(∼8.1%), Fe, Ca, Na, K, and Mg(∼1.5%). All other components occur in small to very small quantities. Major industrial metals (Al, Mg, Fe, Ti, Mn, Cu, Zn, etc.), with a global production above 3×10^7 kg/year, are marked in red, precious metals (Au, Ag,

[8]USGS., Available online, http://minerals. usgs.gov/minerals, 2013.

Pt, Ru, etc.) in purple and so called rare earth elements in blue (Y, La, Yb, Nd, Er, etc.). This latest category is composed of siderophile elements, being depleted and relocated deeper into Earth's core, that have very little tendency to be concentrated in exploitable ore deposits in the crust. But some rare earth components (Ce, Y, Sc) can have similar crustal concentration compared to common place industrial metals (Cr, Ni, Cu, etc.), and even the least abundant ones (Tm, Lu) are roughly 200 times more common than gold for instance.

1.5.2 Estimations of maximum output power

Simple calculations, based on US Geological Survey reserve estimations[8], can give us a rough idea of material challenges for terawatt scale photovoltaic energy production. Of course, the notion of reserve is a tricky one, since it has both a physical and economical subtleties. The main uncertainty factors for reserve estimation are the proprietary nature of the data and the extraction processes of diluted elements. In, Te, Ga for instance are not mined directly but extracted as byproducts of other metals (Zn, Cu, Al) mining processes, and data for Ge reserve from non-US mining companies are hard to find. Anyhow, the point here is only to find estimations of order of magnitude for power and production rate of each main solar cell technology. Following the approach of Tao et al.[9] and Feltrin et al.[10], combined with latest values found for efficiencies, reserves, and production rates, one can try to evaluate material challenges for terawatt scale photovoltaic deployment. We choose to follow a rather simple and optimistic scenario, based on the following assumptions: - Efficiencies are taken from champion lab cells[6] - Estimations of reserves, are taken from USGS[8], and material production rate is considered as constant (see Fig.1.8-a)) - Use of chemical element by other industries is taken into account by arbitrary limiting reserve available for to 25% of the total value - Solar panel degradation over its lifetime is not considered - We use the standard AM1.5G solar spectrum with 1000 W/m^2 - Weather and day/night variation taken into account by a time averaged output power of 20%, corresponding to a daily 4.8 kWh/m^2 - And finally, given that global primary energy consumption in 2012 was roughly equivalent to 17 TW[4,11], we assume this number will reach 30 TW by 2050 and 50 TW by 2100.

- **CdTe**: Tellerium is clearly the limiting element for this technology. If we assume 2μm thick absorber and 22.10^3 tons of reserve, with 127.6 atomic mass unit (amu) the 0.6482 nm lattice constant of blende like CdTe crystalline structure, one can find a maximum wattage of 693 GWp; efficiency of 19.6% is used in this evaluation. That is roughly 139 GW of time averaged output power and thus ∼0.3% of 2100 estimated world primary energy consumption. The present tellurium production is equivalent to 2.8 GWp/year, and this would take ∼ 244 years to reach maximum CdTe solar panel volume.

- **CIGS**: A typical composition of CIGS is $CuIn_{0.7}Ga_{0.3}Se_2$. Estimated Indium reserves, 11.10^3 tons, show that it will be the limiting element by roughly a factor of 10. And thus, using the above-mentioned composition, a chalcopyrite unit cell of $0.574\times0.574\times1.125$ nm^3, 114.8 amu for indium, 2μm thick absorber and 19.8% efficiency, one can find 1.1 TWp max power, which gives 220 GW by time averaging. This latest number correspond to ∼0.4% of the 50 TW projection.

- **GaAs**: arsenic will be the limiting element, but its production clearly dwarfs the one of gallium. Recently, 28.8% was achieved by Alta Devices for lifted off GaAs solar cell under one sun[6,12]. Thus thin film GaAs can potentially enable wafer reuse: assuming 2μm thick absorber and 880.10^3 tons of As reserve, with As 74.9 amu and the 0.56533 nm lattice constant of blende like

[9] C.S. Tao et al., Solar Energy Materials and Solar Cells, **95**: 3176–3180, 2011.
[10] A. Feltrin et al., Renewable Energy, **33**: 180–185, 2008.
[6] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **22**: 1–9, 2014.
[4] BP., Available online, www.bp.com/energyoutlook, 2014.
[11] IEA., Available online, www.worldenergyoutlook.org, 2013.
[12] B.M. Kayes et al., 37th IEEE Photovoltaic Specialists Conference (PVSC), 000004 –000008, 2011.

GaAs crystalline structure, one can find a maximum wattage of 11.5 TWp. That is roughly 2.3TW of time averaged output power and thus ∼18.4% of 2100 estimated world primary energy consumption. However, with the actual gallium production, this would take ∼3000 years to reach this GaAs solar panel volume.

- **Crystalline silicon**: Being one of the most abundant element on earth, there is no risk of shortage.

The results calculated above for CdTe, CIGS, GaAs and c-Si solar cells are gathered in Fig.1.8-b).

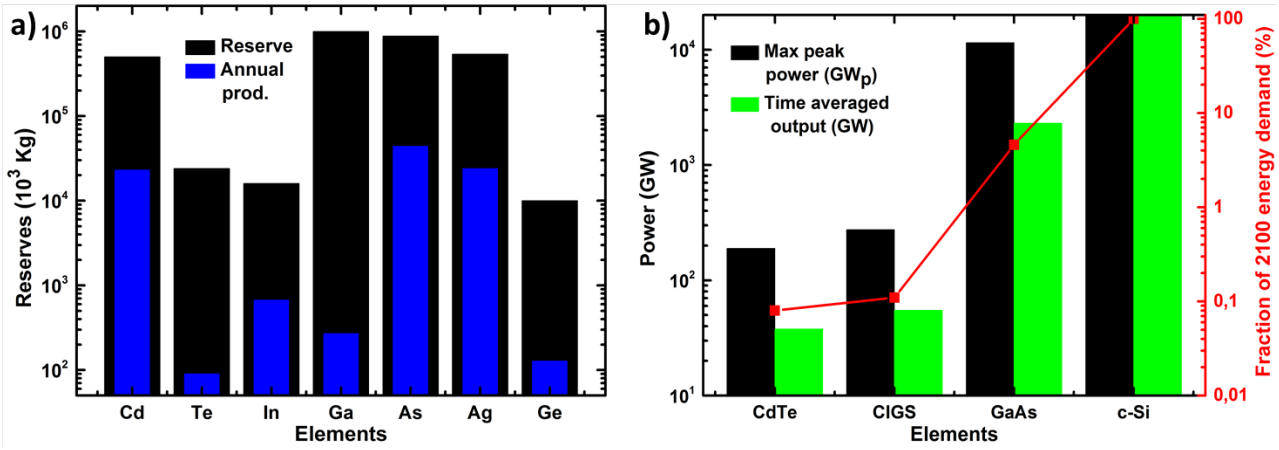


Fig. 1.8 – a) Comparison between estimated reserves and actual production for various material used in solar cells (USGS data[8]). b) Estimated maximum peak and averaged output power for various solar cell technologies, using the approach of Tao[9] and Feltrin[10]. The corresponding fraction (red curve) of the foreseen year 2100 50TW energy demand is reported on right axis.

Nevertheless, contacting metals used in solar cells such as silver are often mentioned as limiting factors. For instance, let us say we use the reserve of 540.10^3 tons of silver, with a density of $10.5 g/cm^3$, transformed in 10 μm thick contacts covering ∼10% of the cell surface area, with 25% Si energy conversion efficiency; this leads to a maximum of 12.8TWp corresponding to a time averaged 2.6 TW, that is roughly 5 percent of the 50 TW scenario of 2100. Moreover, the Actual silver production will limit this volume increase to ∼343 GWp/year.

However, recent studies tend to prove that Cu and/or Al, more abundant and less expensive materials, may be good candidates for Ag substitution: i) Pluto-passivated emitter and rear locally diffused cells (PERL) from Suntech Power company have reached more than 20% efficiency on $155cm^2$ p-type absorber with 90% copper front contact and Al back contact[13] ii) Even 20.4% efficiency was recently reported for $243cm^2$ and 40μm epitaxial lifted off Si absorber, by Solexel Company, using only Al contacts[14]. Thus, silicon solar cell technology is a credible candidate that may reach several terawatts. Considering thin film solar cells, one can see from estimation above that CIGS and CdTe have severe material limitation for terawatt scale PV. However alternative approaches have already shown promising results: 12% efficiency was reported recently by IBM[15] for solar cells with $Cu_2ZnSn(S,Se)_4$ (CZTSSe) absorbers, composed of earth-abundant and non-toxic metals. In addition, amorphous and micro-crystalline silicon are also interesting candidates. Despite their lower efficiency, in the 10 to 11% range at the module size, they can contribute nonetheless to a significant portion of the energy mix: by substituting ZnO electrodes to the commonly used indium tin oxide (ITO) and avoiding the use of silver, like for c-Si, they have no major hindrance to reach TW scale.

[13] Z. Wang et al., Progress in Photovoltaics: Research and Applications, **20**: 260–268, 2012.
[14] P. Kapur et al., 28th EU PVSEC Proceedings, **3DO.7.6**: 2228 –2231, 2013.
[15] M.T. Winkler et al., Energy & Environmental Science, **7**: 1029–1036, 2014.

1.6 Energy payback time

PV technologies produce electricity directly from the sun light, without fossil fuel consumption nor greenhouse gas emission, during its operation. It might thus seem completely clean and with no environmental impact. But one should remember that solar panel fabrication requires energy and emits greenhouse gases. The PV systems environnemental impact are in fact evaluated with life cycle assessment methods. Two indicators are commonly used: the energy payback time and the greenhouse gas emission rate. The energy payback time (EPBT) is defined as the years required for a PV system to generate the amount of energy which compensates the energy consumption over its lifetime cycle (manufacturing, assembly, transportation/installation, maintenance, recycling). The greenhouse gas emission rate quantifies the total emission divided by the amount of electricity generated, over the PV system lifetime cycle.

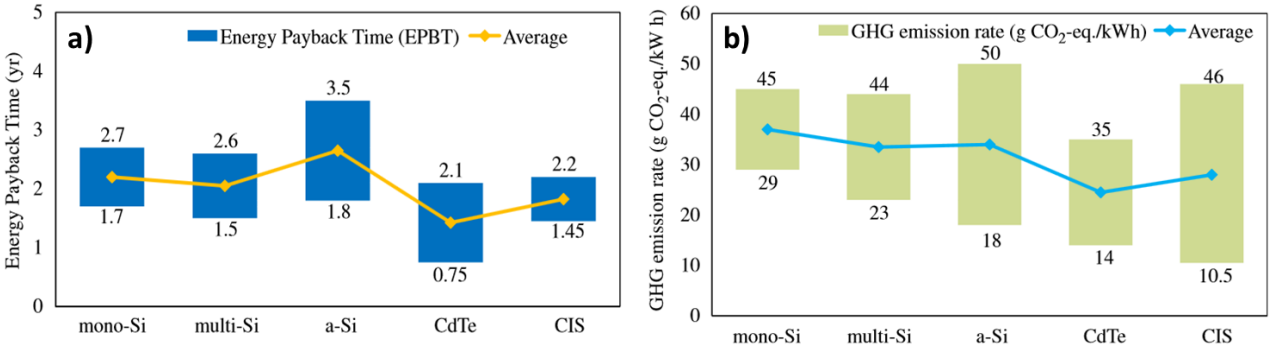


Fig. 1.9 – Energy payback times a) and b) greenhouse gas emission rates for various PV systems.[16]

As shown in Fig.1.9-a) the energy payback time of PV technologies span from 0.75 to 3.5 years[16]. This is rather small compared to lifetime of 25 to 30 years for crystalline silicon panels for instance[1]. For the greenhouse emission, PV systems are estimated to produce between 10 to 50 g CO_{2-eq}/kWh; as a comparison, this is roughly 20 times less than coal power plants. Of course, those numbers may change depending on the details of life cycle analysis process (energy sources used to produce the panel, etc.). But overall, PV appears to be an excellent strategy to produce clean energy.

1.7 Aim and outline of this PhD thesis

Within this general context of photovoltaic energy, this doctoral work is tackling issues from the nanoscale material science to the electrical characterization of solar cells. We have studied thin film deposition tools, performed several types of material analysis, and processed and characterized solar cells based on Si, Ge and GaAs chemical elements. More specifically, we focus on a new and promising way of growing monocrystalline silicon (perfectly ordered semiconductor) that can lead to low cost and high efficiency solar cells: the plasma-enhanced chemical vapor deposition (PECVD). This technique, routinely used by the industry to produce disordered semiconductor materials (a-Si:H, μc-Si:H, etc.) on large areas, is here studied for its rather unknown ability to grow monocrystalline silicon (so-called epitaxy) at low temperature, namely around 200°C. Thus, the aim of this PhD thesis is to gain some insight on the effect of the plasma parameters enabling this unusual growth process, to quantify the layers material properties deposited with this PECVD technique, and to evaluate the potential of solar cell devices based on these layers (thin film monocrystalline silicon). We have finally developed an original and innovative approach to reach high efficiency and low cost solar cells: the combination of crystalline silicon and GaAs semiconductor using the low temperature PECVD technique. The outline of this work is detailed below.

[16] J. Peng et al., Renewable and Sustainable Energy Reviews, **19**: 255–274, 2013.

[1] And like nuclear power plants, the lifetime warranty is regularly increased for solar panels.

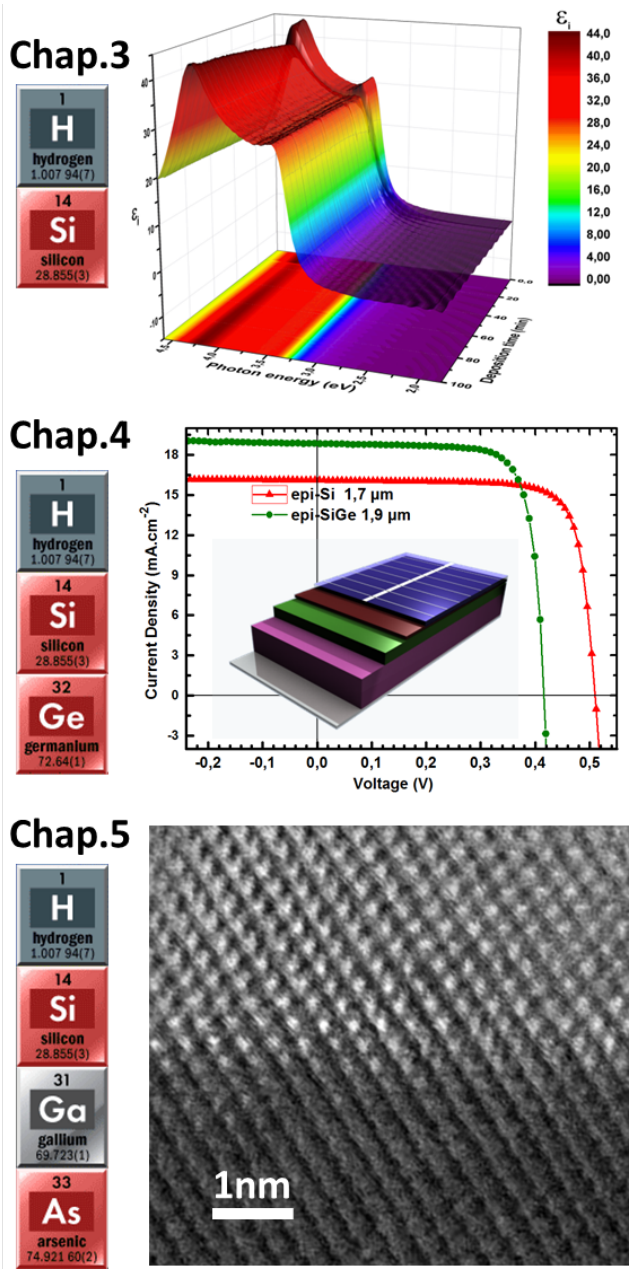


Fig. 1.10 – Thumbnails selected results from chapter 3, 4 and 5, together with the main studied chemical elements.

After this short introduction presenting the context and photovoltaic energy, we are going to focus progressively on the topic of this doctoral work. Thus, in **Chapter 2** we set the basis of the physics of solar cells and introduce the crystallographic concept of epitaxy. Having done so, the main experimental tools used in the following chapters, for semiconductors layers deposition and characterization, are presented. Then, with chapter 3, 4 and 5, illustrated in Fig.1.10, we focus respectively on the growth of mono-crystal materials at low temperature, the use of these mono-crystals as a photo-active layer in thin film solar cells, and finally their combination with III-V semiconductors for tandem photovoltaic device.

Chapter 3, *Low temperature RF-PECVD epitaxial growth*, presents a detailed study of the original growth process of silicon mono-crystal in plasma-enhanced chemical vapor deposition reactor, at temperature around 200°C. Using characterization tools such as in-situ ellipsometry, Raman spectroscopy, transmission electron microscopy, X-ray diffraction and microwave photo-conductance decay, we investigate the link between deposition parameters and crystal quality. By comparing our experimental results with literature data, we gain some insight into this unusual growth mechanism.

In **Chapter 4**, *Thin film PECVD epitaxial solar cells*, we study the possibilities to use the epitaxial layers, as described in chapter 3, to build ultra-thin (few microns thick) solar cells. Results about epitaxial cells on crystalline wafer, epitaxial lift-off of PECVD layers and epitaxial solar cells transferred on low cost substrates are presented. Additionally, we investigate strategies to increase absorption in thin crystalline layers by using photonic nanostructures and alloying silicon with germanium.

Finally, the **Chapter 5**, *Integration of Si on III-V: towards tandem devices*, focuses on the combination of III-V compounds and silicon. Our innovative approach of growing silicon on GaAs at low temperature is presented and compared with literature results in this field. We detail the performance of III-V cells and tunnel junctions fabricated during this thesis and show how they behave when exposed to a H_2 plasma. The crystal quality of low temperature PECVD epitaxial silicon on GaAs is assessed.

This doctoral work is then summarized in the conclusion section which gathers the main contributions added to the research field and perspectives.

References

[1] IPCC. Climate Change 2013: The Physical Science Basis. Contribution of Working Group I to the Fifth Assessment Report of the Intergovernmental Panel on Climate Change. *Cambridge University Press*, ISBN: 978–1–107–66182–0, 2013. (see p. 3)

[2] A. Slaoui and R.T. Collins. Advanced Inorganic Materials for Photovoltaics. *MRS Bulletin*, **32**: 211–218, 2007. doi: 10.1557/mrs2007.24 (see p. 4)

[3] REN21. Renewable energy policy network for the 21st century. *Renewables 2014 global status report*, ISBN: 978–3–9815934–2–6, 2014. (see p. 4)

[4] BP. BP Energy Outlook 2035. *Available online*, www.bp.com/energyoutlook, 2014. (see pp. 4, 5, 9)

[5] B. Burger. Electricity production from solar and wind in Germany in 2014. *Available online*, www.ise.fraunhofer.de, 2014. (see pp. 5, 6)

[6] M.A. Green, K. Emery, Y. Hishikawa, W. Warta, and E.D. Dunlop. Solar cell efficiency tables (version 43). *Progress in Photovoltaics: Research and Applications*, **22**: 1–9, 2014. doi: 10.1002/pip.2452 (see pp. 6, 9)

[7] F. Dimroth, M. Grave, P. Beutel, U. Fiedeler, C. Karcher, T.N.D. Tibbits, E. Oliva, G. Siefer, M. Schachtner, A. Wekkeli, A.W. Bett, R. Krause, M. Piccin, N. Blanc, C. Drazek, E. Guiot, B. Ghyselen, T. Salvetat, A. Tauzin, T. Signamarcheix, A. Dobrich, T. Hannappel, and K. Schwarzburg. Wafer bonded four-junction GaInP/GaAs//GaInAsP/GaInAs concentrator solar cells with 44.7% efficiency. *Progress in Photovoltaics: Research and Applications*, **22**: 277–282, 2014. doi: 10.1002/pip.2475 (see p. 6)

[8] USGS. Minerals Information: Mineral Commodity Summaries. *Available online*, http://minerals.usgs.gov/minerals, 2013. (see pp. 8–10)

[9] C.S. Tao, J. Jiang, and M. Tao. Natural resource limitations to terawatt-scale solar cells. *Solar Energy Materials and Solar Cells*, **95**: 3176–3180, 2011. doi: 10.1016/j.solmat.2011.06.013 (see pp. 9, 10)

[10] A. Feltrin and A. Freundlich. Material considerations for terawatt level deployment of photovoltaics. *Renewable Energy*, **33**: 180–185, 2008. doi: 10.1016/j.renene.2007.05.024 (see pp. 9, 10)

[11] IEA. World Energy Outlook. *Available online*, www.worldenergyoutlook.org, 2013. (see p. 9)

[12] B.M. Kayes, Hui Nie, R. Twist, S.G. Spruytte, F. Reinhardt, I.C. Kizilyalli, and G.S. Higashi. 27.6% Conversion efficiency, a new record for single-junction solar cells under 1 sun illumination. *37th IEEE Photovoltaic Specialists Conference (PVSC)*, 000004 –000008, 2011. doi: 10.1109/PVSC.2011.6185831 (see p. 9)

[13] Z. Wang, P. Han, H. Lu, H. Qian, L. Chen, Q. Meng, N. Tang, F. Gao, Y. Jiang, J. Wu, W. Wu, H. Zhu, J. Ji, Z. Shi, A. Sugianto, L. Mai, B. Hallam, and S. Wenham. Advanced PERC and PERL production cells with 20.3% record efficiency for standard commercial p-type silicon wafers. *Progress in Photovoltaics: Research and Applications*, **20**: 260–268, 2012. doi: 10.1002/pip.2178 (see p. 10)

[14] P. Kapur, M.M. Moslehi, A. Deshpande, V. Rana, J. Kramer, S. Seutter, H. Deshazer, S. Coutant, A. Calcaterra, S. Kommera, Y. Su, D. Grupp, S. Tamilmani, D. Dutton, T. Stalcup, T. Du, and M. Wingert. A Manufacturable, Non-Plated, Non-Ag Metallization Based 20.44% Efficient, 243cm2 Area, Back Contacted Solar Cell on 40μm Thick Mono-Crystalline Silicon. *28th EU PVSEC Proceedings*, **3DO.7.6**: 2228 –2231, 2013. doi: 10.4229/28thEUPVSEC2013-3DO.7.6 (see p. 10)

[15] M.T. Winkler, W. Wang, O. Gunawan, H.J. Hovel, T.K. Todorov, and D.B. Mitzi. Optical designs that improve the efficiency of $Cu_2ZnSn(S,Se)_4$ solar cells. *Energy & Environmental Science*, **7**: 1029–1036, 2014. doi: 10.1039/C3EE42541J (see p. 10)

[16] J. Peng, L. Lu, and H. Yang. Review on life cycle assessment of energy payback and greenhouse gas emission of solar photovoltaic systems. *Renewable and Sustainable Energy Reviews*, **19**: 255–274, 2013. doi: 10.1016/j.rser.2012.11.035 (see p. 11)

Chapter 2

Experimental and theoretical background

Contents

2.1 Plasma enhanced chemical vapor deposition - PECVD

Plasma is by far the most common condition of visible matter in the universe (more than 99%), both by mass and volume. Stars are made of hot and dense plasmas whereas interstellar medium are cold and tenuous. A plasma is a ionized gas with free electrically charged particles, where charge neutrality is globally respected, but not locally. Depending on the type of atoms and molecules, the ratio of ionized to neutral particles, the particle energies, etc., plasmas of different nature can be distinguished. Most of the industrial plasmas are weakly ionized and they thus contain lots of neutral species (radicals, molecules, atoms). Ions and electrons make the plasma strongly influenced by electric and magnetic fields: they behave at low frequency as a conductor and at high frequencies like dielectric medium. Both internal and external fields induce therefore strong collective behaviors of the plasma; electrons for instance are significantly more mobile than ions (due to the large mass ratio) and causes localized charge separation within the plasma.

The so called low temperature plasmas are used in industry for various applications: microelectronics, surface treatment of automotive components, aerospace and biomedical sensors, etc. Those plasmas are produced by electrical discharge through gases using power sources ranging from DC to GHz. Pressures range typically from a fraction of Pa to atmospheric pressures. At low pressure the plasma operates in the so called "glow" regime in which the plasma occupies the chamber volume as opposed to the filamentary mode generally observed at atmospheric pressure. Most of the volume is occupied by quasi-neutral plasma separated from the chamber wall by a narrow region of positive space charge, the "sheaths". In absence of thermal equilibrium, the electrical power is preferentially transferred to electrons heated to thousands of kelvins while heavy particles remain close to room temperature. Electric fields in the sheaths tend to accelerate positive ions perpendicular to the surfaces and ions bombarding surfaces are a crucial process parameter.

During this work, plasma reactors have been used as a tool for the deposition of thin film semiconductor materials. We thus give here a brief introduction to plasma-enhanced chemical vapor deposition (PECVD) as a deposition technique from a material science point of view rather than plasma physics. A more comprehensive study of plasma processes is beyond the scope of this doctoral work, but the reader can find detailed information elsewhere[1,2].

Chemical Vapor Deposition

Chemical vapor deposition (CVD) is a method to grow solids from gaseous source through chemical reactions at high temperatures. Precursor gases are introduced in the reactor where the substrates lie. Part of the precursor gases is adsorbed on the substrate, may diffuse on its surface and is eventually dissociatively chemisorbed. Reaction by-products desorb and are pumped away as well as unused precursors. Continuous pumping prevents from reaching an equilibrium between the surface and the gas phase. Thanks to the low kinetic energy of the reactants and to their possible diffusion on the surface, CVD produces conformal layers even on rough substrates. Compared to physical vapor deposition methods (e.g. sputtering), the precursors are provided by an external source, which can be changed or refilled without opening the reactor. This possibility reduces the risk of contamination and makes this method more adapted for continuous operation. The drawbacks of CVD are the large fraction of precursor gases directly pumped out without being adsorbed on the surface, and the relatively low deposition rate limited by the surface kinetics. Increasing the substrate and gases temperature is a solution to increase this deposition rate, but high temperatures are discrepant with many substrates (polymers, multi-layer substrates where different thermal expansion coefficients could lead to delamination, etc.).

Plasma-enhanced CVD

This is a method derivated from CVD where the precursor gases are partially ionized. The exci-

[1] M.A. Lieberman. *Principles of plasma discharges and materials processing.* 2nd ed Wiley-Interscience, 2005.
[2] P. Chabert. *Physics of radio-frequency plasmas.* Cambridge: Cambridge University Press, 2011.

tation energy is transferred from an oscillating voltage applied to the RF electrode. Since electron temperature is high enough for dissociation, reactive species are created at temperature where the precursor gases would not thermally dissociate; thus PECVD is carried out a substrate temperature much lower than for pure CVD (e.g. 200 instead of 1200°C). The plasma frequency, defined as the frequency of oscillations that occurs after electrons are collectively moved over an elemental distance, gives information about how the plasma will react to external electric stimulation:

$$\omega_{p,j} = \sqrt{\frac{e^2 n_j}{\epsilon_0 m_j}} \tag{2.1}$$

where n_j is the density of species j and m_j is the (effective) mass of species j. When a periodic stimulation is applied to the plasma, the charged species will be able to oscillate at the same frequency if their plasma pulsation is larger than the stimulation pulsation, otherwise species will remain at fixed positions. In a typical hydrogen RF plasma where $n_e = n_i = 10^{10}\ cm^{-3}$, $f_e \sim$ 900MHz and $f_{H^+} \sim$ 2MHz : this means that electrons can react very fast to the RF excitation (13.56MHz) and follow its oscillations, while H+ ions cannot. This difference partly explains one of the fundamental properties of low-temperature plasmas: electrons (temperature around 5eV) are not in thermal equilibrium with ions (temperature about 40meV).

Fig. 2.1 – Pictures of some PECVD reactors: ARCAM the 30 years old home-built reactor[3], ARCAM 200, the automated reactor installed in Thales TRT clean room and the Total/LPICM cluster tool.

Pictures of some PECVD reactors facilities are shown in Fig.2.1. On the left is shown ARCAM[3], the thirty years old home-built set-up which was extensively used during this PhD. ARCAM 200, in the middle, is a more recent and automated version of PECVD reactor, with similar geometry compared to ARCAM, and installed in Thales TRT clean room. The picture on the right hand side is a PECVD cluster with 6 plasma chambers, 1 sputtering and 1 vacuum characterization chamber. This cluster tool, purchased by Total and shared with LPICM, was extensively used towards the end of this PhD: after transferring deposition recipes from ARCAM reactor, we could benefit from its better vacuum quality and in-situ optical characterization tool (ellipsometry).

The process pressure used in this PhD thesis were in the range of 50-2500 mTorr, corresponding to a mean free path between few μm and hundreds of μm. The excitation frequency of power supply was the usual RF 13.56MHz; this value was chosen by international communication standard as an unoccupied frequency. The above mentioned PECVD reactor were all capacitively coupled systems: they consist of two metal electrodes separated by few cm, one being connected to the RF generator through a matching box (to minimize reflected power), and the other one being grounded. The plasma is ignited between the two electrodes, and the sheath arises at the electrodes interfaces. Indeed, because electrons are much lighter than ions, there will be a deficit of electrons near the surfaces and therefore accumulation of positive charges. The resulting potential shape across the electrodes is shown in Fig.2.2-a).

[3]P. Roca i Cabarrocas., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, **9**: 2331, 1991.

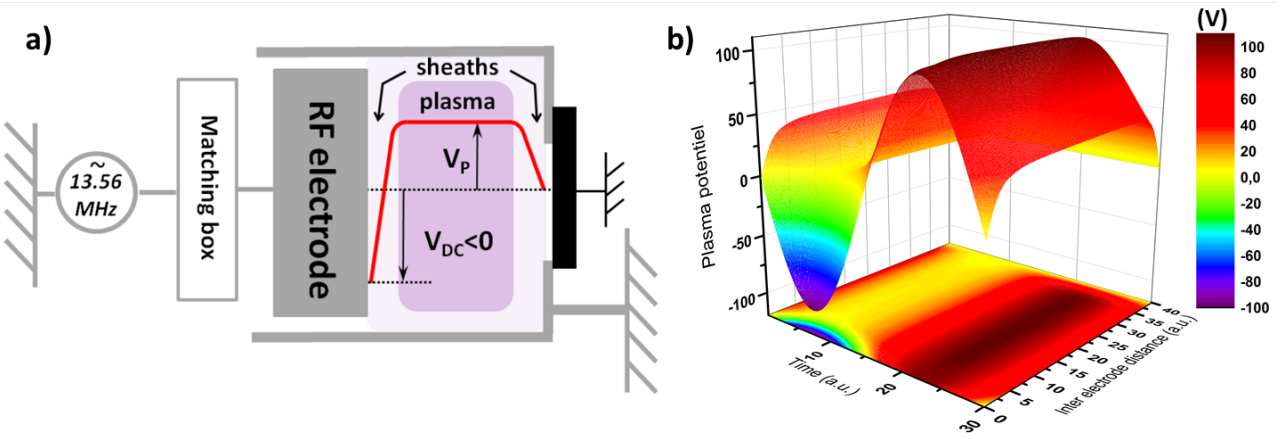


Fig. 2.2 – a) Schematic of potential distribution across the plasma between a RF and a ground electrode[4]. b) Simulation of RF plasma potential evolution during one period between a grounded and an RF electrode. From B. Bruneau.

If the area of the grounded electrode is larger than the one of the RF (as it is the case in ARCAM and in Fig.2.2-a)) the discharge becomes asymmetric and makes RF electrode negatively charged. This behavior is called self-bias or DC bias (V_{dc}). The empirical relation between the electrodes areas and theirs voltage drops is: $V_{RF}/V_{GR} = (A_{RF}/A_{GR})^q$ with q being close to 5/2[1]. Thus for reactors with symmetric electrodes, this self bias is roughly zero. The details of the plasma potential between two electrodes and during one period is shown in Fig.2.2-b) in the symmetrical case. One can see that the time averaged potential is zero on the RF electrode and has a positive value for the plasma bulk. To estimate the value of the plasma potential from the measurement of the RF-excitation peak to peak voltage, one can use the following expression:

$$V_{pl} = 1/2(V_{pp}/2 + V_{dc}) \tag{2.2}$$

As mentioned previously, the plasma is a partly ionized mix of gases. Three kinds of species are present in the plasma: electrons, ions and neutrals. Neutrals can be either stable molecules (like SiH_4) and radicals (like SiH_3). Neutrals and positive ions can take part in the deposition, whereas negative ions are trapped in the bulk of the plasma due to the repulsive forces arising from the sheaths. In deposition plasmas, a huge amount of different chemical reactions can happen. They can be classified in primary and secondary reactions. Primary reactions occur between electrons and neutrals : they create ions or radicals. In the case of SiH_4/H_2 plasmas, the products of reactions are H^+ and Si_yH_x $(0 \leq x \leq 6)$, $(1 \leq y \leq 2)$. These species can react either with the substrate, leading to deposition or etching on the surface, or with themselves and electrons. The latter reactions are called secondary reactions. They lead to the re-formation of precursor gases or to polysilanes. This kind of reactions can eventually produce silicon nano-clusters and even powders in the bulk of the plasma.

ARCAM is central to PICM's activities: it is one of its oldest operating reactors but it is almost continuously running. Fig.2.3 shows some pictures of it; its specific properties are the following:

- It is an "oven-like" reactor: completely heated by thermocoax cables embedded in its walls, this allows the temperature to be homogeneous. The typical operating temperatures are in the range 150°C to 250°C.

- Substrates (up to 4 inch wide) lie face down on a rotating plate which bears six substrate holders. This way, several substrates can be treated in a single pump-down process. In addition, the plasma can be started in front of an empty substrate holder and the substrate to be treated can be moved once the plasma is stable. This feature prevents the samples from being exposed to the plasma transitions (a few seconds), which are a major cause of non-reproducibility.

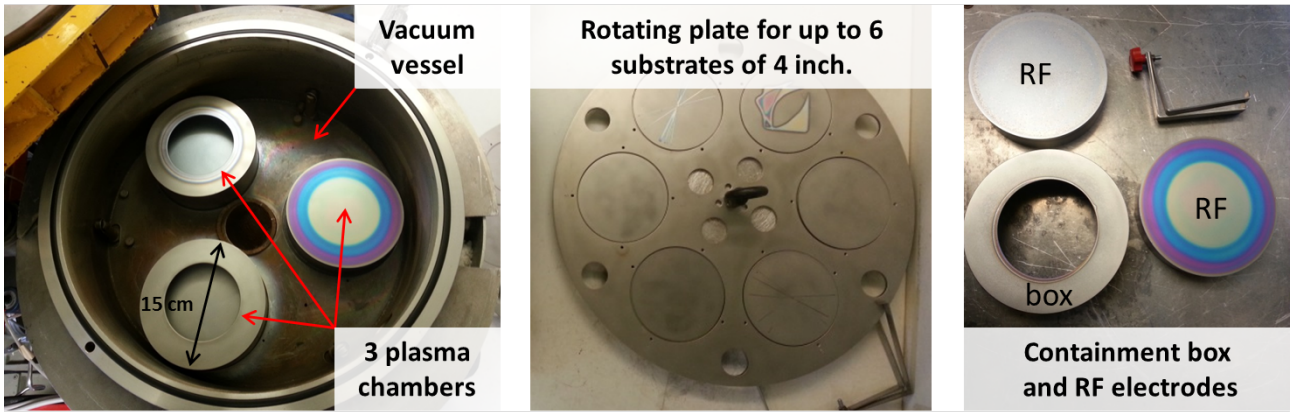


Fig. 2.3 – From left to right: picture of opened ARCAM reactor with the 3 plasma chambers visible, grounded rotating plate with 6×4 inch substrate holders, RF electrode and plasma box.

- It has three RF electrodes, each of them being in a separate plasma box. The plasma boxes allow insulating the plasma and prevent cross-contamination. Each of them is dedicated to one kind of deposition: intrinsic materials, n-doped materials, and p-doped and carbide materials, respectively. In association with the rotating plate, this feature allows fabricating multi-layers structures like PIN cells in a single run and with clean interfaces.

ARCAM has been used in this work, mainly for the deposition of epitaxial layers and N or P-type amorphous layer. It is operated at a base pressure of 1×10^{-6} mbar. Available gases include Ar, SiH_4, H_2, PH_3 (for n doping), $(CH_3)_3B$ (for p doping), SiF_4, GeH_4. The inter-electrode distance d is between 12mm and 28mm.

2.2 Crystalline silicon and epitaxial growth

Solids are characterized by an extended three-dimensional arrangement of atoms, ions, or molecules in which the components are generally in a fixed position. The components can be arranged in a regular repeating three-dimensional array -a crystal lattice- which results in a crystalline solid (ordered structure over a macroscopic scale), or randomly to produce an amorphous solid (structural order over few atoms max.). All the intermediate state between this two extremes are possible. This 3D atomic configuration determines the solid material and electrical properties: i) crystalline solids tends to have sharp edges and faces. ii) Crystalline solids have well-defined physical properties in contrast to amorphous (e.g. melting point). iii) Semiconductor crystals have a precise band gap energy whereas amorphous features band tails and defect states within the gap.

Silicon, like carbon and germanium, crystallizes in a diamond cubic crystal structure: each of its atoms is tetrahedrally bonded to the other four neighboring ones, with a lattice spacing of 5.43 Å at room temperature. The arrangement of silicon atoms in a unit cell of crystalline silicon is presented in Fig.2.4-a): it corresponds to two interpenetrating face-centered cubic primitive lattices. The bulk arrangement of the atoms in the crystal is obtained by stacking this unit cell in the three dimensions. The network of silicon atoms in the crystal is represented in Fig.2.4-b) where the red lines highlight one cubic unit cell. The effect of the periodic arrangement of atoms on electron energy levels is shown in Fig.2.4-c). Isolated atoms have quantified energy levels, but when 2 identical atoms are brought together, the electron wave functions begin to overlap and the quantized energy levels hybridize and split into different levels. Due to Pauli exclusion principle, the discrete energy levels of individual atoms split into bands belonging to the pair instead of to individual atoms. Thus in the case of a crystal, when a large number of atoms are brought together at the inter-atomic equilibrium distance of the crystal, the energy levels are split into a large number of levels which eventually form continuous energy bands. For crystalline silicon, this process is responsible for the formation of the valence and the

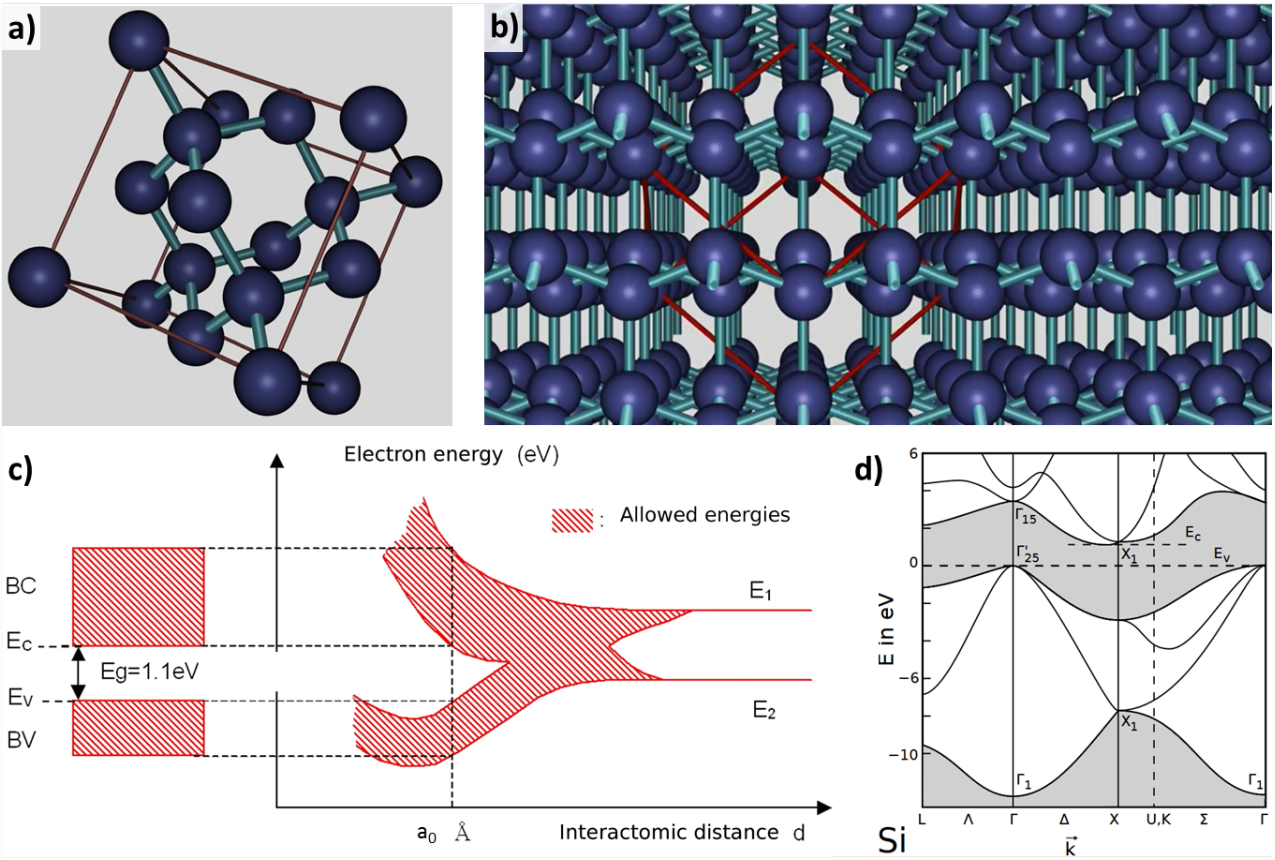


Fig. 2.4 – a) Unit cell of crystalline silicon with diamond cubic structure represented with the stick model. b) Extended crystalline silicon network with the unit cell highlighted in red. From homofaciens. c) Splitting of individual energy levels to energy bands as atoms are brought closer together. From optique-ingenieur. d) Schematics of calculated band structure of crystalline Si[5]. From Wikipedia.

conduction band separated by an energy gap of 1.12 eV at room temperature, as shown in Fig.2.4-c). The electrons wave function in the crystal periodic potential is described by Bloch wave; the complete silicon band structure[5] is shown in Fig.2.4-d) (see solid state physics books[6,7] for further details).

Such thin film monocrystalline materials can be produced by **epitaxy**. Epitaxy is a word derived from the Greek, $\varepsilon\pi\iota$ (epi - placed or resting upon) and $\tau\alpha\xi\iota\zeta$ (taxis - arrangement), which describes the extended single crystal formation on top of a crystalline substrate. It seems that this word was introduced in 1928 by the french mineralogist L. Royer[8]. Two types of epitaxial growth are distinguished: i) the homoepitaxial growth in which the layer is the same as the crystalline substrate and ii) the heteroepitaxial growth, which refers to film and substrates composed of different materials. It may seem useless to extend the crystalline substrate by homoepitaxial growth, but this is actually extremely useful since the epi-layer can have a superior crystalline quality and purity compared to the substrate, and it can also be doped independently; the early dramatic improvement in the yield of transistors was the consequence of the homoepitaxy process. Heteroepitaxy is also routinely used for optoelectronic devices such as lasers or LEDs, and often involves III-V semiconductor compounds. Unlike homoepitaxial growth, heteroepitaxy involves semiconductors with different lattice parameters, and thus different scenarios are possible depending on the lattice mismatch. If the lattice mismatch

[5] J.R. Chelikowsky et al., Physical Review B, **10**: 5095–5107, 1974.
[6] N.W. Ashcroft et al. *Physique des solides*. EDP sciences, 2002.
[7] C. Kittel. *Introduction to solid state physics*. 8th ed Wiley, 2005.
[8] L. Royer., Société française de minéralogie et de cristallographie, **51**: 7–159, 1928.

is very small (e.g. $\sim 0.1\%$ for GaAs and Ge) then the growth is nearly identical to the homoepitaxial case; however differences in polarity or thermal expansion coefficient may create interfacial and bulk defects in the film. If the epitaxial film has a bigger (alternatively smaller) lattice parameter compared to the substrate, then the layer may grow under in plane biaxial compressive (alternatively tensile) strain: the epi-layer lattice deformation results in a bigger (smaller) lattice parameter in the growth direction. This is illustrated on the two left schematics in Fig.2.5-a)[9]. The epi-layer growing in such fully strained configuration corresponds to a so-called pseudomorphic growth. However, after some critical thickness $\boldsymbol{d_c}$ the layer relaxes into a more stable configuration: as shown in Fig.2.5-a), the creation of crystalline defects such as edge dislocations allows the two lattices to accommodate their crystallographic differences. This latter case is called metamorphic growth; there is a huge quantity of scientific papers dealing with metamorphic growth and strategies to minimize crystalline defects and their impact on epitaxial layer electrical properties.

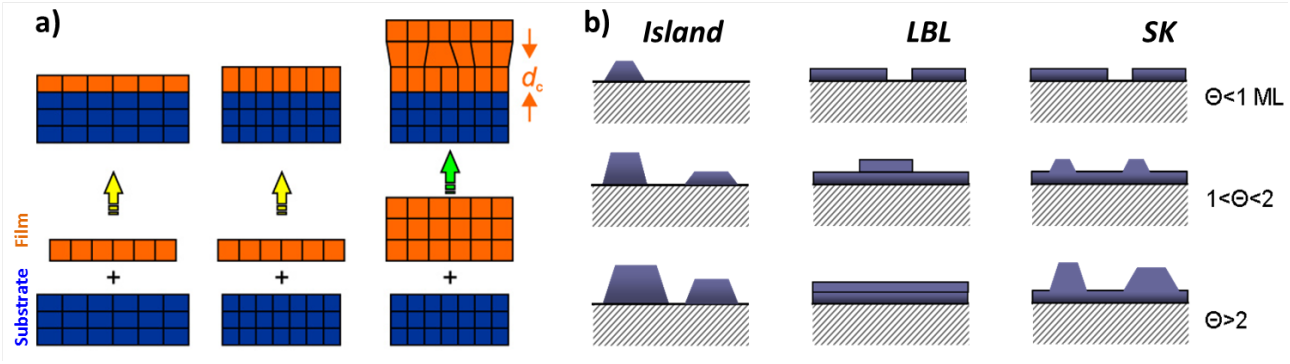


Fig. 2.5 – a) Schematic illustration of hetero-epitaxial growth, from left to right: strained tensile, strained compressive and relaxed epitaxial films[9]. b) Schematics of cross section epitaxial growth mode: from left to right Volmer-Weber (island formation), layer-by-layer and Stranski-Krastanov (layer plus island). From Wikipedia.

Three epitaxial growth mechanisms can be distinguished depending on lattice parameters and interactions strength between adatoms and the surface (chemical potential)[10]; the three modes are represented in Fig.2.5-b). In the Volmer-Weber (VW) growth, adatom-adatom interactions are stronger than those of the adatoms with the surface, thus resulting in the formation of three-dimensional adatom clusters or islands. The second possible growth mechanism is the layer-by-layer growth (Frank-van der Merwe), adatoms attach preferentially to surface step sites resulting in atomically smooth, fully formed layers; this is a 2D growth, in which complete layers form prior to growth of subsequent layers. The third mechanism correspond to the so-called Stranski-Krastanov growth: it is a combination of 2D layer-by-layer growth over a certain thickness above which 3D island growth dominates. The critical layer thickness for the transition is highly dependent on the chemical and physical properties, such as surface energies and lattice parameters, of the substrate and film. Epitaxial growth can be achieved from vapor, liquid or solid phase precusors. The common epitaxial processes are chemical vapor deposition and molecular beam epitaxy; they involve high temperatures and/or ultra high vacuum. The specific PECVD epitaxial growth presented in this manuscript involves neither ultra-high vacuum nor high temperatures. More information about silicon epitaxial growth physical mechanism and technological processes can be found in the following books[11,12].

[9] M. Opel., Journal of Physics D: Applied Physics, **45**: 033001, 2012.
[10] K. Oura, ed. *Surface science: an introduction*. Advanced texts in physics Springer, 2003.
[11] D. Crippa et al. *Silicon epitaxy*. Academic Press, 2001.
[12] B.J. Baliga, ed. *Epitaxial silicon technology*. Academic Press, 1986.

2.3 Crystalline silicon characterizations

Characterizations of thin film mono-crystals, both in-situ during the growth process and ex-situ after deposition, are of foremost importance. To monitor the growth in real-time, in ultra high vacuum environment, surface sensitive electron diffraction techniques such as LEED or RHEED are used. The RHEED technique, reflection high-energy electron diffraction, is based on diffraction of electrons of few tens of keV in grazing incidence, whereas LEED uses electrons of few tens of eV. Post-deposition characterizations of crystalline films are often performed by TEM and XRD. TEM, transmission electron microscopy, is a microscopy technique in which a beam of electrons is transmitted through an ultra-thin specimen, interacting with the sample as it passes through. An image is formed from the interaction of the electrons transmitted through the sample; TEMs are capable of imaging at a significantly higher resolution than light microscopes, owing to the small de Broglie wavelength of electrons[13]. XRD, X-ray diffraction, is also a powerful technique since it is a non destructive technique sampling a macroscopic area/volume of the sample. The crystalline atoms cause a beam of incident X-rays to diffract into many specific directions. By measuring the angles and intensities of these diffracted beams, it is possible to produce a three-dimensional picture of the density of electrons within the crystal; thus the mean positions of the atoms in the crystal can be determined, as well as their chemical bonds, their disorder and various other information[14,15]. During this doctoral work, both TEM and XRD have been used; however in this section we will not present them in details, but rather discuss about two other characterization techniques: ellipsometry and Raman spectroscopy. While being less precise compared to TEM and XRD, they are nonetheless fast characterization techniques and offer valuable information which, as we will see in this manuscript, correlates with TEM and XRD results. In addition, ellipsometry enables to monitor in-situ growth in non-ultra high vacuum environment.

2.3.1 Ellipsometry

Ellipsometry is a technique of surface analysis based on the changes in the state of polarization of light after reflection on the sample, which has been developed with the growing market of microelectronics. It can measure optical constants of materials, thicknesses of thin films, roughness, monitor in situ growing layer, etc.

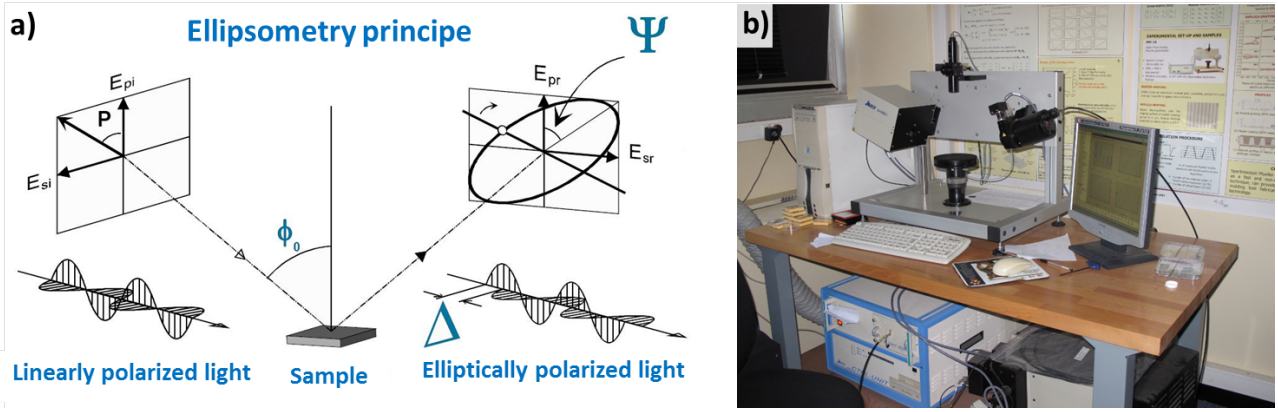


Fig. 2.6 – a) Schematic of ellipsometry principle and b) picture of the ex-situ experimental set-up at LPICM.

The principle of the ellipsometry is the following: an electromagnetic radiation is emitted by a light source, linearly polarized by a polarizer, and then falls onto the sample. After reflection the

[13] D.B. Williams et al. *Transmission electron microscopy: a textbook for materials science.* Springer, 2009.
[14] B.D. Cullity et al. *Elements of x-ray diffraction.* Prentice Hall, 2001.
[15] Y. Waseda. *X-Ray diffraction crystallography: introduction, examples and solved problems.* Springer, 2011.

radiation passes a second polarizer, which is called analyzer, before reaching the detector (see Fig.2.6-a)). Thus it is a specular optical technique which measures the change of polarization upon reflection or transmission. The incident and the reflected beam span the plane of incidence, and the light polarized parallel to this plane is named p-polarized, whereas a polarization direction perpendicular is called s-polarized. The complex reflection coefficients at air-surface interface, or Fresnel equations, are defined as:

$$\underline{r}_p = \frac{\underline{E}_p^r}{\underline{E}_p^i} = \frac{|\underline{E}_p^r|}{|\underline{E}_p^i|} e^{i(\varphi_p^r - \varphi_p^i)} = |\underline{r}_p| e^{i\delta_p} \quad \textit{and} \quad \underline{r}_s = \frac{\underline{E}_s^r}{\underline{E}_s^i} = \frac{|\underline{E}_s^r|}{|\underline{E}_s^i|} e^{i(\varphi_s^r - \varphi_s^i)} = |\underline{r}_s| e^{i\delta_s} \tag{2.3}$$

where the modules $|\underline{r}_p|$ and $|\underline{r}_s|$ stand for the amplitude attenuation and the arguments $\boldsymbol{\delta_p}$ et $\boldsymbol{\delta_s}$ represent the absolute phase change due to reflection. The change in polarization is characterized by the ratio : $\underline{\rho} = \frac{\underline{r}_p}{\underline{r}_s} = \frac{|\underline{E}_p^r|}{|\underline{E}_p^i|} \frac{|\underline{E}_s^i|}{|\underline{E}_s^r|} e^{i(\delta_p - \delta_s)}$ that can be written as :

$$\underline{\rho} = tan\Psi\, e^{i\Delta} \tag{2.4}$$

with $\mathbf{\tan \Psi} = \left|\frac{\underline{r}_p}{\underline{r}_s}\right|$ which represents the module ratio and $\boldsymbol{\Delta} = \boldsymbol{\delta_p} - \boldsymbol{\delta_s}$ the phase difference. Knowing the absolute phases and amplitudes is not necessary, that makes the measurement independent of any fluctuations of the source[16].

The **Pseudo-dielectric function** $\langle \epsilon \rangle$ is obtained from the ellipsometric angles ($\boldsymbol{\Psi}$ & $\boldsymbol{\Delta}$) and the optical model of a perfectly flat sample with infinite thickness. The formula for calculating the pseudo-dielectric function is as follows:

$$\langle \epsilon \rangle = \sin \theta_i^2 \left[1 + \tan \theta_i^2 \left(\frac{1-\rho}{1+\rho} \right)^2 \right] \tag{2.5}$$

in which $\boldsymbol{\rho = \tan \Psi\ \exp(i\Delta)}$ and $\boldsymbol{\theta_i}$ represent the incident angle. The pseudo-dielectric function is equal to the dielectric function if the roughness of the surface is zero. According to the definition of the complex index of materials, $\boldsymbol{N = n + ik}$, the pseudo dielectric function is divided into real and imaginary parts: $\langle \epsilon \rangle = \langle \epsilon_r \rangle + i \langle \epsilon_i \rangle$.

During this doctoral work both ex-situ Horiba Jobin Yvon ellipsometer and in-situ Woollam set-up were used to determine the layer thickness and composition. This was done via some modeling: we have used multilayer descriptions where the model inputs are the thickness, the composition and the dielectric function of each material entering in the composition of the layers. The outputs were the same except that we could ask to fit or not the dielectric function of the materials. The choice of the input dielectric function of the materials used in the model can be taken from a library containing the dielectric functions of materials of interest[16], or described by dispersion laws (generally a Tauc-Lorentz). Even more interesting, is the fact that layers can be modeled using the Bruggeman Effective Medium Approximation[17] (BEMA) which states that new dielectric function can be defined ($\boldsymbol{\epsilon_h}$) for a material from the combination of the dielectric functions of the different materials that constitute this layer, by using the formula:

$$\mathbf{0} = \sum_j \boldsymbol{f_j} \frac{\boldsymbol{\epsilon_j - \epsilon_h}}{\boldsymbol{\epsilon_j + 2\epsilon_h}} \tag{2.6}$$

where $\boldsymbol{\epsilon_j}$ is the dielectric function of the material j with a fraction $\boldsymbol{f_j}$ and $\boldsymbol{\epsilon_h}$ is the effective medium dielectric function. This BEMA is mostly used when one wants to model microcrystalline films or interfacial films.

[16] D.E. Aspnes et al., Physical Review B, **27**: 985, 1983.
[17] D.A.G. Bruggeman., Annalen der Physik, **416**: 636–664, 1935.

In Fig.2.7, we have represented the modeled imaginary part of the pseudo-dielectric ε_i for various epi-Si layer stacks, using the BEMA approximation. Fig.2.7-a) shows ε_i for 500nm epi-si layers on c-Si wafer, with a 2nm interface layer composed of: 10 (squares), 30 (circles) and 50% (triangles) of void. The inset zoom on the low energy part of the spectrum, where a net increasing of oscillations amplitude is detected as the void fraction increased. Thus ellipsometry is sensitive to the wafer interface layer composition, and as we will see further in this manuscript, this interface layer is a key point for lifting-off epitaxial layers. Fig.2.7-b) shows the influence of surface SiO_2 layer on ε_i: the layer stack modeled here is composed of 500nm c-Si layer, grown on c-Si wafer with a 2nm/10% void interface layer. Three spectra are compared: one corresponding to the bare c-Si surface (squares), one with 1 nm SiO_2 layer (circles) and one with 2 nm SiO_2 layer (triangles). A strong decrease of the 4.2 eV ε_i amplitude peak is visible with increasing surface oxide thickness. Consequently, as presented in the next chapter, this 4.2 eV peak amplitude will be very useful to monitor in-situ silicon native oxide etching prior to epitaxial growth. Finally, 2.7-b) shows ε_i spectrum of 1 μm thick layers composed of a mix between c-Si and a-Si:H. With increasing a-Si:H fraction, a net decrease of 3.4 and 4.2 eV ε_i peak amplitude is detected, as well as an increase in the 2-3 eV range. ε_i for the fully amorphous layer has a characteristic large hill shape; all the intermediate compositions exhibit distinct spectrum shape. Thus by fitting, a broad range of material from pure c-Si to microcrystalline and fully amorphous layers can be detected; this enables to quantify the layer crystal quality and detect some potential epi-breakdown (during in-situ measurement).

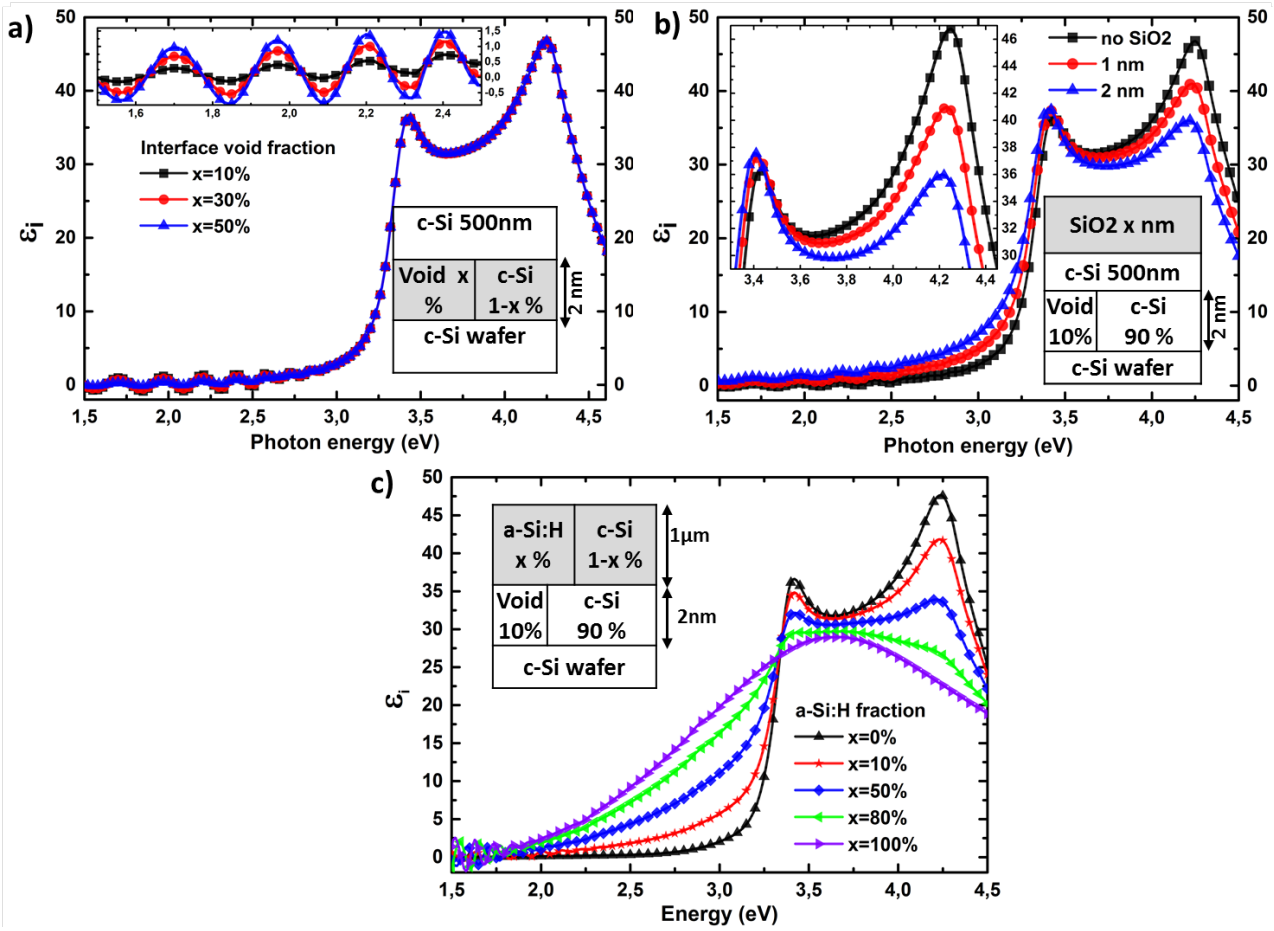


Fig. 2.7 – Imaginary part of the pseudo-dielectric ε_i for various epi-Si films on c-Si wafer as modeled using the HJY DeltaPsi software: a) 500nm epi-Si above 2nm interface layer with 10, 30, 50% void fraction. b) 500 nm c-Si on wafer with 2nm 10% porous interface, covered by 0, 1 and 2 nm of SiO_2. c) 1 μm c-Si on wafer, with an increasing amorphous fraction: 0, 10, 50, 80 and 100%.

2.3.2 Raman

Raman spectroscopy (named after Sir C.V. Raman) is a spectroscopic technique used to observe vibrational, rotational, phonons and other low-frequency modes in a system. It relies on inelastic scattering of monochromatic light, usually from a laser in the visible, near infrared, or near ultraviolet range. The laser light interacts with the atoms and this results in the system being in a so-called virtual energy state for a short period of time before an inelastically scattered photon is emitted. This scattered photon can be either of higher (anti-Stokes) or lower (Stokes) energy than the incoming photon. The difference in energy between the original state and this resulting state after inelastic scattering leads to a shift in the emitted photon's frequency away from the excitation wavelength, the so-called Rayleigh line. This principle is represented in Fig.2.8 schematic on the left hand side. Spontaneous Raman inelastic scattering is typically very weak (scattering cross section in the range of 10^{-28}-10^{-31} cm^2/sr !), and as a result the main difficulty of Raman spectroscopy is separating the weak scattered light from the intense Rayleigh laser light. From the Raman signal, one can extract chemical and structural composition, as well as strain state of the layer: the Raman line peak position is related to species identification, the full width at half maximum (FWHM) is related to lattice disorder and the shift with respect to reference position is linked to the train state of the layer and to temperature variations. To illustrate this point, the Raman spectrum of crystalline silicon, amorphous silicon and partially crystallized silicon layers are displayed in Fig.2.8, on the right hand side. c-Si exhibits a sharp peak centered at 520 cm^{-1} (with typical FWHM of 4-5 cm^{-1}), and with increasing a-Si:H content this peak broadens and decreases while the broad shoulder of amorphous centered at 480 cm^{-1} becomes more and more pronounced. For cubic crystals (Si, Ge, etc.), in normal back scattering configuration, only the third phonon (LO) is observable. More details about Raman theoretical background and its application for stress measurements can be found in the paper of I. De Wolf[18].

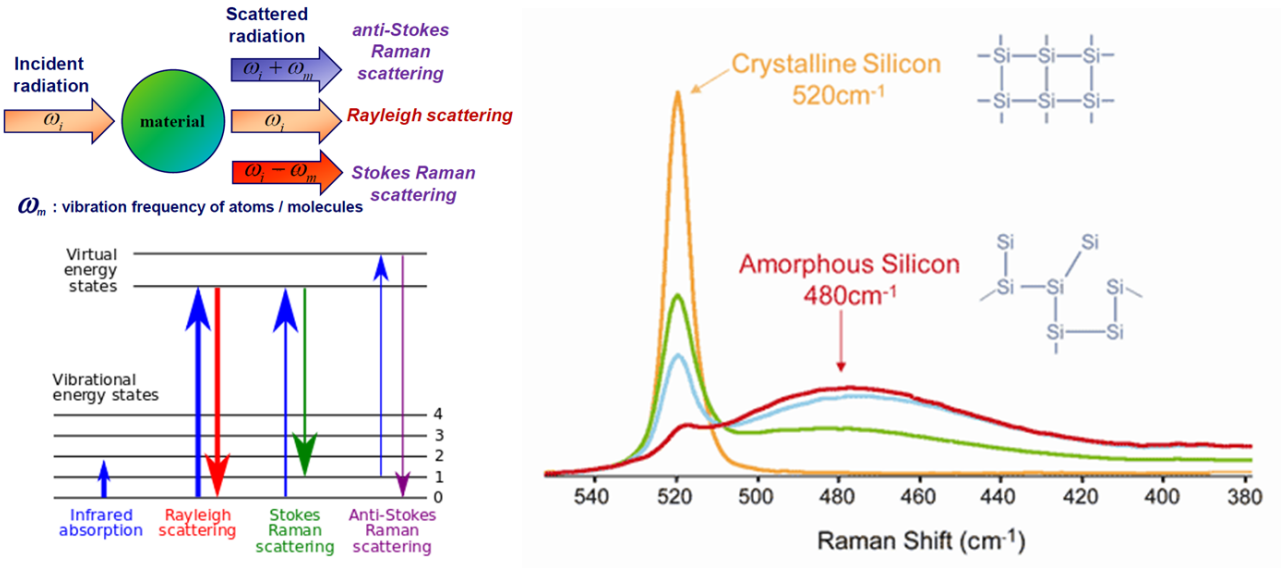


Fig. 2.8 – Left: principle of Raman spectroscopy and right Raman spectra of silicon sample with various crystallinity. From semrock.

Raman spectroscopy is thus very useful for the characterization of epitaxial layers, especially because it gives complementary information compared to ellipsometry. This is illustrated in Fig.2.9-a,b) where we present both ε_i and the Raman spectra of three epitaxial samples. Those samples are epitaxial silicon with similar thicknesses, grown on c-si wafer, but they have undergone different

[18] I.D. Wolf., Semiconductor Science and Technology, **11**: 139–154, 1996.

wafer interface treatments prior to epitaxy (namely a different H_2 plasma exposure times). From the ellipsometry curves, very few differences are noticeable: the ε_i peak amplitude are the same, and the small differences in oscillations period and amplitude visible are related to the layer thickness and interface composition. However if we look at Raman spectra acquired on the same samples (see Fig.2.9-b)) the difference is much more pronounced. As a matter of fact, the three samples have all sharp peaks with FWHM of 5 to 5.5 cm^{-1}, but the peak position is about 519, 520 and 523 cm^{-1} respectively. This peak shift is related to the stress in the layer. Thus Raman spectrum is very efficient for detecting stress, whereas this quantity cannot be detected by ellipsometry. Another example of Raman spectroscopy application is shown in Fig.2.9-c). This graph displays the Raman spectra measured on three epitaxial silicon layers grown on GaAs substrate with different crystal quality. While the peak position is the same, the peak full width at half maximum is changing from 8.5 cm^{-1} for the best sample to 12.5 cm^{-1} for the less crystalline. Both ellipsometry and Raman enables to quantify the crystal quality of the layer; but with Raman spectroscopy it is additionally possible to measure the strain state of the layer. These points will be further discussed in chapters 3 and 5.

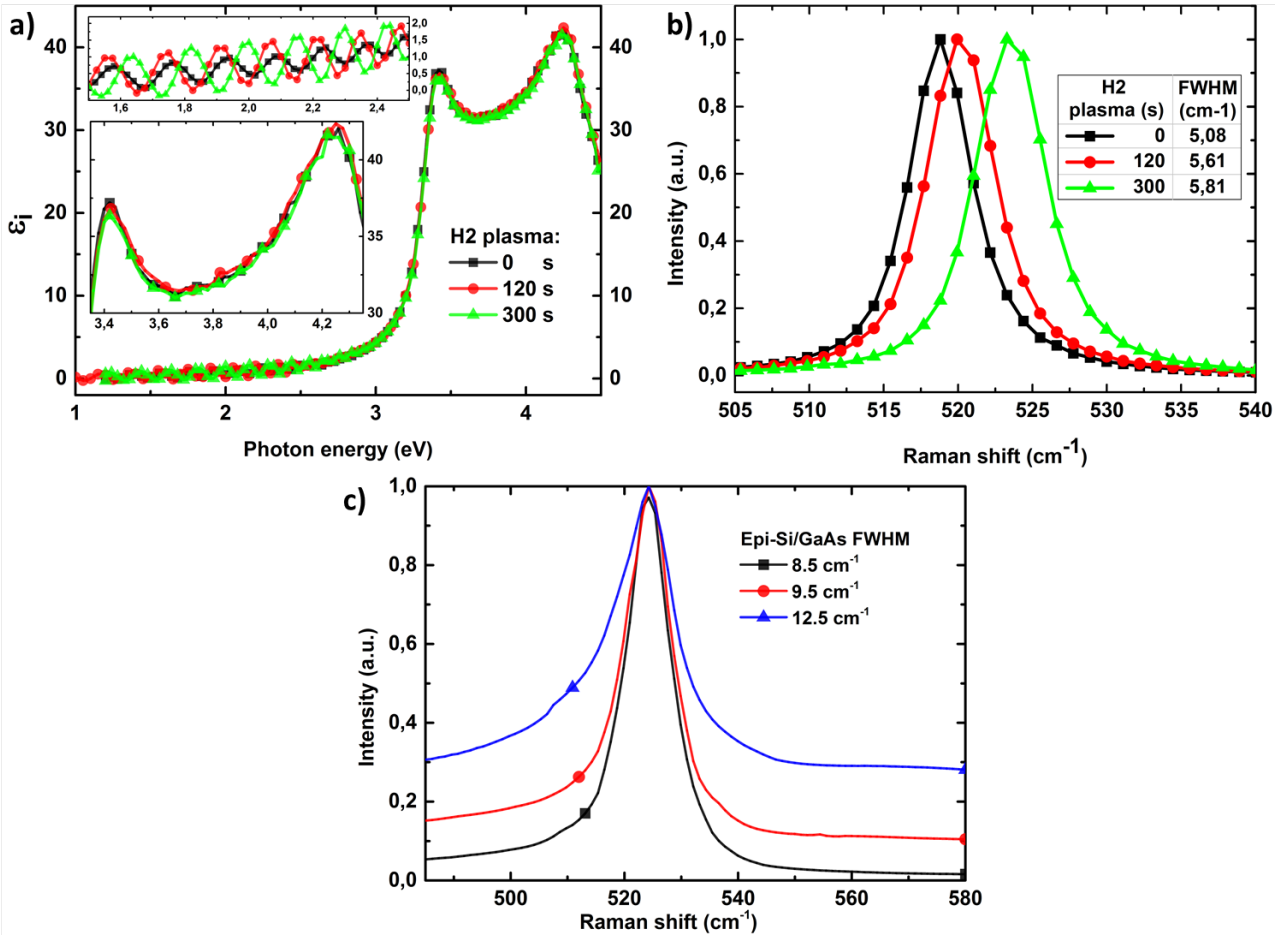


Fig. 2.9 – a) and b) show the ε_i and Raman spectrum for three epi-Si/c-Si samples with similar thicknesses but different wafer surface preparations resulting in strain. c) Raman spectra of epitaxial silicon deposited on GaAs substrate, with various levels of crystal quality.

2.4 Photovoltaic solar cell basics

2.4.1 Properties of sunlight

The sun emits light with a range of wavelength spanning the ultraviolet, visible and infrared sections of the electromagnetic spectrum. The extra-terrestrial sun spectrum is close to the spectrum of a black body at 5800 K (the Sun's surface temperature). A black body emits quanta of radiation, i.e. photons, according to the Bose-Einstein distribution function. Therefore, the photon flux, $\boldsymbol{\Phi_{ph}(E)}$ emitted by a black body at temperature $\boldsymbol{T}$ into an hemisphere, per unit of energy interval and per unit area of emitting surface, is expressed as[19]:

$$\boldsymbol{\Phi_{ph}(E) = \frac{2\pi}{h^3c^2}\left(\frac{E^2}{\exp(\frac{E}{k_B T_s}) - 1}\right)} \tag{2.7}$$

where $\boldsymbol{E}$ is the photon energy. The irradiance $\boldsymbol{F}$, or energy flux density (W.m^{-2}.nm^{-1}), is related to the photon flux and total power density H, or irradiation (W.m^{-2}), according to:

$$\boldsymbol{F(E) = \frac{hc}{\lambda}\Phi_{ph}(E) \qquad and \qquad H = \int_0^\infty F(E)dE} \tag{2.8}$$

The comparison between the 5800K black body spectrum, taking into account the solid angle that the solar cell forms, and the solar irradiance as measured just outside the atmosphere, the so-called AM0 spectrum, is shown in Fig.2.10. The solar power density of AM0 spectrum is roughly 1350 W.m^{-2}; when passing through the atmosphere, light is absorbed and scattered by various atmospheric constituents (H_2O, CO_2, O_2, etc.), so that the spectrum reaching the Earth is attenuated and has a different shape. The standard terrestrial spectrum is Air Mass 1.5 global, AM1.5G, corresponding to the sun being at 48.2° angle of elevation (see Fig.2.10). This atmospheric thickness attenuates the solar spectrum to an irradiation of 900 W.m^{-2}, but AM1.5G is normalized so that the irradiation is 1000 W.m^{-2}. AM0 and AM1.5G spectra are used respectively for spatial and terrestrial solar cells and module performance evaluation.

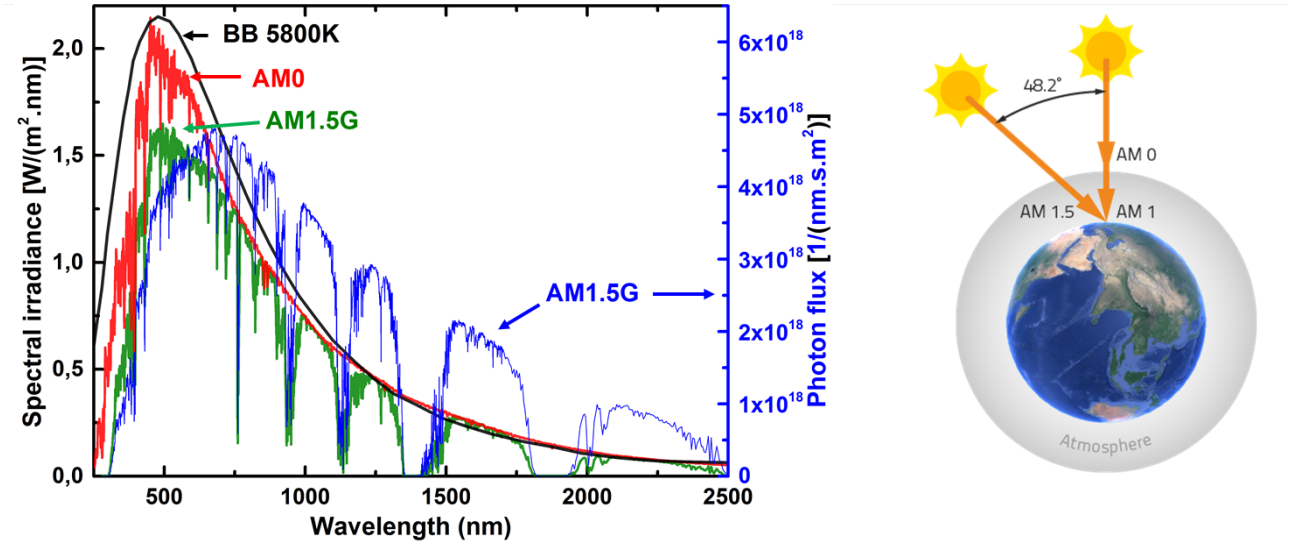


Fig. 2.10 – Spectral irradiance from the sun measured outside Earth's atmosphere (AM0 spectrum), and standard terrestrial irradiance (AM1.5G spectrum) after passing 1.5 air mass, as shown on the right (not at scale). The AM1.5G photon flux is also shown on the right y-axis.

[19] P.K. Nayak et al., Energy & Environmental Science, **5**: 6022–6039, 2012.

2.4.2 p-n junction

The p-n junction is the basis of solar cells and many electronic devices. Such junctions are formed by joining n-type and p-type semiconductor materials, as shown below (See Fig.2.11-a)). If both semiconductors have the same band gap energy, as for classical c-Si solar cells, this is called an homojunction; if the band gaps are different, the band diagram becomes slightly more complex, and we talk about heterojunction. The actual record silicon solar cell[20] is an heterojunction. Since the n-type region has a high electron concentration and the p-type a high hole concentration, electrons diffuse from the n-type side to the p-type side. Similarly, holes flow by diffusion from the p-type side to the n-type side. If the electrons and holes were not charged particles, this diffusion process would continue until the concentration of electrons and holes on the two sides were the same, as it happens if two gasses come into contact with each other. However, in a p-n junction, when the electrons and holes move to the other side of the junction, they leave behind exposed charges on dopant atom sites, which are fixed in the crystal lattice. On the n-type side, the charge transfer leaves positive ions, and on the p-type side, negative ions. This region is called the "depletion region" since the electric field quickly sweeps free carriers out, hence the region is depleted of free carriers.

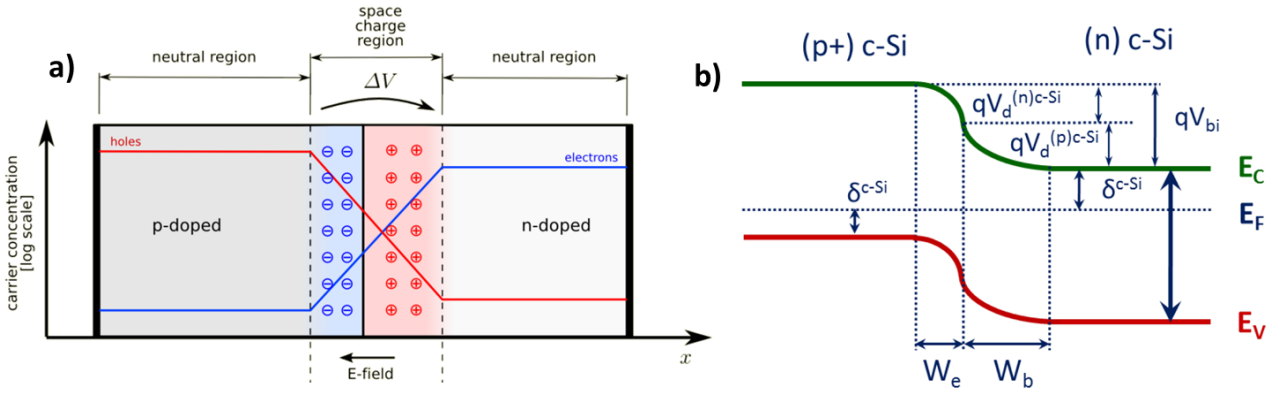


Fig. 2.11 – a) Schematic of a pn junction in thermal equilibrium with zero bias, and corresponding band diagram in the case of a crystalline silicon homojunction. From Wikipedia and M. Labrune[4].

Therefore, an electric field **E** is formed between the positive ions in the n-type material and negative ions in the p-type material; **E** is opposed to the diffusion: it acts as a barrier for majority carriers and a low resistance path for minority carriers. A "built in" potential due to electric field is formed at the junction. This built-in $\boldsymbol{V_{bi}}$ potential corresponds to the band bending of the p-n junction $\boldsymbol{qV_{bi}}$, as shown in Fig.2.11-b)[4]. The depletion region width, $\boldsymbol{W_e + W_h}$ depends on the doping concentration: the depletion region width is reduced when the semiconductors doping level is increased. This p-n junction is crucial for solar cells since it drives the collection of minority carriers which are photo-generated in n and p layers and reach the junction by diffusion.

2.4.3 Electrical model, I-V and EQE characteristics

In the dark, the Shockley diode equation describes the relation between the p-n junction current density $\boldsymbol{J}$ and its voltage $\boldsymbol{V}$:

$$\boldsymbol{J = J_o \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right]} \tag{2.9}$$

[20] Martin A. Green. "Silicon wafer-based tandem cells: The ultimate photovoltaic solution?" in: vol. 8981 2014. 89810L–89810L–6 DOI: 10.1117/12.2044175

[4] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells.* PhD thesis. Ecole Polytechnique, France, May 2011.

where k is the Boltzmann constant, T the temperature, J_o is the saturation current density and n the diode ideality factor. J_o is an important parameter which is linked to charge carriers recombination in the device: a low J_o indicates a high quality p-n junction. Thus measuring the J-V characteristic of a solar in the dark gives already important information. When exposed to light, an additional photo-generated current J_{ph}, flowing in the opposite direction, is created. Additionally, to account for the non-perfect characteristics of the device, parasitic resistances should be considered. Series resistance R_s can typically arise from metal-semiconductor contacts and the shunt resistance R_{sh} corresponds to leakage of current through the cell or around the edges of the device. The simple electrical model describing a solar cell is shown in Fig.2.12-a). The diode equation thus becomes:

$$J = J_0 \left[\exp(q\frac{V - JR_s}{nkT}) - 1\right] + \frac{V - JR_s}{R_{sh}} - J_{ph} \tag{2.10}$$

J-V characteristics of solar cells are measured at 25°C with a solar simulator, which delivers a power density of 100mW.cm^{-2} and reproduces the standard AM1.5G solar spectrum. The typical I-V curve of a solar cell (not normalized by the cell area) under illumination is shown in Fig.2.12-b). Three important points are highlighted: i) The open circuit voltage, V_{oc}, where no current flows, ii) the short-circuit current density, I_{sc}, where there is no voltage, and iii) the maximum power point, V_{mpp}, I_{mpp}, where the current voltage product is maximum. I_{sc} and V_{oc} are the maximum current and voltage respectively of a solar cell; however, at both of these operating points, the power from the solar cell is zero. The maximum power point determines a parameter called fill factor (FF), defined as: $FF = \frac{J_{mpp}V_{mpp}}{J_{sc}V_{oc}}$. Graphically, the FF is a measure of the "squareness" of the J(V) characteristic, and is also the area of the largest rectangle which will fit in the J(V) characteristic. The parasitic resistances decrease the FF as shown in in Fig.2.12-c,d): series resistance decreases the slope at V_{oc} and shunt resistance increases the slope at J_{sc}.

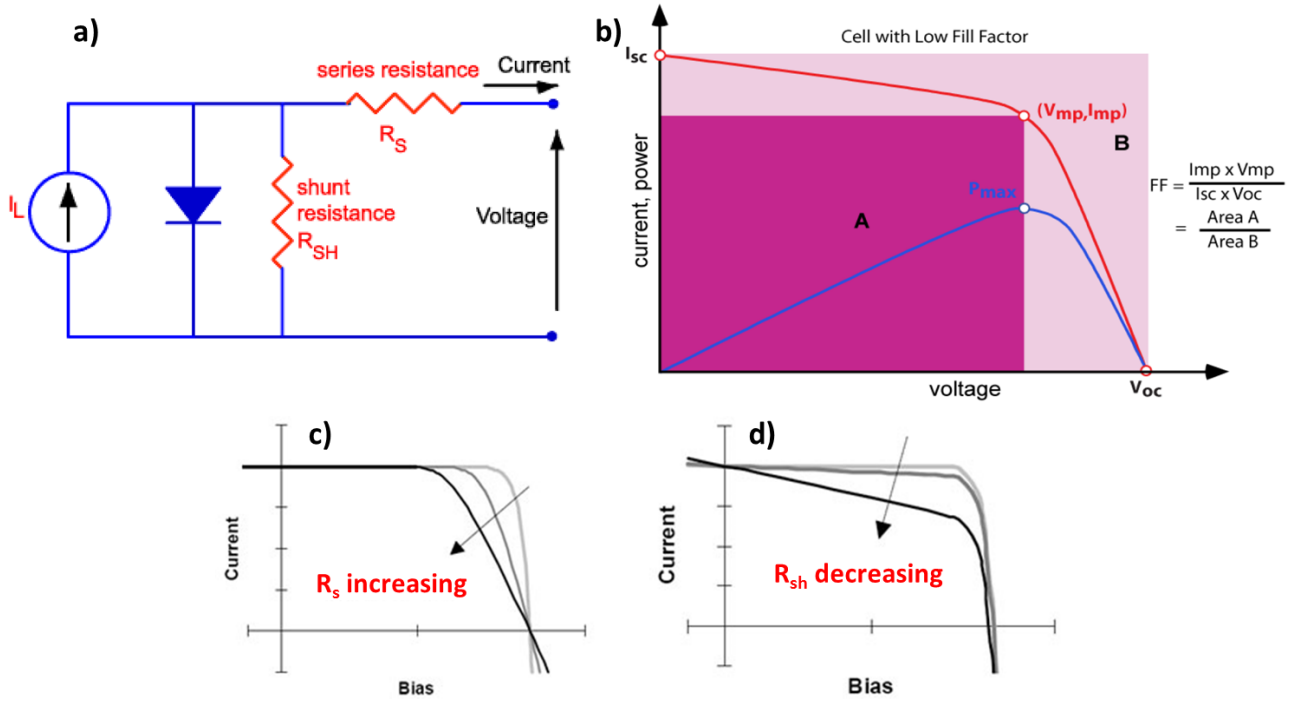


Fig. 2.12 – a) Electrical equivalent circuit for a photovoltaic cell under illumination. b) Current-voltage characteristic of a solar cell under illumination (red curve) and output power (blue curve). The maximum power has coordinates (V_{mp}, I_{mp}). Intersection of red curve with axes gives the values of the open circuit voltage V_{oc} and short-circuit current I_{sc}. c,d) effect of parasitic resistances on solar cell I-V curve. From pveducation.org.

The efficiency η of a solar cell is defined by the ratio between photo-generated electrical power density and the incident light power density:

$$\boxed{\eta = \frac{\mathbf{J_{mp}V_{mp}}}{\mathbf{P_{inc}}} = \frac{\mathbf{J_{sc}V_{oc}FF}}{\mathbf{P_{inc}}}} \tag{2.11}$$

The quantum efficiency (QE) is the probability that an incident photon of energy E will deliver one electron to the external circuit. If all photons of a certain wavelength are absorbed and the resulting minority carriers are collected, then the quantum efficiency at that particular wavelength is 1. Internal quantum efficiency (IQE) refers to the efficiency with which photons that are not reflected or transmitted out of the cell and can generate collectable carriers. By measuring the reflection and transmission of a device, the external quantum efficiency (EQE) curve can be corrected to obtain the IQE (IQE=EQE/(1-R-T)). The quantum efficiency for photons with energy below the band gap is zero. Ideally, the EQE has a square shape shown below (see Fig 2.13), but the quantum efficiency for most solar cells is reduced due to reflection and/or recombination effects.

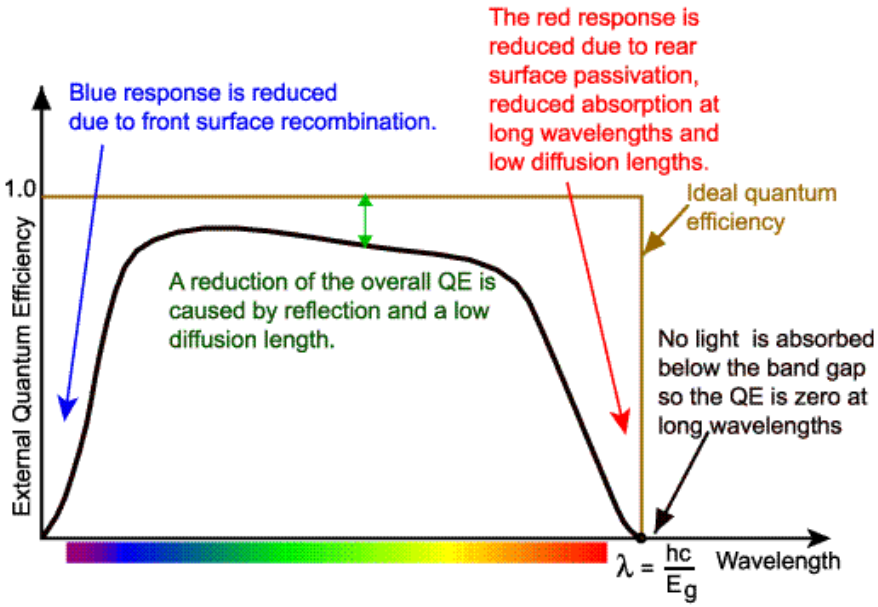


Fig. 2.13 – Example of quantum efficiency curve (EQE), from PVeducation.org.

QE is commonly used to characterize the ability to collect charge carriers generated by different wavelengths of the sun spectrum. As light of different colors is absorbed at differently depths in the solar cell ("blue" absorbed close to the surface and "red" in the bulk), the spectral response provides a depth resolution of the recombination processes, which hinder charge carriers to be collected. It is desirable to have a high QE at wavelengths where the solar flux density is high.

$\boldsymbol{J_{sc}}$ is due to the collection of light-generated carriers; this is the largest current density which may be drawn from the cell. From the EQE characteristic, one can extract the short circuit current:

$$\boldsymbol{J_{sc} = q \int \Phi_{ph}(E) QE(E) dE} \tag{2.12}$$

where $\boldsymbol{\Phi_{ph}(E)}$ represents the spectral photon flux density, i.e. the number of incoming photons with energy $\boldsymbol{h\nu \in [E; E + dE]}$ per unit of time and per unit of surface.

2.4.4 Losses and efficiency limit for single junction solar cells

Before introducing the concept of multijunction solar cells, let us first have a look at the origin of energy conversion losses in a single junction solar cell[21,22]: this is indeed useful to understand which issues are addressed by the multijunction approach. A single junction solar solar can be considered as a heat engine for which the sun acts as the hot reservoir of temperature T_s, and the Earth atmosphere as a cold reservoir of temperature T_a. According to the second law of thermodynamics, the maximum energy conversion efficiency achievable by this heat engine is given by the Carnot limit:

$$\eta_{max} = 1 - \frac{T_a}{T_s} \tag{2.13}$$

Thus, using the 5800K of the Sun's surface temperature and 300K for the atmosphere, the solar energy conversion appears limited to roughly 95%. In a photovoltaic device, this Carnot loss manifest itself as a voltage drop[23] which reduces the open circuit voltage at room temperature by 5% compared to the band gap. According to Kirchoff's law, the solar cell absorbs the sun radiation but also re-emits spontaneously some radiation (non-black body radiation), which also decreases the conversion efficiency. In addition other sources of entropy loss can be identified: i) the incomplete light absorption in the device and the semiconductor material imperfections (IQE<1). ii) The inequality between absorption and emission angles results also in entropy generation because of photon modes expansion. Indeed, the direct solar spectrum is incident within a solid angle (Ω_{abs}=6×10^{-5} str., whereas solar cell emits within a solid angle of up to Ω_{emit}=4π str; this optical étendue mismatch introduces irreversibility which further reduces the V_{oc} by up to 315 mV. The separation of the electron-hole quasi-fermi levels, qV_{oc}, is the upper bond for the solar cell open circuit voltage (see Fig.2.14 band diagram) and the effect of the above mentioned losses on V_{oc} may be approximated by[22,24,25]:

$$qV_{oc} = E_g\left(1 - \frac{T_a}{T_{sun}}\right) - k_B T_a\left[ln\left(\frac{\Omega_{emit}}{\Omega_{abs}}\right) + ln\left(\frac{4n^2}{I}\right) - ln\,(IQE)\right] \tag{2.14}$$

where E_g is the absorber material band gap, k_B the Boltzmann constant, n the absorber refractive index, I the light absorption enhancement factor with respect to the planar case. The solar cell voltage will be further reduced since the maximum power point voltage is typically ∼100 mV lower than V_{oc}. While Carnot and Kirchoff's are intrinsic unavoidable losses, the term $k_B T_a ln\left(\frac{\Omega_{emit}}{\Omega_{abs}}\right)$ in eq.2.14, so-called Boltzmann factor by analogy with statistical thermodynamics, can in principle be reduced down to zero under maximum concentration of the sunlight. Neither incomplete light trapping nor non-radiative recombinations are intrinsic losses, thus they may also in principle be reduced down to zero if a perfect direct band gap semiconductor is used.

But overall, the biggest losses in single junction solar cells come from the mismatch between the broad solar spectrum and the mono-energetic absorption of photons of the single gap material: this simply results in non-absorption of photons with sub-band gap energies. And on the other hand, the carriers generated by high energy photons (compared to E_g) rapidly thermalize down to the conduction band edge loosing energy through lattice phonon interactions. These two processes of transmission and thermalization are illustrated in Fig.2.14 band diagram; they result in more than 40% efficiency drop. The cumulative losses affecting the single junction solar cell efficiency are summarized in Fig.2.14 schematic[22].

[21] L.C. Hirst et al., Progress in Photovoltaics: Research and Applications, **19**: 286–293, 2011.
[22] A. Polman et al., Nature Materials, **11**: 174–177, 2012.
[23] P.T. Landsberg et al., Solid-State Electronics, **42**: 657–659, 1998.
[24] U. Rau et al., Nature Materials, **13**: 103–104, 2014.
[25] H.A. Atwater et al., Nature Materials, **13**: 104–105, 2014.

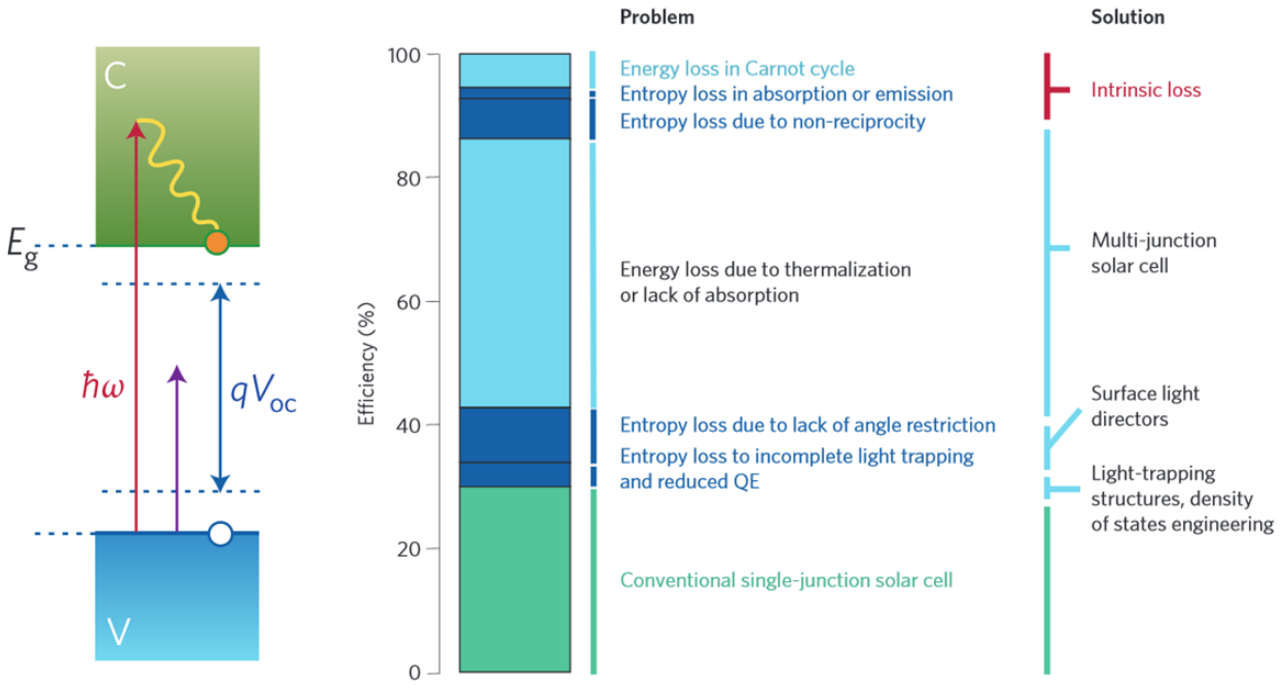


Fig. 2.14 – Energy conversion losses for a single junction solar cell[22].

The most widely used efficiency limit of a single junction solar cell, as published by Shockley and Queisser (SQ)[26], corresponds to roughly 33%. This limit is increased up to slightly more than 40% if concentration or photonic structures are used to reduce the optical étendue mismatch. This 33% SQ limit is represented in Fig.2.15-a), for a c-Si solar cell[27]. The red shade corresponds to the fraction of the incident solar spectral irradiance that can be converted by a c-Si solar cell (band gap 1.12 eV at room temperature), thermalization and transmission losses are indicated by arrows. The existence of an optimum material band gap to maximize photovoltaic energy conversion, in the case of a single junction, can be understood easily: a low band gap semiconductor material absorb a broader spectral range of solar photons (thus achieve a high $\boldsymbol{J_{sc}}$), but at the same time the voltage of the device is reduced and thermalization losses increase. The opposite situation corresponds to a high band gap material which minimizes the thermalization losses and offer a high $\boldsymbol{V_{oc}}$, but suffers on other other hand from high transmission losses. Since the efficiency of a solar cell is driven by the product of the current and the voltage, the best efficiency result from a balance between thermalization and transmission losses.

The SQ limit as a function of solar cell absorber band gap is illustrated in Fig.2.15-b), together with best-in-class solar cells as reported by Green et al.[28]. The maximum of this efficiency curve appears relatively flat between 1.1 and 1.4 eV; thus c-Si, GaAs, InP, CdTe are semiconductor materials with a band gap well suited for solar spectrum energy conversion. The highest efficiency, for a single junction solar cell, has been achieved recently by the company Alta Devices with an epitaxial lift-off GaAs material reaching 28.8%[28]. Given the additional issues that are facing real devices (parasitic recombination, series resistances, contact shadowing, etc.) this device is indeed very close to the SQ limit. In comparison, the c-Si material is limited to a lower value (see dashed blue line), due to the non-radiative Auger recombination process, which causes additional thermalization losses[29].

[26] W. Shockley et al., Journal of Applied Physics, **32**: 510, 1961.
[27] S.W. Glunz., Book: Advanced Concepts in Photovoltaics, , 2014.
[28] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **22**: 1–9, 2014.
[29] A. Richter et al., Energy Procedia, **27**: 88–94, 2012.

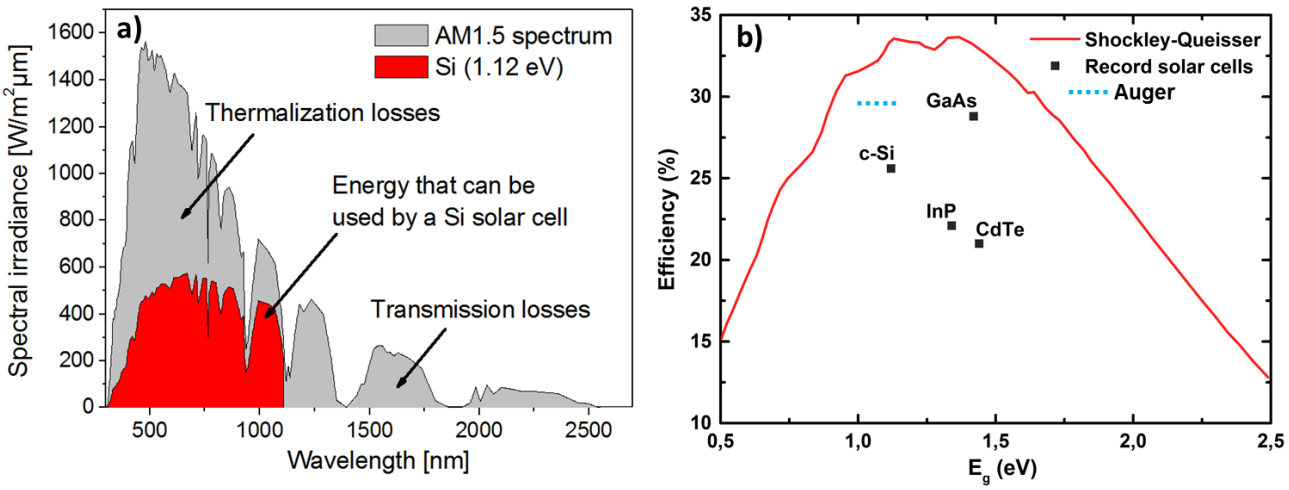


Fig. 2.15 – a) Solar spectral irradiance and fraction (red shade) that can be converted into electricity by a c-Si cell, within the Shockley-Queisser limit[26]. b) Shockley-Queisser limit as a function band gap, compared with best-in-class cells. The dashed line indicate the Auger limit for c-Si[27].

2.4.5 The concept of multijunction solar cells

As mentioned in Fig.2.14, the best solution to date addressing the huge transmission and thermalization losses are multijunction solar cells[30]. The idea is to stack several semiconductor materials with decreasing band gap energies from the cell surface to the bottom of the device. By doing so, a larger portion of the solar spectrum can be absorbed: the high band gap semiconductors are used to absorb the short wavelength radiation and the long wavelength part is transmitted to a second semiconductor beneath, with a lower band gap energy, etc. Splitting the absorption between different gaps reduces both thermalization and transmission issues; III-V semiconductor are the material of choice for multijunction solar cells. This concept is illustrated in Fig.2.16-a) for a solar cell composed of $Ga_{0.49}In_{0.51}P$(1.86eV)/$Ga_{0.99}In_{0.01}As$(1.4eV)/Ge(0.7eV). The fraction of the incident spectral irradiance that can be converted into electricity by each of the sub-cells InGaP/InGaAs/Ge are shaded in blue/green/red respectively. This approach is usually done by growing different semiconductor materials sequentially on one substrate. Note that the multijunction concept has also been successfully applied to thin film silicon layers[31].

As an example, the layer structure of a triple junction InGaP/InGaAs/Ge solar cell is shown in cross section in Fig.2.16-b). The three sub-cells are shaded in blue, green and red; each one is composed of 4 layers: the absorber and the emitter layer, forming the pn junction, and the window and back surface field forming minority carrier barriers for the front and back side of the device respectively. Between each sub-cells, tunnel diodes[32] are used to form a low series resistance electrical connection. Such a monolithic solar cell has the advantage that the final device looks like a conventional single-junction solar cell with only one front and back side contact. Due to the series connection, the overall current in such a solar cell is limited by the lowest current generated by one of the sub-cells, but the sub-cells voltages are added. To keep a high crystal quality in all the layers, the common approach consist in growing epitaxial materials with similar lattice constant. The development of tandem solar cells based on GaInP and GaAs started around 1985[33,34] at NREL, and their efficiency has continuously improved over the years. This is still a very active research field with actual record being 44.7%[35] for a 4 junctions device as measured under a 297-times concentrated solar spectrum (the latest improvements of this

[30] F. Dimroth., physica status solidi (c), **3**: 373–379, 2006.
[31] B. Yan et al., Applied Physics Letters, **99**: 113512–113512–3, 2011.
[32] J.F. Wheeldon et al., Progress in Photovoltaics: Research and Applications, **19**: 442–452, 2011.
[33] J.M. Olson "Multilayer photoelectric cells" pat. US4667059 A .1985
[34] J.M. Olson et al., 18th IEEE Photovoltaic Specialists Conference, 777–780 vol.1, 1988.
[35] F. Dimroth et al., Progress in Photovoltaics: Research and Applications, **22**: 277–282, 2014.

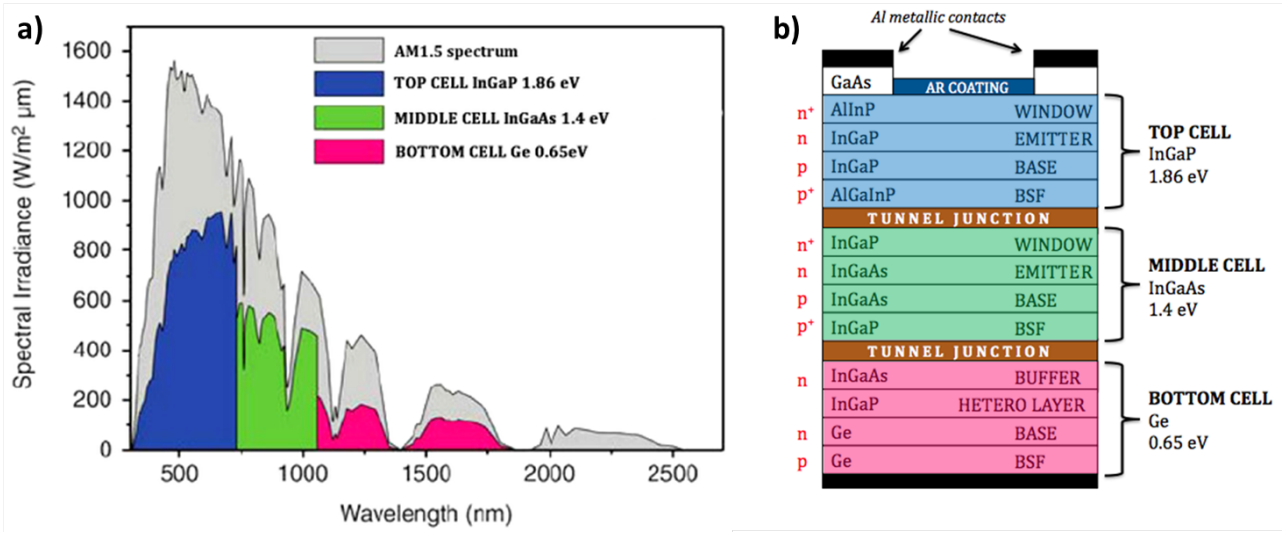


Fig. 2.16 – a) Solar spectral irradiance and fraction that can be converted into electricity by a InGaP(blue shade)/(In)GaAs(green shade)/Ge(red shade) triple junction cell. b) Diagram of layer stack for the corresponding solar cell device. From Wikipedia.

device has even lead to 46.5%). Indeed by concentrating the sunlight, the solar cell area (and thus the required material) can be reduced, while at the same time a logarithmic efficiency increase with the illumination is obtained (decrease of Boltzmann entropy loss). The multijunction approach is foreseen to reach the symbolic 50% threshold in the coming years[36].

[36] A. Luque., Journal of Applied Physics, **110**: 031301, 2011.

References

[1] M.A. Lieberman. *Principles of plasma discharges and materials processing*. 2nd ed Wiley-Interscience, 2005. (see pp. 16, 18)

[2] P. Chabert. *Physics of radio-frequency plasmas*. Cambridge: Cambridge University Press, 2011. (see p. 16)

[3] P. Roca i Cabarrocas. A fully automated hot-wall multiplasma-monochamber reactor for thin film deposition. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, **9**: 2331, 1991. doi: 10.1116/1.577318 (see p. 17)

[4] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells*. PhD thesis. Ecole Polytechnique, France, May 2011. (see pp. 18, 28)

[5] J.R. Chelikowsky and M.L. Cohen. Electronic structure of silicon. *Physical Review B*, **10**: 5095–5107, 1974. doi: 10.1103/PhysRevB.10.5095 (see p. 20)

[6] N.W. Ashcroft, N.D. Mermin, F. Biet, and H. Kachkachi. *Physique des solides*. EDP sciences, 2002. (see p. 20)

[7] C. Kittel. *Introduction to solid state physics*. 8th ed Wiley, 2005. (see p. 20)

[8] L. Royer. Recherches expérimentales sur l'épitaxie ou orientation mutuelle de cristaux d'espéces differentes. *Société française de minéralogie et de cristallographie*, **51**: 7–159, 1928. (see p. 20)

[9] M. Opel. Spintronic oxides grown by laser-MBE. *Journal of Physics D: Applied Physics*, **45**: 033001, 2012. doi: 10.1088/0022-3727/45/3/033001 (see p. 21)

[10] K. Oura, ed. *Surface science: an introduction*. Advanced texts in physics Springer, 2003. (see p. 21)

[11] D. Crippa, D.L. Rode, and M. Masi. *Silicon epitaxy*. Academic Press, 2001. (see p. 21)

[12] B.J. Baliga, ed. *Epitaxial silicon technology*. Academic Press, 1986. (see p. 21)

[13] D.B. Williams and C.B. Carter. *Transmission electron microscopy: a textbook for materials science*. Springer, 2009. (see p. 22)

[14] B.D. Cullity and S.R. Stock. *Elements of x-ray diffraction*. Prentice Hall, 2001. (see p. 22)

[15] Y. Waseda. *X-Ray diffraction crystallography: introduction, examples and solved problems*. Springer, 2011. (see p. 22)

[16] D.E. Aspnes and A.A. Studna. Dielectric functions and optical parameters of Si, Ge, GaP, GaAs, GaSb, InP, InAs, and InSb from 1.5 to 6.0 eV. *Physical Review B*, **27**: 985, 1983. doi: 10.1103/PhysRevB.27.985 (see p. 23)

[17] D.A.G. Bruggeman. Berechnung verschiedener physikalischer Konstanten von heterogenen Substanzen. I. Dielektrizitätskonstanten und Leitfähigkeiten der Mischkörper aus isotropen Substanzen. *Annalen der Physik*, **416**: 636–664, 1935. doi: 10.1002/andp.19354160705 (see p. 23)

[18] I.D. Wolf. Micro-Raman spectroscopy to study local mechanical stress in silicon integrated circuits. *Semiconductor Science and Technology*, **11**: 139–154, 1996. doi: 10.1088/0268-1242/11/2/001 (see p. 25)

[19] P.K. Nayak, G. Garcia-Belmonte, A. Kahn, J. Bisquert, and D. Cahen. Photovoltaic efficiency limits and material disorder. *Energy & Environmental Science*, **5**: 6022–6039, 2012. doi: 10.1039/C2EE03178G (see p. 27)

[20] Martin A. Green. "Silicon wafer-based tandem cells: The ultimate photovoltaic solution?" in: vol. 8981 2014. 89810L–89810L–6 doi: 10.1117/12.2044175 (see p. 28)

[21] L.C. Hirst and N.J. Ekins-Daukes. Fundamental losses in solar cells. *Progress in Photovoltaics: Research and Applications*, **19**: 286–293, 2011. doi: 10.1002/pip.1024 (see p. 31)

[22] A. Polman and H.A. Atwater. Photonic design principles for ultrahigh-efficiency photovoltaics. *Nature Materials*, **11**: 174–177, 2012. doi: 10.1038/nmat3263 (see pp. 31, 32)

[23] P.T. Landsberg and T. Markvart. THE CARNOT FACTOR IN SOLAR-CELL THEORY. *Solid-State Electronics*, **42**: 657–659, 1998. doi: 10.1016/S0038-1101(97)00253-0 (see p. 31)

[24] U. Rau and T. Kirchartz. On the thermodynamics of light trapping in solar cells. *Nature Materials*, **13**: 103–104, 2014. doi: 10.1038/nmat3837 (see p. 31)

[25] H.A. Atwater and A. Polman. Reply to 'On the thermodynamics of light trapping in solar cells'. *Nature Materials*, **13**: 104–105, 2014. doi: 10.1038/nmat3838 (see p. 31)

[26] W. Shockley and H.J. Queisser. Detailed Balance Limit of Efficiency of p-n Junction Solar Cells. *Journal of Applied Physics*, **32**: 510, 1961. doi: 10.1063/1.1736034 (see pp. 32, 33)

[27] S.W. Glunz. CHAPTER 1. Crystalline Silicon Solar Cells with High Efficiency. *Book: Advanced Concepts in Photovoltaics*, 2014. doi: 10.1039/9781849739955-00001 (see pp. 32, 33)

[28] M.A. Green, K. Emery, Y. Hishikawa, W. Warta, and E.D. Dunlop. Solar cell efficiency tables (version 43). *Progress in Photovoltaics: Research and Applications*, **22**: 1–9, 2014. doi: 10.1002/pip.2452 (see p. 32)

[29] A. Richter, F. Werner, A. Cuevas, J. Schmidt, and S.W. Glunz. Improved Parameterization of Auger Recombination in Silicon. *Energy Procedia*, **27**: 88–94, 2012. doi: 10.1016/j.egypro.2012.07.034 (see p. 32)

[30] F. Dimroth. High-efficiency solar cells from III-V compound semiconductors. *physica status solidi (c)*, **3**: 373–379, 2006. doi: 10.1002/pssc.200564172 (see p. 33)

[31] B. Yan, G. Yue, L. Sivec, J. Yang, S. Guha, and C.S. Jiang. Innovative dual function nc-SiOx:H layer leading to a >16% efficient multi-junction thin-film silicon solar cell. *Applied Physics Letters*, **99**: 113512–113512–3, 2011. doi: 10.1063/1.3638068 (see p. 33)

[32] J.F. Wheeldon, C.E. Valdivia, A.W. Walker, G. Kolhatkar, A. Jaouad, A. Turala, B. Riel, D. Masson, N. Puetz, S. Fafard, R. ArÃĹs, V. Aimez, T.J. Hall, and K. Hinzer. Performance comparison of AlGaAs, GaAs and InGaP tunnel junctions for concentrated multijunction solar cells. *Progress in Photovoltaics: Research and Applications*, **19**: 442–452, 2011. doi: 10.1002/pip.1056 (see p. 33)

[33] J.M. Olson "Multilayer photoelectric cells" pat. US4667059 A .1985 (see p. 33)

[34] J.M. Olson, S.R. Kurtz, and A.E. Kibbler. A 21.8% $GaInP_2$/GaAs tandem solar cell. *18th IEEE Photovoltaic Specialists Conference*, 777–780 vol.1, 1988. doi: 10.1109/PVSC.1988.105809 (see p. 33)

[35] F. Dimroth, M. Grave, P. Beutel, U. Fiedeler, C. Karcher, T.N.D. Tibbits, E. Oliva, G. Siefer, M. Schachtner, A. Wekkeli, A.W. Bett, R. Krause, M. Piccin, N. Blanc, C. Drazek, E. Guiot, B. Ghyselen, T. Salvetat, A. Tauzin, T. Signamarcheix, A. Dobrich, T. Hannappel, and K. Schwarzburg. Wafer bonded four-junction GaInP/GaAs//GaInAsP/GaInAs concentrator solar cells with 44.7% efficiency. *Progress in Photovoltaics: Research and Applications*, **22**: 277–282, 2014. doi: 10.1002/pip.2475 (see p. 33)

[36] A. Luque. Will we exceed 50% efficiency in photovoltaics? *Journal of Applied Physics*, **110**: 031301, 2011. doi: 10.1063/1.3600702 (see p. 34)

Chapter 3

Low temperature RF-PECVD epitaxial growth

Contents

There is already a quite broad range of techniques available for silicon epitaxial growth[1]. However almost all the common approaches are based on high temperature processes (namely 800 to 1200°C), and the explanation for this is quite straightforward: a high substrate temperature guarantees a high surface mobility for adatoms. Thus, the adsorbed species on the silicon surface can overcome the potential barrier to be incorporated in an epitaxial configuration. Nevertheless, the ability to grow crystalline material at low temperature is highly desirable for many reasons: i) to avoid dopant/impurities diffusion ii) to limit thermal expansion related issues iii) to lower the cost significantly. Some catalytic CVD techniques, such as Hot Wire CVD (HWCVD), can sustain epitaxial growth for a slightly lower temperature: Teplin et al.[2] reported epitaxial growth down to around 550°C. But further decrease of the temperature results in polycrystalline or even amorphous material. One can argue that in fact, under ultra high vacuum conditions, silicon homoepitaxy is possible down to room temperature, as reported by Eaglesham et al.[3] However at low temperature, the films tend to lose their epitaxial nature beyond a certain thickness, and for room temperature MBE growth, it is in the range of a few nanometers. This critical thickness, which has an exponential temperature dependence, results from the gradual development of defects, crystal faults and roughness which lead to termination of epitaxy when the underlying surface has reached a critical level of deviation from the perfect crystal.

In this chapter, we present our results on silicon epitaxial growth below 200°C by radio frequency plasma enhanced chemical vapor deposition, namely RF-PECVD. Surprisingly enough, using this standard technique usually dedicated to amorphous and microcrystalline material deposition, monocrystalline material a few microns thick can be obtained. To sustain a crystal growth in the 150 to 350°C range, some additional energy besides the thermal one has to be supplied to compensate for the low surface mobility of adatoms, and thus allow high-quality epitaxy. Consequently, in the results presented below, we try to bring answers to the following questions: i) Can we really grow monocrystalline silicon in standard RF-PECVD reactor below 200°C? ii) What material quality can we obtain? iii) How can we explain such an unusual epitaxial growth?

After a brief literature overview, we present our experimental findings and understanding about low temperature RF-PECVD epitaxial growth. By doing so, we constantly put our results in perspective with literature studies.

3.1 Where the story begins: the c-Si/a-Si:H hetero-interface

The LPICM has a strong expertise in the field of thin film silicon deposition assisted by plasma. Over the past 30 years, it has developed a high skill level covering the whole value chain from plasma diagnosis, material characterization up to device testing. However, until recently[4,5], the LPICM was mainly focusing on disordered materials such as hydrogenated amorphous silicon (a-Si:H), polymorphous silicon (pm-Si:H) and microcrystalline silicon (μc-Si:H)[6–9]. The low temperature epitaxial growth phenomena was firstly observed at LPICM as a side effect happening when trying to grow a-Si:H on a clean (100)-oriented c-Si surface[10]. To illustrate this, a high resolution TEM cross section image of the c-Si/a-si:H interface is shown on Fig.3.1. The a-Si:H was deposited by PECVD at 175°C on c-Si (100) wafer cleaned by hydrofluoric acid. It is clear from this image that the atomic order, visi-

[1] G. Beaucarne et al., Thin Solid Films, **511-512**: 533–542, 2006.
[2] C.W. Teplin et al., Applied Physics Letters, **96**: 201901–201901–3, 2010.
[3] D.J. Eaglesham et al., Physical Review Letters, **65**: 1227, 1990.
[4] J. Damon-Lacoste. *Vers une ingénierie de bandes des cellules solaires à hétérojonctions a-Si:H/c-Si. Rôle prépondérant de l'hydrogène.* PhD thesis. Ecole Polytechnique, France, July 2007.
[5] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells.* PhD thesis. Ecole Polytechnique, France, May 2011.
[6] A Fontcuberta i Morral et al., Materials Science and Engineering: B, **69-70**: 559–563, 2000.
[7] S. Kasouit et al., Journal of Non-Crystalline Solids, **299-302, Part 1**: 113–117, 2002.
[8] Y. Veschetti et al., Thin Solid Films, **511-512**: 543–547, 2006.
[9] P. Roca i Cabarrocas et al., Plasma Physics and Controlled Fusion, **50**: 124037, 2008.
[10] J. Damon-Lacoste et al., Journal of Applied Physics, **105**: 063712, 2009.

ble in the substrate, propagates over 1-4 nanometers into the a-Si:H layer, by forming pyramidal shape epitaxial areas. This epitaxial growth at crystalline amorphous interface has been reported by several groups to result in a poor surface passivation[11–13] and thus this low temperature epitaxial growth was somehow black-listed by the heterojunction solar cell community. Obviously, various strategies were found to avoid this epitaxial growth related passivation problems; for example the use of an ultra-thin a-SiC:H layer between the c-Si and the a-Si:H layer[5] can suppress this effect.

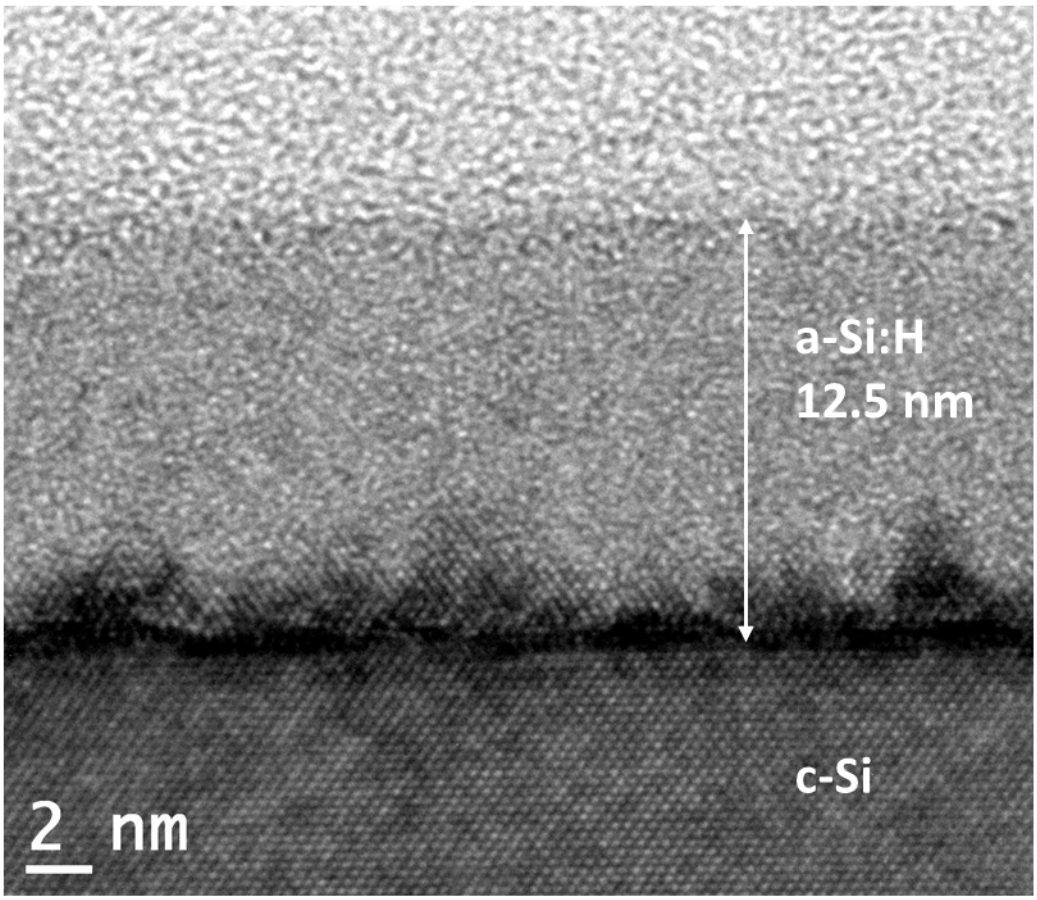


Fig. 3.1 – Cross section high resolution TEM image along (110) direction of c-Si/a-Si:H interface. The a-Si:H is deposited at 175°C in a RF-PECVD reactor on c-Si (100) after native oxide removal by HF dipping. Pyramidal shape epitaxial growth is detected at the interface.

In the deposition conditions of Fig.3.1, the epitaxial growth can however only be sustained over a relatively limited thickness. In this PhD thesis manuscript, tackling the issue from a different perspective, we try to find the best conditions to promote such low temperature epitaxial growth.

3.2 Low temperature PECVD epitaxy literature overview

Publications related to low temperature PECVD epitaxy are relatively scarce. In this section we try to give a brief overview of this topic and its understanding, through the literature published over the last 30 years.

[11] S. De Wolf et al., Applied Physics Letters, **90**: 042111, 2007.
[12] H. Fujiwara et al., Journal of Applied Physics, **101**: 054516–054516–9, 2007.
[13] J.J.H. Gielis et al., Thin Solid Films, **517**: 3456–3460, 2009.

We have to look back to the publications from the 1980's to find the first report of plasma enhanced chemical vapor deposition (PECVD) epitaxial growth. Compared to higher temperature approaches, this was proposed as a solution to minimize diffusion related problems, auto-doping and thermal stress, while enabling high throughput and conformal coverage (unlike MBE process). By that time, deposition was performed at substrate temperatures in the range of 750 to 800°C, after a first step of ex-situ chemical surface cleaning and/or in-situ Ar plasma cleaning (sputtering), from a pure silane plasma in the range of 1 to 100 mTorr. Epitaxial growth rates of few tens of Å/s were mentioned, and epitaxial layers of few microns were demonstrated on (100) as well as (111)-oriented substrates[14,15]. The importance of plasma generated ions energy was already underlined: an additional DC bias was applied to the substrate to increase ion bombardment energy (and thus sputtering effect) during pre-epitaxial surface cleaning step; then the DC bias was switched off to have low energy ions during growth (less defects). Two beneficial effects were attributed to the plasma (compared to CVD at similar temperature): i) an increased deposition rate, due to higher density of reactive species, and ii) enhanced surface mobilities of adsorbed species, thanks to ions flux providing localized surface energy[16]. With no degradation in crystal quality nor in chemical purity, PECVD epitaxy was recognized as a new way to perform "low temperature" epitaxial growth.

This PECVD epitaxial technique was then extended to lower temperature, namely 250 °C, in 1987 by Japanese teams[17,18]. To overcome the transition towards polycrystalline observed by Suzuki et al.[15] for deposition temperatures below 600°C, they used a different plasma chemistry based on Si, H and F: $H_2/SiH_4/SiH_2F_2$ or $H_2/SiF_4/Ar$, as well as higher pressure (1-5 Torr). A growth rate of 1-2 Å/s was obtained on c-Si (100)-oriented substrate, after RCA process for surface cleaning. From low to high SiH_2F_2 flow rate, they observed a transition from microcrystalline to a highly disordered material (amorphous), with epitaxial growth happening in between. This transition was attributed to the competitive effect of hydrogen and fluorine: H terminated surface enhances the precursor migration while F extracts the excess bonded H (HF formation); epitaxial growth would happen for a good balance between these two effects. This technique leads to hydrogen incorporation in the Si layers of few percent and fluorine content around 0.1%. Also, high ion energy produced by high RF power was reported to hinder epitaxial growth.

In 1989, researchers from Xerox company published results showing that PECVD epitaxial growth, in the 150-300°C temperature range, could also be achieved without fluorine in the plasma, using standard SiH_4/H_2 chemistry.[19,20] This effect was explained by a balance between deposition and etching (surface limited process) by atomic hydrogen (reactions forming volatile species). Indeed, they mentioned that hydrogen etches the energetically unfavorable configurations; e.g. in H_2 plasma, a higher etching rate was obtained for amorphous silicon as compared to microcrystalline. They also found that decreasing the temperature from 350 down to 150°C result in H incorporation in the epitaxial film changing by two orders of magnitude, from 10^{19} to $10^{21}cm^{-3}$. The hydrogen, mainly incorporated in the form of platelets ($\sim$ 10 nm size and (111)-oriented), is mostly coming from SiH_4 dissociation as concluded from D_2 plasma experiments. In 1991, another group[21] published an interesting paper focusing on the effect of ion bombardment energy on low temperature epitaxial growth. They came to the conclusion that the low surface mobility for adsorbed species at low temperature, that would prevent from epitaxial growth, can in fact be compensated by controlling the total energy dose on a film surface thanks to low-energy ion bombardment. An optimum energy of about 25 eV at 300°C

[14]T.J. Donahue et al., Applied Physics Letters, **44**: 346–348, 1984.
[15]S. Suzuki et al., Journal of Applied Physics, **54**: 1466–1470, 1983.
[16]J.H. Comfort et al., Applied Physics Letters, **51**: 2016–2018, 1987.
[17]K. Nagamine et al., Jpn. J. Appl. Phys., **26**: L951, 1987.
[18]N. Shibata et al., Jpn. J. Appl. Phys., **26**: L10, 1987.
[19]C.C. Tsai et al., Journal of Non-Crystalline Solids, **114, Part 1**: 151–153, 1989.
[20]C.C. Tsai et al., Journal of Non-Crystalline Solids, **137-138**: 673–676, 1991.
[21]T. Ohmi et al., Journal of Applied Physics, **69**: 2062–2071, 1991.

was found.

In the late 1990's, several groups came to the conclusion that, indeed, hydrogen coverage lowered the Si precursors diffusion on the surface. Looking at the influence of silane dilution in SiH_4/H_2 plasmas, Chen et al.[22] also noticed that an optimum dilution promoted epitaxial growth while low(high) H_2 flux resulted in amorphous(microcrystalline) growth. From a temperature and RF power series experiments, they found a linear relationship between power and deposition rate, and an epitaxial growth activation energy of 0.05 eV between 165 and 300 °C. Rosenbald et al.[23] also claimed that ion bombardment helped to enhance adatoms surface mobility as well as to remove some hydrogen from the surface. However, ions impinging on the surface can also induce bulk damage. And by changing the substrate DC bias, in a low pressure plasma ($\sim$ 10 mTorr), assuming a constant plasma potential, they have shown an ion energy threshold of 15 eV above which defects such as stacking faults start to appear in the layer. By STM investigations of surface morphology of various samples, a link between surface roughness, island growth mode and the presence of stacking faults in the epitaxial layer was established.

During the first decade of this century, most of the articles dealing with low temperature PECVD epitaxial growth are related to the field of photovoltaics. The possibility to grow doped epitaxial layers with this technique was used to form homojunction solar cells: p-type or n-type carrier selective contacts epitaxially grown on c-Si are reported by several groups[24–27]. This epitaxial process was also recognized by the silicon heterojunction community as a side effect during deposition of amorphous silicon on cleaned c-Si (100) surface: a thin epitaxial layer was observed at this interface, resulting in a decrease of the passivation quality and a subsequent reduction of solar cell performances[8,11,28]. Some study published by a Japanese team has also addressed the crucial point of the deposition rate: Kambara et al.[29] have reported PECVD silicon epitaxy as fast as 60 nm/s. However they needed high power and 700°C to reach this value. Over the past ten years, LPICM has been very active in this field of low temperature epitaxy. Building on its strong experience in plasma deposition of thin film silicon amorphous and microcrystalline materials, significant results have been achieved in terms of characterization, devices and understanding[5,10,30–32]; the details of this work will be presented throughout this manuscript. Interestingly enough, one can see that apart from LPICM research group and few sparse proceedings papers[33,34], PECVD epitaxial growth is also an active research area at IBM[35,36], for solar cells and transistors applications.

[22] C.-H. Chen et al., Journal of Crystal Growth, **147**: 305–312, 1995.
[23] C. Rosenblad et al., Journal of Vacuum Science & Technology A, **16**: 2785–2790, 1998.
[24] J. Pla et al., Thin Solid Films, **405**: 248–255, 2002.
[25] M. Farrokh-Baroughi et al., IEEE Electron Device Letters, **28**: 575–577, 2007.
[26] R. Shimokawa et al., Japanese Journal of Applied Physics, **46**: 7612–7618, 2007.
[27] J. Damon-Lacoste et al., 35th IEEE Photovoltaic Specialists Conference (PVSC), 001352–001357, 2010.
[8] Y. Veschetti et al., Thin Solid Films, **511-512**: 543–547, 2006.
[11] S. De Wolf et al., Applied Physics Letters, **90**: 042111, 2007.
[28] H. Fujiwara et al., Applied Physics Letters, **90**: 013503–013503–3, 2007.
[29] M. Kambara et al., Journal of Applied Physics, **99**: 074901, 2006.
[5] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells*. PhD thesis. Ecole Polytechnique, France, May 2011.
[10] J. Damon-Lacoste et al., Journal of Applied Physics, **105**: 063712, 2009.
[30] M. Labrune et al., Thin Solid Films, **518**: 2528–2530, 2010.
[31] M. Moreno et al., EPJ Photovoltaics, **1**: 6, 2010.
[32] R. Cariou et al., Solar Energy Materials and Solar Cells, **95**: 2260–2263, 2011.
[33] H.G. El Gohary et al., 34th IEEE Photovoltaic Specialists Conference (PVSC), 001331–001334, 2009.
[34] A. Mosleh et al., 39th IEEE Photovoltaic Specialists Conference (PVSC), 2646–2650, 2013.
[35] D. Shahrjerdi et al., Journal of Electronic Materials, **41**: 494–497, 2012.
[36] B. Hekmatshoar et al., Applied Physics Letters, **101**: 103906, 2012.

3.3 Surface cleaning prior to epitaxial growth

Achieving an atomically clean and well-ordered wafer surface is a crucial step to enable propagation of the crystal structure from the substrate to the growing layer (epitaxial growth). During this PhD thesis, all the silicon substrates used were (100)-oriented. Indeed, epitaxial growth and regrowth are known to be more difficult on (111)-oriented silicon surfaces[5,37–39]. Both experimental results and molecular dynamics simulations show that a temperature of few hundred degrees higher is needed to achieve good epitaxial growth on (111) compared to (100), on which it can occur close to room temperature. For (100), diffusion constant can be expressed as $D \simeq (1.31.10^3) e^{-0.54/k_B T} cm^2/s$[40]. Epitaxial growth on (111) has a higher propensity of growing stacking fault. Such an orientation sensitivity, especially at low temperature, might be explained by a geometrical argument: in the (100) case, each Si atom in the growing planes has to form two covalent bonds with the underneath plane, to be incorporated in the lattice, while Si atoms incorporated on (111) surfaces need to form only one bond with the underneath plane (and three with the upper planes), which gives more degrees of freedom for an amorphous growth.

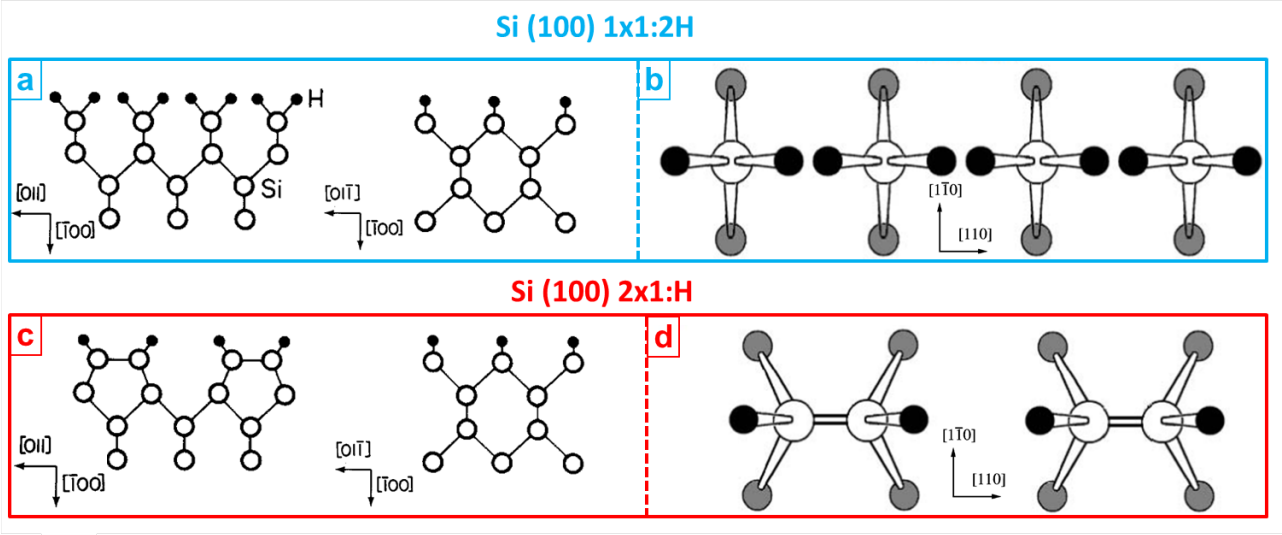


Fig. 3.2 – a), c) Cross sections and b), d) top views diagrams of c-Si (100) hydrogen passivated surface. a) and b) show Si(100) 1×1:2H dihydride surface. c) and d) show Si (100) 2×1:H reconstructed surface. Arrows show crystal orientation. Adapted from [34, 41].

Crystalline silicon, with its diamond lattice structure, forms four covalent bonds to its nearest neighbors. Thus, a clean ideal and unpassivated c-Si(100) surface terminates with two dangling bonds. However this configuration is unstable and the surface reconstructs itself into a lower energy per atom configuration that differs from the bulk. Few monolayers can be modified and the surface typically forms the so called (2×1) periodic structure (dimerization process): two dangling bonds of neighbors Si atoms merge into one covalent bond. Depending on the chemical/physical treatment applied on this surface, the remaining dangling bonds may be passivated by H atoms: this results in a so called monohydride configuration, as shown on Fig. 3.2c-d). There are a lot of studies focusing on

[5] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells*. PhD thesis. Ecole Polytechnique, France, May 2011.
[37] L. Csepregi et al., Journal of Applied Physics, **49**: 3906–3911, 1978.
[38] B.E. Weir et al., Applied Physics Letters, **59**: 204–206, 1991.
[39] U.K. Das et al., Applied Physics Letters, **92**: 063504, 2008.
[40] C. Roland et al., Physical Review B, **46**: 13428–13436, 1992.

Si(100) surface reconstruction under various conditions[41–44]; both experimental and simulation results show that hydrogen terminated surfaces are mostly (2 × 1) monohydride around 400°C, while room temperature H-passivated surfaces may be in 1x1 dihydride configuration, as shown on Fig. 3.2a-b). From simulations, it appears that monohydride surface is more apt for epitaxy, since activation energy for Si adatom diffusion on a dihydride surface (isotropic, 2.7eV) is significantly higher than either the bare (0.6 and 1eV, parallel and perpendicular to the dimer row) or monohydride surfaces (1.5 and 1.7eV, parallel and perpendicular to the dimer row)[45,46].

For several decades now, very high temperature annealing under ultra-high vacuum conditions has been used to produce such ideal surfaces: after an ex-situ cleaning step (e.g. acetone in ultrasonic bath), the wafer is heated and maintained at 900°C for sufficient time for out-gassing, and then a rapid (1min) plateau at 1200-1250°C is applied. This can produce nearly ideal surface as confirmed by Auger-electron spectra and clear spotty (2 × 1) RHEED (reflection high-energy electron diffraction) patterns[47]. However, these are conditions very different from the low temperature PECVD: neither ultra-high vacuum nor high temperature have been used in this doctoral work. Indeed, detailed in-situ surface analysis in our experimental conditions would be required to investigate surface state before epitaxial growth. Thus, while a detailed study at the atomic scale was beyond the scope of this work, a low temperature process for native oxide removal prior to epitaxial growth was nevertheless a crucial step.

3.3.1 Wet chemical cleaning

The importance of clean silicon substrate surfaces has been recognized by the semiconductor industry since the early 50's. A thin (∼1.5 nm) native oxide layer is always present on the surface of silicon wafers where various impurities can be found: traces of metals, particles, organic compounds, etc. This amorphous SiO_2 surface layer prevents from low temperature epitaxial growth. Since oxide removal by ultra-high vacuum and high temperatures is not very attractive from an industrial point of view, alternative wafer cleaning chemistries have been developed. There is a plethora of chemical mixtures and processes for c-Si surface cleaning, depending on the required surface state and the targeted contaminants removal. Most widely used solutions are: i) Diluted (1-5%) hydrofluoric acid (HF), which etches very efficiently SiO_2 at room temperature but is less efficient on metals and organic contaminant ii) The so-called PIRANHA solution, H_2SO_4:H_2O_2 3:1 at T∼ 140°C, which has a strong action on organic contaminants and iii) the RCA cleaning, composed of the SC1 step NH_4OH:H_2O_2(30%):H_2O 1:1:5 at 80°C for particles removal and the SC2 step HCL(37%):H_2O_2(30%):H_2 1:1:6 for metals removal. Particles removal can also be addressed using ultrasonic treatments; the reader can find more details about silicon cleaning technology evolution in the review paper published by Kern[48].

During this doctoral work, for the chemical cleaning part, we have mainly used a 5% hydrofluoric acid (HF) solution (sometimes combined with PIRANHA solution). HF is extremely corrosive and difficult to handle, but well known for its ability to dissolve glass by reacting with SiO_2. In the late 1980's, Yablonovitch et al.[49] have also demonstrated that HF treated silicon surfaces are very inactive from an electrical point of view: they reported surface recombination velocities as low as 0.25 cm/s on (111)-oriented Si. The explanation for this is that HF etching of native oxide results in H-terminated surface with virtually no dangling bonds, by forming gaseous or water-soluble silicon fluorides. As a matter of fact, by covalently satisfying all surface bonds, the surface states are shifted out of the

[41] F. Stucki et al., Solid State Communications, **47**: 795–801, 1983.
[42] J.J. Boland., Phys. Rev. Lett., **67**: 1539–1542, 1991.
[43] Y. Wang et al., Phys. Rev. B, **48**: 1678–1688, 1993.
[44] K. Yokoyama et al., Jpn. J. Appl. Phys., **39**: L113, 2000.
[45] S. Jeong et al., Physical Review Letters, **79**: 4425–4428, 1997.
[46] J. Nara et al., Phys. Rev. Lett., **79**: 4421–4424, 1997.
[47] J.W. Rabalais et al., Phys. Rev. B, **53**: 10781–10792, 1996.
[48] W. Kern., J. Electrochem. Soc., **137**: 1887–1892, 1990.
[49] E. Yablonovitch et al., Phys. Rev. Lett., **57**: 249–252, 1986.

band gap. Despite the fact that Si-F bond strength is far greater than the binding energy of Si-H ($\sim$ 6.0 eV vs $\sim$ 3.5 eV), both experimental results and quantum-chemical calculations[50,51] indicate that reactions leading to H-terminated surfaces are more energetically accessible. This H-terminated Si surface, as confirmed by the experimental results presented in this chapter, is favorable for subsequent epitaxial growth.

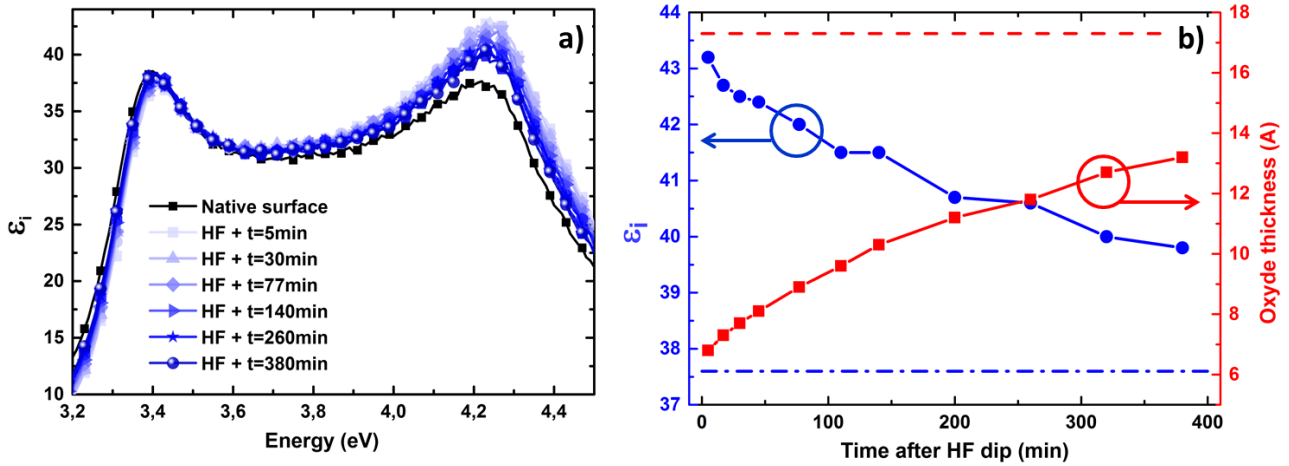


Fig. 3.3 – Time evolution of the imaginary part of the pseudo-dielectric function ε_i of a c-Si (100) wafer after 30s 5%HF dip, as obtained by spectroscopic ellipsometry measurements (in air at RT). a) ε_i measured at various times after HF-dip. b) Maximum of ε_i at 4.2 eV (left axis, circles) and fitted surface oxide thickness (right axis, squares) as function of time.

However, this excellent Si-H passivation of the surface is not stable: native oxide regrowth happens if the sample is kept in air or DI water. This process requires the presence of both oxygen and water. The growth rate of the native oxide can be decreased by lowering moisture concentration, if the c-Si is air-exposed, or by lowering dissolved oxygen concentration, if the sample is in DI water[52]. The kinetics of this reaction also depends on roughness and surface orientation (e.g. (111) has a slower oxidation rate compared to (100))[53]. While the first oxide monolayer may form very rapidly after chemical cleaning if there is air-exposure, it is generally admitted that almost no change in oxide thickness happens during the first hour or so. During our experimental work, due to the sample transfer between the chemical fume-hood and the deposition reactor, there were always a few minutes of air exposure before the pumping step. In addition, there was no specific air-control system, since the plasma reactor was not located in a clean room. Also, observing a hydrophobic surface cannot be used as an accurate indicator of oxide-free surface, since oxidation process may start by oxidization of the Si back bonds while keeping the surface hydrogen terminated. And since this process is catalyzed by water, we did not use DI water rinsing after the HF-dip, but rather nitrogen blowing to dry the sample[1].

Thus to gain some insight on this oxidation process in our experimental conditions, we have performed spectroscopic ellipsometry measurements to monitor the c-Si(100) surface evolution after HF-dip. Fig.3.3-a) shows the imaginary part of pseudo-dielectric function (ε_i) measured before and after HF-dip, at various times. A clear increase of the maximum around 4.2 eV is observed right after HF-dip compared to out-of-the-box c-Si wafer surface (black squares), and then a slow decrease happens. The penetration depth at 4.2 eV being around 5 nm for c-Si, this is a good energy range to

[50] T. Takahagi et al., Journal of Applied Physics, **64**: 3516–3521, 1988.
[51] G.W. Trucks et al., Physical Review Letters, **65**: 504–507, 1990.
[52] M. Morita et al., Journal of Applied Physics, **68**: 1272–1281, 1990.
[53] W Henrion et al., Applied Surface Science, **202**: 199–205, 2002.
[1] Be sure that your nitrogen gas line has the required purity level. Few times during this thesis, the failure in passivation or epitaxial growth was linked to the N_2 line contaminated ... with oil.

probe surface changes. Consequently we have plotted the amplitude of the pseudo-dielectric function 4.2 eV maximum (left axis, circles) as a function of time on Fig.3.3-b). Time 0 corresponds to the first measurement ∼2 min after the HF-dip. The decrease of ε_i is correlated to an increase in the surface oxide thickness as deduced from modeling the experimental data using DeltaPsi2 software[2] (right axis, squares). One can see that right after HF, already 6-7 Å of oxide are detected by this technique; then the following thickness increase is well fitted using the formula $y = a + \sqrt{b \times t}$, which can be linked to some oxygen diffusion phenomenon from the surface[3]. Recovering the initial native oxide can take days; however with respect to epitaxial growth or passivation quality, the air-exposure time after HF-dip and before pumping in the reactor should clearly be minimized. As we will see in this chapter, this 6-7 Å surface oxide grown in the first minute and which creates an unperfect wafer interface, does not prevent from good epitaxial growth nor from efficient passivation. Possible explanations for this could be a non-continuous SiO_2 surface coverage, or also an etching effect of the plasma removing partly this oxide at the beginning of the growth. Also, probing such a 5Å thick layer is close to the precision limit of our experimental ellipsometry set-up.

3.3.2 Dry plasma cleaning

HF is already widely used by the semiconductor industry. However, regarding cost and safety issues (and environment footprint), switching from a wet chemical process to a dry plasma step can be attractive. Plasma etching is indeed a well-known and important field of plasma physics; a lot of research papers can be found on this topic, and many industrial processes, e.g. in microelectronics, are based on plasma etching. Etching may occur when reactive species formed by the plasma and the atoms from a surface react to form a volatile compound. Since many inorganic halides are volatile in the temperature and pressure range compatible with silicon process steps, halogen-bearing gases are widely employed for plasma etching; they may be used in mixtures with O_2 to increase the etching rate. A comprehensive review on the design of plasma etchants can be found in the study published by Flamm and Donnelly[54]. It is well known that both Si and SiO_2 can be etched by plasma, and a vast majority of the commonly used gases are based on fluorine: CF_4, SF_6, XeF_2, F_2, etc. Looking more specifically at SiO_2 etching, it is generally admitted that F atoms are mainly responsible for this effect[55], SiF_4 and O_2 being the main reaction products. It was also proven that increased reaction rates are obtained if the surface is exposed to ion bombardment[56].

At LPICM, SiF_4 gas was originally used in combination with Ar and H_2 (see R. Brenot's PhD thesis[57]) to deposit high quality microcrystalline silicon layers[58]. However, the possibility of using SiF_4 for silicon oxide etching was investigated more recently: Moreno et al. have shown that dry plasma cleaning by SiF_4 around 200°C can replace the SiO_2 HF etching step in the heterojunction process flow[59]. They have exposed a silicon substrate, covered by native oxide, to various RF-PECVD SiF_4 plasma conditions while monitoring the surface evolution by in-situ real time spectroscopic ellipsometry (RTSE). For crystalline silicon, the second peak of the imaginary part of the pseudo-dielectric function, which appears at 4.2 eV, is indeed very sensitive to the surface state (both roughness and oxide). A maximum for this peak amplitude was found after ∼300 s of pure SiF_4 plasma, corresponding to a minimum oxide thickness and surface roughness. An additional 30 s H_2 plasma, to remove remaining fluorine atoms and produce a better H-terminated surface, followed by the deposition of an a-Si:H layer, enabled to reach high minority carrier lifetime (∼ 1.5 ms) and a low surface recombi-

[2] Software developed by Horiba Jobin Yvon.

[3] Not operating in a clean room, this kinetics fluctuates with weather, e.g. during Palaiseau's monsoon season.

[54] D.L. Flamm et al., Plasma Chem Plasma Process, **1**: 317–363, 1981.

[55] D.L. Flamm et al., Journal of Applied Physics, **50**: 6211–6213, 1979.

[56] J.W. Coburn et al., Journal of Applied Physics, **50**: 3189–3196, 1979.

[57] R. Brenot. *Corrélation entre mode de croissance et propriétés de transport du silicium microcristallin, établie par réflectométrie micro-onde et ellipsométrie.* PhD thesis. Ecole Polytechnique, France, 2000.

[58] J.-C. Dornstetter et al., IEEE Journal of Photovoltaics, **3**: 581–586, 2013.

[59] M. Moreno et al., Solar Energy Materials and Solar Cells, **94**: 402–405, 2010.

nation velocity (9 cm/s). Thus, this experiment was the proof that SiO_2 can be properly etched by SiF_4 without damaging the surface. In addition, it was also shown at LPICM, that this SiF_4 etching step was compatible with subsequent epitaxial growth[5,31] and that it enabled to tune the interface composition and porosity[60]. From late 2012, a new PECVD deposition cluster tool (industrial-like), purchased by Total Company in the framework of LPICM/Total Joint Research Team - PVSIXT, has been available for depositions. One of the 6 PECVD chambers was dedicated to the study of low temperature epitaxial growth, with the help of a Woollam in-situ ellipsometer enabling full spectrum ($\sim$ [0.8-6] eV) measurement every second. Consequently, after some developments, the transfer of the SiF_4 cleaning recipe from the old home-built ARCAM reactor[61] to the this new cluster tool was successfully achieved[4].

A c-Si wafer was loaded into the chamber, and a 20 min waiting time for thermalization and outgassing was necessary to reach a base vacuum around 5.10^{-7} mbar. We found the following optimum plasma conditions for efficient oxide removal: 20 sccm of SiF_4, 250 mTorr and $\sim$ 0.15 W/cm^2 for 190 s at a substrate temperature of 200°C. The pressure was raised at 750 mTorr before switching the power on, and then rapidly decreased to 250 mTorr. This resulted in a $\sim$ 1 min transition regime before having stabilized plasma conditions. A relatively high V_{dc} ($\sim$ -60 V) was observed during this transition, and after 1min, a V_{dc} around -20 V was measured. This SiF_4 plasma cleaning step could be monitored by in-situ real time spectroscopic ellipsometry as shown on Fig.3.4. The time evolution of the imaginary part of the pseudo-dielectric function (ε_i), measured at 4.2 eV, is represented by the blue curve in a). The value of 4.2 eV corresponds to the energy position of the second characteristic peak of crystalline silicon, which is very sensitive to the surface, since the absorption depth at this specific energy is $\sim$ 4-5 nm.

Four sequential time steps can be distinguished: i) the surface of out-of-the-box c-Si wafer before any treatment (grey shade) ii) plasma cleaning of native oxide (red shade) iii) the c-Si oxide-free surface, measured with plasma off (grey shade) and iv) the begin of the epitaxial growth (green shade). During the first step, before plasma ignition, ε_i is stable around 43: it corresponds to c-Si surface with its native oxide, measured under vacuum. Then, after a short transition drop, there is a clear increase of ε_i up to $\sim$ 49, which is linked to the etching of native oxide. Ideally, one should stop this etching process when the maximum amplitude of ε_i is reached, because further exposure of bare c-Si surface to SiF_4 plasma can create some roughness. In this particular case, the etching step was a little bit too long, and we see that ε_i starts to decrease after reaching a maximum, as the result of surface roughening. In the step iii) the plasma is off, the chamber is under vacuum, and we see that ε_i remains high and relatively constant: it corresponds to a stable oxide free surface. The last step corresponds to the epitaxial growth: after a drop of ε_i during the plasma ignition and stabilization, the imaginary part of the pseudo-dielectric function reaches $\sim$45. The full ellipsometry spectrum measured before (squares, t=2min) and after oxide cleaning (circles, t=9.6min), as well as during epitaxial growth (triangles, t=20.8min), are shown in Fig.3.4-b); the above-mentioned increase of ε_i with surface native oxide etching at 4.2 eV is clearly visible. During epitaxial growth, ε_i amplitude is slightly smaller, compared to the the curve after SiF_4 cleaning: this can be explained by a the combination of some surface roughness and a slightly lower quality of the epitaxial material compared to the FZ c-Si wafer. The other features of the epitaxial curve, namely oscillations in 1-3 eV range and peak amplitude at 3.4 eV, are further discussed in the next session.

[31] M. Moreno et al., EPJ Photovoltaics, **1**: 6, 2010.
[60] M. Moreno et al., Journal of Materials Research, **28**: 1626–1632, 2013.
[61] P. Roca i Cabarrocas., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, **9**: 2331, 1991.
[4] Transferring deposition/etching recipes from the old reactor to the new PECVD cluster took indeed several months.

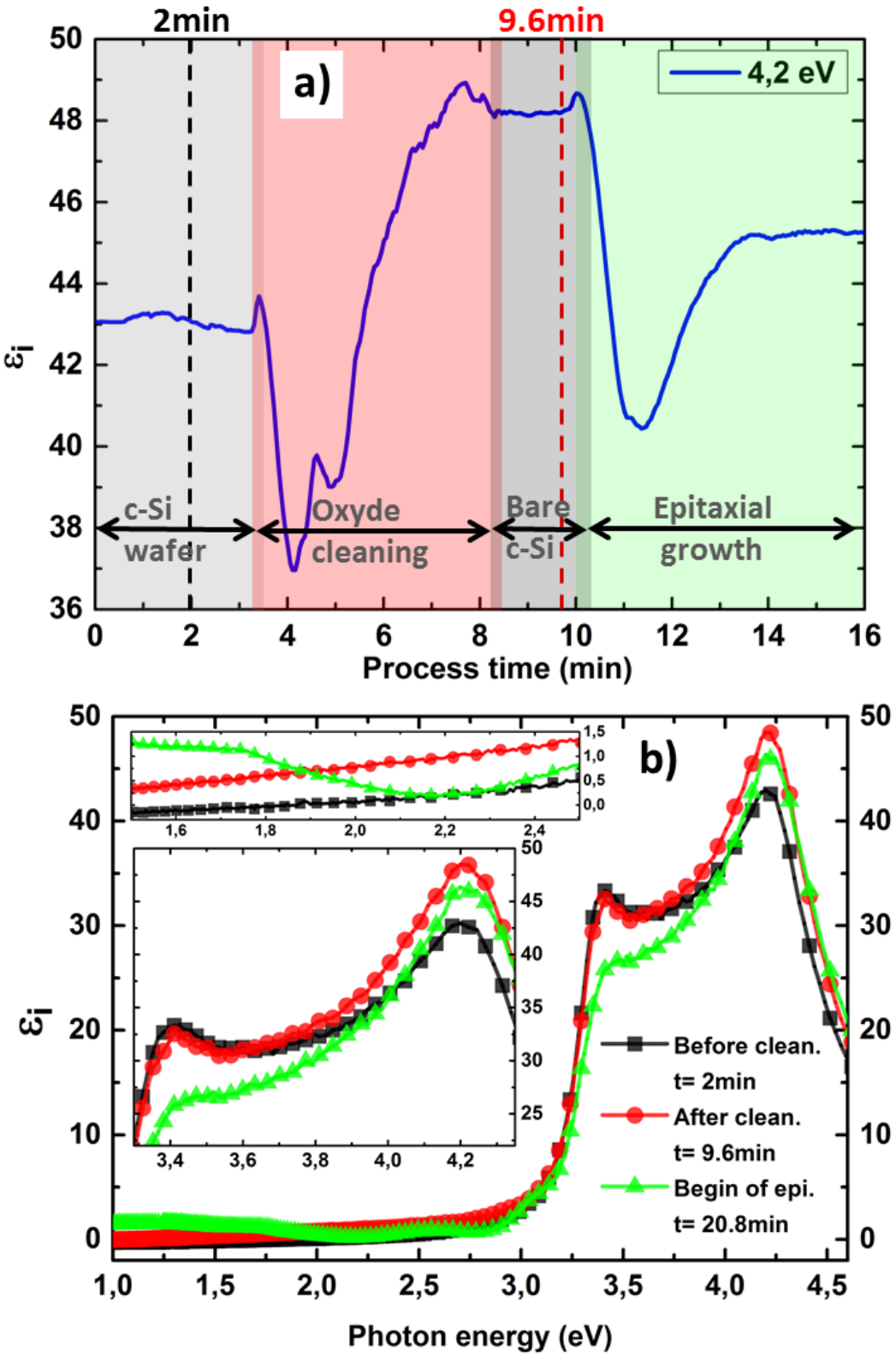


Fig. 3.4 – In-situ real time spectroscopic ellipsometry monitoring of c-Si (100) native oxide cleaning by SiF_4 plasma. a) time evolution of ε_i at 4.2 eV (blue curve) during 4 steps: i) before plasma ignition (native surface - grey shade) ii) during plasma etching (red shade) iii) after plasma etching, with plasma off (grey shade) iv) beginning of epitaxial growth (green shade). The full spectrum in-situ acquisitions before and after the SiF_4 plasma etching step (dash-lines at 2 and 9.6 min) are shown on b), together with ε_i measured during epitaxy (t=20.8 min).

3.4 Properties of LT RF-PECVD epitaxial silicon

3.4.1 Influence of silane dilution

Back in 1987, Nagamine et al.[17] mentioned the important link between gas ratio and material quality. Their experimental conditions were relatively close to ours: PECVD deposition at 250°C on c-Si (100)-oriented substrate from $SiH_4/SiH_2F_2/H_2$ precursors. They were investigating the influence of SiH_2F_2 flux on the crystallinity of the deposited material for a fixed 100 sccm of H_2, 1 sccm of SiH_4 and a total pressure of few Torrs. The material changes were deduced from in-situ RHEED measurements. They could observe a microcrystalline film when using no SiH_2F_2, that is highly diluted SiH_4, and then by increasing SiH_2F_2 to 5 sccm, a perfect monocrystalline film was obtained. A relatively sharp threshold toward amorphous material was observed beyond 10 sccm. This early experiment gave the proof that low temperature epitaxial growth happens at the transition between microcrystalline silicon conditions (high dilution in H_2) and amorphous conditions (less diluted Si precursors), and that a relatively high pressure may be favorable.

More recently, some studies have been published on the influence of SiH_4 dilution in hydrogen, for LT-PECVD epitaxial growth. Mosleh et al.[34], for example, used high resolution cross section TEM to see the change in crystallinity in ∼20 nm films. Working at 250°C and 500 mTorr, they could observe monocrystal growth for SiH_4/H_2 flux ratio of 2 and 3.3%; and then breakdown into amorphous material, after ∼10 nm of growth, was obtained for a ratio of 5%. Shahrjerdi et al.[35] have performed similar test series but they were using XRD to probe the crystallinity and the strain at the same time. They reported epitaxial growth over a few tens of nm for an SiH_4/H_2 ratio in the range of 10 to 14%, and they have been able to correlate the increase of hydrogen content in the epi-layer, for low SiH_4/H_2 ratio, with the increase of compressive strain.

During the first part of this PhD thesis work, depositions were mainly performed on the old home-built reactor called ARCAM[61]. With this set up, the deposition of a series of samples with various silane dilutions gave results consistent with the work of Nagamine et al.[17]: starting from a low silane flux, for a fixed H_2 flow rate, the deposited material was microcrystalline, whereas at high silane flux, thus higher SiH_4/H_2 ratio, it resulted in amorphous material[62]. The epitaxial conditions were found at the transition between these two materials, for a SiH_4/H_2 ratio of ∼10 to 15 %. Those numbers are in good agreement with the ones published by IBM[35]. As for the differences observed with the values reported by Mosleh et al.[34], it may be explained by experimental set-up variations (reactor geometry, mass flow controllers calibration, etc.). This argument seems to be confirmed by the experiments performed on the new PECVD cluster tool used mainly during the last year of this doctoral thesis work. Once again, a series of samples with various silane fluxes was deposited, in order to find back the epitaxial conditions on this new reactor, using the following conditions: - a constant total pressure of 2.3 Torr - a fixed H_2 flux of 200 sccm - a substrate temperature of 190°C - and a power density of 100 mW/cm^2. The depositions were performed on (100)-oriented c-Si wafers cleaned by HF-dip. The 900s exposure to the plasma resulted in a film thickness in the range of 40 to 200 nm depending on the silane dilution. The corresponding experimental results characterized by ex-situ ellipsometry and Raman spectroscopy (λ=473nm) are displayed on Fig.3.5. The imaginary part of the pseudo-dielectric function is displayed on a), for the samples with the following SiH_4 fluxes: 1 sccm (squares), 4 sccm (circles) and 7 sccm (triangles). The Raman spectra measured on the same three samples are shown in the inset of Fig.3.5-a). The featureless shape of ε_i for a SiH_4 flow rate of 7 sccm combined with the broad peak centered at 480 cm^{-1} measured by Raman is a direct confirmation of the amorphous state of this layer. The sample deposited with 1 sccm of silane has some visible peaks

[17] K. Nagamine et al., Jpn. J. Appl. Phys., **26**: L951, 1987.
[34] A. Mosleh et al., 39th IEEE Photovoltaic Specialists Conference (PVSC), 2646–2650, 2013.
[35] D. Shahrjerdi et al., Journal of Electronic Materials, **41**: 494–497, 2012.
[61] P. Roca i Cabarrocas., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, **9**: 2331, 1991.
[62] P. Roca i Cabarrocas et al., Journal of Non-Crystalline Solids, **358**: 2000–2003, 2012.

in ε_i at 3.4 and 4.2 eV, however the low amplitude compared to the expected values for crystalline silicon[5] is characteristic of a microcrystalline material. Last but not least, the sample obtained for a SiH_4 flow rate of 4 sccm with a high ε_i peak amplitude corresponds to a monocrystalline layer, which exhibits also a sharp Raman peak around 520 cm^{-1}.

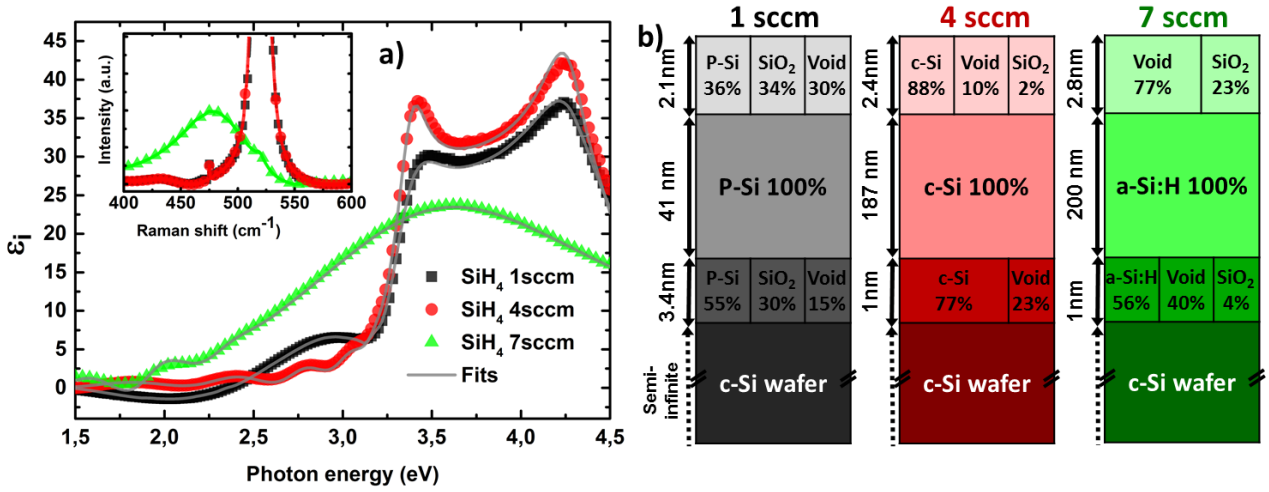


Fig. 3.5 – Influence of silane dilution, in SiH_4/H_2 plasmas, on layer crystallinity, monitored by ex-situ ellipsometry and Raman spectroscopy. The ε_i of layers deposited with a SiH_4 flow rate of 1 sccm (squares), 4 sccm (circles) and 7 sccm (triangles) are shown on graph a) together with the fits (grey lines) to the optical models described on b).

Further proof of the material crystallinity can be obtained by fitting the ellipsometry data with optical models, as shown on Fig.3.5-b). The dielectric functions corresponding to the bulk layer stack was fitted using the dispersion curve of a large grain poly-Si[63] for the 1 sccm sample, the dispersion curve of monocrystalline silicon[64] for the 4 sccm and a Tauc-Lorentz dispersion formula for the 7 sccm amorphous silicon layer[65]. An interface and a surface layer were added, by combining those materials with a void fraction and some silicon oxide using the Bruggeman effective approximation theory[66]. The top layer is useful to model the roughness and oxide present on the surface and the first layer above the wafer describes the imperfect interface. Qualitatively, the amplitude of the oscillations visible in the 1.5 to 3 eV range is linked to the composition of this wafer interface layer, and the period of those oscillations is related to the film thickness. The grey line curves on Fig.3.5-a) are the fitting results corresponding to the optical models described on Fig.3.5-b). The free parameters were the thicknesses and the material fraction in each layer. We found an excellent agreement between data and fits (figure of merit χ^2<0.5): the 1 sccm sample was perfectly fitted by 41 nm of bulk poly-Silicon, the 4 sccm by 187 nm of 100% monocrystalline material and the 7 sccm by 200 nm of 100% a-Si:H. The fitting uncertainties are typically a fraction of Å for the thicknesses and about a percent for the compositions. The composition of the top and bottom interface layers will be discussed later in this manuscript (see sections dealing with surface analysis, and PECVD epi-layer detachment in the next Chapter). The optimized deposition conditions for LTE in our PECVD cluster tool as well as for the home-built PECVD ARCAM reactor[61], are described in the Tab.3.1. These two reactors are different in several ways: i) ARCAM has plasma confinement boxes, an asymmetry factor around 2 for the electrodes, hot-wall heating system. ii) The PECVD cluster chambers are more symmetrical, have no confinement boxes, does not have a uniform heating system, but it is equipped with gas shower head

[5] $\varepsilon_i \sim 37$ at 3.4 eV and 47 at 4.2 eV for a perfectly flat and oxide-free surface.

[63] G.E. Jr Jellion et al., Applied Physics Letters, **62**: 3348–3350, 1993.
[64] D.E. Aspnes et al., Physical Review B, **27**: 985, 1983.
[65] G.E. Jellison Jr. et al., Thin Solid Films, **377-378**: 68–73, 2000.
[66] D.A.G. Bruggeman., Annalen der Physik, **416**: 636–664, 1935.

	Temp. (°C)	Pressure (Torr)	SiH_4 (sccm)	H_2 (sccm)	Power (mW/cm^2)	Electrode gap (mm)
Cluster (i)epi-Si	190	2.3	4	200	40 - 100	22
ARCAM (i)epi-Si	175	2.2	34	500	40 - 60	17

Tab. 3.1 – Optimized deposition conditions of intrinsic low temperature PECVD epitaxial growth in the two reactors used during this doctoral thesis.

and view port for ellipsometry.

The complete experimental series of silane dilution is shown on Fig.3.6-a). On the left axis, one can read the amplitude of ε_i at 3.4 (triangles) and 4.2 eV (circles), as measured by ex-situ ellipsometry, as a function of the silane flow rate. The top axis is the corresponding $SiH_4/(H_2+SiH_4)$ ratio in %; in theory $SiH_4/(H_2+SiH_4)$ is a better definition for the dilution compared to SiH_4/H_2. However, in our plasma conditions consisting of highly diluted silane in H_2, these two ratios give sensibly the same result, and thus we will use SiH_4/H_2 when referring to the dilution. The Raman FWHM peak as a function of the silane dilution (first right axis - squares) as well as the deposition rate (second right axis - diamonds), deduced from ellipsometry fitting, are also presented Fig.3.6-a). Without the need of using a detailed modeling, the maximum in the amplitude of ε_i curves gives a good idea of the silane window for epitaxial growth: 3 to 5 sccm, that is SiH_4/H_2 from 1.5 to 2.5%. The Raman FWHM for the crystalline silicon peak provides additional information: the more defective the crystalline material is, the broader the peak. Consequently, the best quality of epitaxial layers is obtained here for 2 to 2.5% silane to hydrogen dilution. The relatively abrupt transition toward amorphous material at 7 sccm is also correlated with a drastic change in the chemical composition of the layer: the comparison of hydrogen depth profile by SIMS analysis (see Fig.3.6-b)) in an epitaxial and an amorphous layer reveals more than one order of magnitude higher hydrogen content in the latter.

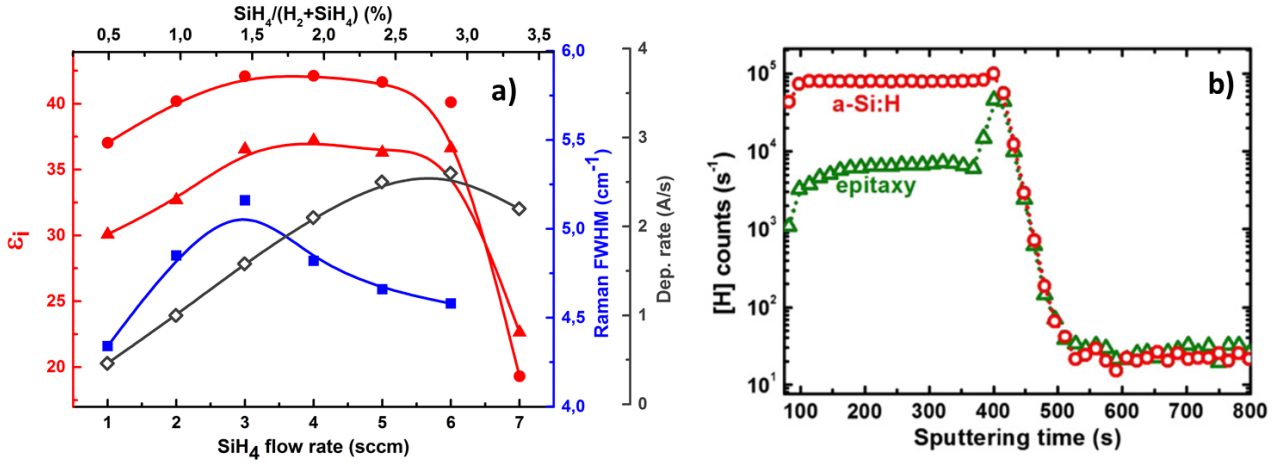


Fig. 3.6 – Influence of silane dilution, in SiH_4/H_2 plasma, on layer crystallinity as monitored by ex-situ ellipsometry and Raman spectroscopy. a) ε_i at 3.4 eV (red triangles) and 4.2 eV (red circles), versus SiH_4 flow rate. The first right axis shows the Raman FWHM (blue squares) and the second right axis (black diamonds) corresponds to the deposition rates deduced from ellipsometry fitting. b) SIMS profile for hydrogen of an epitaxial (triangles) and an amorphous (circles) layers[62].

Thus, for this new experimental set up, an epitaxial window has been found, as expected, at the transition between microcrystalline and amorphous material, but this time the optimum SiH_4/H_2 was around 1.5-2.5%. Interestingly enough, this series of samples was co-deposited on glass substrates. We found that the transition to amorphous material happens at lower flux on Corning glass (Cg) substrates: if the optimum silane dilution conditions for epitaxy are used for a co-deposition on c-Si

wafer and glass substrates, the material deposited on c-Si is monocrystalline, whereas the one deposited on glass is amorphous (or polymorphous, but not microcrystalline)[62].

3.4.2 Surface characterizations

Using the above mentioned optimum silane dilution for this epitaxial growth, we investigated the possibility of growing thick layers (typically few microns). It is well-known that, at least in the world of MBE epitaxial growth, there is a critical thickness above which the epitaxial growth becomes highly defective and eventually breaks down into amorphous material; this critical thickness h_{epi} increases exponentially with the increase of temperature. And so, even if no temperature cut-off for silicon epitaxy on silicon has been reported, Eaglesham et al. have shown that h_{epi} is as low as 10-30 Å at room temperature and does not exceed 20 nm at 200°C[3]. In addition, they demonstrated[67] that the presence of hydrogen reduces even more this h_{epi}, by the indirect effect of surface roughening. Obviously, those limits do not apply for low temperature RF-PECVD epitaxial growth. Indeed, we have already reported a 187 nm epi-Si on c-Si grown at 190°C in the previous section. However, the growth mechanism is most likely completely different: in PECVD environment, the pressure is several orders of magnitude higher, there are radicals and ions with a broad distribution of energy impinging onto the surface, hydrogen is used as the carrier gas, there are some high order clusters and nanoparticles Si_xH_y formed in the plasma phase, etc[68].

So we decided to deposit layers of few microns thick to see whether an upper limit h_{epi} could be identified. Indeed, with our current deposition rate of ∼0.7 μm/h, all we needed was a little bit of patience, since few hours was necessary to reach the thickness of few microns. Using real time in-situ ellipsometry, we recorded the ε_i function during epitaxial growth. The resulting 3D data are displayed on Fig.3.7. The two bottom axes are the photon energy and the deposition time, and the z-axis is ε_i. The step in the 3.4 and 4.2 eV peaks close to the time origin corresponds to the transition between the wafer surface and the beginning of the growth. This could be explained by a slightly defective interface and island type growth, but also by some local temperature increase on the growing surface (in [330-400]°C temperature range, ε_i at 4.2eV reaches 38-40). Another interesting feature is the oscillations in the low energy range of the spectrum [1.5-2.5] eV: those are the thickness interferences. Overall, the important result here is that the two characteristic crystalline silicon peaks remain well defined with a high amplitude. This is the proof of a sustained crystalline growth, which in this example reaches a thickness of 1 μm.

We also did depositions of even thicker layers. The results are shown on Fig.3.8, where a) shows the ellipsometry spectrum measured on such a thick layer, and b) a cross section SEM picture of the same epi-layer. The ε_i experimental points are the blue circles on a) and the fit, corresponding to the optical model shown in the inset, is the red curve. The excellent match between the measured data and the fitting curve, especially in the low energy range where oscillations are visible, gives credit to the model: in this example we deposited 3.4 μm of 100% monocrystalline material. The fit reveals a top layer of 2 nm being composed of 77% of c-Si, 20% of void and 3% of SiO_2 and an interface layer of 1 nm composed of 40% c-Si, 30% SiO_2 and 30% void. The question whether the fitted composition of this buried interface is realistic will be addressed later on, however we can already qualitatively see that a highly defective and probably porous layer of 1 nm is detected at the interface. The material was also examined by SEM: the cross section picture of the epi-Si layer is displayed on Fig.3.8-b). The wafer and the epi-layer are clearly visible, and the epi-Si looks compact, with no specific defects detected with this imaging technique. The thickness measured on the SEM picture is around 3.3μm, which is very close to that found by ellipsometry; the small discrepancy may be linked to some thickness variation over the sample area.

[3] D.J. Eaglesham et al., Physical Review Letters, **65**: 1227, 1990.
[67] D.J. Eaglesham et al., Journal of Applied Physics, **74**: 6615–6618, 1993.
[68] P. Roca i Cabarrocas et al., MRS Proceedings, **1426**: 319–329, 2012.

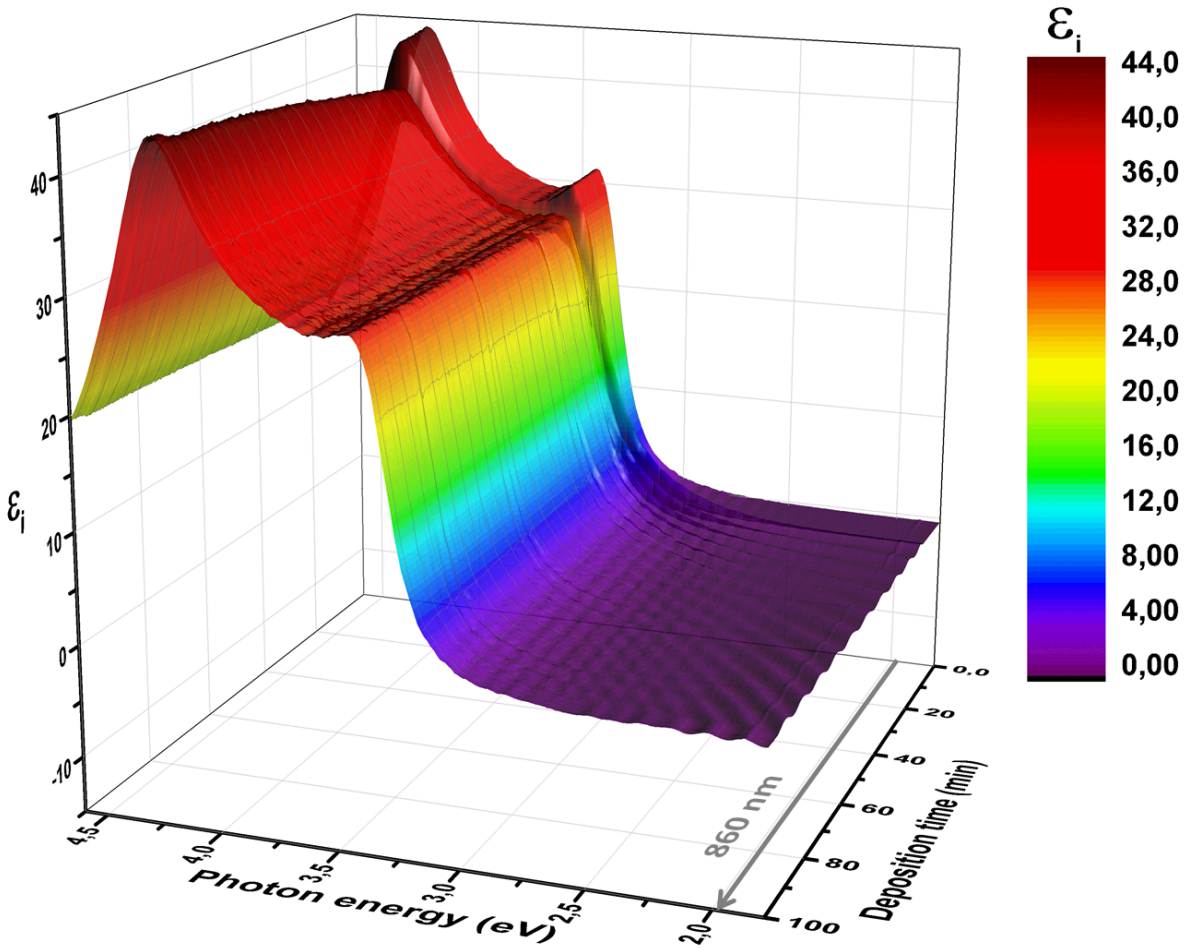


Fig. 3.7 – Time evolution during epitaxial growth of ε_i obtained by real time spectroscopic ellipsometry at the optimum SiH_4/H_2 ratio. The oscillations in 1.5-2.5 eV range are thickness-related interferences fringes. The amplitude of ε_i peaks at 3.4 and 4.2 eV remaining high during deposition is the fingerprint of epitaxial growth. The step in the peak amplitude close to the origin corresponds to the transition between wafer surface and growing film.

The standard sample size used in our reactors is a 4 inch. wafer (∼10.16 cm), although we often work on smaller pieces like 5×5 cm^2 or even 1×1 $inch.^2$. The previously shown 3.4 μm epi-Si sample was deposited on a full 4 inch. wafer, and thus we decided to perform uniformity analysis. Using the mapping option of the ellipsometry software DeltaPsi2, full spectrum acquisitions were measured on this sample on 38 different spots. Each time, the beam, which has an ellipsoidal shape, probes a surface of ∼1×2 mm^2. The 38 spectra were then fitted using the procedure described in the previous section, to extract the bulk thickness of the epi-layer. This thickness is then plotted on a color map, as shown on Fig.3.9-a). X and Y are the coordinates with respect to the center of the sample, the visible points are the measurement spots and the shades of grey are the fitted layer thicknesses spanning from 3.27 μm to 3.5 μm. The average thickness is 3.37 μm and uniformity[6] is 3.5%. This is a relatively good uniformity, despite a 4 inch substrate covering roughly 50% of electrode surface and no showerhead electrode for the gas injection[69]. We do not have a clear explanation for this thickness pattern, but it is most likely linked to gas path flow, and the electrodes shape.

A series of samples of various thicknesses was deposited, in order to study the surface roughness

[6]The formula used in DeltaPsi2 software for the uniformity is: (Max-Min)/(Max+Min).

[69]L. Sansonnens et al., Plasma Sources Science and Technology, **9**: 205–209, 2000.

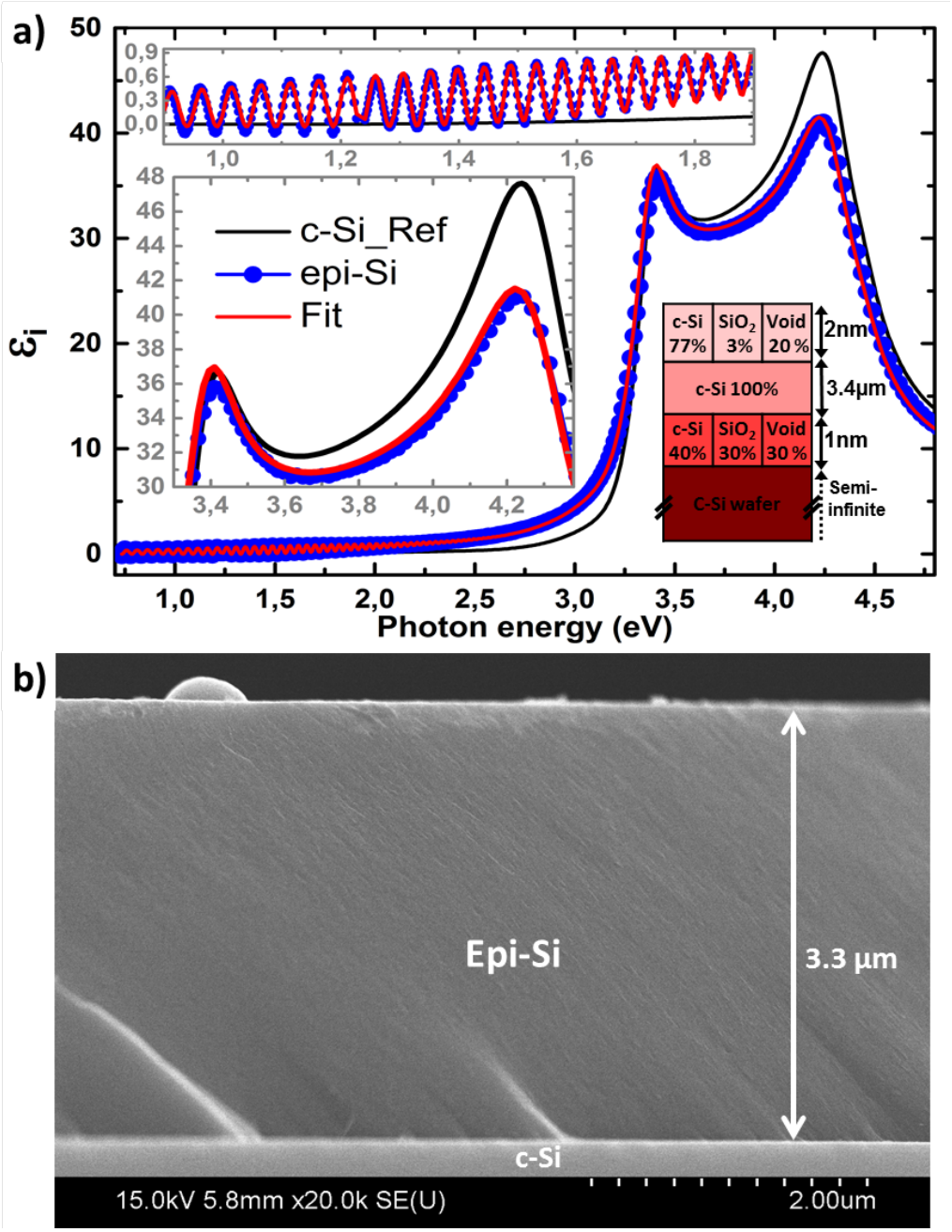


Fig. 3.8 – a) Ex-situ ellipsometry spectrum of a 3.4 μm low temperature epitaxial silicon on a c-Si wafer (blue circles). The epitaxial layer was deposited by RF-PECVD from SiH_4/H_2 plasma at 2.3 Torr. The red curve is the fitting result obtained with the multilayer optical model described in the inset, and reference c-Si ε_i curve is given in black. b) Cross section SEM picture of the same sample.

evolution with thickness. No critical thickness was observed up to ~6 μm, and we were mostly limited by the deposition rate to go beyond this value, since no depositions were allowed at night. Fig.3.9-b) shows the RMS roughness deduced from AFM scan over a 2×2 μm^2 surface. As a reference, the measured roughness of the out-of-the-box c-Si wafer is represented by a black circle on the graph. One can see that the roughness remains below 3 nm for all samples, and no clear trend can be detected. Still, the lowest roughness is observed for the smallest epitaxial thickness. The change in roughness is most likely related to small changes of the epitaxial quality due to some fluctuations in the experimental conditions. From the inset showing the 3D surface of the c-Si surface, some hill shape structures

can be recognized. While it is not reasonable to draw conclusions on the growth mechanism from a simple surface analysis, the pattern observed here, and also on many other PECVD epitaxial samples, is probably the signature of an island growth mode, as reported by Rosenblad et al.[23].

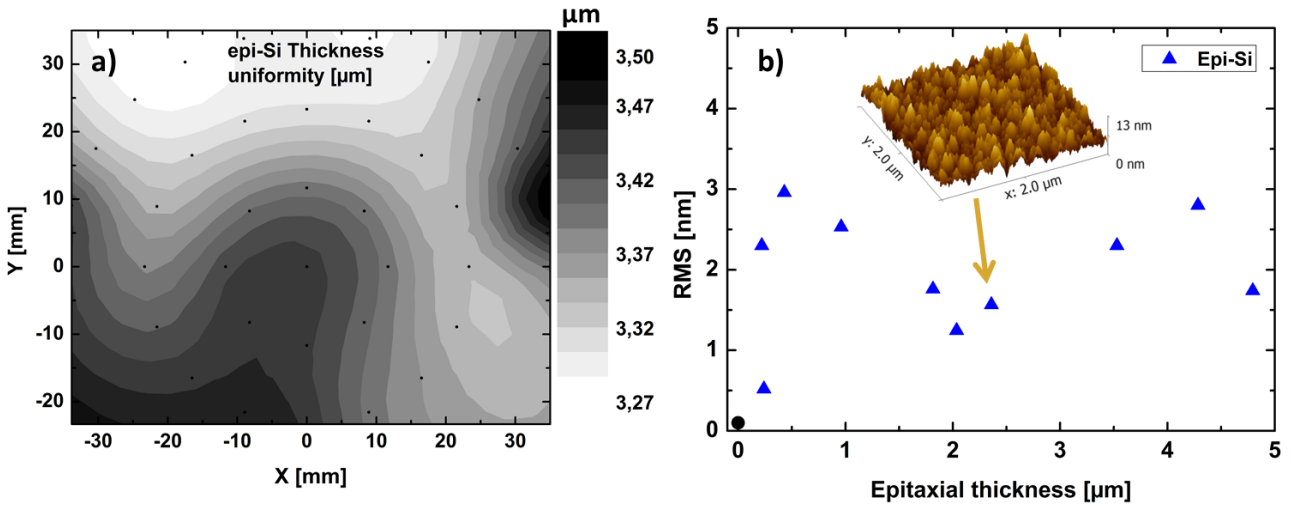


Fig. 3.9 – a) Map of epitaxial silicon thickness, deduced from fitting 38 ellipsometry spectra over a 4 inch sample. Average thickness is 3.37 μm and uniformity is 3.5%. b) RMS roughness measured by AFM on 2x2 μm^2 areas for c-Si wafer (circle) and low temperature epitaxial silicon of various thicknesses (triangles).

3.4.2.1 Anisotropic etching of epitaxial silicon

In addition to ellipsometry and AFM characterizations, we have also performed anisotropic etching experiments to further assess the quality of the low temperature RF-PECVD material. For more than 45 years now, the semiconductor industry has been using the an-isotropic etching technique to control diffuse doping profile or insulate integrated circuit chips[70]. Unlike isotropic etches (e.g. HF, HNO_3, CH_3COOH, etc.), anisotropic has an etching rate which differs from one crystallographic orientation to another. It is indeed well established that, for some etching solutions (111)-oriented planes have the lowest etching rate compared to the other family planes, for both Si and Ge. Usually this anisotropic etching is performed in hydroxides solutions such as KOH, NaOH or TMAH $(CH_3)_4NOH$. The red-ox chemical reaction involved is based on silicon oxidation and water reduction:

$$Si_{(s)} + 2HO^-_{(aq)} + 4H_20 \longrightarrow Si(OH)^{++}_{2\,(aq)} + 2H_{2g} + 4HO^-_{(aq)} \tag{3.1}$$

As a reminder, Fig.3.10-a) shows the example of the most common low Miller index planes of crystalline silicon, that is (100), (110) and (111), and their position in the cubic structure. As mentioned by Bean at al.[71], an important parameter for anisotropic etching is the packing density as well as the available bonds in the crystallographic planes. The schematics on Fig.3.10-b) clearly show that in FCC crystals, the packing density is decreasing according to: (111)>(100)>(110)[72]. Consequently, one would expect that both etching rate and epitaxial growth would be considerably faster in <110> direction compared to <100>, and even more so than in the <111> direction.

[23] C. Rosenblad et al., Journal of Vacuum Science & Technology A, **16**: 2785–2790, 1998.
[70] D.B. Lee., Journal of Applied Physics, **40**: 4569–4574, 1969.
[71] K.E. Bean et al., IEEE Transactions on Electron Devices, **25**: 1185–1193, 1978.
[72] K.E. Jensen et al., Soft Matter, **9**: 320–328, 2012.

	KOH 34 wt.%, 71°C	TMAH 20 wt.%, 80°C
Etching rate	μm.min^{-1}	μm.min^{-1}
(100)	0.629	0.603
(110)	1.292	1.114
(111)	0.009	0.017

	KOH 34 wt.%, 71°C	TMAH 20 wt.%, 80°C
Etching ratio		
(100)/(110)	0.49	0.54
(100)/(111)	74	37
(110)/(111)	151	68

Tab. 3.2 – Typical etching rates of c-Si crystal planes in KOH and TMAH, from Shikida et al.[73].

Considering the etching rates, as reported by Shikida et al.[73], this assumption is true for both KOH and TMAH: v(110)>v(100)>v(111). The typical values of the etching rates and selectivities are shown in Tab.3.2. Considering the epitaxial growth or regrowth, as mentioned above in this manuscript, it is well known that it is slower and more difficult to grow high quality epitaxial layers on (111)-oriented surfaces at low temperature, compared to (100). However the differences in growth rate and epitaxial quality for (110) and (100) are less clear; Csepregi et al.[37] did not mention a higher regrowth rate on (110) compared to (100). However, another study[74] claims that heterostructure growth by MBE results in higher interface quality on (110) compared to (100) (no reconstructions and reduced anti-phase domains in the case of GaAs on Ge).

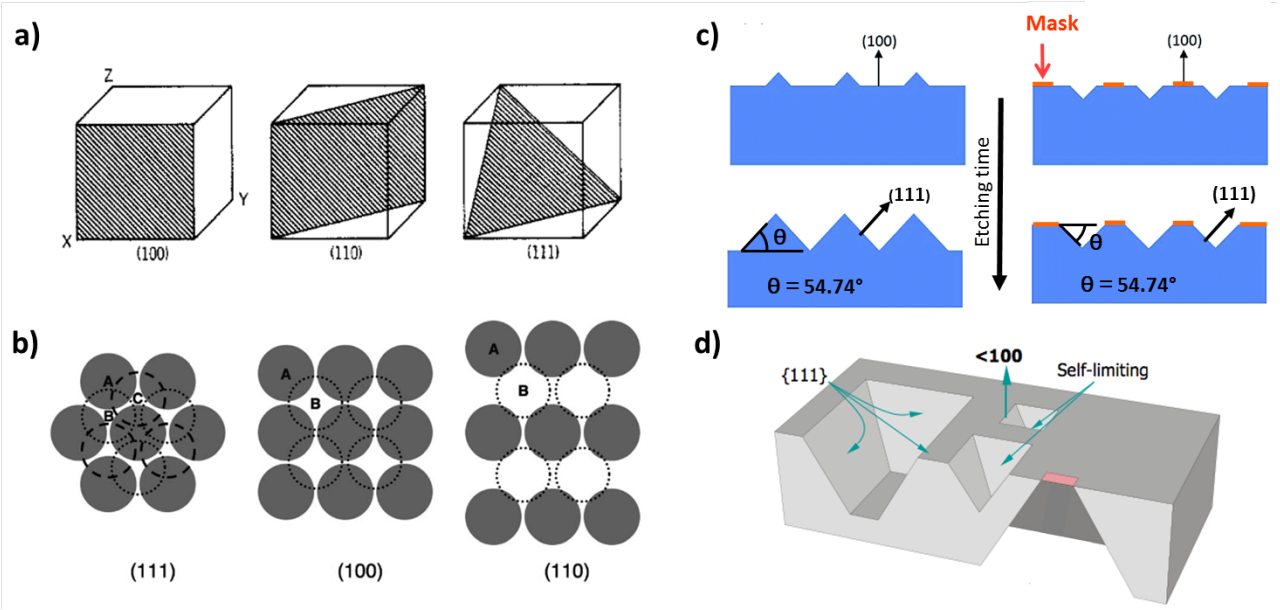


Fig. 3.10 – a) Low crystallographic index planes of silicon. b) Schematic of stacking sequences for (111), (100) and (110) planes in an FCC crystal. Dash circles show the atomic positions in the upper plane. c) Schematics of standard pyramidal texturing of (100) surface (left) and inverted pyramids created through a mask (right). d) Example of possible etch-limiting or self-limiting 3D patterns achieved by using a mask and anisotropic etching of c-Si (100). From ref.[71,72,75].

This selectivity with respect to the crystalline orientation can be used to produce various types of topography on crystalline silicon. As shown on Fig.3.10-c), the etching of a bare (100) surface will result in pyramids: the fast etching of (100) planes will stop when two revealed (111) planes intersect.

[73] M. Shikida et al., Sensors and Actuators A: Physical, **80**: 179–188, 2000.
[37] L. Csepregi et al., Journal of Applied Physics, **49**: 3906–3911, 1978.
[74] H. Kroemer et al., Applied Physics Letters, **36**: 763–765, 1980.

If no specific mask is applied, anisotropic etching of c-Si results in a field of random pyramids of few microns height, with a 54.74° base angle, with respect to the surface, corresponding to the angle between (100) and (111) planes. If a mask is used to protect some fraction of the (100) surface, this will result in holes with (111) walls inclined at 54.74° with respect to the surface. A large variety of structures can be designed; the Fig.3.10-d) shows an example of etch-limiting or self-limiting 3D patterns obtained by masking some parts of the c-Si (100) surface.

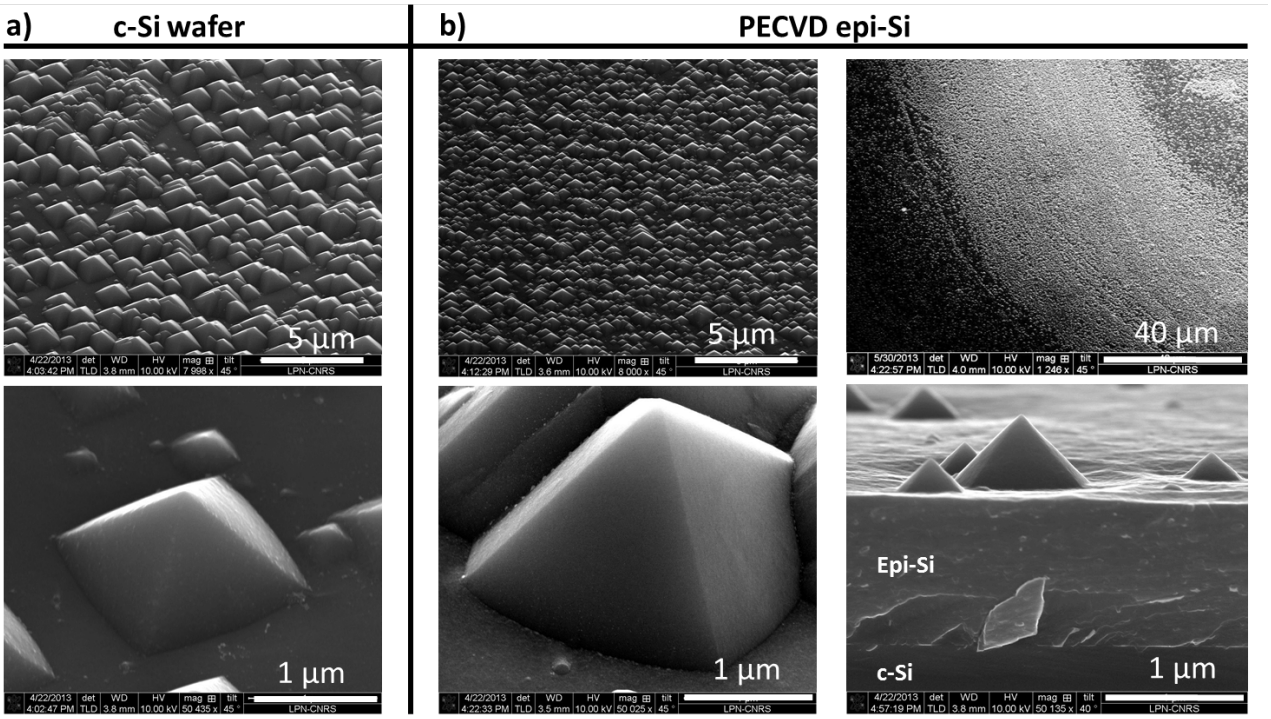


Fig. 3.11 – a) SEM pictures of c-Si (100)-oriented wafer textured by KOH at LPN-CNRS: broad view (top) and zoom on a single pyramid (bottom). The same chemical texturation process is applied on PECVD epitaxial silicon in b): broad view (top pictures) and zoom on a single pyramid from a tilted view and cross section (bottom pictures).

Since anisotropic etching reveals crystallographic planes, we decided to etch our low temperature epitaxial layers to get a qualitative information on the layer crystalline quality. This work was performed in collaboration with Inès Massiot, Andrea Cattoni and Stéphane Collin from LPN-CNRS in the frame of Nathisol ANR project. A 2.4 μm epitaxial layer has been etched under the same conditions as a reference (100) c-Si FZ wafer. The first step was a short desoxidation of the surface using HF (5% HF, 20s) and then, using H_2O:KOH:IPA mixture (89.5mL:2.97g:4.5mL) under magnetic stirring at $\sim$ 75°C, we have tested the influence of etching time on surface morphology. The addition of IPA (isopropyl alcohol) in the etching solution is known[76] to produce smoother surfaces and better pyramids morphology. Around 3 min were needed to produce well defined shaped pyramids on the epitaxial silicon, then the pyramids density increased up to 5 min etching. Additional etching time resulted in lower quality features. Fig.3.11-a,b) show the random pyramids textured on c-Si wafer and epitaxial silicon after 5 min etching in the same conditions. Well defined pyramids are obtained in both cases, thus confirming the good crystal quality of the PECVD layer. However, a few differences can be observed: i) larger pyramids are formed on c-Si ii) fluctuation of the pyramids density appears in some places iii) by imaging the layer in cross section, a significant decrease in the layer thickness ($\sim$1 μm) is observed. Indeed, removing few microns of material to form pyramids on a 200 μm thick wafer is negligible, whereas removing 1 micron out of a 2 μm thick epi-layer is more problematic.

[76] I. Zubel et al., Sensors and Actuators A: Physical, **93**: 138–147, 2001.

The spatial fluctuations of pyramid density may result from the combination of two effects, namely a variation in the epitaxial layer quality and an inhomogenious etching due to bubble formation at the surface of Si in KOH solutions. Better homogeneity on larger scale may be achieved thanks to N_2 bubbling during the etching step.

3.4.3 Assessing the crystal quality

3.4.3.1 High resolution TEM analysis

To investigate the crystal quality of our LTE layers at a much smaller scale, we have performed cross section transmission electron microscopy (TEM) analysis. TEM is a very powerful technique to characterize materials down to the atomic level, which requires a good understanding in several fields: crystallography, diffraction, inelastic scattering, spectroscopy, etc. While the light microscopes[7] are limited by the Rayleigh criterion to few hundreds of nanometers in resolution, it is possible to reach much better resolution with electrons whose wavelength is proportional to the inverse of the square root of their energy, according to Louis de Broglie's famous equation[8]. But on the other hand, TEM is not a sampling tool: it is probing only a very tiny volume of the sample[9]. "Know the forest before you start looking at the veins in the leaves on the trees", those are the words of Williams and Carter at the beginning of their very comprehensive book on TEM[77]. Since we had already performed macroscopic optical characterizations of our samples (ellipsometry, Raman, etc.), SEM characterization looking at the micron scale, logically it was interesting to go down to the nanometric scale. The following results were acquired thanks to the great help of two expert microscopists at LPICM: Rosa Ruggeri (visiting PhD candidate) and Jean-Luc Maurice.

For TEM analysis, it is essential to work with a piece of sample thin enough to allow a significant transmission of the incident beam through the sample (typically ∼100 nm for silicon). To obtain such electron transparent samples from wafer based samples, a polishing step is required. This can be mechanical polishing, with diamond pads, followed by an ion milling step to obtain sub-micron thickness and roughness, or the full thinning/polishing process may be achieved by focused ion beam - FIB. Using the FIB preparation[10] technique, a 4 μm thick PECVD epitaxial layer grown on c-Si (100) wafer has thus been thinned down along the (110) direction for TEM observation. The (110) direction corresponds to the planes perpendicular to the growth direction and it is the natural cleavage planes of (100)-oriented wafers. In other words, this crystallographic direction enables to observe the sample in cross section.

The result obtained after the above mentioned preparation step is shown on Fig.3.12-a). This is a SEM picture of the epi-Si/c-Si cross section. The two layers with different contrasts visible in SEM are: i) the top carbon protective layer and ii) the epi-Si/c-Si stack in the bottom. To differentiate the epitaxy from the wafer, TEM images were acquired with a JEOL 2010 FEG microscope equipped with a Schottky field emission gun operating at an acceleration voltage of 200 kV. One can distinguish the epi-layer from the wafer thanks to the different contrast and the interface visible as an horizontal line at roughly 1/3 from the bottom of the TEM image on Fig.3.12-b). The V-shaped light grey material in the middle of this image is an amorphized area, due to the ion beam during the FIB thinning step. c) is the higher magnification image of the small rectangle area in b). For this magnification, the difference between the silicon wafer and the epi-layer is more visible: the wafer is more uniform (bottom), whereas the epi-layer has some leopard contrast related to some defects in the crystal. A high resolution image of the interface (Fig.3.12-d)) is obtained for a magnification of x280000. From

[7] More precisely visible light microscope since some 'light microscopes' are actually heavy.

[8] In reality, for acceleration voltage $\geq$ 100keV, the velocity of electrons becomes greater than half the speed of the light, and relativistic effects cannot be ignored.

[9] The total volume of material examined by TEM since the 1950's is estimated around 10^3 mm^3.

[77] D.B. Williams et al. *Transmission electron microscopy: a textbook for materials science.* Springer, 2009.

[10] FIB preparation by D. Troadec at IEMN, via the French RENATECH network.

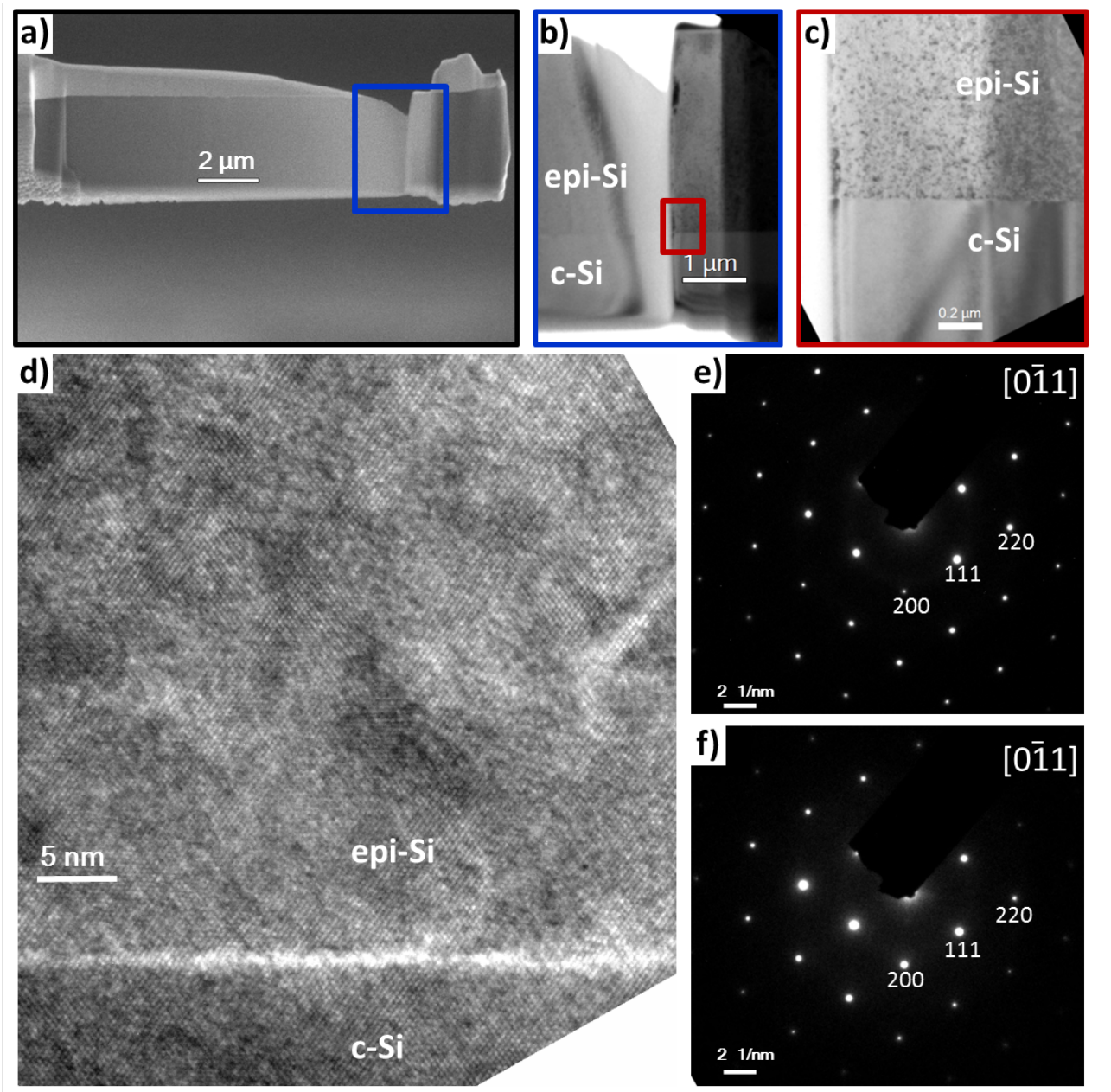


Fig. 3.12 – a) SEM image of a slice of epi-Si on c-Si wafer prepared by FIB. b) Cross section TEM image of the same sample at low magnification. A zoom of the rectangle area is shown in c). Two materials are visible: the 4 μm thick epi-Si at the top and c-Si wafer at the bottom. The vertical limit on the left side corresponds to material amorphized by the ion beam during FIB. d) HRTEM cross section image of the epi-Si/c-Si interface. e) and f) Diffraction pattern obtained in the bulk of the epitaxial layer and in the substrate respectively.

this image, we can draw the following conclusions: i) The interface between the wafer and the epitaxy is visible here as a relatively thin ($\sim$1nm) and defective white line. ii) Despite the defective interface, the crystalline structure propagates from the substrate to the epi-layer: crystal planes can be seen clearly in the substrate as well as the grown film. While we do not have a perfect interface nor a totally defect-free crystalline material, this is however a strong proof of the ability of growing monocrystalline material below 200°C by PECVD. The monocrystal quality can be further assessed by looking at the diffraction patterns: Fig.3.12-e) and f) show the diffraction obtained respectively in the bulk of epitaxial film and in the substrate. In both cases, sharp points corresponding to the c-Si family planes

of a well-defined FCC monocrystal are visible.

3.4.3.2 Focus on the defects

While our LTE silicon is clearly a monocrystal, it is nonetheless not a defect-free material. From the high resolution picture of the interface in Fig.3.12-d), it is already possible to distinguish some imperfections in the crystal structure (stacking faults, etc.). In the case of epitaxial growth on (100) FCC crystals, most of the defects lie in the (111) family planes. Thus, to try to identify the type of defects in our material, we have performed image treatment to isolate the contribution of the (111) planes to the HRTEM image. The process and results are shown on Fig.3.13. Starting from a HRTEM image of the epi-layer at the wafer interface (Fig.3.13-a), we applied a fast Fourier transform algorithm with Gatan DigitalMicrograph software, to obtain the equivalent of the diffraction pattern, as shown on the right side of Fig.3.13. Then a mask is used to select some (111) family plane spots, and the image is reconstructed using only those planes contribution thanks to an inverse FFT algorithm. The resulting image is displayed, in temperature color scale, in Fig.3.13-b). On the left hand side, we show 3 zooms, on selected areas where some defects are present. The defect number 1 corresponds for instance to an edge dislocation, and the two others show some type of lattice distortion.

Using different observation conditions we were able to identify a relatively high density of another type of defects present in our layers: hydrogen platelets. Those hydrogen platelets are elongated defects consisting of one or more missing planes forming a cavity in the crystal. H-terminated silicon bonds are delimiting this type of defects, and they may also contain some molecular hydrogen. An atomistic model of H-platelets is shown on Fig.3.14-d). By defocusing or tilting around specific crystallographic axis, it is possible to enhance the contrast of that type of defects. By doing so, we were able to take cross section TEM images of epitaxial samples, as visible on Fig.3.14-a,b), highlighting hydrogen platelets parallel to the interface and in (111) planes in the epitaxy, respectively. Such types of defects were also reported by Tsai et al.[20]. From 150°C to 350°C, they could observe by TEM a significant decrease of the H-platelet density; moreover they found a good correlation with SIMS measurement for H-content in the film. They calculated an average separation distance of 80 nm for platelets, in a layer grown at 350°C, corresponding to an H concentration of $\sim 1.3\times10^{19}\text{cm}^{-3}$. For the results shown on Fig.3.14, the growth was performed at 175°C, and as expected, a higher density of platelets was found. From the TEM image, we can count the platelets in the two visible (111) planes. The thickness of the TEM slice is then estimated thanks to the convergent beam electron diffraction (CBED) technique[78], and by assuming an equal density in all the four (111) plane families, an H-platelet density around $1\times10^{16}\text{cm}^{-3}$ is found. This is a high density, in good agreement with the H content around $1\times10^{20}\text{cm}^{-3}$ found by SIMS in those epi-layers. Interestingly enough, Tsai et al.[20], by doing epitaxial growth with SiH_4/D_2 plasmas, were able to prove that the hydrogen incorporated in the epi-layer is roughly 17 times more likely to come from SiH_4 related species than from H_2.

If those defects were all recombination centers, the layer would have very poor electrical properties. For instance, assuming that all platelets are active recombination centers, with a density n=1.10^{16}cm^{-3} and a cross section σ=10 nm^2, a rough estimation of epitaxy bulk lifetime τ_b can be performed using the following equation: $\tau_b^{-1} = n\sigma v_{th}$. With v_{th}=$2.3.10^7$ cm/s, the electron thermal velocity at 300K, it results in $\tau_b \sim 4.10^{-11}$s. However, by definition, H-platelets are made up with H terminated silicon bonds, which provide a good passivation. Based on the electrical properties of these layers, as presented in the next section and chapter, it is relatively clear that the density of electrically active recombination centers in the epi-layer is much lower.

[20] C.C. Tsai et al., Journal of Non-Crystalline Solids, **137-138**: 673–676, 1991.
[78] D. Delille et al., Ultramicroscopy, **87**: 5–18, 2000.

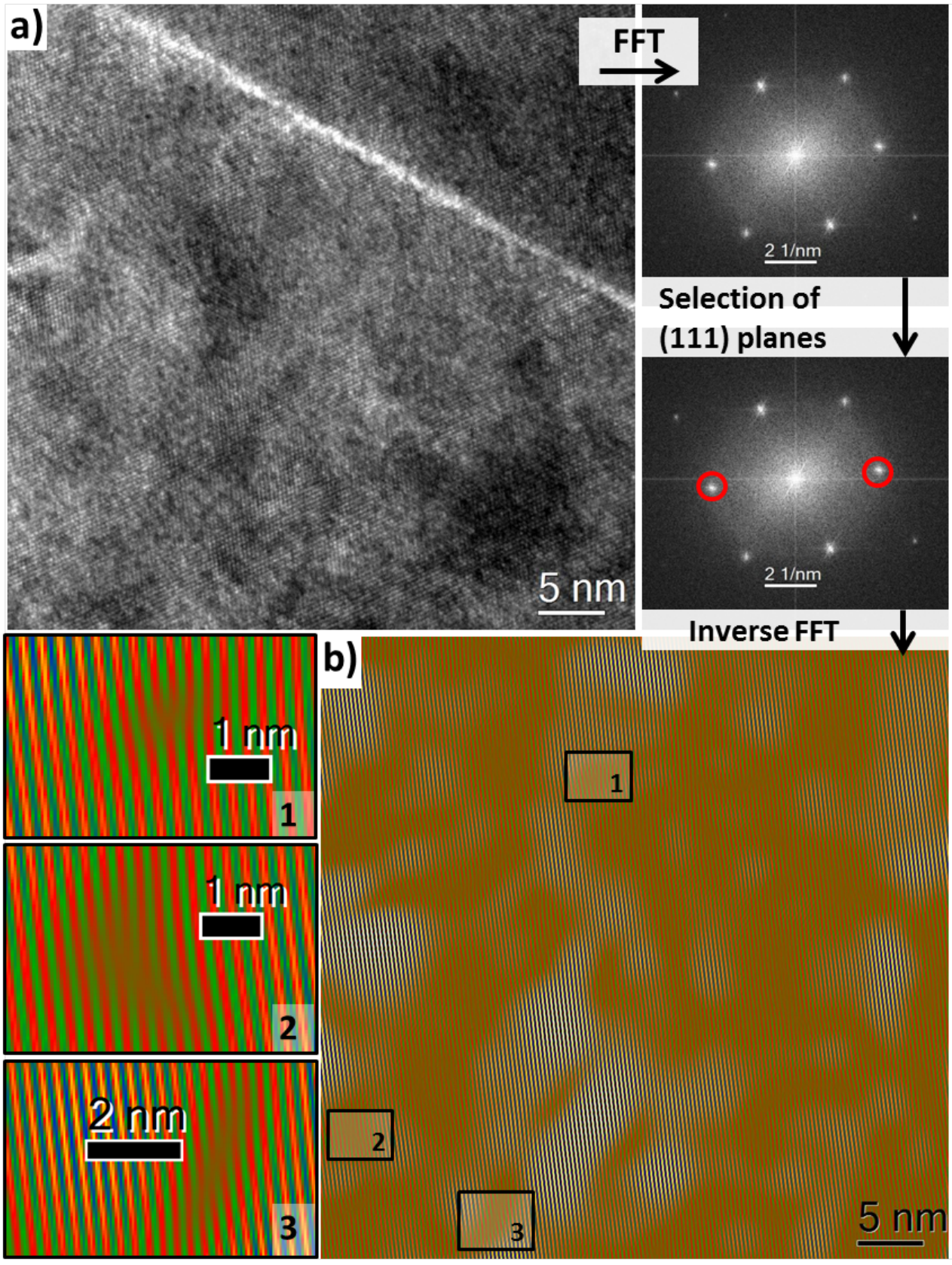


Fig. 3.13 – Processing of epi-Si/c-Si interface HRTEM images a) to highlight defects in the (111) planes: after doing a FFT, a mask is applied to select two (111) family planes (red circles). By doing an inverse FFT, the HRTEM image is reconstructed with only this (111) contribution, in b). The 3 colored pictures are the zooms on some defects in the reconstructed image.

On Fig.3.14-c) is displayed a high resolution TEM cross section image of the bulk of the epi-Si, with visible defects lying in (111) planes. There are some striking similarities, in terms of contrast, with the simulated map of stress component $\boldsymbol{\sigma_{yy}}$ around a (100) H-platelet by Moras et al.[79]. On this simulated map, the red represents the tensile stress and the blue the compression. Thus, the platelets, by distorting the crystal network, induce some stress locally in the film, and this distortion of the crystal is responsible for the leopard-shape contrast of the epi-layer observed by TEM. Given the high concentration of hydrogen in the layer, one can expect to detect also some stress at the macroscopic level. Indeed, while the H-platelets are here obtained as a side effect of growing epitaxial silicon at low temperature in hydrogen rich environment, they are highly desirable for other applications. The stress and H cavities can be used to exfoliate semiconductor layers. This is the base principle of the Smart

[79]G. Moras et al., Physical Review Letters, **105**: 075502, 2010.

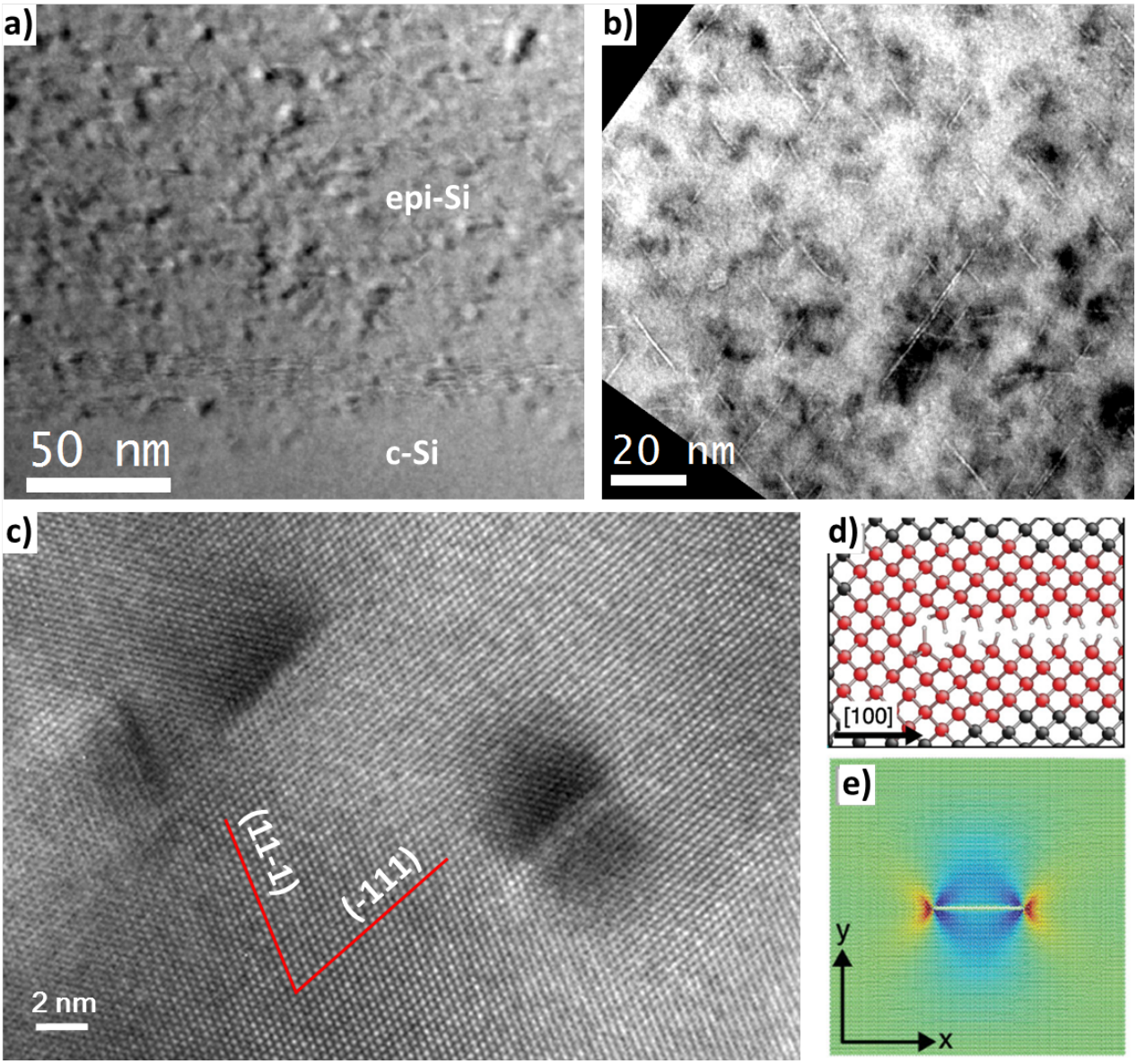


Fig. 3.14 – a) and b) Two beam bright field TEM image of epi-Si/c-Si interface tilted around [111] direction, and [004] direction. Hydrogen platelets parallel to the interface and in (111) planes are visible. c) High resolution image in (110) axis zone with defects lying in the (111) planes. d) Atomistic model of (100) hydrogen platelet and e) simulated map of stress component $\boldsymbol{\sigma_{yy}}$ (red tension, blue compression), from Moras et al.[79].

Cut process[80], originally patented by M. Bruel[81] in 1993 and commercially used by Soitec to produce engineered substrates such as SOI. Thus a large number of papers dealing with H implantation in silicon, platelet nucleation, stress and lift off can be found[82–85]. More details on this topic will be presented in the next chapter.

3.4.3.3 XRD analysis

The strain state of low temperature PECVD epitaxial silicon has been investigated by reciprocal space mapping (RSM) for the symmetric (004) and asymmetric (224) Bragg reflections of the c-Si substrate. The data were acquired with Rigaku Smartlab diffractometer in triple axis configuration, thanks to A. Shalimov from Rigaku company. Fig.3.15 shows the 3-dimensions (004) and (224) reciprocal space maps (RSMs) of a 5.15 μm thick epi-Si on (100) oriented silicon substrate. The corresponding peaks reciprocal coordinates, denoted as (Q_x, Q_z, in $Å^{-1}$), the full width at half maximum (FWHM) and the intensity are measured using the automatic peak search routine. The two peak contributions visible on both (004) and (224) maps are attributed to the substrate (high intensity and small FWHM) and epi-layer, thus confirming the monocrystal quality of PECVD epi-Si. A distinct contribution of the layer and wafer despite homoepitaxy scenario is explained by the strain state of epi-Si, and RSMs can be used to get more quantitative information. The epitaxial layer coordinates in the reciprocal space are expressed with respect to the unstrained reference silicon substrate (s): $\Delta Q_i^{(hkl)} = Q_{i,epi}^{(hkl)} - Q_{i,s}^{(hkl)}$ where i = x, z and (hkl) are the Miller indices. For $Q_i^{(hkl)}$ a scaling factor of $\lambda/4\pi$ is used, to work with wavelength independent dimensionless quantities. The resulting coordinates are thus expressed in reciprocal lattice units [rlu]. From the two RSMs we found $\Delta Q_x^{(004)}=0$ and $\Delta Q_x^{(224)} \simeq 0$, thus no tilt angle was found between substrate and epi-Si, and the layer is fully strained. Since the substrate has no mis-orientation, we do not consider anisotropic misfit relaxation; the in-plane $a_{\parallel}$ epi-layer lattice constant along [110] and out-of-plane $a_{\perp}$ lattice constant along [001] are then calculated from corresponding (004) and (224) reciprocal space coordinates[86]:

$$a_{\parallel,epi} = a_s \cdot \left(1 - \frac{\Delta Q_x^{(224)}}{\sqrt{2}\frac{\lambda}{a_s} + \Delta Q_x^{(224)}} \right) \tag{3.2}$$

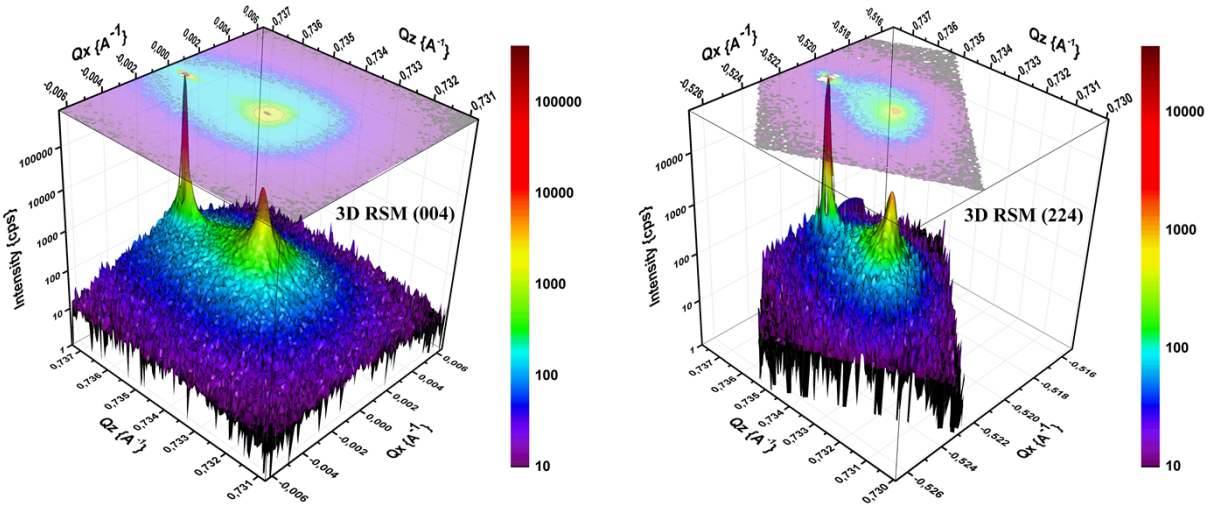
$$a_{\perp,epi} = a_s \cdot \left(1 - \frac{\Delta Q_z^{(004)}}{\frac{2\lambda}{a_s} + \Delta Q_z^{(004)}} \right) \tag{3.3}$$

with a_s=5.4307 Å, the crystalline silicon lattice constant, λ=1.5405 Å the incident $CuK_{\alpha 1}$ radiation wavelength, and ΔQ_i expressed in rlu. Once those strained unit cell epi-layer parameters are extracted, that is $a_{\parallel,epi}$ and $a_{\perp,epi}$, the bulk lattice constant of the corresponding fully relaxed epi-layer with cubic unit cell $a_{0,epi}$ is deduced from the following equations:

$$\varepsilon_{\parallel,epi} = \frac{a_{0,epi} - a_{\parallel,epi}}{a_{0,epi}} \tag{3.4}$$

$$\varepsilon_{\perp,epi} = \frac{a_{0,epi} - a_{\perp,epi}}{a_{0,epi}} \tag{3.5}$$

[80] M. Bruel et al., Japanese Journal of Applied Physics, **36**: 1636–1641, 1997.
[81] M. Bruel *Process for manufacturing thin film layers of semiconductor material* EP Patent App. EP19,920,402,520 1993
[82] S.T. Pantelides et al., Solid State Phenomena, **69-70**: 83–92, 1999.
[83] Y. Zheng et al., Journal of Applied Physics, **89**: 2972–2978, 2001.
[84] T. Hochbauer et al., Journal of Applied Physics, **92**: 2335–2342, 2002.
[85] X. Hebras et al., Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, **262**: 24–28, 2007.
[86] T. Roesener et al., Journal of Crystal Growth, **368**: 21–28, 2013.



Peaks	004				224			
	Intensity (cps)	FWHM dQx ; dQz ($Å^{-1}$)	Qx ($Å^{-1}$)	Qz ($Å^{-1}$)	Intensity (cps)	FWHM dQx ; dQz ($Å^{-1}$)	Qx ($Å^{-1}$)	Qz ($Å^{-1}$)
c-Si wafer	1,25E6	8.4E-5 ; 6.2E-5	0	0.73675	8.8E4	6.8E-5 ; 1.1E-5	-0,52085	0,73666
Epi-Si layer	1,42E4	2.0E-4 ; 2.8E-4	0	0.73413	1,42E4	5.6E-4 ; 7.3E-4	-0,52089	0,73413

Fig. 3.15 – left: XRD (004) and right (224) reciprocal space maps of 5.15 μm PECVD epitaxial silicon grown on c-Si (100) wafer, indicating that the epi-Si layer is fully strained.

$$\varepsilon_{\perp,epi} = -2\frac{C_{12}}{C_{11}}.\varepsilon_{\parallel,epi} \tag{3.6}$$

Where $\varepsilon_{\parallel,epi}$ and $\varepsilon_{\perp,epi}$ are the elastic strains related to deformation in each direction, and C_{11}=16.6×10^{11}dyn.cm^{-2}, C_{12}=6.4×10^{11}dyn.cm^{-2} the silicon bulk elastic constant at 300 K. The results are gathered in Table 3.3: a higher bulk lattice parameter, $a_{0,epi}$=5.4325 Å, is found compared to pure silicon, and this is attributed to distortion induced by the high hydrogen content in the crystal[35]. We found that the in-plane elastic strain is compressive, with $a_{\parallel,epi}$=5.4308 Å lattice matched to the wafer, and an out-of-plane tensile strain +0.024%. This tetragonal lattice unit confirms the pseudomorphic epitaxial growth of hydrogenated Si (epi-Si:H) on c-Si substrate. The relaxation parameter defined as: R=($a_{\parallel,epi}$-a_s)/($a_{0,epi}$-a_s), can be used to quantify the plastic deformation of the epi-layer related to the substrate. We found R $\simeq$ 5.5% for this 5.15 μm in-plane compressively strained low temperature epi-Si layer.

	In-plane		Out-of-plane		Bulk	
	$a_{\parallel,epi}$ (Å)	$\varepsilon_{\parallel,epi}$ (%)	$a_{\perp,epi}$ (Å)	$\varepsilon_{\perp,epi}$ (%)	$a_{0,epi}$ (Å)	R (%)
5.15 μm epi-Si	5.4308	+0.031	5.4338	-0.024	5.4325	5.5

Tab. 3.3 – Calculated epi-Si lattice parameters obtained from RSMs.

Indeed, the stress in the layer is closely related to its hydrogen content. So both the growth temperature[20] and the hydrogen dilution[35] are important parameters to tune this stress level. In addition, the quality of the wafer/epi-Si interface plays also a significant role on the layer stress. For example, the influence of a pure H_2 plasma treatment of the interface, after in-situ SiF_4 plasma cleaning, is shown on Fig.3.16. The ε_i curves of three samples are shown on a): without H_2 plasma treatment (black squares), with 120s of H_2 plasma exposure (red circles) and 300s (green triangles). These three samples were exposed to the same epitaxial growth conditions, and looking at the ε_i

peaks amplitude, very little changes were observable in the crystalline quality. The inset zooming on the low energy oscillations reveals slightly higher amplitude for longer H_2 plasma exposure, which is most likely linked to a change in the porosity of the interface layer. The Raman spectrum measured on the same samples gives further information (see Fig.3.16-b): the peak position is strongly shifted towards higher values with increasing H_2 plasma exposure time. The 0, 120 and 300s samples are respectively the black, red and green curve referring to the left-bottom axis. As indicated in the legend this increasing compressive stress is concomitant with a small increase of the FWHM (from 5.08 to 5.8). The blue curve (squares, top-right axis) represents the Raman peak position as a function of H_2 plasma exposure time: once again the trend toward a strong compressive stress for long exposure time is clear.

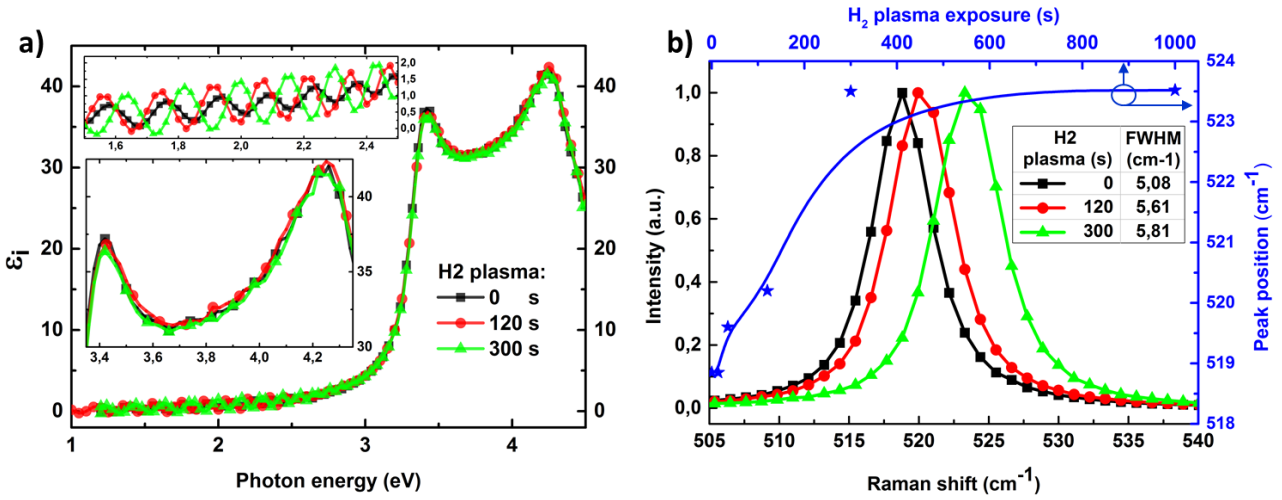


Fig. 3.16 – a) Ellipsometry measurements: ε_i for 3 epitaxial samples with different initial H_2 plasma interface treatment time: 0s (squares), 120s (circles) and 300s (triangles). b) Left-bottom axis display the Raman spectra of the three same samples showing a significant peak shift toward the compressive state. The blue curve (stars, top-right axis) shows the crystalline peak position as a function of H_2 plasma exposure time. FWHM is indicated in the legend.

It is indeed possible to get quantitative information on the strain in the layer from the crystalline silicon peak shift[87]. For a biaxially strained Si(100) film, the shift of the Si band relative to the strain free position is given by[88]:

$$\Delta\omega_{si} = \omega_{si} - \omega_{strain} = \frac{1}{\omega_0}\left(\frac{pS_{12}}{S_{11}+S_{12}} + q\right)\varepsilon_{\parallel} = b\varepsilon_{\parallel} \tag{3.7}$$

where S_{11} and S_{12} are the elastic compliance constants, p and q are the phonon deformation potential and $\varepsilon_{\parallel}$ is the in-plane strain as defined previously. The values of silicon constants found in literature are reported in Tab.3.4. The coefficient b is the strain-shift coefficient and ω_{si} and ω_{strain} are the frequencies of the Si modes in the strain-free reference and strained layer respectively. Values reported in literature[88] for this b coefficient in silicon range from -715 to -832 cm^{-1}. Thus one can see from equation 3.7 that a shift toward higher frequencies ($\omega_{strain}>\omega_{si}$) results in a compressive strain while the opposit ($\omega_{strain}<\omega_{si}$) is linked to a tensile strain. If we take ω_{si}=520cm^{-1}, b=-800cm^{-1} then the calculated values of $\varepsilon_{\parallel}$ are in the range of [-0.14 - 0.45]%. The corresponding stress can also be calculated from the Raman shift with the following equation: σ(MPa)=-500$\Delta\omega$(cm^{-1})[89]. Thus, we can conclude that these interface treatments enable to control the strain state of the layer from tensile to compressive.

[87] I.D. Wolf., Semiconductor Science and Technology, **11**: 139–154, 1996.
[88] S. Nakashima et al., Journal of Applied Physics, **99**: 053512–053512–6, 2006.
[89] V.T. Srikar et al., Journal of Microelectromechanical Systems, **12**: 779 –787, 2003.

	Chandrasekhar et al.[90]	Anastassakis et al.[91]	I. De Wolf et al.[87]
$\frac{p}{\omega_0^2}$	-1.43±0.07	-1.85±0.06	-1.46
$\frac{q}{\omega_0^2}$	-1.89±0.09	-2.31±0.06	-1.89
$\frac{r}{\omega_0^2}$	-0.89±0.03	-0.71±0.02	-0.59

	A. Brantley et al.[92]
Si elastic constants	cm^2/dyn
S_{11}	0.768×10^{-12}
S_{12}	-0.214×10^{-12}
S_{44}	1.26×10^{-12}

Tab. 3.4 – Literature values for Si phonon deformation potential[87,90,91] and Si elastic constants[92].

To sum up, both the hydrogen incorporated in the epitaxial silicon, which depends on the growth temperature and the silane dilution, and the quality/treatment of the interface (roughness, porosity, defects, etc.) are the controlling buttons for the stress of LTE layers.

3.4.4 Electrical properties

3.4.4.1 Background doping

In this PhD thesis we have been working mainly with intrinsic epitaxial layers (non-intentionally doped). Indeed the concentration of impurities such as C and O are typically in the range of 10^{19} cm^{-3} as obtained by SIMS, in the case of epi-layers deposited at 175°C in a PECVD reactor with no load-lock. Oxygen is known to occupy mostly interstitial lattice sites in the crystalline silicon lattice; however in some conditions, complexes such as SiO_4 may form and act as donors; such oxygen related n-type background doping is also reported for μc-Si material[93]. So one could expect a n-type background doping in the low-temperature epi-Si. To check this hypothesis we have performed Hall effect measurements on 500 nm intrinsic epi-Si deposited in our standard conditions and bonded to a glass substrate[11]. A small drawing of the stack is shown in Fig.3.17, and the measured donor concentration, resistivity and mobility are reported in Tab3.5. As expected, the background doping impurities results in an n-type doping, equivalent to an electrically active carrier concentration of $4.6\times10^{17}cm^{-3}$. All of samples measured on glass were found n-type with a doping from 1 to $5\times10^{17}cm^{-3}$. A similar doping range has been reported by DeBoer et al.[94]. They also mention mobilities equivalent to those of bulk crystalline silicon, but this is in the case of layers grown at 450-525°C using high vacuum electron-cyclotron-resonance plasma deposition. Here we found a lower electron mobility of $59cm^2/(V.s)$ (as compared to $\sim$ $1350cm^2/(V.s)$ for c-Si), which can be attributed to i) a higher defect concentration due to the deposition temperature below 200°C and ii) the epitaxial layer transfer process which may create some additionnal stress, defects and cracks in the layer. Another study on PECVD non-intentionally doped epi-layers electrical properties was performed with Soitec, but this time for epi-layers grown on SOI wafers. The electron and hole mobilities, without layer transfer step, measured on Pseudo-MOSFET transistors[95], was 400 and 125 $cm^2/(V.s)$ respectively.

[93] H. Keppner et al., Appl Phys A, **69**: 169–177, 1999.
[11] the process of epi-Si transfer and bonding will be explained in more details in the next chapter.
[94] S.J. DeBoer et al., Applied Physics Letters, **66**: 2528–2530, 1995.
[95] S. Cristoloveanu et al., ECS Transactions, **50**: 249–258, 2013.

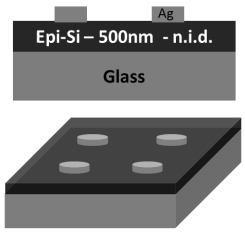


Fig. 3.17 – 1×1 cm^2 sample of 500 nm non intentionnaly doped epi-Si bonded to glass, with Ag contacts.

	n-type doping cm^{-3}	Resistivity Ω.cm	Mobility $cm^2/(V.s)$
500nm epi-Si Room Temp.	4.6E17	0.23	59

Tab. 3.5 – Carrier concentration, resistivity and mobility for a non-intentionally doped 500 nm epi-Si bonded to a glass substrate, as measured by Hall effect.

3.4.4.2 Phosphorous and boron doped layers

Controlling the doping is of course highly desirable for many applications. Working at low temperature enables the formation of p-n junctions with very sharp doping profiles. Thus, for instance in the field of photovoltaics, LTE can be favorably used to form emitters with well controlled doping profile[24–26,30], unlike conventional crystalline solar cells where the junction is formed by high temperature diffusion processes. The n(p)-type doping of LTE layers can be realized by adding small amount of phosphorous(boron) containing gases in the plasma. In our lab, we use phosphine (PH_3) as the n-type dopant gas and diborane B_2H_6 or trimethylboron ($(CH_3)_3B$) for the p-doped layers. In the frame of this doctoral work, we did not spend much time working on the doping topic[12]. From the previous work carried out by M. Labrune at LPICM[5], it was clear that a high doping level can easily be achieved: both n and p-type epi-layers doped in the range of $1\times10^{20}cm^{-3}$, as measured by Hall effect, were reported. Using gas cylinders with 2% of $(CH_3)_3B$ or B_2H_6 diluted in H_2, and 0.1% of PH_3 diluted in H_2, and the lowest accessible value of the mass flow controller, doped epi-layers at around $1\times10^{19}cm^{-3}$ were obtained. Thus a precise control of the doping level, especially for the low to intermediate values, would require some even more diluted cylinders. Based on ellipsometry results, it seems that doping with B_2H_6 resulted in a lower crystalline defect density compared to trimethylboron which contains carbon. In the case of epi-layers doped with PH_3, for a similar doping level compared to B_2H_6, the crystal quality seemed to be more affected for the n-layers[13]. In any case, a detailed study on the influence of the doping level on the crystalline quality and the mobilities in LT PECVD epitaxy is still needed. In literature, Shahrjerdi et al.[35] also claimed a $2\times10^{20}cm^{-3}$ electrically active donor concentration while keeping a good crystal quality as measured by XRD. Other details about RF-PECVD doped epi-layers may be found in thesis manuscripts from the University of Waterloo, Canada[96,97].

3.4.4.3 Assessing minority carrier lifetime in epi-layers

In the world of crystalline silicon solar cells, the measurement of minority carrier lifetime to assess material quality and surface passivation is very common. This is routinely achieved by using quasi steady state photoconductance, a method popularized by Sinton and Cuevas in the mid 1990's[98].

[24] J. Pla et al., Thin Solid Films, **405**: 248–255, 2002.
[25] M. Farrokh-Baroughi et al., IEEE Electron Device Letters, **28**: 575–577, 2007.
[26] R. Shimokawa et al., Japanese Journal of Applied Physics, **46**: 7612–7618, 2007.
[30] M. Labrune et al., Thin Solid Films, **518**: 2528–2530, 2010.
[12] #Guilty
[5] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells*. PhD thesis. Ecole Polytechnique, France, May 2011.
[13] "[...]phosphorous was very efficient in decreasing the epitaxial quality" M. Labrune, PhD thesis, 2011
[96] H.E. Gohary. *Development of Low-Temperature Epitaxial Silicon Films and Application to Solar Cells*. PhD thesis. University of Waterloo, Canada, Sept. 2010.
[97] R.T. Samadzadeh. *A Novel Buried-Emitter Photovoltaic Cell for High Efficiency Energy Conversion*. PhD thesis. University of Waterloo, Canada, Feb. 2013.
[98] R.A. Sinton et al., Applied Physics Letters, **69**: 2510–2512, 1996.

This technique relies on eddy current: a flash light of typically 20-1000 μs creates photo-generated carriers in a semiconductor material, and the corresponding excess photoconductance is probed by a coil placed below the sample. However this tool, while being available in the laboratory, could not measure reliably samples smaller than a quarter of 4 inch. wafer; indeed this set-up, the WCT-120 by Sinton Instrument, is not designed for small size thin film materials.

To probe the minority carrier lifetime in our epi-layers, we also used a more flexible home-built time resolved microwave conductivity set-up (TRMC), also often referred as μW-PCD. In our experimental setup, the probed area was few mm^2. A comprehensive description of this set-up and the technique itself can be found in the PhD thesis of R. Brenot[57]. This set-up was also later used by S. Kasouit as reported in his PhD thesis[99]. For this manuscript, TRMC was used to probe lifetime in epi-Si layers, thanks to the valuable help of A. D'Acremont, J.-C. Vanel and J. Nassar. The principle is to create excess carriers, this time with a pulsed laser, and to detect the corresponding changes in the sample's photoconductance. This can be done thanks to a continuous measurement of microwave reflectivity. The detected change in reflectivity is indeed proportional to the photoconductance induced by the laser pulse[100]. Detailed theoretical understanding of this effect was published in the mid 1980's[101,102]. The general equation describing the 1D time evolution of excess minority carriers, e.g. electrons, in a semiconductor slice of thickness W centered on the origin of a z axis, is based on the sum of 3 terms: laser generation, diffusion and recombination[57]:

$$\frac{\partial \Delta n}{\partial t} = \overbrace{D\frac{\partial^2 \Delta n}{\partial z^2}}^{\text{Diffusion}} \overbrace{-\frac{\Delta n}{\tau_{bulk}}}^{\text{Recombination}} \overbrace{+\ \alpha(1-r)N_0\gamma_q(t)e^{\alpha(z-\frac{W}{2})}}^{\text{Laser generation}} \quad and \quad \overbrace{\begin{cases} D(\frac{\partial \Delta n}{\partial z})_{\frac{w}{2}} = -S_1.\Delta n_{|\frac{w}{2}} \\ D(\frac{\partial \Delta n}{\partial z})_{-\frac{w}{2}} = S_2.\Delta n_{|-\frac{w}{2}} \end{cases}}^{\text{Boundary conditions}} \tag{3.8}$$

where $\Delta n(z,t)$ is the density of excess electrons, D is the diffusion coefficient of electrons, and the surface recombination velocities S_1 and S_2 are the boundary conditions. The bulk recombination is considered as constant, with a characteristic lifetime τ_{bulk}, and the 532 nm laser delivers pulses of typically 4 ns FWHM. Thus carriers dynamics below this 4 ns will not be detectable with this set-up. But for silicon we are probing lifetimes of few orders of magnitude higher, so this pulse width is not a problem and the laser generation term can be neglected for solving the excess carrier equation. The solution of equation 3.8 with the above mentioned boundary conditions is a sum of exponential decay modes with different characteristic times. The short characteristic times are associated to higher order surface decay modes and the effective lifetime, corresponding to the fundamental mode, is given by[103,104]:

$$\begin{cases} \frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \left(\frac{W}{S_1+S_2} + \frac{W^2}{\pi^2 D}\right)^{-1} \\ \frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S}{W} \quad \text{if} \quad S_1 = S_2 \ \text{and} \ S \ll \frac{\pi^2 D}{2W} \end{cases} \tag{3.9}$$

where τ_{eff} is the effective lifetime corresponding to the fundamental decay mode of TRMC measurement. For lifetime measurement on wafer, the bulk lifetime is often assumed infinite and the

[57] R. Brenot. *Corrélation entre mode de croissance et propriétés de transport du silicium microcristallin, établie par réflectométrie micro-onde et ellipsométrie.* PhD thesis. Ecole Polytechnique, France, 2000.
[99] S. Kasouit. *Mécanismes de croissance et transport dans le silicium microcristallin fluoré. Application aux transistors en couches minces et transfert technologique.* PhD thesis. Ecole Polytechnique, France, 2003.
[100] M. Kunst et al., Thin Solid Films, **450**: 159–162, 2004.
[101] M. Kunst et al., Journal of Applied Physics, **60**: 3558–3566, 1986.
[102] K.L. Luke et al., Journal of Applied Physics, **61**: 2282, 1987.
[103] A.W. Stephens et al., Journal of Applied Physics, **76**: 363, 1994.
[104] A.B. Sproul., Journal of Applied Physics, **76**: 2851, 1994.

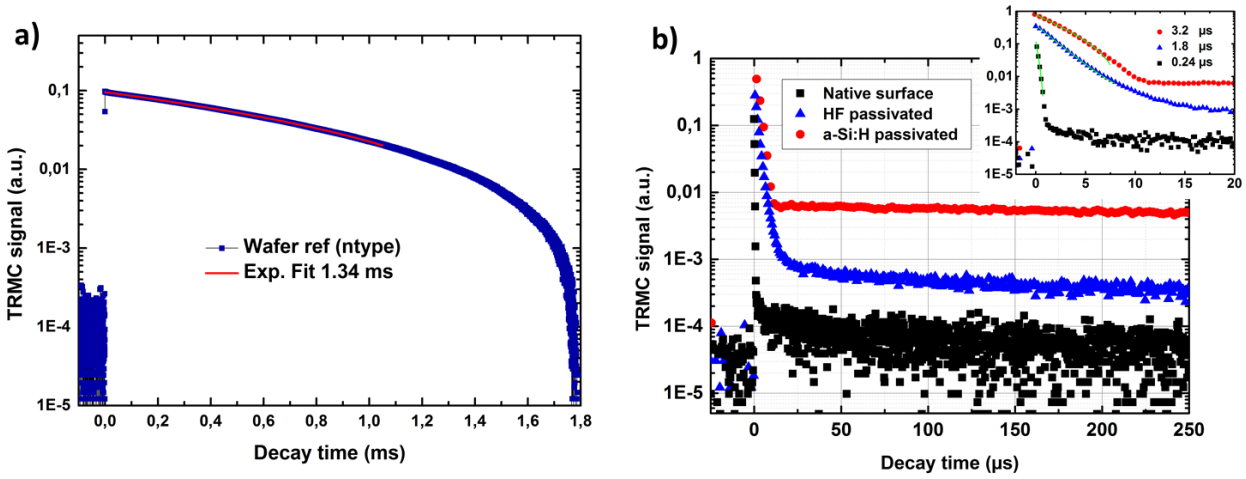


Fig. 3.18 – TRMC measurements for minority carrier lifetime probing on: a) a mirror-polished double side a-Si:H passivated 280μm thick n-type ρ=1-5 Ohm.cm c-Si FZ wafer and b) a 25 μm thick Cz c-Si wafer with three different surface passivations. Blue squares on a) are the experimental points and the exponential fit is the red curve. On b), the black squares are the data from the out-of-the-box sample, the blue triangles are from the HF passivated sample and the red circles from a double side a-Si:H passivated sample.

surface recombination velocities are the unknown parameters. But here, we know that in our epi-Si layers the bulk lifetime is lower than in perfect silicon crystal. However, from the expression (3.9), one can see that without knowing exactly the sample's surface recombination velocities, τ_{eff} gives a lower bound for bulk lifetime τ_{bulk}. The TRMC measurements itself should also be done carefully: a too high injection level and/or a non homogeneous generation (αw>1), α being the absorption coefficient, will produce non-linear effects and a distorted signal[57].

In order to test the set-up we have first performed lifetime measurements on FZ n-type c-Si wafers passivated on both sides with amorphous silicon. That type of sample is known to have a high lifetime due to the outstanding bulk material quality and the excellent surface passivation provided by a-Si:H. The result is shown in Fig.3.18-a) where the measured TRMC signal is shown in blue and the exponential fit in red. A strong signal was detected with a clear decay over millisecond time scale; the measured injection level was in the range of 10^{16}cm^{-3}. From the fitting, a characteristic decay time of 1.34 ms is found, which is typically the expected range of values for this type of sample.

After this first confirmation, we decided to perform measurements on a thinner wafer, namely a Cz p-type ρ=1-5 Ohm.cm 25 μm c-Si, with different surface passivations. The result is shown in Fig.3.18-b). Being Cz and p-type, a lower lifetime could be expected. The TRMC signal as a function of time is plotted for the native wafer surface (black squares), for the same wafer dipped in HF (blue triangles) and after a-Si:H both-side passivation (red circles). From this graph a reasonable trend in decay time can be observed with the increasing surface passivation quality: roughly 22 μs for native surface, $\sim$ 80 μs for HF dip and $\sim$ 400 μs for a-Si:H passivation. In addition, for this sample, shorter decay times were also observable: as shown in the inset, we found 0.24 μs, 1.8 μs and 3.2 μs for native, HF and a-Si:H passivated surfaces respectively. Those shorter decay times are most likely related to surface decay modes.

Thus after checking that the set-up could suitably measure high and low lifetime and give a reasonable trend when changing the surface passivation quality, we performed measurements on epi-Si layers. In their nice paper, Walter et al.[105] probed lifetime of epi-layers attached to their c-Si crystal seed substrate. But in our case, the laser beam and the microwave guide arrive on the

[105] D. Walter et al., Progress in Photovoltaics: Research and Applications, **22**: 180–188, 2014.

opposite side of the sample, so measurement on epi-layers attached to the substrate is less straight forward. Consequently, in order to remove possible influence of the wafer on the measurement, we have performed TRMC on free standing epi-Si layers[14]. In the few microns thickness range, crystalline silicon is completely flexible and not mechanically self-supporting. So we have used epi-Si flakes of few mm^2; this size was big enough to get a good TRMC signal. The measurement was performed on a 6 μm epi-Si layer dipped in HF, and, as a comparison, on a 1.1 μm thin slice of c-Si (so called epi-free), passivated by a-Si:H on both sides, and produced at IMEC by a specific exfoliation technique[106]. The results are displayed in Fig.3.19-a), where both epi-PECVD layer (black squares) and epi-free layer (red squares) exhibit a short (<1μs) and long decay time (>50μs). We think that the short decay time corresponds to the effective lifetime whereas the long decay time may be linked to some defect assisted trapping detrapping mechanisms. Indeed it is well known[15] that traps in crystalline silicon as well as in p-n junctions or inversion layers can lead to artificially high measured values of effective lifetimes with photoconductance decay techniques[107,108]. If, due to material quality or defects created during the transfer process, shallow levels are present in the band gap, some trapping detrapping effect, which is not directly related to recombination kinetics, may enhance the apparent lifetime.

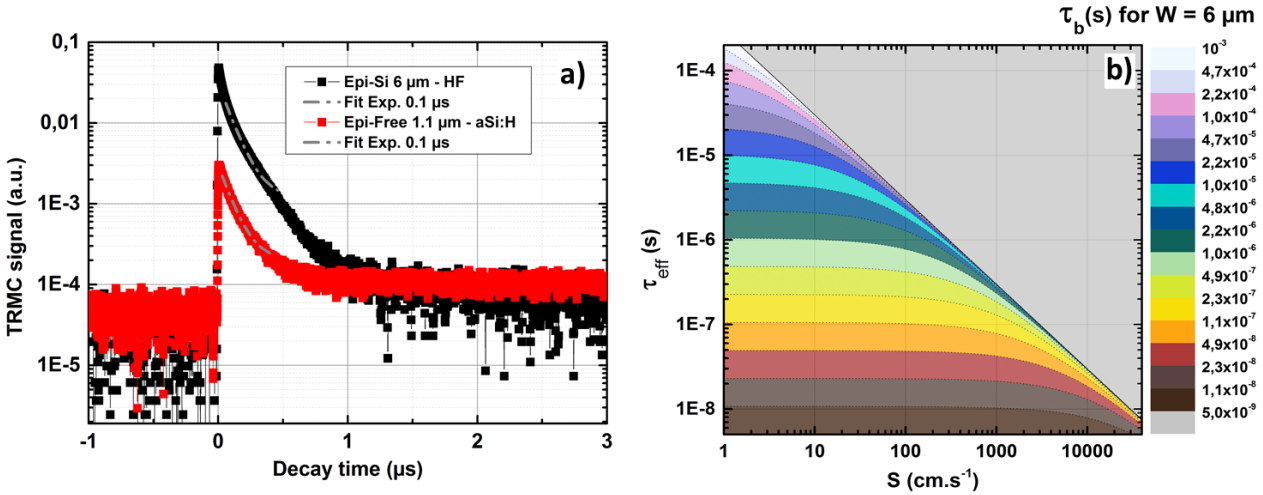


Fig. 3.19 – TRMC measurements for minority carrier lifetime probing on: a) a 6 μm both side HF-passivated epi-Si sample and on 1.1 μm epi-free both sides a-Si:H passivated sample. Both samples have a ∼0.1 μs characteristic decay time. Fig. b) shows the theoretical bulk lifetime τ_{bulk} map for a 6 μm c-Si sample as a function of the effective lifetime τ_{eff} and the surface recombination velocity (assumed here equal on both sides).

Consequently, focusing on the short decay time, we could fit the exponential decrease to find a τ_{eff} of 0.1μs for both samples. The first comment is that both materials have similar effective lifetimes, despite an epitaxial growth below 200°C for the first one and a formation process above 1000°C for the second one. However one should remember that the samples have different thicknesses, different passivations and also different lift-off processes; so the conclusion is not straight forward. A series of samples with various thicknesses or calibrated passivation could help to extract more precisely the bulk lifetime. This effective lifetime can nonetheless be compared to the literature data. If we look at results on thicker layers, namely epi-foil of 40-50 μm grown by CVD at 1130°C, then effective lifetimes up to 100-200 μs have been reported[109]. Yet, lifetime values for thicknesses around 10 μm are much smaller: Walter et al.[105] have typically measured effective lifetime of few μs. Indeed the effective lifetime is

[14] Details about detachment procedure are explained in the next chapter.
[106] V. Depauw et al., Progress in Photovoltaics: Research and Applications, **19**: 844–850, 2011.
[15] But we could "rediscover" the problem.
[107] D. Macdonald et al., Applied Physics Letters, **74**: 1710–1712, 1999.
[108] D.-H. Neuhaus et al., 3rd World Conference on Photovoltaic Energy Conversion, **1**: 91–94 Vol.1, 2003.
[109] H.S. Radhakrishnan et al., Progress in Photovoltaics: Research and Applications, , 2013.

more sensitive to a change in surface recombination velocity for smaller thicknesses. While it is not possible to get a quantitative value for the bulk lifetime out of those simple measurements, Fig.3.19-b) shows, on an indicative basis, a color map of τ_{bulk} values in the τ_{eff} and S plane, deduced from the equation (3.9), for a 6 μm thin silicon slice. In addition, other microwave photoconductance decay measurements were performed with Soitec, on a commercial μ-PCD set-up for PECVD epi-layers grown at LPICM on SOI wafers. A range of 50-150 μs, for the bulk epi-Si lifetime, was found.

3.5 Material evolution with thickness in LT RF-PECVD

As mentioned earlier, low temperature epitaxy is nothing new. For instance, Eaglesham et al.[67] have reported epitaxial growth of Si on c-Si at room temperature, and Thiesen et al.[110] also claimed epitaxial growth at 195°C by HWCVD. However they could sustain epitaxial growth over 1-3 nm and 140 nm respectively. So the important figure is not whether epitaxial growth is possible with a given technique at low temperature, but rather the value of the critical thickness before the monocrystal breaks down into amorphous or polycrystalline material. Indeed, depending on the growth conditions, material quality can vary a lot over the film thickness. As shown in Fig.3.6, silane dilution in H_2 is one key parameter: a too high or too low dilution will result in epi-breakdown into mirocrystalline or amorphous material. Moreover, the results were obtained from a 15 min deposition series, where only the silane flow rate was changed. Most likely, by repeating the same experiment but with a longer deposition time, the SiH_4 dilution range for a sustained epitaxial growth will be sharper. The idea behind this is that, if the deposition parameters are slightly off the optimum values, this will result in a smaller critical thickness. In this section, we study how the material was changing with thickness i) when the optimum growing conditions are used and ii) when a deviation from the optimum conditions was introduced by changing the ion bombardment energy on the substrate.

3.5.1 Epitaxial quality improvement with thickness

On most of our low temperature epitaxial silicon samples, a defective epi-Si/c-Si interface was detected by ellipsometry (interferences in the 1-2.5 eV range, see Fig.3.8). The presence of this imperfect interface was also confirmed by cross section TEM high resolution images (see Fig.3.12). Various types of defects can be detected at the interface: stacking faults, point defects, platelets, dislocations, SiO_2 islands, etc. This can be partially explained by the imperfect cleaning process (e.g. simple HF dipping) which can create some small roughness, and the subsequent air exposure before loading the sample and pumping down the reactor which can form SiO_2. Also, the low temperature epitaxial growth mode which likely proceeds by islands, may account for this defective interface layer. Thus, realizing that our process results in a poor crystal quality at the wafer interface, we decided to investigate how this could change over the epitaxial thickness, when optimized deposition conditions were used.

The crystal quality evolution with thickness was investigated for epitaxial samples of few microns by means of in-situ real-time spectroscopic ellipsometry and Raman spectroscopy performed on epi-Si/c-Si cross section after deposition. The time evolution of ε_i monitored in-situ is shown on Fig.3.20. The epitaxial growth was performed on SOI (Silicon-On-Isulator) wafers from Soitec company. The substrate consisted of a 14 nm c-Si (100) surface layer with a 20 nm thick SiO_2 buried oxide layer, with a 700 μm thick c-Si carrier wafer below. After an in-situ SiF_4 plasma surface cleaning step, the epitaxial growth was performed for up to 1.5 μm while monitoring ellipsometry data on the growing film every 2s on the full [1-6] eV range. The 3D surface of ε_i as a function of time (in min.) and energy is displayed on Fig.3.20-a). The color scale represents ε_i amplitude. The first striking feature is the well-defined oscillations in the low energy range with a continuous decrease in amplitude. This effect is linked to the presence of the 20 nm buried oxide which produces a strong optical index contrast.

[67] D.J. Eaglesham et al., Journal of Applied Physics, **74**: 6615–6618, 1993.
[110] J. Thiesen et al., Applied Physics Letters, **75**: 992–994, 1999.

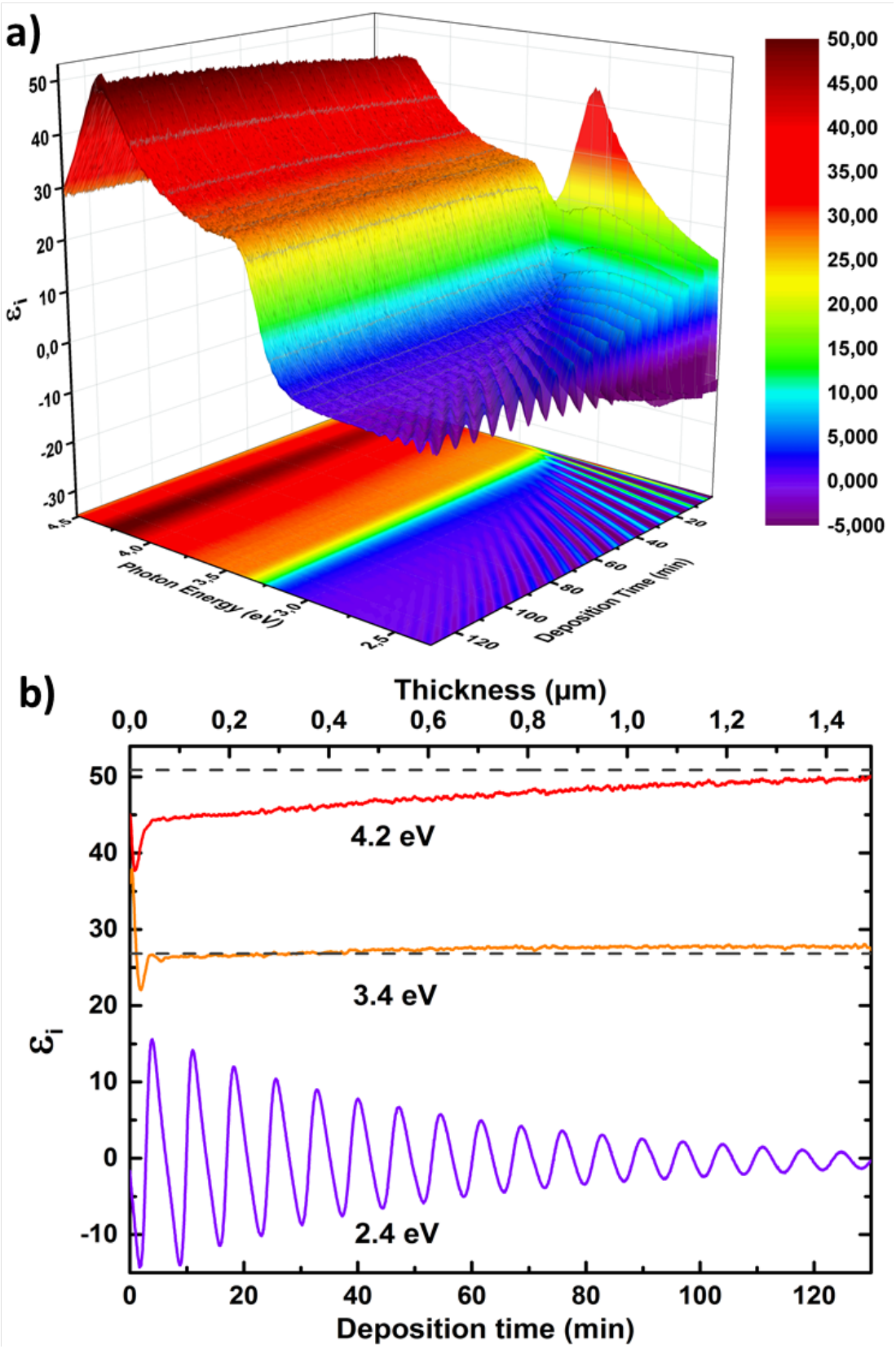


Fig. 3.20 – a) Time evolution of ε_i recorded by real time spectroscopic ellipsometry during PECVD silicon epitaxial growth at 175°C, on 14 nm SOI wafer. b) time evolution of ε_i at specific energies during this deposition: 2.4, 3.4 and 4.2 eV. Dash lines represent ε_i 3.4 and 4.2 eV peak amplitude of c-Si surface as measured after in-situ surface cleaning, prior to epitaxial growth.

Further details about this part of the spectrum are visible on Fig.3.20-b) where the time evolution of ε_i at 2.4, 3.4, and 4.2 eV is shown[16]. The bottom purple curve shows ε_i at 2.4 eV as a function of time; where the oscillations are linked to the growing film thickness. From the very stable oscillation frequency detected, we can conclude that the deposition rate is constant during the whole deposition. The decreasing amplitude is explained by the increasing film thickness which gradually buries the oxide below the epitaxial film.

The other interesting information visible on this in-situ data is the evolution of the 3.4 and 4.2 eV ε_i peak amplitude. This effect, not so easy to detect on the ε_i 3D curve, appears clearly on Fig.3.20-b) where ε_i at 3.4 and 4.2 eV as a function of time are plotted. The top red curve corresponds to 4.2 eV, and the middle curve is the 3.4 eV. The horizontal dash-lines indicate the amplitude of ε_i on the c-Si surface after oxide removal and before epitaxial growth. For these two energies, ε_i is very sensitive to the layer surface quality in the first 5-10 nm: a high peak amplitude is the signature of an excellent crystal quality with a small roughness. We see that peak amplitudes, relatively low at the beginning, continuously increase during the deposition. ε_i at 4.2 eV reaches the same amplitude value as the clean c-Si surface before epitaxy, after 130 min of deposition. And ε_i at 3.4 eV even slightly surpasses the amplitude measured before the epitaxial growth. From these two trends, we can conclude that starting from a defective interface, the crystal quality is improving with epitaxial thickness.

This crystal quality improvement upon epitaxial growth has been further studied by post deposition Raman mapping of epi-Si/c-Si cross sections. Results of the measurements on a 4 μm epitaxial layer grown on standard c-Si wafer are shown on Fig.3.21. a) shows the crystalline peak FWHM map and b) the peak position map for the same sample; the scanned area covers a 21.5×5 μm^2. Every measured pixel has a size of 0.2×0.2 μm^2 while the spatial resolution of the microscope for λ= 532 nm is 0.36 μm. Thus each pixel shown here corresponds indeed to a slightly larger physical area. The optical filter for the laser and the scan speed have been adapted prior to this measurement in order to avoid any heating related effect. The top of the sample starts at $\sim$ 3 μm from the top of the map, then at $\sim$ 7 μm the interface with the wafer is clearly visible, and further below is the crystalline silicon wafer. For the top $\sim$ 3 μm of the map, the laser is not probing the sample, so the data in this area should be discarded. On both FWHM and peak position maps, this scanned area reveals a perfect lateral homogeneity. The depth profile for this sample is shown on Fig.3.21-c,d). The blue curves (circles) correspond to the scanned area shown on a) and b), and the black curves (squares) come from a scan in a different area of the same sample. As shown on c), the depth evolution of the FWHM is the following: starting from a low value of $\sim$ 4 cm^{-1} measured on the high quality c-Si wafer, the FWHM reaches a maximum close to the epi-Si/c-Si interface (7-7.5 cm^{-1}), and then there is a constant decrease down to $\sim$ 6.5 cm^{-1} close to the surface. On the two spots the trend is the same, and the values are very close. Since this peak broadening is linked to the presence of crystal defects, this FWHM depth profile is in good agreement with the previously shown in-situ ellipsometry measurement: crystal quality is improving when epitaxial growth starts from a defective interface. On the peak position depth profile (see Fig.3.21-d) one can see a strong drop from the stable level in c-Si to the epi-layer. There is then an evolution from a highly stressed interface to a lower stressed film at the surface. The same trend is observed on the two spots (blue and black curves). The shift in the c-Si peak position between these two spots is attributed to a different temperature in the Raman set-up environment, since the measurements were performed on two different days. According to equation (3.7), it is possible to deduce the strain state of the layer from the Raman peak position with respect to the reference crystalline silicon. For example here, looking at spot 2 depth profile, we have $\omega_{Si} - \omega_{strain}$ = [0.55-1.05] cm^{-1}, thus assuming a strain coefficient b = -800 cm^{-1}, this particular sample is in tensile strain with $\varepsilon_{||}$ equal to -0.13% at the interface and -0.07% close to the surface.

[16]Penetration depths in c-Si at 2.4, 3.4 and 4.2 eV are respectively 1315, 10 and 5 nm.

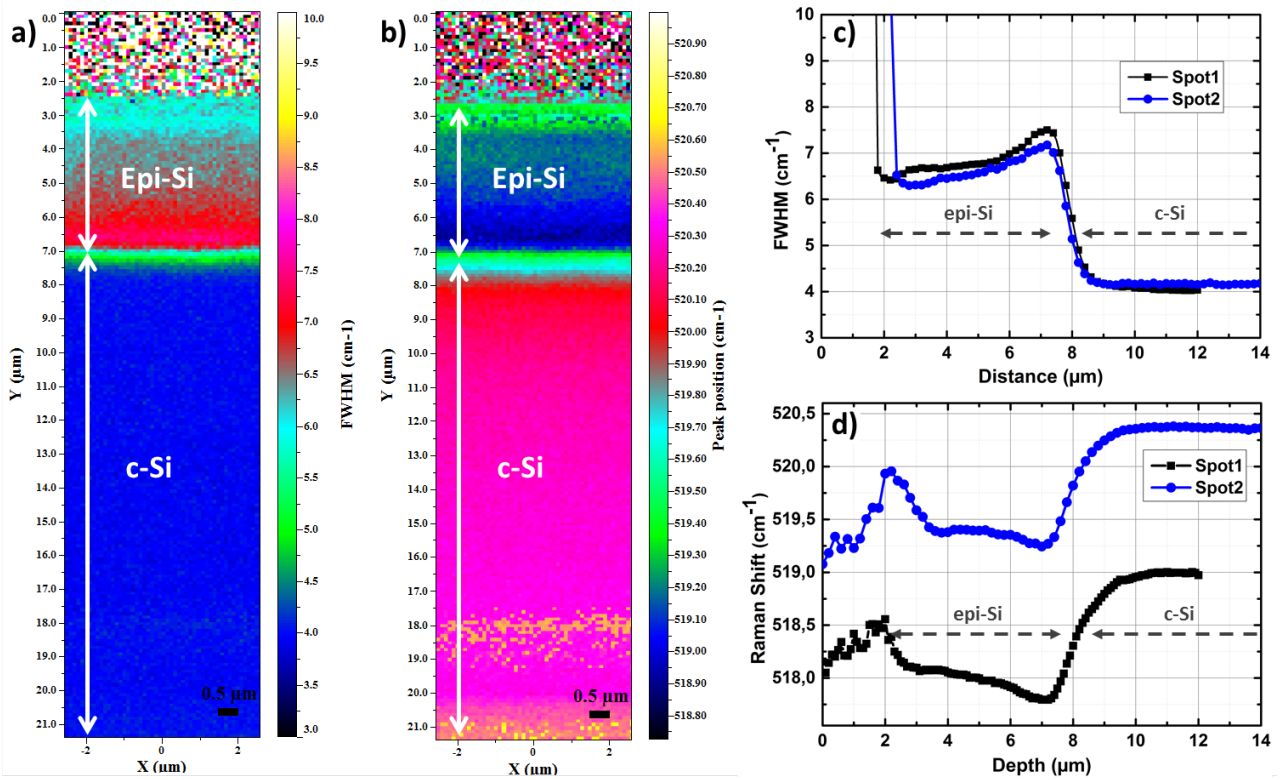


Fig. 3.21 – Raman cross section mappings of a 4 μm epitaxial sample on c-Si substrate. The FWHM map is shown on a) and the peak position map is shown on b). From top to bottom, epi-Si surface is visible at $\sim$2.5 μm and c-Si interface at $\sim$7 μm. c) and d) represent respectively the lateral average line scan of FWHM and peak position over maps a) and b). In both cases the measurement is done on 2 different spots of the same sample.

To sum up, a crystal quality improvement is detected by both real time in-situ ellipsometry measurements and cross section post-deposition Raman mapping. It happens likely because the interface is defective. In the presence of an atomically perfect interface, this effect would most likely disappear. From our measurements we can infer that the crystal defects rising from the interface do not propagate throughout the epi-layer, but are rather confined to the interface or progressively suppressed with the increasing epitaxial layer thickness. The physical explanation for this effect is not clear yet, but we can think of the beneficial healing effect of hydrogen[111] as a possible explanation, and also impurities level and outgassing may decrease with deposition time.

3.5.2 Influence of ion energy on crystal quality

Working at low temperature, the mobility of adsorbed species is drastically reduced compared to an epitaxial scenario at 800°C and beyond. Nevertheless, the characterization results presented in this chapter provide the clear evidence that even below 200°C, a monocrystal growth can be sustained over few microns. The missing piece of the puzzle, in other words the additional energy besides the thermal one, may originate from the combination of various physico-chemical processes. Since one of the specificities of PECVD environment is the presence of relatively low energy ions impinging on the sample surface, this process is likely meaningful. In the field of PVD deposition, this effect is already known and relatively well documented under the name of ion-assisted deposition (IAD). This approach is based on electron-gun evaporation and subsequent partial ionization of the silicon atoms. The created ions are accelerated toward the substrate with a typical energy of 20 eV, and

[111] H.-L. Thi Le et al., Chemical Physics Letters, **610-611**: 223–227, 2014.

excellent crystal quality with wafer like majority carrier electrical properties have been reported[112,113] for deposition temperatures slightly below 500°C. So in this section, we try to investigate the effect of ion energy on LTE; this work[114] was done with the fruitful partnership of B. Bruneau, presently PhD student at LPICM working on tailored voltage waveform plasmas.

Indeed, the effect of ion energy in PECVD epitaxy for temperatures below 200°C, and its variation with total pressure during deposition has not been studied to date. To address this issue, we performed PECVD epitaxial growth using a dilute SiH_4/H_2 mixture at different pressures: above 2 Torr, that is the deposition conditions used for the results mentioned previously in this manuscript, and below 1 Torr, namely 800 mTorr, assuming that the chemistry is supposed to be mainly driven by higher order silanes (Si_xH_y, with x>1, radicals or ions) above 2 Torr and by SiH_y radicals and ions below 1 Torr. Three different approaches were used to change the impinging ions energy: (i) tuning the plasma excitation waveform, (ii) applying a negative DC bias on the substrate, and (iii) increasing the RF power supplied to the plasma. In any case, the maximum kinetic energy a positive ion may acquire is determined by the difference between the plasma potential, V_{pl} and the substrate potential (often grounded). The influence on epitaxial growth quality was investigated by ellipsometry, Raman spectroscopy and cross sectional TEM. In all cases, the deposition was performed on (100) FZ c-Si wafers, cleaned either by HF-dipping of in-situ SiF_4 plasma.

Low pressure regime

For the low pressure regime, we used Tailored Voltage Waveforms (TVW) PECVD to vary the ion energy. By increasing the number of applied harmonics in capacitively coupled plasmas, TVW enable a good control over ion flux and ion energy[115–117]. In this pressure regime, the deposition was performed on Philix reactor. The waveform was here varied by playing on the phase shift, which results in change on the self-bias (V_{dc}). Thus this phase shift changes the potential drop between the plasma and the substrate, and consequently changes the maximum ion energy in the same way. The results of a series of samples deposited under epitaxial conditions by tuning the plasma potential, V_{pl}, from 9 V to 47 V with TVW, are shown on Fig.3.22. All films were about 1 μm in thickness. Fig.3.22-a) shows the spectroscopic ellipsometry (SE) measurements performed ex-situ, from which we extracted the amplitude of ε_i at 3.4 eV and 4.2 eV, i.e. the two characteristic peaks of crystalline silicon (left red axis). Raman spectroscopy was performed on the same samples with a 473 nm laser (having a penetration depth smaller than layer thickness), and the extracted Full Width at Half Maximum (FWHM) of the crystalline peak is plotted in grey (right axis). One can see that for V_{pl} below ∼30-35 V, ε_i is about 35 at 3.4 eV and 40 at 4.2 eV, which is characteristic of monocrystalline silicon, and that it decreases down to 20 when V_{pl} is increased above ∼ 35 V. This indicates that the epitaxial growth is lost when ion energy increases above. These results are consistent with Raman analysis, as the FWHM increases from about 6 cm^{-1} to 13 cm^{-1} when V_{pl} is increased, indicating lower crystalline domains size and more defects. The inset of Fig.3.22-a) shows the Raman spectra of samples deposited at V_{pl}=9 V (solid black line) and 47 V (dashed blue line). Not only an increase in the FWHM can be detected for V_{pl}=47 V, but this is also accompanied by the appearance of a broad shoulder at 480 cm^{-1}, which is the fingerprint of an amorphous phase. The above-mentioned transition was also detected by real time SE measurements, which were performed during the epitaxial growth, as shown in Fig.3.22-b,c) for samples deposited at V_{pl}=9 V and 47 V, respectively. At V_{pl}=9V, the growth is homogeneous and remains epitaxial throughout the deposition and at the contrariwise, for V_{pl}=47 V, the material changes during the deposition as demonstrated by the huge drop in ε_i amplitude corresponding to the loss of epitaxial growth. This is confirmed by cross-section Transmission Electron Microscopy (TEM)

[112] L. Oberbeck et al., Journal of Applied Physics, **88**: 3015–3021, 2000.
[113] T.A Wagner et al., Materials Science and Engineering: B, **89**: 319–322, 2002.
[114] B. Bruneau et al., IEEE Journal of Photovoltaics, **Early Access Online**: , 2014.
[115] B.G. Heil et al., Journal of Physics D: Applied Physics, **41**: 165202, 2008.
[116] T. Lafleur et al., Applied Physics Letters, **101**: 124104, 2012.
[117] B. Bruneau et al., Journal of Applied Physics, **115**: 084901, 2014.

images of these samples, shown on Fig.3.22-d,e): a low V_{pl} (9V) results in a monocrystalline material over the whole sample thickness whereas a high V_{pl} leads to the formation of an amorphous phase clearly visible in TEM image.

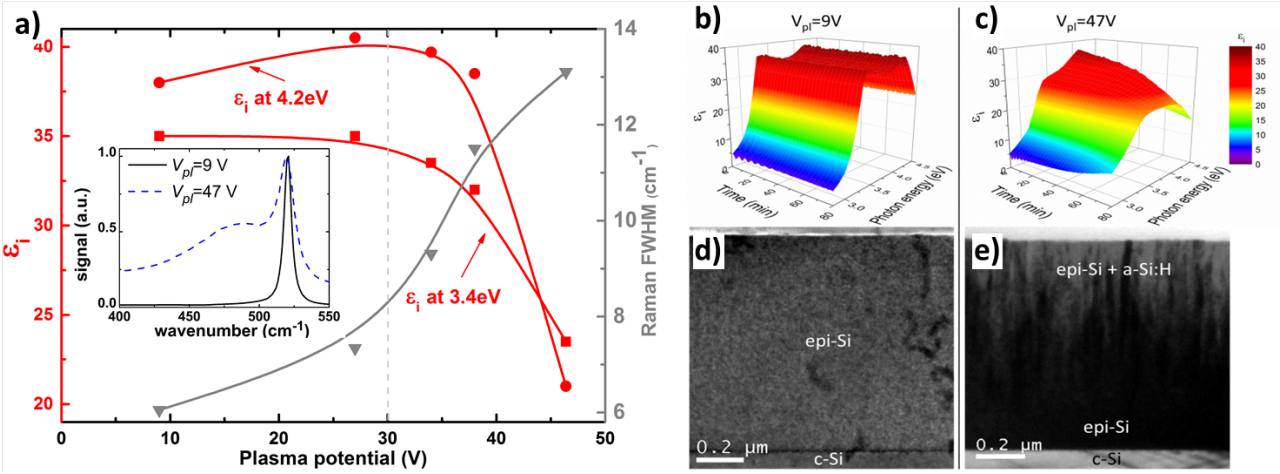


Fig. 3.22 – Series of samples deposited when changing the plasma potential (V_{pl}). a) Maxima of ε_i at 3.4 eV (left axis, circles) and 4.2 eV (left axis, squares), obtained by ellipsometry, and Raman FWHM (right axis, triangles), as a function of V_{pl}. The inset shows Raman spectra for samples deposited at V_{pl}=9 V (solid black line) and V_{pl}=47 V (dashed blue line). Time evolution of ε_i obtained by real time spectroscopic ellipsometry for: b) V_{pl} = 9 V, where epitaxial growth is visible, and c) V_{pl} = 47 V where epitaxial breakdown happens. TEM cross section images along <110> axis of samples: d) V_{pl}=9 V and e) V_{pl}=47 V.

Since the experimentally supported reason for the epitaxy breakdown under the plasma conditions of this study is the presence of SiH_x^+ ions with energy above 35 eV, one could expect a different behavior at higher pressure, for numerous reasons. Firstly, due to a more collisional sheath (for ions), fewer ions would arrive with the maximal energy V_{pl}. Secondly, due to the higher plasma density, the ions and molecules react to form Si_xH_y, with x>1 and clusters. With a change in the dominant Si ion, the energy threshold for the epitaxy breakdown could be modified.

High pressure regime

For the high pressure study, namely 2.3 Torr, the ion energy was changed by applying a DC bias on the RF electrode, in ARCAM reactor, as well as changing the power for classical sine wave excitation, in the cluster tool reactor. Fig.3.23-a) shows ε_i at 3.4 eV and 4.2 eV, as a function of the negative external bias V_{dc} applied to the RF electrode[118]. Samples were deposited simultaneously on the grounded electrode (blue) and on the RF electrode (red). Concerning the RF electrode, the maximum energy positive ions could get is equal to $V_{pl} + |V_{dc}|$. The absolute value of V_{dc} therefore gives a lower bound to the maximum ion energy arriving on the RF electrode. As V_{dc} is increased, the amplitude of the two peaks decreases for the samples deposited on the RF electrode, showing a lesser quality of epitaxy. On the grounded electrode, no significant change could be observed, possibly because the ion energy only slightly decreases on this electrode when $|V_{dc}|$ is increased.

To get more quantitative results on this effect, a second series of depositions was done for this high pressure regime, for which the power was changed from 5 W to 60 W and both the peak to peak voltage V_{pp} and the self-bias V_{dc} were monitored during deposition. From these quantities, one can obtain the plasma potential V_{pl}, namely the maximum energy an ion arriving on the grounded

[118] P. Roca i Cabarrocas. *Science des matériaux et techniques du réacteur dans le dépôt par procédé plasma RF de photopiles et d'autres dispositifs en silicium amorphe hydrogéné.* PhD thesis. Ecole Polytechnique, France, 1988.

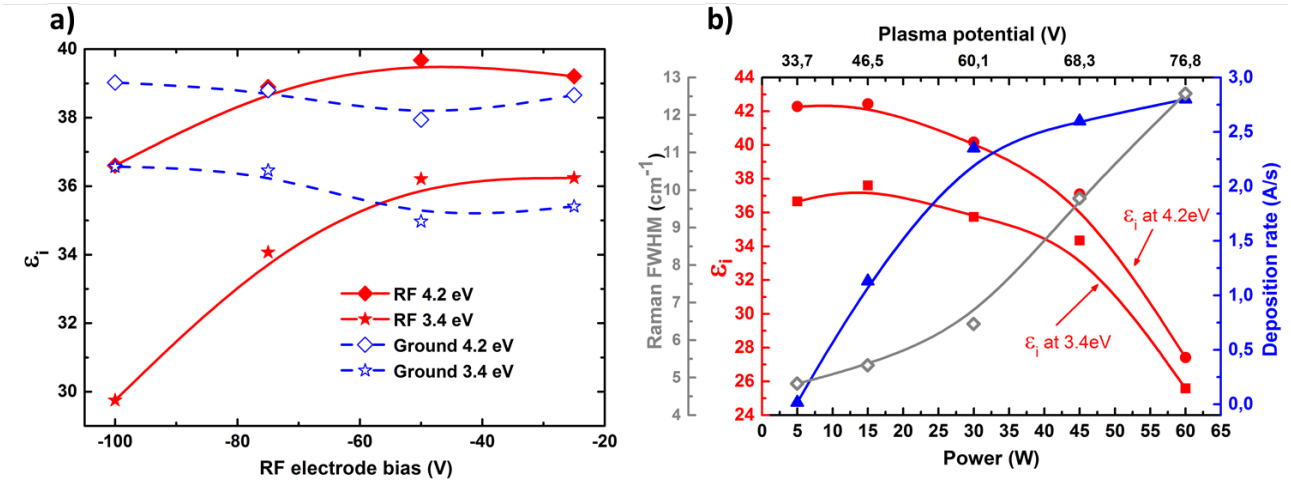


Fig. 3.23 – a) Amplitude of ε_i of the epitaxial layers at 3.4 eV (stars) and 4.2 eV (diamonds), measured by ellipsometry, as a function of the applied DC bias on the RF electrode. Samples are attached on RF (full red symbols) and grounded electrode (open blue symbols). b) Evolution of the deposition rate (right axis, blue triangles) and ε_i 3.4 eV and 4.2 eV peaks (left axis, red squares and circles) as a function of the coupled power (bottom axis), and the plasma potential (top axis). The second left axis shows the Raman FWHM (grey diamonds).

electrode could get, from the following expression: $\boldsymbol{V_{pl}} = 1/2.(\boldsymbol{V_{pp}}/2+\boldsymbol{V_{dc}})$. On Fig.3.23-b), the red curves show $\boldsymbol{\varepsilon_i}$ peak values as a function of the RF power (bottom x axis). The $\boldsymbol{V_{pl}}$, calculated from the above mentioned formula, is displayed on top x axis. Once again, the amplitude of the two $\boldsymbol{\varepsilon_i}$ peaks decreases when $\boldsymbol{V_{pl}}$ is increased. Thus, from the decrease of the amplitudes, one could expect a loss of epitaxy at high $\boldsymbol{V_{pl}}$. This is confirmed by the full width at half maximum (FWHM) of the crystalline peak obtained by Raman Spectroscopy (grey curve, second left axis), which increases significantly with $\boldsymbol{V_{pl}}$. The deposition rate is also reported on Fig.3.23-b), and it seems to reach a plateau at high RF power values, possibly due to a high depletion of silane (silane flow rate of 4 sccm). So to remove the possible influence of a fully depleted SiH_4 regime, some complementary depositions with a higher silane flow rate (7 sccm) for this high power regime were performed, and the epitaxial growth could not be sustained.

The crystal quality evolution with the $\boldsymbol{V_{pl}}$ has been further investigated with the Secco etching process[119]. This wet chemical etching process is known to reveal the dislocations and lattice defects, and thus is useful to characterize the epitaxial quality[120]. The friendly mixture is composed of both (a) the highly corrosive HF at 48% and (b) the extremely toxic $K_2Cr_2O_7$, 44,1g ([Cr]=0.3M) diluted in 1000mL, in the proportions (a):(b)=1:2. The etching rate is supposed to be around 25nm/s. The results of the Secco etching performed on the 15, 30 and 45W samples are shown on the SEM pictures displayed on Fig.3.24. The ratio indicated in the top left corner corresponds to the etched thickness over the initial film thickness, in nanometers. From this picture, the decreasing crystalline quality is directly visible with the higher pits and cracks density appearing for the increasing power. The 45W, full of cracks, is microcrystalline like, the 30W is monocrystalline with a high density of crystalline defects and the 15W has no visible defects at this scale, and thus crystalline defects density is lower than $\sim 8\times10^5 cm^2$.

However, compared to the low pressure scenario, one can see the signature of good epitaxial quality growth for $\boldsymbol{V_{pl}}$ as high as 45 V, indicating that the energy threshold observed in the low pressure regime, above which no epitaxy can be obtained, does not apply here. In addition, looking at the epitaxy under low $\boldsymbol{V_{pl}}$ in high and low pressure conditions, the high pressure seems to give better epitaxial quality as judged by $\boldsymbol{\varepsilon_i}$ peak amplitude and Raman FWHM. Overall, the impinging ion energy clearly

[119] F. Secco d'Aragona., J. Electrochem. Soc., **119**: 948–951, 1972.
[120] E. Schmich et al., Prog. Photovolt: Res. Appl., **16**: 159–170, 2008.

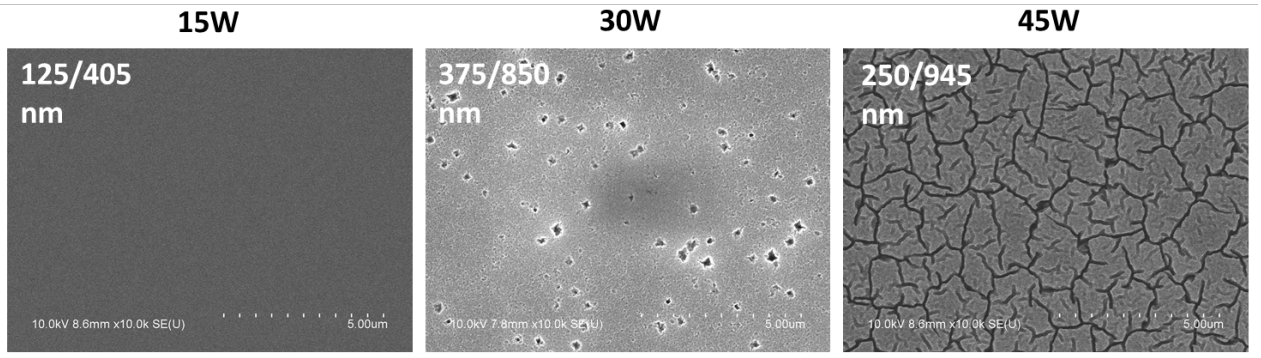


Fig. 3.24 – SEM picture of epi-Si samples after a Secco chemical etching step to reveal dislocations and lattice defects. The three samples are grown under 15, 30 and 45W of RF-power, and the top-left values on the picture refer to the ratio of etched film thickness over initial film thickness.

plays an important role in LTE, since in the two pressure conditions an upper bound is detected. The possible explanations for this effect are discussed in the next section.

3.6 Growth mechanism: an open discussion

Low temperature epitaxial growth in PECVD environment is not yet clearly understood. Indeed a lot of experiments are still needed to clarify the situation: plasma studies, in-situ time resolved surface analysis, etc. Also simulations (e.g. molecular dynamics) could strongly support such investigations. In any case, such fundamental studies were beyond the scope of this industrially funded PhD thesis work. So this section does not pretend to bring evidence of THE physical process explaining LTE, but rather discuss a possible interpretation scheme under the light of our experimental results and available literature.

3.6.1 The role of ions

As mentioned earlier, the role of ion energy has been particularly investigated by the ion beam epitaxy community. While in MBE the resulting film structure is mainly influenced by substrate temperature and atom arrival rate, in the ion assisted approach, the use of hyperthermal particles brings some flexibility. Both experiments and simulation results indicate that a controlled ion energy can significantly relax the lower temperature bound to sustain epitaxial growth. The possibility to lower the epitaxial growth temperature in the presence of kinetic ions is determined by a balance between beneficial effects, such as local relaxation or enhanced diffusion and detrimental effects such as lattice damage, sputtering etc. For example Rabalais et al.[47] used direct ion beam epitaxy from $^{28}Si^{+}$ ions on c-Si(100) to find the epitaxial window in the 8-80 eV energy range and 40-500°C temperature range. They found an effective energy window for epitaxial growth at low temperature, which broadened with the increasing temperature, as shown on Fig.3.25-a). Down to 150°C, the appropriate energy range is very narrow around 20 eV, at 200°C the range is around 15-25 eV, then the lower energy bound disappears around 300°C while the higher energy bound keeps increasing. This broadening with temperature is most likely explained by additional thermal vibrations and atomic mobility with increasing temperature.

Using molecular-dynamics algorithm, Hensel et al.[121] could confirm the beneficial effect of Si atoms of this energy range. In their calculation, based on a modified Stillinger-Weber potential for the Si atoms interaction, they studied 2 growth scenarios on a Si(100) 2×1 at 300K: i) a regular flux of 2 eV

[47] J.W. Rabalais et al., Phys. Rev. B, **53**: 10781–10792, 1996.
[121] H. Hensel et al., Phys. Rev. B, **58**: 2050–2054, 1998.

atoms ("MBE" scenario) and ii) a flux of 2 eV atoms with 2% admixture of 30 eV atoms ("IAD" scenario). They found that in the second case the growth stayed crystalline over many more mono-layers compared to the first case. They also concluded that bonds rearrangement rather than atom mobility seemed to be responsible for this epitaxial growth. Other molecular-dynamics simulations from Murty and Atwater suggested that 20 eV Argon ions induced surface displacement without damaging the bulk[122]. They concluded that the adatoms diffusion was not significantly enhanced, but that ion bombardment increased the formation rate of single adatoms. In another experimental study[123], they showed that ion irradiation could lead to hydrogen removal and beam-induced (2×1) reconstruction, on a dihydride terminated Si(100); and this monohydride surface is known to be more favorable for epitaxial growth.

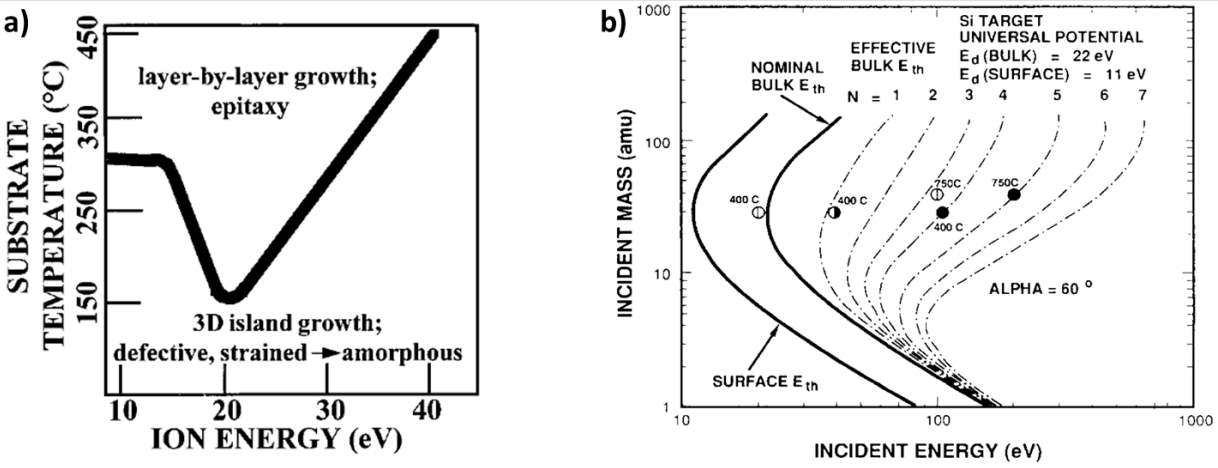


Fig. 3.25 – a) Substrate temperature vs ion-energy phase diagram for silicon homoepitaxy, from Rabalais et al.[47] b) Contours of surface and bulk displacement threshold energy in an incident-mass/incident-energy plane for a c-Si target. Data points show literature results for MBE growth where high quality crystal (open symbol), marginal epitaxial quality (half open circles) and poor film quality (filled circles) are obtained. From Brice et al.[124].

Interestingly enough, these energy values can be compared with fundamental constants of the crystalline silicon lattice such as surface and bulk displacement threshold. Some calculations for this effect were reported by Brice et al.[124] as shown in Fig.3.25-b). They present their results in an incident-mass/incident-energy plane, where the set of curves from left to right indicates the surface displacement threshold energy, the nominal bulk displacement energy, the effective bulk displacement energy (which takes into account the energy loss at the surface). Then the dash line curves correspond to a bulk displacement in the second mono-layer below the surface, the third, etc. From this graph one can see that the incoming particles with a mass closer to the Si atoms are the most efficient to induce displacement. In other words for a given incoming particle energy, the collision can induce more easily a surface displacement if the particle mass is close to the target Si atom mass. For a Si^+ ion impinging onto the crystalline lattice, the surface displacement threshold is in the range of 10-15 eV and the energy needed to displace an atom in the first sub-surface monolayer is around 30-35 eV. If a higher mass is considered (e.g. Si_xH_y with x>1) the surface and bulk threshold energy become higher. On the same graph, they have also reported MBE growth results where high quality is obtained (open symbols), marginal quality epitaxy (half open circles) and poor quality films (filled circles). Together these results suggest that a displacement on the surface or on the first sub-monolayer is beneficial for

[122] M.V. Ramana Murty et al., Physical Review B, **45**: 1507–1510, 1992.
[123] M. V. Ramana Murty et al., Applied Physics Letters, **62**: 2566–2568, 1993.
[124] D.K. Brice et al., Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, **44**: 68–78, 1989.

high quality epitaxy, and then displacement in the monolayers further below will reduce the epitaxy quality, unless high temperature is used (∼700°C), which allows defects to migrate and annihilate at the surface.

However, there is much less literature dealing with ion energy experimental work in PECVD environment. One can cite the work of Rosenblad et al.[23] in the late 1990's, in which an ion energy threshold for PECVD epitaxy at ∼10 mTorr and ∼500°C was reported: above 15 eV, a sharp increase in stacking fault density and surface roughness was observed.

In our case, as presented in the previous experimental section, only an upper bond threshold energies could be detected: around 30-35 eV for epitaxial growth at 800 mTorr and 50-55 eV at 2.3 Torr. These results are consistent with recent work on microcrystalline silicon[117], where a growth model has been proposed which indicates that SiH_x^+ ions with energy above 30 eV can locally change the crystalline orientation by displacing atoms in the bulk of the layer (i.e. below the surface), and prevent from epitaxial growth. Thus, unlike Rosenblad et al.[23], who found lower epitaxial quality above 15 eV, and unlike Rabalais et al.[47], who found no epitaxy below 15 eV at low temperature, we found no difference above and below 15 eV so far. Notwithstanding these apparent differences, the details of these experiments can account for these disperse findings. In the working conditions of Rabalais et al., only Si ions contribute to the growth. In PECVD environment, in SiH_4/H_2 chemistry, a lot of atomic hydrogen is present in the plasma. And as discussed in the next section, hydrogen can play important roles such as etching weak bonds or providing local annealing effect. This could be an argument for the non-detected lower energy bound of 15 eV. In the experiments of Rosenblad et al., first the pressure is much lower, thus a bigger fraction of incident ions are impinging the surface with the plasma potential energy, and second they also use argon ions which may have a different impact compared to Si ions. Our experimental results (Fig.3.22 and Fig.3.23) can be explained by following arguments:

- As the pressure is increased, the collision frequency in the sheath of the plasma increases significantly, which lowers the mean ion energy compared to the maximum ion energy (V_{pl}). In the high pressure regime, it is plausible to have a V_{pl} (and therefore a maximum ion energy) above 30-35 V (or eV), but with a negligible flux of ions with an energy above 30-35 eV. Therefore, the energy threshold condition would be relaxed towards higher V_{pl}.

- If the dominant ions are Si_xH_y, with x>1 at high pressure, the energy threshold, which depends on the mass of the incoming ion as shown on Fig.3.25-b), would be shifted to higher value. Indeed, the cross-section of the inelastic collision between an ion and the atoms of the layer, depends on the mass difference between the ion and the Si atom. Therefore, increasing the mass of the incoming ion should decrease the cross-section, and thus increase the energy threshold above which this ion can displace an atom in the layer (see Fig.3.25-b). And by looking at the problem with a different figure of merit, namely the energy per atom, the conclusion remains the same. Doubtlessly, the total energy of the particle, which cannot exceed V_{pl}, would then be divided into more atoms, mitigating the effect at hand. In addition, the higher the number of atoms in the ion, the easier to dissipate the kinetic energy internally, by vibrations for instance, favoring elastic collisions with respect to the inelastic collision.

While we cannot discriminate yet between these arguments; it seems indeed likely that both of the above-mentioned effects play a role in this ion energy shift observed at higher pressure.

If an increase of the deposition rate is to be targeted, then the ability to increase the ion and reactive species flux while keeping the ion energy below the above mentioned energy threshold is an essential feature. This may be realized using tailored voltage waveform instead of sine wave excitation,

[23] C. Rosenblad et al., Journal of Vacuum Science & Technology A, **16**: 2785–2790, 1998.
[117] B. Bruneau et al., Journal of Applied Physics, **115**: 084901, 2014.

if this gives enough decoupling on a large pressure range. But also, more easily, this could be achieved by using a higher frequency sine wave excitation, the so called VHF mode. With this latter technique, ions energy and ions flux are not independent, however higher frequencies are known to produce a higher current of less energetic ions compared to RF at 13.56 MHz[125]. This should be beneficial for LTE.

3.6.2 The role of hydrogen

The role of hydrogen in PECVD growth of μc-Si:H is often explained by three different effects, namely etching, surface diffusion and chemical annealing[126]. We discuss below on the suitability of these effects in the context of low temperature epitaxial growth.

Deposition/etching balance

One of the roles of atomic hydrogen in low temperature PECVD deposition is the etching of the weakly bonded silicon atoms, which are not in a crystallographic configuration for epitaxial growth. This etching phenomenon proceeds via the formation of volatile SiH_4 through a multi-step mechanism involving atomic hydrogen and SiH_x species at the surface[127]. The first argument to support this idea, is the fact that disordered materials, like a-Si:H, are etched faster in presence of atomic hydrogen compared to crystalline ones[19,128–130]. In their publication, Tsai et al.[19] proposed that the transition from microcrystalline to epitaxy and then to amorphous, as observed in Fig.3.6 in this PhD thesis, can be explained by a balance between film deposition and etching. The net reaction for this could be expressed as follow:

$$\mathbf{SiH_{x(plasma)} \underset{R_2}{\overset{R_1}{\rightleftharpoons}} Si_{(solid)} + xH_{(plasma)}} \tag{3.10}$$

A high dilution of SiH_4 in H_2 then pushes the reaction in the reverse direction: it increases R_2. In this case the growth rate is low and the fast etching creates some roughness and crystalline defects: this is the microcrystalline phase. A good balance between R_1 and R_2 corresponds to epitaxial growth conditions, with a higher deposition rate compared to μc-Si:H material. Then increasing further the SiH_4 flow rate will move the equilibrium toward lower etching effect, and thus a-Si:H material. The fact that a high dilution in inert gases instead of H_2, such as He, does not result in a growth rate reduction also supports this idea of etching balance.

Effect on adatoms mobility

Back in the 1990's, one can find nice experimental studies focusing on the role of molecular hydrogen in low temperature MBE Si epitaxial growth[67,131]. It was found that, below H desorption temperature, hydrogen significantly reduces the epitaxial critical thickness. The loss of epitaxy was believed to be linked to a progressive increase of surface roughness during growth. The hydrogen, by limiting surface diffusion of adatoms, was thus found to be indirectly responsible for the roughness and epitaxy breakdown. More recent studies have brought some contrasted conclusions: Ji et al.[132] claim that both SiH and SiH_2 surface units can block the Si adatom diffusion, and thus increase surface roughness, whereas Cereda et al.[133] found that hydrogen promoted ordered growth through various channels including etching promoted diffusion at T>300°C. In addition, some exchanges seem also

[125] A. Perret et al., Applied Physics Letters, **86**: 021501, 2005.
[126] J. Perrin., Journal of Non-Crystalline Solids, **137-138, Part 2**: 639–644, 1991.
[127] J. Abrefah et al., Surface Science, **209**: 291–313, 1989.
[19] C.C. Tsai et al., Journal of Non-Crystalline Solids, **114, Part 1**: 151–153, 1989.
[128] H.N. Wanka et al., Journal of Physics D: Applied Physics, **30**: L28, 1997.
[129] I. Solomon et al., Journal of Non-Crystalline Solids, **164-166, Part 2**: 989–992, 1993.
[130] F. Kail et al., Philosophical Magazine, **84**: 595–609, 2004.
[67] D.J. Eaglesham et al., Journal of Applied Physics, **74**: 6615–6618, 1993.
[131] S.H. Wolff et al., Applied Physics Letters, **55**: 2017–2019, 1989.
[132] J.-Y. Ji et al., Physical Review B, **70**: , 2004.
[133] S. Cereda et al., Physical Review Letters, **100**: 046105, 2008.

possible between the surface units and the adatom, in such a way that H is kept as a surfactant on the growth front. Anyhow, from those results, H-terminated surfaces did not seem to produce any surface diffusion enhancement effect. However in PECVD environment, precursors also come in the form of ions with a given energy, and thus the effect on surface diffusion in these conditions is less straightforward. For PECVD growth of μc-Si:H, H-coverage is indeed believed to provide surface diffusion enhancement[134].

Chemical annealing

Another role of atomic hydrogen is discussed in literature: this is the so-called chemical annealing[135]. The idea behind this is that some chemical surface reactions, such as hydrogen abstraction, can release a considerable energy, and thus enhance locally the effective surface temperature. For example let us consider the adsorption of atomic hydrogen on a Si surface dangling bond followed by the abstraction of the chemisorbed H by a second incident atomic H:

$$\mathbf{H_{at} + -Si \longrightarrow H-Si} \tag{3.11}$$

$$\mathbf{H_{at} + H-Si \longrightarrow H_2(g) + -Si} \tag{3.12}$$

Reaction (3.12) is about 1 eV exothermic, and has a relatively low activation energy. Based on the surface monohydride Si-H bond energy of $\sim$ 81 kcal/Mole and the H-H bond energy of $\sim$ 104 kcal/Mole, Koleske et al.[136] estimated the enthalpy change ($\mathbf{\Delta}$H) for the reactions (3.11) and (3.12) to be -104 kcal/Mole. Molecular dynamics simulations also concluded that atomic hydrogen produced a chemically induced ordering. More specifically, this could be through bond breaking and reforming reactions which are facilitated by H insertion and result in the suppression of strained Si-Si bonds.

Obviously, the experimental results shown in this chapter do not provide enough proof to fully support or rebut these three above-mentioned effects of hydrogen during the LTE Si growth. But they are still reasonable working hypothesis, and the field is still open for further experiments and simulations to clarify these phenomena.

3.6.3 The role of nanoparticles

At the beginning of this chapter, we have shown that epitaxial growth was un-intentionally obtained, on a limited thickness, at c-Si/a-Si:H interface when trying to passivate c-Si surface. Such a-Si:H deposition is usually performed at relatively low pressure ($\sim$ 50 mTorr), where cluster/powder formation in the plasma phase is often considered to be negligible. However the epitaxial growths performed in this doctoral thesis were under much higher pressure, namely 2-2.5 Torr, where plasma synthesized clusters are formed easily. Some similar deposition conditions are known to produce crystalline clusters embedded in an amorphous matrix when using a glass substrate, that is the so-called polymorphous silicon[137–139]. Those high pressure conditions were also reported to promote germanium epitaxial growth on GaAs in GeH_4/H_2 plasmas[17], and evidences of Ge nanocrystal could be observed on TEM grids[140]. Over the past years, the LPICM has produced many studies dealing with this topic, and the reader is advised to look into the following review papers[62,141] for more information.

[134] A. Matsuda., Thin Solid Films, **337**: 1–6, 1999.
[135] K. Nakamura et al., Jpn. J. Appl. Phys., **34**: 442, 1995.
[136] D.D. Koleske et al., The Journal of Chemical Physics, **99**: 5619–5622, 1993.
[137] P. Roca i Cabarrocas et al., Thin Solid Films, **403-404**: 39–46, 2002.
[138] K.-H. Kim. *Hydrogenated polymorphous silicon: establishing the link between hydrogen microstructure and irreversible solar cell kinetics during light soaking.* PhD thesis. Ecole Polytechnique, France, Oct. 2012.
[139] M. Khenkin et al., 39th IEEE Photovoltaic Specialists Conference (PVSC), 0563–0567, 2013.
[17] See next Chapter for more details.
[140] E.V. Johnson et al., Applied Physics Letters, **92**: 103108, 2008.
[62] P. Roca i Cabarrocas et al., Journal of Non-Crystalline Solids, **358**: 2000–2003, 2012.
[141] P. Roca i Cabarrocas et al., Journal of Physics D: Applied Physics, **40**: 2258–2266, 2007.

While the presence of plasma synthesized clusters (amorphous or crystalline) in our high pressure deposition regime is established, the question of how significantly they contribute to the epitaxial growth is still lacking direct experimental evidence. However molecular dynamic simulations may help to gain some insight into the possible mechanisms. First Brulin et al.[142] have shown that hydrogen may induce crystallization of clusters in the plasma phase, and Thi Le et al.[143] even came to the conclusion that plasma born clusters such as $Si_{29}H_{24}$ can reach their melting temperature (here $\sim$ 1650 K) as a result of reactions with atomic hydrogen. By simulating various types of cluster size and changing their impact energies on c-Si (100)-oriented surfaces, Ning et al.[144,145] could find some conditions where crystalline growth occurs. More details can be found in the PhD thesis of Thi Le[146]. The kinetic energy of impinging particles plays again a crucial role: the epitaxial growth seems to happen when the cluster impact energy is high enough to promote a phase transition to the liquid state for both cluster atoms and surface atoms involved in the collision. In addition, her simulations show the existence of an optimum incident angle (around 30°) for enhanced epitaxial efficiency, that enables a better spreading of the cluster's atoms at the surface, a larger surface diffusion and a better rearrangement in a crystalline way.

Clearly, it is not an easy task to bring strong experimental evidence of such growth mechanism. And since the above-mentioned mechanisms happen at the picosecond scale, this would probably require a highly precise spatial and time-resolved in-situ set-up. Thus, whether and how much the cluster-enhanced epitaxial growth mechanism can explain the low temperature epitaxial growth remains an open question.

[142] Q. Brulin et al., Journal of Non-Crystalline Solids, **352**: 1055–1058, 2006.
[143] H.-L. Thi Le et al., Phys. Status Solidi A, **211**: 294–300, 2014.
[144] N. Ning et al., Thin Solid Films, **517**: 6234–6238, 2009.
[145] N. Ning et al., The Journal of Physical Chemistry A, **114**: 3297–3305, 2010.
[146] H.-L. Thi Le. *Molecular dynamics simulations of H-induced plasma processes and cluster-catalyzed epitaxial growth of thin silicon films.* PhD thesis. Ecole Polytechnique, France, Jan. 2014.

3.7 Summary and perspectives

Takeaway Message - Low temperature RF-PECVD epitaxial growth

- Epitaxial growth at low temperature (150-350°C) by PECVD has been reported since the 1980's. However, the literature on this topic is relatively sporadic and, unlike other epitaxial growth techniques (CVD, MOCVD, MBE, etc.), it does not benefit from the expertise of a strong scientific community.
- In PECVD SiH_4/H_2 plasmas below 200°C, a high SiH_4 dilution results in μc-Si:H, a low SiH_4 dilution leads to a-Si:H. Epitaxial growth happens at the transition, and can be sustained up to several microns without breakdown. The monocrystal quality of the layer is confirmed by ellipsometry, Raman, TEM, XRD, etc.
- Dry plasma cleaning of native c-Si surface can be achieved using SiF_4 precursor at 175°C. This step advantageously removes the need of using HF-based wet chemical etching or high temperature steps prior to epitaxial growth.
- This LTE material is highly hydrogenated: H concentration may reach few times 10^{20} cm^{-3} for this "epi-Si:H" material. Hydrogen incorporation is responsible for platelets lying in (111) and (100) planes, and H-platelets induce some strain in the epi-Si:H layer. Consequently by tuning the H content (growth temperature, precursor dilution, etc.) the stress in the epi-layer can be tuned accordingly.
- Intrinsic LTE has a typical electron(hole) mobility of 400(125) $cm^2/(V.s)$. Bulk lifetime measured by standard μ-PCD technique is in the range of 100 μs. Those values are altered if the epi-layer is lifted-off and transferred. Superior electrical properties are expected for a growth temperature around 300-350°C.
- Material grown below 200°C is changing with thickness: under optimum epitaxial conditions the crystal quality improves from a slightly defective interface to the top of the layer. However un-optimized deposition parameters will result in epi-breakdown.
- The beneficial effects of hyperthermal particles on epitaxy are well-known in the ion beam assisted epitaxy community. In PECVD, the epitaxy breaks down above a pressure dependent energy threshold (30-35 eV at 0.8 Torr and 50-55 eV at 2.3 Torr). Those values can be compared to c-Si bulk displacement threshold energies. A temperature increase will enable sustained epitaxy for higher ions energy.
- Hydrogen has an important role in the growth process: etching of weak bonds, chemical annealing, etc. Possibly, plasma synthesized nano-particles have also a non-negligible role in this LTE growth.
- While epitaxial growth rates reported here are always in the range of 1-3 Å/s, there should not be any physical limitation to increase it by one order of magnitude at least. Raising the deposition temperature around 300-350°C and tuning independently the ion flux and ion energy would certainly help. This may be achieved by changing the plasma excitation frequency or wave form.
- PECVD LTE is not yet mature. The relative freshness of this scientific topic however means that there is room for interesting progress; for example, this LTE technique can be extended to other elements ($Si_{1-x}Ge_x$, III-V, etc.). Potentially a lot of applications can benefit from this field.

References

[1] G. Beaucarne, F. Duerinckx, I. Kuzma, K. Van Nieuwenhuysen, H. J. Kim, and J. Poortmans. Epitaxial thin-film Si solar cells. *Thin Solid Films*, **511-512**: 533–542, 2006. doi: 10.1016/j.tsf.2005.12.003 (see p. 38)

[2] C.W. Teplin, K. Alberi, M. Shub, C. Beall, I.T. Martin, M.J. Romero, D.L. Young, R.C. Reedy, P. Stradins, and H.M. Branz. Mechanisms controlling the phase and dislocation density in epitaxial silicon films grown from silane below 800°C. *Applied Physics Letters*, **96**: 201901–201901–3, 2010. doi: doi:10.1063/1.3422474 (see p. 38)

[3] D.J. Eaglesham, H.-J. Gossmann, and M. Cerullo. Limiting thickness h_{epi} for epitaxial growth and room-temperature Si growth on Si(100). *Physical Review Letters*, **65**: 1227, 1990. doi: 10.1103/PhysRevLett.65.1227 (see pp. 38, 51)

[4] J. Damon-Lacoste. *Vers une ingénierie de bandes des cellules solaires à hétérojonctions a-Si:H/c-Si. Rôle prépondérant de l'hydrogène.* PhD thesis. Ecole Polytechnique, France, July 2007. (see p. 38)

[5] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells.* PhD thesis. Ecole Polytechnique, France, May 2011. (see pp. 38, 39, 41, 42, 46, 66)

[6] A Fontcuberta i Morral, J Bertomeu, and P Roca i Cabarrocas. The role of hydrogen in the formation of microcrystalline silicon. *Materials Science and Engineering: B*, **69-70**: 559–563, 2000. doi: 10.1016/S0921-5107(99)00324-4 (see p. 38)

[7] S. Kasouit, S. Kumar, R. Vanderhaghen, P. Roca i Cabarrocas, and I. French. Fluorine and hydrogen effects on the growth and transport properties of microcrystalline silicon from SiF4 precursor. *Journal of Non-Crystalline Solids*, **299-302, Part 1**: 113–117, 2002. doi: 10.1016/S0022-3093(01)01187-5 (see p. 38)

[8] Y. Veschetti, J. C. Muller, J. Damon-Lacoste, P. Roca i Cabarrocas, A. S. Gudovskikh, J. P. Kleider, P. J. Ribeyron, and E. Rolland. Optimisation of amorphous and polymorphous thin silicon layers for the formation of the front-side of heterojunction solar cells on p-type crystalline silicon substrates. *Thin Solid Films*, **511-512**: 543–547, 2006. doi: 10.1016/j.tsf.2005.12.166 (see pp. 38, 41)

[9] P. Roca i Cabarrocas, Y. Djeridane, Th Nguyen-Tran, E. V. Johnson, A. Abramov, and Q. Zhang. Low temperature plasma synthesis of silicon nanocrystals: a strategy for high deposition rate and efficient polymorphous and microcrystalline solar cells. *Plasma Physics and Controlled Fusion*, **50**: 124037, 2008. doi: 10.1088/0741-3335/50/12/124037 (see p. 38)

[10] J. Damon-Lacoste and P. Roca i Cabarrocas. Toward a better physical understanding of a-Si:H/c-Si heterojunction solar cells. *Journal of Applied Physics*, **105**: 063712, 2009. doi: 10.1063/1.3091283 (see pp. 38, 41)

[11] S. De Wolf and M. Kondo. Abruptness of a-Si:H/c-Si interface revealed by carrier lifetime measurements. *Applied Physics Letters*, **90**: 042111, 2007. doi: 10.1063/1.2432297 (see pp. 39, 41)

[12] H. Fujiwara and M. Kondo. Effects of a-Si:H layer thicknesses on the performance of a-Si:H/c-Si heterojunction solar cells. *Journal of Applied Physics*, **101**: 054516–054516–9, 2007. doi: doi:10.1063/1.2559975 (see p. 39)

[13] J.J.H. Gielis, B. Hoex, P.J. van den Oever, M.C.M. van de Sanden, and W.M.M. Kessels. Silicon surface passivation by hot-wire CVD Si thin films studied by in situ surface spectroscopy. *Thin Solid Films*, **517**: 3456–3460, 2009. doi: 10.1016/j.tsf.2009.01.076 (see p. 39)

[14] T.J. Donahue, W.R. Burger, and R. Reif. Low-temperature silicon epitaxy using low pressure chemical vapor deposition with and without plasma enhancement. *Applied Physics Letters*, **44**: 346–348, 1984. doi: 10.1063/1.94754 (see p. 40)

[15] S. Suzuki and T. Itoh. Effect of SiGe buffer layer for low-temperature Si epitaxial growth on Si substrate by rf plasma chemical vapor deposition. *Journal of Applied Physics*, **54**: 1466–1470, 1983. doi: 10.1063/1.332173 (see p. 40)

[16] J.H. Comfort and R. Reif. Plasma-enhanced deposition of high-quality epitaxial silicon at low temperatures. *Applied Physics Letters*, **51**: 2016–2018, 1987. doi: 10.1063/1.98278 (see p. 40)

[17] K. Nagamine, A. Yamada, M. Konagai, and K. Takahashi. Epitaxial Growth of Silicon by Plasma Chemical Vapor Deposition at a Very Low Temperature of 250°C. *Jpn. J. Appl. Phys.*, **26**: L951, 1987. doi: 10.1143/JJAP.26.L951 (see pp. 40, 48)

[18] N. Shibata, K. Fukuda, H.irokazu Ohtoshi, J.-i. Hanna, S. Oda, and I. Shimizu. Preparation of Polycrystalline Silicon by Hydrogen-Radical-Enhanced Chemical Vapor Deposition. *Jpn. J. Appl. Phys.*, **26**: L10, 1987. doi: 10.1143/JJAP.26.L10 (see p. 40)

[19] C.C. Tsai, G.B. Anderson, R. Thompson, and B. Wacker. Control of silicon network structure in plasma deposition. *Journal of Non-Crystalline Solids*, **114, Part 1**: 151–153, 1989. doi: 10.1016/0022-3093(89)90096-3 (see pp. 40, 80)

[20] C.C. Tsai, G.B. Anderson, and R. Thompson. Low temperature growth of epitaxial and amorphous silicon in a hydrogen-diluted silane plasma. *Journal of Non-Crystalline Solids*, **137-138**: 673–676, 1991. doi: 16/S0022-3093(05)80210-8 (see pp. 40, 59, 63)

[21] T. Ohmi, K. Hashimoto, M. Morita, and T. Shibata. Study on further reducing the epitaxial silicon temperature down to 250°C in low-energy bias sputtering. *Journal of Applied Physics*, **69**: 2062–2071, 1991. doi: 10.1063/1.348732 (see p. 40)

[22] C.-H. Chen and T.-R. Yew. Silicon epitaxial growth by plasma enhanced chemical vapor deposition from SiH_4H_2 at 165-350 °C. *Journal of Crystal Growth*, **147**: 305–312, 1995. doi: 10.1016/0022-0248(95)80011-5 (see p. 41)

[23] C. Rosenblad, H. R. Deller, A. Dommann, T. Meyer, P. Schroeter, and H. von Känel. Silicon epitaxy by low-energy plasma enhanced chemical vapor deposition. *Journal of Vacuum Science & Technology A*, **16**: 2785–2790, 1998. doi: 10.1116/1.581422 (see pp. 41, 54, 79)

[24] J. Pla, E. Centurioni, C. Summonte, R. Rizzoli, A. Migliori, A. Desalvo, and F. Zignani. Homojunction and heterojunction silicon solar cells deposited by low temperature-high frequency plasma enhanced chemical vapour deposition. *Thin Solid Films*, **405**: 248–255, 2002. doi: 10.1016/S0040-6090(01)01709-6 (see pp. 41, 66)

[25] M. Farrokh-Baroughi and S. Sivoththaman. A Novel Silicon Photovoltaic Cell Using a Low-Temperature Quasi-Epitaxial Silicon Emitter. *IEEE Electron Device Letters*, **28**: 575–577, 2007. doi: 10.1109/LED.2007.897873 (see pp. 41, 66)

[26] R. Shimokawa, M. Yamanaka, and I. Sakata. Very Low Temperature Epitaxial Growth of Silicon Films for Solar Cells. *Japanese Journal of Applied Physics*, **46**: 7612–7618, 2007. doi: 10.1143/JJAP.46.7612 (see pp. 41, 66)

[27] J. Damon-Lacoste, M. Labrune, S. Granata, D. Daineka, and P. Roca i Cabarrocas. Crystalline silicon solar cells with doped epitaxial silicon films obtained at low-temperature by PECVD. *35th IEEE Photovoltaic Specialists Conference (PVSC)*, 001352–001357, 2010. doi: 10.1109/PVSC.2010.5614370 (see p. 41)

[28] H. Fujiwara and M. Kondo. Impact of epitaxial growth at the heterointerface of a-Si:H/c-Si solar cells. *Applied Physics Letters*, **90**: 013503–013503–3, 2007. doi: doi:10.1063/1.2426900 (see p. 41)

[29] M. KAMBARA, H. YAGI, M. SAWAYANAGI, and T. YOSHIDA. High rate epitaxy of silicon thick films by medium pressure plasma chemical vapor deposition. *Journal of Applied Physics*, **99**: 074901, 2006. DOI: 10.1063/1.2181279 (see p. 41)

[30] M. LABRUNE, M. MORENO, and P. ROCA I CABARROCAS. Ultra-shallow junctions formed by quasi-epitaxial growth of boron and phosphorous-doped silicon films at 175°C by RF-PECVD. *Thin Solid Films*, **518**: 2528–2530, 2010. DOI: 10.1016/j.tsf.2009.09.143 (see pp. 41, 66)

[31] M. MORENO and P. ROCA I CABARROCAS. Ultra-thin crystalline silicon films produced by plasma assisted epitaxial growth on silicon wafers and their transfer to foreign substrates. *EPJ Photovoltaics*, **1**: 6, 2010. DOI: 10.1051/epjpv/2010001 (see pp. 41, 46)

[32] R. CARIOU, M. LABRUNE, and P. ROCA I CABARROCAS. Thin crystalline silicon solar cells based on epitaxial films grown at 165°C by RF-PECVD. *Solar Energy Materials and Solar Cells*, **95**: 2260–2263, 2011. DOI: 10.1016/j.solmat.2011.03.038 (see p. 41)

[33] H.G. EL GOHARY and S. SIVOTHTHAMAN. Influence of different RTP temperature profiles on low temperature epitaxially grown PECVD Si emitters. *34th IEEE Photovoltaic Specialists Conference (PVSC)*, 001331–001334, 2009. DOI: 10.1109/PVSC.2009.5411264 (see p. 41)

[34] A. MOSLEH, S.A. GHETMIRI, B.R. CONLEY, H. ABU-SAFE, Z. WAQAR, M. BENAMARA, S.-Q. YU, and H.A. NASEEM. Nucleation-step study of silicon homoepitaxy for low-temperature fabrication of Si solar cells. *39th IEEE Photovoltaic Specialists Conference (PVSC)*, 2646–2650, 2013. DOI: 10.1109/PVSC.2013.6745017 (see pp. 41, 42, 48)

[35] D. SHAHRJERDI, B. HEKMATSHOAR, S. BEDELL, M. HOPSTAKEN, and D. SADANA. Low-Temperature Epitaxy of Compressively Strained Silicon Directly on Silicon Substrates. *Journal of Electronic Materials*, **41**: 494–497, 2012. DOI: 10.1007/s11664-011-1807-6 (see pp. 41, 48, 63, 66)

[36] B. HEKMATSHOAR, D. SHAHRJERDI, M. HOPSTAKEN, J.A. OTT, and D.K. SADANA. Characterization of thin epitaxial emitters for high-efficiency silicon heterojunction solar cells. *Applied Physics Letters*, **101**: 103906, 2012. DOI: 10.1063/1.4751339 (see p. 41)

[37] L. CSEPREGI, E. F. KENNEDY, J. W. MAYER, and T. W. SIGMON. Substrate-orientation dependence of the epitaxial regrowth rate from Si-implanted amorphous Si. *Journal of Applied Physics*, **49**: 3906–3911, 1978. DOI: 10.1063/1.325397 (see pp. 42, 55)

[38] B.E. WEIR, B.S. FREER, R.L. HEADRICK, D.J. EAGLESHAM, G.H. GILMER, J. BEVK, and L.C. FELDMAN. Low-temperature homoepitaxy on Si(111). *Applied Physics Letters*, **59**: 204–206, 1991. DOI: 10.1063/1.105966 (see p. 42)

[39] U.K. DAS, M.Z. BURROWS, M. LU, S. BOWDEN, and R.W. BIRKMIRE. Surface passivation and heterojunction cells on Si (100) and (111) wafers using DC and RF plasma deposited Si:H thin films. *Applied Physics Letters*, **92**: 063504, 2008. DOI: 10.1063/1.2857465 (see p. 42)

[40] C. ROLAND and G.H. GILMER. Epitaxy on surfaces vicinal to Si(001). I. Diffusion of silicon adatoms over the terraces. *Physical Review B*, **46**: 13428–13436, 1992. DOI: 10.1103/PhysRevB.46.13428 (see p. 42)

[41] F. STUCKI, J. A. SCHAEFER, J. R. ANDERSON, G. J. LAPEURE, and W. GOPEL. Monohydride and dihydride formation at Si(100) 2x1: A high resolution electron energy loss spectroscopy study. *Solid State Communications*, **47**: 795–801, 1983. DOI: 10.1016/0038-1098(83)90069-8 (see pp. 42, 43)

[42] J.J. BOLAND. Evidence of pairing and its role in the recombinative desorption of hydrogen from the Si(100)-2x1 surface. *Phys. Rev. Lett.*, **67**: 1539–1542, 1991. DOI: 10.1103/PhysRevLett.67.1539 (see p. 43)

[43] Y. WANG, M. SHI, and J. W. RABALAIS. Structure of the Si{100} surface in the clean (2x1), (2x1)-H monohydride, (1x1)-H dihydride, and c(4x4)-H phases. *Phys. Rev. B*, **48**: 1678–1688, 1993. DOI: 10.1103/PhysRevB.48.1678 (see p. 43)

[44] K. Yokoyama, T. Ochi, A. Yoshimoto, Y. Sugawara, and S. Morita. Atomic Resolution Imaging on Si(100)2x1 and Si(100)2x1:H Surfaces with Noncontact Atomic Force Microscopy. *Jpn. J. Appl. Phys.*, **39**: L113, 2000. doi: 10.1143/JJAP.39.L113 (see p. 43)

[45] S. Jeong and A. Oshiyama. Adsorption and Diffusion of Si Adatom on Hydrogenated Si(100) Surfaces. *Physical Review Letters*, **79**: 4425–4428, 1997. doi: 10.1103/PhysRevLett.79.4425 (see p. 43)

[46] J. Nara, T. Sasaki, and T. Ohno. Adsorption and Diffusion of Si Atoms on the H-Terminated Si(001) Surface: Si Migration Assisted by H Mobility. *Phys. Rev. Lett.*, **79**: 4421–4424, 1997. doi: 10.1103/PhysRevLett.79.4421 (see p. 43)

[47] J.W. Rabalais, A.H. Al-Bayati, K.J. Boyd, D. Marton, J. Kulik, Z. Zhang, and W.K. Chu. Ion-energy effects in silicon ion-beam epitaxy. *Phys. Rev. B*, **53**: 10781–10792, 1996. doi: 10.1103/PhysRevB.53.10781 (see pp. 43, 77–79)

[48] W. Kern. The Evolution of Silicon Wafer Cleaning Technology. *J. Electrochem. Soc.*, **137**: 1887–1892, 1990. doi: 10.1149/1.2086825 (see p. 43)

[49] E. Yablonovitch, D. L. Allara, C. C. Chang, T. Gmitter, and T. B. Bright. Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces. *Phys. Rev. Lett.*, **57**: 249–252, 1986. doi: 10.1103/PhysRevLett.57.249 (see p. 43)

[50] T. Takahagi, I. Nagai, A. Ishitani, H. Kuroda, and Y. Nagasawa. The formation of hydrogen passivated silicon single-crystal surfaces using ultraviolet cleaning and HF etching. *Journal of Applied Physics*, **64**: 3516–3521, 1988. doi: 10.1063/1.341489 (see p. 44)

[51] G.W. Trucks, K. Raghavachari, G.S. Higashi, and Y.J. Chabal. Mechanism of HF etching of silicon surfaces: A theoretical understanding of hydrogen passivation. *Physical Review Letters*, **65**: 504–507, 1990. doi: 10.1103/PhysRevLett.65.504 (see p. 44)

[52] M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, and M. Ohwada. Growth of native oxide on a silicon surface. *Journal of Applied Physics*, **68**: 1272–1281, 1990. doi: 10.1063/1.347181 (see p. 44)

[53] W Henrion, M Rebien, H Angermann, and A Rö seler. Spectroscopic investigations of hydrogen termination, oxide coverage, roughness, and surface state density of silicon during native oxidation in air. *Applied Surface Science*, **202**: 199–205, 2002. doi: 10.1016/S0169-4332(02)00923-6 (see p. 44)

[54] D.L. Flamm and V.M. Donnelly. The design of plasma etchants. *Plasma Chem Plasma Process*, **1**: 317–363, 1981. doi: 10.1007/BF00565992 (see p. 45)

[55] D.L. Flamm, C.J. Mogab, and E.R. Sklaver. Reaction of fluorine atoms with SiO2. *Journal of Applied Physics*, **50**: 6211–6213, 1979. doi: 10.1063/1.325755 (see p. 45)

[56] J.W. Coburn and H.F. Winters. Ion- and electron-assisted gas-surface chemistryâĂŤAn important effect in plasma etching. *Journal of Applied Physics*, **50**: 3189–3196, 1979. doi: 10.1063/1.326355 (see p. 45)

[57] R. Brenot. *Corrélation entre mode de croissance et propriétés de transport du silicium microcristallin, établie par réflectométrie micro-onde et ellipsométrie*. PhD thesis. Ecole Polytechnique, France, 2000. (see pp. 45, 67, 68)

[58] J.-C. Dornstetter, S. Kasouit, and P. Roca i Cabarrocas. Deposition of High-Efficiency Microcrystalline Silicon Solar Cells Using SiF /H /Ar Mixtures. *IEEE Journal of Photovoltaics*, **3**: 581–586, 2013. doi: 10.1109/JPHOTOV.2012.2221683 (see p. 45)

[59] M. Moreno, M. Labrune, and P. Roca i Cabarrocas. Dry fabrication process for heterojunction solar cells through in-situ plasma cleaning and passivation. *Solar Energy Materials and Solar Cells*, **94**: 402–405, 2010. doi: 16/j.solmat.2009.10.016 (see p. 45)

[60] M. MORENO, G. PATRIARCHE, and P. ROCA I CABARROCAS. Fine-tuning of the interface in high-quality epitaxial silicon films deposited by plasma-enhanced chemical vapor deposition at 200°C. *Journal of Materials Research*, **28**: 1626–1632, 2013. DOI: 10.1557/jmr.2013.52 (see p. 46)

[61] P. ROCA I CABARROCAS. A fully automated hot-wall multiplasma-monochamber reactor for thin film deposition. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, **9**: 2331, 1991. DOI: 10.1116/1.577318 (see pp. 46, 48, 49)

[62] P. ROCA I CABARROCAS, R. CARIOU, and M. LABRUNE. Low temperature plasma deposition of silicon thin films: From amorphous to crystalline. *Journal of Non-Crystalline Solids*, **358**: 2000–2003, 2012. DOI: 10.1016/j.jnoncrysol.2011.12.113 (see pp. 48, 50, 51, 81)

[63] G.E. JR JELLION, M.F. CHISHOLM, and S.M. GORBATKIN. Optical functions of chemical vapor deposited thin-film silicon determined by spectroscopic ellipsometry. *Applied Physics Letters*, **62**: 3348–3350, 1993. DOI: 10.1063/1.109067 (see p. 49)

[64] D.E. ASPNES and A.A. STUDNA. Dielectric functions and optical parameters of Si, Ge, GaP, GaAs, GaSb, InP, InAs, and InSb from 1.5 to 6.0 eV. *Physical Review B*, **27**: 985, 1983. DOI: 10.1103/PhysRevB.27.985 (see p. 49)

[65] G.E. JELLISON JR., V.I. MERKULOV, A.A. PURETZKY, D.B. GEOHEGAN, G. ERES, D.H. LOWNDES, and J.B. CAUGHMAN. Characterization of thin-film amorphous semiconductors using spectroscopic ellipsometry. *Thin Solid Films*, **377-378**: 68–73, 2000. DOI: 10.1016/S0040-6090(00)01384-5 (see p. 49)

[66] D.A.G. BRUGGEMAN. Berechnung verschiedener physikalischer Konstanten von heterogenen Substanzen. I. Dielektrizitätskonstanten und Leitfähigkeiten der Mischkörper aus isotropen Substanzen. *Annalen der Physik*, **416**: 636–664, 1935. DOI: 10.1002/andp.19354160705 (see p. 49)

[67] D.J. EAGLESHAM, F.C. UNTERWALD, H. LUFTMAN, D.P. ADAMS, and S.M. YALISOVE. Effect of H on Si molecular beam epitaxy. *Journal of Applied Physics*, **74**: 6615–6618, 1993. DOI: 10.1063/1.355101 (see pp. 51, 70, 80)

[68] P. ROCA I CABARROCAS, K.H. KIM, R. CARIOU, M. LABRUNE, E.V. JOHNSON, M. MORENO, A.T. RIOS, S. ABOLMASOV, and S. KASOUIT. Low Temperature Plasma Synthesis of Nanocrystals and their Application to the Growth of Crystalline Silicon and Germanium Thin Films. *MRS Proceedings*, **1426**: 319–329, 2012. DOI: 10.1557/opl.2012.1094 (see p. 51)

[69] L. SANSONNENS, A.A. HOWLING, and C. HOLLENSTEIN. A gas flow uniformity study in large-area showerhead reactors for RF plasma deposition. *Plasma Sources Science and Technology*, **9**: 205–209, 2000. DOI: 10.1088/0963-0252/9/2/314 (see p. 52)

[70] D.B. LEE. Anisotropic Etching of Silicon. *Journal of Applied Physics*, **40**: 4569–4574, 1969. DOI: 10.1063/1.1657233 (see p. 54)

[71] K.E. BEAN and K.E. BEAN. Anisotropic etching of silicon. *IEEE Transactions on Electron Devices*, **25**: 1185–1193, 1978. DOI: 10.1109/T-ED.1978.19250 (see pp. 54, 55)

[72] K.E. JENSEN, D. PENNACHIO, D. RECHT, D.A. WEITZ, and F. SPAEPEN. Rapid growth of large, defect-free colloidal crystals. *Soft Matter*, **9**: 320–328, 2012. DOI: 10.1039/C2SM26792F (see pp. 54, 55)

[73] M. SHIKIDA, K. SATO, K. TOKORO, and D. UCHIKAWA. Differences in anisotropic etching properties of KOH and TMAH solutions. *Sensors and Actuators A: Physical*, **80**: 179–188, 2000. DOI: 10.1016/S0924-4247(99)00264-2 (see p. 55)

[74] H. KROEMER, K.J. POLASKO, and S.C. WRIGHT. On the (110) orientation as the preferred orientation for the molecular beam epitaxial growth of GaAs on Ge, GaP on Si, and similar zincblende-on-diamond systems. *Applied Physics Letters*, **36**: 763–765, 1980. DOI: 10.1063/1.91643 (see p. 55)

[75] Y.-T. Lu and A.R. Barron. Anti-reflection layers fabricated by a one-step copper-assisted chemical etching with inverted pyramidal structures intermediate between texturing and nanopore-type black silicon. *J. Mater. Chem. A*, **2**: 12043–12052, 2014. doi: 10.1039/C4TA02006E (see p. 55)

[76] I. Zubel and M. Kramkowska. The effect of isopropyl alcohol on etching rate and roughness of (1 0 0) Si surface etched in KOH and TMAH solutions. *Sensors and Actuators A: Physical*, **93**: 138–147, 2001. doi: 10.1016/S0924-4247(01)00648-3 (see p. 56)

[77] D.B. Williams and C.B. Carter. *Transmission electron microscopy: a textbook for materials science*. Springer, 2009. (see p. 57)

[78] D. Delille, R. Pantel, and E. Van Cappellen. Crystal thickness and extinction distance determination using energy filtered CBED pattern intensity measurement and dynamical diffraction theory fitting. *Ultramicroscopy*, **87**: 5–18, 2000. doi: 10.1016/S0304-3991(00)00067-X (see p. 59)

[79] G. Moras, L.C. Ciacchi, C. Elsasser, P. Gumbsch, and A. De Vita. Atomically Smooth Stress-Corrosion Cleavage of a Hydrogen-Implanted Crystal. *Physical Review Letters*, **105**: 075502, 2010. doi: 10.1103/PhysRevLett.105.075502 (see p. 61)

[80] M. Bruel, B. Aspar, and A.-J. Auberton-Herve. Smart-Cut: A New Silicon On Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding[*1]. *Japanese Journal of Applied Physics*, **36**: 1636–1641, 1997. doi: 10.1143/JJAP.36.1636 (see p. 62)

[81] M. Bruel *Process for manufacturing thin film layers of semiconductor material* EP Patent App. EP19,920,402,520 1993 (see p. 62)

[82] S.T. Pantelides and F.A. Reboredo. Hydrogen Platelets in Crystalline Silicon - Precursors for the 'Smart Cut'. *Solid State Phenomena*, **69-70**: 83–92, 1999. doi: 10.4028/www.scientific.net/SSP.69-70.83 (see p. 62)

[83] Y. Zheng, S.S. Lau, T. Hochbauer, A. Misra, R. Verda, X.-M. He, M. Nastasi, and J.W. Mayer. Orientation dependence of blistering in H-implanted Si. *Journal of Applied Physics*, **89**: 2972–2978, 2001. doi: 10.1063/1.1334921 (see p. 62)

[84] T. Hochbauer, A. Misra, M. Nastasi, and J.W. Mayer. Physical mechanisms behind the ion-cut in hydrogen implanted silicon. *Journal of Applied Physics*, **92**: 2335–2342, 2002. doi: 10.1063/1.1494844 (see p. 62)

[85] X. Hebras, P. Nguyen, K.K. Bourdelle, F. Letertre, N. Cherkashin, and A. Claverie. Comparison of platelet formation in hydrogen and helium-implanted silicon. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, **262**: 24–28, 2007. doi: 10.1016/j.nimb.2007.04.158 (see p. 62)

[86] T. Roesener, V. Klinger, C. Weuffen, D. Lackner, and F. Dimroth. Determination of heteroepitaxial layer relaxation at growth temperature from room temperature X-ray reciprocal space maps. *Journal of Crystal Growth*, **368**: 21–28, 2013. doi: 10.1016/j.jcrysgro.2013.01.007 (see p. 62)

[87] I.D. Wolf. Micro-Raman spectroscopy to study local mechanical stress in silicon integrated circuits. *Semiconductor Science and Technology*, **11**: 139–154, 1996. doi: 10.1088/0268-1242/11/2/001 (see pp. 64, 65)

[88] S. Nakashima, T. Mitani, M. Ninomiya, and K. Matsumoto. Raman investigation of strain in Si/SiGe heterostructures: Precise determination of the strain-shift coefficient of Si bands. *Journal of Applied Physics*, **99**: 053512–053512–6, 2006. doi: doi:10.1063/1.2178396 (see p. 64)

[89] V.T. Srikar, A.K. Swan, M.S. Unlu, B.B. Goldberg, and S.M. Spearing. Micro-Raman measurement of bending stresses in micromachined silicon flexures. *Journal of Microelectromechanical Systems*, **12**: 779 –787, 2003. doi: 10.1109/JMEMS.2003.820280 (see p. 64)

[90] M. CHANDRASEKHAR, J.B. RENUCCI, and M. CARDONA. Effects of interband excitations on Raman phonons in heavily doped n-Si. *Physical Review B*, **17**: 1623–1633, 1978. DOI: 10.1103/PhysRevB.17.1623 (see p. 65)

[91] E. ANASTASSAKIS, A. CANTARERO, and M. CARDONA. Piezo-Raman measurements and anharmonic parameters in silicon and diamond. *Physical Review B*, **41**: 7529–7535, 1990. DOI: 10.1103/PhysRevB.41.7529 (see p. 65)

[92] W.A. BRANTLEY. Calculated elastic constants for stress problems associated with semiconductor devices. *Journal of Applied Physics*, **44**: 534–535, 1973. DOI: doi:10.1063/1.1661935 (see p. 65)

[93] H. KEPPNER, J. MEIER, P. TORRES, D. FISCHER, and A. SHAH. Microcrystalline silicon and micromorph tandem solar cells. *Appl Phys A*, **69**: 169–177, 1999. DOI: 10.1007/s003390050987 (see p. 65)

[94] S.J. DEBOER, V.L. DALAL, G. CHUMANOV, and R. BARTELS. Low temperature epitaxial silicon film growth using high vacuum electron-cyclotron-resonance plasma deposition. *Applied Physics Letters*, **66**: 2528–2530, 1995. DOI: 10.1063/1.113156 (see p. 65)

[95] S. CRISTOLOVEANU, I. IONICA, A. DIAB, and F. LIU. (Invited) The Pseudo-MOSFET: Principles and Recent Trends. *ECS Transactions*, **50**: 249–258, 2013. DOI: 10.1149/05005.0249ecst (see p. 65)

[96] H.E. GOHARY. *Development of Low-Temperature Epitaxial Silicon Films and Application to Solar Cells*. PhD thesis. University of Waterloo, Canada, Sept. 2010. (see p. 66)

[97] R.T. SAMADZADEH. *A Novel Buried-Emitter Photovoltaic Cell for High Efficiency Energy Conversion*. PhD thesis. University of Waterloo, Canada, Feb. 2013. (see p. 66)

[98] R.A. SINTON and A. CUEVAS. Contactless determination of current-voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data. *Applied Physics Letters*, **69**: 2510–2512, 1996. DOI: 10.1063/1.117723 (see p. 66)

[99] S. KASOUIT. *Mécanismes de croissance et transport dans le silicium microcristallin fluoré. Application aux transistors en couches minces et transfert technologique*. PhD thesis. Ecole Polytechnique, France, 2003. (see p. 67)

[100] M. KUNST, H.-C. NEITZERT, and A. SANDERS. Characterization of InP and GaAs films by contactless transient photoconductivity measurements. *Thin Solid Films*, **450**: 159–162, 2004. DOI: 10.1016/j.tsf.2003.10.063 (see p. 67)

[101] M. KUNST and G. BECK. The study of charge carrier kinetics in semiconductors by microwave conductivity measurements. *Journal of Applied Physics*, **60**: 3558–3566, 1986. DOI: doi:10.1063/1.337612 (see p. 67)

[102] K.L. LUKE and L.-J. CHENG. Analysis of the interaction of a laser pulse with a silicon wafer: Determination of bulk lifetime and surface recombination velocity. *Journal of Applied Physics*, **61**: 2282, 1987. DOI: doi:10.1063/1.337938 (see p. 67)

[103] A.W. STEPHENS, A.G. ABERLE, and M.A. GREEN. Surface recombination velocity measurements at the siliconâĂŞsilicon dioxide interface by microwave-detected photoconductance decay. *Journal of Applied Physics*, **76**: 363, 1994. DOI: doi:10.1063/1.357082 (see p. 67)

[104] A.B. SPROUL. Dimensionless solution of the equation describing the effect of surface recombination on carrier decay in semiconductors. *Journal of Applied Physics*, **76**: 2851, 1994. DOI: doi:10.1063/1.357521 (see p. 67)

[105] D. WALTER, P. ROSENITS, B. BERGER, S. REBER, and W. WARTA. Determination of the minority carrier lifetime in crystalline silicon thin-film material. *Progress in Photovoltaics: Research and Applications*, **22**: 180–188, 2014. DOI: 10.1002/pip.2242 (see pp. 68, 69)

[106] V. Depauw, Y. Qiu, K. Van Nieuwenhuysen, I. Gordon, and J. Poortmans. Epitaxy-free monocrystalline silicon thin film: first steps beyond proof-of-concept solar cells. *Progress in Photovoltaics: Research and Applications*, **19**: 844–850, 2011. doi: 10.1002/pip.1048 (see p. 69)

[107] D. Macdonald and A. Cuevas. Trapping of minority carriers in multicrystalline silicon. *Applied Physics Letters*, **74**: 1710–1712, 1999. doi: 10.1063/1.123663 (see p. 69)

[108] D.-H. Neuhaus, P.J. Cousins, and A G. Aberle. Trapping and junction-related perturbations of the effective excess carrier lifetime. *3rd World Conference on Photovoltaic Energy Conversion*, **1**: 91–94 Vol.1, 2003. (see p. 69)

[109] H.S. Radhakrishnan, F. Dross, M. Debucquoy, P. Rosenits, K. Van Nieuwenhuysen, I. Gordon, J. Poortmans, and R. Mertens. Evaluation of the influence of an embedded porous silicon layer on the bulk lifetime of epitaxial layers and the interface recombination at the epitaxial layer/porous silicon interface. *Progress in Photovoltaics: Research and Applications*, 2013. doi: 10.1002/pip.2336 (see p. 69)

[110] J. Thiesen, E. Iwaniczko, K. M. Jones, A. Mahan, and R. Crandall. Growth of epitaxial silicon at low temperatures using hot-wire chemical vapor deposition. *Applied Physics Letters*, **75**: 992–994, 1999. doi: 10.1063/1.124576 (see p. 70)

[111] H.-L. Thi Le, N.C. Forero-Martinez, and H. Vach. Hydrogen-induced healing of cluster-damaged silicon surfaces. *Chemical Physics Letters*, **610-611**: 223–227, 2014. doi: 10.1016/j.cplett.2014.07.034 (see p. 73)

[112] L. Oberbeck and R.B. Bergmann. Electronic properties of silicon epitaxial layers deposited by ion-assisted deposition at low temperatures. *Journal of Applied Physics*, **88**: 3015–3021, 2000. doi: doi:10.1063/1.1287530 (see p. 74)

[113] T.A Wagner, L Oberbeck, and R.B Bergmann. Low temperature epitaxial silicon films deposited by ion-assisted deposition. *Materials Science and Engineering: B*, **89**: 319–322, 2002. doi: 10.1016/S0921-5107(01)00807-8 (see p. 74)

[114] B. Bruneau, R. Cariou, J. Dornstetter, M. Lepecq, J.-L. Maurice, P. Roca i Cabarrocas, and E. Johnson. Ion Energy Threshold in Low-Temperature Silicon Epitaxy for Thin-Film Crystalline Photovoltaics. *IEEE Journal of Photovoltaics*, **Early Access Online**: 2014. doi: 10.1109/JPHOTOV.2014.2357256 (see p. 74)

[115] B.G. Heil, U. Czarnetzki, R.P. Brinkmann, and T. Mussenbrock. On the possibility of making a geometrically symmetric RF-CCP discharge electrically asymmetric. *Journal of Physics D: Applied Physics*, **41**: 165202, 2008. doi: 10.1088/0022-3727/41/16/165202 (see p. 74)

[116] T. Lafleur, P. A. Delattre, E. V. Johnson, and J. P. Booth. Separate control of the ion flux and ion energy in capacitively coupled radio-frequency discharges using voltage waveform tailoring. *Applied Physics Letters*, **101**: 124104, 2012. doi: 10.1063/1.4754692 (see p. 74)

[117] B. Bruneau, J. Wang, J.-C. Dornstetter, and E. V. Johnson. Growth mechanisms study of microcrystalline silicon deposited by SiH4/H2 plasma using tailored voltage waveforms. *Journal of Applied Physics*, **115**: 084901, 2014. doi: 10.1063/1.4866693 (see pp. 74, 79)

[118] P. Roca i Cabarrocas. *Science des matériaux et techniques du réacteur dans le dépôt par procédé plasma RF de photopiles et d'autres dispositifs en silicium amorphe hydrogéné.* PhD thesis. Ecole Polytechnique, France, 1988. (see p. 75)

[119] F. Secco d'Aragona. Dislocation Etch for (100) Planes in Silicon. *J. Electrochem. Soc.*, **119**: 948–951, 1972. doi: 10.1149/1.2404374 (see p. 76)

[120] E. Schmich, H. Lautenschlager, T. Friess, F. Trenkle, N. Schillinger, and S. Reber. n-Type emitter epitaxy for crystalline silicon thin-film solar cells. *Prog. Photovolt: Res. Appl.*, **16**: 159–170, 2008. doi: 10.1002/pip.783 (see p. 76)

[121] H. HENSEL and H.M. URBASSEK. Simulation of the influence of energetic atoms on Si homoepitaxial growth. *Phys. Rev. B*, **58**: 2050–2054, 1998. DOI: 10.1103/PhysRevB.58.2050 (see p. 77)

[122] M.V. RAMANA MURTY and H.A. ATWATER. Defect generation and morphology of (001) Si surfaces during low-energy Ar-ion bombardment. *Physical Review B*, **45**: 1507–1510, 1992. DOI: 10.1103/PhysRevB.45.1507 (see p. 78)

[123] M. V. RAMANA MURTY, HARRY A. ATWATER, A. J. KELLOCK, and J. E. E. BAGLIN. Very low temperature (400°C) silicon molecular beam epitaxy: The role of low energy ion irradiation. *Applied Physics Letters*, **62**: 2566–2568, 1993. DOI: 10.1063/1.109298 (see p. 78)

[124] D.K. BRICE, J.Y. TSAO, and S.T. PICRAUX. Partitioning of ion-induced surface and bulk displacements. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, **44**: 68–78, 1989. DOI: 10.1016/0168-583X(89)90690-3 (see p. 78)

[125] A. PERRET, P. CHABERT, J. JOLLY, and J.-P. BOOTH. Ion energy uniformity in high-frequency capacitive discharges. *Applied Physics Letters*, **86**: 021501, 2005. DOI: 10.1063/1.1848183 (see p. 80)

[126] J. PERRIN. Plasma and surface reactions during a-Si:H film growth. *Journal of Non-Crystalline Solids*, **137-138, Part 2**: 639–644, 1991. DOI: 10.1016/S0022-3093(05)80202-9 (see p. 80)

[127] J. ABREFAH and D. R. OLANDER. Reaction of atomic hydrogen with crystalline silicon. *Surface Science*, **209**: 291–313, 1989. DOI: 10.1016/0039-6028(89)90077-0 (see p. 80)

[128] H.N. WANKA and M.B. SCHUBERT. High silicon etch rates by hot filament generated atomic hydrogen. *Journal of Physics D: Applied Physics*, **30**: L28, 1997. DOI: 10.1088/0022-3727/30/8/002 (see p. 80)

[129] I. SOLOMON, B. DRÉVILLON, H. SHIRAI, and N. LAYADI. Plasma deposition of microcrystalline silicon: the selective etching model. *Journal of Non-Crystalline Solids*, **164-166, Part 2**: 989–992, 1993. DOI: 10.1016/0022-3093(93)91164-X (see p. 80)

[130] F. KAIL, A. FONTCUBERTA I MORRAL, A. HADJADJ, P. ROCA I CABARROCAS, and A. BEORCHIA. Hydrogen-plasma etching of hydrogenated amorphous silicon: a study by a combination of spectroscopic ellipsometry and trap-limited diffusion model. *Philosophical Magazine*, **84**: 595–609, 2004. DOI: 10.1080/14786430310001635440 (see p. 80)

[131] S.H. WOLFF, S. WAGNER, J.C. BEAN, R. HULL, and J.M. GIBSON. Hydrogen surface coverage: Raising the silicon epitaxial growth temperature. *Applied Physics Letters*, **55**: 2017–2019, 1989. DOI: 10.1063/1.102149 (see p. 80)

[132] J.-Y. JI and T.-C. SHEN. Low-temperature silicon epitaxy on hydrogen-terminated Si(001) surfaces. *Physical Review B*, **70**: 2004. DOI: 10.1103/PhysRevB.70.115309 (see p. 80)

[133] S. CEREDA, F. ZIPOLI, M. BERNASCONI, LEO MIGLIO, and F. MONTALENTI. Thermal-Hydrogen Promoted Selective Desorption and Enhanced Mobility of Adsorbed Radicals in Silicon Film Growth. *Physical Review Letters*, **100**: 046105, 2008. DOI: 10.1103/PhysRevLett.100.046105 (see p. 80)

[134] A. MATSUDA. Growth mechanism of microcrystalline silicon obtained from reactive plasmas. *Thin Solid Films*, **337**: 1–6, 1999. DOI: 10.1016/S0040-6090(98)01165-1 (see p. 81)

[135] K. NAKAMURA, K. YOSHINO, S. TAKEOKA, and I. SHIMIZU. Roles of Atomic Hydrogen in Chemical Annealing. *Jpn. J. Appl. Phys.*, **34**: 442, 1995. DOI: 10.1143/JJAP.34.442 (see p. 81)

[136] D.D. KOLESKE, S.M. GATES, and J.A. SCHULTZ. Facile abstraction of chemisorbed D on Si(100) by atomic H. *The Journal of Chemical Physics*, **99**: 5619–5622, 1993. DOI: 10.1063/1.465955 (see p. 81)

[137] P. Roca i Cabarrocas, A. Fontcuberta i Morral, and Y. Poissant. Growth and optoelectronic properties of polymorphous silicon thin films. *Thin Solid Films*, **403-404**: 39–46, 2002. DOI: 10.1016/S0040-6090(01)01656-X (see p. 81)

[138] K.-H. Kim. *Hydrogenated polymorphous silicon: establishing the link between hydrogen microstructure and irreversible solar cell kinetics during light soaking*. PhD thesis. Ecole Polytechnique, France, Oct. 2012. (see p. 81)

[139] M. Khenkin, A. Kazanskii, A. Emelyanov, P. Forsh, K.H. Kim, R. Cariou, and P. Roca i Cabarrocas. Structural, optical and photoelectric properties of hydrogenated polymorphous silicon. *39th IEEE Photovoltaic Specialists Conference (PVSC)*, 0563–0567, 2013. DOI: 10.1109/PVSC.2013.6744214 (see p. 81)

[140] E.V. Johnson, G. Patriarche, and P. Roca i Cabarrocas. Directional growth of Ge on GaAs at 175° using plasma-generated nanocrystals. *Applied Physics Letters*, **92**: 103108, 2008. DOI: 10.1063/1.2895636 (see p. 81)

[141] P. Roca i Cabarrocas, T. Nguyen-Tran, Y. Djeridane, A. Abramov, E. Johnson, and G. Patriarche. Synthesis of silicon nanocrystals in silane plasmas for nanoelectronics and large area electronic devices. *Journal of Physics D: Applied Physics*, **40**: 2258–2266, 2007. DOI: 10.1088/0022-3727/40/8/S04 (see p. 81)

[142] Q. Brulin, N. Ning, and H. Vach. Hydrogen-induced crystallization of amorphous silicon clusters in a plasma reactor. *Journal of Non-Crystalline Solids*, **352**: 1055–1058, 2006. DOI: 10.1016/j.jnoncrysol.2006.01.049 (see p. 82)

[143] H.-L. Thi Le, N.C. Forero-Martinez, and H. Vach. Heating and melting of plasma-born hydrogenated silicon clusters by reactions with atomic hydrogen. *Phys. Status Solidi A*, **211**: 294–300, 2014. DOI: 10.1002/pssa.201330337 (see p. 82)

[144] N. Ning, S.M. Rinaldi, and H. Vach. An atomic-scale study of hydrogenated silicon cluster deposition on a crystalline silicon surface. *Thin Solid Films*, **517**: 6234–6238, 2009. DOI: 10.1016/j.tsf.2009.02.086 (see p. 82)

[145] N. Ning and H. Vach. Deposition Dynamics of Hydrogenated Silicon Clusters on a Crystalline Silicon Substrate under Typical Plasma Conditions. *The Journal of Physical Chemistry A*, **114**: 3297–3305, 2010. DOI: 10.1021/jp909446c (see p. 82)

[146] H.-L. Thi Le. *Molecular dynamics simulations of H-induced plasma processes and cluster-catalyzed epitaxial growth of thin silicon films*. PhD thesis. Ecole Polytechnique, France, Jan. 2014. (see p. 82)

Chapter 4

Thin film PECVD epitaxial solar cells

Contents

Silicon solar cells have a long history[1] which started in 40's when Bell Telephone Laboratories Inc. patented the first "Light-sensitive electric device"[2], and in the mid 50's, with Bell Labs' first commercial silicon photovoltaic panel, which featured a power conversion efficiency of 5-6 %[1]. Research and development efforts have quickly raised efficiency up to 15% in 1960, and the significant progress achieved in the 90' resulted in a world record 24.7% for a PERL (passivated emitter, rear locally diffused) cell on a 400 μm p-type FZ substrate[3]. From 1999 to 2013, this record remained unbeaten: indeed the well-known value of 25% is nothing but the same above mentioned 24.7% record updated with the new reference solar spectrum[4]. In 2014, a small but nonetheless remarkable improvement was achieved: Panasonic Corporation succeeded to bring efficiency up to 25.6% with a completely different architecture[5]. Their results, presented at the conference IEEE-PVSC 40th in Denver, were obtained with an interdigitated back contact heterojunction solar cells for a 150 μm CZ n-type wafer, on a 143.7 cm^2 area. Parameters and small schematics of this two "historic" cells are shown in Fig.4.1.

	Wafer	Area [cm^2]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF [%]	η [%]
IBC HIT 2014 Panasonic	**150 µm CZ n-type**	**147.3**	**740**	**41.8**	**82.7**	**25.6**
PERL 1999 UNSW	**400 µm FZ p-type**	**4**	**706**	**42.7**	**82.8**	**25**

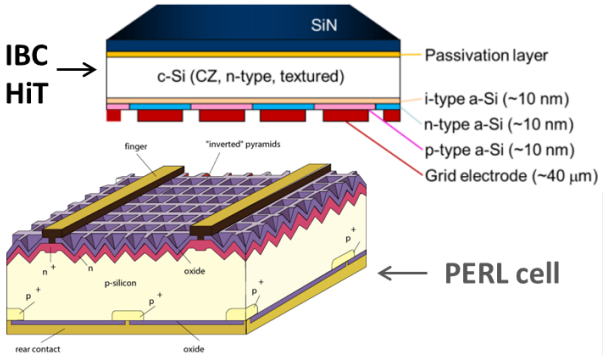


Fig. 4.1 – Schematics and diode parameters for the previous and actual silicon record cells: the UNSW PERL cell[4] and the Panasonic IBC HiT.[5]

The theoretical efficiency limit for silicon (E_g=1.12 eV), based on detailed balance calculations[6], is around 33%. However the unrealistic assumptions (infinite carrier mobility, complete absorption above the gap, etc.) of this approach over-estimate the result. More realistic calculations based on Si real absorption coefficient, including in addition the Auger recombination and the free carrier absorption, lead to a theoretical optimum of 29.8% for a 100 μm cell[7]. Indeed actual Si performances are relatively close to their maximum, and the very flat efficiency curve over the past 15 years confirms that this technology has come very close to its practical limitations. The challenge is now to produce high efficiency on large area and at low cost; at the cell level, this can be achieved by reducing the amount of material usage. Since the highly purified silicon required for the absorber layer is one of the main components of the panel cost, the general trend is to reduce the wafer thickness, as shown in Fig.4.1: between 1999 and 2014, the wafer thickness in record cells was reduced from 400 to 150 μm. Nowadays research focuses on silicon cells in the 1-50 μm range and this brings many challenges: i) finding new light trapping concepts to compensate for the incomplete absorption ii) achieving excellent passivation on both sides iii) producing and handling c-Si layer of few microns, etc. The previous chapter has shown an innovative way to produce thin film monocrystalline silicon layers, namely the low temperature PECVD epitaxy. In this chapter, we study the possibilities to use those epi-layers in few microns thick solar cells. After a brief literature overview, we first present the results of thin film epitaxial cells on wafer, and then expose the strategies tested to increase absorption: i) the use of germanium and ii)the lift-off and implementation of photonic nanostructures.

[1] M.A. Green., Progress in Photovoltaics: Research and Applications, **17**: 183–189, 2009.
[2] R.S. Ohl "Light-Sensitive Electric Device" pat. 2402662 U.S. Classification: 136/261 June 1946
[1] Science: Solar Batteries, Time magazine, 3 May 1954, Sun Electricity
[3] J. Zhao et al., Progress in Photovoltaics: Research and Applications, **7**: 471–474, 1999.
[4] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **17**: 85–94, 2009.
[5] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **22**: 1–9, 2014.
[6] W. Shockley et al., Journal of Applied Physics, **32**: 510, 1961.
[7] T. Tiedje et al., IEEE Transactions on Electron Devices, **31**: 711–716, 1984.

4.1 Challenges in reducing the silicon absorber thickness

On the one hand, there is the crystalline silicon solar cell technology, by far the dominant technology on the market, which can reach up to 25.6% at the cell level and module efficiency in the 23% range[5], and which require large thicknesses (150-200 μm) mostly to ease handling and processing. Crystalline silicon can reach high efficiency thanks to high minority-carrier lifetime, and c-Si based modules have an excellent long term stability. On the other hand, there are thin film silicon based technologies, using much less active material and lower processing cost, but reaching lower efficiencies, with the actual record being 16.3% initial efficiency for triple junction[8]. The bridge between these two technologies is thin film crystalline silicon solar cells[9], which can potentially combine the best of both worlds: i) high lifetime and high quality c-Si material and ii) lower processing cost and material usage. Indeed, thin film crystalline silicon has the potential to reduce material cost compared to current c-Si wafer technology, while at the same time avoiding material scarcity, toxicity and/or stability problems that are encountered by several thin film solar cell technologies[10]. A transition from wafer based cells to sub-50 μm device can seriously reduce the silicon consumption per watt: from ~4g/W for classical wafers (including kerf losses) to a projected ~0.2g/W. Thus research in this field is now focusing on three axes: i) Production of thin c-Si layers with a thickness of a 1-50 μm, ii) their transfer to low cost substrates, and iii) advanced light trapping schemes - such as plasmonic and photonic structures - to compensate transmission losses in ultra-thin layers. This section describes the state of the art results from literature, and challenges associated with this thickness reduction.

4.1.1 Overview of thin c-Si cells in literature

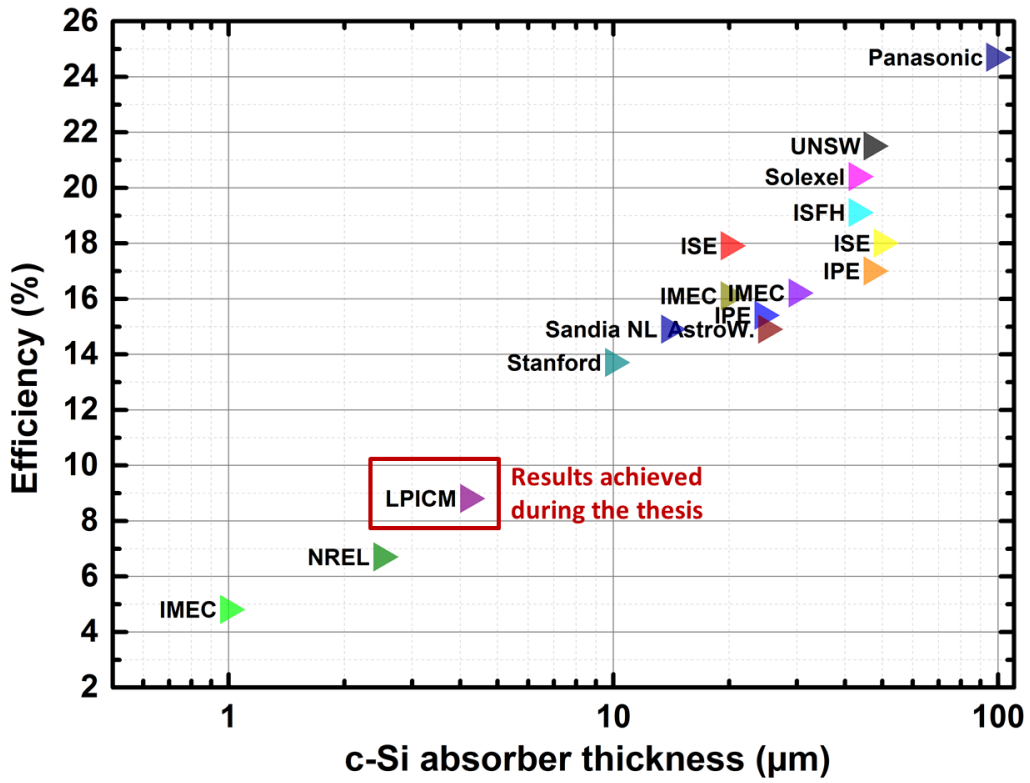


Fig. 4.2 – Monocrystalline silicon solar cells results from literature, plotted in a efficiency/absorber thickness plan. References and more details are shown in Fig.4.3

One of the important milestones in reducing c-Si absorber thickness was the proof of concept

[5] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **22**: 1–9, 2014.
[8] B. Yan et al., Applied Physics Letters, **99**: 113512–113512–3, 2011.
[9] F. Dross et al., Prog. Photovolt: Res. Appl., **20**: 770–784, 2012.
[10] V. Fthenakis., Renewable and Sustainable Energy Reviews, **13**: 2746–2750, 2009.

device reported by Wang et al.[11] in 1996. Starting from a thick high efficiency PERL cell (namely 400μm and 23.5%) they have performed chemical thinning to reduce the absorber thickness down to 47μm, and could achieve 21.5% efficiency, the losses being mainly due to a reduction of ~ 3 mA/cm^2 in the short circuit current. While this approach is not attractive from an industrial point of view, it was however a significant step forward in demonstrating that high efficiency is possible in sub-50 μm c-Si. On the top right corner of Fig.4.2 the 24.7% in 98μm milestone achieved by Panasonic in 2013, represents the state of the art result from wafer based technology[12]. Industry being rather conservative, it is often moving forward by small incremental steps, and c-Si PV technology has been following this wafer thinning path for a while now (see reports of International Technology Roadmap for Photovoltaic - ITRPV) . More innovative approaches are being explored for thicknesses in the 1-40 μm range; indeed producing and handling wafers around 100 μm becomes tricky, and in the few tens of μm range, the silicon is no longer self-supporting for classical wafer sizes[2]. Despite representing many different technologies, the best research results of Fig.4.2 are relatively well aligned in the semi-log plot; it underlines indeed the need for new light trapping concepts, and also raises the question of the upper trapping limit.

More details about those literature results are shown in Fig.4.3. The solar cell devices are classified according to their fabrication process: i) wafer based ii) wafer exfoliation or thinning iii) epitaxial lift-off and iv) epitaxial cells on wafer. Exfoliation or etching techniques have shown very good results so far, since the absorber itself is a part of its parent's wafer, and thus the material can have similar electrical quality (if separation process does not alter it). While the etching approach of Wang et al.[11] or Jeong et al.[13], who remove material starting from a 400 μm wafer and from a SOI wafer with 10 μm device layer respectively, is more a proof of concept, the exfoliation techniques are probably more industrially relevant since they may be performed several times on a same wafer/ingot. Saha et al.[14] use metal layers to create stress and control the exfoliation, Cruz-Campa[15] approach is based on lithography, masking and selective chemical etching of sub-surface layer, and Trompoukis[16] are using an epitaxy-free layer-transfer process based on the reorganization of macro-pores upon annealing. The two other categories, the wafer equivalent and epitaxial lift-off, are bottom up approaches. The idea is to grow the monocrystalline silicon absorber layer on a crystal seed (which shall be inexpensive and/or re-used). In most cases, the epitaxy itself is performed by CVD at 1100°C, and the lift-off, if any, is achieved thanks to a fragile porous silicon layer below the surface created by electrochemical HF bath prior to epitaxial growth[17–23]. An alternative epitaxial technique to produce c-si layers of few microns, namely HWCD around 700°C, is being explored at NREL in the group of Branz et al.[24,25]. Our innovative approach lies in the fact that we use a very low epitaxy temperature (<200°C) to produce the monocrystalline absorber[26]; this type of device will be explained in details in the next section.

[11] A. Wang et al., Progress in Photovoltaics: Research and Applications, **4**: 55–58, 1996.
[12] M. Taguchi et al., IEEE Journal of Photovoltaics, **4**: 96–99, 2014.
[2] e.g. A 25μm 4 inch c-Si wafer holded with tweezers will bend and break (alternatively will be ok) if the surface is parallel (alternatively perpendicular) to the ground.
[13] S. Jeong et al., Nature Communications, **4**: , 2013.
[14] S. Saha et al., MRS Online Proceedings Library, **1493**: 51–58, 2013.
[15] J.L. Cruz-Campa et al., Solar Energy Materials and Solar Cells, **95**: 551–558, 2011.
[16] C. Trompoukis et al., Applied Physics Letters, **101**: 103901–103901–4, 2012.
[17] P. Kapur et al., 28th EU PVSEC Proceedings, **3DO.7.6**: 2228 –2231, 2013.
[18] J.H. Petermann et al., Progress in Photovoltaics: Research and Applications, **20**: 1–5, 2012.
[19] M. Reuter et al., Solar Energy Materials and Solar Cells, **93**: 704–706, 2009.
[20] R.B. Bergmann et al., Solar Energy Materials and Solar Cells, **74**: 213–218, 2002.
[21] P. Rosenits et al., Thin Solid Films, **519**: 3288–3290, 2011.
[22] I. Kuzma-Filipek et al., Progress in Photovoltaics: Research and Applications, **20**: 350–355, 2012.
[23] K. Van Nieuwenhuysen et al., Thin Solid Films, **518**: S80–S82, 2010.
[24] H.M. Branz et al., Thin Solid Films, **519**: 4545–4550, 2011.
[25] K. Alberi et al., Applied Physics Letters, **96**: 073502, 2010.
[26] R. Cariou et al., 28th EU PVSEC Proceedings, **3DO.7.5**: 2225 –2227, 2013.

	Research group	Epitaxy	Thick [µm]	Solar cell parameters V_{oc} [mV]	J_{sc} [mA/cm²]	FF [%]	η [%]	Details
wafer	Panasonic – Taguchi et al. (2014)	-	98	750	39.5	83.2	24.7	HiT cell on thin wafer
Exfoliation or etching	UNSW – Wang et al. (1996)	-	47	698	37.9	81.1	21.5	Wafer chemical thinning, PERL cell
	AstroWatt inc. – Saha et al.(2013)	-	25		34.4		14.9	Lift off: patented kerfless exfoliation technique from parent wafer
	Sandia NL – Cruz-Campa et al. (2011)	-	14	597	31.8	78.4	14.9	250 µm wide IBC cell etched from wafer
	Standford – Jeong et al. (2013)	-	10	623	29	76	13.7	10 µm SOI layer, carrier wafer etched. IBC cell nanocones light trapping.
	IMEC – Trompoukis et al. (2012)	-	1	434	15.5	72	4.8	HiT cell with NIL on Epi-free
Epitaxial lift off	Solexel inc. – Kapur et al. (2014)	CVD	43			80.1	20.4	Lift off
	ISFH – Petermann et al. (2012)	CVD, 1100°C	43	650	37.8	77.6	19.1	Lift off, transfer from porous silicon, random pyramids, PERC cell
	IPE – Reuter et al. (2009)	CVD	47	634	36	74.6	17	Lift off, transfer from porous silicon, epitaxial BSF & emitter
	IPE – Bergmann et al. (2002)	CVD, 1100°C	46.5 24.5	645 636	32.8 30.4	78.2 79.7	16.6 15.4	Lift off, transfer from porous silicon, random pyramids, epitaxial BSF
Wafer equivalent approach	Fraunhofer ISE – Rosenits et al. (2011)	CVD, 1100°C	50 20	631 626	36.1 35.9	79 79.6	18 17.9	Standard diffused emitter, no surface texture
	IMEC – Kuzma-filipek et al. (2012)	CVD, 1100°C	30	633.6	31.7	80.8	16.2	Porous back reflector, epitaxial BSF + emitter base. Diffused emitter.
	IMEC – Van Nieuwenhuysen et al. (2010)	CVD, 1100°C	20	621	33.2	78.0	16.1	Porous back reflector, BSF, epitaxial base & emitter, plasma surface texture
	NREL – Branz et al. (2011)	HWCVD, 760°C	2.5	550	18	68	6.7	No surface texture
	LPICM – R. Cariou et al. (2013)	RF-PECVD, 175°C	4.2	539	20.2	80.5	8.8	No surface texture

Fig. 4.3 – Thin film crystalline silicon solar cells results from literature, classified according to their production process and by decreasing efficiency. Data extracted from Ref.[11–24,26]

4.1.2 Absorption and short-circuit current in thin film c-Si

With silicon's indirect band gap, the incomplete optical absorption in thin film c-Si ($\lesssim$50 μm) is a real issue: an insufficient electron-hole (e-h) pair generation clearly limits the short circuit current (J_{sc}) of the device. If we consider a slice of material of thickness d, with $\alpha(E)$ being the energy dependent optical absorption coefficient, the absorbance for a single light path (sp) is equal to: $a_{sp}(E) = 1 - e^{-\alpha(E)\,d}$. In Fig.4.4-a), the right and bottom axis show, in grey shade, the AM1.5 G-173 standard solar spectrum as a function of wavelength. The fraction of the photon flux that can be absorbed in a single pass through 1, 3, 10, 50, 100 μm c-Si slab, are shaded with different colors. The AM1.5 G-173 photon flux is here converted into ideal J_{sc} per wavelength (mA/[cm^2.nm]), according to the following assumptions: i) zero reflection losses (R=0) and ii) 100% internal quantum efficiency (IQE=1), i.e. every created e-h pair is collected. By integrating over the entire spectrum one can calculate the ideal J_{sc} as a function of absorber thickness. The result is displayed in Fig.4.4-a) top and left axis: for example the ideal single pass J_{sc} (black line, triangles) of a 3 μm c-Si absorber reaches the relatively low value of 20.5 mA/cm^2, and several hundred are needed to go above 42 mA/cm^2.

It is hopefully possible to increase significantly the absorbance (for material with index >1) by using light trapping solutions such as non-specular textured surface and back reflectors. By introducing some roughness (at front and/or back cell's surface) the light is deflected away from the angle of incidence and remains trapped until it is either absorbed or scattered back into the escape cone. Thus from a ray optics perspective, the conventional light trapping effect is based on total internal reflection between the semiconductor material and the surrounding medium; this results in a much longer propagation distance, and thus a significant absorption enhancement. It can be shown[27] that

[27] E. Yablonovitch., Journal of the Optical Society of America, **72**: 899–907, 1982.

the maximum enhancement factor in this ray optics approach is $4n^2/\sin^2(\theta)$, where θ is the angle of the emission cone for the semiconductor with index n, in a given surrounding medium. A Lambertian surface ensures a perfect randomization of light scattering events[28], and this isotropic response results in θ=90°, thus the maximum enhancement factor becomes $4n^2$, often called Lambertian or Yablonovitch limit. This $4n^2$ limit is valid under three main assumptions: i) the transmitted or reflected light is randomized with isotropic angular distribution at every energy ii) the weak absorption regime is verified $4n^2\alpha(E)d \ll 1$ and iii) the ray optics is valid, i.e. the film thickness d and the light trapping features periodicity is much larger than the wavelength λ/n in the semiconductor material. The corresponding maximum enhancement factor for silicon under this assumptions is $4n^2$=50. More recently, an analytic expression for light path enhancement in the case of arbitrary absorption has been calculated by M. Green[29]. In fact the maximum absorption enhancement is lower when the weak absorption assumption is relaxed. If light trapping features and film thickness become closer to the wavelength scale, those above mentioned Yablonovitch and Green limits are no longer valid, and the light needs to be treated as a wave, this is the so-called photonic regime[30–33].

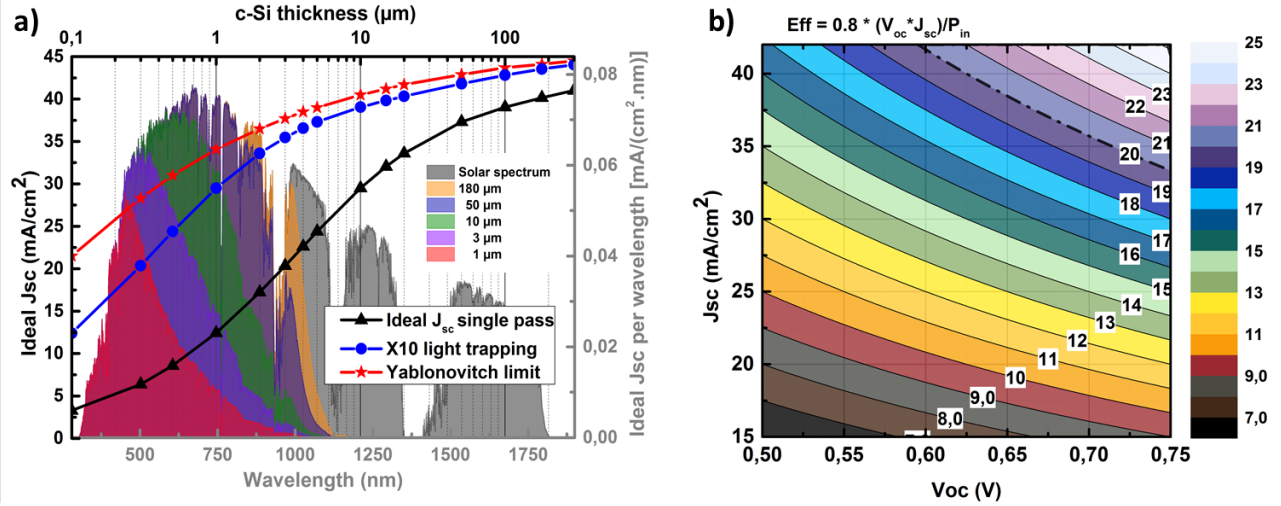


Fig. 4.4 – a) Ideal current density per wavelength for AM1.5G solar spectrum (bottom & right axis, grey shade). Single pass absorption of c-Si slab with 1, 3, 10, 50 and 100 μm are shaded in colors. By integration, the ideal J_{sc} (R=0 and IQE=1) is calculated for single path (top & left axis, triangles), ×10 light trapping (circles) and $4n^2$ Yablonovitch limit (stars). b) shows the efficiency map in V_{oc}/J_{sc} plan for a device with 80% fill factor.

Using the classic ray optics approach, light path enhancements of 10 to 20 times are routinely achieved with random pyramids of few microns etched on c-Si(100), as presented in the previous chapter (see Fig.3.11). The ideal J_{sc} as a function of thickness for the case of ×10 (circles) and $4n^2$ limit (stars) is shown in Fig.4.4-a). This shows that light trapping enables to significantly enhance the current over the whole 1-100 μm range. Looking more specifically at an absorber thickness of 3μm (typical value for PECVD LTE cells of this chapter), we can compare the ideal current density in the 3 above-mentioned light trapping scenarios: i) the single pass gives 20.5 mA/cm^2, ii) the ×10 result in 35.5 mA/cm^2 and iii) a Lambertian light trapping limit leads to 37.7 mA/cm^2. A rough estimation of achievable efficiencies for such a thin c-Si slab can be deduced from Fig.4.4-b), where the contour map of efficiency in a V_{oc}/J_{sc} plan is shown, assuming a fill factor of 80% (Eff.=0.8.V_{oc}.J_{sc}/P$_{in}$). Reaching 20% efficiency in such device requires: i) V$_{oc}$ ~675 mV and the hard to achieve J_{sc} of 37.7 mA/cm^2,

[28] P. Sheng., IEEE Transactions on Electron Devices, **31**: 634–636, 1984.
[29] M.A. Green., Progress in Photovoltaics: Research and Applications, **10**: 235–241, 2002.
[30] H.A. Atwater et al., Nature Materials, **9**: 205–213, 2010.
[31] Z. Yu et al., Opt. Express, **18**: A366–A380, 2010.
[32] A. Polman et al., Nature Materials, **11**: 174–177, 2012.
[33] A. Bozzola et al., Opt. Express, **20**: A224–A244, 2012.

or ii) V_{oc} ∼720 mV if the current is 35 mA/cm^2 (that is roughly a ×10 light trapping). Tiedje at al.[7] have shown that, for an hypothetical solar cell in which the only loss mechanisms are radiative and Auger recombinations, and free carrier absorption, the V_{oc} is increasing with decreasing thickness: the open circuit voltage is expected to increase from ∼760 mV at 100 μm to above 800 mV for a 10 μm thin absorber. Apart from the 747 mV in a 58 μm wafer reported by Sanyo (now Panasonic) in 2011[34], this is in contrast with all the V_{oc} achieved so far in sub-50μm devices which are more in the 620 to 650 mV range (see Fig.4.3). This discrepancy is explained by the fact that Tiedje et al. ignore the surface recombination issues; indeed surface passivation becomes more critical for thinner devices, especially for high aspect ratio light trapping features which enhance by several times the actual surface area compared to the projected surface (flat case). So even if their predicted efficiency decreases only by ∼ 1.5% absolute when the absorber is reduced from 100 μm (29.8%) down to 10 μm, achieving both high light path enhancement and excellent surface passivation is very challenging. A highly demanding but achievable target could be 15% for 5-10 μm c-Si absorber and 20% for a ∼10-15 μm absorber.

4.2 Low temperature PECVD epitaxial solar cells

Nowadays, silicon has a comfortable (> 80%) share of the market and it will most probably remain the dominant technology for the next decades. As already mentioned, it is abundant, non-toxic and has a strong industrial background; consequently, cost reduction is the next challenge for un-subsidized TW scale deployment. The silicon still represents more than ∼ 40% of the cost of c-Si PV modules, because of the costly steps: - production of Si feed stock material from silane or trichlorosilane - Ingot growth at T>1400°C - kerf losses of about 50% during sawing, etc. Therefore it will be difficult to decrease Si PV cost significantly without eliminating the wafer as we know it today; innovating concepts that save materials and drive down the cost while keeping high efficiencies are needed. The bottom up approach of silicon epitaxy from silane, on low cost substrate or with layer transfer, is promising to go way below 0.5 $/W. In this context, it is likely that the future of crystalline silicon cells will be based on thin epitaxial films deposited on or transferred to low cost substrates. Ideally, c-Si efficiency could be obtained for the area cost of a-Si:H panels. Many groups are working in that direction (See Fig.4.3), but our innovative approach stands apart from others, since we are using PECVD, the standard tool of amorphous silicon deposition, to produce monocrystalline silicon at temperature around 200°C.

4.2.1 Experimental results

Heavily boron-doped, (100)-oriented Si wafers with a resistivity of 0.02-0.05 Ω.cm and a thickness of 525 μm were used as a substrate for the epitaxial growth, and as the electrical contact of the solar cell. The wafer native oxide is removed by a 30 seconds dip in a 5%-diluted hydrofluoric acid solution (see section *3.3.1 Wet chemical cleaning*) just before loading them into a standard (13.56 MHz) capacitively coupled RF-PECVD reactor[35]. Intrinsic (non-intentionally-doped) epitaxial Si layers of various thicknesses (0.9 - 4.2 μm) were deposited from the dissociation of SiH_4/H_2 hydrogen mixtures and completed with the deposition of a standard (n+)a -Si:H emitter in the same PECVD reactor, without breaking vacuum, using SiH_4/H_2 and PH_3 (gas cylinder of 1% diluted in H_2). The substrate temperature was kept at 175°C throughout the deposition process. The area of the cells, 2×2 cm^2 for the largest ones, was defined by sputtering ITO through a shadow mask and evaporating Al grid contacts. Note that all the interfaces are flat and that there is no light trapping scheme. The structure of the devices is shown in Fig.4.5-a) and a top view picture of a 2×2 and a 1×1 cm cell is shown in Fig.4.5-c). The undoped epitaxial layer was deposited under the optimum conditions described in Tab.3.1. The amorphous emitter growing sequence includes the deposition of an ultra-thin a-SiC:H

[7] T. Tiedje et al., IEEE Transactions on Electron Devices, **31**: 711–716, 1984.
[34] K. Maki et al., 37th IEEE Photovoltaic Specialists Conference (PVSC), 000057–000061, 2011.
[35] P. Roca i Cabarrocas., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, **9**: 2331, 1991.

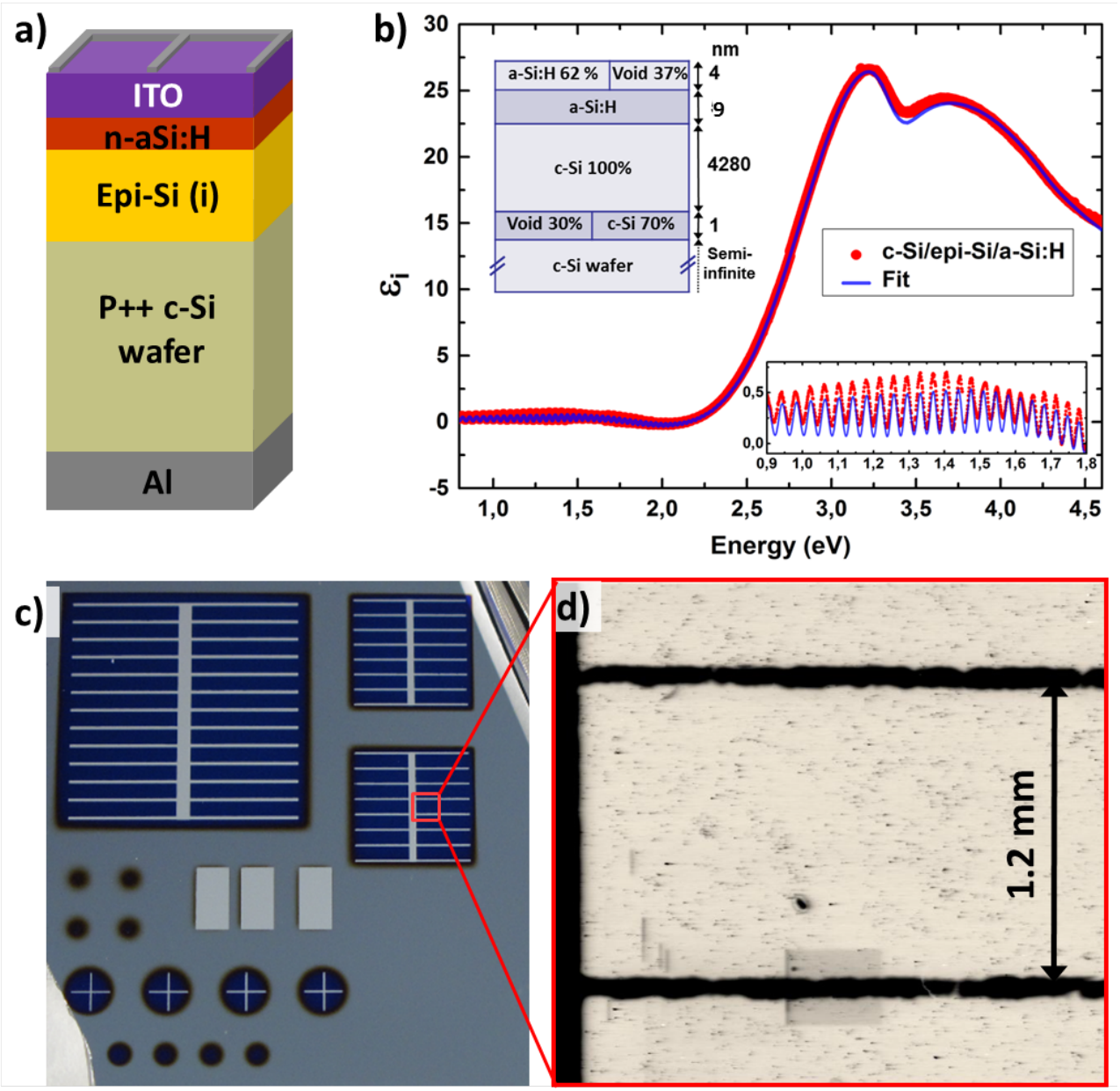


Fig. 4.5 – a) Schematic representation of the epitaxial solar cell stack. b) Ellipsometry measurement on : (p++)c-Si/(i)epi-Si/(n)aSi:H (red points) and corresponding fit (blue line) with the optical model detailed in the graph. The inset is a zoom on the low energy oscillations. c) Top view picture of a 2×2 and 1×1 cm cells. d) EBIC image of epitaxial solar cells for defect counting.

layer on epi surface to obtain a sharp epi-Si/a-Si:H interface[36], followed by the deposition of intrinsic and n-type a-Si:H layers; the corresponding deposition parameters are listed in Tab.4.1.

The imaginary part of the pseudo-dielectric function ε_i corresponding to the full layer stack (p++)c-Si/(i)epi-Si/(n)aSi:H measured by ellipsometry is shown in Fig.4.5-b). The blue line corresponds to the fitting of the experimental data (red dots) with the optical model detailed in the graph inset. The spectrum of the solar cell stack is dominated by that of the ∼ 13 nm a-Si:H emitter which buries the characteristic c-Si signature. Fitting is performed with an optical model using the

[36] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells.* PhD thesis. Ecole Polytechnique, France, May 2011.

dispersion curve of monocrystalline silicon for the epi-layer, as obtained by Aspnes[37], a Tauc-Lorentz dispersion formula for the amorphous silicon layer[38], as well as layers combining these materials with a void fraction, using the Bruggeman effective approximation theory[39]. The oscillations (see inset) observed at low photon energies (< 3 eV) can be accounted by a very thin interface layer between the film and the wafer, allowing us to determine precisely the thickness of the epitaxial film. The fit of the layer stack (blue line) perfectly reproduces the experimental spectrum (red circles) and reveals a 4.2 μm thick 100% crystalline epitaxial layer, with a thin defective/porous interface layer (30% void) between the c-Si wafer and the epi-Si layer. The a-Si:H emitter can be accurately described as a 100% amorphous silicon layer of 13 nm having a roughness of 4 nm.

	Temp. (°C)	Pressure (mTorr)	H_2 (sccm)	SiH_4 (sccm)	PH_3 (sccm)	CH_4 (sccm)	Power (mW/cm^2)	Electrode gap(mm)	time (min)
a-SiC:H	175	90	40	25	-	50	6	28	0.5
a-Si:H	175	100	40	50	-	-	6	28	1
(n)a-Si:H	175	115	40	50	1	-	6	28	3

Tab. 4.1 – Optimized deposition conditions for n-type amorphous silicon emitter on epitaxial silicon.

The electron-beam-induced current (EBIC) mode of scanning electron microscopy is a unique non-destructive electrical measurement method to characterize local electrical activities of defects in semiconductors[40]. In particular, this technique can be used for threading dislocations counting in Si and SiGe eptaxial layers[25,41,42]. We have thus performed SEM and EBIC plan view image of a 3.2 μm epitaxial cell solar cell; the result is displayed in Fig.4.5-d): a threading dislocation density of about 1.0×10^5 cm^2 is found. This relatively low defect density is consistent with the results obtained using Secco etching on epi-layers deposited at low power, as shown in the previous chapter. Threading dislocation density is known to impact the V_{oc} of epitaxial cells[43]; however it is rather unlikely for us to be limited by those defects, since our material is well passivated with hydrogen.

Fig.4.6-a) shows the current-voltage characteristics under 1 sun AM1.5G spectrum of 6 heterojunction solar cells for which we only varied the thickness of the intrinsic absorber layer. The corresponding J_{sc}, V_{oc}, FF and efficiency are listed in Tab.4.2. As expected, the short circuit current of the solar cells increases with the thickness of the absorber layer: from 10.9 mA.cm^{-2} for the sample without epitaxial absorber to 20.2 mA.cm^{-2} for the 4.2 μm solar cell. This current is produced by just a single pass of light: front surface is flat and there is no back surface reflection because of the 525μm thick wafer. As a comparison, the ideal J_{sc} calculated previously from a single path of light through a 4 μm thick epi-Si layer is 22.6 mA/cm^2. This unexpected small difference between the experimental J_{sc} and the ideal value suggests that the highly doped wafer may contribute to the current.

The most striking feature is the high values of the FF achieved for these devices, which compare favourably with these of heterojunction solar cells produced on c-Si wafers in our laboratory[44]. Fill factor, as it is sensitive to recombination and parasitic resistances, is a key parameter in thin film solar cells: a good FF indicates good transport properties in the intrinsic layer, and consequently good epitaxial quality. Interestingly enough, the thicker cells exhibit higher FF suggesting that the quality

[37] D.E. Aspnes et al., Physical Review B, **27**: 985, 1983.
[38] G.E. Jellison Jr. et al., Thin Solid Films, **377-378**: 68–73, 2000.
[39] D.A.G. Bruggeman., Annalen der Physik, **416**: 636–664, 1935.
[40] H.J. Leamy., Journal of Applied Physics, **53**: R51–R80, 1982.
[25] K. Alberi et al., Applied Physics Letters, **96**: 073502, 2010.
[41] C.W. Teplin et al., Applied Physics Letters, **96**: 201901–201901–3, 2010.
[42] X.L. Yuan et al., Applied Physics Letters, **84**: 3316–3318, 2004.
[43] K. Alberi et al., Applied Physics Letters, **101**: 123510, 2012.
[44] J. Damon-Lacoste et al., Journal of Applied Physics, **105**: 063712, 2009.

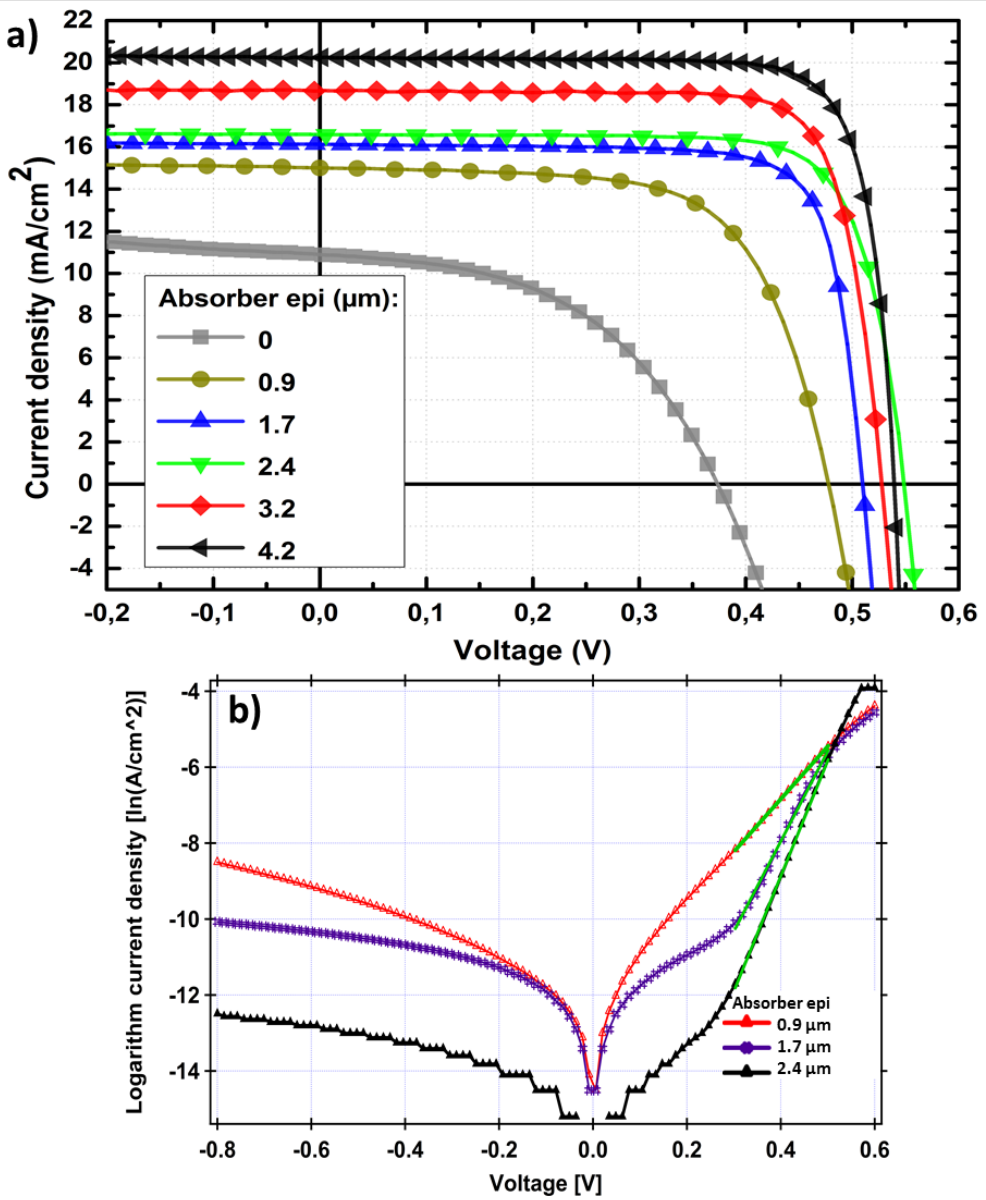


Fig. 4.6 – a) Current-Voltage characteristics under AM1.5G spectrum of solar cells (p++)c-Si/(i)epi-Si/(n)a-Si:H, having different epitaxial absorber thicknesses: 0, 0.9, 1.7, 2.4, 3.2, 4.2 μm. b) Corresponding dark I-V characteristics of selected samples.

of the intrinsic absorber layer improves with thickness. This is in good agreement with crystal quality improvement with thickness detected by in-situ ellipsometry and cross section Raman Spectroscopy, as explained in the previous chapter. The V_{oc} is also improving with thickness but reaches its maximum for 2.4μm thick absorber: 546 mV. This relatively low value is most likely due to interface recombination rather than bulk (e.g. at dislocations): indeed, being grown below 200°C in H rich plasma, the epi-layer is well hydrogenated; V_{oc} as high as 570 mV are reported in literature for $10^8 cm^{-2}$ TDD passivated by hydrogen[43]. The thicker the intrinsic epitaxial layer, the less the device is penalized by the p++c-Si/epi-layer interface defect density; indeed, the ex-situ native oxide wet chemical cleaning prior epitaxy is also responsible for some variability in the interface quality. Our best cell reaches an efficiency of 8.8% with a FF of 80.5%, a V_{oc} of 539 mV and a J_{sc} of 20.2 $mA.cm^{-2}$. The high values of fill factor demonstrate the viability of using epitaxial growth by PECVD at 175°C for the production of thin c-Si films. Note that the efficiency of these solar cells compares very favorably with

that of similar devices produced by HWCVD at 700°C[24] (see Fig.4.3). It should be noted that results shown in Fig.4.6 and Tab.4.2 are measured before annealing. In fact, the J_{sc} and FF improves upon annealing at 180°C (30 min) in forming gas atmosphere, resulting in up to 0.5% absolute efficiency improvement (measured on the 3.2 μm device). However too high temperature annealing shall be avoided: the 4.2 μm device performance was decreased due to higher series resistance after annealing 30min around 210°C. Anyhow, a detailed study on annealing effect on electrical properties of the epi-Si layer and the whole device is still needed.

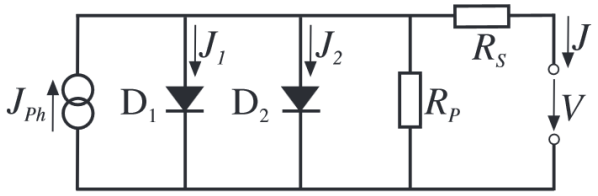


Fig. 4.7 – Equivalent circuit of a solar cell according to the two-diode model.

$$J = J_{ph} - \frac{V + JR_s}{R_p} - J_{o1}\left(e^{\frac{q(V-JR_s)}{n_1 k_B T}} - 1\right) - J_{o2}\left(e^{\frac{q(V-JR_s)}{n_2 k_B T}} - 1\right) \tag{4.1}$$

Dark I-V measurements are also very useful to extract information on the solar cell device: the ideality factor n and the dark saturation current density J_o. Fig.4.7 shows the equivalent circuit for a solar cell, in the two-diode model[45]. In this model, the relation between the external current density J and voltage V is transcendental, as shown in equation 4.1. The illumination is represented by a current source J_{ph}. The diodes, D_2 and D_1, are used to represent respectively SRH recombination currents in the space charged region, and SRH and Auger recombination elsewhere. R_s and R_p are the parasitic shunt and parallel resistances respectively, J_{oi}, n_i the dark saturation current density and ideality factor of diode i; k_B the Boltzmann's constant and T the temperature. This equation can be solved numerically or with a specific algorithm[46]. Depending on the expected precision and solar cell characteristic, a simpler one diode model may also be used to fit the dark I-V characteristic; in this case it is possible to find an explicit solution for the current and the voltage in terms of W-functions[47]. However for the sake of simplicity, we have neglected the parasitic resistances to fit the dark I-V curves; since J_{ph} is equal to zero in dark conditions, equation 4.1 is simplified into equation 4.2:

$$J = J_o\left(e^{\frac{qV}{nk_BT}} - 1\right) \tag{4.2}$$

$$ln(J) = ln(J_o) + \frac{q}{nk_BT}V \tag{4.3}$$

Thus, when the voltage is high enough to neglect the -1 term (V∼50-100mV), the ideality factor can be deduced from the slope in a semilog plot, and the J_o extracted from the y-axis intercept (see eq.4.3). The ideality factor is a function of the voltage; at low(high) voltage the dark I-V is dominated by shunt(series) resistance effects.

The dark I-V characteristics of epitaxial solar cells with 0.9, 1.7 and 2.4 μm absorber are displayed in a semi-log plot in Fig.4.6-b). The curves are fitted around 0.4V, where the value of n is stable; J_o and n values are listed in Tab.4.2. The increase of absorber thickness from 0.9μm to 2.4μm translates into an ideality factor and J_o decrease from 2.78 to 1.27 and from 4160 to 0.76 nA/cm^2 respectively. This decrease is due to lower recombination for thicker epi-layers and therefore brings another proof of epitaxial electrical quality improvement with thickness. By way of comparison, the best wafer based silicon solar cells can reach J_o as low as few tens of fA/cm^2.

[24] H.M. Branz et al., Thin Solid Films, **519**: 4545–4550, 2011.
[45] M. Wolf et al., Advanced Energy Conversion, **3**: 455–479, 1963.
[46] S. Suckow et al., Progress in Photovoltaics: Research and Applications, **22**: 494–501, 2014.
[47] A. Ortiz-Conde et al., Solid-State Electronics, **44**: 1861–1864, 2000.

Epi thickness (μm)	n	J_0 (nA/cm^2)	V_{oc} (mV)	J_{sc} (mA/cm^2) I-V	J_{sc} (mA/cm^2) EQE	FF (%)	Efficiency (%)
0	-	-	373	10.9	-	49	1.99
0.9	2.78	4160	478	15	-	66	4.7
1.7	1.63	270	501	16.1	12.8	78.6	6.4
2.4	1.27	0.76	546	16.6	15.4	77	7
3.2	-	-	527	18.7	18.4	79	7.7
4.2	-	-	539	20.2	21.6	80.5	8.8

Tab. 4.2 – (p++)c-Si/(i)epi-Si/(n)a-Si:H epitaxial solar cells characteristics extracted from dark/light I-V measurements and EQE.

Quantum efficiency measurements were performed on the epitaxial solar cells, and the results are shown in Fig.4.8-a) together with the device reflectivity measured with an integrated sphere (dashed line). The following observations can be made: i) EQE is higher on the whole 400-1100nm range for thicker absorber. ii) EQE at 400nm is relatively low, but there is an improvement with absorber thickness up to 3.2 μm and remains similar for the 4.2μm device. iii) The peak EQE (around 580nm) and red part of the spectrum are significantly improved with thickness. The relatively low value of EQE around 400 nm is partially explained by the high reflectivity of ITO (>50% at 400nm) in this range. The short wavelength (around 400nm) are fully absorbed in the first hundreds nanometers of the device, thus the EQE improvement obtained in this range with increasing absorber thickness is the proof of better epitaxial quality and better a-Si:H/epi-Si interface. Epitaxial quality may have reached its maximum quality from a thickness of 3.2μm. The improvement in the higher wavelength range is also linked to the higher absorption in the absorber. The long wavelength response (>900nm) remains low because this part of the spectrum is mainly absorbed in the highly doped wafer. Indeed, as shown in Tab.4.2, the device with no epitaxial layer, (p++)c-Si/(n)a-Si:H, exhibits a non negligible 10.9mA/cm^2; however the efficiency remains low, around 2%, because of recombination in the highly doped wafer. The question of how much the wafer contributes to the device performance, question often neglected in literature (wafer contributions from 0 to 1mA/cm^2 are often mentioned[25]), will be addressed with insight from simulations in the next section. By integration with the solar spectrum, the J_{sc} is calculated from the EQE data. The resulting current density is compared to the solar

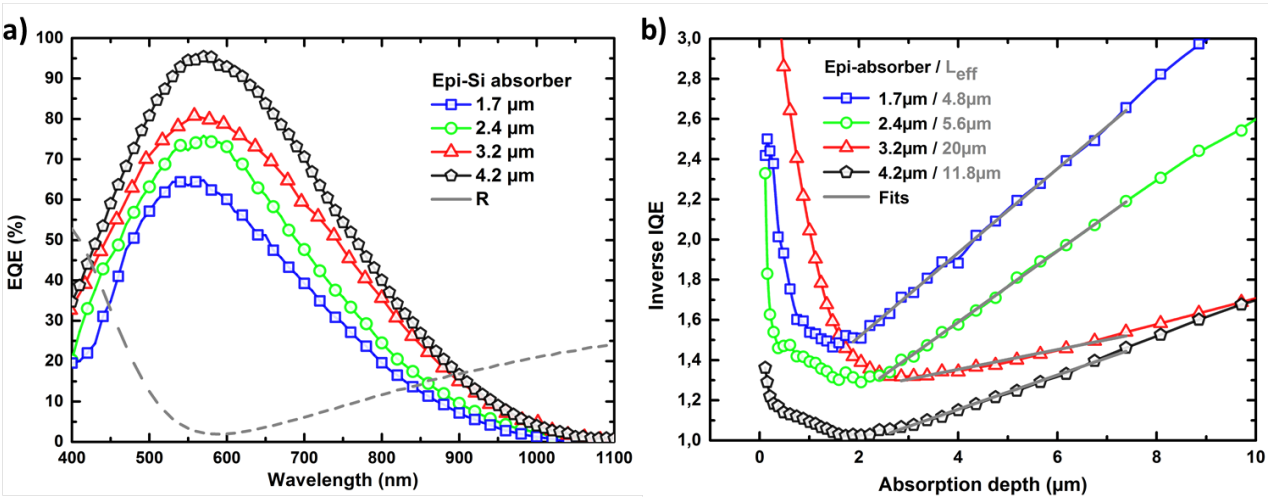


Fig. 4.8 – a) EQE for (p++)c-Si/(i)epi-Si/(n)a-Si:H solar cells with various epitaxial thicknesses. The dash-line represents the reflectivity of the final device including the ITO anti-reflection layer as shown in Fig.4.5-a). b) Inverse quantum efficiency IQE^{-1} as a function of absorption length. Effective diffusion length L_{eff} is deduced from linear fit.

simulator values in Tab.4.2. For the 2.4 and 3.2μm epi-cells, there is less than 2% relative discrepancy between the two techniques, thus the J_{sc} value is reliable. However, the best cell for instance has more than 1 mA/cm^2 higher current from EQE; this could be linked to calibration problems by the time of the measurement. It should be precised that the I-V measurement is performed on 4 cm^2 whereas EQE is acquired for a small area ($\sim$2$\times$4mm); contact finger shading effect may introduce some variability.

To a large extent, the performance of silicon solar cells is determined by the recombination of minority carriers photo-generated in the absorber layer. The main parameters describing this recombination are surface recombination velocity and bulk diffusion length. IQE measurement contains some information on those two quantities. As reported by Basore[48], if the absorption depth (L_α=1/α) is small compared to the thickness of the absorber layer, the IQE is linked to the effective diffusion length L_{eff} according to equation 4.4. The factor cos(θ) accounts for the longer effective path of the light in the case of textured c-Si surface; thus here the flat interfaces yield cos(θ)=1. This effective diffusion length depends on the bulk diffusion length and the back surface recombination velocity and the diffusivity (L,S,D) according to equation 4.5.

$$IQE^{-1} = 1 + cos(\theta)\frac{L_\alpha}{L_{eff}} \quad (4.4) \qquad L_{eff} = L\,\frac{1 + (SL/D)\,tanh(W/L)}{(SL/D)\,tanh(W/L)} \quad (4.5)$$

W represents here the thickness of the cell. By expanding eqation 4.5 in the case of L$\gg$W, we obtain equation 4.6. A lower limit for the bulk diffusion length (L=(Dτ)$^{1/2}$) and an upper limit for back surface recombination velocity can thus be deduced[49] as shown in eqations 4.7 and 4.8.

$$L = \sqrt{\frac{W L_{eff}}{1 + \frac{S}{D}(W - L_{eff}}} \quad (4.6) \qquad L \geqslant L_{min} = \sqrt{W L_{eff}} \quad (4.7) \qquad S < S_{max} = \frac{D}{L_{eff} - W} \quad (4.8)$$

The geometric mean of the absorber thickness and the effective diffusion length sets therefore a lower limit for the bulk diffusion length. Thus, in literature, IQE data is often used to get L_{eff} and to estimate the bulk diffusion length and the back surface recombination velocity for epitaxial silicon solar cells in the 10-50μm range[18,19,50].

The inverse IQE plot of our PECVD epitaxial solar cells is displayed in Fig.4.8-b). The curves show a linear increase from an absorption depth of 2μm and above. Since the layers are few microns thick, the condition L_α<W is not really fulfilled. However using the above-mentioned fitting procedure, we could extract effective diffusion length having realistic order of magnitude: 4.8, 5.6, 20 and 11.8 μm respectively for the 1.7, 2.4, 3.2, 4.2 μm thick epitaxial solar cells. The cells having similar structures and fabrication processes, the comparison of L_{eff} is a priori relevant: the net increase with the epitaxial thickness confirms the improvement of electrical properties (except for the 4.2 μm, which may have a lower bulk quality or higher surface recombination velocity). By using eq.4.7 and eq.4.8, we find for the cell with the best L_{eff} a lower bound for the bulk diffusion length of 8μm and an upper bound for the back surface recombination velocity, that is recombination velocity at the wafer/epi-Si interface, of 1900 cm/s (with D=3.2cm^2/s). While the trend and values obtained with this approach seem reasonable, the results should however be taken with care since the validity limit of the equations are not completely fulfilled here.

[48] P.A. Basore., 33th IEEE Photovoltaic Specialists Conference (PVSC), 147–152, 1993.
[49] M. Hirsch et al., Solid-State Electronics, **38**: 1009–1015, 1995.
[18] J.H. Petermann et al., Progress in Photovoltaics: Research and Applications, **20**: 1–5, 2012.
[19] M. Reuter et al., Solar Energy Materials and Solar Cells, **93**: 704–706, 2009.
[50] J.H. Werner et al., Applied Physics Letters, **62**: 2998–3000, 1993.

4.2.2 Insights from modeling

The influence on thin film crystalline solar cells of epitaxial absorber thickness, bulk diffusion length and impurity concentration has been studied with PC1D software by a team from NREL. The study, published by Alberi et al.[25], also correlates simulation results with experimental devices for which the epitaxial absorber is grown by HWCVD at 700°C. They found that L_{eff} orders of magnitude below the millimeter range required for 200-300 μm thick wafer cells is needed: an effective diffusion length of 3 times the absorber thickness is required for efficient carrier collection; they predict that a 5μm thick epi-cell should reach 12% with single light pass and above 15% efficiency with x10 light trapping. In addition, since the bulk life time scales inversely with the concentration of impurities/point defects, the maximum density a cell of thickness W can tolerate is proportional to W^{-2}. Thus a 2μm epitaxial cell can tolerate a 10^4 higher contaminant/point defects compared to 200μm cell: that is 10^{17}-10^{18}cm^{-3}. Looking at dislocation density in the epitaxial layer, they come to the conclusion that since efficient carrier collection happens for L_{eff} greater than $\sim$3W and the distance between dislocations density l_d is roughly limiting L_{eff} according to $l_d/2$, dislocation spacing should be greater than 6W; that is 5.10^5cm^{-2} for a 2μm cell, 1.10^5cm^2 for a 5 μm cell. But if the defects are passivated by hydrogen, the upper bound for dislocation density is relaxed. Note that contrary to the high temperature HWCVD approach, our PECVD epitaxial layers are "self" passivated by their high hydrogen content.

To get more insight on the epitaxial absorber thickness influence in our solar cells, we have performed PC1D modeling. The influence of the emitter/base thickness on EQE has been investigated using the p-i-n layer stack shown in Fig.4.5-a). Material parameters used for modeling this c-Si/a-Si heterojunction are the result of an optimization made by Lien et al.[51]. We have used the experimentally measured front reflectance of ITO (see grey crosses in Fig.4.9-a)) in the simulation, the diffusion length in the epi-Si layer was set to 300μm and epi-Si front and back surface recombination velocities were set to zero. The bulk diffusion length (the surface recombination velocities) is set intentionally higher (lower) than the real device, to estimate the maximum achievable efficiency. The results of the device simulation for different emitter and base thicknesses, as well as experimentally measured EQE of 1.7μm (circles) and 2.4μm (squares) epitaxial cells, are shown in Fig.4.9-a). The graph is composed of two groups of curves: i) those corresponding to devices having a thick emitter (60 nm) and variable base thickness (right part) and ii) those corresponding to devices having a thick base (100μm) and a variable emitter thickness (left part). Since carriers generated in the emitter by the short wavelength photons are subject to surface and bulk emitter recombination, the short wavelength EQE is particularly sensitive to surface passivation and emitter thickness. The simulated device with same structural parameters as the 2.4μm p-i-n solar cell, is represented by black circles. At 800 nm, simulation predicts a 35% EQE, whereas the fabricated device reaches 25%. This discrepancy may be explained by a high recombination velocity at the back epi-Si/c-Si interface. In the blue region of the spectrum, two main reasons can explain the discrepancy between model and experimental data: i) The ITO anti-reflective coating of our device absorbs a non-negligible fraction of the incident light. The simulation does not take into account those losses. ii) The interface between epitaxial silicon and amorphous top layer may be rough, and thus produce a higher recombination velocity with respect to a sharp a-Si:H/c-Si wafer interface. Anyhow, the simulated device reaches almost 22 mA.cm^{-2} with a V_{oc} of 530 mV and 9% efficiency.

[51] S.-Y. Lien et al., Progress in Photovoltaics: Research and Applications, **17**: 489–501, 2009.

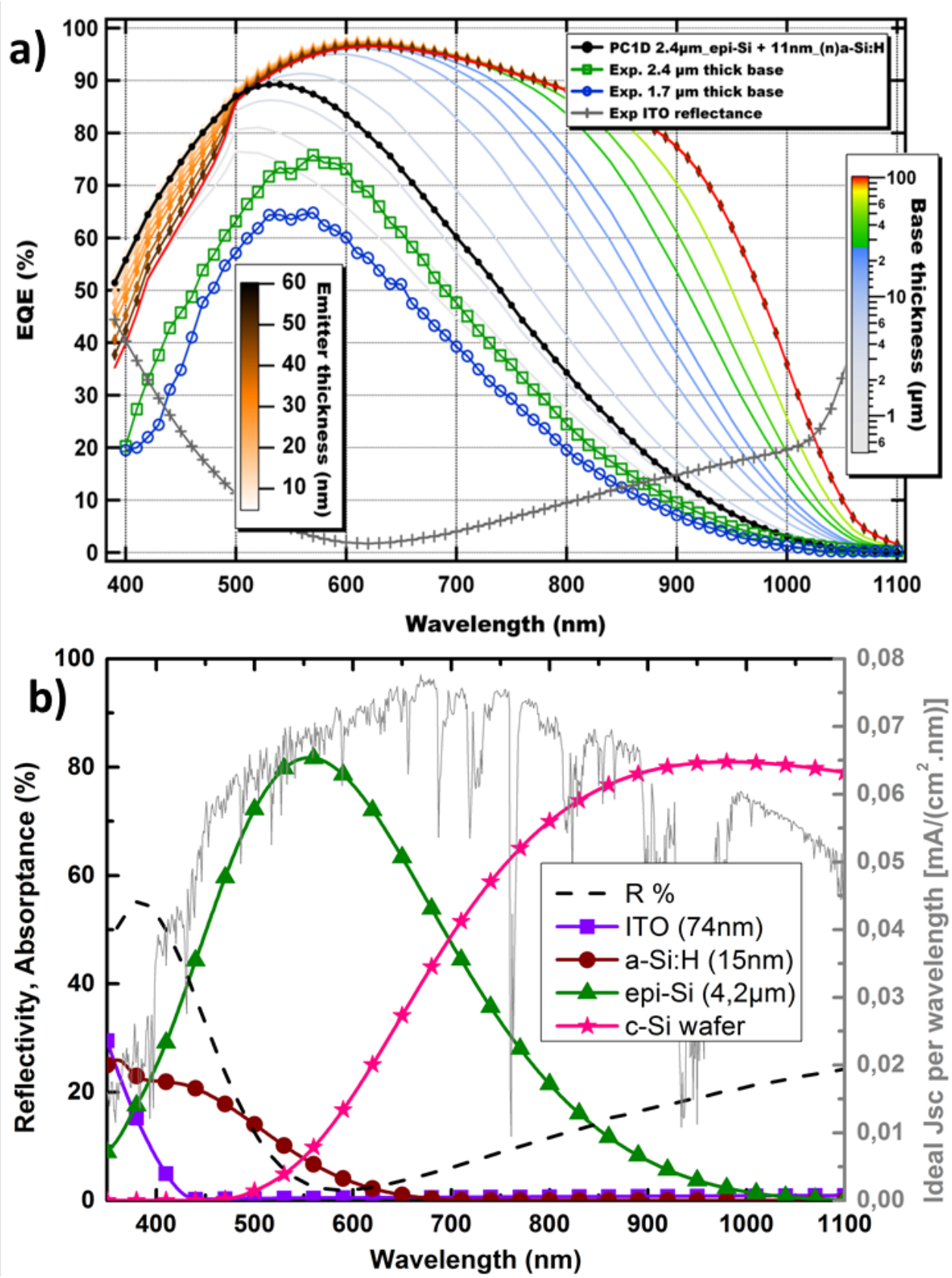


Fig. 4.9 – PC1D simulations of EQE obtained by varying the emitter (5 to 60nm) and the base (0.5 to 100μm) thickness for the structure described in Fig.4.5-a); experimental EQE of 1.7μm (circles) and 2.4μm (squares) cells. b) Simulation of absorption splitting in the solar cell as calculated by optical transfer matrix method; the ideal J_{sc} is represented in grey.

The details of absorption splitting between the various layers of the device were investigated by optical simulations: a 4.2μm epitaxial solar cell (structure shown in Fig.4.5-a)) has been modeled using a transfer-matrix method code developed internally by M. Foldyna. The result is displayed in Fig.4.9-b). The grey curve (bottom and right axis) represents the ideal J_{sc} per wavelength, the dash line is the reflectivity of the device, and closed symbols show the absorption in ITO (squares), a-Si:H (circles), epi-Si layer (triangles) and wafer (stars). One can see that ITO absorption becomes relatively negligible above 400nm, however absorption in the amorphous layer is quite significant up to 600nm. The absorption in those two layers corresponds to an ideal J_{sc} loss of 0.6 and 2 mA/cm^2 respectively. Thus, as seen in Fig.4.9-a), the amorphous emitter layer should be as thin as possible, provided that it fulfills its passivation and junction formation duty. Our experimental devices typically have 12-15nm emitter thickness, but there should be efficiency improvement going below 10nm. In this model, the 4.2μm epitaxial layer produces a maximum of 16.2 mA/cm^2, to be compared with the $\sim$20 mA/cm^2 measured under the solar simulator. This discrepancy is explained by the contribution of the highly doped wafer, which starts to absorb significantly above 500nm. The strong absorption at long wavelength (900nm and above) does not correspond to a high EQE, because such photo-generated carriers are not collected. However electron-hole pairs generated in the front part of the c-Si wafer can contribute to the solar cell current. When keeping the epitaxial layer on the wafer, the absorber thickness should be increased beyond 5μm to have a negligible wafer contribution to the current density.

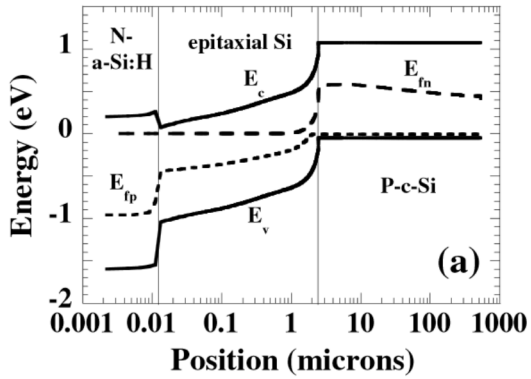


Fig. 4.10 – Simulated energy band diagram for a 2.4μm PECVD epitaxial solar cell[52].

Epi-Si DOS (cm^{-3})	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Efficiency (%)
10^{13}	16.62	0.558	81.5	7.56
10^{14}	16.62	0.556	81.2	7.51
10^{15}	**16.62**	**0.547**	**77.8**	**7.07**
5×10^{15}	16.60	0.511	72.1	6.12
10^{16}	16.54	0.584	70	5.6
5×10^{16}	15.92	0.410	64.6	4.22
10^{17}	15.19	0.379	62.2	3.58

Tab. 4.3 – Solar cell sensitivity to Gaussian defect inside epi-Si layer. Bolded line corresponds to the actual 2.4μm PECVD epi-Si device[52].

Further detailed electrical-optical modeling of these epitaxial solar cell devices were realized by the team of P. Chatterjee[52]. The simulations are based on the one-dimensional Amorphous Semiconductor Device Modeling Program (ASDMP)[53], later extended to also model crystalline silicon and HIT cells[54], which solves the Poisson's equation and the two carrier continuity equations under steady state conditions for a given device structure, and yields the dark and illuminated J-V and EQE characteristics; the program is ab-initio in its electrical part. The expressions for the free and trapped charges, the recombination term, the boundary conditions and the solution technique in this program are similar to the AMPS computer code[55]. The gap state model consists of the tail states and two Gaussian distribution functions to simulate the deep dangling bond states in the case of the amorphous layers, while in the epi-Si layer and c-Si substrate the tails are absent. The defect density on the surfaces of the epi-Si film is modeled by a defective layer 5 nm thick; thus, for example, a volume defect density of $\sim 2.10^{17}$cm^{-3} translates into a surface defect density N_{ss} of 10^{11} cm^{-2}.

The complex refractive indexes of each layer are inputs in the model, the band gap of epi-Si is taken identical to c-Si, and two-third of the band discontinuity is apportioned on the valence side.

[53] P. Chatterjee et al., MRS Online Proceedings Library, **426**: null, 1996.
[54] M. Nath et al., Journal of Applied Physics, **103**: 034506, 2008.
[55] P.J. McElheny et al., Journal of Applied Physics, **64**: 1254–1265, 1988.

Other input parameters are: thickness of the individual layers, the doping and defect densities inside the emitter (deduced from measured activation energies) and the carrier mobilities in the epi-Si layer (from measurement). The main parameters obtained by fitting the measured illuminated J-V and EQE curves therefore are the defect densities at the front and back of the epi-Si layer and the defect density in the volume of this layer. The corresponding simulated band diagram is shown in Fig.4.10. A high electric field is present at the epi-si/c-si interface and thus electron-hole pairs generated in the wafer close to the interface are well separated. The low electric field inside the (p++)c-Si wafer and the large number of defects result in a poor collection from the bulk of the wafer. An excellent fit of the 2.4 μm epi-cell was obtained for a Gaussian bulk defect density (DOS) of 10^{15}cm^{-3} 0.4 eV above the conduction band, and an epi-layer front and back surface defect density of 10^{11} and 10^{12} cm^{-2}. The sensitivity of the device to bulk Gaussian DOS is resumed in Tab.4.3. One can see that roughly 10 mV V_{oc} and 3.5 absolute % FF improvement can be expected by reducing the DOS of one order of magnitude. This reasonnable higher bulk quality may be achieved using PECVD epitaxial layers at temperature higher than 200°C, in a reactor with less contamination sources (e.g. equipped with a load lock, etc.).

The sensitivity of the solar cell output parameters against epi-Si/(n)a-Si:H and epi-Si/(p++)c-Si wafer surface defect density, respectively $N_{ss,f}$ and $N_{ss,b}$, is detailed in Tab.4.4. A drastic device performance degradation happens for $N_{ss,b}$ higher than $\sim 5.10^{11}$cm^{-2} or $N_{ss,f}$ higher than $\sim 10^{12}$cm^{-2}. This higher sensitivity to the defect states at the rear epi-Si/(P++)c-Si interface with respect to the top (n)a-Si:H/epi-Si junction is mainly explained by the valence band gradient at the back interface which yields a strong favorable field that helps with the hole collection.

$N_{ss,f}$ (cm^{-2})	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Efficiency (%)
10^{10}	16.63	547	77.8	7.07
10^{11}	**16.63**	**547**	**77.8**	**7.07**
5.10^{11}	16.68	546	77.8	7.09
10^{12}	6.75	542	78	7.09
5.10^{12}	16.77	404	64.8	4.39
10^{13}	16.41	369	59.6	3.61

$N_{ss,b}$ (cm^{-2})	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Efficiency (%)
10^{10}	16.63	592	74.8	7.37
10^{11}	16.63	591	74.9	7.36
5.10^{11}	16.63	582	75.8	7.34
10^{12}	**16.63**	**547**	**77.8**	**7.07**
5.10^{12}	16.61	394	66.3	4.35
10^{13}	16.60	360	62.9	3.76

Tab. 4.4 – Sensitivity of a 2.4μm cell to the defect density at the rear c-Si/epi-Si interface, $N_{ss,b}$, for a fixed front epi-Si/(n)a-Si:H interface defect density $N_{ss,f} = 10^{11}$cm^{-2}; and front sensitivity for a fixed $N_{ss,b} = 10^{12}$cm^{-2}. Bolded values correspond to the fitted[52] J-V parameters and surface defect density for our experimental 2.4μm PECVD epi cell.

Keeping constant the parameters of the actual 2.4 μm cell, the effect of an increase in absorber thickness on the efficiency (without additional light trapping) is displayed in Fig.4.11: up to 10μm thick epitaxial layer, the efficiency increases to reach slightly more than 10%; then thicker absorber, with same electrical properties, will improve marginally the efficiency up to 17μm where efficiency starts to drop. Finally, starting from the simulated parameters corresponding to the real 2.4 μm device, improvement paths are identified and their cumulative effects are quantified in Tab.4.5. First an increase in epi absorber thickness up to 5μm enables to reach 20.3 mA/cm^2 and an efficiency of 8.6%. This simulation was performed before the fabrication of the 4.2 μm cell, which has indeed attained this level of current density. Then reducing the back epi-layer surface defect density down to 5.10^{11}cm^{-2} enable to increase V_{oc} at 580 mV. This is an important result since our experimental device is penalized by its low V_{oc}; and this could be practically achieved by using in-situ wafer native oxide cleaning instead of ex-situ wet HF dip (see previous chapter). By randomly texturing the front surface of such a 5μm device, the current could reach 25 mA/cm^2 and even further 29 mA/cm^2 for a double side textured (e.g. if the layer is lifted-off); thus the final device including the above-mentioned

improvements could reach around 13% efficiency.

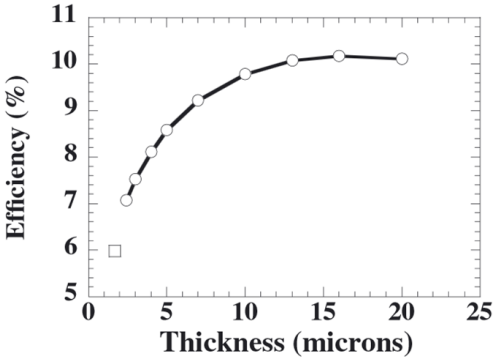


Fig. 4.11 – Simulated effect of epi-absorber thickness increase with fixed electrical properties[52].

Solar cell parameters	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Eff. (%)
Real device	16.6	546	77	7.0
Model	16.63	547	77.8	7.07
epi-Si=5μm	**20.35**	549	76.7	8.57
$\mathbf{N_{ss,b} = 5.10^{11}cm^{-2}}$	20.36	**580**	74.7	8.83
Textured front	**25.53**	589	75	11.27
Textured front&back	**29.21**	594	75	13.02

Tab. 4.5 – Cumulative improvements for the initial 2.4μm epitaxial solar cell model. At each step, the main diode parameter responsible for the efficiency increase is bolded[52].

4.3 Light trapping in thin film monocrystalline layers

Increasing the absorption in the thin crystalline layer is an important action-lever to reach higher efficiencies. Light trapping, especially random pyramids of few microns in size, is routinely used in wafer based silicon solar cells. As shown in the previous chapter, selective etching can efficiently produce random pyramids on PECVD epitaxial silicon. To implement this light trapping feature in our c-Si(p++)/epi-Si/n-aSi:H epitaxial solar cell, the sample is taken out of the PECVD reactor after the epitaxial step, the wet chemical etching of random pyramids is done in a KOH/IPA solution, and, after HF surface cleaning, the sample is loaded again in the PECVD reactor to form the n-aSi:H emitter layer. The comparison between EQE of flat and textured epitaxial cells is shown in Fig4.12. The two samples come from the same epitaxial run, but one piece has gone through the additional step of wet selective etching to form random pyramids before the deposition the a-Si:H emitter.

The black curve (squares) corresponds to the sample with flat interfaces, and the red one (triangles) to the sample with random pyramids. The difference in EQE pyramids-flat is represented in blue (right axis, circles). The EQE of the textured cell in the short wavelength range is higher, up to $\sim$ 575nm, but then the flat cell exhibits a higher EQE in all the long wavelength range. Such difference may seem surprising, since the light trapping features should enhance the light path inside the absorber layer and thus one could expect an improved EQE in the long wavelength range. In fact, this behavior is explained by the etching process: when forming pyramids, a significant amount of material is removed. For example, starting from a 2μm thick epitaxial layer, the etching of 1μm high pyramids will leave a maximum of 1μm epitaxial layer beneath. Thus if the light path is effectively enhanced, the real thickness of the layer is significantly decreased, and this produces the EQE shift visible in Fig.4.12. This result illustrates the limitation of standard light trapping features in thin film c-Si solar cells. Advanced light trapping concepts, such as photonics and plasmonics, may overcome this problem.

4.3.1 Trapping light in thin film c-Si solar cells

Crystalline silicon, with its indirect band gap, has a relatively weak absorption in the main part of the solar spectrum ($\sim$600-1000nm); thus thin film crystalline silicon solar cells in the 1-20 μm thickness range requires strong light path enhancement to keep a high current density. The c-Si flat surface reflects indeed around 35% of the incoming light at 600nm. In addition to light trapping geometries, this reflection issue is commonly addressed by using anti-reflection coatings (ARC). Such dielectric layers are deposited on top of the silicon layer, and a minimum reflection for a given wavelength can be achieved if reflected waves at the front and the back of the ARC produce destructive

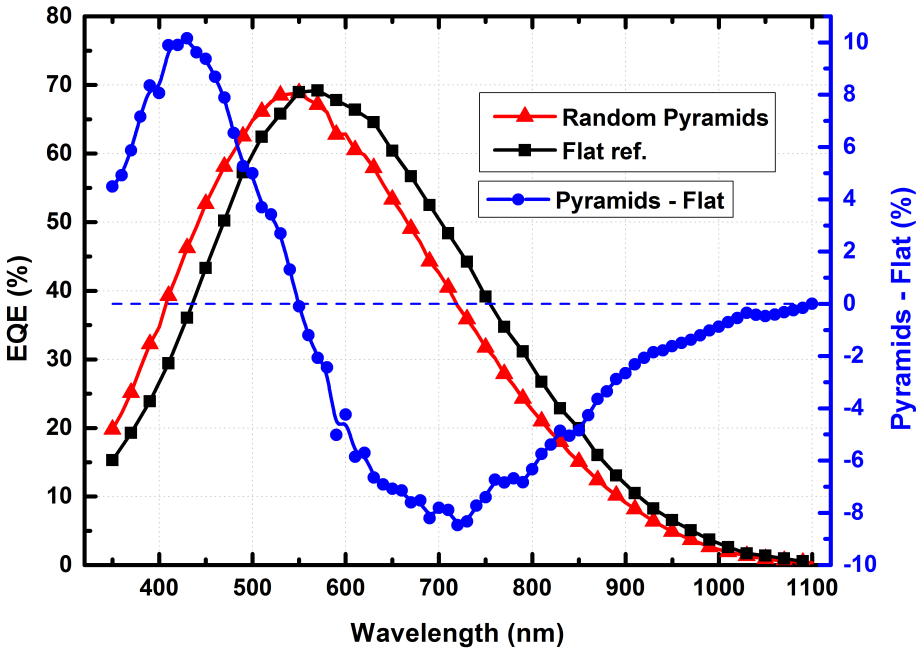


Fig. 4.12 – Comparison of EQE for c-Si(p++)/epi-Si/n-aSi:H solar cells with flat (squares) and random pyramids textured (triangles) epitaxial absorber. The blue curve (right axis, circles) shows the difference between textured and flat EQE.

interferences. Thus the thickness (W) and the refractive indices (n) of the ARC should be chosen according to $W = \lambda/4n$ and $n = \sqrt{n_{Si} \times n_o}$, where n_{si} and n_o are the index of silicon and surrounding material dielectric layer. For c-Si cells, silicon nitride or indium tin oxide (ITO) are often used as ARC layers. To minimize reflection at the wavelength of the maximum solar spectrum photon flux (∼650nm), we have been using 80-90 nm of ITO, deposited by sputtering, on our epitaxial solar cells. For a broader band anti-reflection effect, dielectric layers with decreasing refractive index from the semiconductor layer to the air can be stacked. For example ZnS/MgF_2 or TiO_2/SiO_2 double layers are often used in the field of III-V cells. Up to 4 ARC layers are used in multi-junction devices to keep reflection below 5% on the whole 400-1800 nm range[56].

Literature results

For thin film c-Si, advanced strategies combining broadband anti-reflection effect with strong absorption enhancement are needed. Indeed, the standard random pyramids used in wafer based solar cells, which scatter light over a large angular range, are not well suited for thin film c-Si because: i) the roughness would exceed the film thickness ii) the surface enhancement increase surface recombination issues. New light trapping concepts, such as plasmonic[30,57] or dielectric nanostructures and photonics[32] crystals or diffraction gratings, are excellent candidates to provide efficient light trapping in thin film crystalline materials; the ray optics does not hold at this scale: the light propagation encounter near-field effects, resonances and wave guide modes. The absorption enhancement in a nanopatterned c-Si slab is linked to both impedance matching effect (between c-Si and surrounding medium) and mode coupling. It is shown, at least theoretically, that absorption enhancement much beyond the Yablonovitch limit ($4n^2$, also called the lambertian/ergodic limit) is achievable in this

[56] D.J. Aiken., Solar Energy Materials and Solar Cells, **64**: 393–404, 2000.
[30] H.A. Atwater et al., Nature Materials, **9**: 205–213, 2010.
[57] R.A. Pala et al., Advanced Materials, **21**: 3504–3509, 2009.
[32] A. Polman et al., Nature Materials, **11**: 174–177, 2012.

approach[31,58,59]. There is a prolific literature exploring the absorption enhancement produced by various type of nanostructures (see Fig.4.13-a,b,c)) with numerical simulations tools (RCWA, FDTD, etc.): double side diffraction gratings: stripes[60] or nanocones[61], metallic arrays[62], quasi-random structures[63], etc. In addition a growing number of papers deal with the experimental fabrication of such advanced light trapping structures and the measurement of their optical properties. SEM pictures of some nanostructures found in literature are gathered in Fig.4.13-d) to i): -Holes formed by hole-mask colloidal lithography (HCL) and inverted pyramids formed by nanoimprint lithography (NIL) and wet etching[64] -Black silicon formed by metal assisted etching[65] -Microphotonic parabolic concentrator structures fabricated via direct laser lithography[66,67] -Silver nanoparticles evaporated through porous alumina[30] -Spherical nanoshells formed by wet chemical synthesis[68].

However, incorporating such nanostructured features in working photovoltaic devices remains challenging, as testified by the small number of papers presenting efficient nanostructured solar cells. Since solar cells target the production of electrical power through charge carrier generation and collection, optical benefits of light trapping features should not be out-weighted by material degradation due to nanopatterning. Indeed, while excellent optical properties may be achieved over a large wavelength range (e.g. black silicon reflectance as low as 1% on the whole 0.5-2.5 μm range are demonstrated[69]), keeping high quality electrical properties with such nanostructures is very challenging. Excellent surface passivation should be achieved, since the nanopatterning produces significant surface enhancement compared to the flat case; in addition, to minimize Auger recombination in the nanostructures[65], it is highly desirable to form the junction on the opposite side of the layer. By choosing carefully the design and nanopatterning/etching technique, and by applying a highly conformal passivation layer, very low surface recombination velocities are achievable: Trompoukis et al.[70] have reduced surface recombination velocity down to 8 cm/s on inverted NIL pyramids on epi-foils passivated by a-Si:H, and Otto et al.[71] could reach 13 cm/s on black silicon passivated by Al_2O_3. We can mention the following successful example of nanophotonic solar cells (see Fig.4.13): j) 1 μm epi-free cell formed using nanoimprint lithography[16] reaching 15.5 mA/cm^2 and k) 10 μm c-Si with nanocones formed by colloidal lithography[13] reaching 29 mA/cm^2.

The nanostructures can be classified into 3 categories: i)Periodic ii)Partially disordered and iii)Random. The periodic nanostructures, i.e. photonic crystals, have their Fourier spectra typically consisting of series of sharp peaks corresponding to strong resonances for well-defined angles and wavelengths. Since for solar cell devices, a broad band and broad angle light trapping is desirable, periodic nanocrystals are probably not the optimum patterns. A random texturation will lead to broad-band but weak enhancement. Several studies conclude that quasi-random, or controlled disorder, is the best compromise: by introducing the right amount of disorder into the structure, the sharp photonic crystals resonances are gradually broadened while retaining aspects of the high-peak

[31] Z. Yu et al., Opt. Express, **18**: A366–A380, 2010.
[58] D.M. Callahan et al., Nano Lett., **12**: 214–218, 2012.
[59] C. Wang et al., Scientific Reports, **3**: , 2013.
[60] X. Meng et al., Opt. Express, **20**: A560–A571, 2012.
[61] K. X. Wang et al., Nano Letters, **12**: 1616–1619, 2012.
[62] I. Massiot et al., Applied Physics Letters, **101**: 163901, 2012.
[63] E.R. Martins et al., Nature Communications, **4**: 2665, 2013.
[64] C. Trompoukis et al., Phys. Status Solidi A, , 2014.
[65] J. Oh et al., Nature Nanotechnology, **7**: 743–748, 2012.
[66] J.H. Atwater et al., Applied Physics Letters, **99**: 151113, 2011.
[67] Emily D. Kosten et al., Light: Science & Applications, **2**: e45, 2013.
[68] Y. Yao et al., Nature Communications, **3**: 664, 2012.
[69] X. Liu et al., Energy & Environmental Science, , 2014.
[70] C. Trompoukis et al., Progress in Photovoltaics: Research and Applications, , 2014.
[71] M. Otto et al., Applied Physics Letters, **100**: 191603–191603–4, 2012.
[16] C. Trompoukis et al., Applied Physics Letters, **101**: 103901–103901–4, 2012.
[13] S. Jeong et al., Nature Communications, **4**: , 2013.

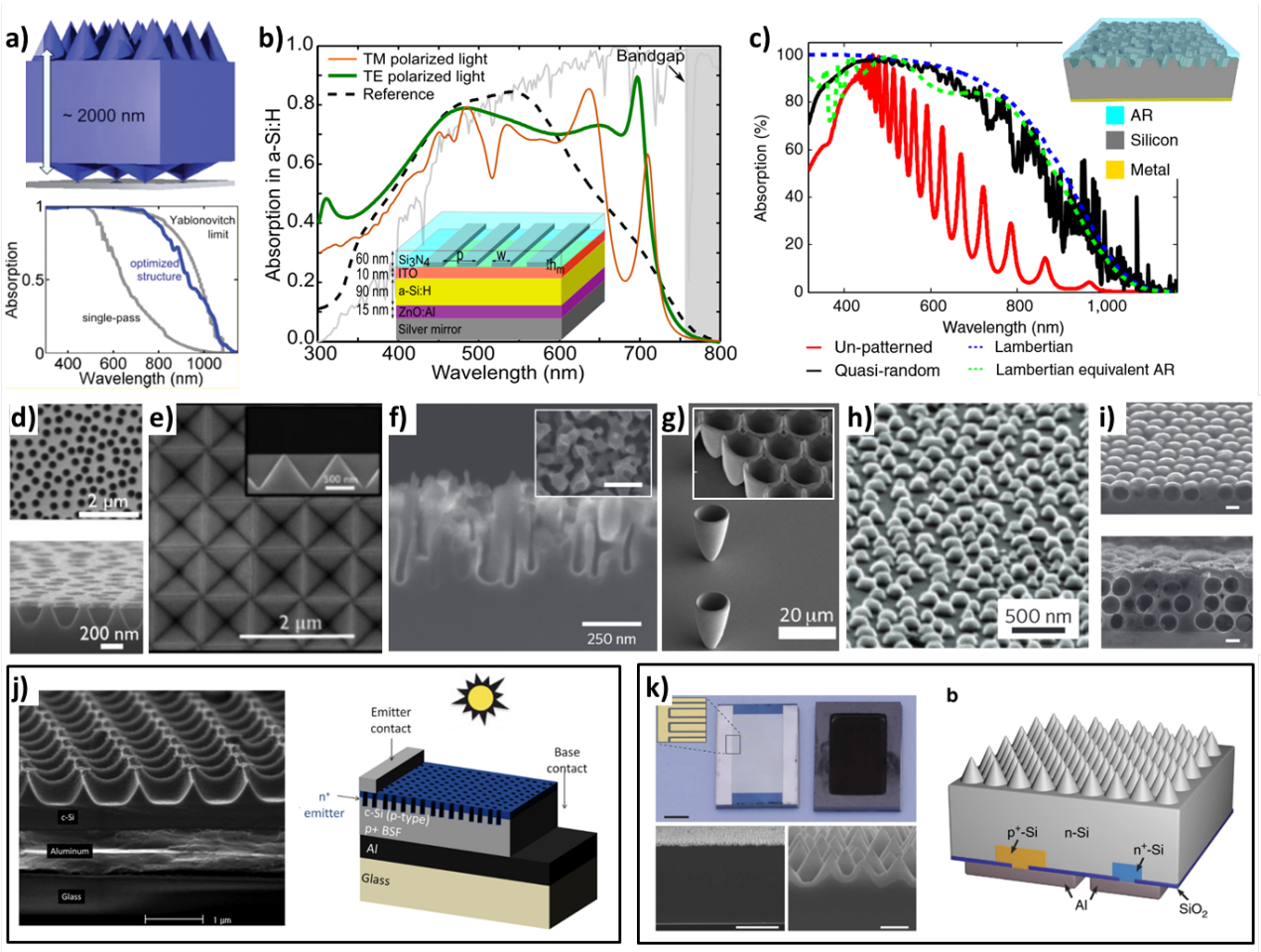


Fig. 4.13 – a)Absorption in 2μm c-Si layer with double side nanocone gratings, calculated by RCWA. b)Absorption enhancement from RCWA simulation with 1D silver array for 90nm a-Si:H layer. c)RCWA calculated absorption spectra of 1μm c-Si thin film patterned by a quasi-random super cell (black) and un-patterned (red). From d to f): SEM pictures of light trapping photonic/plasmonic nanostructures: holes, inverted pyramids, black silicon, parabolic reflectors, Ag nanoparticles, spherical nanoshells. Thin film c-Si solar cells including photonic nanostructures: j) 1μm epi-free reaching 15.5mA/cm^2 and k) 10μm c-Si reaching 29 mA/cm^2. From Ref. [13, 16, 30, 61–68].

absorption. Superior light trapping properties have thus been demonstrated by simulation and experimentally for designs with short range correlation or large period grating with a unit cell containing fine structures [63,72–74]. Ultimately, getting rid of any planar configuration, the absorber layer can be fully nanostructured, for example using nanowires in which absorption thickness and carrier collection length are decoupled, and which exhibit excellent light trapping properties[75]. This approach is studied in LPICM, with a small and productive team working on plasma synthesized nanowire silicon solar cells[76–79].

[72] A. Oskooi et al., Applied Physics Letters, **100**: 181110, 2012.
[73] E.R. Martins et al., Physical Review B, **86**: 041404, 2012.
[74] F. Pratesi et al., Opt. Express, **21**: A460–A468, 2013.
[75] P. Krogstrup et al., Nat Photon, **7**: 306–310, 2013.
[76] P.-J. Alet et al., J. Mater. Chem., **18**: 5187–5189, 2008.
[77] L. Yu et al., Applied Physics Letters, **97**: 023107, 2010.
[78] B. O'Donnell et al., Journal of Non-Crystalline Solids, **358**: 2299–2302, 2012.
[79] S. Misra et al., Solar Energy Materials and Solar Cells, **118**: 90–95, 2013.

Alternatively, nanostructures can be decoupled from the active material to keep the excellent surface recombination achievable on a flat interface. The use of high refractive index dielectric nanoparticles to produce multiple Mie scattering events, eventually combined with metallic nanoparticles[80], has shown promising results: Lee et al.[81] could demonstrate a significant absorption enhancement with TiO_2 nanoparticles located on the rear side of the cell, and Spinelli et al.[82] could reach 4 ms effective lifetime with $\sim$ 3% averaged broad range reflectivity using Al_2O_3 to passivate flat wafer interface and nanopatterned TiO_2 anti-reflective coating on the front surface.

4.3.2 Nanostructured silicon solar cells

The following work has been done within the framework of two research projects: the french ANR NATHISOL (NAnophotonics for THIn film crystalline silicon SOLar cells) and the european FP7 PhotoNVoltaics (Nanophotonics for ultra-thin crystalline silicon photovoltaics). NATHISOL gathers 4 partners: - Nanotechnology Institute of Lyon (INL-CNRS) - Laboratory of Photonics and Nanostructures (LPN-CNRS) - Laboratory of Physics of Interfaces and Thin Films (LPICM-CNRS) and - Total Energies Nouvelles[3]. The project is based on thin (2-5μm thick) crystalline silicon films absorber grown by low temperature PECVD, and aims at producing a >13% efficient solar cell transferred to a foreign substrate, with the help of advanced plasmonic and photonic structures. Some part of the results achieved in this project can be found in the thesis manuscript of I. Massiot[83].

PhotoNVoltaics gathers 7 partners: - Interuniversitair Micro-Electronica Centrum (IMEC) - Nanotechnology Institute of Lyon (INL-CNRS) - Laboratory of Physics of Interfaces and Thin Films (LPICM-CNRS) - Facultés Universitaires Notre-Dame de la Paix (FUNP) - Obducat Technologies AB (OBDU) - Chalmers University of Technology (Chalmers) and - Total Energies Nouvelles. This project targets the production of efficient nanostructured thin film Si solar cells based on a broad range of materials and techniques: the silicon materials in this project are poly or monocrystalline, produced by PECVD, APCVD or epi-free process, and several nanopatterning and etching processes are tested. It also targets more fundamental studies such as the optimal pattern design (order/controlled disorder/disorder, etc.).

Experimental results

In both projects, the LPICM was involved in nanostructures passivation and solar cells fabrication. Thus, the simulation part and the various patterning methods will not be detailed here; the reader can find a broader presentation of PhotoNVoltaics project in the paper from Trompoukis et al.[64]. Following a top down approach, the nanostructures were first tested on high quality FZ wafers and then the process was extended to ultra-thin PECVD epitaxial silicon layers. This work has been done in collaboration with two post-doc researchers at LPICM: Ismael Cosme Bolanos and Wanghua Chen.

The fabrication of nanostructures studied in this work involves two main processes: 1) definition of the mask by lithography techniques, namely here by using nanoimprint lithography (NIL)[84] and 2) etching process for the formation of the pattern via dry plasma reactive ion etching (RIE), wet chemical etching using tetramethyl ammonium hydroxide (TMAH). The nanoimprint step has been performed in OBDUCAT facilities and the etching (wet and dry) were done at IMEC. The impact of the nanopatterning, for the wet and for the dry process, on the c-Si wafer's passivation quality as well as on solar cell performances were tested. Two 280μm thick float zone (FZ) silicon wafers, p-type with a resistivity of 1-5 Ω.cm and (100)-oriented were used for this purpose. The nanopattern,

[80] S. Jain et al., Progress in Photovoltaics: Research and Applications, , 2014.
[81] B.G. Lee et al., Applied Physics Letters, **99**: 064101, 2011.
[82] P. Spinelli et al., Applied Physics Letters, **102**: 233902, 2013.
[3] TOTAL Energies Nouvelles R&D, Tour Michelet 24 cours Michelet - La Défense 10 92069 Paris La Défense Cedex.
[83] I. Massiot. *Design and fabrication of nanostructures for light-trapping in ultra-thin solar cells.* PhD thesis. Université Paris Sud - Paris XI, Oct. 2013.
[84] L.J. Guo., Advanced Materials, **19**: 495–513, 2007.

a periodic square array of holes, was fabricated by nanoimprint lithography (NIL) using a polymer resist spin-coated directly on the c-Si surface (dry sample) or on a SiO_2 hard mask (wet sample).

- In the case of the wet etched sample, the SiO_2 film on both sides was deposited to serve as a hard mask for patterning one side and to prevent random etching on the other side during the wet chemical process. The pattern has been transferred from the resist to the SiO_2 hard mask by CHF_3/O_2 plasma-etching and then the chemical etching of the c-Si surface was performed with 10% tetramethyl ammonium hydroxide (TMAH) diluted in water at 80°C. After the TMAH etching, an H_2SO_4/ H_2O_2 (so called SPM) + HF mixture was used to remove the residual resist and the SiO_2 hard mask on both sides.

- For the dry etched samples, the pattern was directly transferred to the c-Si Surface from the NIL resist by reactive ion etching (RIE) using a SF_6/O_2 gas mixture under a total pressure of 100 mTorr. The resist mask was removed with SPM + HF solution.

On both samples, before passivation, the native oxide was removed by a 60s 5% HF dipping. A capacitively coupled RF (13.56 MHz) PECVD reactor has been used to deposit an a-SiC:H/a-Si:H stack at 175°C from a SiH_4 and CH_4 gas mixtures. The ultrathin a-SiC:H film ($\sim$1nm) was used to prevent epitaxial growth on the (100) c-Si surface. The 20nm-thick a-Si:H film was grown from the dissociation of 50 sccm of silane at a pressure of 50 mTorr. Finally, HiT solar cell structures were fabricated on the 280μm nanopatterned wafers with a 25nm emitter consisting of a-SiC:H/a-Si:H/(n+)a-Si:H stack deposited by PECVD (similar condition to Tab.4.1). To complete the structure, the back stack consisting of a-SiC:H/a-Si:H/(p+) a-Si:H was deposited by the dissociation of trimethylboron and SiH_4. An active solar cell area of 1 cm^2 was defined by sputtering ITO through a shadow mask followed by Al grid contact evaporation through a shadow mask. Back contacts were also formed by Al evaporation on the whole surface. The effect of the nanopatternig on the electronic properties was quantified by probing the effective minority carrier lifetime (τ_{eff}) deduced from photo-conductance decay measured with a Sinton WCT-120s setup. The topography of the nanopatterned wafers was studied by scanning electron microscopy (SEM) and the total spectral reflectance was measured in the wavelength range of 300nm to 1100nm using an integrating sphere. The solar cell parameters of the HiT structures were extracted from current-voltage measurements under AM1.5G illumination and external quantum efficiency (EQE) measurements.

Experimental results of wafer nanopatterning and reflectivity are displayed in Fig.4.14. The top left picture shows a piece of 4 inch wafer nanopatterned with the wet etching process. The visible colors are the result of diffraction of the white light coming on the nanostructures. The SEM cross sections of the patterns formed on the (100) FZ c-Si wafers for wet and dry etched samples are shown on the left side of the figure. The TMAH wet chemical etching through the NIL SiO_2 hard mask is based on the different etch rates for the (111) and (100) crystallographic planes (see previous chapter), and results in a periodic array of inverted nanopyramids with the (111)-oriented walls. On the other hand, dry plasma etching being independent of the crystal orientation, parabolic shapes are obtained on the c-Si surface. The final structures have a depth and a diameter of about 300nm for the dry etched sample and the wet etched pyramids have a 500nm square base with a 54.7° top angle. As a result of the dry etching processes, the sidewalls of the craters are slightly corrugated, contrary to the faceted aspect in the case of wet etching. On the right side of Fig.4.14 are plotted the total reflectance as a function of wavelength, measured at an angle of incidence of 8°, for flat, dry and wet etched samples. This measurements are done before the deposition of a-Si:H and ITO, thus they correspond to the nanostructured surface only. The total reflectance decreases significantly for both dry and wet etched samples, as compared to the mirror polished flat wafer. For these specific topographies, the wet etched sample exhibits a slightly lower reflectance than the dry etched one. Compared to the classic random pyramid etching process, this approach attractively offers improved light trapping with a minimal material waste; in addition, a carefully optimized pattern design would provide further

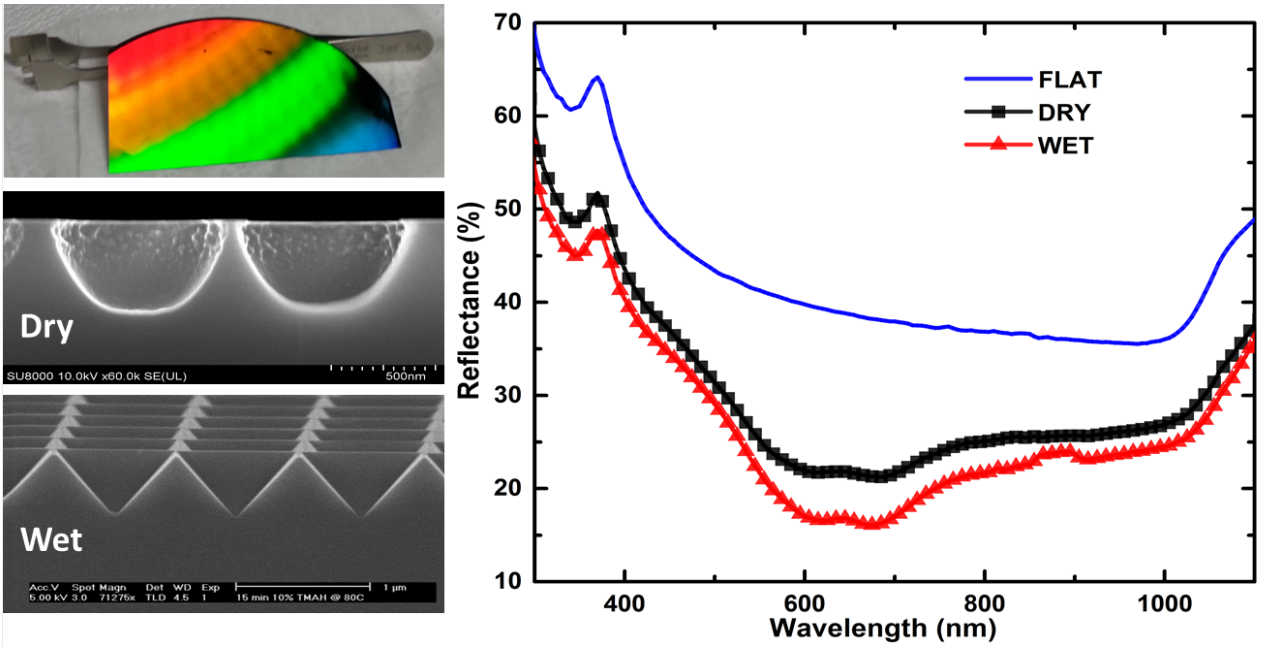


Fig. 4.14 – Left: picture of a nanostructured (inverted pyramids) piece of c-Si 4 inch wafer; cross section section SEM of two nanopatterned samples: dry etched holes and wet etched inverted pyramids. Right: total reflectance measured with an integrating sphere for a flat polished silicon surface and for the wet and dry etched nanostructures shown on the left.

reflectance reduction.

The effective lifetime versus the injection level, as measured by photo-conductance decay, is shown in Fig.4.15-a) for the flat, wet and dry etched samples. The effective lifetime reflects the recombination processes in the bulk and at the surfaces and is defined as follows[85,86]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{S_{front} + S_{back}}{W} \tag{4.9}$$

where τ_{bulk} is the bulk lifetime, W the thickness of the substrate, and S_{Front} and S_{Back} are the recombination velocities in the front and the back surfaces respectively. We used a double side a-Si:H passivated 280μm reference wafer to calculate the recombination velocity on a flat surface S_{flat}, assuming that τ_{bulk} is infinite and that the passivation is symmetrical at the front and back surfaces. With this result, the nanopatterned surface recombination velocity S_{np} has been calculated for the wet and dry sample according to $S_{textured} = W/\tau_{eff} - S_{flat}$.

The reference sample shows the highest value of 2.2 ms whereas the nanopatterned wet and dry etched samples encounter respectively a 3 to 5 times reduction in carrier lifetime, as measured for an excess carrier concentration of 2.10^{15}cm^{-3}. This trend is confirmed by TRMC measurements as shown in Fig.4.15-b): TRMC decay time of 711, 350 and 210 μs are found. While it is more tricky to get well calibrated absolute values with our home-built TRMC set-up compared to the commercial photo-conductance set-up, both methods give the same conclusion: $\tau_{Flat} > \tau_{Wet} > \tau_{Dry}$. With the equation 4.9, the effective surface recombination velocities were calculated assuming that all flat surfaces have the same passivation quality. The results, 52, 33 and 6 cm/s for the dry, wet and flat sample, confirm an important damage to the surface by the dry process, leading to the lowest lifetime value from all studied samples. The passivation quality of the wet etched sample is also reduced compared to the flat sample, but the degradation is less important than for the dry etched sample. In addition,

[85] A.W. Stephens et al., Journal of Applied Physics, **76**: 363, 1994.
[86] A.B. Sproul., Journal of Applied Physics, **76**: 2851, 1994.

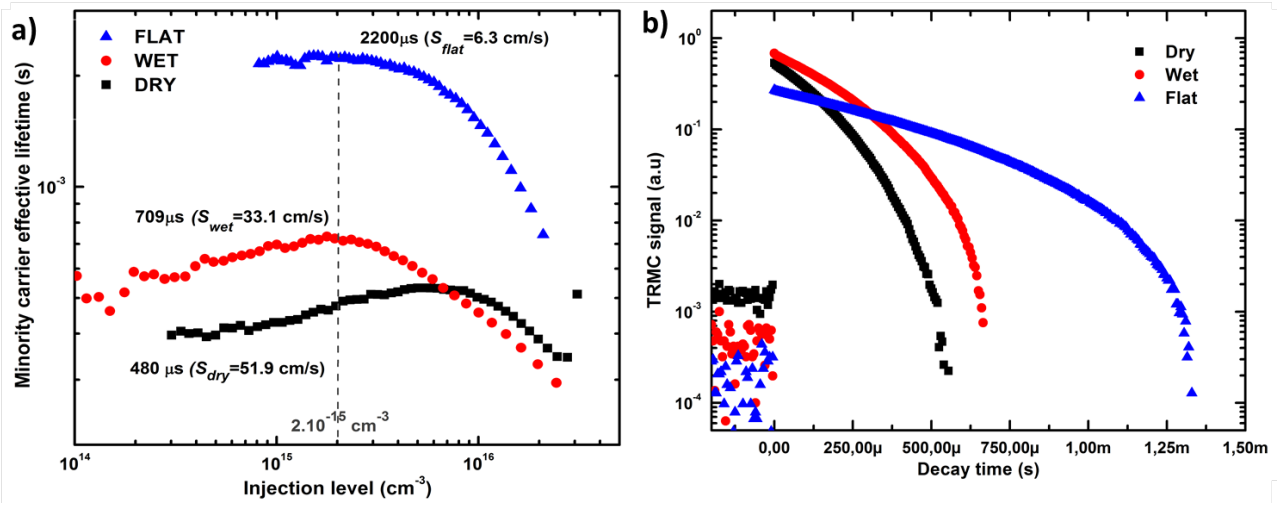


Fig. 4.15 – Comparison of effective minority carrier lifetimes for flat, dry etched and wet etched nanopatterned a-Si:H passivated 280-μm thick (FZ) p-type c-Si wafers, measured by a) photoconductance and b) Time resolved microwave conductivity.

as reported in literature[70], the passivation of such inverted pyramids can achieve better results, since recombination velocities below 10 cm/s are reported.

The current-voltage characteristics of wafer based HiT nanopatterned solar cells, after a post-frabrication 30 min annealing at 175°C in N_2/H_2, is displayed in Fig.4.16-a). The flat solar cell exhibits a V_{oc} of 580mV, a J_{sc} of 26.4 mA/cm^2, a fill factor of 71.4% resulting in an efficiency of 11%. Both dry and wet etched samples have a higher current (respectively 28.1 and 29.3 mA/cm^2), thus proving the beneficial effect of light trapping on the short circuit current. The dry etched sample has the lowest performances, as expected; its efficiency, below 10%, is penalized by a lower V_{oc} (550mV) and series resistances. The wet etched sample has comparable efficiency with the flat reference sample, but with higher current, 10 mV higher V_{oc} and a lower fill factor. This good V_{oc} is the proof of a good passivation of the surface, passivation which is improved by the final annealing treatment. The highest short circuit current density, 29.3mA/cm^2, measured for the wet etched sample, is in good agreement with the reflectance shown in Fig.4.14. The increase in the short-circuit current has also been confirmed by external quantum efficiency (EQE) measurements. Indeed, as shown in Fig.4.16-b), for short wavelengths, where EQE is sensitive to the device surface (passivation quality, optical losses), the EQE is higher for both dry and wet etched samples compared to the flat solar cell. This means that despite a lower passivation quality on the nanopatterned samples, the lower reflectivity produces an overall EQE improvement in this region. To be more precise, one should have plotted IQE to get rid of reflectance differences between the samples; however, the reflectance on the final device has not been measured yet. However, EQE comparison for the nanopatterned samples, in the short wavelength region, shows a lower increase for the dry sample, this is a logical consequence of the higher surface recombination velocity and higher reflectance of the dry sample compared to the wet etched sample. The relatively high series resistance found in both dry and wet etched samples was identified by cross section SEM (not shown here) to come from some conformality problems of ITO (mainly on dry etched sample) and/or metal contacts. This could be improved by choosing more conformal deposition techniques. Around 1000nm, the dry etched sample has lower EQE compared to the two other samples; this is likely the result of a lower passivation quality on the back side of this sample; indeed since the 3 samples come from the same wafer box, only the surface passivation quality and texturation are variables. By integration with the AM1.5G solar spectrum, one can get the short circuit current density. While the highest current is still found for the wet etched sample with this technique, the results obtained, 30.8, 26.3 and 26.4 mA/^{2} show some discrepancy with the solar

simulator results. The origin of those differences may be explained by the fact that our experimental set-up is measuring EQE on a very small spot (∼2×2mm) whereas the I-V is measured for a 1cm^2 cell. Thus there is probably some variation in passivation quality or nanostructures shape over the surface of the solar cells.

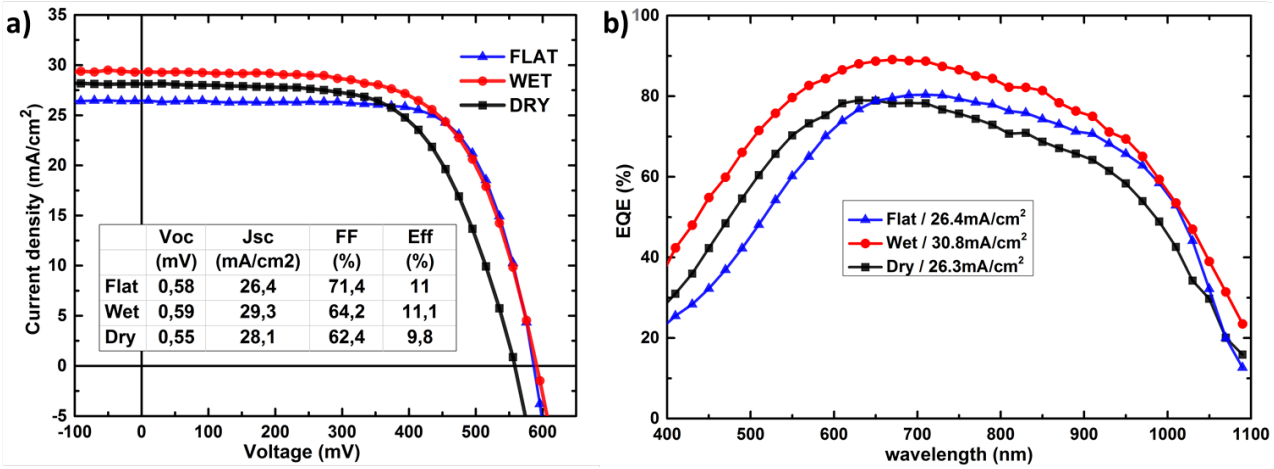


Fig. 4.16 – a) J-V characteristics of flat, dry etched and wet etched nanopatterned wafer HiT cells. b) Corresponding EQE curves.

To sum up, from reflectance and passivation measurements, the inverted pyramids produced by NIL and wet etching was found to be the best compromise between optical trapping properties and minimized electrical degradation of the surface. These results were confirmed by a good $\boldsymbol{V_{oc}}$ and superior current density in the case of HiT wafer based cells with NIL inverted pyramids. Thus both electrical and optical characterizations demonstrate that the wet etching process is a promising method; the next step is then to implement such nanopatterns on ultra-thin crystalline silicon film where classic texturation leading to high material waste cannot be applied. Finally electro-optical simulations are also required to find out the best pattern and design (size, filling factor, etc.) that maximize absorption and collection for the thin film device; this crucial aspect is being studied in PhotoNVoltaics and Nathisol projects.

However, working with the above-mentioned un-optimized nanoimprint patterns, first nanostructured epitaxial solar cells have been fabricated by using the same structure as presented in fig.4.5-a) but with a textured epi-Si/a-Si:H interface. The schematics of the cell is shown in fig.4.17-a). To form such a structure, the sample is taken out of the PECVD reactor after the epitaxial growth of the absorber layer for the nanoimprint and etching steps, which are done respectively at Obducat and IMEC. The resulting pattern for the dry and wet etching process is visible in Fig.4.17-b,c) cross section SEM. One can see that the pattern is not very well defined; indeed the PECVD epitaxial having a slightly lower material quality compared to the bulk c-Si, the etching recipes behave differently on PECVD epi-Si and c-Si wafer. For the inverted pyramids, the mask should be carefully aligned with crystallographic axes, mask's strips width should also be adjusted since the etching selectivity of (111)/(100) is different from a high quality FZ substrate, and the etching conditions (temperature, dilution, time). For this first test, none of this parameters have been optimized, and as a result, the pattern is poorly defined. Notwithstanding these imperfect nanopatterns, solar cells were formed by HF-cleaning of the surface followed by PECVD deposition of a-Si:C/a-Si:H/n-a-Si:H to form the emitter layer. The flat reference epitaxial cell (4.4$\boldsymbol{\mu}$m absorber thickness) has been compared with the dry and wet etched cells under solar simulator. The results are shown in Fig.4.17-d).

For this specific batch, the flat cell resulted in a 5.9% with 490mv $\boldsymbol{V_{oc}}$, a $\boldsymbol{J_{sc}}$ of roughly 16 mA/cm^2 and a fill factor of ∼ 75%. The dry etched sample has shown a significantly lower performance, namely 1.5%, with a 100 mV lower $\boldsymbol{V_{oc}}$ and a $\boldsymbol{J_{sc}}$ reduced more than twice. Clearly, this etching conditions and

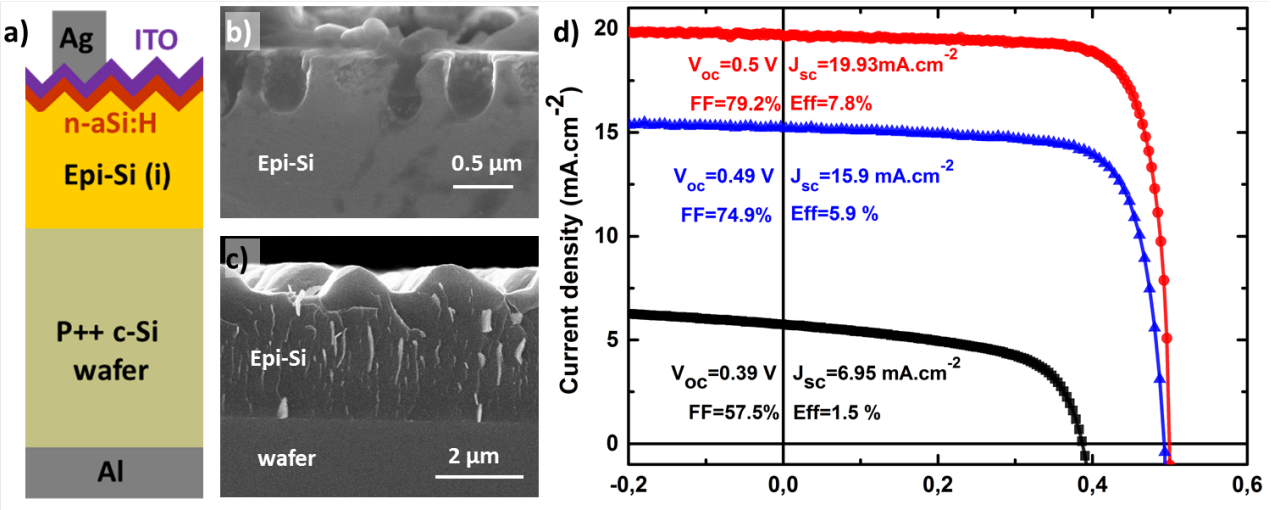


Fig. 4.17 – a) Diagram of nanopattern epi-Si cell on wafer. Cross section SEM picture of poorly defined nanopatterns on epi-Si: b) holes and c) inverted pyramids. d) Comparison of J-V characteristics for a flat, hole shaped and inverted pyramids epi-si cells.

the passivation of the holes have failed for this sample. On the opposite, the wet-etched sample could reach 19.9 mA/cm^2 and an efficiency of 7.8% with a similar $\boldsymbol{V_{oc}}$ compared to the flat sample. Those absolute values remain below our best flat epitaxial cell (see Tab.4.2), but the huge improvement in short-circuit current without degradation of the $\boldsymbol{V_{oc}}$ is clearly showing that this patterning approach is relevant for ultra-thin epitaxial solar cells.

4.4 Detachment and transfer of thin film c-Si layers

4.4.1 Literature overview

The epitaxial solar cells previously presented in this manuscript were all made on highly doped wafer, acting mainly as a crystal seed and contact material. However the lift-off and transfer of such low temperature epitaxial layers is attractive since it opens up a lot of possibilities: i) Independent electrical characterization of epitaxial layers ii) Production of ultra-thin monocrystalline layers of various thicknesses on low cost substrate (e.g. flexible plastic) ii) Potential substrate re-use iii) Increased light trapping for transferred epi-Si cells with appropriate back side processing, etc.

Various lift-off techniques can be found in literature to produce 1-50$\boldsymbol{\mu}$m thick silicon slabs. They can be separated in two classes: i) the cleaving approach and ii) the porous silicon based methods.

- Cleaving can be induced for instance by hydrogen implantation to create an in-depth cleavage zone[87–90]. This is the basis of the Smart-Cut process from the company SOITEC, a process which was initially developed at CEA-Leti in the nineties[91,92]. Other processes based on both hydrogen and thermal stress are also reported[93]. Indeed, the differences in thermal expansion coefficients between silicon and a stressor layer (e.g. Al, Cr, Ag, Ni, etc.) combined with an adjusted annealing profile enable to control the stress induced in the c-Si and lift-off of a Si

[87] S.T. Pantelides et al., Solid State Phenomena, **69-70**: 83–92, 1999.
[88] Y. Zheng et al., Journal of Applied Physics, **89**: 2972–2978, 2001.
[89] T. Hochbauer et al., Journal of Applied Physics, **92**: 2335–2342, 2002.
[90] X. Hebras et al., Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, **262**: 24–28, 2007.
[91] M. Bruel *Process for manufacturing thin film layers of semiconductor material* EP Patent App. EP19,920,402,520 1993
[92] M. Bruel et al., Japanese Journal of Applied Physics, **36**: 1636–1641, 1997.
[93] R.A. Rao et al., 37th IEEE Photovoltaic Specialists Conference (PVSC), 001504 –001507, 2011.

slab of few tens of microns[94,95]. This metal assisted stress engineering can also be used to exfoliate semiconductor layers at room temperature: this is the so called controlled spalling process developed by Bedell and co-workers of IBM Thomas J. Watson Center[96,97]. Excellent flexible devices have been achieved using this control spalling approach, such as GaInP/GaAs tandem solar cells[98] with efficiency above 28% or promising silicon integrated circuit on plastic[99].

- The second approach for producing ultra-thin c-Si layers is based on porous silicon[100]. Two regions with different porosity are created under the surface by electrochemical etching of the wafer in an HF solution: - the top most layer with a low porosity, thus used as a crystal seed layer for subsequent epitaxial growth - Below the low porosity layer, a high porosity layer weakly attached to the substrate, allowing an easy lift-off of epi film. There are plenty of thin film c-Si cells in the 20-50μm ranged produced with the porous silicon process[18–20], including the actual 20.4 % record cell of Solexel[17]. There is also the so called Epi-free process, developed at IMEC[101,102], which is somehow based on a porous layer too: an array of regular pores ($\sim$ 550nm) are formed by UV-lithography and reactive ion etching, and then upon a strong annealing in non-oxidizing ambient (1150°, N_2 or H_2) the surface reorganizes leading to the formation of a 1-2μm thick Si layer on voids. This technique has been used to produce a transferred 1.1μm cell reaching 4.8% efficiency[16]. More recently a combination of photolithography and electrochemical etching has been used to produce a "silicon millefeuille"[103]: several stacks of high and low porosity layers are produced and re-arranged upon annealing into a juxtaposition of c-Si slabs of few microns separated by voids.

As for PECVD epitaxial layers, Moreno et al.[104,105] have shown that a porous wafer/epi interface layer enables lift-off at moderate annealing temperature ($\sim$ 400°C). This approach will be further detailed in this section.

4.4.2 PECVD epitaxy on Epifree

As mentioned above, the Epifree process enables the production of 1-2μm thick c-Si layers suspended on a void rich layer. This ultra-thin c-Si layer can then easily be lifted-off if glued to another substrate (c-Si is not self-supporting for such thin thickness).

A picture of this Epifree material is represented in Fig.4.18-a): 4 square areas of Epifree (orange color) are visible on this 8 inch c-Si wafer. The color change from orange at the wafer center to greenish on the side is linked to a variation of the shape and density of voids below the Epifree layer. A roughness of 1.7nm is found by AFM, which is pretty low given the high aspect ratio of the material before annealing. Fluctuation of the voids size and shape below the 1.2μm surface c-Si may be responsible for the wavy aspect of the surface visible in AFM. Cross section SEM pictures taken at different times during the annealing step of the Epifree process[101] are displayed in b): from top to

[94] F. Dross et al., Applied Physics A, **89**: 149–152, 2007.
[95] I. Gordon et al., Solar Energy Materials and Solar Cells, **95, Supplement 1**: S2–S7, 2011.
[96] S.W. Bedell et al., IEEE Journal of Photovoltaics, **2**: 141 –147, 2012.
[97] S.W. Bedell et al., Journal of Physics D: Applied Physics, **46**: 152002, 2013.
[98] Davood Shahrjerdi et al., Nano Letters, , 2012.
[99] D. Shahrjerdi et al., Advanced Energy Materials, **3**: 566–571, 2013.
[100] C.S. Solanki et al., Solar Energy Materials and Solar Cells, **83**: 101–113, 2004.
[18] J.H. Petermann et al., Progress in Photovoltaics: Research and Applications, **20**: 1–5, 2012.
[19] M. Reuter et al., Solar Energy Materials and Solar Cells, **93**: 704–706, 2009.
[20] R.B. Bergmann et al., Solar Energy Materials and Solar Cells, **74**: 213–218, 2002.
[17] P. Kapur et al., 28th EU PVSEC Proceedings, **3DO.7.6**: 2228 –2231, 2013.
[101] V. Depauw et al., Journal of Applied Physics, **106**: 033516–033516–10, 2009.
[102] V. Depauw et al., Progress in Photovoltaics: Research and Applications, **19**: 844–850, 2011.
[16] C. Trompoukis et al., Applied Physics Letters, **101**: 103901–103901–4, 2012.
[103] D. Hernàndez et al., Applied Physics Letters, **102**: 172102–172102–4, 2013.
[104] M. Moreno et al., EPJ Photovoltaics, **1**: 6, 2010.
[105] M. Moreno et al., Journal of Materials Research, **28**: 1626–1632, 2013.

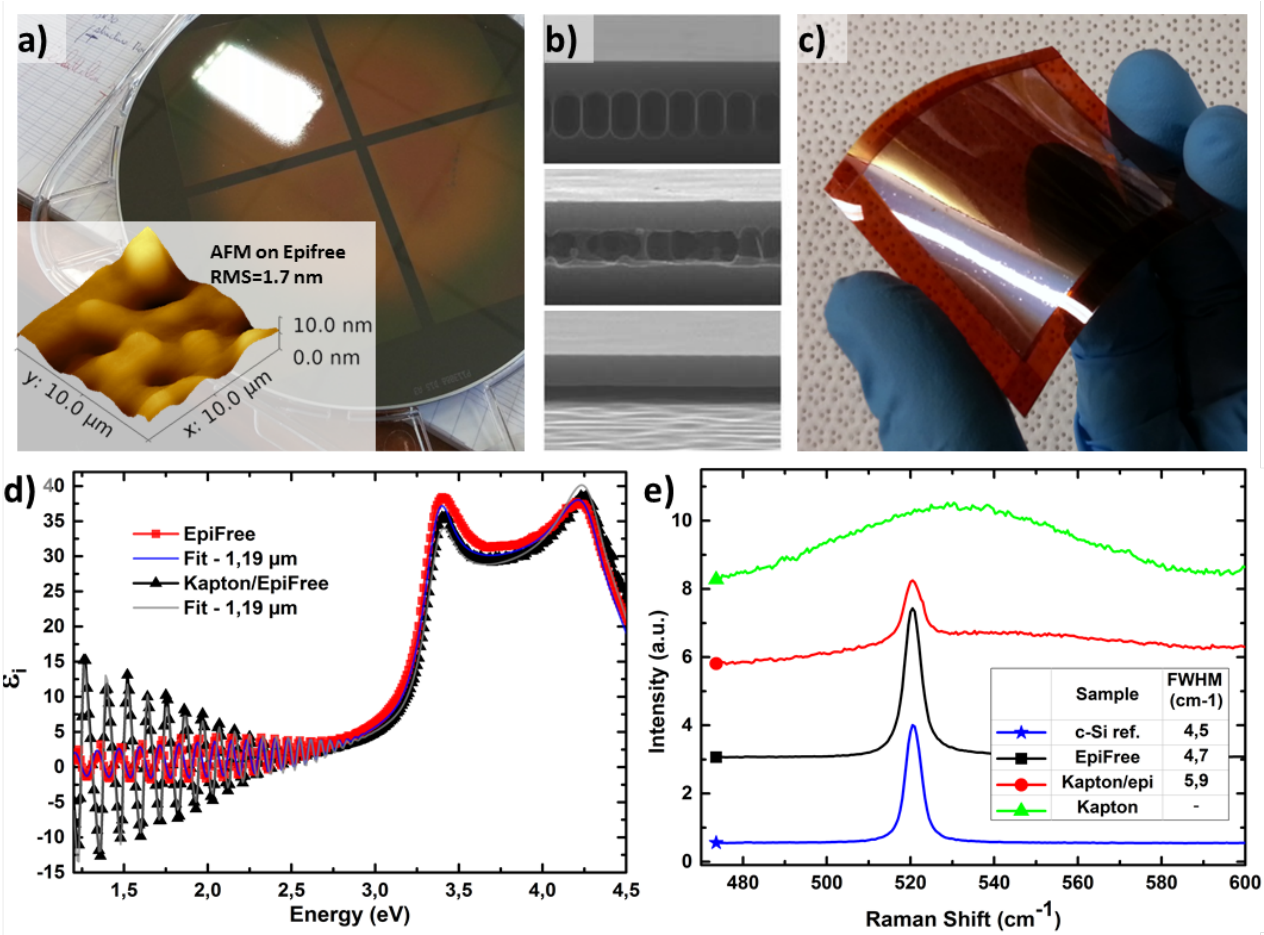


Fig. 4.18 – a) 8 inch. wafer with square areas of Epifree material. AFM roughness of Epifree surface. b) SEM pictures of voids evolution during the formation process of Epifree[101]. c) 5×5 cm^2 and 1.19μm thick Epifree peeled off with kapton tape. d) Experimental data and fits of the pseudo-dielectric function of Epifree before (squares) and after (triangles) kapton lift-off. e) Raman spectra of kapton (triangles), c-Si wafer (star), Epifree (square) and Epifree on kapton tape (circle).

bottom, an increase of the pore size for longer annealing is visible. The final material has void areas with a lateral extension of several tens of microns, thus a very weak attachment to the substrate. This is illustrated in Fig.4.18-c), where a $\sim 5\times 5 cm^2$ Epifree sample is glued on kapton tape. Indeed by applying manually a small pressure between a piece of kapton tape on Epifree material, the thin c-Si slab is peeled off easily. Ellipsometry measurements have been performed before and after this kapton tape assisted lift-off, the results are shown in Fig.4.18-d). The imaginary part of the pseudo-dielectric function ε_i of the Epifree material before lift-off is represented in red (squares) and the Epifree on kapton in black (triangles). The same thickness, namely 1.19μm, is found by fitting ε_i before and after the lift-off, thus confirming that the full layer is reported on kapton. The impact of this simple transfer process on Epifree crystalline quality has been checked by Raman spectroscopy, with a 632nm laser. In Fig.4.18-e) are gathered the Raman spectra of a c-Si reference wafer (star symbols), the kapton tape alone (triangles), the Epifree (squares) and the Epifree transferred on kapton tape (circles). The full width at half maximum (FWHM) of the c-Si peak provides a good indication of the crystal quality; here the Epifree FWHM, 4.7cm^{-1}, is very close to the one of c-Si reference, 4.5cm^{-1}, thus confirming the excellent crystal quality of this material. After the kapton peel off step, a FWHM of 5.9 cm^{-1} is found: the layer is slightly altered by the lift-off step, which may create some cracks, but remains of good quality, as also seen from the high ε_i amplitude measured by ellipsometry.

As shown above, the Epifree material is very easy to lift-off, however its thickness is limited to

$\sim$2μm, while a 5 to 10 μm thick c-Si slab would boost significantly the short circuit current. Thus we have tried to thicken Epifree material by means of low temperature PECVD epitaxial growth. Both an Epifree sample and a standard c-Si wafer were cleaned by HF dip, and then loaded into the PECVD reactor. The epitaxial growth was performed at 175°C in a SiH_4/H_2 plasma. The ε_i functions for the two co-deposited samples, measured ex-situ after deposition, are shown in Fig.4.19. The first peak (at 3.4 eV) of ε_i has an amplitude close to 37 in both cases and the second crystalline peak (at 4.2 eV) reaches slightly more than 42 on wafer and slightly below 42 on Epifree. Such high amplitudes are a good proof of the excellent epitaxial quality on Epifree, which is almost similar to that achieved on c-Si, despite a 1.7 nm roughness and relatively wavy surface of the initial epi-free (see Fig.4.18-a) AFM). The inset shows also a zoom on the low energy part of the spectrum, where the visible oscillations are related to thickness and wafer interface composition. For the epitaxial growth on wafer, a film thickness of 1.62μm is found by fitting this experimental data. For the epitaxial growth on Epifree, the fringes with higher amplitude and smaller period in the low energy part betray a thicker layer and a higher contrast at wafer interface, due to the void rich layer below the Epifree. The total thickness deduced from fitting the ellipsometry data is 2.99μm, which confirms that the Epifree thickness could be more than doubled with this approach. A small diagram on the right part of Fig.4.19 sums-up the process flow of Epifree thickening and lift-off. The Epifree material can be used as a crystal seed layer which has the advantage of providing both a high quality crystal surface for epitaxial growth and a weak attachment to the substrate (void rich layer beneath) enabling easy transfer. Further work is still needed to explore more precisely how the material quality is affected by the transfer of this double stack, and to find out the best solar cell design compatible with this approach.

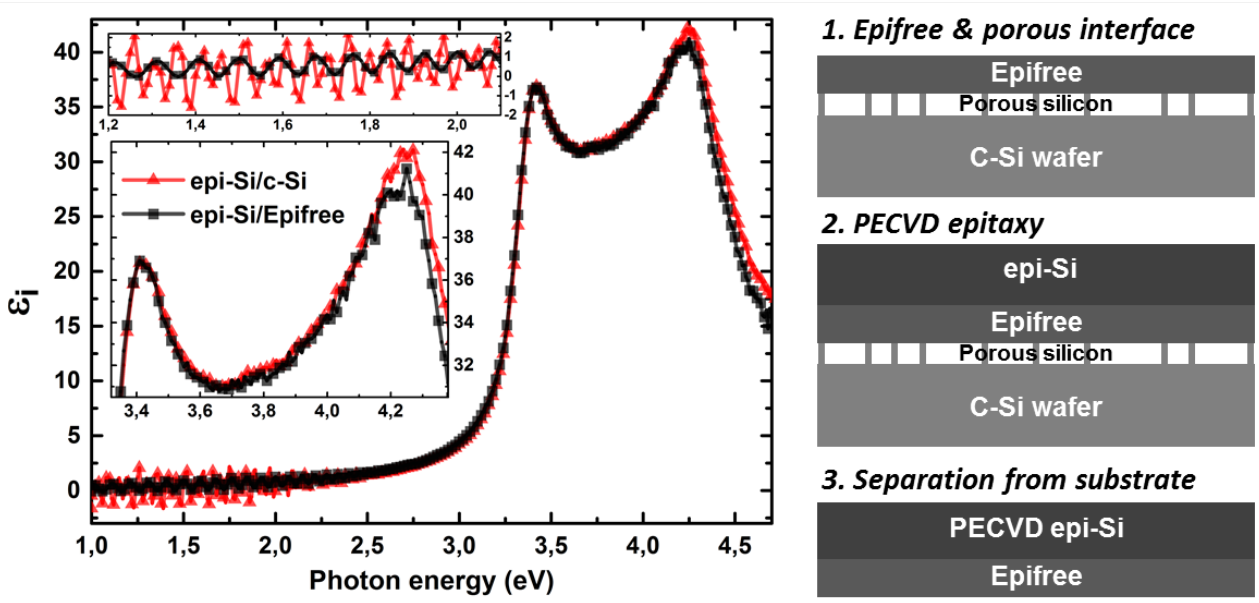


Fig. 4.19 – Left: ellipsometry measurement of ε_i for 1.6μm PECVD Si epitaxial growth at 175°C on c-Si wafer (triangles) and on Epifree (squares). Right: diagram of PECVD epitaxy on Epifree, a possible path to produce and detach ultra-thin c-Si slab of few microns.

4.4.3 PECVD Epi-Si lift-off

The transfer of a PECVD layer grown on Epifree is an interesting process, since it can probably reach a high yield and reproducibility, however this is certainly not the most simple, logical and cost effective approach (lithography step, annealing above 1100°C, etc.). More interestingly, Moreno et al.[104] have demonstrated the possibility to peeling PECVD epitaxially grown layers with a short post-deposition annealing step at 450°C. By varying the on H_2/SiF_4 ratio in Ar dilution, they could obtain a H-rich wafer interface layer[105] (creating nanocavities), which provides an easy to cleave direction.

Their epitaxial growth was based on $SiF_4/H_2/Ar$ plasma, a different chemistry compared to the SiH_4/H_2 used in this thesis, and the lift-off was performed thanks to a rapid annealing above 400°C of the epi-layer covered by metal and polymid. Indeed, there are two possible effects explaining this phenomena:

- The presence of an H-rich mechanically weak interface layer which acts as a preferential cleavage plane.
- The stress in the epi-Si layer, which can originate internally from its high hydrogen content, or externally from a stressor layer and thermal expansion upon annealing.

It is also likely that hydrogen diffusion during the annealing enlarge the nanocavities at the interface with the wafer. We present here our experimental results and understanding of this lift-off process for PECVD epitaxial layers grown in SiH_4/H_2 plasmas.

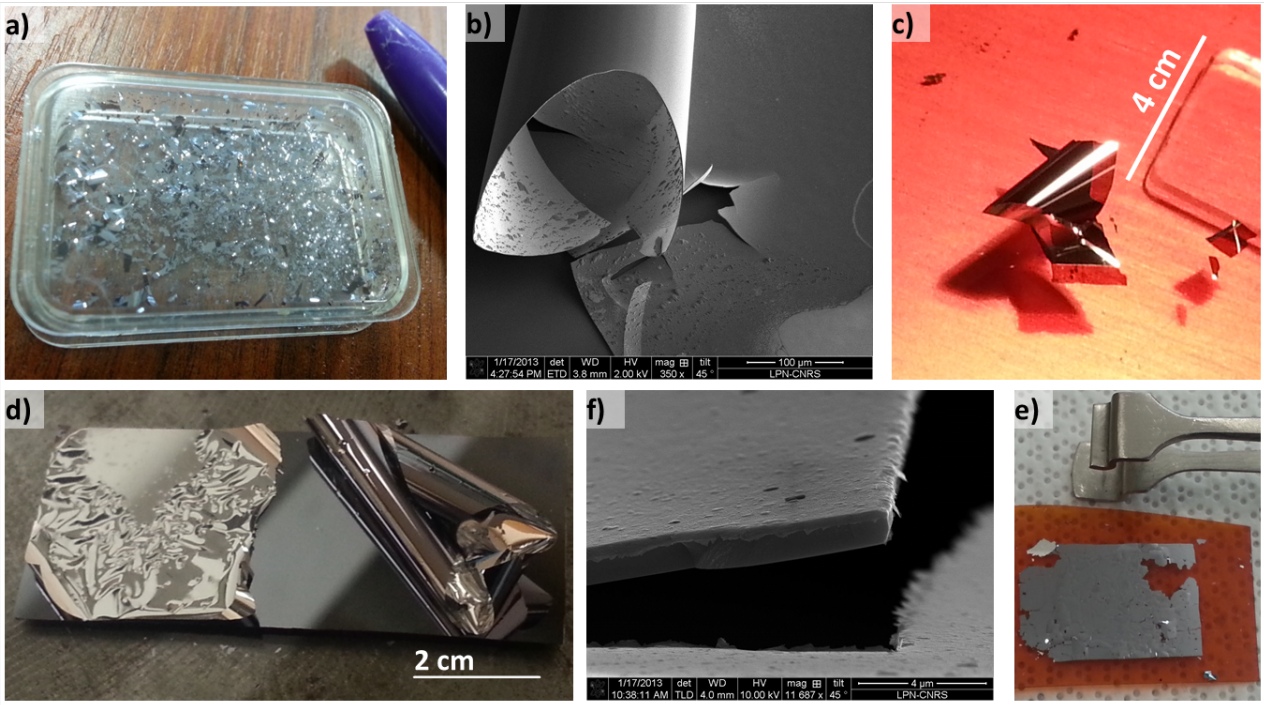


Fig. 4.20 – Examples of various lifted-off PECVD epi-Si layers (1-4μm thick): a,b) small and big epi-flakes obtained by annealing few seconds the sample at 400°C. c) SEM picture of a bended small epi-Si flake. Large lifted-off areas are obtained when providing mechanical support: d) with metal evaporated on epi-layer before annealing, e) by gluing the epi on kapton tape. f) SEM picture of lift-off starting edge for metal covered epi-Si.

Thus we first performed rapid thermal annealing on our standard epi-Si layers grown on wafer without any specific interface treatment. The annealing was performed with a simple heating plate (25-550°C range) at atmospheric pressure, in air. Surprisingly enough, we could lift-off some of the epi-Si samples despite no specific growth condition nor stressor layers. Pictures illustrating such lift-off are displayed in Fig.4.20-a,b,c). In some cases, annealing is not even necessary to perform lift-off: applying a mechanical perturbation, like wafer cleavage, initiate the lift-off and, if no transfer substrate is used, this result in silicon flakes of few millimeters size (see Fig.4.20-a)). The SEM picture in Fig.4.20-b) shows that small flakes may present strong bending, with here a few hundreds of μm diameter pipe shape. In most cases, the layer does not blow-up into flakes, and annealing is required for the detachment. In this case, larger self-supporting epi-Si sheets can be lifted-off, as shown in Fig.4.20-c). Of course, if this detached epi-Si layer is to be further processed, it is much more convenient to find

a better mechanical support to manipulate the layer. We have thus tried to perform lift-off of epi-Si layers with few hundreds of nanometers metal evaporated on top of it (Al), as shown in Fig.4.20-d): few centimeters square c-Si sheets are detached from the substrate, but this metal thickness is still not enough to prevent from bending and wrapping.

A SEM picture of the epi-Si (covered with 200nm Al) lift-off edge corner is shown in 4.20-f). The use of kapton tape to peel off and transfer the epi-Si layer has been also tested. The picture of an Al/epi-Si glued on kapton tape is shown in 4.20-e). The kapton tape can indeed support a brief temperature peak of 400°C; however the silicon adhesive used in kapton tape starts to deteriorate and evaporate. It was thus not possible to apply the tape before the annealing step; the epi-Si sample was removed from heating plate just when the lift-off begins and the kapton tape was applied right away. While large area samples could be obtained, this technique was penalized by its lack of reproducibility. Moreover, a better control of the peel off (speed, curvature radius, etc.) would be required to minimize cracks formed with this technique.

The interplay between annealing time and annealing temperature for epi-Si lift-off has been studied on one PECVD epi-Si sample. The result is plotted in Fig.4.21-a). The required annealing time span from 18 min at 280°C to 20s at 400°C; in this semi-log scale, there is a good linearity between the time and the inverse of the annealing temperature. The comparison between Raman spectrum of a 4μm thick epi-Si layer before lift-off and small free standing epi-Si flakes of the same layer after the detachment is shown in Fig.4.21-b). The layer before annealing (triangles) is right shifted compared to the c-Si reference (black curve) and the epi-Si flakes after detachment (circles) is left-shifted compare to the c-Si reference. Assuming bi-axial in plane stress, one can calculate (see eq.3.7) an $\varepsilon_{\parallel}$ of 0.07% before lift-off (compressive state, as mentioned in the previous chapter) and -0.07% after (tensile state). Note that the epi-Si flake is not perfectly flat and its stress is linked to its curvature. Overall, we have seen in the previous chapter that the layer stress depends on its hydrogen content and the interface quality with the wafer. Thus there is some variability from sample to sample depending on the wafer cleaning procedure, and the growth temperature; the curve in Fig.4.21-a) may thus be shifted upward or downward depending on the sample properties.

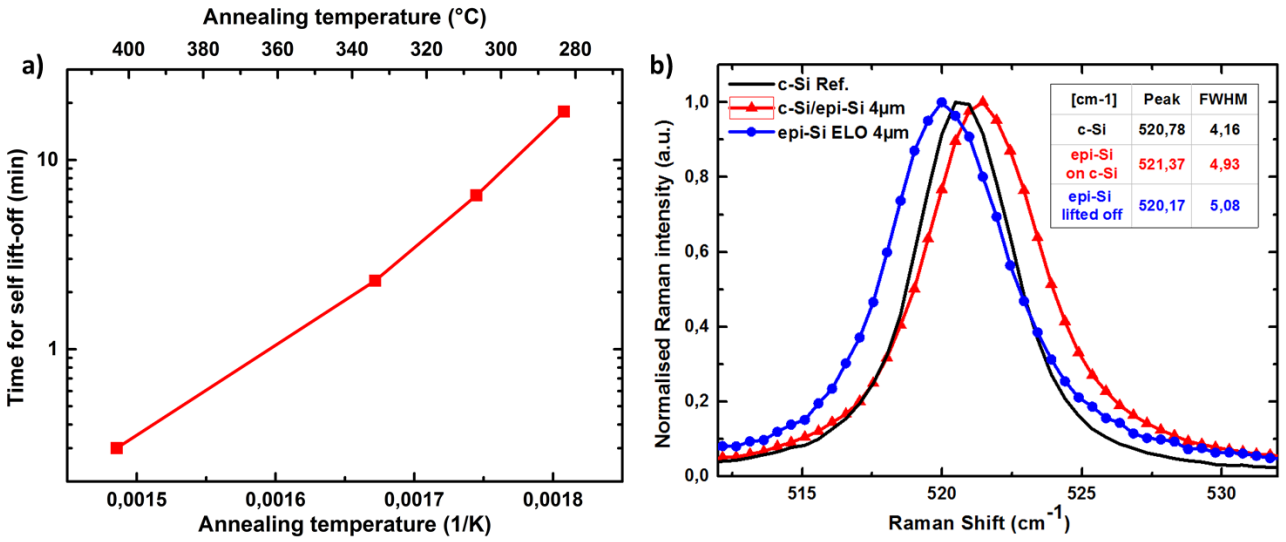


Fig. 4.21 – a) Required annealing time for epi-Si detachment as a function of annealing temperature. b) Raman spectra of epi-Si on wafer (triangles), free standing detached epi-Si flake (circles) and reference c-Si wafer.

To further investigate the link between wafer/epi-Si interface properties and low temperature PECVD epi-Si lift-off, we have performed cross section TEM analysis. Five PECVD epi-Si/c-Si sam-

ples, selected for their different interface quality, were thinned/polished by focused ion beam - FIB[4]. The interface between epitaxial silicon and wafer has been investigated with the aberration-corrected scanning electron microscopy (STEM; model No. JEOL JEM 2200FS AU7) available at LPN-CNRS, with the expert microscopists J.-L. Maurice and G. Patriarche. The high resolution cross section images along <110> axis of two samples are represented in Fig.4.22 and 4.22; the first sample was chosen for its robust epi-Si/c-Si interface: the layer does not lift-off upon annealing up to 550°C, whereas the second one is easily lifted-off for an annealing temperature above $\sim$ 300°C. Both conventional bright field and high-angle annular dark field (HAADF) images are shown for the two samples. HAADF images are formed by collecting high-angle scattered electrons with an annular dark-field detector in scanning TEM. Using this imaging method, there is a strong dependence of STEM image intensity on average atomic numbers of the scatterer elements encountered by the incident probe; it is generally admitted that the STEM-HAADF intensity I can be expressed as[106,107]:

$$\boldsymbol{I = k \sum n_i {Z_i}^{\alpha}} \tag{4.10}$$

where k is a constant, n_i are the number of atoms with atomic number Z_i in the probed volume, and $\boldsymbol{\alpha}$ a constant value in the range of 1.6 to 1.9[108]. Thus, a region with lighter elements or simply less atoms will appear darker on a HAADF image; if the sample thickness is uniform, the HAADF contrast is a function of the material density/chemical composition.

Fig.4.22-a) shows the conventional bright field image of the sample which has a strong interface (no lift-off upon annealing observed). With this technique, the interface is barely visible, in good agreement with the expected absence of weak/porous layer for this sample. The nearly perfect interface quality is confirmed by the HAADF picture of the same interface displayed in Fig.4.22-b). Indeed there is a $\sim$2nm wide slightly darker region at the interface. Since this sample was thinned down by FIB, the thickness is uniform and the contrast is not linked to a variation of number of atoms but rather to the presence of atoms with smaller atomic numbers compared to Si (H & O). The line scan showing HAADF normalized intensity (with respect to the wafer), perpendicular to the interface and averaged laterally on 4nm, is shown in the inset. The very small drop in intensity (and thus density) is confirmed by this technique.

[4]FIB preparation by D. Troadec at IEMN, via the French RENATECH network.
[106]S.J. Pennycook., Ultramicroscopy, **30**: 58–69, 1989.
[107]P.D. Nellist et al., Advances in Imaging and Electron Physics, **Volume 113**: 147–203, 2000.
[108]Z.W. Wang et al., Physical Review B, **84**: 073408, 2011.

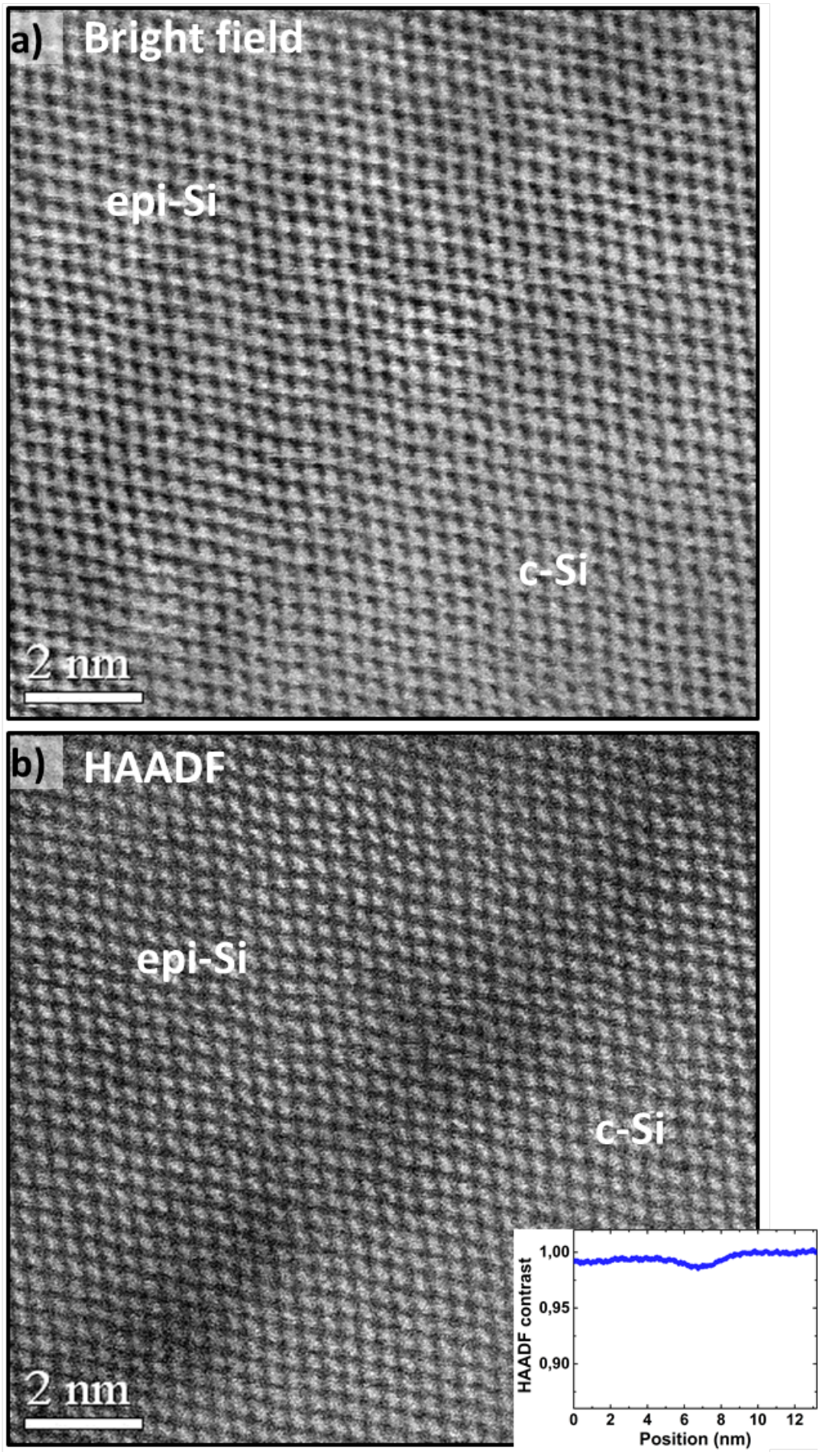


Fig. 4.22 – a) High resolution cross section scanning TEM bright field image along <110> axis of a clean epi-Si/c-Si interface. b) STEM-HAADF image of the same sample: a very small contrast change is visible at the interface. The normalized (with respect to wafer) HAADF contrast scan perpendicular to the interface, averaged on a 4nm wide rectangle is shown in the inset.

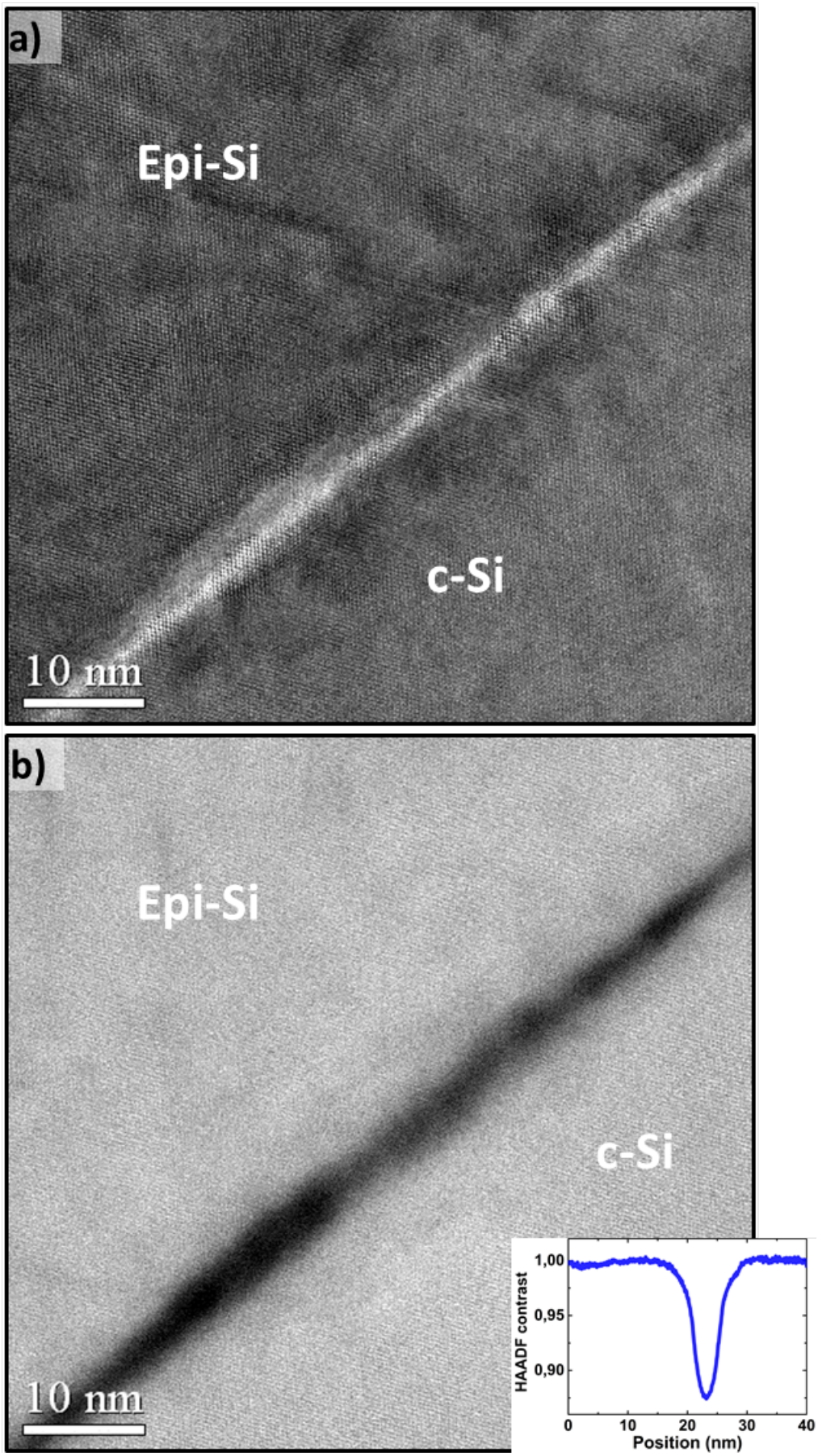


Fig. 4.23 – a) High resolution cross section scanning TEM bright field image along <110> axis of a weak epi-Si/c-Si interface. b) STEM-HAADF image of the same sample: a strong contrast is visible at the interface. The normalized (with respect to wafer) HAADF contrast scan perpendicular to the interface, averaged on a 5nm wide rectangle is shown in the inset.

Fig.4.23-a) shows the bright field high resolution cross section STEM image of the sample with an expected weak interface (easy layer lift-off with annealing at 300° and beyond). The interface appears blurry and well contrasted even in bright field mode. The defective nature of the interface for this sample is further confirmed by the HAADF image in Fig.4.23-b): the interface appears much darker compared to the epi-Si or the c-Si. The line scan showing HAADF normalized intensity (with respect to the wafer), perpendicular to the interface and averaged laterally on 5nm, is shown in the inset. The huge drop in intensity (and thus density) is confirmed by this technique. The interface itself is globally darker but has some contrast and thickness inhomogeneities. In any case this is a strong proof of the low density of the interface; this low density is most likely linked to the presence of H-platelets (see Fig.3.14) and also to the presence of residual surface oxide from imperfect surface cleaning. This comparison of high resolution STEM bright field and HAADF images of the interface for the two sample which differ by their ability to be lifted-off is a strong proof that a low density interface is a key point to enable lift-off of PECVD epi-Si layers. For those two samples, an HF-dipping was used to clean wafer's native oxide before loading into the reactor. However they were deposited in two different reactors:

- The sample with a nearly perfect interface (Fig.4.22) has been deposited in the new PECVD cluster tool, a reactor bought by Total Company and shared with LPICM-CNRS. It is equipped with a load-lock, thus the sample is loaded in the deposition chamber, kept at 200°C, within a minute and roughly ten minutes are needed to reach a base pressure in the range of 5.10^{-7}mb.

- The sample with the weak interface (Fig.4.23) and easy to lift-off was deposited after the same chemical cleaning of the surface, but in the old home built Arcam reactor[35]. This reactor does not have a load lock, and thus the pumping time to reach the same base vacuum is ∼4-5 times longer.

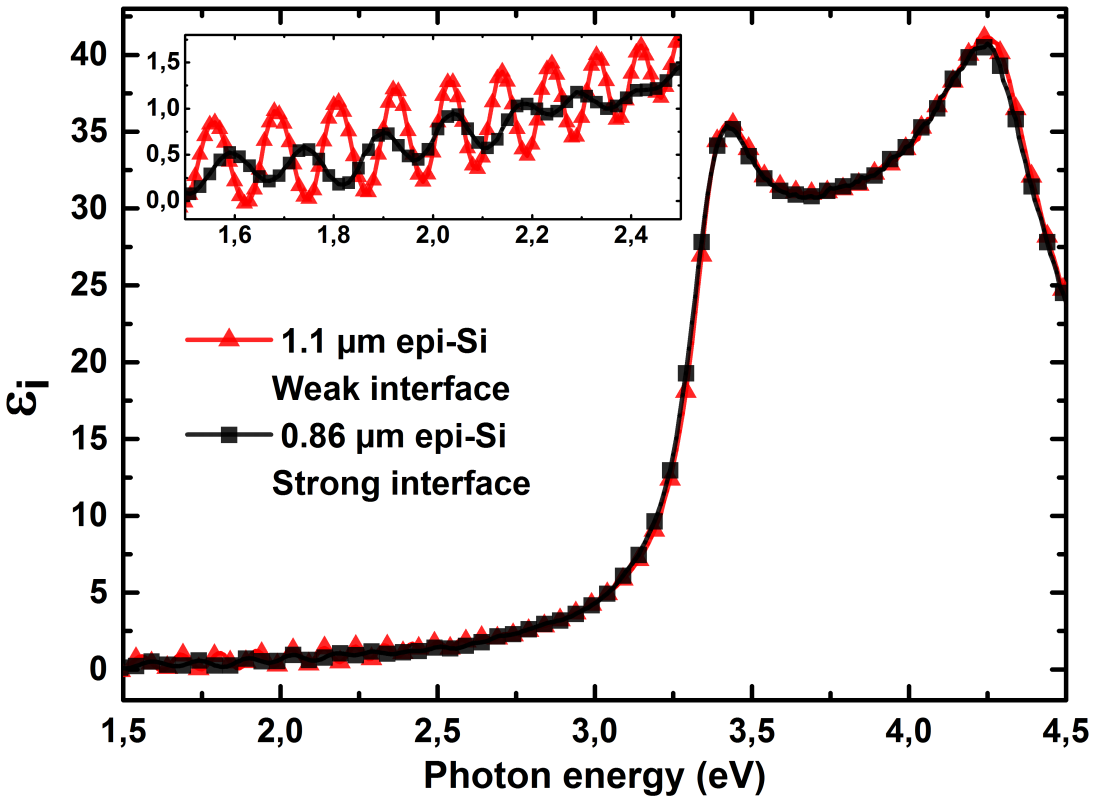


Fig. 4.24 – Ellipsometry spectra for the two samples shown in Fig.4.22 and Fig.4.23: epi-Si with strong (squares) and weak (triangles) wafer interfaces.

[35] P. Roca i Cabarrocas., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, **9**: 2331, 1991.

Thus the quality of the vacuum and the pumping rate are linked to the quality of the interface between epi-Si and wafer. Looking at the ellispometry spectra (see Fig.4.24) of the two samples (that have similar thicknesses) shown in Fig.4.22 and Fig.4.23, we see that the difference in epi-Si/wafer interface density is also detected with this technique: the sample with low interface density (triangles) has a higher amplitude of ε_i oscillations in the 1.5-3 eV range. By fitting these spectra, we find a 5.2nm interface thickness composed of 9% void and 91% c-Si for the low density sample and 2.3nm with 6% void for the other sample.

The same HAADF analysis has been performed on 5 epi-Si/c-Si samples which differ by their cleaning prior epitaxy, deposition reactor and consequently by their ability to be lifted-off. Their deposition conditions and the HAADF intensity contrast of the interface or bulk epi-Si area with respect to the substrate, $(I_{area} - I_{ref})/I_{ref}$, are reported in Fig.4.25.

Epi-Si Sample		A	B	C	D	E
PECVD reactor	Arcam	√	√	√		
	Cluster				√	√
Wafer cleaning	Wet: HF	√	√	√	√	
	Dry: SiF_4					√
Lift-off with 300-400°C annealing			√	√		

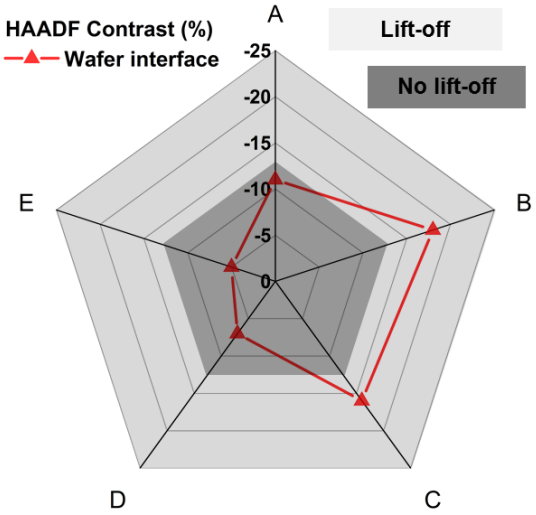


Fig. 4.25 – Left: 5 samples analyzed by STEM-HAADF; they differ by their cleaning prior epitaxy, deposition reactor and consequently by their ability to be lifted-off. Sample D is shown in Fig.4.22 and sample B in 4.23. Right: interface HAADF intensity contrast with respect to c-Si substrate for the 5 samples.

One can see that only two samples (B and C) deposited in the old reactor with a long pumping time can be easily lifted-off. These two samples were cleaned by HF-dipping prior epitaxial growth. The averaged interface HAADF contrast is reported in Fig.4.25 diagram on the right side: they both have a drop of contrast at the interface, and thus a drop of density, of 15-20%; the three other samples which does not lift-off have a lower density drop at the interface, typically 5-10%. Thus two areas are defined on the graph: - the area corresponding to a strong interface which do not break upon annealing, with HAADF contrast $\leq$ 15% (dark grey shade) and - the area corresponding to weak interface, which enables easy lift-off with moderate annealing, with HAADF contrast $\geq$ 15% (light grey shade). Considering the epi-Si contrast with respect to the c-Si wafer, the difference is less important, $\pm$ few percent around zero, and there is no clear trend between the samples.

To conclude, we have shown that the presence of a low density interface is a key point to perform PECVD epi-Si lift-off. This weak interface is most likely composed of H-platelets and some remaining silicon oxide, as confirmed by SIMS and TEM (see previous chapter). But a more reproducible process to form this type of weak interface still needs to be found. Moreno et al.[104], with H_2/Ar/SiH_4 plasma chemistry, could control this interface in-situ. In SiH_4/H_2 epitaxial plasma, in-situ cleaning with SiF_4 followed by H_2 plasma prior epitaxy was effective to tune the stress in the epi-layer (see Fig.3.16) but did not help to lift-off the layer. Thus if stress can help to enable the layer detachment, this is probably not enough (or at least this level of stress is not enough): a weak/porous H-rich interface is needed, and it should be preferentially created by interface plasma treatment. In any case, this

approach, a sort of low cost SmartCut process, is very promising and has already been patented at LPICM[109].

Large areas lift-off

Using epi-Si samples with a weak/porous interface, alternative lift-off processes were tested to improve reproducibility and handling compared to the home-made methods shown in Fig.4.20: i) lift-off with a polymer buffer on glass and ii) anodic bonding to glass substrate. The first approach is the one developed at LPN-CNRS within the frame of the ANR Nathisol project: the idea is to use a polymer layer to glue the epi-Si on a glass substrate and then perform annealing to obtain a flat epi-Si layer on polymer/glass. The polymer, typically PDMS or OrmoStamp, can stand the short annealing time required for the lift-off; the difference in thermal expansion upon annealing creates some stress which may contribute to detach the layer. A picture of a 2.5μm thick and 1×2 cm^2 epi-Si transferred with this process on glass and OrmoStamp is shown in Fig.4.26-a). The corresponding Raman spectrum (Fig.4.26-b)) shows a sharp crystalline peak with a FWHM of 5.4 cm^{-1}, which testifies that the excellent epitaxial crystal quality is preserved with this transfer technique. In addition, the AFM scans (see Fig.4.26-c)) of the substrate after lift-off and of the layer surface transferred on OrmoStamp/glass reveal a relatively low RMS roughness of 0.9nm on the two surfaces. This is a proof that the epi-Si/c-Si interface acts as a sharp cleavage plane. The ellipsometry measurement on the epi-Si layer before and after transfer are displayed in Fig.4.26d). At low energy, the small amplitude of ε_i oscillations for the of epi-Si/c-Si sample (triangles) is characteristic of the wafer interface. After lift-off, the oscillations amplitude is significantly increased, due to the Fabry-Perot effect of light traveling back and forth in the epi-Si layer. By fitting, the exact same thickness is found before and after detachment, thus confirming that the epi-Si/c-Si interface is a sharp cleavage plane. However, the difference in ε_i amplitude at 4.2eV, roughly 42 before and 35 after, indicates a low crystalline quality for the first few nanometers of the surface (which was the epi-Si/c-Si interface before lift-off). This can be due to alteration of crystal quality due to lift-off and transfer. But let us remind that, as shown in the previous chapter, the epitaxial quality is improving with thickness, and that layers close to the wafer interface are more defective. Thus the lower crystal quality for the epi-Si surface after transfer can also be understood because this new upper surface corresponds to the first nanometers of epitaxial growth before lift-off.

[109] P. Roca i Cabarrocas et al. "Method for producing a multilayer film including at least one ultrathin layer of crystalline silicon, and devices obtained by means of said method" pat. US20120208358 A1

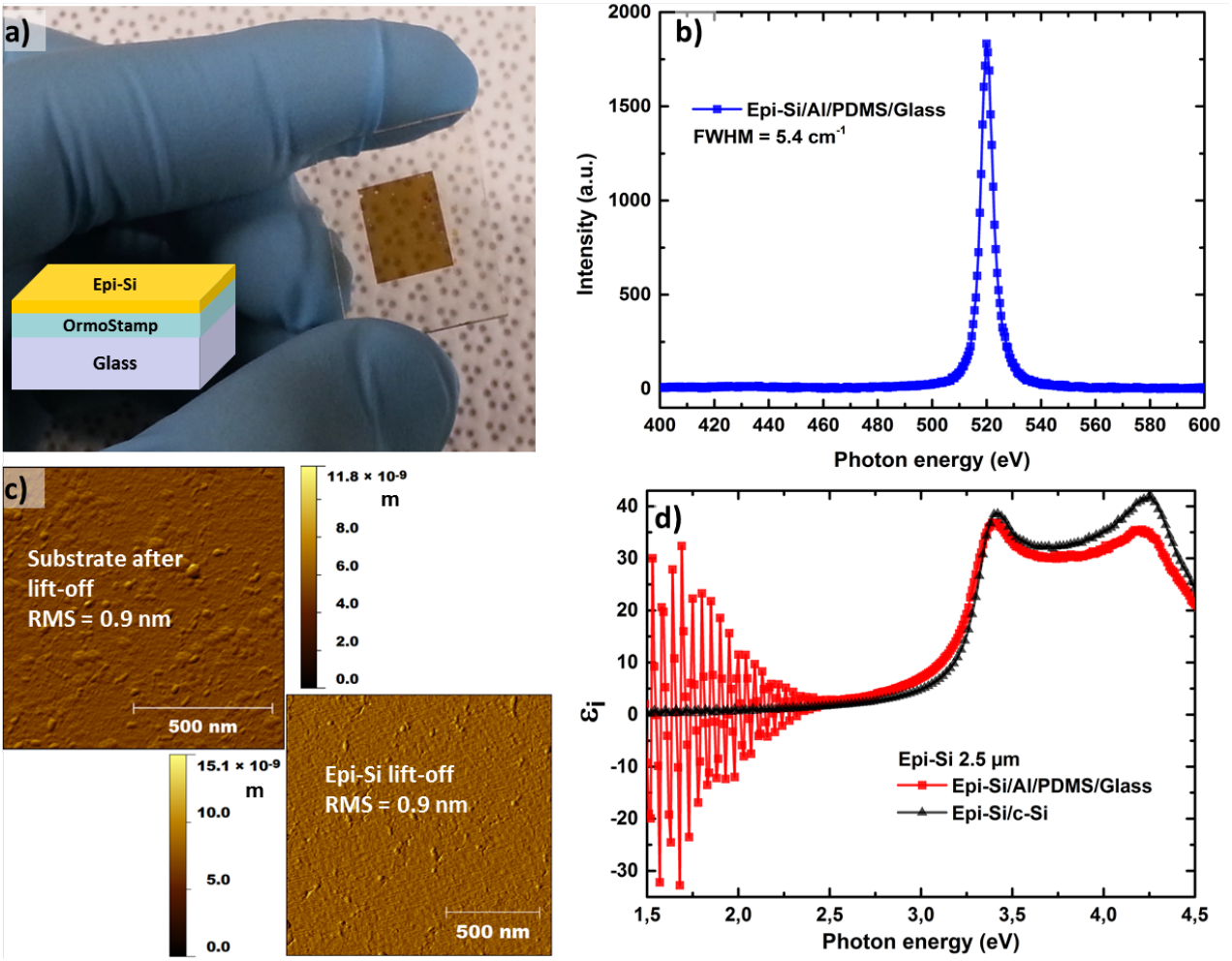


Fig. 4.26 – a) Transferred 2.5μm thick epi-Si on glass with an Ormostamp buffer layer. b) Raman spectrum of the epi-Si on glass having a FWHM of 5.4 cm^{-1}. c) AFM scan of the substrate after lift-off and of the layer on glass: both have a 0.9nm RMS roughness. d) Ellipsometry spectrum of the same layer on wafer and after being transferred onto glass substrate.

The second approach to transfer large area PECVD epi-Si layers is the anodic bonding[110,111]. This technique, performed at IMEC within the EU-FP7 project PhotoNVoltaics, is a well-known process used to create covalent bonds between a silicon and a borosilicate glass substrate containing a high density of alkali ions. In anodic bonding, the wafer is placed between the chuck and the top tool used as bond electrode, at temperatures between 200 and 500°C (below glass transition temperature). A typical applied voltage of 1kV is used between the chuck and the top electrode to cause a diffusion of glass sodium ions (Na^+) out of the bond interface toward the backside of the glass (cathode). With this depletion of Na^+ ions, the volume at the bonding surface becomes negatively charged because of the remaining oxygen ions (O^{2-}). This produces a positive volume charge in the silicon wafer on the opposite side of the bonding. As a result, a few micrometer thick high-impedance depletion region is developed at the bond barrier in the glass wafer. The electrical field intensity in the depletion region is so high that the oxygen ions drift to the bond interface and pass out to react with the silicon to form a SiO_2 layer. Simultaneously, a pressure is applied to create intimate contact between the surfaces and ensure good electrical conduction across the wafer pair. The thin oxide layer formed between the bond surfaces, ensures an irreversible connection between the glass and the wafer.

[110] T.M.H. Lee et al., Sensors and Actuators A: Physical, **86**: 103–107, 2000.
[111] J. Wei et al., Journal of Micromechanics and Microengineering, **13**: 217, 2003.

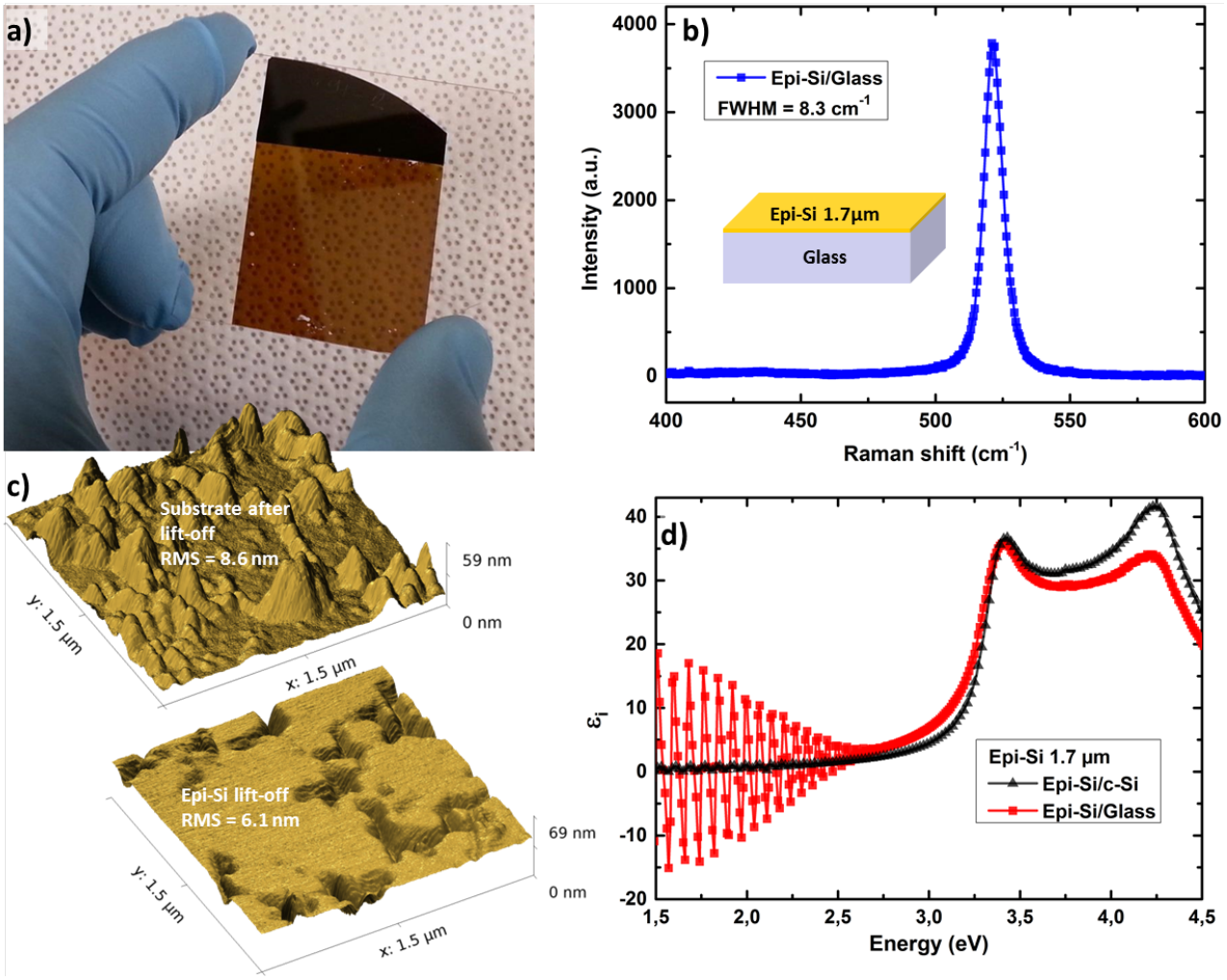


Fig. 4.27 – a) Transferred 1.7μm thick epi-Si bonded to glass substrate. b) Raman spectrum of the epi-Si on glass having a FWHM of 8.3 cm^{-1}. c) AFM scan of the substrate and epi-layer after lift-off and of the layer on glass: their RMS roughness is respectively 8.6 and 6.1nm. d) Ellipsometry spectrum of the same layer on wafer and on glass substrate.

A 1.7μm thick and $\sim$ 10cm^2 epi-Si layer bonded to MEMPax Schott glass (at 400°C and 1kV, with a EVG 520 machine) is shown in Fig.4.27-a). Few small areas where the bonding failed are visible on the bottom side of the sample, but overall the homogeneity is excellent, especially given that no polishing surface treatment was used (just a standard cleaning: piranha 10 min + HF/HCl dip 2 min), and that the bonding conditions were not optimized. The Raman peak of the epi-Si on glass (Fig.4.27-b)) has a FWHM of 8.3cm^{-1}. This is higher compared to the polymer buffer assisted transfer shown in Fig.4.26. Looking at AFM scan, we found a 8.6nm RMS roughness for the substrate surface after lift-off, and 6.1nm for the epi-Si bonded to glass. Moreover, from the surface topography displayed in Fig.4.27-c), hills shaped and valley shaped (few tens of nm height) surfaces are found for the substrate and the layer respectively. Several tests are needed to understand whether this shape is anecdotal or related to some aspect of the anodic bonding process. The imaginary part of the pseudo-dielectric function ε_i of the layer before and after lift-off is shown in Fig.4.27-d). The interpretation we can make from those curves is similar to the one aforesaid for the Fig.4.26-d). Thickness fringes at low energy have the same period, thus confirming that the full layer is transferred, and the higher amplitude is linked to the high index contrast between Si and glass on the back side. Once again the ε_i 4.2eV peak amplitude is reduced from $\sim$42 to $\sim$35, probably due to the exposure of what was the first nanometers of the epitaxial growth.

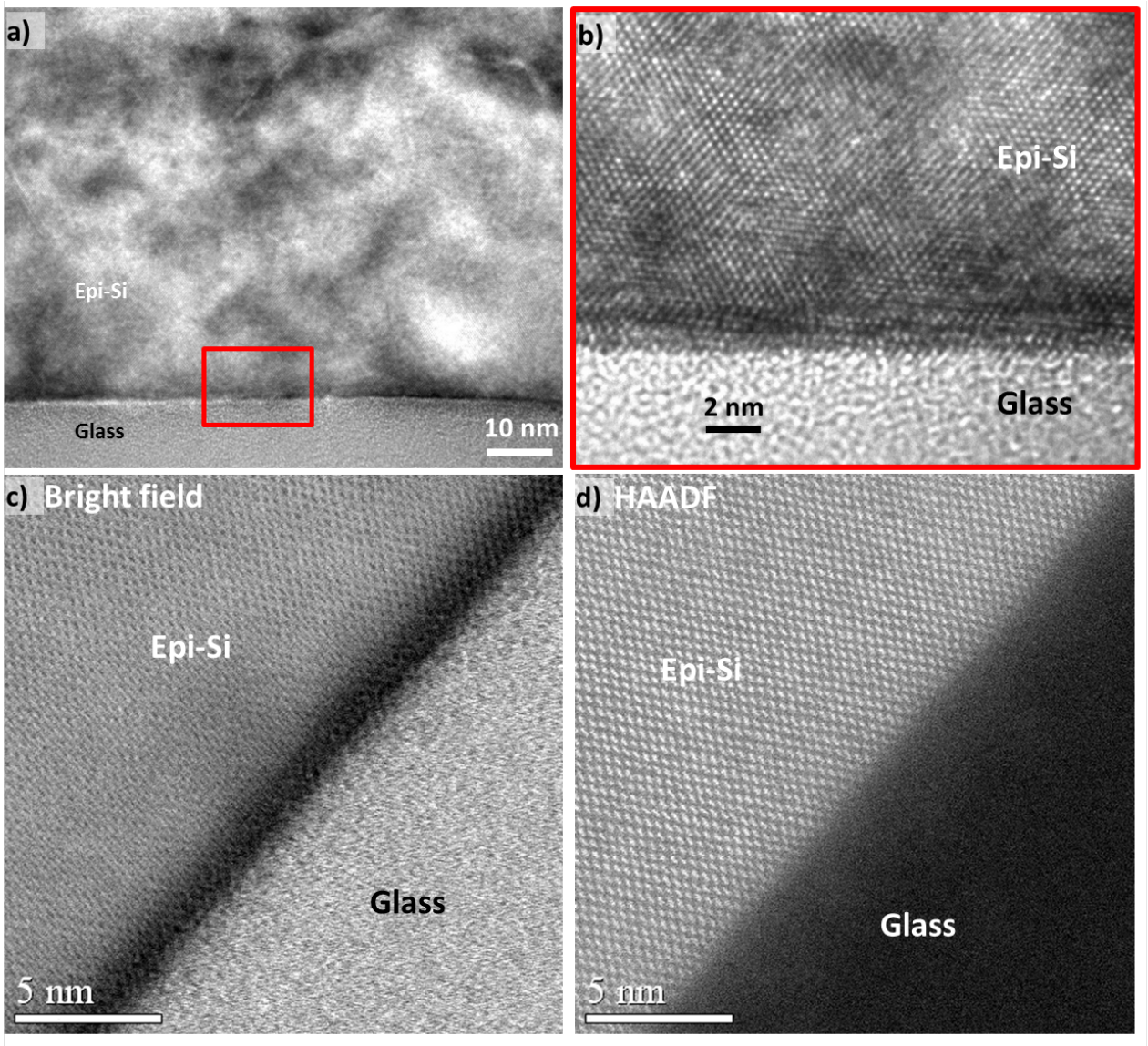


Fig. 4.28 – a) Bright field TEM cross section along <110> axis of epi-Si/glass interface with b) a high resolution zoom on the interface. c) High resolution STEM bright field and d) HAADF of the same sample.

From the AFM and Raman analysis it appears that the bonding process is more damaging the material compared to the polymer buffer approach. However this should be considered as preliminary results and clearly more work is required to evaluate how the electrical properties (e.g lifetime) are altered with the transfer process.

Cross section TEM and SEM high resolution images of the bonding interface, acquired at LPICM-CNRS and LPN-CNRS, are shown in Fig.4.28. a) and b) show a medium magnification and high resolution zoom of the interface. Some defects such as stacking faults are visible, but the epi-Si adhesion and conformality with the glass interface is excellent. Similarly, the bright field c) and HAADF STEM d) images show an excellent crystal quality for the transferred epi-Si and a sharp transition with the glass substrate.

Finally, the need for superior light trapping in thin film c-Si layers of few microns is illustrated in Fig.4.29. On this picture, Palaiseau's romantic sunset is seen through a 1.5 μm thick PECVD epi-Si layer grown at 175°C and bonded to glass substrate. The short wavelengths of the sun light are absorbed and thus the sample appears yellowish. Of course there is no back reflector in this sample, but this gives a visual confirmation that if high efficiency is targeted with such a thickness, huge

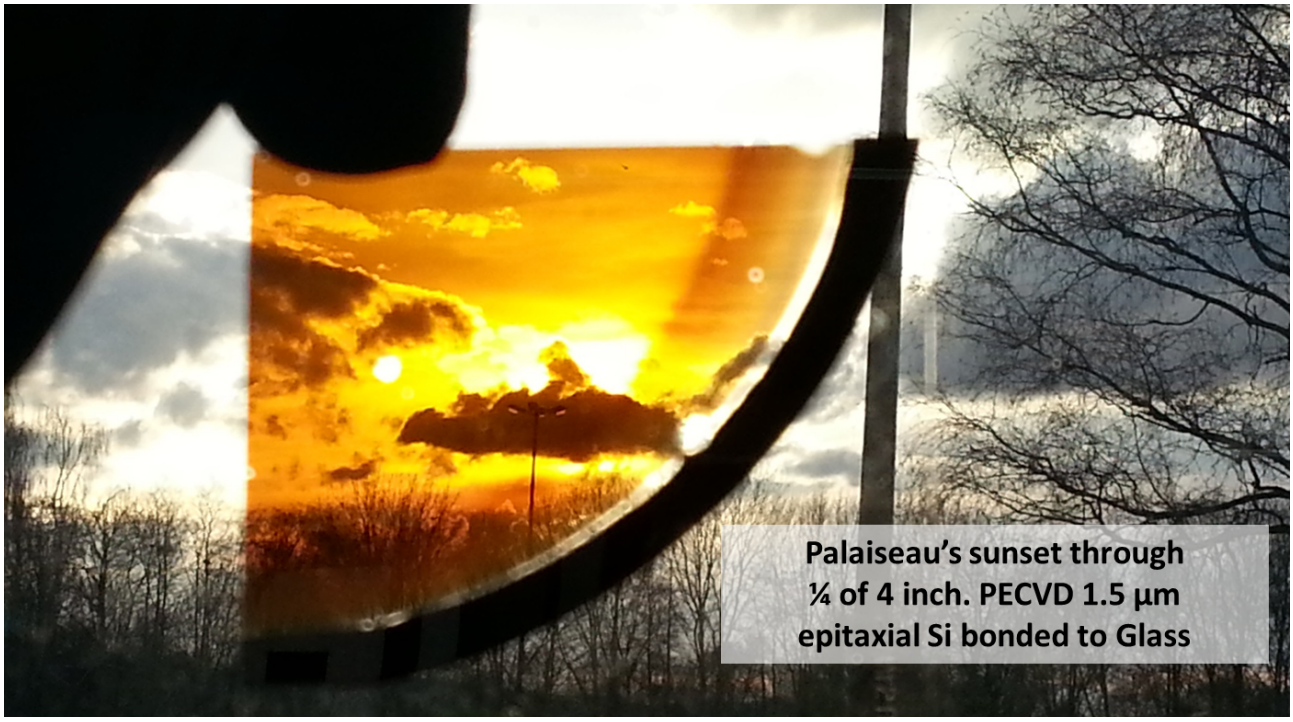


Fig. 4.29 – Experimental proof of transmission losses in 1.5 μm thick epitaxial silicon bonded to glass substrate.

trapping effect for the long wavelength are required. Alternatively, some semi-transparent photovoltaic applications could be considered; and in any case, a lot of different fields (microelectronics, etc.) could benefit from this low cost epi-Si transfer process.

4.4.4 Transferred PECVD epi-Si cells

During the early stage of Nathisol and PhotoNVoltaic projects, a significant part of the work on PECVD was focusing on testing and improving the lift-off processes. Now, at the time of the writing of this manuscript, the first PECVD lifted-off solar cells start to be functional. Those preliminary cell results are briefly presented here.

Several cell architectures and process flow are explored in the two projects. One possibility is shown in Fig.4.30: this is a transferred PECVD epi-Si cell including plasmonic mirror on the back side and inverted nanopyramids on the front side. For this architecture, the transfer process can be either with a polymer buffer or by anodic bonding. Starting from an intrinsic epitaxial layer, the epitaxial growth would end with a doped area used in the final device as a back surface field. The back side light trapping features (plasmonic mirror) can be deposited before lift-off and the front side nanopatterning would be performed after lift-off.

However such an optimized device has not been produced yet: much simpler stacks were tested first. One example of a lifted-off and transferred cell is shown in Fig.4.31. The stack is simply composed of glass/PDMS/Al/epi-Si(2.5μm)/(i)-(n)a-Si:H/ITO/Al, thus there is no p-doped layers. It is not excluded that some diffusion of Al happens during the lift-off annealing step, thus creating a p-type doping on the back Si side. The transfer is done with a PDMS buffer, and the access to the Al back contact is done by etching the epi-Si layer down to the Al by RIE (SF_6/O_2), the ITO circular plot being used as a mask. The resulting 0.03 cm^2 cell was measured under dark conditions, and the semi-log I-V characteristic is plotted in Fig.4.31-b). The diode behavior is clearly visible, but it corresponds to a high J_o and ideality factor. Unfortunately the measurement under AM1.5G could not be done for this sample: repeated dark I-V measurement with inappropriate contacting tips size

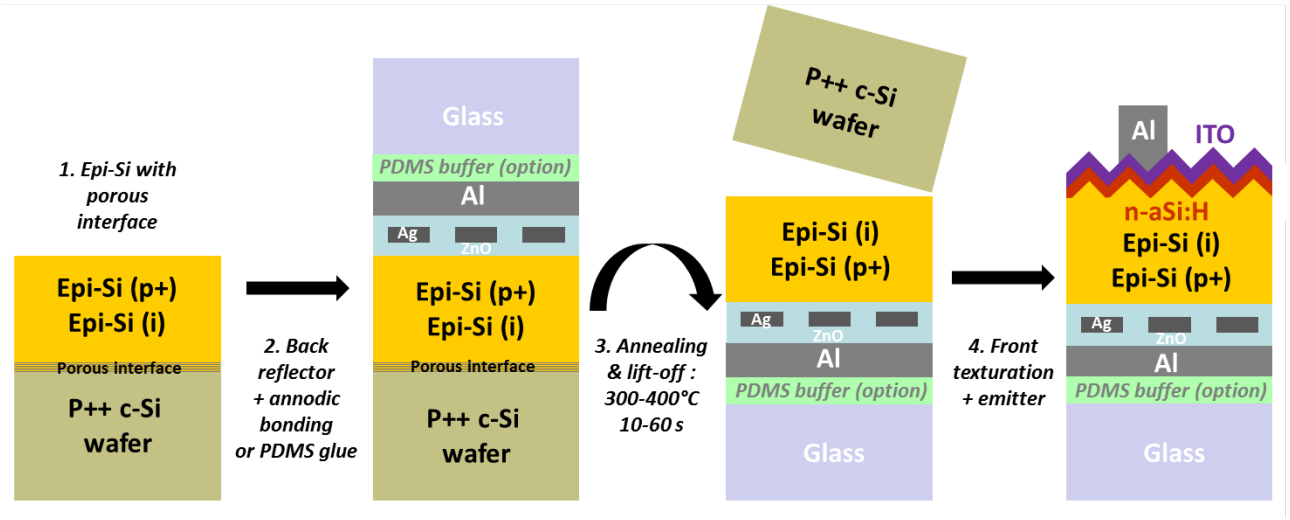


Fig. 4.30 – Diagram of a possible fabrication process for a lift-off PECVD epitaxial solar cell with plasmonic and photonic light trapping features .

resulted in macroscopic holes and cracks destroying the cell.

Fig.4.32-a) shows the top view picture, the diagram of the layer stack and cross section SEM picture of a PECVD epi-Si bonded to glass substrate. The circular blue spots on the picture are ITO and the grey color around is the Al back contact. The access to the back contact is also achieved here by RIE using ITO as a protecting mask. For this sample, a (n)μc-SiO$_x$ was deposited on top of the epi-Si, and is thus in contact with the Al on the back side after lift-off. The front side of the device is composed of (p)a-Si:H and ITO. The layers are visible on the cross section SEM picture. This device was tested under solar simulator and with EQE measurements; the results are shown in Fig.4.32-b). Parasitic resistances are visible on the J-V curve and this results in a poor fill factor of 56%. The V_{oc}, reaching only 342mV, indicates a poor material quality. Indeed the effect of anodic bonding on epi-Si bulk or passivation properties is still unknown. However the device shows a current of 19.9mA/cm^2, which is promising given that this current is created in 4μm epi-Si only. Compared to the solar cells shown in Fig.4.6, here there is no parasitic contribution of the wafer to the current. There is a small

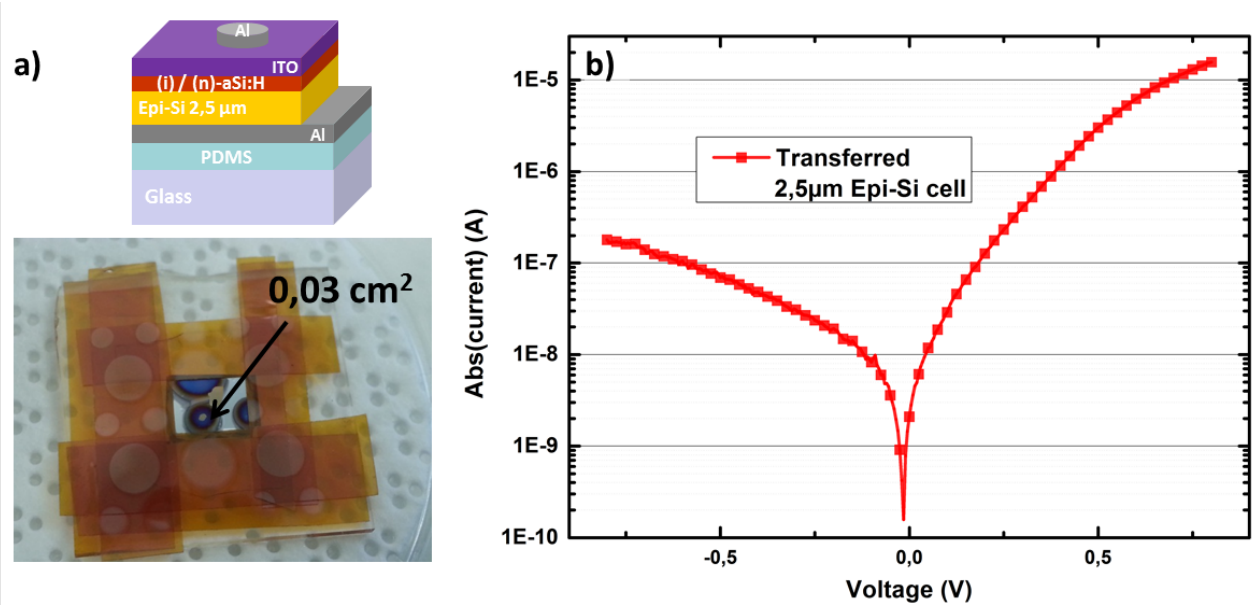
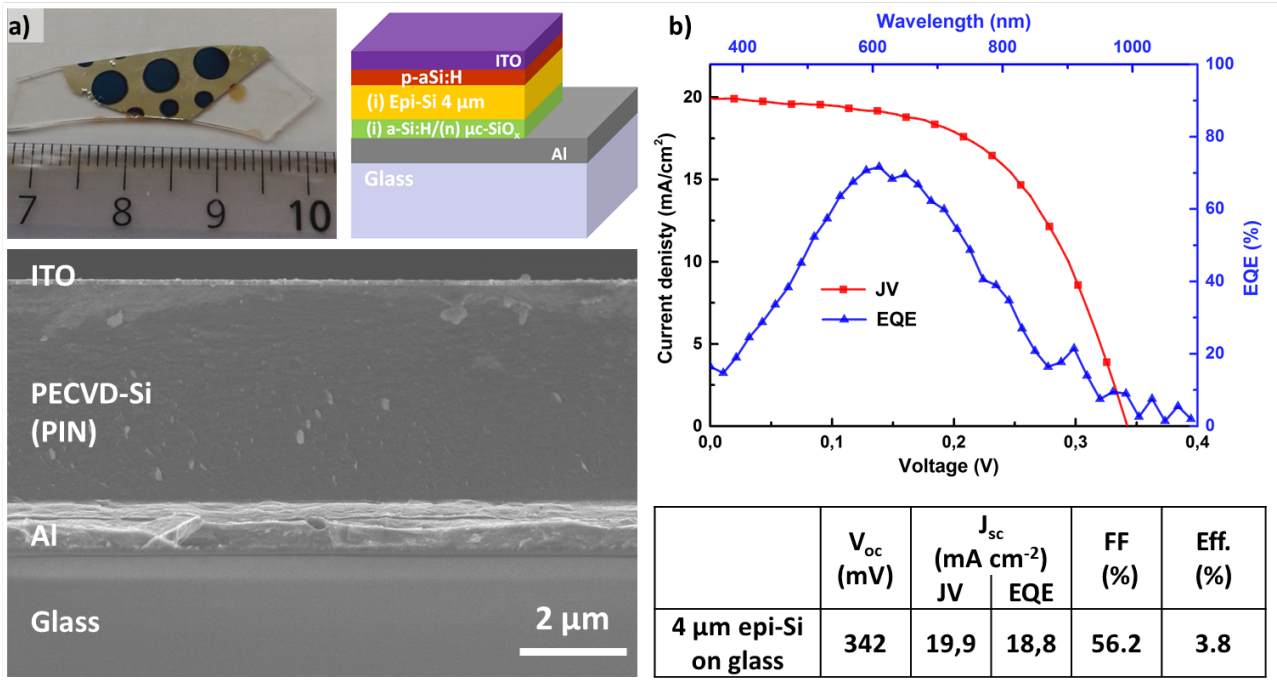


Fig. 4.31 – a) Diagram of the layer stack and top view picture of a 2.5 μm thick PECVD epi-Si cell transferred on glass/PDMS substrate. b) Corresponding dark I-V characteristic.

1mA/cm^2 discrepancy between the current density calculated by EQE and I-V. But our EQE set-up is probing only a local area, whereas the I-V is collecting current from the whole cell surface. The efficiency of this first PECVD device reaches 3.8%.



	V_{oc} (mV)	J_{sc} (mA cm^{-2}) JV	J_{sc} (mA cm^{-2}) EQE	FF (%)	Eff. (%)
4 µm epi-Si on glass	342	19,9	18,8	56.2	3.8

Fig. 4.32 – a) Top view picture, diagram of the layer stack and SEM cross section image of a 4μm PECVD epi-Si cell bonded to glass substrate. b) J-V curve and EQE of the solar cell device, with corresponding parameters listed in the table.

4.5 From silicon to germanium

Germanium and silicon-germanium alloys were also studied during this thesis. This family of materials is indeed very attractive: i) germanium has a very strong absorption in the long wavelength range and a high carrier mobility ii) Ge is also almost lattice matched to some III-V semiconductors such as GaAs iii) SiGe has a tunable band gap with composition and stress, and thus can be used as a bottom cell in multijunctions, etc. Indeed, the efficiency of a solar cell, beyond the technological limits, is based on how much light it can absorb. This is why industry and researchers have been looking for multi-junction solar cells made up of materials with different band gap energies. Ge and its alloys with silicon is a good candidate: i) in the field of thin film amorphous and nanocrystalline solar cells, the record power conversion efficiency of 16.3% (initial) is hold by a triple junction which includes an amorphous SiGe cell[8]. ii) In the field of III-V multijunctions for space and terrestrial concentration PV, the record triple junction cell with above 40% efficiency was based on GaInP/GaAs/Ge in past years[112]. The epitaxial growth of Ge below 200°C by PECVD has already been demonstrated in LPICM-CNRS with the work of Johnson et al.[113] (Ge on GaAs) and with Labrune et al.[114] (Si/Ge multilayers on GaAs). Thus, in this section, we present our results on LTE PECVD epitaxial growth of Ge and SiGe and the use of this materials in solar cell devices.

[8] B. Yan et al., Applied Physics Letters, **99**: 113512–113512–3, 2011.
[112] W. Guter et al., Applied Physics Letters, **94**: 223504, 2009.
[113] E.V. Johnson et al., Applied Physics Letters, **92**: 103108, 2008.
[114] M. Labrune et al., EPJ Photovoltaics, **3**: 30303, 2012.

4.5.1 Low temperature PECVD epitaxial growth of Ge

Germanium based electronic devices became an active research topic since the first transistor realization[115], which opened the path to microelectronics. However, silicon quickly flooded the semiconductor research and industry due to lower cost, abundance, and its oxide providing excellent surface passivation. However, more recently, germanium based electronic devices have gained a renewed interest since silicon device scaling down is rapidly approaching its limit. Due to its higher carrier mobility with respect to Si, Ge has been proposed as a possible candidate for the next generation of high mobility channel devices. From an optical perspective, Ge benefits from high refraction index, a strong absorption coefficient, and a minimal optical dispersion, which are useful for lenses and optical elements for infrared imaging.

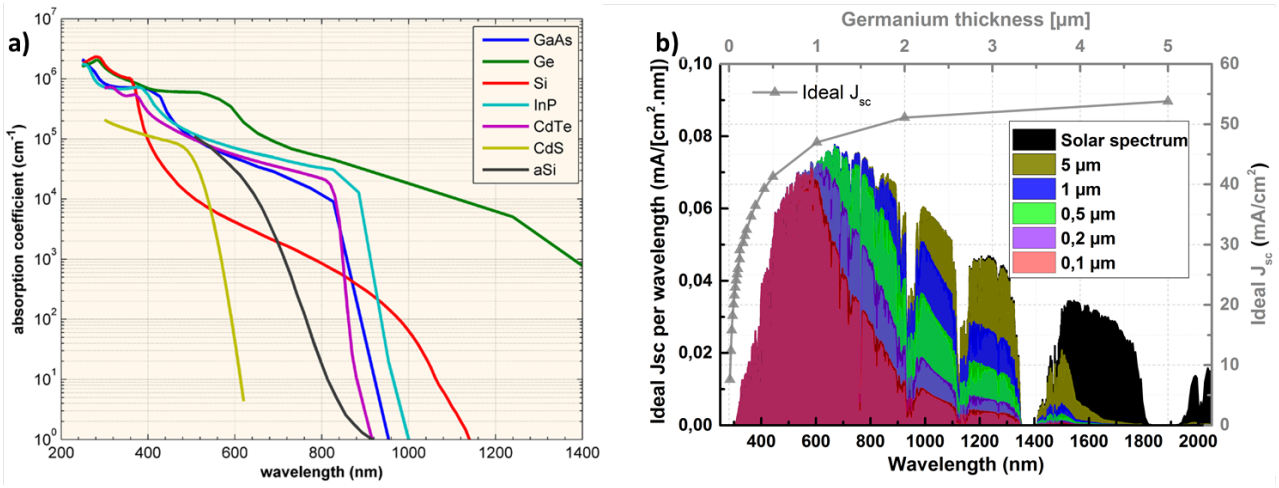


Fig. 4.33 – a) Absorption coefficients of various semiconductors; Ge has the strongest absorption for middle and long wavelength range (from pveducation.org). b) Ideal current density per wavelength for AM1.5G solar spectrum (bottom & left axis, dark shade). Single pass absorption of c-Ge slab with 0.1, 0.2, 0.5, 1 and 5μm thicknesses are shaded in colors. By integration, the ideal $\boldsymbol{J_{sc}}$ (R=0 and EQE=1) is calculated for a single path (top & right axis, triangles), as a function of Ge thickness.

The absorption coefficient of germanium is high from the middle to long wavelength range in comparison with many other semiconductors, as shown in Fig.4.33-a). Using this absorption coefficient and the AM1.5G solar spectrum, one can calculate the ideal $\boldsymbol{J_{sc}}$ per wavelength (assuming single light path, no reflection, and EQE=1) for various Ge thicknesses. This quantity is displayed in Fig.4.33-b), bottom and left axis, where fraction of the solar spectrum converted into electricity by various Ge thicknesses (0.1, 0.2, 0.5, 1 and 5μm) are shaded in colors. The $\boldsymbol{J_{sc}}$ as a function of Ge thickness (top and right axis, triangles), calculated by integration with the solar spectrum, is plotted on the same graph. The strong absorption of Ge results in a high $\boldsymbol{J_{sc}}$: roughly 45 mA.cm^{-2} can be obtained in 1 μm c-Ge, as compared to 12.5 mA.cm^{2} in a c-Si slab of the same thickness. Of course, we should keep in mind that efficiency is driven by the product of $\boldsymbol{J_{sc}}$ and $\boldsymbol{V_{oc}}$; the low band gap of Ge (0.66 eV) and thus the $\boldsymbol{V_{oc}}$ of Ge cell is indeed less optimum compared to silicon, for a single junction configuration. The record efficiency for a single junction with a germanium absorber is around 8%[116].

An improvement in germanium processing, passivation and growth, can impact many different fields: opto-electronics, large area electronics, fiber optics and photovoltaics. In this latter field, as mentioned previously, germanium is widely used as a bottom cell in record triple junction devices[112] thanks to its strong absorption coefficient together with high mobility and a band gap of 0.66 eV. More-

[115] J. Bardeen et al., Physical Review, **74**: 230–231, 1948.
[116] N.E. Posthuma et al., IEEE Transactions on Electron Devices, **54**: 1210–1215, 2007.

over, its lattice constant is closely matched to III-V materials (Ge∼5.657nm and GaAs∼5.653nm). However germanium is a scarce and thus expensive material. Driven by the industrial request of cost reduction, research is thus moving attention towards new techniques to obtain attractive semiconductor materials on low cost substrates. The main ways to meet this target are crystallization of amorphous materials by novel techniques preserving the substrate[117–120] or deposition of epitaxial layers, eventually combined with lift-off processes for transfer on a flexible support.

Within this context, the growth of high quality germanium with a smooth surface epi-layer on Si is a crucial step for III-V materials integration with the existing silicon process technology. It has been a hot research topic for many years[121–124]. The main problem arises from the 4.2% lattice mismatch (at 300K) between Ge and Si which ends up with misfit dislocations and other defects (e.g. twins). Indeed, using buffer layers and specific growth processes, high quality c-Ge can be epitaxially grown on Si using several growth steps involving temperatures above 600°C[123,125]. However, low temperature deposition is useful for many applications; among the benefits of low temperature epitaxy we would like to emphasize: i) the absence of thermal strain induced by differences in thermal expansion coefficients; ii) having a hydrogen terminated surface (less reactive), which is a key for low impurity incorporation in non UHV systems; and iii) significant cost reduction thanks to well established low temperature plasma CVD reactors. Thus we present here our results on thin film epitaxial germanium (epi-Ge) grown by standard RF-PECVD below 200°C, on c-Ge and c-Si substrates. This deposition technique has been widely used for decades to produce amorphous and micro-crystalline materials, but the plasma conditions promoting epitaxial growth of Ge at such low temperature is a much more recent result[113,114]. Compared to high temperature CVD epitaxial growth or ultra-high vacuum MBE technique, this approach targets lower cost. This work done at LPICM-CNRS received great help from S. Almosni, R. Ruggeri and J. Nassar.

Focus on c-Ge surface

Since the depositions were done at low temperature, an appropriate surface cleaning method was required to remove native oxide before epitaxial growth. In the case of c-Si surface, the HF-dipping and in-situ SiF_4 plasma cleaning are efficient techniques (see section "Surface cleaning prior to epitaxial growth" in the previous chapter). For c-Ge few processes have been tested, and the result are presented in Fig.4.34.

The surface in Fig.4.34-a) corresponds to ε_i measured in-situ by ellipsometry (on Philix reactor) of a c-Ge wafer exposed to a pure SiF_4 plasma. The measurement is done in the energy range 3.4-4.4 eV, and the plasma ignition corresponds to the zero time. Since high energy photons are probing the surface (e.g. 4.1 eV corresponds to a ∼6nm of penetration depth in c-Ge), this spectral region is sensitive to surface changes such as oxide cleaning. Indeed the presence of germanium native oxide reduces the amplitude of ε_i in 3.4-4.4 eV. The conditions used here were 30 mTorr of pure SiF_4 and 5W; this resulted in a V_{dc} of -110V. The huge increase of ε_i from a peak amplitude of ∼24 before to a value of ∼26.5 after the SiF_4 plasma is the proof of Ge oxide removal. This result suggests that, like in the case of c-Si surface cleaning, a SiF_4 plasma is efficient to etch away the native oxide. Alternative cleaning methods were also tested and the results are gathered in Fig.4.34-b). This graph represents ε_i in the 1.5-4.5 eV range measured ex-situ by ellipsometry for c-Ge wafers with various surface treatments. The black line represents the reference curve for c-Ge[37] at room temperature. The

[117] G. Mannino et al., Applied Physics Letters, **97**: 022107–022107–3, 2010.
[118] F. Vega et al., Journal of Applied Physics, **75**: 7287–7291, 1994.
[119] T. Sameshima et al., Thin Solid Films, **487**: 67–71, 2005.
[120] G. Fisicaro et al., Microelectronic Engineering, **88**: 488–491, 2011.
[121] M. Bosi et al., Progress in Crystal Growth and Characterization of Materials, **56**: 146–174, 2010.
[122] R. Ginige et al., Semiconductor Science and Technology, **21**: 775–780, 2006.
[123] J.M. Hartmann et al., Journal of Crystal Growth, **310**: 5287–5296, 2008.
[124] E.A. Fitzgerald et al., Journal of Vacuum Science & Technology B, **10**: 1807–1819, 1992.
[125] Y.H. Tan et al., Thin Solid Films, **520**: 2711–2716, 2012.
[37] D.E. Aspnes et al., Physical Review B, **27**: 985, 1983.

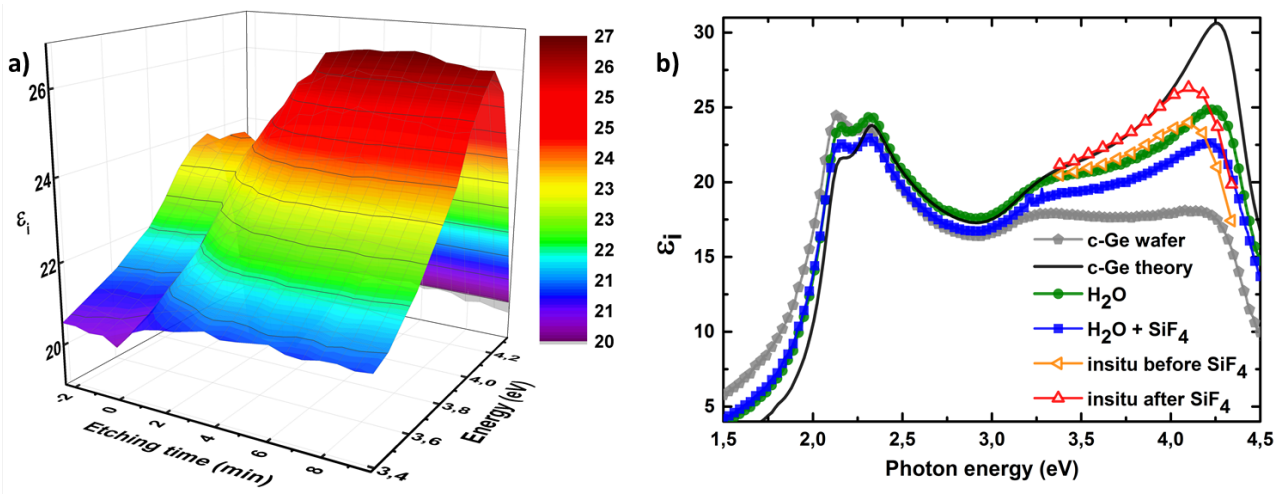


Fig. 4.34 – a) In-situ real time spectroscopic ellipsometry acquisition on a c-Ge wafer exposed to SiF_4 plasma showing ε_i time evolution in the 3.4-4.4 eV range. b) Comparison of c-Ge ε_i after various surface treatments to remove the native oxide.

orange and red triangles are the in-situ acquisitions at 175°C, extracted from Fig.4.34-a), measured before and after the plasma cleaning step. One can see the positive effect of SiF_4 with the curve getting closer to the theoretical value.

However, to be more quantitative, those in-situ curves should actually be compared to reference c-Ge spectrum at the same temperature (175°C). The grey curve (pentagons) is the measurement on c-Ge with its native oxide. The green curve (circles) corresponds to c-Ge after 15 min rinsing in DI water; the blue curve (squares) 15 min DI water with an additional 5 min SiF_4 plasma etching step. It appears that the simple DI water cleaning is relatively efficient removing c-Ge native oxide. In literature, it is acknowledged that both GeO and GeO_2 are present on Ge surface, the latter being soluble in water[126]. To further investigate the effect of DI water on c-Ge surface, cross section TEM has been performed. For the sample shown in Fig.4.35, after a 15 min DI water rinsing, the sample was loaded into a PECVD reactor to deposit a standard a-Si:H layer and thus protect the c-Ge surface. The bright field image presented in Fig.4.35-a) shows a sharp and epitaxial regrowth free transition between c-Ge and a-Si:H. No oxide is detected with this imaging technique.

Energy filtered TEM (EFTEM) mode has been performed to investigate more precisely the presence of oxide. With this technique it is possible to select only electrons of particular kinetic energies to form the image. If a very thin sample is illuminated with a beam of high-energy electrons, inelastic scattering when passing through the sample results in a loss of energy and a change in momentum, which in the case of inner shell ionization is characteristic of the chemical element. By using a magnetic prism and an adjustable slit, it is possible to collect only electrons which have lost a specific amount of energy. Thus by selecting the ionization edges of interest, EFTEM can produce elemental maps. Here we show in Fig.4.35-b) the cross section EFTEM image of the c-Ge surface obtained by selecting the oxygen ionization edge; the bright areas correspond to the presence of oxygen atoms. Oxygen is detected at the interface between a-Si:H and the glue, but much less signal is visible at the c-Ge/a-Si:H interface. From this result, we can conclude that DI water cleaning is probably effective when subsequent epitaxial growth is targeted; however this interface, given the simple cleaning process, would probably have poor electrical properties. In fact, the germanium oxide is not a good dielectric, and c-Ge surface is defective and hard to passivate[126].

[126]S. Rivillon et al., Applied Physics Letters, **87**: 253101, 2005.

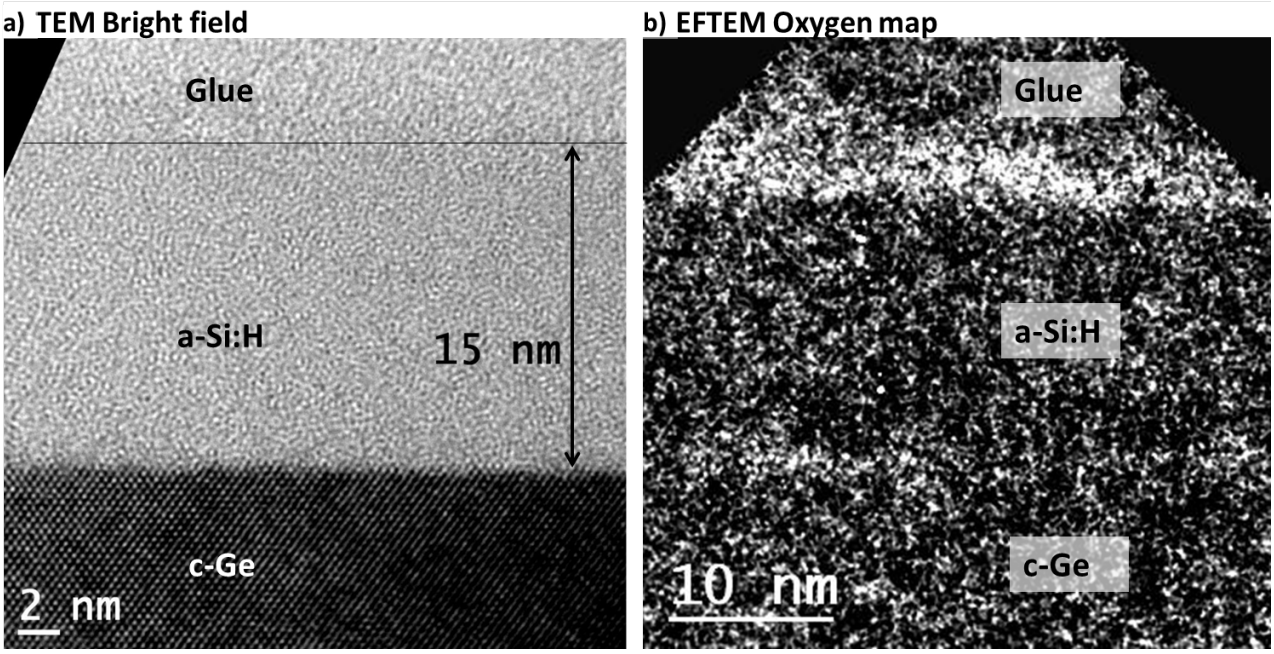


Fig. 4.35 – a) TEM cross section along <110> axis of c-Ge (100) wafer cleaned with DI water and passivated with 15nm of a-Si:H. b) EFTEM oxygen map of the same sample.

Epi-Ge on c-Ge and c-Si substrates

In the following study[127], germanium layers were deposited on both c-Ge and c-Si substrates, using the PECVD "ARCAM" reactor[35] at temperatures from 175 to 200°C. P-type Si (100) and Ge (100) substrates with resistivity below 10^{-2} Ω.cm were dipped in 5% HF and deionized water (18.3 MΩ.cm) respectively, for oxide removal. The substrates were then immediately loaded into the reactor, with no load-lock chamber, and pumped down to 10^{-7} mbar within 45 min. Reactive species are created from dissociation of a mixture of GeH_4 and H_2, with the deposition conditions listed in Tab.4.6.

	Temp. (°C)	Pressure (Torr)	GeH_4 (sccm)	H_2 (sccm)	Power (mW/cm^2)	Electrode gap (mm)
Intrinsic epi-Ge	175-200	1.9	5	200	50	17

Tab. 4.6 – Optimized deposition conditions for intrinsic germanium low temperature PECVD epitaxial growth.

The growth was performed at a rate of about 5 Å.min^{-1} and thicknesses up to 168 nm were deposited. a-Si:H layers were deposited on top of epitaxial layers, from a silane plasma under a total pressure of 0.13 mbar and RF power density of 6 mW.cm^{-2} (deposition rate 0.5 Å.s^{-1}). The epi-Ge films were simultaneously deposited on c-Ge wafers and c-Si wafers. The epitaxial Ge layers were first characterized by spectroscopic ellipsometry to determine compositions and thicknesses. The crystal quality, interface composition, defects and strain were analyzed by TEM, using a JEOL JEM 2010 F TEM microscope at an acceleration voltage of 200 kV, equipped with a Gatan electron energy loss image filtering for energy filtered EFTEM analysis. The defects density was also evaluated by the etch pit density technique[128].

[127] R. Cariou et al., AIP Advances, **4**: 077103, 2014.
[35] P. Roca i Cabarrocas., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, **9**: 2331, 1991.
[128] H.-C. Luan et al., Applied Physics Letters, **75**: 2909–2911, 1999.

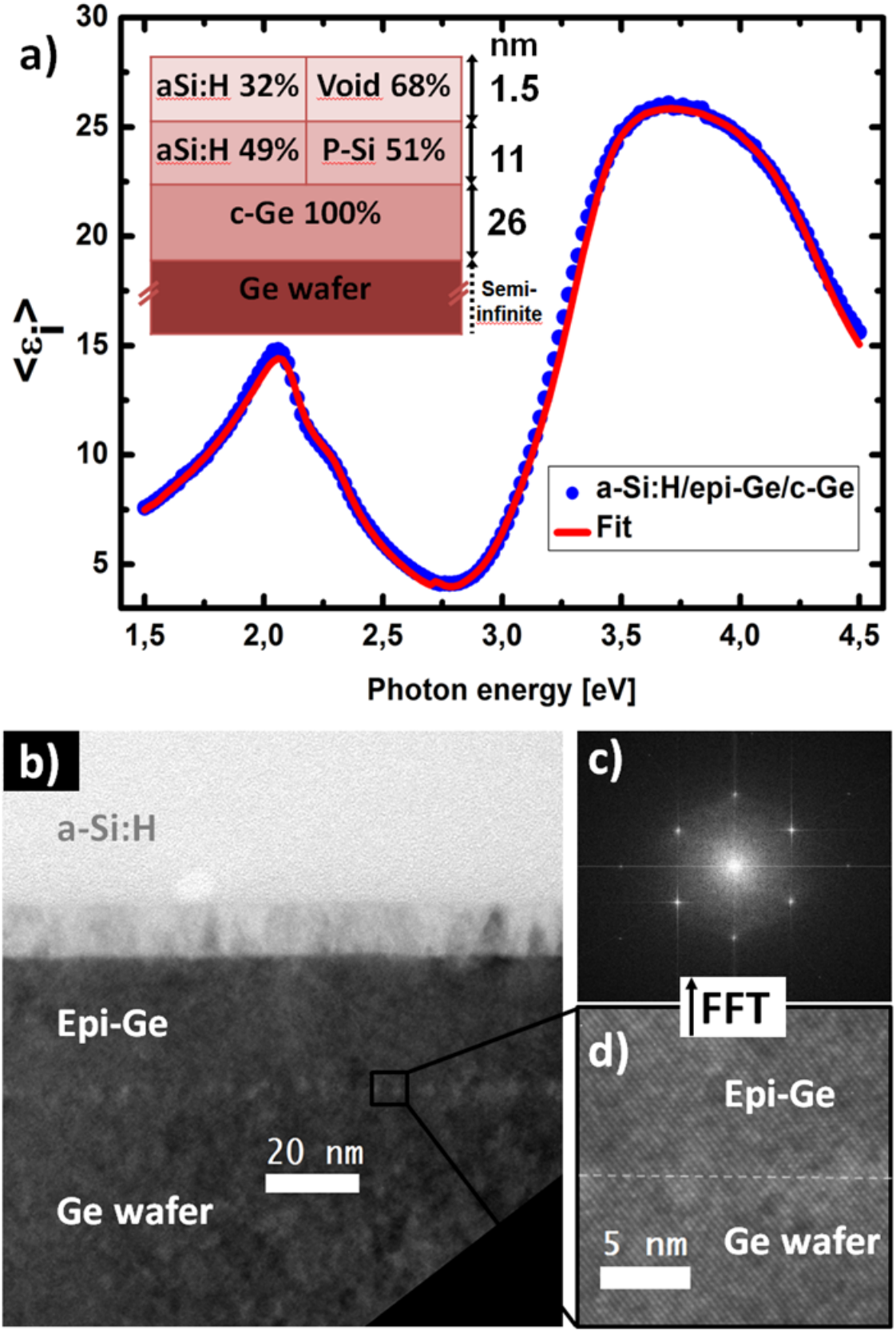


Fig. 4.36 – a) Ellipsometry spectrum of epitaxial germanium on c-Ge wafer, covered by a-Si:H. The red line is the fit of experimental data (circular points) according to the model in the inset. b) HRTEM cross section of the sample. c) FFT image of epi-Ge/c-Ge interface area enlarged in d).

Fig.4.36-a) shows the ε_i function of the epi-Ge coated with a-Si:H film (circles) on c-Ge substrate and fitting (red line) with the optical model detailed in inset. The dispersion curve of monocrystalline Ge was used for the epi-Ge layer model[37], and a combination of Tauc-Lorentz dispersion formula, large grain polycrystalline silicon (poly-Si) and void for the top a-Si:H layer (Bruggemann approximation). The fit shows an excellent agreement with the experimental data, thus giving a first proof that the layer is monocrystalline Ge. However, no interface layer was found between wafer and epi-layer, which are described by the same material, thus it was difficult to directly extract epi-Ge thickness from the model. Consequently, a first approximation of Ge deposited thickness was extracted by fitting ellipsometry spectra measured of germanium films co-deposited on crystalline Si wafer and glass substrates. Using this procedure our stack was well described by 12.5 nm of a-Si:H, with a 50% crystalline fraction and 1.5 nm roughness, covering 26 nm of 100 % monocrystalline epi-Ge layer. The partial crystallinity of the a-Si:H layer is linked to some epitaxial regrowth at the epi-Ge/a-Si:H interface; this effect indeed absent on c-Ge/a-Si:H interface. Specific treatments, such as the ultra-thin a-SiC:H layer used in the c-Si/a-Si:H interface, should suppress this effect[36].

These results were correlated with TEM analysis, as shown by cross-section micrograph in Fig.4.36-b). Less than 1 nm discrepancy was observed between the thicknesses deduced from ellipsometry and bright field TEM image, thus confirming that Ge homoepitaxy thickness can be accurately deduced from fitting ellipsometry data of co-deposited Ge on c-Si and glass substrates. Once again, it is interesting to note that a simple deionized water cleaning process results in a very good structural interface, as visible by high resolution TEM (4.36-d)). This is in good agreement with the absence of interface layer between epi-Ge and c-Ge found by ellipsometry. Proof of the excellent crystal quality is visible from atom periodicity and Fast Fourier Transform (FFT) of the interface showing sharp points (4.36-c)). The 50% crystallinity top mixed phase a-Si:H/p-Si deduced from optical modeling is explained by pyramidal shape epitaxial regrowth inside the a-Si:H layer. Thus, the ellipsometry data and TEM analysis are consistent, and they together constitute the evidence of high quality epitaxial Ge grown on Ge substrate by PECVD at 175°C.

We have then extended this approach to hetero-epitaxy of Ge on c-Si, and both ellipsometry and TEM were used to characterize the layer. Fig.4.37-a) shows the optical model deduced from ellipsometry: the total film thickness is 168nm with the epi-Ge/air interface described by a 3.8 nm of mixed c-Ge, GeO2 and voids layer. Accurate data fitting requires to use $Si_{1-x}Ge_x$ alloy for the first 48 nm, with x=0.95, and a 100% crystalline germanium for the last 116 nm. To confirm the presence of Si inside germanium layer, suggested by ellipsometric modeling, we have performed energy dispersive X-ray spectroscopy (EDX) on the same sample: we found about 8% of silicon, which is in good agreement with the above mentioned value. As the Ge deposition is performed in a plasma reactor otherwise mostly dedicated to silicon, contamination from silicon residues on the reactor walls is likely. If desired, appropriate cleaning and pre-coating of the chamber walls should allow a significant reduction of this Si incorporation.

[36] M. Labrune. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells.* PhD thesis. Ecole Polytechnique, France, May 2011.

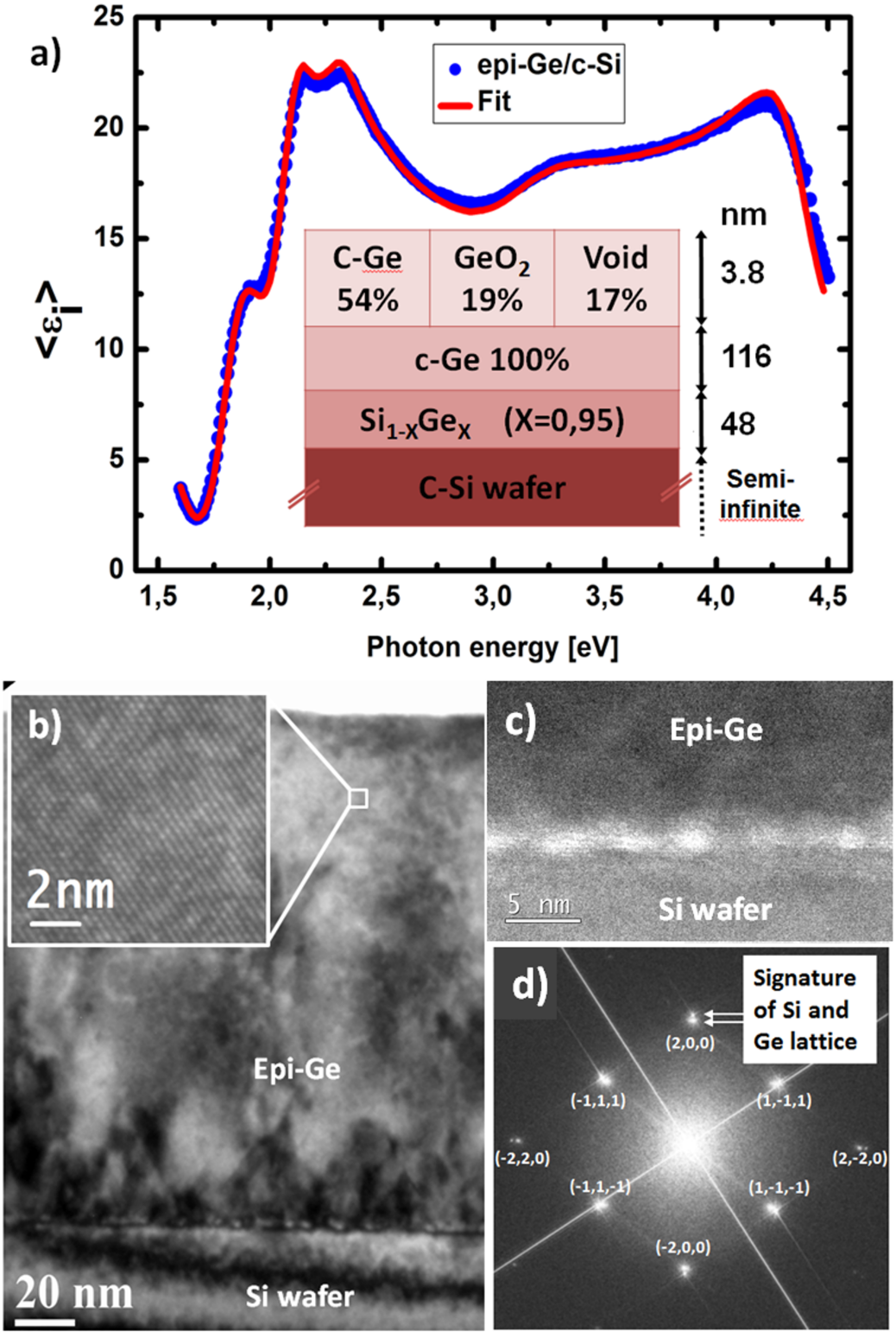


Fig. 4.37 – a) Ellipsometry spectrum of a 168 nm thick epitaxial germanium layer on a c-Si. The red line is the fit of the experimental data (circles) according to the model in the inset. b) Cross-section TEM picture of the same sample, with a high resolution zoom on Ge bulk close to the layer's top. c) EFTEM oxygen map acquired at the wafer interface. White spots are the silicon oxide islands, characterized. Inset d) shows FFT of the whole stack with double pattern corresponding to a relaxed Ge grown on c-Si wafer.

However, Si incorporation in epi-Ge film may have the beneficial effect of smoothing the structural transition. The lattice parameter for SiGe alloys is indeed given by[129]:

$$a_{Si_{1-x}Ge_x} = 0.5431 + 0.01992x + 0.0002733x^2 \ \ (nm) \tag{4.11}$$

In the case of 5-8% Si in Ge matrix, it gives a lattice parameter in the range of [0.5610-0.5616] nm, as compared to 0.5657 nm for bulk Ge: this is a $\sim$ -0.8 % of mismatch with respect to Ge. Thus, a controlled SiGe graded alloy from interface should contribute to reduce even further defects in Ge layers.

TEM cross section analysis was performed on this sample; the result is shown in Fig.4.37-b). It is possible to recognize two regions characterized by different crystal quality: i) a high concentration of dislocations and stacking faults is lying in the first $\sim$50 nanometers, arising from the 4.2% mismatch between Si and Ge lattice. Fig.4.37-c) shows an EFTEM oxygen map acquired at the wafer interface, the white spots at the interface correspond to silicon oxide islands, characterized by plasmon electron energy loss centered at 26 eV; the presence of this oxide is probably explained by an imperfect wafer cleaning. As a matter of fact, as shown previously, we systematically observe a higher concentration of impurities (O, C, H) at the interface, owing to the fact that we use a non UHV environment. ii) A clear improvement in layer crystalline quality with increasing epitaxial thickness: close to the surface few defects are visible, as testified by inset zoom in Fig.4.37-b). Thus, the defective area near the interface with the substrate probably releases the strain, and germanium adopts its own lattice parameter for the thicker epitaxial growth. This is confirmed by the FFT (see 4.37-d)): double pattern for each point is distinguishable, which is the signature of the two lattice parameters Si and Ge. Epitaxial Ge on Si is known to follow the Stranski-Krastanov (SK) growth mechanism[130] under a variety of experimental deposition conditions (yet high temperature), in which Ge films remain continuous up to a few monolayers before breaking into high density Ge islands. In our deposition conditions, namely low temperature (175°C) and hydrogen rich plasma, the growth likely proceed by islands. The presence of plasma synthesized Ge nanoclusters that can contribute to the growth has also been demonstrated experimentally[113].

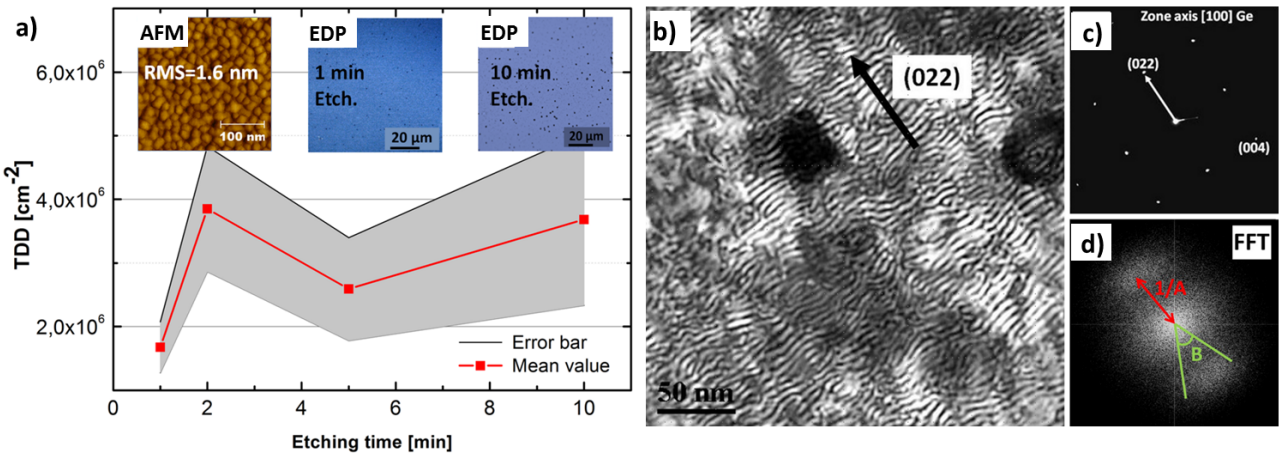


Fig. 4.38 – a) Time evolution of surface threading dislocation density (TDD), for epi-Ge on c-Si etched by iodine solution. Inset shows AFM image of a 168 nm thick Ge on Si prior etching. Optical images of Ge after 1 min and 10 min chemical etching for etching pit counting. b) Plan-view TEM of epi-Ge on c-Si (100); the fringes are the Moiré pattern obtained in two beam condition using the (220) Si reflection, as shown in b). c) FFT of the Moiré pattern; A is the average value of the fringes spacing and the angle B is related to the distortions in the crystal.

[129] V.T. Bublik et al., physica status solidi (b), **65**: K79–K84, 1974.
[130] D. J. Eaglesham et al., Physical Review Letters, **64**: 1943–1946, 1990.

The surface quality of Ge deposited on Si was examined by AFM in tapping mode, and by measuring the etching pit density (EDP). Wet chemical etching by iodine solution [CH3COOH (65mL)|HNO3 (20mL)|HF(10mL)|I2(30mg)] is a well-established[128] method for measuring surface threading dislocation density (TDD) on Ge/Si systems. The surface was found to have a RMS roughness of 1.6 nm as shown in Fig.4.38-a), and TDD in the range of few $10^{6}\mathrm{cm}^{-2}$ were found for a 100 nm thick layer. Those values compare favorably with epitaxial Ge layer produced by chemical vapor deposition in the range 400-600°C range, followed by a post-growth anneal at 825°C[125]. Fig.4.38-a) shows the TDD versus etching time with corresponding optical microscope images of Ge surfaces after 1 and 10 min. We observe a small TDD increase with time (and thus with depth from the initial surface) with a stabilization around $5.10^{6}\mathrm{cm}^{-2}$.

Quantitative strain characterization was based on TEM observation of Moir*é* patterns. Moir*é* patterns are produced when two crystals with different lattice parameters overlap and the inter-distance between the fringes in the Moir*é* patterns is strictly related to those lattice parameters[131,132]. Fig.4.38-b) shows the Moir*é* pattern (fringes) obtained in two beams bright field configuration, for an epi-Ge/c-Si sample observed in plan-view, choosing one of the (220) directions 4.38-c). The sample was tilted in such a way that all the reflections around the silicon [100] zone axis were far from the exact Bragg position. This configuration strongly reduces the diffraction contrast arising from defects and allows us to see the Moir*é* pattern clearly. The non-continuous fringes reveal some complex structure on defects, which would require further investigation. However, to get quantitative information on the lattice parameter, the FFT was analyzed, as shown in Fig.4.38-d). The average value of the inter-distance fringes A, is deduced from the distance between the center of the FFT and the center of the halo, that is 1/A; B is related to the bending of the fringes coming from distortions in the Ge epitaxial domains. Thus, measuring A we are able to know the inter-distance of (220) plane $\mathrm{d}_{\boldsymbol{epiGe(220)}}$. Assuming symmetry in the x-y plane for this face-centered cubic system, one can find the lattice parameter $\mathrm{a}_{\boldsymbol{epiGe}}$, and the biaxial strain $\boldsymbol{\varepsilon}$:

$$\begin{aligned} \boldsymbol{d_{epiGe(220)}} &= \boldsymbol{A \times d_{Si(220)}/(A - d_{Si(220)})} \\ \boldsymbol{a_{epiGe}} &= \boldsymbol{d_{epiGe} \times (h^2 + k^2 + l^2)^{1/2}} \\ \boldsymbol{\varepsilon} &= \boldsymbol{(a_{epiGe} - a_{Ge})/a_{Ge}} \end{aligned} \tag{4.12}$$

For a perfect crystal, one can find in literature $\mathrm{d}_{\boldsymbol{Si(220)}} = 0.1919\mathrm{nm}$ and $\mathrm{a}_{\boldsymbol{Ge}} = 0.5657\mathrm{nm}$; with the experimental value A = 5.221±0.074nm (error introduced by pixel size) we finally get $\boldsymbol{\varepsilon}$ = -0.39±0.06%. This confirms that despite the 4.2% mismatch between those two crystals, there is a good relaxation of epi-Ge crystal grown on c-Si wafer. Besides, the non-zero value and the negative symbol of $\boldsymbol{\varepsilon}$ reveals a slightly compressively residual strain.

In summary, epitaxial germanium growth by standard RF-PECVD at 200°C on both c-Ge and c-Si substrates was demonstrated. Investigation of the material quality by means of ellipsometry, TEM, AFM and chemical etching has proven a good crystalline quality of the layers. Supported by HRTEM analyses, we have shown that ellipsometry data fitting can provide accurate determination of the layers thickness, composition, and interface quality. Excellent structural quality epi-Ge on c-Ge has been grown by this simple low temperature process. For epi-Ge on c-Si substrate, stacking faults arising from the Si and Ge mismatch, as well as Si contamination, are mostly located in the first tens of nanometers above interface, and then crystal quality improves with thickness. With a 200 nm epi-Ge layer, a relatively low roughness and low surface threading dislocation density can be achieved. From Moir*é* patterns analysis, we found a residual slightly compressively strain in the range of -0.4%.

The integration of such epi-Ge material in a solar cell device remains challenging. The various attempt we could make during this thesis were not very successful. In fact, several factors were making

[131] Peter Bernhard Hirsch. *Electron microscopy of thin crystals.* en Butterworths, 1965.
[132] G. Capellini et al., Journal of Applied Physics, **107**: 063504–063504–8, 2010.

this task difficult: i) firstly our Ge deposition rate being around $0.1 Å.s^{-1}$, growing few hundreds nanometers thick absorber requires a long time. ii) Secondly, the surface passivation of Ge is more difficult compared to silicon and iii) low resistive ohmic contacts to Ge are difficult to achieve because of strong Fermi-level pinning on Ge[133,134]. Additional work would be required to address properly those issues in order to obtain efficient solar cells based on epi-Ge absorber.

4.5.2 Low temperature growth of SiGe alloys

In addition to the growth of epitaxial germanium, we have also explored the possibility of growing SiGe alloys, since this material system has many interesting properties. Indeed, alloying silicon with germanium is a complementary solution for absorption enhancement[135]. SiGe heterostructures have the potential to improve state of the art Si technologies, and they are already used in a large field of applications (HBT, MOSFETS, solar cells, quantum structures, etc.)[136]. Band gap, lattice parameter and electrical properties being tunable with Ge atomic fraction and strain, SiGe is also a good candidate for integration of III-V materials on silicon, as well as for low energy band gap junction in tandem solar cells[8,137,138]. Absorption depth and energy gap as a function of Ge % in the alloy are presented in Fig.4.39.

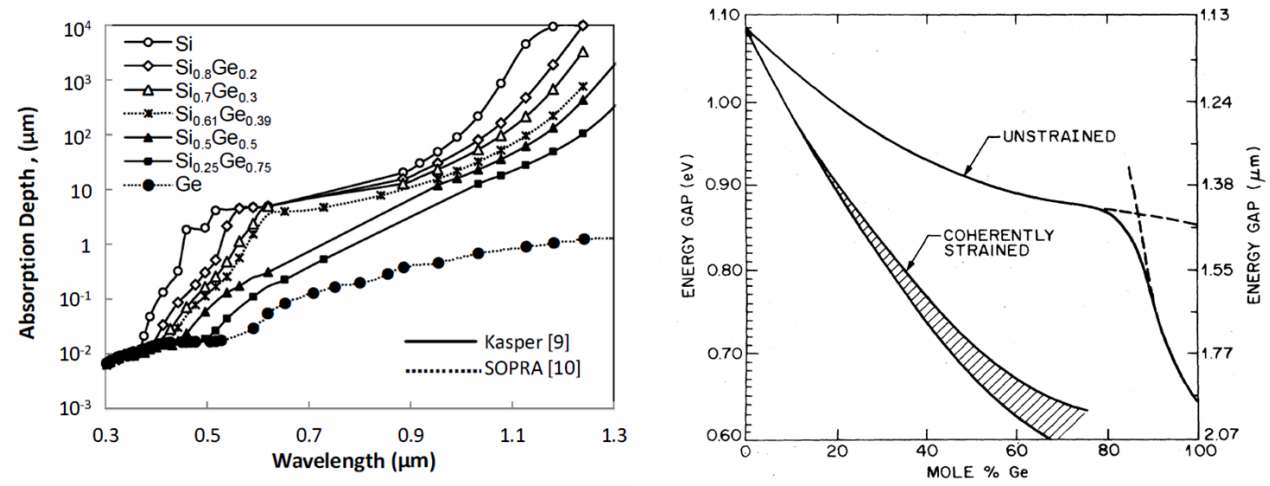


Fig. 4.39 – a) Absorption depth as a function of wavelength for different Ge percentages, from Hadi et al.[139] and b) SiGe energy gap as a function of Ge% for coherently strained (pseudomorphic growth on Si) and unstrained scenario, from People et al.[137]

An overview of thin film single junction solar cells from literature with different SiGe absorbers, sorted by SiGe deposition temperature[139–145], is displayed in Tab.4.7. Among those approaches, we focus on heterojunction solar cells which benefit from the monocrystal SiGe (c-SiGe) absorber quality

[133] K. Martens et al., Applied Physics Letters, **98**: 013504–013504–3, 2011.
[134] A. Dimoulas et al., Applied Physics Letters, **89**: 252110–252110–3, 2006.
[135] R. Braunstein et al., Physical Review, **109**: 695–710, 1958.
[136] Y. Shiraki et al., Surface Science Reports, **59**: 153–207, 2005.
[137] R. People., Physical Review B, **32**: 1405–1408, 1985.
[138] S.A. Ringel et al., Progress in Photovoltaics: Research and Applications, **10**: 417–426, 2002.
[139] S.A. Hadi et al., 38th IEEE Photovoltaic Specialists Conference (PVSC), 000005–000008, 2012.
[140] Y.-H. Chen et al., Thin Solid Films, **529**: 7–9, 2013.
[141] M. Isomura et al., Solar Energy Materials and Solar Cells, **74**: 519–524, 2002.
[142] T. Matsui et al., Solar Energy Materials and Solar Cells, **93**: 1100–1102, 2009.
[143] K. Said et al., Thin Solid Films, **337**: 85–89, 1999.
[144] K. Said et al., IEEE Transactions on Electron Devices, **46**: 2103–2110, 1999.
[145] R. Oshima et al., Journal of Crystal Growth, **378**: 226–229, 2013.

and a high open circuit voltage thanks to the excellent surface passivation provided by the amorphous (a-Si:H) emitter. Unlike conventional deposition techniques, we show here that both low temperature, namely 175°C, and $Si_{1-x}Ge_x$ epitaxy are compatible, using standard PECVD. This work received great help from graduates students N. Ramay and J. Tang.

Ref.	Absorber			V_{oc}	J_{sc}	FF	η
	Material	Deposition	(μm)	(mV)	(mA/cm^2)	(%)	(%)
Chen[140]	a-SiGe	VHF-PECVD/200°C	0.13	560	19.8	57.6	6.38
Isomura[141]	μc-$Si_{0.8}Ge_{0.2}$	RF-PECVD/∼200°C	0.5	397	22.7	62.3	5.6
Matsui[142]	μc-$Si_{0.8}Ge_{0.2}$	VHF-PECVD/200°C	1	427	24.1	61.6	6.33
Said[143]	c-$Si_{0.9}Ge_{0.1}$	RP-CVD/750°C	15	559	24.2	76	10.3
Oshima[145]	c-$Si_{0.58}Ge_{0.42}$	MBE/550°C	2	233	8.25	50.9	1
Hadi[139]	c-$Si_{0.44}Ge_{0.56}$	LP-CVD/900°C	2	323	21.16	68	4.7
This work	epi-$Si_{0.73}Ge_{0.27}$	PECVD/175°C	1.9	416	18.8	77.5	6.1

Tab. 4.7 – Summary of single junction $Si_{1-x}Ge_x$ solar cells from literature.

Epitaxial layers are grown on (100) oriented c-Si wafers cleaned by 30s dip in 5% HF solution. In a standard PECVD reactor, the deposition was done at 175°C from the following gas precursors: pure SiH_4, H_2 and 2% GeH_4 diluted in H_2, referred as GeH_4 in this study. This growth process occurs at a pressure of 2.6 mbar, with a RF-power density of 50 mW/cm^2. SiGe layers with thicknesses of 200-500 nm were epitaxially grown with $GeH_4/(SiH_4+ GeH_4)$ gas flux ratio in the 0-0.55 range. Ellipsometry, Raman spectroscopy, TEM, SIMS and GDOES were used to qualify material composition and quality. Then, thicker epitaxial layers were grown to make solar cells.

Since RF-PECVD epitaxial growth of crystalline SiGe alloys at such low temperature has not yet been reported, a set of samples with various thicknesses and composition has been deposited to calibrate the process. As low temperature plasma parameters to promote Si or Ge epitaxy have already been optimized, similar conditions were used for SiGe growth. Under a constant H_2 flow rate of 500 sccm, the germane to silane gas flow ratio has been changed under a constant pressure of 2.6 mbar. Fig.4.40 displays ε_i function for a PECVD epitaxial SiGe layer. This data was fitted by a four layer optical model, as shown in the inset: i) semi-infinite crystalline silicon wafer, ii) interface between wafer and epitaxy, modeled by a mix, according to Bruggemann effective medium approximation, of voids, residual SiO_2 due to imperfect cleaning and $Si_{1-x}Ge_x$, iii) epitaxial $Si_{1-x}Ge_x$ layer, and iv) a surface layer composed of $Si_{1-x}Ge_x$ and voids, standing for the roughness of epi-layer. Thicknesses and compositions were the free parameters; the resulting fitted values are shown in the inset: 220 nm of crystalline $Si_{0.65}Ge_{0.35}$ with a 2.5 nm roughness, grown on a 1.4 nm imperfect interface layer, is found for this sample. The excellent agreement, obtained using this fitting model, with the experimental data confirms that low temperature epitaxial layer is a mono-crystalline SiGe layer.

The ε_i function of epitaxial layers with various thickness and compositions, together with fits and reference spectra for bulk c-Si (dash line), c-$Si_{0.51}Ge_{0.49}$ (dot line) and bulk c-Ge (dash dot line), are shown in Fig.4.41-a). The grey curves represent SiGe samples with $GeH_4/(SiH_4+ GeH_4)$ ratio varied from 0 (squares), i.e. pure silicon epitaxy, to 0.55 (diamonds) corresponding to 35% Ge in the alloy. A clear evolution from c-Si to c-Ge is visible when increasing this gas ratio: silicon peak amplitude at 4.2 eV decreases towards the Ge peak and the 3.4 eV silicon peak is progressively downshifted in terms of energy position and amplitude. The layer structure and stoichiometry are deduced from fitting experimental curves with the optical model and material database provided by Horiba Jobin Yvon

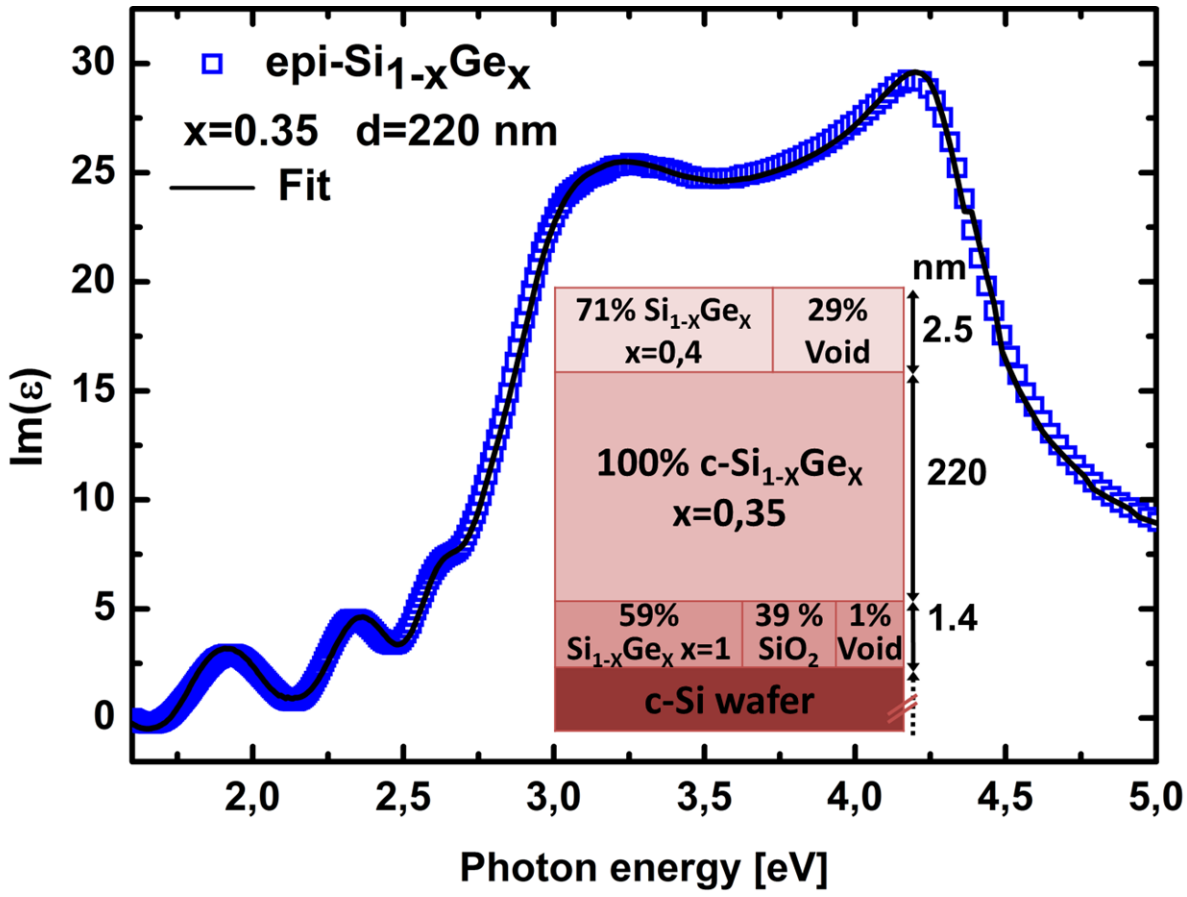


Fig. 4.40 – Imaginary part of the pseudo-dielectric function ε_i of epitaxial $Si_{0.65}Ge_{0.35}$ sample deposited at 175°C by PECVD on c-Si(100). Experimental data (squares) together with thickness/composition fit result (black line). Inset shows the optical fitting model.

software DeltaPsi 2, with the fitting procedure described above. Based on such modeling, Fig.4.41-b) shows the Ge % deduced from fitting (triangles) on left axis, as a function of GeH_4 concentration in the gas phase $GeH_4/(SiH_4+ GeH_4)$. The error bars on Ge % given by this procedure are typically in the range of 0.2-0.5%, that is smaller than the symbol size. Up to 35 % Ge, we found that the epi-$Si_{1-x}Ge_x$ composition varies linearly (dash line, R^2=0.96). Note that this fit does not intercept the (0;0) point, probably due to mass flow controller offset in our experimental set-up. GeH_4 concentration in the gas phase predominantly determines the composition of SiGe alloy; moreover the fraction of Ge incorporated in the layer is much higher than the GeH_4 fraction in gas phase (GeH_4 precursor being 2% diluted in H_2). In fact, this difference is a well-known effect in PECVD, attributed to the lower activation energy of dissociation and sticking coefficient for germane with respect to silane[146]. Non-linear dependence with $GeH_4/(SiH_4+ GeH_4)$ has been reported[147], however this was in the case of $Si_{1-x}Ge_x$ with x > 35%.

To corroborate Ge% deduced from SE fitting, the Ge composition has also been investigated using Raman, GDOES and SIMS techniques. The Raman spectrum of SiGe alloys is characterized by three main peaks, around spectral regions of 300, 400 and 500 cm^{-1}, corresponding respectively to Ge-Ge, Si-Ge and Si-Si LO phonon modes. Experimental Raman spectra measured on low temperature epi-SiGe with various compositions are shown in Fig.4.42-a): the three first order peaks are visible, together with an additional peak coming from the c-Si substrate. The data were acquired at room

[146] J.R. Doyle et al., Journal of Applied Physics, **71**: 4727–4738, 1992.
[147] T. Matsui et al., Journal of Non-Crystalline Solids, **352**: 1255–1258, 2006.

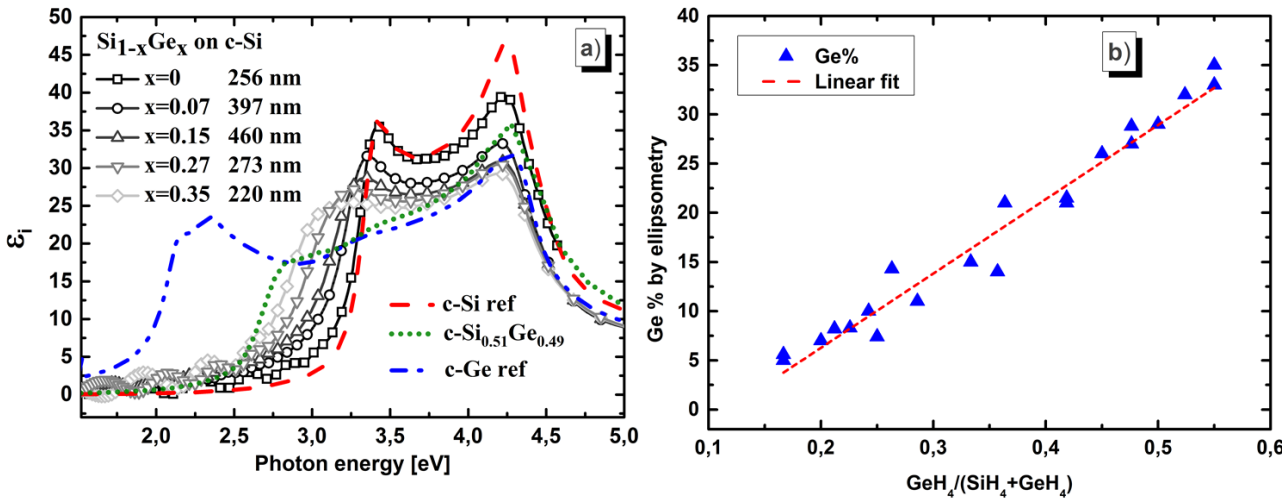


Fig. 4.41 – a) ε_i function of PECVD epitaxial $Si_{1-x}Ge_x$ on c-Si with x in [0-35]% (Grey symbols), bulk c-Si, c-$Si_{0.51}Ge_{0.49}$ and c-Ge references (dash, dot and dash dot lines). b) Ge % in epi-SiGe deduced by ellipsometry as a function of $GeH_4/(SiH_4+ GeH_4)$ gas flow rate ratio (triangles), and linear fit (dashed line). Error bars are smaller than symbols size.

temperature with laser excitation wavelength of 532 nm; the influence of the penetration depth was also tested using $\boldsymbol{\lambda} = 473$ nm and 633 nm excitation lasers. At 532 nm, the absorption depth changes from 1.5 $\boldsymbol{\mu}$m in pure silicon to 350 nm for $Si_{0.75}Ge_{0.35}$.

The inset in Fig.4.42-a) shows the Si-Si peaks from substrate and SiGe material; the wafer peak becomes less visible with increasing Ge% and thickness. Si-Si LO mode, in SiGe, shifts with Ge composition (14% to 32%) from 514 to 500 cm^{-1}. In addition to the shift, Raman band broadening is also an important parameter, since it is related to inhomogeneities, alloy clustering and crystallographic defects (e.g. twins defects). In our case, the FWHM of Si-Si peaks varies between 5.7 to 8 cm^{-1}, which is close to the value of ~ 5 cm^{-1} for bulk monocrystalline material[148,149], thus confirming that good crystal quality is achieved. Note that measurements at increasing laser power densities, prior to acquisition, were done to determine the threshold above which the Raman spectrum is affected by laser heating. Below this threshold, the Raman peak frequency shift is an accurate signature of the layer stress and composition; consequently, by fitting the spectrum, we were able to determine both strain state and Ge % in epi-$Si_{1-x}Ge_x$ films, using the following equations (valid for x < 0.5)[150]:

$$\begin{aligned} \omega_{Si-Si}\ (cm^{-1}) &= 520.0 - 68x + \Delta_{Si}.\Sigma \\ \omega_{Si-Ge}\ (cm^{-1}) &= 400.5 + 14.2x + \Delta_{SiGe}.\Sigma \end{aligned} \tag{4.13}$$

Where x refers to Ge fraction, $\boldsymbol{\Sigma} = \varepsilon/0.0417$ is the normalized strain and $\boldsymbol{\Delta_i}$ are constant parameters equal to 34 and 24 cm^{-1} for Si and SiGe respectively. Ge-Ge peaks being less intense, we did not use that part of the spectrum in this study. The Ge% from Raman fitting plotted versus Ge% from SE data is represented by open symbols in Fig.4.42-b): squares correspond to 473nm laser excitation, circles to 532 nm and triangles to 633 nm. The data obtained with three lasers show an excellent linear correlation with x deduced by SE (see x=y dash line): while 473 nm laser results have a slope of 1.1, red and green lasers exhibit a slope of 0.970 and 1,025, with an absolute Ge% agreement within ±2.8% and ±1.6% respectively.

[148] J. Olivares et al., Thin Solid Films, **358**: 56–61, 2000.
[149] M.R. Islam et al., The European Physical Journal - Applied Physics, **27**: 325–328, 2004.
[150] J.C. Tsang et al., Journal of Applied Physics, **75**: 8098–8108, 1994.

Further chemical characterizations were done with optical (GDOES) and mass spectrometry (SIMS). In both cases Ge% was extracted (without the use of commercial calibrated SiGe sample) using the intensity ratio from the epi-SiGe layer: Ge%=$I_{Ge}/I_{Si}+I_{Ge}$. The resulting data has a relatively good linear correlation with SE results, as shown in Fig.4.42-b): GDOES (stars symbols) has an R-square of 0.95 and SIMS (diamonds) of 0.90. The small fitting offset observed by SIMS can be explained by the non-linear variation of sputtering rate and ionization yield with chemical composition, known as matrix effect. For both GDOES and SIMS, the linear fitting has a slope far from the unit value, and consequently those techniques cannot lead to an absolute quantification of Ge% without composition calibrated reference samples. With the intention of reducing the matrix effects, SIMS analysis was also performed in MCs^+ mode, where polyatomic ions formed with primary Cs atoms ($SiCs^+$ and $GeCs^+$) were detected instead of mono-atomic Si and Ge. A suppression of the matrix effects for SiGe alloys with MCs^+ detection mode has already been reported, for given primary beam energy, angle and chemical composition range[151,152]. In our case, with 5keV Cs^+ primary beam energy , the MCs^+ results could be linearly fitted with a R-square of 0.96 and a slope of 0.9 (see close circles in Fig.4.42-b). This corresponds to an absolute Ge% difference with SE within $\pm$2.9%. Thus to conclude, we found a linear correlation with ellipsometry for Ge fraction with Raman, SIMS and GDOES measurements. Moreover, the accuracy of ellipsometry is demonstrated thanks to direct quantitative measurements of the chemical composition with two independent techniques: Raman and SIMS-MCs^+.

Based on equation 4.13 the strain in our epi-SiGe layers has been extracted, with the assumption that samples were under biaxial strain in the x-y plane of (100) orientation. Theoretical relaxed $Si_{1-x}Ge_x$ lattice parameter has an x dependent misfit with the c-Si lattice in the range of 0 to 4.17%: for example, a 30% Ge alloy has about 1% misfit with the silicon substrate. In Fig.4.43-a), the position of Si-Si mode in SiGe is presented as a function of Ge content deduced from data obtained by SE; both red (circles) and green (squares) lasers excitation data are shown. As a guide to the eyes, fully strained (solid line) and fully relaxed (dash line) are represented on the graph. Even though there is a small discrepancy between the results of the two probing lasers, one can see that epi-$Si_{1-x}Ge_x$ with $x \leq 0.2$ is half or fully strained, whereas results are very close to fully relaxed for $x \geq 0.25$. Given the relatively strain transition seen in this graph, roughly 20% Ge concentration is probably a threshold above which threading dislocations appear for these given deposition conditions.

In the case of SiGe epitaxial growth on silicon, it is well known that when the SiGe layer is below a composition dependent critical value, the layer is lattice matched and fully strained (pseudomorphic growth). But once the epilayer thickness exceeds this critical thickness h_c, the strain is relaxed via misfit dislocations at the SiGe/Si interface, and consequently threading dislocations extend through the SiGe layer (metamorphic scenario). However, pseudomorphic growth is possible beyond the thermodynamic equilibrium value: e.g. one order of magnitude higher h_c was reported by MBE growth at 550°C[137]. This metastable regime can be sustained for even higher SiGe thicknesses if a lower growth temperature is used[153]. Thus, the stress relaxation observed by Raman indicates that beyond $\sim$20% Ge the layers exceed the metastable limit for this deposition conditions, and more defects and threading dislocations could be present in this material composition.

[151] D. Marseilhan et al., Applied Surface Science, **255**: 1412–1414, 2008.
[152] B. Saha et al., Applied Physics A, **108**: 671–677, 2012.
[153] E. Kasper et al., Applied Surface Science, **224**: 3–8, 2004.

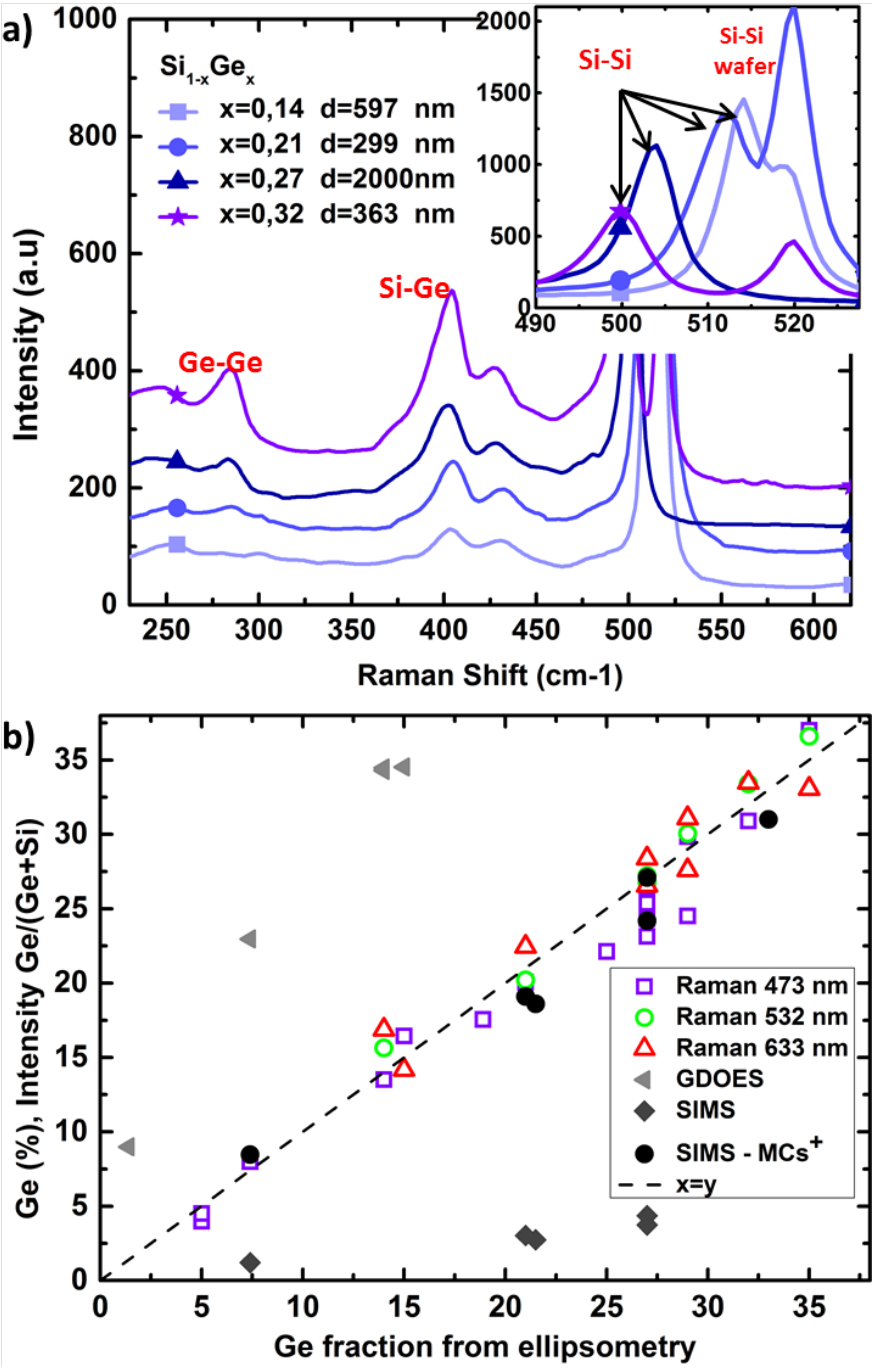


Fig. 4.42 – a) Raman spectra of epitaxial $Si_{1-x}Ge_x$ grown on c-Si by PECVD at 175°C, with x = 0.14, 0.21, 0.27 and 0.32. The data are acquired with a 532 nm laser at room temperature. The inset zooms on the Si-Si peak. b) Ge% deduced from Raman, GDOES, SIMS and SIMS-MCs^+ as a function of Ge% deduced from the ellipsometry analysis.

To further investigate the change in crystal structure before and after the relaxation, as deduced from Raman spectroscopy, two samples were examined by TEM cross section along the <110> axis. The results are shown in Fig.4.43: while epi-$Si_{\mathbf{0.89}}Ge_{\mathbf{0.11}}$ on c-Si (see Fig.4.43-b)) shows good crystal quality confirmed by diffraction pattern (Fig.4.43-c)) and high resolution zoom of the bulk (Fig.4.43-d), some threading dislocations are found for $Si_{\mathbf{0.82}}Ge_{\mathbf{0.18}}$ (Fig.4.43-e). In both samples, defects such as H platelets are detected; this is visible for instance on the high magnification inset Fig.(Fig.4.43-d). Together with other point defects, this explains the black-spotted aspect of the layer. Thus both Raman and TEM analysis confirm the existence of a threshold for misfit relaxation through thread-

ing dislocations and stacking faults. While there is a small discrepancy observed for Ge% at which dislocations appear by Raman and TEM, one should keep in mind that TEM is a very local analysis technique, whereas Raman is probing a much larger area. Thus we can conclude that epitaxial growth of SiGe at 175°C on c-Si (100) is nearly pseudomorphic for x$\leq$0.18-0.2, and with higher germanium content (x$\geq$0.18-0.2), the growth becomes metamorphic.

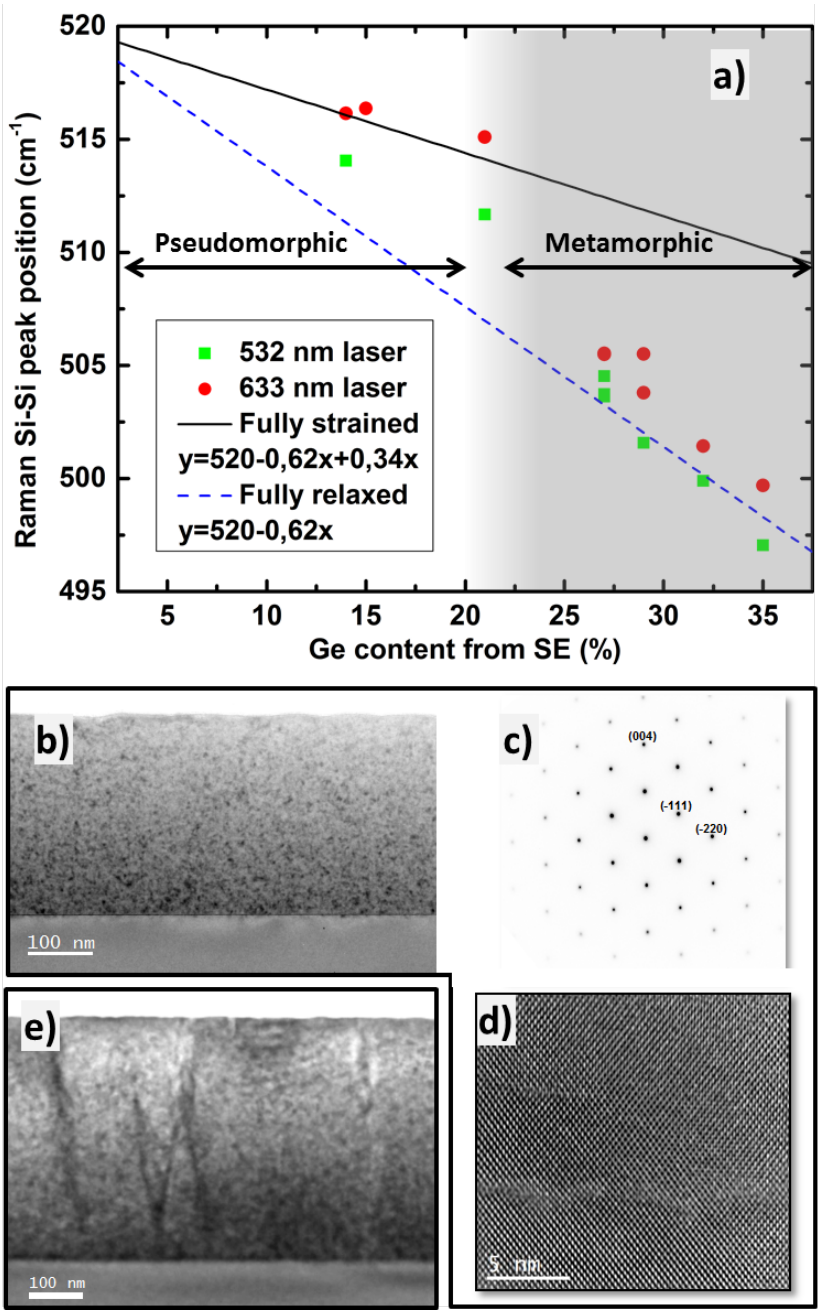


Fig. 4.43 – a) Raman shift for Si-Si peak as function of Ge %, in SiGe alloy grown on c-Si (100), measured with green (squares) and red (circles) lasers. Solid and dash lines represent respectively theoretical fully strained and fully relaxed scenarios. b) Cross section TEM images along <110> axis of $Si_{0.89}Ge_{0.11}$ on c-Si. The layer diffraction pattern is shown in c). d) High resolution zoom of layer bulk showing a platelet defect. e) Threading dislocations are visible for $Si_{0.82}Ge_{0.18}$/c-Si by cross section TEM images along <110>.

Solar cells

In order to study the effect of alloying Ge with Si on solar cell performances, two compositions were investigated: - a 1.7μm epitaxial silicon (epi-Si) - a 1.8μm epitaxial $Si_{0.83}Ge_{0.27}$. Without breaking vacuum, but in separate plasma chambers, (n)a-Si:H emitter layer (see Tab.4.1) was deposited on top of previously mentioned epitaxial layers to form the solar cell heterojunction. In the case of SiGe absorber, an extremely thin (∼1 nm) epitaxial silicon cap layer was deposited before the amorphous emitter, to reduce interface states and produce similar interface properties compared to the epi-Si cell[139,154]. The area of the cells (4 cm^2), was defined by the ITO layer sputtered through a shadow mask. The front contact grid and the full plate back contact were realized by aluminum evaporation. Then, the J-V characteristics and external quantum efficiency (EQE) of the device with and without Ge are compared[155,156].

The influence of the composition of a $Si_{1-x}Ge_x$ alloy on the expected short circuit current as well as on the EQE was first investigated by simple absorption calculations, and by using PC1D software. Based on reference absorption coefficients of various c-SiGe alloys, the ideal J_{sc} has been calculated as a function of SiGe thickness, assuming EQE=1 and R=0; the results are shown in Fig.4.44-a). One can see that above ∼10% Ge in silicon, there is a gain in absorption which results in a higher J_{sc} for every thickness. For example, a 1 μm thick c-Si absorber will produce a ∼12 mA.cm^{-2} J_{sc} whereas the same thickness of $Si_{0.63}Ge_{0.37}$ will result in ∼ 20 mA.cm^{-2}. For the solar cell, the model developed for epi-Si solar cells[155] was modified and adapted to describe the c-Si(p++)/epi-$Si_{1-x}Ge_x$/n-aSi:H structure. The EQE of a solar cells with 2μm SiGe of various compositions are shown in Fig.4.44-b). From pure Si to 54 % Ge in the alloy, a significant improvement in the long wavelength range happens.

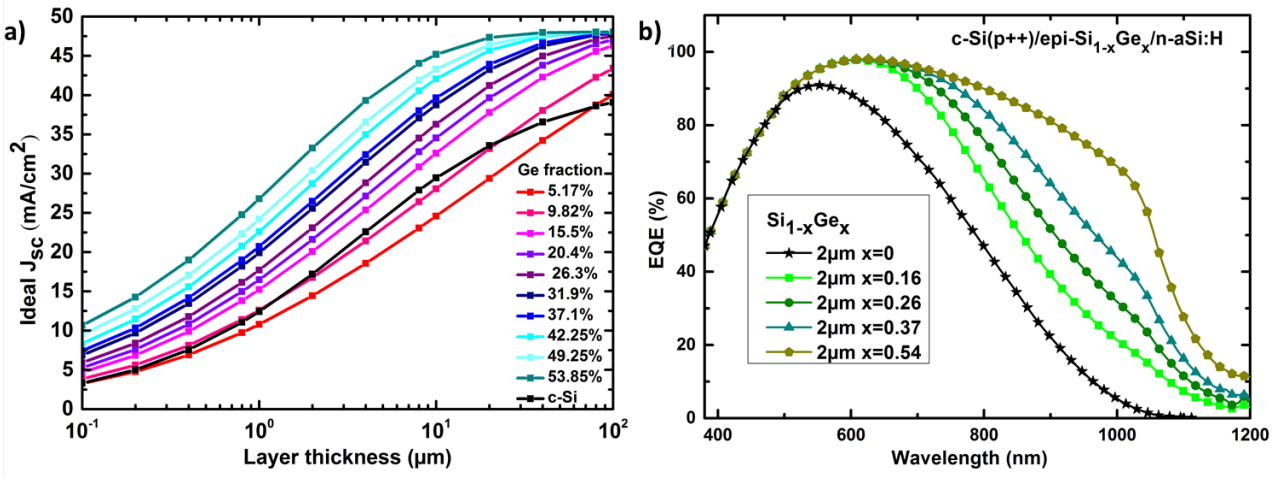


Fig. 4.44 – a) Ideal J_{sc} (EQE=1, R=0) as a function of SiGe thickness for various germanium fraction. b) PC1D model of EQE variation with Ge content for a c-Si(P++)/epi-SiGe/n-aSi:H solar cell.

To qualify the electrical properties of this low temperature epi-SiGe material, heterojunction solar cells were processed using a wafer equivalent structure with the epitaxial SiGe used as an absorber: (p++)c-Si wafer/(i)epi-$Si_{0.73}Ge_{0.27}$(1.9μm)/a-Si:H(4nm)/(n+)a-Si:H(10nm). Despite the presence of threading dislocations for such SiGe alloy composition, as seen above, a high Ge % in the absorber was chosen to get a significant absorption enhancement compared to silicon. A similar solar cell was fabricated, but with an epi-Si (1.7 μm) absorber (see Fig.4.45 scheme). The characterization of those

[154]S.A. Hadi et al., ECS Transactions, **41**: 3–14, 2011.
[155]R. Cariou et al., Solar Energy Materials and Solar Cells, **95**: 2260–2263, 2011.
[156]R. Cariou et al., SPIE proceedings, 84700B–84700B, 2012.

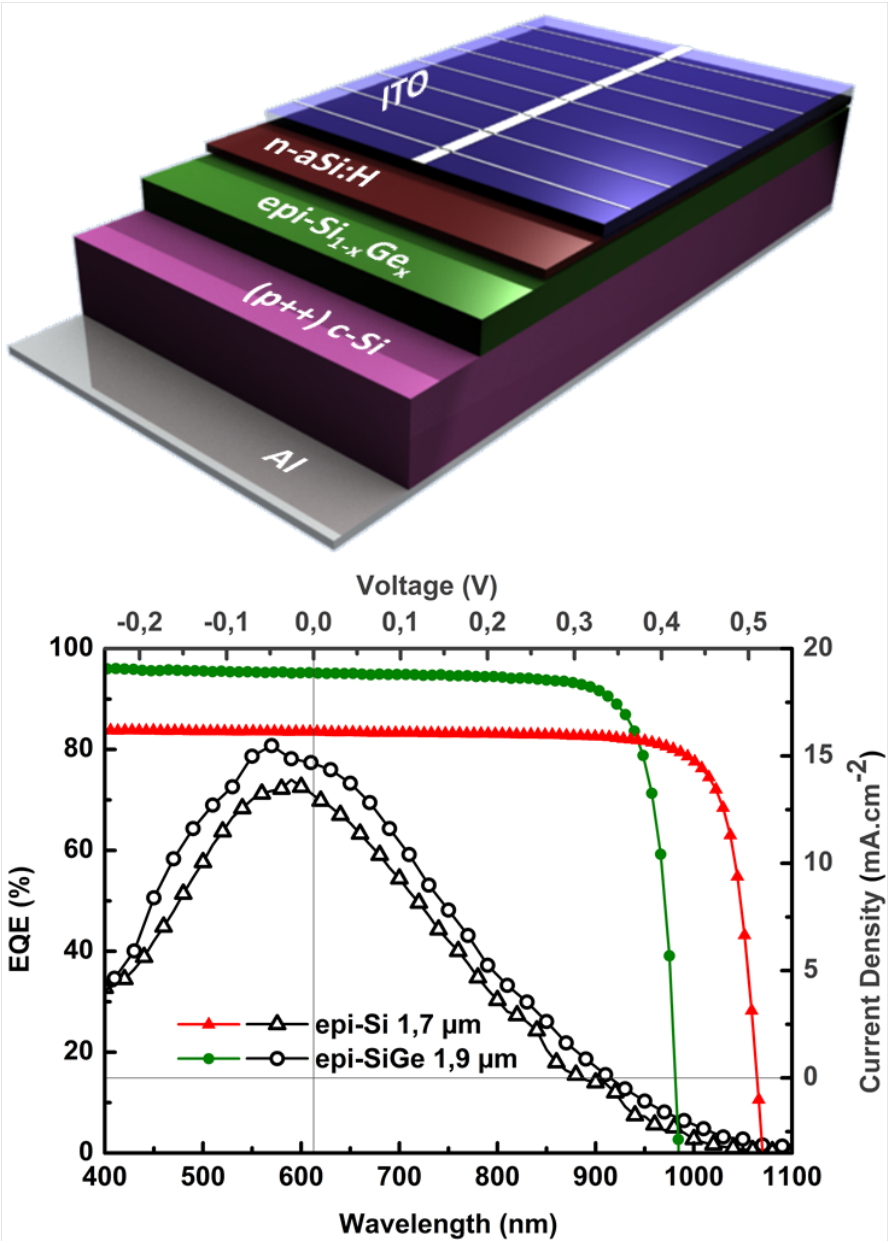


Fig. 4.45 – Left: 3D representation of c-Si(p++)/epi-SiGe/n-aSi:H PIN solar cells. Comparison of IV (top and right axis) and EQE (left and bottom axes) curves for solar cells with 2 different absorbers: 1.7μm epi-Si (triangles) and a 1.9μm epi-$Si_{\mathbf{0.73}}Ge_{\mathbf{0.27}}$ (circles). The corresponding diode parameters are listed in Tab.4.8

two solar cells are also presented in Fig.4.45: the bottom and left axis represent EQE over 400-1100 nm range, while top and right axis are for the J-V characteristics. Both cells show a high fill factor around 78%, as reported in Tab.4.8, with conversion efficiencies of 6.1% and 6.4% for SiGe and Si cells respectively.

With the assumption of no reflection losses and 100% IQE one would expect around 7 mA/cm^2 additional current in the SiGe device compared to the epi-Si one. Our results show that the current gain is limited to a 2 mA/cm2 additional current in SiGe device; this smaller increase can be partly explained by a lower crystal quality in SiGe and probably also by a smaller parasitic contribution of the c-Si wafer to the photocurrent, due to stronger absorption of SiGe. The reduction in band gap with Ge incorporation is roughly 10% in the case of relaxed alloy having 27% of Ge, thus the $\boldsymbol{V_{oc}}$ of $Si_{\mathbf{0.73}}Ge_{\mathbf{0.27}}$ should be also at least 10% lower compared to that of the epi-Si cell, that is $\sim$ 450 mV. We

obtain experimentally 416 mV; the additional decrease being most probably explained by crystalline defects such as threading dislocations. The EQE curves show higher values in the case of SiGe over the whole spectrum. While this trend is explained by a higher absorption in the long wavelength region, higher EQE in short wavelength region is likely linked to better ITO and emitter performances of the SiGe cell. By integration of EQE with solar Spectrum, short-circuit current density is calculated in both cases (see Tab.4.8), and less than 3.5% discrepancy with J-V curve is obtained.

Sample (μm)	V_{oc} (mV)	J_{sc} (mA/cm^2) I-V	EQE	FF %	Efficiency %
epi-Si 1.7μm	501	16.1	16.7	78.6	6.4
$Si_{0.73}Ge_{0.27}$ 1.9μm	416	18.8	18.7	77.5	6.1

Tab. 4.8 – Solar cell parameters measured with solar simulator and EQE set-up for thin film Si and SiGe epitaxial cells.

To sum up, by introducing a SiGe absorber, higher current and lower V_{oc} with respect to the epi-Si cell with similar thickness are obtained. Stronger absorption and band gap reduction can explain this trend; however crystal defects most probably deteriorate the SiGe cell performance. Nevertheless, a fill factor of 77.5% suggests that this material quality remains high, and defects are probably well passivated by hydrogen. To our knowledge, the 6.1% efficiency in 1.9μm epi-$Si_{0.73}Ge_{0.27}$ is state of the art results for this technology; it compares very favorably with similar solar cells deposited above 500°C or with ultra-high vacuum techniques (see Tab.4.7). Further improvement are expected if graded SiGe buffer layer is grown to even lower defect density in the absorber.

4.6 Summary and perspectives

Takeaway Message - Thin film epitaxial solar cells

- Thin film crystalline silicon solar cells are building a bridge between the world of thin film silicon and monocrystalline technologies. The c-Si cell of tomorrow is most likely <40 μm with an efficiency >20%.
- PECVD epitaxial solar cells on wafer reaching 8.8% efficiency, for a 4.2μm thick absorber, have been demonstrated. The corresponding fill factor of 80.5% is a proof of the high electrical quality of such epi-Si layers. The best diffusion length extracted from the inverse IQE reaches 20μm. In c-Si(p++)/epi-Si/n-aSi:H cells, the highly doped wafer contributes to the current up to few mA/cm^2.
- The thin c-Si absorbers (below 20μm) can accommodate much more defects and impurities: lower diffusion length, compared to thick c-Si wafers, is possible without penalizing efficiency. H-passivation effectively reduces the impact of crystalline defects (e.g. dislocations) impact. However the importance of surface passivation is greater in thinner absorber.
- The classic light trapping based on ray optics is not suitable for ultra-thin c-Si; new concepts such as plasmonic and photonics treating light as a wave are required. Nanostructures can efficiently enhance absorption in thin film c-Si by impedance matching and mode coupling effects.
- A balance between optimum optical trapping features and surface passivation quality should be found. Keeping flat interfaces for the active material and using nanopatterned dielectric media could be a solution. Experimental realization of nanostructured epitaxial and wafer based cells suggest that wet etched inverted pyramids are the best solution.
- Lift-off on PECVD epi-Si layers is necessary to process the solar cell back side and improve light trapping. PECVD epitaxy on Epifree material offers an easy lift-off approach. More interestingly, a low density epi-Si/c-Si interface layer allows epi-Si lift-off at moderate annealing temperature (300-400°C).
- In the framework of Nathisol and PhotoNvoltaics projects, PECVD epi-Si layers of few cm^2 were transferred on PDMS/Glass or directly bonded to glass. Proof of concept of transferred cells with flat interfaces was achieved.
- Epitaxial growth of Ge and SiGe were demonstrated on c-Ge and c-Si substrates. High crystal quality has been achieved and SiGe alloys with Ge content up to 35% were obtained. A record 1.9μm epi-SiGe cell with a 18.8 mA/cm^2, FF of 77.5% and 6.1% efficiency was fabricated.

References

[1] M.A. GREEN. The path to 25% silicon solar cell efficiency: History of silicon cell evolution. *Progress in Photovoltaics: Research and Applications*, **17**: 183–189, 2009. DOI: 10.1002/pip.892 (see p. 96)

[2] R.S. OHL "Light-Sensitive Electric Device" pat. 2402662 U.S. Classification: 136/261 June 1946 (see p. 96)

[3] J. ZHAO, A. WANG, and M.A. GREEN. 24.5% Efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates. *Progress in Photovoltaics: Research and Applications*, **7**: 471–474, 1999. DOI: 10.1002/(SICI)1099-159X(199911/12)7:6<471::AID-PIP298>3.0.CO;2-7 (see p. 96)

[4] M.A. GREEN, K. EMERY, Y. HISHIKAWA, and W. WARTA. Solar cell efficiency tables (version 33). *Progress in Photovoltaics: Research and Applications*, **17**: 85–94, 2009. DOI: 10.1002/pip.880 (see p. 96)

[5] M.A. GREEN, K. EMERY, Y. HISHIKAWA, W. WARTA, and E.D. DUNLOP. Solar cell efficiency tables (version 43). *Progress in Photovoltaics: Research and Applications*, **22**: 1–9, 2014. DOI: 10.1002/pip.2452 (see pp. 96, 97)

[6] W. SHOCKLEY and H.J. QUEISSER. Detailed Balance Limit of Efficiency of p-n Junction Solar Cells. *Journal of Applied Physics*, **32**: 510, 1961. DOI: 10.1063/1.1736034 (see p. 96)

[7] T. TIEDJE, E. YABLONOVITCH, G.D. CODY, and B.G. BROOKS. Limiting efficiency of silicon solar cells. *IEEE Transactions on Electron Devices*, **31**: 711–716, 1984. DOI: 10.1109/T-ED.1984.21594 (see pp. 96, 101)

[8] B. YAN, G. YUE, L. SIVEC, J. YANG, S. GUHA, and C.S. JIANG. Innovative dual function nc-SiOx:H layer leading to a >16% efficient multi-junction thin-film silicon solar cell. *Applied Physics Letters*, **99**: 113512–113512–3, 2011. DOI: 10.1063/1.3638068 (see pp. 97, 138, 148)

[9] F. DROSS, K. BAERT, T. BEARDA, JAN D., V. DEPAUW, O. EL DAIF, I. GORDON, A. GOUGAM, J. GOVAERTS, S. GRANATA, R. LABIE, X. LOOZEN, R. MARTINI, A. MASOLIN, B. O'SULLIVAN, Y. QIU, J. VAES, D. VAN GESTEL, J. VAN HOEYMISSEN, A. VANLEENHOVE, K. VAN NIEUWENHUYSEN, S. VENKATACHALAM, M. MEURIS, and J. POORTMANS. Crystalline thin-foil silicon solar cells: where crystalline quality meets thin-film processing. *Prog. Photovolt: Res. Appl.*, **20**: 770–784, 2012. DOI: 10.1002/pip.1238 (see p. 97)

[10] V. FTHENAKIS. Sustainability of photovoltaics: The case for thin-film solar cells. *Renewable and Sustainable Energy Reviews*, **13**: 2746–2750, 2009. DOI: 10.1016/j.rser.2009.05.001 (see p. 97)

[11] A. WANG, J. ZHAO, S.R. WENHAM, and M.A. GREEN. 21.5% Efficient thin silicon solar cell. *Progress in Photovoltaics: Research and Applications*, **4**: 55–58, 1996. DOI: 10.1002/(SICI)1099-159X(199601/02)4:1<55::AID-PIP111>3.0.CO;2-P (see pp. 98, 99)

[12] M. TAGUCHI, A YANO, S. TOHODA, K. MATSUYAMA, Y. NAKAMURA, T. NISHIWAKI, K. FUJITA, and E. MARUYAMA. 24.7 % Record Efficiency HIT Solar Cell on Thin Silicon Wafer. *IEEE Journal of Photovoltaics*, **4**: 96–99, 2014. DOI: 10.1109/JPHOTOV.2013.2282737 (see pp. 98, 99)

[13] S. JEONG, M.D. MCGEHEE, and Y. CUI. All-back-contact ultra-thin silicon nanocone solar cells with 13.7% power conversion efficiency. *Nature Communications*, **4**: 2013. DOI: 10.1038/ncomms3950 (see pp. 98, 99, 114, 115)

[14] S. SAHA, E.U. ONYEGAM, D. SARKAR, M.M. HILALI, R.A. RAO, L. MATHEW, D. JAWARANI, D. XU, R.S. SMITH, U.K. DAS, J.G. FOSSUM, and S.K. BANERJEE. Exfoliated 25μm Si Foil for Solar Cells with Improved Light-Trapping. *MRS Online Proceedings Library*, **1493**: 51–58, 2013. DOI: 10.1557/opl.2013.222 (see pp. 98, 99)

[15] J.L. Cruz-Campa, M. Okandan, P.J. Resnick, P. Clews, T. Pluym, R.K. Grubbs, V.P. Gupta, D. Zubia, and G.N. Nielson. Microsystems enabled photovoltaics: 14.9% efficient 14 μm thick crystalline silicon solar cell. *Solar Energy Materials and Solar Cells*, **95**: 551–558, 2011. doi: 10.1016/j.solmat.2010.09.015 (see pp. 98, 99)

[16] C. Trompoukis, O. El Daif, V. Depauw, I. Gordon, and J. Poortmans. Photonic assisted light trapping integrated in ultrathin crystalline silicon solar cells by nanoimprint lithography. *Applied Physics Letters*, **101**: 103901–103901–4, 2012. doi: doi:10.1063/1.4749810 (see pp. 98, 99, 114, 115, 122)

[17] P. Kapur, M.M. Moslehi, A. Deshpande, V. Rana, J. Kramer, S. Seutter, H. Deshazer, S. Coutant, A. Calcaterra, S. Kommera, Y. Su, D. Grupp, S. Tamilmani, D. Dutton, T. Stalcup, T. Du, and M. Wingert. A Manufacturable, Non-Plated, Non-Ag Metallization Based 20.44% Efficient, 243cm2 Area, Back Contacted Solar Cell on 40μm Thick Mono-Crystalline Silicon. *28th EU PVSEC Proceedings*, **3DO.7.6**: 2228 –2231, 2013. doi: 10.4229/28thEUPVSEC2013-3DO.7.6 (see pp. 98, 99, 122)

[18] J.H. Petermann, D. Zielke, J. Schmidt, F. Haase, E.G. Rojas, and R. Brendel. 19%-efficient and 43 μm-thick crystalline Si solar cell from layer transfer using porous silicon. *Progress in Photovoltaics: Research and Applications*, **20**: 1–5, 2012. doi: 10.1002/pip.1129 (see pp. 98, 99, 107, 122)

[19] M. Reuter, W. Brendle, O. Tobail, and J.H. Werner. 50 μm thin solar cells with 17.0% efficiency. *Solar Energy Materials and Solar Cells*, **93**: 704–706, 2009. doi: 10.1016/j.solmat.2008.09.035 (see pp. 98, 99, 107, 122)

[20] R.B. Bergmann, C. Berge, T.J. Rinke, J. Schmidt, and J.H. Werner. Advances in monocrystalline Si thin film solar cells by layer transfer. *Solar Energy Materials and Solar Cells*, **74**: 213–218, 2002. doi: 10.1016/S0927-0248(02)00070-3 (see pp. 98, 99, 122)

[21] P. Rosenits, F. Kopp, and S. Reber. Epitaxially grown crystalline silicon thin-film solar cells reaching 16.5% efficiency with basic cell process. *Thin Solid Films*, **519**: 3288–3290, 2011. doi: 10.1016/j.tsf.2010.12.150 (see pp. 98, 99)

[22] I. Kuzma-Filipek, F. Dross, K. Baert, J.L. Hernandez, S. Singh, K. Van Nieuwenhuysen, and J. Poortmans. >16% thin-film epitaxial silicon solar cells on 70-cm2 area with 30-μm active layer, porous silicon back reflector, and Cu-based top-contact metallization. *Progress in Photovoltaics: Research and Applications*, **20**: 350–355, 2012. doi: 10.1002/pip.1146 (see pp. 98, 99)

[23] K. Van Nieuwenhuysen, M. RÃl'caman Payo, I. Kuzma-Filipek, J. Van Hoeymissen, G. Beaucarne, and J. Poortmans. Epitaxially grown emitters for thin film silicon solar cells result in 16% efficiency. *Thin Solid Films*, **518**: S80–S82, 2010. doi: 10.1016/j.tsf.2009.10.061 (see pp. 98, 99)

[24] H.M. Branz, C.W. Teplin, M.J. Romero, I.T. Martin, Q. Wang, K. Alberi, D.L. Young, and P. Stradins. Hot-wire chemical vapor deposition of epitaxial film crystal silicon for photovoltaics. *Thin Solid Films*, **519**: 4545–4550, 2011. doi: 10.1016/j.tsf.2011.01.335 (see pp. 98, 99, 105)

[25] K. Alberi, I.T. Martin, M. Shub, C.W. Teplin, M.J. Romero, R.C. Reedy, E. Iwaniczko, A. Duda, P. Stradins, H.M. Branz, and D.L. Young. Material quality requirements for efficient epitaxial film silicon solar cells. *Applied Physics Letters*, **96**: 073502, 2010. doi: 10.1063/1.3309751 (see pp. 98, 103, 106, 108)

[26] R. Cariou, I. Massiot, R. Ruggeri, N. Ramay, J. Tang, A. Cattoni, S. Collin, J. Nassar, and P. Roca i Cabarrocas. Low Temperature Epitaxial Growth of Si and SiGe and Their Transfer to Foreign Substrate. *28th EU PVSEC Proceedings*, **3DO.7.5**: 2225 –2227, 2013. doi: 10.4229/28thEUPVSEC2013-3DO.7.5 (see pp. 98, 99)

[27] E. YABLONOVITCH. Statistical ray optics. *Journal of the Optical Society of America*, **72**: 899–907, 1982. DOI: 10.1364/JOSA.72.000899 (see p. 99)

[28] P. SHENG. Optical absorption of thin film on a Lambertian reflector substrate. *IEEE Transactions on Electron Devices*, **31**: 634–636, 1984. DOI: 10.1109/T-ED.1984.21582 (see p. 100)

[29] M.A. GREEN. Lambertian light trapping in textured solar cells and light-emitting diodes: analytical solutions. *Progress in Photovoltaics: Research and Applications*, **10**: 235–241, 2002. DOI: 10.1002/pip.404 (see p. 100)

[30] H.A. ATWATER and A. POLMAN. Plasmonics for improved photovoltaic devices. *Nature Materials*, **9**: 205–213, 2010. DOI: 10.1038/nmat2629 (see pp. 100, 113–115)

[31] Z. YU, A. RAMAN, and S. FAN. Fundamental limit of light trapping in grating structures. *Opt. Express*, **18**: A366–A380, 2010. DOI: 10.1364/OE.18.00A366 (see pp. 100, 114)

[32] A. POLMAN and H.A. ATWATER. Photonic design principles for ultrahigh-efficiency photovoltaics. *Nature Materials*, **11**: 174–177, 2012. DOI: 10.1038/nmat3263 (see pp. 100, 113)

[33] A. BOZZOLA, M. LISCIDINI, and L.C. ANDREANI. Photonic light-trapping versus Lambertian limits in thin film silicon solar cells with 1D and 2D periodic patterns. *Opt. Express*, **20**: A224–A244, 2012. DOI: 10.1364/OE.20.00A224 (see p. 100)

[34] K. MAKI, D. FUJISHIMA, H. INOUE, Y. TSUNOMURA, T. ASAUMI, S. TAIRA, T. KINOSHITA, M. TAGUCHI, H. SAKATA, H. KANNO, and E. MARUYAMA. High-efficiency HIT solar cells with a very thin structure enabling a high Voc. *37th IEEE Photovoltaic Specialists Conference (PVSC)*, 000057–000061, 2011. DOI: 10.1109/PVSC.2011.6185845 (see p. 101)

[35] P. ROCA I CABARROCAS. A fully automated hot-wall multiplasma-monochamber reactor for thin film deposition. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, **9**: 2331, 1991. DOI: 10.1116/1.577318 (see pp. 101, 130, 142)

[36] M. LABRUNE. *Silicon surface passivation and epitaxial growth on c-Si by low temperature plasma processes for high efficiency solar cells*. PhD thesis. Ecole Polytechnique, France, May 2011. (see pp. 102, 144)

[37] D.E. ASPNES and A.A. STUDNA. Dielectric functions and optical parameters of Si, Ge, GaP, GaAs, GaSb, InP, InAs, and InSb from 1.5 to 6.0 eV. *Physical Review B*, **27**: 985, 1983. DOI: 10.1103/PhysRevB.27.985 (see pp. 103, 140, 144)

[38] G.E. JELLISON JR., V.I. MERKULOV, A.A. PURETZKY, D.B. GEOHEGAN, G. ERES, D.H. LOWNDES, and J.B. CAUGHMAN. Characterization of thin-film amorphous semiconductors using spectroscopic ellipsometry. *Thin Solid Films*, **377-378**: 68–73, 2000. DOI: 10.1016/S0040-6090(00)01384-5 (see p. 103)

[39] D.A.G. BRUGGEMAN. Berechnung verschiedener physikalischer Konstanten von heterogenen Substanzen. I. Dielektrizitätskonstanten und Leitfähigkeiten der Mischkörper aus isotropen Substanzen. *Annalen der Physik*, **416**: 636–664, 1935. DOI: 10.1002/andp.19354160705 (see p. 103)

[40] H.J. LEAMY. Charge collection scanning electron microscopy. *Journal of Applied Physics*, **53**: R51–R80, 1982. DOI: 10.1063/1.331667 (see p. 103)

[41] C.W. TEPLIN, K. ALBERI, M. SHUB, C. BEALL, I.T. MARTIN, M.J. ROMERO, D.L. YOUNG, R.C. REEDY, P. STRADINS, and H.M. BRANZ. Mechanisms controlling the phase and dislocation density in epitaxial silicon films grown from silane below 800°C. *Applied Physics Letters*, **96**: 201901–201901–3, 2010. DOI: doi:10.1063/1.3422474 (see p. 103)

[42] X.L. YUAN, T. SEKIGUCHI, S.G. RI, and S. ITO. Detection of misfit dislocations at interface of strained Si/Si0.8Ge0.2 by electron-beam-induced current technique. *Applied Physics Letters*, **84**: 3316–3318, 2004. DOI: 10.1063/1.1734688 (see p. 103)

[43] K. Alberi, H.M. Branz, H. Guthrey, M.J. Romero, I.T. Martin, C.W. Teplin, P. Stradins, and D.L. Young. Dislocation-limited open circuit voltage in film crystal silicon solar cells. *Applied Physics Letters*, **101**: 123510, 2012. doi: 10.1063/1.4754142 (see pp. 103, 104)

[44] J. Damon-Lacoste and P. Roca i Cabarrocas. Toward a better physical understanding of a-Si:H/c-Si heterojunction solar cells. *Journal of Applied Physics*, **105**: 063712, 2009. doi: 10.1063/1.3091283 (see p. 103)

[45] M. Wolf and H. Rauschenbach. Series resistance effects on solar cell measurements. *Advanced Energy Conversion*, **3**: 455–479, 1963. doi: 10.1016/0365-1789(63)90063-8 (see p. 105)

[46] S. Suckow, T. M. Pletzer, and H. Kurz. Fast and reliable calculation of the two-diode model without simplifications. *Progress in Photovoltaics: Research and Applications*, **22**: 494–501, 2014. doi: 10.1002/pip.2301 (see p. 105)

[47] A. Ortiz-Conde, F.J. Garcia Sanchez, and J. Muci. Exact analytical solutions of the forward non-ideal diode equation with series and shunt parasitic resistances. *Solid-State Electronics*, **44**: 1861–1864, 2000. doi: 10.1016/S0038-1101(00)00132-5 (see p. 105)

[48] P.A. Basore. Extended spectral analysis of internal quantum efficiency. *33th IEEE Photovoltaic Specialists Conference (PVSC)*, 147–152, 1993. doi: 10.1109/PVSC.1993.347063 (see p. 107)

[49] M. Hirsch, U. Rau, and J.H. Werner. Analysis of internal quantum efficiency and a new graphical evaluation scheme. *Solid-State Electronics*, **38**: 1009–1015, 1995. doi: 10.1016/0038-1101(95)98669-T (see p. 107)

[50] J.H. Werner, S. Kolodinski, U. Rau, J.K. Arch, and E. Bauser. Silicon solar cell of 16.8 μm thickness and 14.7% efficiency. *Applied Physics Letters*, **62**: 2998–3000, 1993. doi: 10.1063/1.109169 (see p. 107)

[51] S.-Y. Lien and D.-S. Wuu. Simulation and fabrication of heterojunction silicon solar cells from numerical computer and hot-wire CVD. *Progress in Photovoltaics: Research and Applications*, **17**: 489–501, 2009. doi: 10.1002/pip.900 (see p. 108)

[52] S. Chakraborty, R. Cariou, M. Labrune, P. Roca i Cabarrocas, and P. Chatterjee. Feasibility of using thin crystalline silicon films epitaxially grown at 165 °C in solar cells: A computer simulation study. *EPJ Photovoltaics*, **4**: 45103, 2013. doi: 10.1051/epjpv/2013014 (see pp. 110–112)

[53] P. Chatterjee, F. Leblanc, M. Favre, and J. Perrin. A Global Electricai-Optical Model of Thin Film Solar Cells on Textured Substrates. *MRS Online Proceedings Library*, **426**: null, 1996. doi: 10.1557/PROC-426-593 (see p. 110)

[54] M. Nath, P. Chatterjee, J. Damon-Lacoste, and P. Roca i Cabarrocas. Criteria for improved open-circuit voltage in a-Si:H(N)/c-Si(P) front heterojunction with intrinsic thin layer solar cells. *Journal of Applied Physics*, **103**: 034506, 2008. doi: 10.1063/1.2838459 (see p. 110)

[55] P.J. McElheny, J.K. Arch, H.-S. Lin, and S.J. Fonash. Range of validity of the surface-photovoltage diffusion length measurement: A computer simulation. *Journal of Applied Physics*, **64**: 1254–1265, 1988. doi: 10.1063/1.341843 (see p. 110)

[56] D.J. Aiken. High performance anti-reflection coatings for broadband multi-junction solar cells. *Solar Energy Materials and Solar Cells*, **64**: 393–404, 2000. doi: 10.1016/S0927-0248(00)00253-1 (see p. 113)

[57] R.A. Pala, J. White, E. Barnard, J. Liu, and M.L. Brongersma. Design of Plasmonic Thin-Film Solar Cells with Broadband Absorption Enhancements. *Advanced Materials*, **21**: 3504–3509, 2009. doi: 10.1002/adma.200900331 (see p. 113)

[58] D.M. CALLAHAN, J.N. MUNDAY, and H.A. ATWATER. Solar Cell Light Trapping beyond the Ray Optic Limit. *Nano Lett.*, **12**: 214–218, 2012. DOI: 10.1021/nl203351k (see p. 114)

[59] C. WANG, S. YU, W. CHEN, and C. SUN. Highly Efficient Light-Trapping Structure Design Inspired By Natural Evolution. *Scientific Reports*, **3**: 2013. DOI: 10.1038/srep01025 (see p. 114)

[60] X. MENG, E. DROUARD, G. GOMARD, R. PERETTI, A. FAVE, and C. SEASSAL. Combined front and back diffraction gratings for broad band light trapping in thin film solar cell. *Opt. Express*, **20**: A560–A571, 2012. DOI: 10.1364/OE.20.00A560 (see p. 114)

[61] K. X. WANG, Z. YU, V. LIU, Y. CUI, and S. FAN. Absorption Enhancement in Ultrathin Crystalline Silicon Solar Cells with Antireflection and Light-Trapping Nanocone Gratings. *Nano Letters*, **12**: 1616–1619, 2012. DOI: 10.1021/nl204550q (see pp. 114, 115)

[62] I. MASSIOT, C. COLIN, N. P*é*R*é*-LAPERNE, P. ROCA I CABARROCAS, C. SAUVAN, P. LALANNE, J.-L. PELOUARD, and S. COLLIN. Nanopatterned front contact for broadband absorption in ultra-thin amorphous silicon solar cells. *Applied Physics Letters*, **101**: 163901, 2012. DOI: 10.1063/1.4758468 (see pp. 114, 115)

[63] E.R. MARTINS, J. LI, Y. LIU, V. DEPAUW, Z. CHEN, J. ZHOU, and T.F. KRAUSS. Deterministic quasi-random nanostructures for photon control. *Nature Communications*, **4**: 2665, 2013. DOI: 10.1038/ncomms3665 (see pp. 114, 115)

[64] C. TROMPOUKIS, I. ABDO, R. CARIOU, I. COSME, W. CHEN, O. DEPARIS, A. DMITRIEV, E. DROUARD, M. FOLDYNA, E.G. CAUREL, I. GORDON, B. HEIDARI, A. HERMAN, L. LALOUAT, K.-D. LEE, J. LIU, K. LODEWIJKS, F. MANDORLO, I. MASSIOT, A. MAYER, V. MIJKOVIC, J. MULLER, R. OROBTCHOUK, G. POULAIN, P. PROD'HOMME, P. ROCA I CABARROCAS, C. SEASSAL, J. POORTMANS, R. MERTENS, O. EL DAIF, and V. DEPAUW. Photonic nanostructures for advanced light trapping in thin crystalline silicon solar cells. *Phys. Status Solidi A*, 2014. DOI: 10.1002/pssa.201431180 (see pp. 114–116)

[65] J. OH, H.-C. YUAN, and H.M. BRANZ. An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures. *Nature Nanotechnology*, **7**: 743–748, 2012. DOI: 10.1038/nnano.2012.166 (see pp. 114, 115)

[66] J.H. ATWATER, P. SPINELLI, E. KOSTEN, J. PARSONS, C.V. LARE, J.V.D. GROEP, J.G.D. ABAJO, A. POLMAN, and H.A. ATWATER. Microphotonic parabolic light directors fabricated by two-photon lithography. *Applied Physics Letters*, **99**: 151113, 2011. DOI: 10.1063/1.3648115 (see pp. 114, 115)

[67] EMILY D. KOSTEN, JACKSON H. ATWATER, JAMES PARSONS, ALBERT POLMAN, and HARRY A. ATWATER. Highly efficient GaAs solar cells by limiting light emission angle. *Light: Science & Applications*, **2**: e45, 2013. DOI: 10.1038/lsa.2013.1 (see pp. 114, 115)

[68] Y. YAO, J. YAO, V.K. NARASIMHAN, Z. RUAN, C. XIE, S. FAN, and Y. CUI. Broadband light management using low-Q whispering gallery modes in spherical nanoshells. *Nature Communications*, **3**: 664, 2012. DOI: 10.1038/ncomms1664 (see pp. 114, 115)

[69] X. LIU, P.R. COXON, M. PETERS, B. HOEX, J.M. COLE, and D.J. FRAY. Black silicon: fabrication methods, properties and solar energy applications. *Energy & Environmental Science*, 2014. DOI: 10.1039/C4EE01152J (see p. 114)

[70] C. TROMPOUKIS, O. EL DAIF, P. PRATIM SHARMA, H. SIVARAMAKRISHNAN RADHAKRISHNAN, M. DEBUCQUOY, V. DEPAUW, K. VAN NIEUWENHUYSEN, I. GORDON, R. MERTENS, and J. POORTMANS. Passivation of photonic nanostructures for crystalline silicon solar cells. *Progress in Photovoltaics: Research and Applications*, 2014. DOI: 10.1002/pip.2489 (see pp. 114, 119)

[71] M. Otto, M. Kroll, T. Kasebier, R. Salzer, A. Tunnermann, and R.B. Wehrspohn. Extremely low surface recombination velocities in black silicon passivated by atomic layer deposition. *Applied Physics Letters*, **100**: 191603–191603–4, 2012. doi: doi:10.1063/1.4714546 (see p. 114)

[72] A. Oskooi, P.A. Favuzzi, Y. Tanaka, H. Shigeta, Y. Kawakami, and S. Noda. Partially disordered photonic-crystal thin films for enhanced and robust photovoltaics. *Applied Physics Letters*, **100**: 181110, 2012. doi: 10.1063/1.4711144 (see p. 115)

[73] E.R. Martins, J. Li, Y. Liu, J. Zhou, and T.F. Krauss. Engineering gratings for light trapping in photovoltaics: The supercell concept. *Physical Review B*, **86**: 041404, 2012. doi: 10.1103/PhysRevB.86.041404 (see p. 115)

[74] F. Pratesi, M. Burresi, F. Riboli, K. Vynck, and D.S. Wiersma. Disordered photonic structures for light harvesting in solar cells. *Opt. Express*, **21**: A460–A468, 2013. doi: 10.1364/OE.21.00A460 (see p. 115)

[75] P. Krogstrup, H.I. Jorgensen, M. Heiss, O. Demichel, J.V. Holm, M. Aagesen, J. Nygard, and A. Fontcuberta i Morral. Single-nanowire solar cells beyond the Shockley-Queisser limit. *Nat Photon*, **7**: 306–310, 2013. doi: 10.1038/nphoton.2013.32 (see p. 115)

[76] P.-J. Alet, L. Yu, G. Patriarche, S. Palacin, and P. Roca i Cabarrocas. In situ generation of indium catalysts to grow crystalline silicon nanowires at low temperature on ITO. *J. Mater. Chem.*, **18**: 5187–5189, 2008. doi: 10.1039/B813046A (see p. 115)

[77] L. Yu, B. O'Donnell, J.-L. Maurice, and P. Roca i Cabarrocas. Core-shell structure and unique faceting of Sn-catalyzed silicon nanowires. *Applied Physics Letters*, **97**: 023107, 2010. doi: 10.1063/1.3464557 (see p. 115)

[78] B. O'Donnell, L. Yu, M. Foldyna, and P. Roca i Cabarrocas. Silicon nanowire solar cells grown by PECVD. *Journal of Non-Crystalline Solids*, **358**: 2299–2302, 2012. doi: 10.1016/j.jnoncrysol.2011.11.026 (see p. 115)

[79] S. Misra, L. Yu, M. Foldyna, and P. Roca i Cabarrocas. High efficiency and stable hydrogenated amorphous silicon radial junction solar cells built on VLS-grown silicon nanowires. *Solar Energy Materials and Solar Cells*, **118**: 90–95, 2013. doi: 10.1016/j.solmat.2013.07.036 (see p. 115)

[80] S. Jain, V. Depauw, V.D. Miljkovic, A. Dmitriev, C. Trompoukis, I. Gordon, P. Van Dorpe, and O. El Daif. Broadband absorption enhancement in ultra-thin crystalline Si solar cells by incorporating metallic and dielectric nanostructures in the back reflector. *Progress in Photovoltaics: Research and Applications*, 2014. doi: 10.1002/pip.2533 (see p. 116)

[81] B.G. Lee, P. Stradins, D.L. Young, K. Alberi, T.-K. Chuang, J.G. Couillard, and H.M. Branz. Light trapping by a dielectric nanoparticle back reflector in film silicon solar cells. *Applied Physics Letters*, **99**: 064101, 2011. doi: 10.1063/1.3615796 (see p. 116)

[82] P. Spinelli, B. Macco, M.A. Verschuuren, W.M.M. Kessels, and A. Polman. Al_2O_3/TiO_2 nano-pattern antireflection coating with ultralow surface recombination. *Applied Physics Letters*, **102**: 233902, 2013. doi: 10.1063/1.4810970 (see p. 116)

[83] I. Massiot. *Design and fabrication of nanostructures for light-trapping in ultra-thin solar cells*. PhD thesis. Université Paris Sud - Paris XI, Oct. 2013. (see p. 116)

[84] L.J. Guo. Nanoimprint Lithography: Methods and Material Requirements. *Advanced Materials*, **19**: 495–513, 2007. doi: 10.1002/adma.200600882 (see p. 116)

[85] A.W. Stephens, A.G. Aberle, and M.A. Green. Surface recombination velocity measurements at the siliconâĂŞsilicon dioxide interface by microwave-detected photoconductance decay. *Journal of Applied Physics*, **76**: 363, 1994. doi: doi:10.1063/1.357082 (see p. 118)

[86] A.B. SPROUL. Dimensionless solution of the equation describing the effect of surface recombination on carrier decay in semiconductors. *Journal of Applied Physics*, **76**: 2851, 1994. DOI: doi:10.1063/1.357521 (see p. 118)

[87] S.T. PANTELIDES and F.A. REBOREDO. Hydrogen Platelets in Crystalline Silicon - Precursors for the 'Smart Cut'. *Solid State Phenomena*, **69-70**: 83–92, 1999. DOI: 10.4028/www.scientific.net/SSP.69-70.83 (see p. 121)

[88] Y. ZHENG, S.S. LAU, T. HOCHBAUER, A. MISRA, R. VERDA, X.-M. HE, M. NASTASI, and J.W. MAYER. Orientation dependence of blistering in H-implanted Si. *Journal of Applied Physics*, **89**: 2972–2978, 2001. DOI: 10.1063/1.1334921 (see p. 121)

[89] T. HOCHBAUER, A. MISRA, M. NASTASI, and J.W. MAYER. Physical mechanisms behind the ion-cut in hydrogen implanted silicon. *Journal of Applied Physics*, **92**: 2335–2342, 2002. DOI: 10.1063/1.1494844 (see p. 121)

[90] X. HEBRAS, P. NGUYEN, K.K. BOURDELLE, F. LETERTRE, N. CHERKASHIN, and A. CLAVERIE. Comparison of platelet formation in hydrogen and helium-implanted silicon. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, **262**: 24–28, 2007. DOI: 10.1016/j.nimb.2007.04.158 (see p. 121)

[91] M. BRUEL *Process for manufacturing thin film layers of semiconductor material* EP Patent App. EP19,920,402,520 1993 (see p. 121)

[92] M. BRUEL, B. ASPAR, and A.-J. AUBERTON-HERVE. Smart-Cut: A New Silicon On Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding[*1]. *Japanese Journal of Applied Physics*, **36**: 1636–1641, 1997. DOI: 10.1143/JJAP.36.1636 (see p. 121)

[93] R.A. RAO, L. MATHEW, S. SAHA, S. SMITH, D. SARKAR, R. GARCIA, R. STOUT, A. GURMU, E. ONYEGAM, D. AHN, D. XU, D. JAWARANI, J. FOSSUM, and S. BANERJEE. A novel low cost 25 μm thin exfoliated monocrystalline Si solar cell technology. *37th IEEE Photovoltaic Specialists Conference (PVSC)*, 001504 –001507, 2011. DOI: 10.1109/PVSC.2011.6186244 (see p. 121)

[94] F. DROSS, J. ROBBELEIN, B. VANDEVELDE, E. VAN KERSCHAVER, I. GORDON, G. BEAUCARNE, and J. POORTMANS. Stress-induced large-area lift-off of crystalline Si films. *Applied Physics A*, **89**: 149–152, 2007. DOI: 10.1007/s00339-007-4195-2 (see p. 122)

[95] I. GORDON, F. DROSS, V. DEPAUW, A. MASOLIN, Y. QIU, J. VAES, D. VAN GESTEL, and J. POORTMANS. Three novel ways of making thin-film crystalline-silicon layers on glass for solar cell applications. *Solar Energy Materials and Solar Cells*, **95, Supplement 1**: S2–S7, 2011. DOI: 10.1016/j.solmat.2010.11.031 (see p. 122)

[96] S.W. BEDELL, D. SHAHRJERDI, B. HEKMATSHOAR, K. FOGEL, P.A. LAURO, J.A. OTT, N. SOSA, and D. SADANA. Kerf-Less Removal of Si, Ge, and III-V Layers by Controlled Spalling to Enable Low-Cost PV Technologies. *IEEE Journal of Photovoltaics*, **2**: 141 –147, 2012. DOI: 10.1109/JPHOTOV.2012.2184267 (see p. 122)

[97] S.W. BEDELL, K. FOGEL, P. LAURO, D. SHAHRJERDI, J.A. OTT, and D. SADANA. Layer transfer by controlled spalling. *Journal of Physics D: Applied Physics*, **46**: 152002, 2013. DOI: 10.1088/0022-3727/46/15/152002 (see p. 122)

[98] DAVOOD SHAHRJERDI and STEPHEN W. BEDELL. Extremely Flexible Nanoscale Ultrathin Body Silicon Integrated Circuits on Plastic. *Nano Letters*, 2012. DOI: 10.1021/nl304310x (see p. 122)

[99] D. SHAHRJERDI, S.W. BEDELL, C. BAYRAM, C.C. LUBGUBAN, K. FOGEL, P. LAURO, J.A. OTT, M. HOPSTAKEN, M. GAYNESS, and D. SADANA. Ultralight High-Efficiency Flexible InGaP/(In)GaAs Tandem Solar Cells on Plastic. *Advanced Energy Materials*, **3**: 566–571, 2013. DOI: 10.1002/aenm.201200827 (see p. 122)

[100] C.S. Solanki, R.R. Bilyalov, J. Poortmans, J. Nijs, and R. Mertens. Porous silicon layer transfer processes for solar cells. *Solar Energy Materials and Solar Cells*, **83**: 101–113, 2004. doi: 10.1016/j.solmat.2004.02.016 (see p. 122)

[101] V. Depauw, I. Gordon, G. Beaucarne, J. Poortmans, R. Mertens, and J.-P. Celis. Large-area monocrystalline silicon thin films by annealing of macroporous arrays: Understanding and tackling defects in the material. *Journal of Applied Physics*, **106**: 033516–033516–10, 2009. doi: doi:10.1063/1.3183942 (see pp. 122, 123)

[102] V. Depauw, Y. Qiu, K. Van Nieuwenhuysen, I. Gordon, and J. Poortmans. Epitaxy-free monocrystalline silicon thin film: first steps beyond proof-of-concept solar cells. *Progress in Photovoltaics: Research and Applications*, **19**: 844–850, 2011. doi: 10.1002/pip.1048 (see p. 122)

[103] D. Hernàndez, T. Trifonov, M. Garìn, and R. Alcubilla. "Silicon millefeuille": From a silicon wafer to multiple thin crystalline films in a single step. *Applied Physics Letters*, **102**: 172102–172102–4, 2013. doi: doi:10.1063/1.4803009 (see p. 122)

[104] M. Moreno and P. Roca i Cabarrocas. Ultra-thin crystalline silicon films produced by plasma assisted epitaxial growth on silicon wafers and their transfer to foreign substrates. *EPJ Photovoltaics*, **1**: 6, 2010. doi: 10.1051/epjpv/2010001 (see pp. 122, 124, 131)

[105] M. Moreno, G. Patriarche, and P. Roca i Cabarrocas. Fine-tuning of the interface in high-quality epitaxial silicon films deposited by plasma-enhanced chemical vapor deposition at 200°C. *Journal of Materials Research*, **28**: 1626–1632, 2013. doi: 10.1557/jmr.2013.52 (see pp. 122, 124)

[106] S.J. Pennycook. Z-contrast stem for materials science. *Ultramicroscopy*, **30**: 58–69, 1989. doi: 10.1016/0304-3991(89)90173-3 (see p. 127)

[107] P.D. Nellist and S.J. Pennycook. The principles and interpretation of annular dark-field Z-contrast imaging. *Advances in Imaging and Electron Physics*, **Volume 113**: 147–203, 2000. doi: 10.1016/S1076-5670(00)80013-0 (see p. 127)

[108] Z.W. Wang, Z.Y. Li, S.J. Park, A. Abdela, D. Tang, and R.E. Palmer. Quantitative Z-contrast imaging in the scanning transmission electron microscope with size-selected clusters. *Physical Review B*, **84**: 073408, 2011. doi: 10.1103/PhysRevB.84.073408 (see p. 127)

[109] P. Roca i Cabarrocas and M. Moreno "Method for producing a multilayer film including at least one ultrathin layer of crystalline silicon, and devices obtained by means of said method" pat. US20120208358 A1 (see p. 132)

[110] T.M.H. Lee, D.H.Y. Lee, C.Y.N. Liaw, A.I.K. Lao, and I.-M. Hsing. Detailed characterization of anodic bonding process between glass and thin-film coated silicon substrates. *Sensors and Actuators A: Physical*, **86**: 103–107, 2000. doi: 10.1016/S0924-4247(00)00418-0 (see p. 133)

[111] J. Wei, H. Xie, M.L. Nai, C.K. Wong, and L.C. Lee. Low temperature wafer anodic bonding. *Journal of Micromechanics and Microengineering*, **13**: 217, 2003. doi: 10.1088/0960-1317/13/2/308 (see p. 133)

[112] W. Guter, J. Schoone, S.P. Philipps, M. Steiner, G. Siefer, A. Wekkeli, E. Welser, E. Oliva, A.W. Bett, and F. Dimroth. Current-matched triple-junction solar cell reaching 41.1% conversion efficiency under concentrated sunlight. *Applied Physics Letters*, **94**: 223504, 2009. doi: 10.1063/1.3148341 (see pp. 138, 139)

[113] E.V. Johnson, G. Patriarche, and P. Roca i Cabarrocas. Directional growth of Ge on GaAs at 175° using plasma-generated nanocrystals. *Applied Physics Letters*, **92**: 103108, 2008. doi: 10.1063/1.2895636 (see pp. 138, 140, 146)

[114] M. LABRUNE, X. BRIL, G. PATRIARCHE, L. LARGEAU, O. MAUGUIN, and P. ROCA I CABARROCAS. Epitaxial growth of silicon and germanium on (100)-oriented crystalline substrates by RF PECVD at 175 ÂřC. *EPJ Photovoltaics*, **3**: 30303, 2012. DOI: 10.1051/epjpv/2012010 (see pp. 138, 140)

[115] J. BARDEEN and W.H. BRATTAIN. The Transistor, A Semi-Conductor Triode. *Physical Review*, **74**: 230–231, 1948. DOI: 10.1103/PhysRev.74.230 (see p. 139)

[116] N.E. POSTHUMA, J. VAN DER HEIDE, G. FLAMAND, and J. POORTMANS. Emitter Formation and Contact Realization by Diffusion for Germanium Photovoltaic Devices. *IEEE Transactions on Electron Devices*, **54**: 1210–1215, 2007. DOI: 10.1109/TED.2007.894610 (see p. 139)

[117] G. MANNINO, C. SPINELLA, R. RUGGERI, A. LA MAGNA, G. FISICARO, E. FAZIO, F. NERI, and V. PRIVITERA. Crystallization of implanted amorphous silicon during millisecond annealing by infrared laser irradiation. *Applied Physics Letters*, **97**: 022107–022107–3, 2010. DOI: doi:10.1063/1.3459959 (see p. 140)

[118] F. VEGA, R. SERNA, C.N. AFONSO, D. BERMEJO, and G. TEJEDA. Relaxation and crystallization kinetics of amorphous germanium films by nanosecond laser pulses. *Journal of Applied Physics*, **75**: 7287–7291, 1994. DOI: doi:10.1063/1.356663 (see p. 140)

[119] T. SAMESHIMA, H. WATAKABE, H. KANNO, T. SADOH, and M. MIYAO. Pulsed laser crystallization of silicon-germanium films. *Thin Solid Films*, **487**: 67–71, 2005. DOI: 10.1016/j.tsf.2005.01.037 (see p. 140)

[120] G. FISICARO, A. LA MAGNA, G. PICCITTO, and V. PRIVITERA. Laser annealing of SiGe and Ge based devices. *Microelectronic Engineering*, **88**: 488–491, 2011. DOI: 10.1016/j.mee.2010.09.014 (see p. 140)

[121] M. BOSI and G. ATTOLINI. Germanium: Epitaxy and its applications. *Progress in Crystal Growth and Characterization of Materials*, **56**: 146–174, 2010. DOI: 10.1016/j.pcrysgrow.2010.09.002 (see p. 140)

[122] R. GINIGE, B. CORBETT, M. MODREANU, C. BARRETT, J. HILGARTH, G. ISELLA, D. CHRASTINA, and H.V. KÃD'NEL. Characterization of Ge-on-Si virtual substrates and single junction GaAs solar cells. *Semiconductor Science and Technology*, **21**: 775–780, 2006. DOI: 10.1088/0268-1242/21/6/011 (see p. 140)

[123] J.M. HARTMANN, A.M. PAPON, V. DESTEFANIS, and T. BILLON. Reduced pressure chemical vapor deposition of Ge thick layers on Si(0 0 1), Si(0 1 1) and Si(1 1 1). *Journal of Crystal Growth*, **310**: 5287–5296, 2008. DOI: 10.1016/j.jcrysgro.2008.08.062 (see p. 140)

[124] E.A. FITZGERALD, Y.-H. XIE, D. MONROE, P.J. SILVERMAN, J.M. KUO, A.R. KORTAN, F.A. THIEL, and B.E. WEIR. Relaxed Ge_xSi_{1x} structures for III-V integration with Si and high mobility two-dimensional electron gases in Si. *Journal of Vacuum Science & Technology B*, **10**: 1807–1819, 1992. DOI: 10.1116/1.586204 (see p. 140)

[125] Y.H. TAN and C.S. TAN. Growth and characterization of germanium epitaxial film on silicon (001) using reduced pressure chemical vapor deposition. *Thin Solid Films*, **520**: 2711–2716, 2012. DOI: 10.1016/j.tsf.2011.11.046 (see pp. 140, 147)

[126] S. RIVILLON, Y.J. CHABAL, F. AMY, and A. KAHN. Hydrogen passivation of germanium (100) surface using wet chemical preparation. *Applied Physics Letters*, **87**: 253101, 2005. DOI: 10.1063/1.2142084 (see p. 141)

[127] R. CARIOU, R. RUGGERI, X. TAN, GIOVANNI MANNINO, J. NASSAR, and P. ROCA I CABARROCAS. Structural properties of relaxed thin film germanium layers grown by low temperature RF-PECVD epitaxy on Si and Ge (100) substrates. *AIP Advances*, **4**: 077103, 2014. DOI: 10.1063/1.4886774 (see p. 142)

[128] H.-C. Luan, D.R. Lim, K.K. Lee, K.M. Chen, J.G. Sandland, K. Wada, and L.C. Kimerling. High-quality Ge epilayers on Si with low threading-dislocation densities. *Applied Physics Letters*, **75**: 2909–2911, 1999. doi: doi:10.1063/1.125187 (see pp. 142, 147)

[129] V.T. Bublik, S.S. Gorelik, A.A. Zaitsev, and A.Y. Polyakov. Calculation of the Binding Energy of Ge-Si Solid Solution. *physica status solidi (b)*, **65**: K79–K84, 1974. doi: 10.1002/pssb.2220650249 (see p. 146)

[130] D. J. Eaglesham and M. Cerullo. Dislocation-free Stranski-Krastanow growth of Ge on Si(100). *Physical Review Letters*, **64**: 1943–1946, 1990. doi: 10.1103/PhysRevLett.64.1943 (see p. 146)

[131] Peter Bernhard Hirsch. *Electron microscopy of thin crystals*. en Butterworths, 1965. (see p. 147)

[132] G. Capellini, M. De Seta, Y. Busby, M. Pea, F. Evangelisti, G. Nicotra, C. Spinella, M. Nardone, and C. Ferrari. Strain relaxation in high Ge content SiGe layers deposited on Si. *Journal of Applied Physics*, **107**: 063504–063504–8, 2010. doi: doi:10.1063/1.3327435 (see p. 147)

[133] K. Martens, R. Rooyackers, A. Firrincieli, B. Vincent, R. Loo, B. De Jaeger, M. Meuris, P. Favia, H. Bender, B. Douhard, W. Vandervorst, E. Simoen, M. Jurczak, D.J. Wouters, and J. A Kittl. Contact resistivity and Fermi-level pinning in n-type Ge contacts with epitaxial Si-passivation. *Applied Physics Letters*, **98**: 013504–013504–3, 2011. doi: doi:10.1063/1.3530437 (see p. 148)

[134] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E.K. Evangelou. Fermi-level pinning and charge neutrality level in germanium. *Applied Physics Letters*, **89**: 252110–252110–3, 2006. doi: doi:10.1063/1.2410241 (see p. 148)

[135] R. Braunstein, A.R. Moore, and F. Herman. Intrinsic Optical Absorption in Germanium-Silicon Alloys. *Physical Review*, **109**: 695–710, 1958. doi: 10.1103/PhysRev.109.695 (see p. 148)

[136] Y. Shiraki and A. Sakai. Fabrication technology of SiGe hetero-structures and their properties. *Surface Science Reports*, **59**: 153–207, 2005. doi: 10.1016/j.surfrep.2005.08.001 (see p. 148)

[137] R. People. Indirect band gap of coherently strained Ge_xSi_{1-x} bulk alloys on ãĂĹ001ãĂĽ silicon substrates. *Physical Review B*, **32**: 1405–1408, 1985. doi: 10.1103/PhysRevB.32.1405 (see pp. 148, 152)

[138] S.A. Ringel, J.A. Carlin, C.L. Andre, M.K. Hudait, M. Gonzalez, D.M. Wilt, E.B. Clark, P. Jenkins, D. Scheiman, A. Allerman, E.A. Fitzgerald, and C.W. Leitz. Single-junction InGaP/GaAs solar cells grown on Si substrates with SiGe buffer layers. *Progress in Photovoltaics: Research and Applications*, **10**: 417–426, 2002. doi: 10.1002/pip.448 (see p. 148)

[139] S.A. Hadi, P. Hashemi, N. DiLello, A. Nayfeh, and J.L. Hoyt. Thin film a-Si/c-$Si_{1-x}Ge_x$/c-Si heterojunction solar cells with Ge content up to 56%. *38th IEEE Photovoltaic Specialists Conference (PVSC)*, 000005–000008, 2012. doi: 10.1109/PVSC.2012.6317556 (see pp. 148, 149, 155)

[140] Y.-H. Chen, J.-C. Liu, Y.-R. Chen, J.-W. Lin, C.-H. Chen, W.-H. Lu, and C.-N. Li. Enhancing performance of amorphous SiGe single junction solar cells by post-deposition thermal annealing. *Thin Solid Films*, **529**: 7–9, 2013. doi: 10.1016/j.tsf.2012.06.019 (see pp. 148, 149)

[141] M. ISOMURA, K. NAKAHATA, M. SHIMA, S. TAIRA, K. WAKISAKA, M. TANAKA, and S. KIYAMA. Microcrystalline silicon-germanium solar cells for multi-junction structures. *Solar Energy Materials and Solar Cells*, **74**: 519–524, 2002. DOI: 10.1016/S0927-0248(02)00069-7 (see pp. 148, 149)

[142] T. MATSUI, C.W. CHANG, T. TAKADA, M. ISOMURA, H. FUJIWARA, and M. KONDO. Thin film solar cells based on microcrystalline silicon-germanium narrow-gap absorbers. *Solar Energy Materials and Solar Cells*, **93**: 1100–1102, 2009. DOI: 10.1016/j.solmat.2008.12.023 (see pp. 148, 149)

[143] K. SAID, J. POORTMANS, M. CAYMAX, R. LOO, A. DAAMI, G. BREMOND, O. KRUGER, and M. KITTLER. High quality, relaxed SiGe epitaxial layers for solar cell application. *Thin Solid Films*, **337**: 85–89, 1999. DOI: 10.1016/S0040-6090(98)01390-X (see pp. 148, 149)

[144] K. SAID, J. POORTMANS, M. CAYMAX, JOHAN F. NIJS, L. DEBARGE, E. CHRISTOFFEL, and A. SLAOUI. Design, fabrication, and analysis of crystalline Si-SiGe heterostructure thin-film solar cells. *IEEE Transactions on Electron Devices*, **46**: 2103–2110, 1999. DOI: 10.1109/16.792004 (see p. 148)

[145] R. OSHIMA, Y. WATANABE, M. YAMANAKA, H. KAWANAMI, I. SAKAMOTO, K. MATSUBARA, and I. SAKATA. High-quality SiGe films grown with compositionally graded buffer layers for solar cell applications. *Journal of Crystal Growth*, **378**: 226–229, 2013. DOI: 10.1016/j.jcrysgro.2012.12.154 (see pp. 148, 149)

[146] J.R. DOYLE, D.A. DOUGHTY, and A. GALLAGHER. Plasma chemistry in silane/germane and disilane/germane mixtures. *Journal of Applied Physics*, **71**: 4727–4738, 1992. DOI: 10.1063/1.350663 (see p. 150)

[147] T. MATSUI, K. OGATA, M. ISOMURA, and M. KONDO. Microcrystalline silicon-germanium alloys for solar cell application: Growth and material properties. *Journal of Non-Crystalline Solids*, **352**: 1255–1258, 2006. DOI: 10.1016/j.jnoncrysol.2005.11.144 (see p. 150)

[148] J. OLIVARES, P. MARTIN, A. RODRIGUEZ, J. SANGRADOR, J. JIMENEZ, and T. RODRIGUEZ. Raman spectroscopy study of amorphous SiGe films deposited by low pressure chemical vapor deposition and polycrystalline SiGe films obtained by solid-phase crystallization. *Thin Solid Films*, **358**: 56–61, 2000. DOI: 10.1016/S0040-6090(99)00711-7 (see p. 151)

[149] M.R. ISLAM, M. YAMADA, N.V. ABROSIMOV, M. KIYAMA, and M. TATSUMI. Raman scattering characterization of residual strain and alloy composition in bulk $Si_{1x}Ge_x$ crystal. *The European Physical Journal - Applied Physics*, **27**: 325–328, 2004. DOI: 10.1051/epjap:2004124 (see p. 151)

[150] J.C. TSANG, P.M. MOONEY, F. DACOL, and J.O. CHU. Measurements of alloy composition and strain in thin Ge_xSi_{1-x}layers. *Journal of Applied Physics*, **75**: 8098–8108, 1994. DOI: doi:10.1063/1.356554 (see p. 151)

[151] D. MARSEILHAN, J.P. BARNES, F. FILLOT, J.M. HARTMANN, and P. HOLLIGER. Quantification of SiGe layer composition using MCs^+ and MCs_2^+ secondary ions in ToF-SIMS and magnetic SIMS. *Applied Surface Science*, **255**: 1412–1414, 2008. DOI: 10.1016/j.apsusc.2008.06.048 (see p. 152)

[152] B. SAHA, P. CHAKRABORTY, H. GNASER, M. SHARMA, and M.K. SANYAL. Exact compositional analysis of SiGe alloys by matrix effect compensated MCs^+-SIMS. *Applied Physics A*, **108**: 671–677, 2012. DOI: 10.1007/s00339-012-6949-8 (see p. 152)

[153] E. KASPER and S. HEIM. Challenges of high Ge content silicon germanium structures. *Applied Surface Science*, **224**: 3–8, 2004. DOI: 10.1016/j.apsusc.2003.08.022 (see p. 152)

[154] S.A. HADI, P. HASHEMI, A. NAYFEH, and J. HOYT. Thin Film a-Si/c-$Si_{1-x}Ge_x$/c-Si Heterojunction Solar Cells: Design and Material Quality Requirements. *ECS Transactions*, **41**: 3–14, 2011. DOI: 10.1149/1.3628603 (see p. 155)

[155] R. Cariou, M. Labrune, and P. Roca i Cabarrocas. Thin crystalline silicon solar cells based on epitaxial films grown at 165°C by RF-PECVD. *Solar Energy Materials and Solar Cells*, **95**: 2260–2263, 2011. doi: 10.1016/j.solmat.2011.03.038 (see p. 155)

[156] R. Cariou, R. Ruggeri, P. Chatterjee, J.-L. Gentner, and P. Roca i Cabarrocas. Silicon epitaxy below 200°C: towards thin crystalline solar cells. *SPIE proceedings*, 84700B–84700B, 2012. doi: 10.1117/12.929741 (see p. 155)

Chapter 5

Integration of Si on III-V: towards tandem devices

Contents

Silicon is the most widely used material in microelectronics. Indeed, it features numerous advantages: small mass density, good thermal conductivity, excellent properties of SiO_2, abundance and low cost, non-toxicity, maximum wafer diameter, tremendous amount of research, mature industrial processes, etc. In the field of computer chips, the exponential rise in the power of electronics over the past 50 years has been fuelled by an increase in the density of silicon transistors and their logic performance improvements. Nowadays, the old strategy of shrinking down the transistor dimension is getting close to the limit: the power density dissipated by logic chips becomes critical. Indeed, continuous increase in transistors density requires a reduction in operating voltage, but this compromises the switch speed. One attractive solution is to introduce new channel materials such as III-V semiconductors, which exhibit much higher carriers mobilities[1] (see Fig.5.1-a)). The integration of III-V on silicon, e.g. via wafer bonding techniques, is also a key element for photonic integrated circuits on silicon[2,3]. The interest of this approach stems from the expectation that the maturity and low cost of CMOS-technology can be applied for advanced photonics. The goal is to take the best of two worlds: III-V compounds for their efficient light emission and amplification, and silicon for its low loss and high index contrast wave-guiding properties. This approach has been experimentally validated at III-VLab with the fabrication of InP lasers on SOI wafers[4–7].

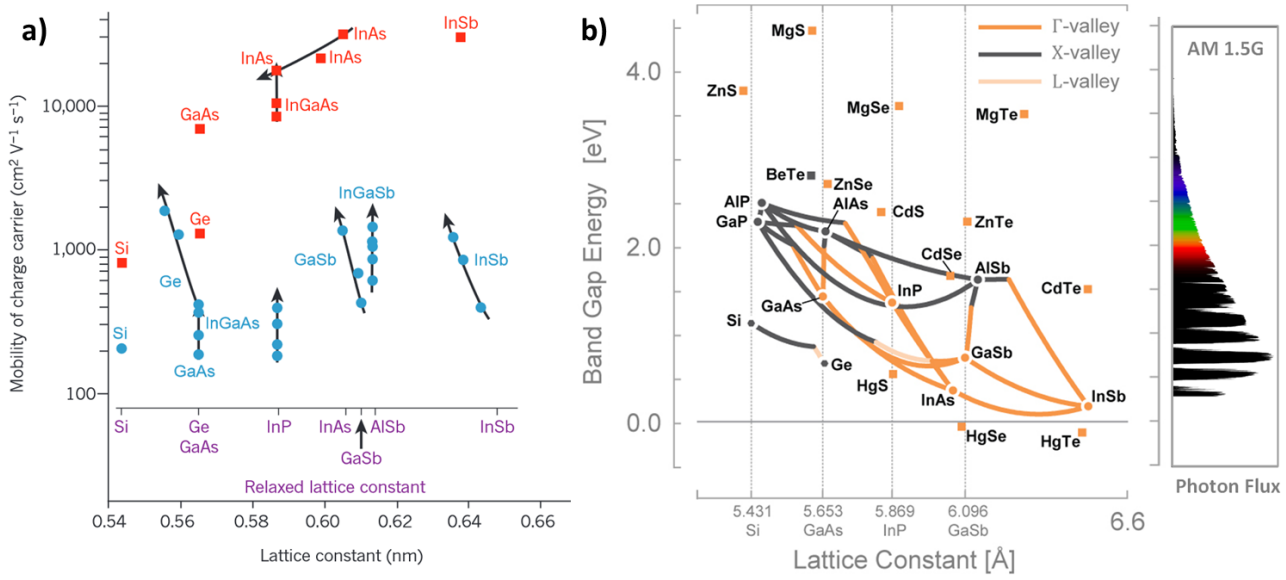


Fig. 5.1 – a) Highest reported mobility of electrons (squares) and holes (circles) at room temperature as function of lattice constant (cubic unit), from Alamo et al.[1]. The effect of bi-axial compressive stress is represented by arrows. b) Band gap versus lattice constant for II-VI and III-V alloys, and AM1.5G solar spectrum power density. Connecting lines represent ternary compositions between binary alloys; their colors represent which conduction band valley is lowest in energy (Γ-valley, direct band gap, X- and L- valleys are indirect band gaps.). From kmontgomery.net.

The family of III-V compound semiconductors, such as GaAs, AlAs, InAs, InP and their ternary and quaternary alloys, combine elements in columns III and V of the periodic table. Some III-V compounds have unique optical and electronic properties such as the ability to efficiently emit and detect light. They are well suited for the construction of a variety of hetero-structures; their band gap energies and lattice constants can be controlled widely. This is illustrated in Fig.5.1-b), which

[1] J.A. del Alamo., Nature, **479**: 317–323, 2011.
[2] A.W. Fang et al., Optics Express, **14**: 9203–9210, 2006.
[3] G. Roelkens et al., Laser & Photonics Reviews, **4**: 751–779, 2010.
[4] A. Le Liepvre et al., IEEE Photonics Technology Letters, **25**: 1582–1585, 2013.
[5] M. Lamponi et al., IEEE Photonics Technology Letters, **24**: 76–78, 2012.
[6] S. Keyvaninia et al., Optics Express, **21**: 3784–3792, 2013.
[7] G.-H. Duan et al., SPIE Novel In-Plane Semiconductor Lasers XIII, **9002**: 90020X–90020X–6, 2014.

shows the broad range of III-V semiconductors (and few II-VI) in a Band Gap/Lattice constant plane; the AM1.5G solar spectrum power density is displayed on an indicative basis, on the right side of the graph. Hence, III-V are widely used in lasers, light-emitting diodes and detectors for optical communications, instrumentation and sensing. The III-V integrated circuit industry is a well developed ecosystem, based on highly automated, reliable and sophisticated processes, producing devices for applications as diverse as smartphones, cellular base stations, satellite communications, fiber-optic systems, astronomy, defense systems and photovoltaics.

In this latter field, crystalline silicon has been the material of choice for decades and it still represents more than 80% of the PV market. Record power conversion efficiency of 25.6% has been reported recently[8]. The maximum detailed balanced theoretical efficiency for Si cells is around 33.6%, however this result is based on ideal material properties[9], and in reality reaching 75 to 80% of the above mentioned calculated theoretical efficiency is an empirical upper limit. A proven way to reach higher efficiencies successfully consists in stacking p-n diodes, made of III-V semiconductors, in series with different band gaps spanning over a broad solar spectrum range; this is the so-called multijunction configuration[10]. Multijunction solar cells based on III-V materials can reach significantly higher power conversion compared to silicon: for instance, Spectrolab has recently claimed 38.8% efficiency under 1 sun illumination and the world record of 44.7% under concentration was recently achieved by the Fraunhofer ISE team of F. Dimroth[11] (and even the yet non-certified 46.5%). Indeed by concentrating the sunlight, the solar cell area (and thus the required material) can be reduced, while at the same time a logarithmic efficiency increase with the illumination is obtained. However, the III-V compounds remain expensive and relatively scarce (compared to silicon), thus they are mainly used in specific applications such as space and terrestrial concentrator photovoltaics. Silicon and III-V materials have complementary properties and a PV device combining the advantages of the III-V multi-junction solar cells with the benefits of Si as the most wide-spread photovoltaic material would be a significant breakthrough toward high efficiency and low cost solar energy. In this chapter we are focusing on the combination of III-V and silicon, targeting photovoltaics tandem devices. After a brief presentation of theoretical potential of III-V/Si system, we summarize the strategies developed in literature for III-V/Si integration, and present our new approach, namely the growth of silicon on III-V. Then the results and building blocks towards III-V/Si tandem device obtained during this thesis work are exposed.

5.1 Theoretical performances for III-V/Si solar cells

It is always useful to look into maximum theoretical efficiency when a new device design is to be investigated. These calculations can be done with the detailed balance technique, introduced by Shockley and Queisser in 1961[9]. This widely used method makes several important assumptions: - Infinite mobility, allowing carrier collection from anywhere they are created - Complete absorption for all photons above the material band gap. Moreover, the detailed balance approach considers only the radiative recombination channel, and thus over-estimates the maximum efficiency, especially for indirect band gap semiconductors such as silicon. This point has been improved by Tiedje and coworkers[12] who could include the free carrier absorption effect as well as Auger recombination to the detailed balance limit. In the eighties, the detailed balance limit was also extended to calculate theoretical efficiency limit for multijunction solar cells[13,14]. By stacking several pn junctions with different gaps, the cell is sensitive to a greater part of the solar spectrum; thermalization and transmission

[8] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **22**: 1–9, 2014.
[9] W. Shockley et al., Journal of Applied Physics, **32**: 510, 1961.
[10] H. Cotal et al., Energy & Environmental Science, **2**: 174–192, 2009.
[11] F. Dimroth et al., Progress in Photovoltaics: Research and Applications, **22**: 277–282, 2014.
[9] W. Shockley et al., Journal of Applied Physics, **32**: 510, 1961.
[12] T. Tiedje et al., IEEE Transactions on Electron Devices, **31**: 711–716, 1984.
[13] C.H. Henry., Journal of Applied Physics, **51**: 4494–4500, 1980.
[14] A. De Vos., Journal of Physics D: Applied Physics, **13**: 839, 1980.

E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	η (%)	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	η (%)
Unconstrained AM1.5G Spectrum									*Constrained AM1.5G spectrum*								
1.34	—	—	—	—	—	—	—	33.68	1.34	—	—	—	—	—	—	—	33.68
0.94	1.73	—	—	—	—	—	—	46.06	0.94	1.60	—	—	—	—	—	—	45.71
0.93	1.40	2.05	—	—	—	—	—	51.94	0.94	1.37	1.90	—	—	—	—	—	51.58
0.70	1.13	1.64	2.23	—	—	—	—	55.91	0.71	1.11	1.49	2.00	—	—	—	—	55.31
0.69	0.98	1.38	1.81	2.40	—	—	—	58.37	0.70	1.01	1.33	1.67	2.14	—	—	—	57.61
0.69	0.94	1.19	1.53	1.92	2.45	—	—	59.93	0.69	0.96	1.20	1.47	1.79	2.24	—	—	59.41
0.69	0.94	1.15	1.41	1.72	2.11	2.57	—	61.36	0.69	0.93	1.14	1.37	1.60	1.90	2.33	—	60.78
0.51	0.70	0.94	1.15	1.41	1.73	2.11	2.57	62.34	0.51	0.75	0.98	1.18	1.40	1.63	1.92	2.35	61.42
Unconstrained maximum concentration									*Constrained maximum concentration*								
1.11	—	—	—	—	—	—	—	40.74	1.11	—	—	—	—	—	—	—	40.74
0.77	1.70	—	—	—	—	—	—	55.80	0.76	1.54	—	—	—	—	—	—	55.47
0.62	1.26	2.10	—	—	—	—	—	63.75	0.60	1.14	1.82	—	—	—	—	—	63.15
0.52	1.03	1.61	2.41	—	—	—	—	68.67	0.49	0.93	1.38	2.01	—	—	—	—	67.85
0.45	0.88	1.34	1.88	2.65	—	—	—	72.00	0.44	0.81	1.17	1.58	2.18	—	—	—	71.02
0.40	0.78	1.17	1.60	2.12	2.87	—	—	74.41	0.38	0.71	1.01	1.33	1.72	2.30	—	—	73.33
0.36	0.70	1.04	1.40	1.81	2.32	3.06	—	76.22	0.37	0.66	0.92	1.18	1.48	1.85	2.42	—	75.09
0.33	0.64	0.94	1.25	1.59	1.98	2.47	3.20	77.63	0.30	0.60	0.83	1.06	1.29	1.57	1.96	2.50	76.19

Fig. 5.2 – Theoretical efficiencies and optimum band gap values for multijunction solar cells with up to 8 sub-cells, in both series connection and unconstrained configuration. Efficiencies are calculated for AM1.5G spectrum and under maximum concentration. From Bremner et al.[15].

losses are reduced.

The detailed balance efficiencies for multijonction with up to 8 sub-cells are displayed in Fig.5.2. In their calculations, Bremner et al.[15] have distinguished the case of series-connected cells and unconstrained configuration. Both scenarios are examined under AM1.5G spectrum and maximum concentration. The unconstrained design, for which the cells are optically coupled but electrically independent (no current matching), shows a slightly superior efficiency. However , the constrained design is the most widely used since it comes with a much simpler contacting scheme. The optimum band gap sets for 1, 2, 3 and 4 series connected junctions under AM1.5G spectrum are 1.34, 0.94/1.6, 0.94/1.37/1.90 and 0.71/1.11/1.49/2.00 eV, reaching respectively 33.68, 45.71, 51.58 and 55.31 % efficiency. Thus, the optimum low band gap cell for dual and triple junction is slightly below 1 eV; this requirement can be met with a SiGe bottom cell. In the case of 4 junctions device, silicon band gap is well suited for the second bottom cell.

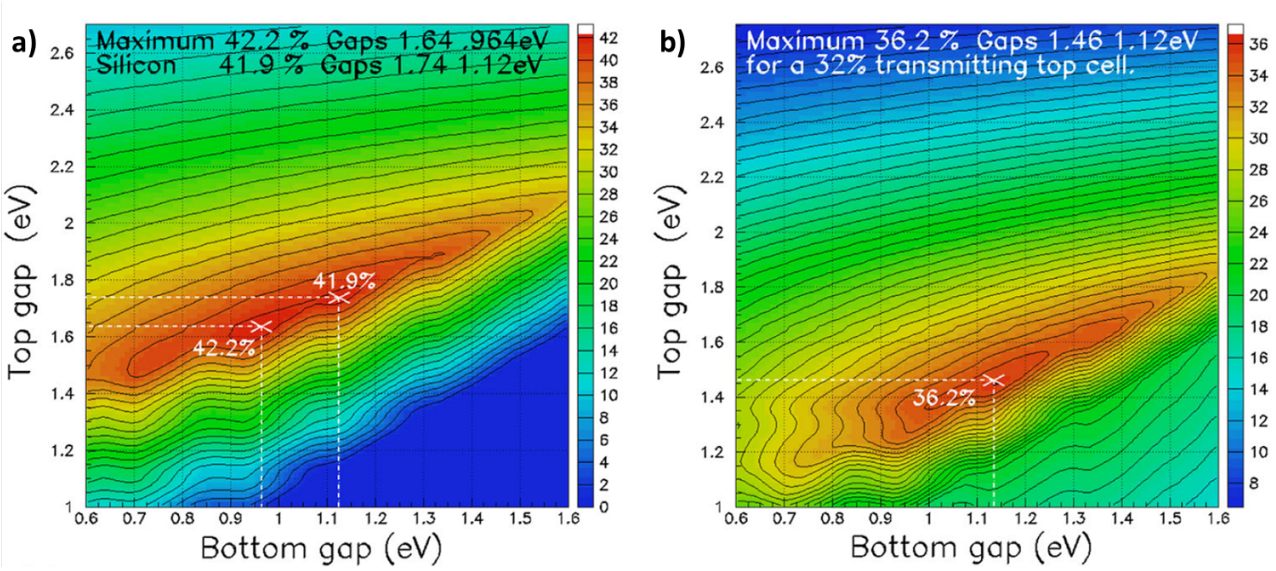


Fig. 5.3 – Theoretical efficiencies for a dual junction device under AM1.5G spectrum showing: a) two maxima, 42.2% at 0.96/1.64 eV and 41.9% at 1.12/1.74 eV and b) one maximum, 36.2% at 1.46/1.12 eV, in the case of a thin top cell (32% optical transmission) for current matching with Si bottom cell. From Connolly et al.[16].

[15] S.P. Bremner et al., Progress in Photovoltaics: Research and Applications, **16**: 225–233, 2008.

Looking more precisely at the **dual junction**, the efficiency contour plot as a function of top and bottom band gap is shown in Fig.5.3-a). Two maxima are visible: i) the one previously mentioned at $\sim$ 0.96/1.64 eV and ii) a second maximum which includes the silicon band gap: 1.12/1.74 eV reaching a slightly lower but still high efficiency, namely 41.9% as calculated by Connolly et al.[16]. Thus, if not the absolute maximum, the combination silicon with a high band gap material has nonetheless the potential to reach high efficiency. The small discrepancy between various theoretical efficiencies reported in literature is linked to author's assumptions during the calculations (numerical method, solar spectrum, recombination channels, material parameters, etc.). If sub-cells with less than unit EQE are considered, then the optimum becomes different: the contour plot in the case of a 32% optically transparent top cell is shown in Fig.5.3-b); the new maximum of 36.2% efficiency corresponds to a 1.46/1.12 eV tandem. This partially transparent top cell is an interesting scenario which should allow easier current matching for non-perfect materials.

In the case of **triple junctions**, the traditional solar cells are typically made of GaInP/GaAs/Ge and can reach efficiencies in the 41% range[17]. Germanium acts here as a substrate and as the bottom p-n junction. However Ge is not the most adapted material: i) the band gap is not optimal: 0.66 eV produces excess current in the bottom cell which is lost due to the series connection of the junctions; ii) Ge is an expensive and scarce material; iii) it has a poor thermal conductivity, etc. So research focuses on reducing the germanium thickness and/or finding a new bottom cell material. In fact, silicon is an appealing choice to replace Ge, since it has an adapted 1.12 eV band gap, it is widely available at low cost, it has a better thermal conductivity and mechanical strength, and it also benefits from a well-established industry. In addition, the theoretical detailed balance efficiency for a $Ga_{0.51}In_{0.49}P$/GaAs/Si triple junction is high[18]: roughly 46.9% under 1 sun, as shown in Fig.5.4-a) and 53.9% under a concentration of 500 suns, as shown in Fig.5.4-b). Nevertheless, a more realistic upper limit can be estimated with the correction factor 0.75 or 0.8, thus this device potential is around 35% at 1 sun and 40% under 500 suns. This is basically the same potential than a metamorphic Ge based triple junction, but with a much more advantageous and attractive solution for the bottom cell.

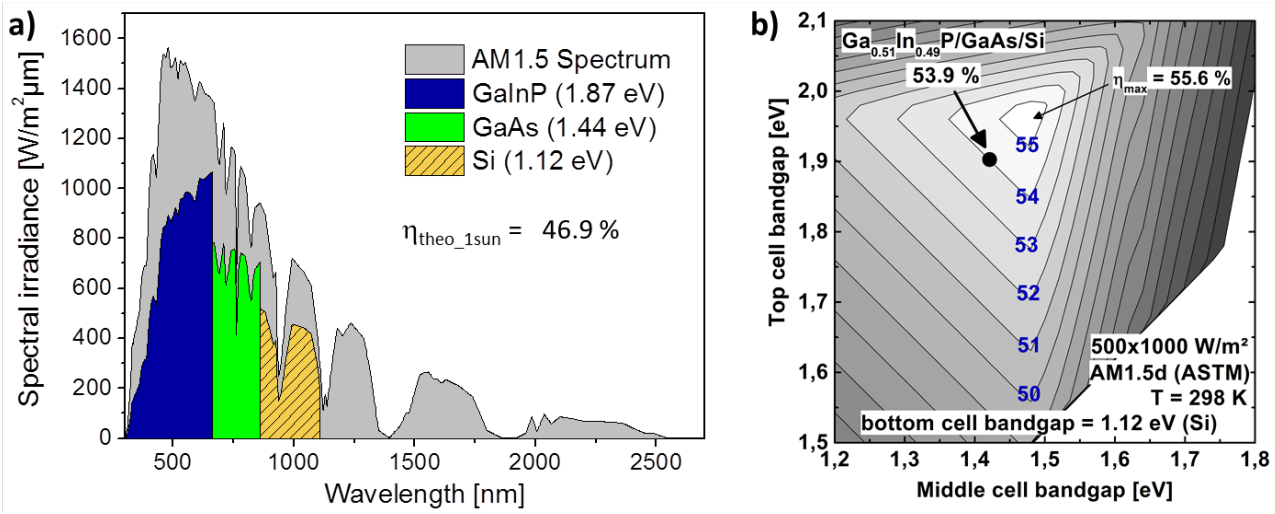
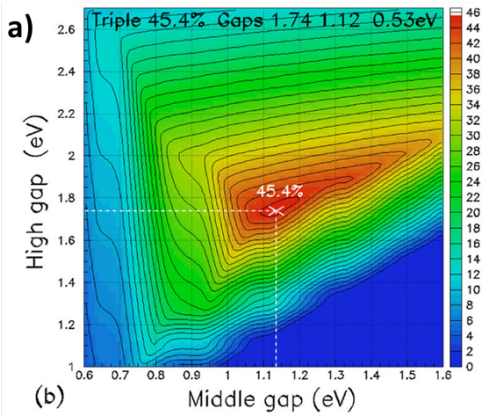


Fig. 5.4 – a)The AM1.5G spectrum and the fraction that can in theory be converted into electricity by a GaInP/GaAs/Si triple junction. b) Triple junction efficiency map at 500X, as a function of top & middle cell band gap, for a fixed Si bottom cell. From Derendorf et al.[18]

Alternatively, instead of being used as the bottom cell, the silicon gap appears to be also fairly well adapted as a middle cell band gap. This is illustrated in the efficiency contour plot from Connolly et al.[16], displayed in Fig.5.5-a). Using the combination of 1.74/1.12/0.53 eV band gap materials,

[16] J.P. Connolly et al., Progress in Photovoltaics: Research and Applications, , 2014.
[17] W. Guter et al., Applied Physics Letters, **94**: 223504, 2009.
[18] K. Derendorf et al., IEEE Journal of Photovoltaics, **3**: 1423–1428, 2013.

a)



b)

Device	Number of Junctions	Efficiency (%)
AlGaAs/GaAs	2	36.7
AlGaAs/GaAs/Si	3	41.5
AlGaAs/GaAs/InGaAs	3	41.3
AlGaAs/GaAs/Si/InGaAs	4	45.7
AlGaAs/GaAs-Si	3	43.1
AlGaAs/GaAs-InGaAs	3	46.4
AlGaAs/GaAs-Si-InGaAs	4	49

'/' denotes current matched junctions
'-' denotes separate electrical connection

Fig. 5.5 – a)Triple junction solar cell radiative limit efficiency under Am1.5G solar spectrum, as function of top and middle cell band gap; the maximum efficiency when using Si as a middle cell is 45.4% (1.174/1.12/0.53eV). From Connelly et al[16]. b) Simulated performances of III-V/Si multijunctions in series and with separated electrical connection. From Mathews et al.[19].

efficiency of 45.4% is calculated under 1 sun AM1.5G; this only $\sim$ 1.5% lower compared to a triple junction with Si as a bottom cell. However this design is probably more complicated since both front and back silicon interfaces have to be precisely controlled.

When used in a **quadruple junction**, silicon is well adapted as a second bottom cell. Efficiencies between 55 and 57 % are calculated by Bremner[15] an Zhaler[20] (see Fig.5.2 and Fig.5.6). Indeed both silicon and germanium are well suited for a quadruple junction device : the diagram of a 4 junction device based on Ge and Si bottom cell is shown in Fig.5.6-b), and the corresponding detailed balance efficiency is around 57%, as shown in a). Bypassing the detailed balanced calculation, Mathews et al.[19] could developed a rather simple 1D electrical and optical model to calculate maximum efficiencies in series and independently connected cells.

a)

Series-connected triple-junction on a Si subcell	Band gap (eV)	Subcell 1	2.00
		Subcell 2	1.49
		Subcell 3	1.12
	Efficiency		0.512
Optimum series-connected four-junction	Band gap (eV)	Subcell 1	2.00
		Subcell 2	1.49
		Subcell 3	1.12
		Subcell 4	0.72 (GaSb)
	Efficiency		0.579
Series-connected GaInP/GaAs/ InGaAsP/InGaAs four-junction	Band gap (eV)	Subcell 1	1.90
		Subcell 2	1.42
		Subcell 3	1.02
		Subcell 4	0.60
	Efficiency		0.549
Series-connected four-junction with Si and Ge subcells	Band gap (eV)	Subcell 1	2.00
		Subcell 2	1.49
		Subcell 3	1.12
		Subcell 4	0.67
	Efficiency		0.574
Independently-connected five-junction	Band gap (eV)	Subcell 1	2.50
		Subcell 2	1.93
		Subcell 3	1.53
		Subcell 4	1.13
		Subcell 5	0.70
	Efficiency		0.612

b)

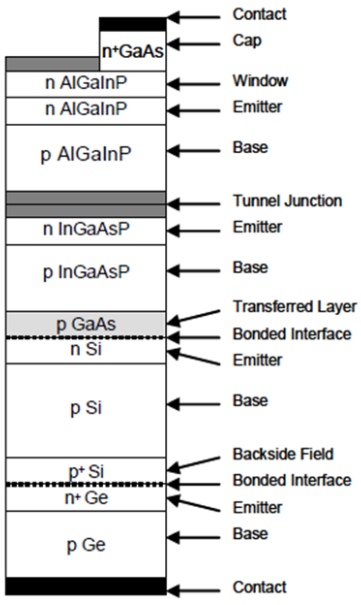


Fig. 5.6 – a) Detailed-balanced efficiency calculations for wafer-bonded enabled solar cells under 100 suns AM1.5D spectrum. b) Schematic of a 4 junction series-connected cell (2/1.49/1.12/0.67eV) with active Si and Ge bottom cells. From Zahler PhD thesis[20].

[20] J.M. Zahler. *Materials integration for high-performance photovoltaics by wafer bonding.* PhD thesis. California Institute of Technology, 2005.

[19] I. Mathews et al., Optics Express, **20**: A754–A764, 2012.

Their results are displayed in Fig.5.5-b). For a quadruple configuration, they found 45.7% in a AlGaAs/GaAs/Si/InGaAs device, and 3% absolute improvement if the same materials are used in a 6 terminals configuration. However even if the sub-cells are assembled by simple mechanical stacking, the 6 terminal configuration implies a complex contacting scheme which may be difficult to implement at the industrial level.

5.2 Pathways to combine III-V and Silicon: literature overview

As shown in the previous section, the silicon band gap is well adapted for multijunctions: while not being the exact optimum band gap, this material can potentially reach very high efficiencies when used in dual, triple and quadruple junction solar cells in combination with III-V materials. However, once the theoretical efficiencies are known, then the big question of how to combine the different semiconductor compounds should be addressed. In fact, the epitaxial growth of III-V on silicon encounter two considerable obstacles: i) first, the difference in lattice constant; indeed as shown in Fig.5.1-b), the variety of gaps available in the III-V family corresponds to a wide range of lattice parameters, but very few III-V compounds are lattice matched to silicon. For example, GaAs and Si have both a Zinc blende crystal structure, but with respectively 5.65 and 5.43Å lattice parameter at room temperature; this corresponds to a $\sim 4\%$ lattice mismatch. ii) Second, the difference in thermal expansion coefficient. This is illustrated in Fig.5.7-a) where III-V, Si and Ge thermal expansion coefficients as a function of lattice parameter are represented; the inset shows the variation of Si and GaAs lattice from room temperature to 450°C.

For more than 30 years, researchers have attempted to combine Si and GaAs, thus the problems encountered during growth of GaAs on Si are well documented[21–23]. Some of them are already well addressed: this is the case of the polar/non-polar interface (e.g. GaAs/Si interface). This polarity difference results in anti-phase domains (APD)[24], which consists of crystallographic regions where atoms are swapped with respect to their order in a perfect lattice system (e.g. an As atom occupies the position of a Ga atom).

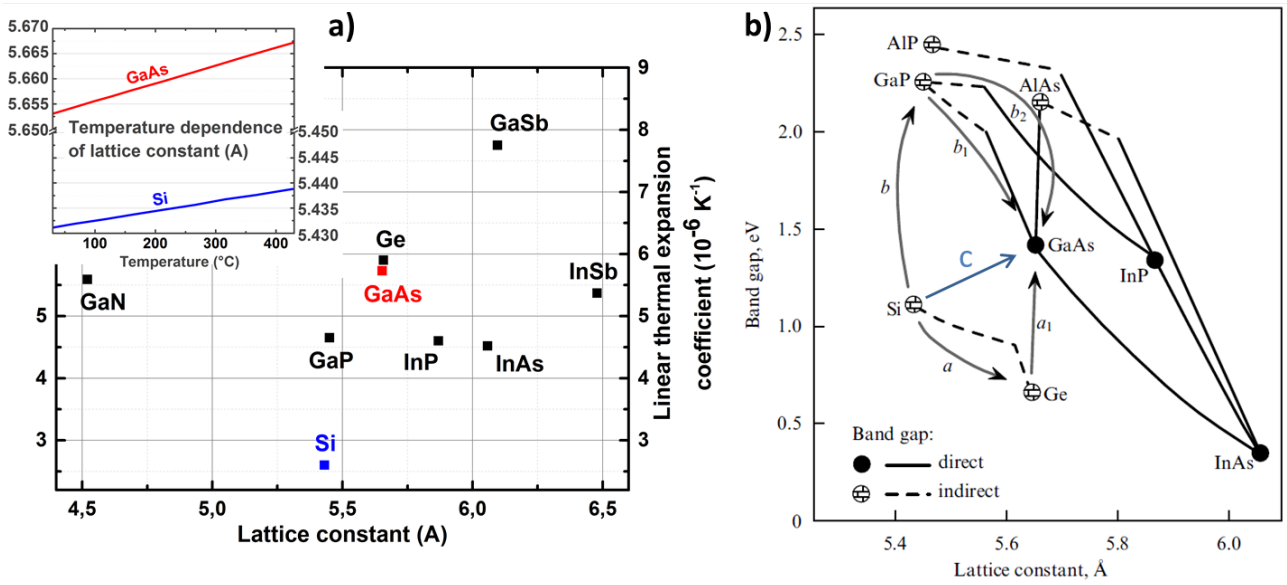


Fig. 5.7 – a) Lattice constant and linear thermal expansion coefficients of III-V, Si and Ge. From Kawanami et al.[22]. b) Band gap versus lattice constant for Si, Ge and III-V compounds. Arrows indicate transition pathways from Si to GaAs. From Bolkhovityanov et al.[21].

[21] Pchelyakov O.P. Bolkhovityanov Y.B., Physics-Uspekhi, **51**: 437, 2008.
[22] H. Kawanami., Solar Energy Materials and Solar Cells, **66**: 479–486, 2001.
[23] H. Kroemer et al., Journal of Crystal Growth, **95**: 96–102, 1989.
[24] M. Kawabe et al., Japanese Journal of Applied Physics, **26**: L944, 1987.

This problem was successfully solved by using Si substrates deflected by 4-6° from the (100) plane[25,26]. But the two previously mentioned lattice and thermal mismatches are more serious. Indeed, lattice mismatch results in a high density of dislocations and a high stress in the growing crystal, and since the GaAs growth is usually performed at high temperature (e.g. 600-700° in MOCVD reactors), additional dislocations and cracks appear upon cooling, due to thermal expansion mismatch with silicon. For the GaAs on Si system, in literature, we can distinguish various approaches to tackle this issue: i) the first one consist in growing directly GaAs on Si and see how the high defect density is affecting the targeted device. This path is represented in Fig.5.7-b) by the arrow c. ii) Another possibility consists in using buffer layers between the substrate and the active active layer, to accommodate the strain and the lattice parameter. This path is represented by arrows a and b on Fig.5.7-b). iii) Finally, it is also possible to bring together GaAs and Si with non-epitaxial techniques, such as wafer bonding. Some examples of those three approaches, in the field of solar cells, are detailed below.

5.2.1 Direct epitaxial growth of III-V on silicon

The heteroepitaxial growth of GaAs on Si, results in strain and various types of crystalline defects: lattice distortions, stacking faults, misfit dislocations that can extend in the epi-layer and generate threading dislocations throughout the structure, etc. The large mismatch of GaAs/Si system, namely $\sim 4\%$, typically results in poor crystal quality with threading dislocation density as high as 10^8-10^9cm^{-2}. Such high defect density can be easily detected by TEM cross section: in the bright field of GaAs/Si interface produce by Luxmoore et al.[27], (see Fig.5.8-a)), the threading dislocations are visible as darker lines spreading in the GaAs epi-layer. Various types of dislocations can be found in a defective crystal, as an example, a 3D molecular model of an edge dislocation[28], caused by the termination of a plane of atoms in the middle of a crystal, is shown in Fig.5.8-b).

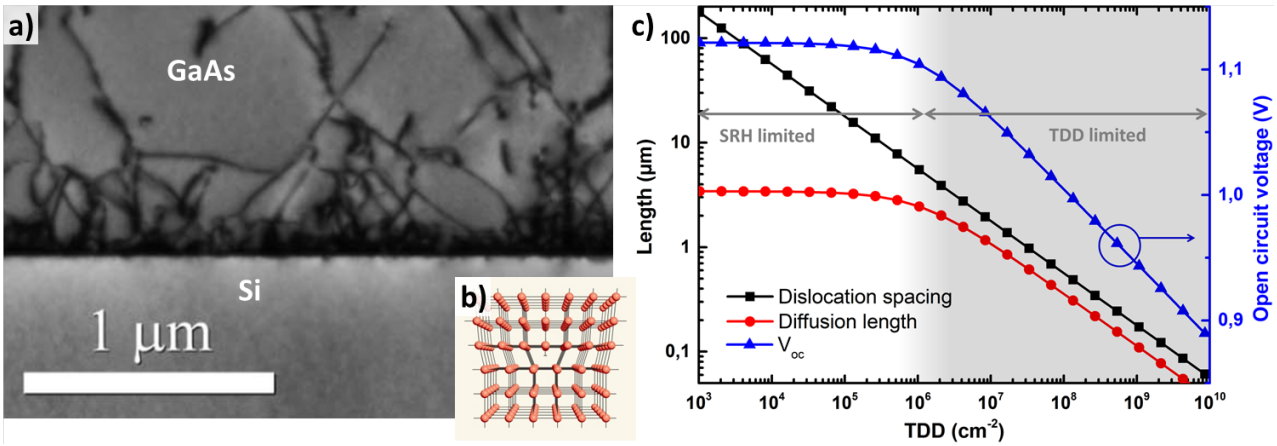
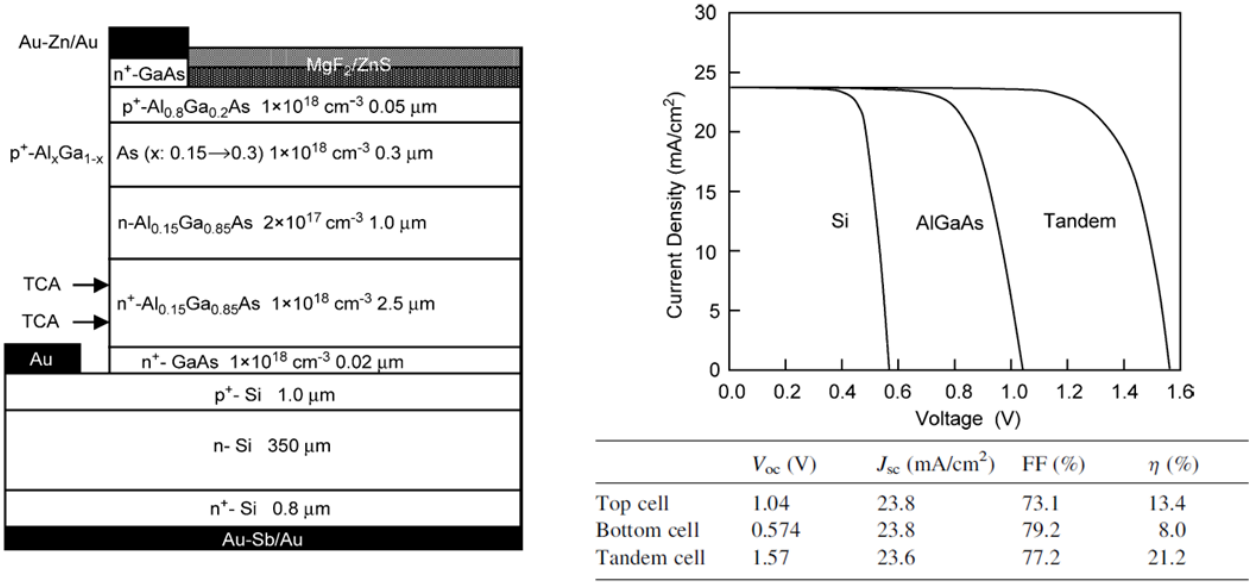


Fig. 5.8 – a) Cross section TEM bright field image of threading dislocations spreading from Si substrate into GaAs epi-layer. From Luxmoore et al.[27]. b) 3D molecular model showing a dislocation edge (extra atomic plane)[28]. c) Left: averaged dislocation spacing (squares) and minority carrier diffusion length (circles), in 1 μm GaAs (n-type 1×10^{17}cm^{-3}, 20ns lifetime), as function of threading dislocation density (TDD). Right: open circuit voltage (triangles) as function of TDD. A dislocation limited region appears above $\sim$ 10^6cm^{-2}. Adapted from[29,30].

Threading dislocations are indeed very effective in reducing mobility and acting as mid gap recombination centers. As a matter of fact, dislocations play a dominant role in solar cell performances;

[25] R. Fischer et al., Applied Physics Letters, **47**: 397–399, 1985.
[26] A. Georgakilas et al., Applied Surface Science, **102**: 67–72, 1996.
[27] I.J. Luxmoore et al., Scientific Reports, **3**: , 2013.
[28] P.J. McNally., Nature, **496**: 37–38, 2013.

their impact on material and device properties are relatively well documented[29,30]. Dislocation recombination centers reduce the minority-carrier lifetime and diffusion length, which translates at the device level into a short-circuit current reduction and an increase of the excess leakage current. Up to a density of $10^8 cm^{-2}$, the increase of dislocation density is reported to have a relatively small effect on carrier mobility, but the concomitant decrease in diffusion length impacts significantly the solar cell performance. If we assume a constant mobility and solve the 1D continuity transport equation with dislocations as boundary conditions, it is possible to evaluate the impact of dislocation density on diffusion length and V_{oc} using semi-empirical expressions[29,30]. For example, the variation of these two quantities with dislocation density, for a 1μm thick n-type GaAs absorber, with n=$2\times10^{17} cm^{-3}$ and τ_p=20ns minority carriers lifetime, is shown in Fig.5.8-c). Two regions can be distinguished: i) the low threading dislocation density region, TDD $\leq 10^6 cm^{-2}$, where diffusion length is much smaller than the average dislocation spacing. In this region, diffusion length is mainly limited by bulk recombination, namely SRH. ii) The dislocation limited region, for TDD$\geq 10^6 cm^{-2}$. This threshold value is doping dependent: materials with higher(lower) doping level have a lower(higher) bulk lifetime, and thus the TDD limited region is shifted towards higher(lower) value with increasing(decreasing) doping. While the impact of TDD density on J_{sc} can be minimized by appropriate solar cell design, the effect on open circuit voltage is less forgiving; along with fill factor they are the limiting factor for III-V cells on a mismatch substrate. The diffusion coefficient being relatively independent of the dislocation density, the ratio D/L_D increases with higher dislocation density, and this leads to an increased saturation current density J_0 and lower V_{oc}. More specifically, dislocation related recombination in the depletion region will generate large recombination current and shunt paths across the junction. The quantitative impact of TDD on V_{oc} is shown in Fig.5.8-c): a TDD increase from 10^6 to $10^8 cm^{-2}$ results in a $\sim$ 100 mV drop for the V_{oc}.



	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	η (%)
Top cell	1.04	23.8	73.1	13.4
Bottom cell	0.574	23.8	79.2	8.0
Tandem cell	1.57	23.6	77.2	21.2

Fig. 5.9 – AlGaAs/Si tandem solar cell fabricated by direct epitaxial growth on Si with corresponding IV curves under 1 sun AM0 spectrum, and solar cells parameters. From Jimbo et al.[31].

To date, the best solar cell efficiency achieved with this direct epitaxial growth approaches is 21.2% under 1 sun AM0 spectrum, for a tandem AlGaAs/Si device[31,32]. Details about the structure and its performances are shown in Fig.5.9. However, the reported J_{sc} of 23.6mA/cm^2 is probably overestimated, since a tandem with silicon cannot exceed $\sim$ 22mA/cm^2.

[29] M. Yamaguchi et al., Journal of Applied Physics, **58**: 3601–3606, 1985.
[30] S.A. Ringel et al., Progress in Photovoltaics: Research and Applications, **10**: 417–426, 2002.
[31] T. Jimbo et al., Sci. Technol. Adv. Mater., **6**: 27, 2005.
[32] M. Umeno et al., Solar Energy Materials and Solar Cells, **41-42**: 395–403, 1996.

Some advanced strategies such as the implementation of strained layer super-lattice acting as barrier layers for the dislocation combined with thermal cyclic annealing can help to reduce the defect density in the upper most epi-layer[27,33,34]. Alternatively, the option of using Si lattice-matched quaternary alloys, such as GaNPAs, has also been explored by NREL for instance, however the low minority carrier lifetime of those materials was crippling for solar cells applications[35].

5.2.2 III-V on Si via buffer layers

Another possibility to limit the deleterious effect of dislocations, is to use interfacial buffer layers between the Si substrate and the active III-V material; it helps to reduce and relax the effects of the abrupt changes of lattice constant and polarity problems. If the Si substrate is to be used as a bottom cell, then the buffer layer should be transparent (higher gap compared to silicon) and conductive, to maximize the current of the bottom cell and minimize resistance losses. GaAsP seems to be a promising material for the buffer layer, with the following design: i) First a nearly lattice GaP layer (see Fig.5.1-b)) is grown on Si ii) and then a step graded GaAsP layer, for which the As content is gradually increased, is used to get closer to GaAs lattice parameter. This path is illustrated by arrows b and b1 in Fig.5.7-b). A schematic of such layer stack is shown in Fig.5.10-a), and the lattice parameter increasing from Si to GaAs is visible in the XRD reciprocal space mappings in Fig.5.10-b), as published by Roesener et al.[36]

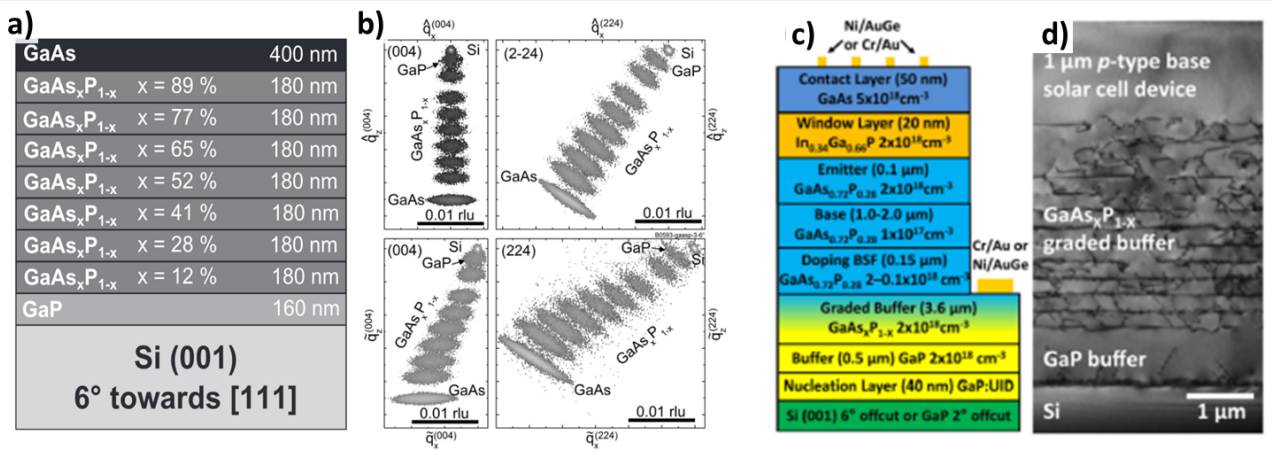


Fig. 5.10 – a) Schematic of $GaAs_xP_{1-x}$ buffer grown on Si substrate and b) the corresponding XRD (004) and (224) reciprocal space mappings. From Roesener et al.[36]. c) GaAsP solar cell grown on Si substrate with graded buffer layers, d) is the corresponding cross section TEM picture, with visible dislocations pattern confined in the buffer layer. From Lang et al.[37].

This growth scenario starts to be well understood and controlled[38], dislocation densities in the range of $10^7 cm^{-2}$ are reported; research groups are now focusing on producing solar cells with this approach[37,39,40]. However, to date, GaAsP buffer layer cells have lower efficiencies compared to the direct epitaxial growth; for instance, tandem GaInP/GaAs grown via buffer layers on inactive Si substrate around 16% are reported in literature[41]. Other buffer layer materials are also reported in literature: for instance, SiGe is another possibility to make the transition between Si and GaAs, as

[33] M. Kaya et al., Superlattices and Microstructures, **35**: 35–44, 2004.
[34] M. A. Putyato et al., Russian Physics Journal, **53**: 906–913, 2011.
[35] J. Geisz., NREL Conference paper, 520–36991, 2004.
[36] T. Roesener et al., Journal of Crystal Growth, **368**: 21–28, 2013.
[38] T. Nguyen Thanh et al., Journal of Applied Physics, **112**: 053521–053521–8, 2012.
[37] J.R. Lang et al., Applied Physics Letters, **103**: 092102, 2013.
[39] T.J. Grassman et al., IEEE Journal of Photovoltaics, **Early Access Online**: , 2014.
[40] Tyler J. Grassman et al., 82560R–82560R, 2012.
[41] F. Dimroth et al., IEEE Journal of Photovoltaics, **4**: 620–625, 2014.

shown in Fig.5.7-b) by arrows a and a_1. Threading dislocations densities in the range of $10^6 cm^{-2}$ are reported with a best efficiency of ∼18% for a single GaAs cell on SiGe/Si[30,42,43]. However, if Si/III-V tandem device is the targeted device, using a lower band gap as an intermediate buffer layer will definitely reduce the current of the lower Si cell. Alternatively, mechanically weak alloys, such as GaSb or AlSb, which can relax thermal and lattice mismatch faster, are also under focus[44,45]; some recent papers also mentioned graphene assisted Van Der Waals epitaxial growth[46].

5.2.3 Non-epitaxial techniques to combine III-V/Si

A solid can be joined directly to another solid at temperatures as low as room temperature, by pressing them together, provided they have mirror-polished, flat and ideally clean surfaces: this is the so-called **wafer bonding**. When pressing together surfaces, they interact via Van Der Waals forces; however several bonding techniques (plasma activated, under ultra-high vacuum, etc.) enable to achieve strong covalent bonds between the two materials (e.g. InP/Si[47], GaAs/InAs[48]), even down to room temperature[49,50]. In this way crystal mismatch issues are suppressed; the top III-V cells can be grown lattice matched on a III-V substrate, with a sacrificial layer in between. Then, once the top cell has been bonded to Si carrier/bottom cell, the sacrificial layer can be etched away and the substrate re-used after proper surface restoration steps.

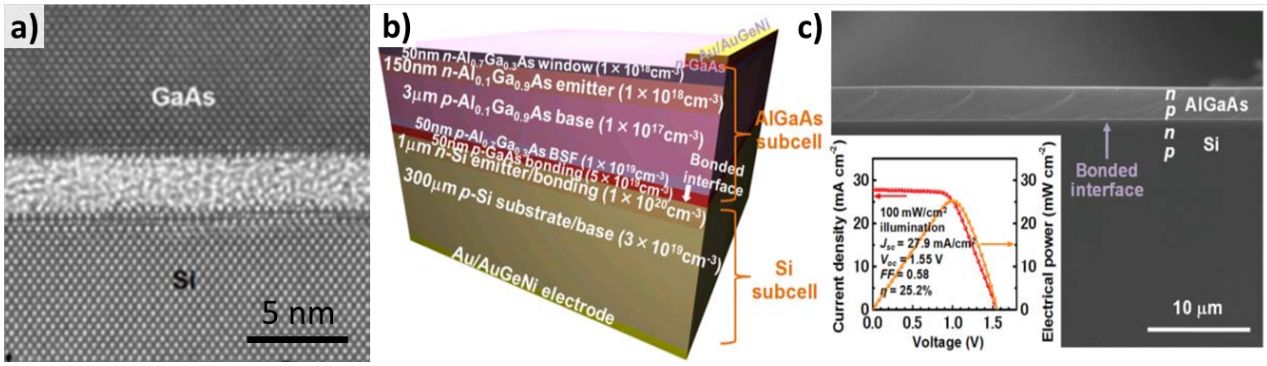


Fig. 5.11 – a) Cross section TEM image of a GaAs/Si bonding interface. b) Schematic diagram of AlGaS/Si wafer bonded solar cell. c) Corresponding cross section SEM picture with IV performances shown in the inset. From Tanabe et al.[51].

An example of wafer bonded GaAs/Si interface is shown in Fig.5.11-a). The integrity of the crystal is well preserved, except for a thin amorphized interface layer[51]. This results in additional series resistances, however promising devices have been realized with this approach: 25% are reported for a bonded tandem AlGaAs/Si under 1 sun illumination (See Fig.5.11-b,c)). However, here again the current of $27.9 mA/cm^2$ appears overestimated (it may be lamp calibration, or surface estimation issues) compared to the max $22 mA/cm^2$ achievable in tandem with bottom silicon. Fraunhofer ISE is also very active in this field, and triple junction GaInP/GaAs/Si may reach 30% in a near future[18,41]. Additionally, it should be mentioned that the actual world record solar cells, 44.7% under ∼ 300 suns, is a 4 junction device, realized by bonding 2 bottom cells grown on InP and 2 top cells grown

[42] C.L. Andre et al., IEEE Transactions on Electron Devices, **52**: 1055 –1060, 2005.
[43] J. Faucher et al., Applied Physics Letters, **103**: 191901, 2013.
[44] H. Uchida et al., Journal of Crystal Growth, **150, Part 1**: 681–684, 1995.
[45] D. Huffaker., SPIE Newsroom, **Available online**: , 2008.
[46] Y. Alaskar et al., Advanced Functional Materials, n/a–n/a, 2014.
[47] J.M. Zahler et al., MRS Online Proceedings Library, **1012**: , 2007.
[48] K. Tanabe et al., Applied Physics Letters, **89**: 102106, 2006.
[49] P. Ramm et al. *Handbook of wafer bonding*. English Weinheim: Wiley-VCH, 2012.
[50] C.Y. Yeo et al., Applied Physics Letters, **102**: 054107–054107–4, 2013.
[51] K. Tanabe et al., Scientific Reports, **2**: , 2012.
[18] K. Derendorf et al., IEEE Journal of Photovoltaics, **3**: 1423–1428, 2013.

on GaAs[11]. Even if substrate re-use is possible, the question whether this technique is suitable for solar production on large area and large scale (silicon standards) remains open. Indeed, compared to the direct or buffer assisted epitaxial scenario, the bonding requires more steps and careful surface preparations.

Alternatively, the **mechanical stacking** or adhesive bonding approach seems to give promising results. It consists in using transparent glues to stack solar cells grown separately; sub-cells can be independently connected, thus relaxing the current matching constraint. Tandem[52] and even 4 junction devices[53] are reported. This technique is appealing since it seems easily compatible with the existing silicon technology; however the question of the glue mechanical strength and aging properties should be addressed.

5.3 Growing Silicon on III-V: a new paradigm

As presented above, the general and logical trend for combining III-V with silicon is to use silicon as a substrate and add few microns of III-V material above it. However, to buck this trend, we decided to explore the opposite route of growing silicon on III-V, namely on GaAs, using the low temperature epitaxial growth technique presented in this manuscript. The general idea and targeted III-V/Si device is shown in Fig.5.12 schematic.

- The first step is the MOCVD growth. Starting from a GaAs substrate, a buffer layer and a sacrificial layer are grown in lattice matched configuration. The sacrifial layer can be classically made of AlAs[54,55], or InP based materials such as GaInP of InAlP[56]; it will serve to release the active III-V layers from the substrate. The top cell is grown inverted on this sacrificial layer. Targeting a tandem solar cell device for 1 sun application, the materials are chosen to fit with one of the two maximum efficiency point shown in Fig.5.3-a): 1.64/0.96 eV or 1.74/1.12 eV. The AlGaAs ternary alloy can be used for the top cell since it has a tunable band gap with Al composition: for example 17% of Al corresponds roughly to 1.63 eV and 24% to 1.74 eV. Following this top cell, a tunnel junction is grown: it can be either in III-V materials or in silicon (in the next step) or even half III-V half silicon.

- The second step involves the epitaxial growth of the bottom cell by PECVD, at low temperature, on top of the previously MOCVD grown layers. This cell is made of Si(Ge) material, for which the band gap can be tuned between 1.12 eV (Si) and 0.66 eV(Ge). The maximum efficiency is expected for pure silicon in combination with 1.74 eV top cell or for 0.96/1.63 eV tandem, and this can be achieved with $\sim$ 40% of Ge in the bottom cell. As mentioned above, half or the totality of the tunnel junction interconnecting the top and bottom cell can be made in Si(Ge) materials. The top most surface of this epitaxial structure is then processed as a back side (reflector, contacts, etc.).

- The last step consists in lifting off the whole structure glued to a low cost substrate (that may be flexible) thanks to the sacrificial layer that can be selectively chemically etched, for example using HF in the case of AlAs. After this transfer, the interface which was initially in contact with the sacrificial layer becomes the sun facing one, and consequently need to be processed (contacts, anti-reflection layer, etc.). The initial substrate may be re-used after appropriate

[11] F. Dimroth et al., Progress in Photovoltaics: Research and Applications, **22**: 277–282, 2014.
[52] I. Mathews et al., Progress in Photovoltaics: Research and Applications, n/a–n/a, 2014.
[53] X. Sheng et al., Nature Materials, **13**: 593–598, 2014.
[54] J.J. Schermer et al., Thin Solid Films, **511-512**: 645–653, 2006.
[55] A.T.J. Van Niftrik. *The epitaxial lift-off method : III/V materials and HF etch process studies*. PhD thesis. Radboud University, Netherlands, 2008.
[56] C.-W. Cheng et al., Nature Communications, **4**: 1577, 2013.

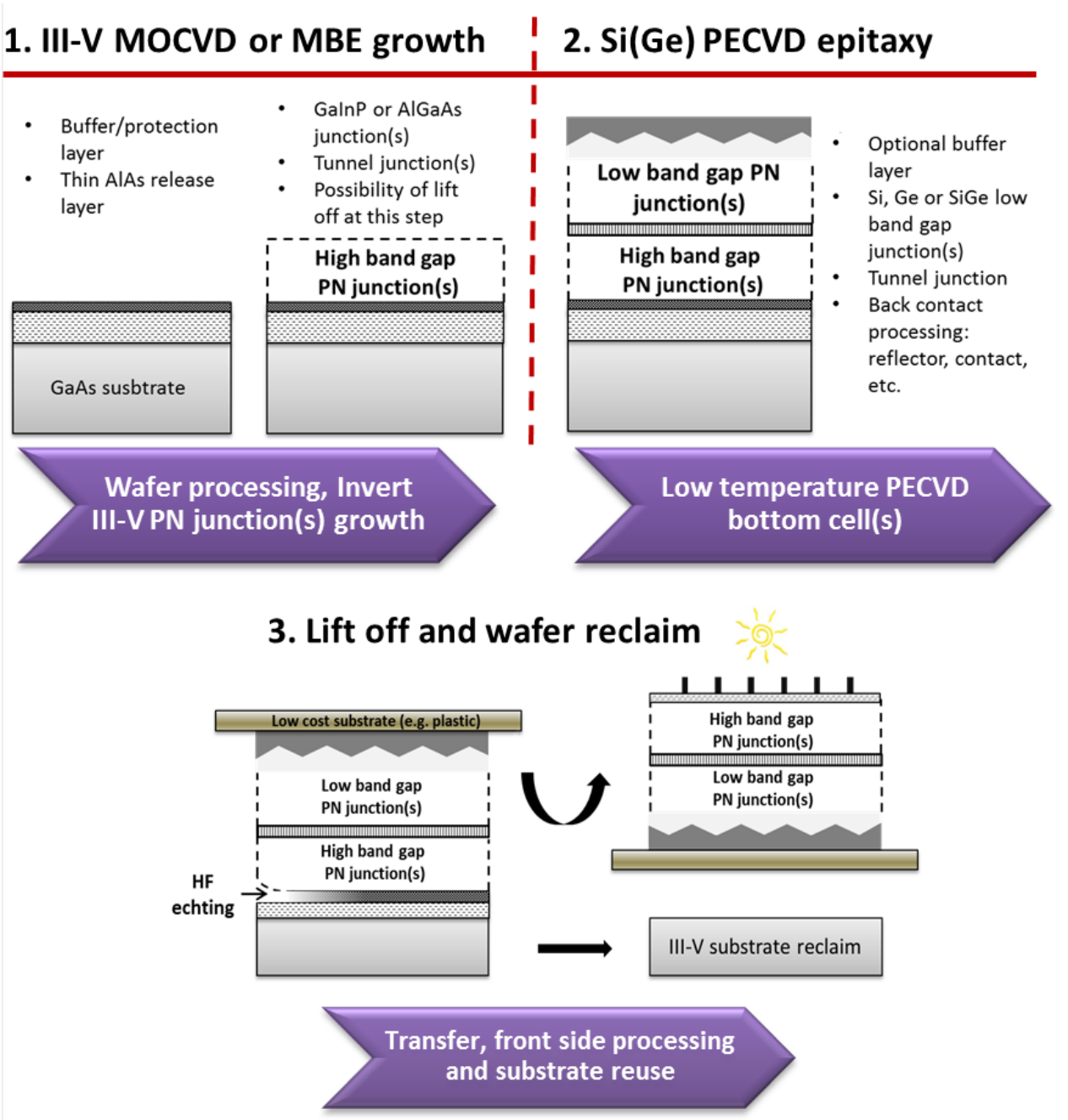


Fig. 5.12 – Description of the three fabrication steps of the inverted metamorphic tandem solar cell, combining III-V (MOCVD) and Si(Ge) (PECVD) materials, investigated in the French ANR research project IMPETUS.

substrate healing[57–59].

This approach is explored within the Framework of the French ANR research project **IMPETUS**. This project gathers 3 partners: LPICM, III-VLab and LGEP. The LGEP carries out the simulation and modelling part, as well as some material and device characterizations, the III-VLab brings its expertise in the field of III-V semiconductor growth and processing, and the LPICM focuses on low temperature PECVD epitaxial growth and solar cells.

[57] A. van Geelen et al., Materials Science and Engineering: B, **45**: 162–171, 1997.
[58] G.J. Bauhuis et al., Progress in Photovoltaics: Research and Applications, **18**: 155–159, 2010.
[59] K. Lee et al., Journal of Applied Physics, **111**: 033527–033527–6, 2012.

This reverse scenario of growing Si on III-V is not just a scientific curiosity, if features indeed several advantages:

- First of all, by using an inverted growth, the top cell is grown first lattice matched on a III-V wafer, and thus the crystal quality can be perfect. Inverted growth enables to reuse the wafer, and if this is repeated several times (e.g. few tens), then cell cost can decrease significantly.

- The second step, growing the Si(Ge) bottom cell, is done at low temperature by PECVD. This low temperature process minimizes thermal expansion and diffusion related problems.

- In this reverse approach, the polarity problems are completely suppressed, since the (Al)GaAs is grown lattice matched on GaAs, and the Si(Ge) grown on top of it is a non-polar material.

- Experimental[60] an theoretical work[61] seems to agree on the fact that kink formation energy (at least for 90° α glide) and dislocations migration energy are higher in silicon compared to gallium arsenide. Thus if grown at the same temperature, there might be less partial dislocations and stacking faults in Si grown on GaAs compared to GaAs grown on Si.

5.3.1 Estimation of maximum efficiency

Obviously, one of the main issues associated with this design and approach, is the finite thickness of the Si(Ge) bottom cell compared to classical III-V/Si tandem design which features a c-Si wafer of several hundreds of microns. With our PECVD epitaxial approach, which typically has a growth rate of $\sim$ 2Å/s, the thickest layers we could deposit so far was in the 5-10μm range. This is indeed limiting for bottom cell especially with the weak absorption of silicon. Several strategies can be used to increase the absorption and current in the bottom cell:

- The first evident option is to further increase the bottom cell thickness (e.g. around 20μm). This may be achieved by increasing the PECVD epi-Si deposition rate by a factor of about 3-4.

- To improve the absorption in the bottom cell, we can also alloy silicon with germanium, which results in a significantly higher and extended (above 1100nm) absorption for the same thickness.

- The second degree of freedom is the thickness of the top cell, it is indeed possible to thin down the top cell in order to achieve current matching if the bottom cell is the weakest. This point is explained in the paper of Connolly et al.[16]; in this situation, the gap combination should also be chosen more carefully, since the optimum is different from the situation of full absorption assumed in most of the efficiency maps from literature. This point is illustrated in Fig.5.3-a) and b); in the case of a 32% transparent top cell, the optimum band gap combination is 1.46/1.12 eV but the maximum theoretical efficiency is $\sim$ 6 points smaller compared to the full absorption case.

- And finally it should be possible to implement differential area illumination for the top and bottom cells. By intentionally reducing the area of the top III-V cell (e.g. by etching), additional illumination is allowed to impinge on the extra area, thus boosting the current generated by the bottom Si cell to match the current of the top one. The current matching condition corresponds to a certain ratio of the bottom cell area to the top cell area. This concept has already been successfully implemented in a GaInP/InGaAS/Si triple junction device reaching 25.5% in 2 terminal configuration under 1 sun[62].

[60] I. Yonenaga., Materials Transactions, **46**: 1979–1985, 2005.
[61] S. Oberg et al., Physical Review B, **51**: 13138–13145, 1995.
[16] J.P. Connolly et al., Progress in Photovoltaics: Research and Applications, , 2014.
[62] J. Yang et al., 27th EU PVSEC Proceedings, **1BO.12.6**: 160 –163, 2012.

To get more insight into the achievable current densities, we have performed optical modeling of the layer stack using materials refractive indexes and a transfer matrix code developed internally by M. Foldyna. Two examples of absorption splitting between the layers for two different stacks is shown in Fig.5.13-a) and b). The first simulated layer stack is $Al_{0.17}Ga_{0.83}As(1.63eV)/Si_{0.57}Ge_{0.43}(0.96eV)$ with $1.2/5.4\mu m$ thicknesses.

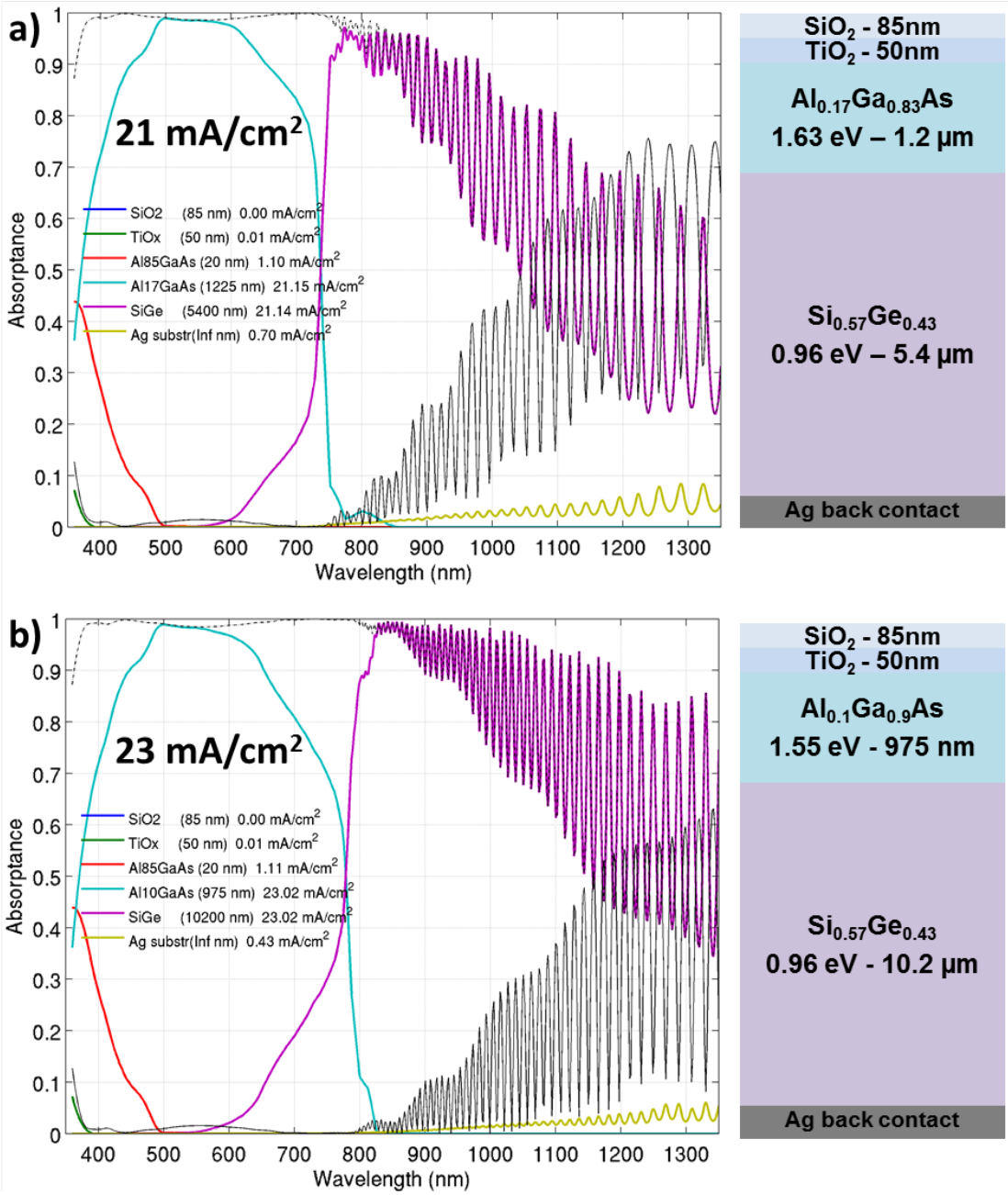
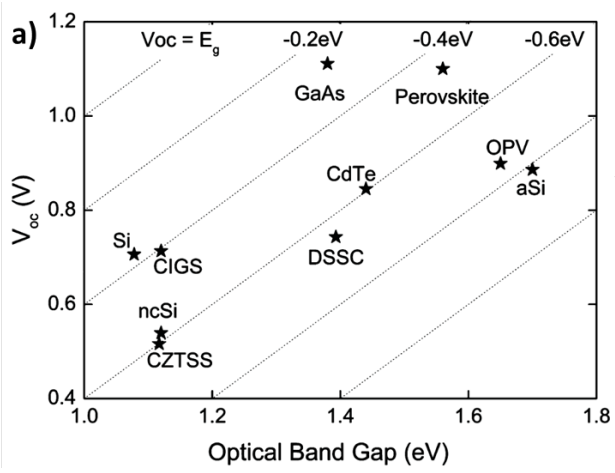


Fig. 5.13 – Absorption in a tandem solar cell modeled by transfer matrix method. Two tandem III-V/Si are presented: a) $Al_{0.17}Ga_{0.83}As/Si_{0.57}Ge_{0.43}$ $1.2/5.4\mu m$ reaching maximum of 21 mA/cm^2 (IQE=1). b) $Al_{0.1}Ga_{0.9}As/Si_{0.57}Ge_{0.43}$ $0.975/10.2\mu m$ reaching maximum of 23 mA/cm^2 (IQE=1).

A double layer SiO_2/TiO_2 with (85nm/50nm) is used as an anti-reflective coating, the 20nm window layer is composed of the high band gap $Al_{0.85}Ga_{0.15}As$, and silver is used as a back reflector. The absorption splitting between the different layers, as a function of wavelength, is shown in Fig.5.13-a). Small losses happen at the window layer ($\sim$ 1mA/cm^2), and at the back reflector ($\sim$ 0.7mA/cm^2). This latter loss can be reduced by using an optical spacer such as ITO in between the silver and the SiGe. Overall, this structure is lattice matched at 21 mA/cm^2, if we assume a 100% IQE.

The second simulated layer stack is $Al_{0.1}Ga_{0.9}As(1.55eV)/Si_{0.57}Ge_{0.43}(0.96eV)$ with $0.975/10.2\mu m$ thicknesses. The same anti-reflection layers and back reflector are used for this second design. The absorption splitting between the layers, as a function of wavelength, is shown in Fig.5.13-b). Of course the same loss happens at the window layer ($\sim 1mA/cm^2$), but the higher absorption in the bottom cell results in a smaller loss at back reflector ($\sim 0.4mA/cm^2$). Overall, this structure is current matched at 23 mA/cm^2, if we assume a 100% IQE (ideal material). In reality, IQE will be lower than one, especially in the bottom cell because of the presence of mismatch related defects. A 20 mA/cm^2 current density in such device would already be a significant achievement; however, if we use the concept of differential area illumination, 23 mA/cm^2 may be achievable.

Considering the V_{oc}, one can look into literature to estimate a realistic value. The optical band gap and V_{oc} of various solar cell technologies are reported in Fig.5.14-a)[63] . To date the best Si and GaAs cells show a V_{oc} 0.3 to 0.4 eV lower than their optical band gap. This figure of merit, $W_{oc} = E_g/q - V_{oc}$ is indeed very useful to evaluate the cell quality and compare different technologies. The best W_{oc} from literature[64–69] for GaInP, AlGaAs, GaAs, Si and GaAs are reported in Fig.5.14-b); the values are spread between 0.31 V for GaAs to 0.45 V for AlGaAs.



b)

Material	GaInP	AlGaAs	GaAs	Si	Ge
W_{oc} (V)	0.35	0.45	0.31	0.37	0.38

c)

Tandem band gaps	0.96/1.55	0.96/1.63	1.12/1.74
V_{oc} (V) Woc = 0.95V	1.56	1.64	1.9
J_{sc} (mA/cm²) Finite thicknesses	23	21	19
Efficiency (%) FF=80%	28.7	27.5	28.8

Fig. 5.14 – a) Open-circuit voltage V_{oc} versus optical band gap E_g for the best-in-class solar cells.[63] b) Numerical values of W_{oc}, the differences between band gap and V_{oc}[64–69]. c) Efficiencies for a III-V/Si tandem cell with thin Si(Ge) bottom cell thickness, based on current calculations shown in Fig.5.13 and W_{oc} from literature.

Based on these current and voltage considerations, we can try to estimate a realistic efficiency target for our III-V(MOCVD)/Si(PECVD) target device. Considering a W_{oc} of 0.45 V for the top cell and 0.5 eV for the bottom one, the predicted V_{oc} is in the range of 1.56 to 1.9 depending on the chosen gap combination (see Fig.5.14-c). The corresponding efficiencies, based on the current simulated from the transfer matrix method and a 80% FF, are in the range of 27-29%. While those numbers are only estimations made by hand, it underlines at least the paramount importance of the current density in this device design. Proper electrical and optical modeling of the device is being performed in the project IMPETUS to adjust gaps, materials and thicknesses and to get the highest efficiency. From a silicon point of view, efficiencies in the 27-29% range are of course attractive, however from a III-V point of view, the device should have efficiency higher than the best single GaAs cell (28.8%)[8] in order to be attractive.

[63] H.J. Snaith., The Journal of Physical Chemistry Letters, **4**: 3623–3630, 2013.
[64] R.R. King et al., Progress in Photovoltaics: Research and Applications, **19**: 797–812, 2011.
[65] J.F. Geisz et al., Applied Physics Letters, **103**: 041118, 2013.
[66] B.M. Kayes et al., 37th IEEE Photovoltaic Specialists Conference (PVSC), 000004 –000008, 2011.
[67] G.F. Virshup et al., Applied Physics Letters, **47**: 1319–1321, 1985.
[68] M. Taguchi et al., IEEE Journal of Photovoltaics, **4**: 96–99, 2014.
[69] N.E. Posthuma et al., IEEE Transactions on Electron Devices, **54**: 1210–1215, 2007.
[8] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **22**: 1–9, 2014.

5.4 III-V Solar cells and tunnel junctions

The III-VLab has a strong expertise in III-V materials for opto-electronic and photonic devices, but photovoltaics was not a research topic in this lab so far. LPICM has a strong expertise in silicon based solar cells, but much less knowledge in the field of III-V materials and photovoltaic devices. Thus one of the challenge and milestone of this thesis work was to fabricate classic III-V solar cells by building on the knowledge of both sides. In this section, we present our progress to reach state of the art III-V solar cells and tunnel junctions.

5.4.1 Literature overview

Gallium Arsenide (GaAs) solar cells have been around for many years: they were classically grown by MOCVD epitaxy on 0.35mm thick GaAs or Ge wafers. Already back to 1997, efficiencies around 24% were reported[57]; indeed the GaAs band gap, of 1.42 eV at room temperature, is close to the single junction optimum band gap for AM1.5G solar spectrum. Moreover, GaAs is a direct band gap semiconductor and only few microns are needed to absorb totally the photons above its band gap. Thus more recently, researchers have focused on the fabrication of ultra-thin ($\sim 2\mu$m) GaAs solar cells and their separation from the growth substrate. The detachment of the active material from the substrate enables the use of a back reflector, and thus a lifted-off solar cell requires approximately half of the active region thickness to absorb the same amount of photon compared to the wafer based cell. In addition the substrate may be reused, thus cutting down the cost. Miller et al.[70] have also shown that a reflective back contact enables photon recycling (when radiative recombination is dominant) by trapping light and concentrating the carrier in a thin layer; this results in an increased open circuit voltage compared to the wafer based equivalent device.

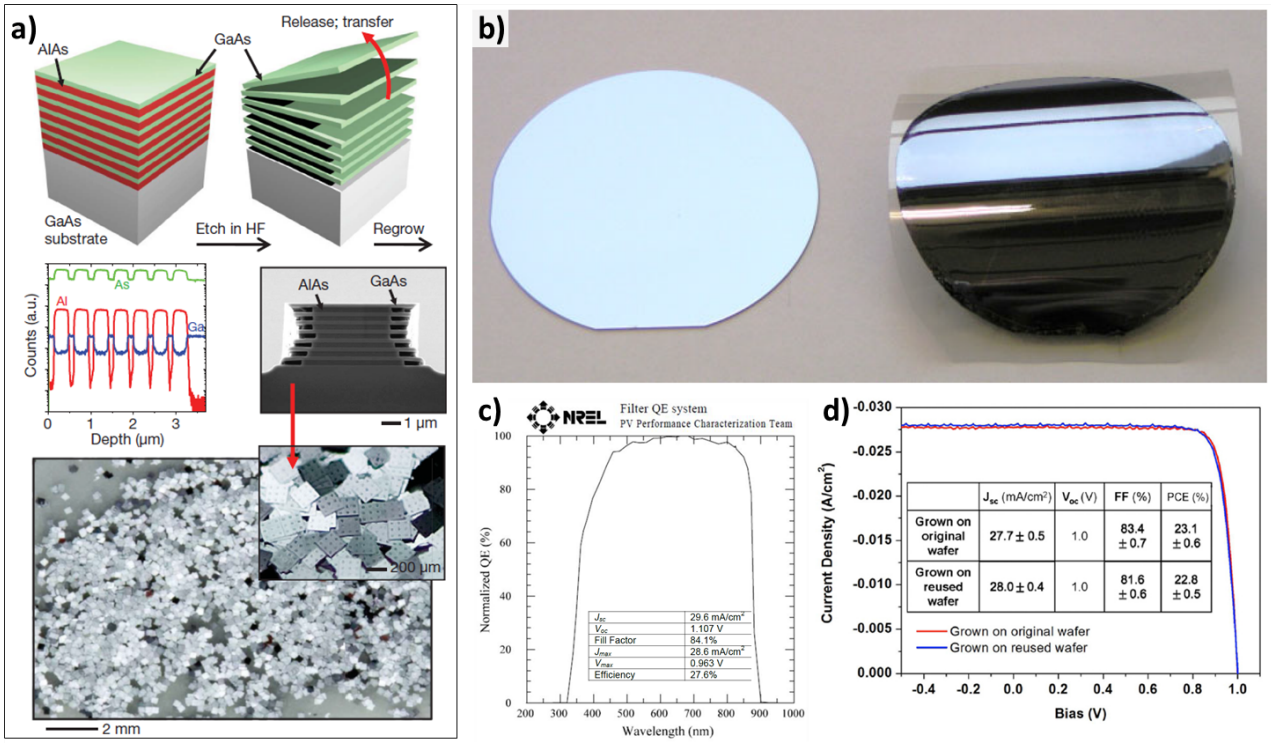


Fig. 5.15 – a) Lift-off of multiple GaAs layers and devices separated by sacrifical AlAs layers; from Yoon et al.[71]. b) Epitaxial lifted-off 2 inch. and 1μm thick GaAs layer reported on flexible substrate; from Schermer et al.[54]. c) EQE of Alta devices record solar cell reaching 28.8% under 1 sun[8,66]. d) Comparison of GaAs cells before and after substrate reuse; From Lee et al.[59].

[57] A. van Geelen et al., Materials Science and Engineering: B, **45**: 162–171, 1997.
[70] O.D. Miller et al., IEEE Journal of Photovoltaics, **2**: 303–311, 2012.

The recent progress, since $\sim$ 2005, in GaAs solar cells performance was made possible thanks to the layer lift-off processes. The detachment of monocrystalline layers from their growth substrate is since then an active research field, and various techniques are successfully explored: i) Control spalling[72,73] ii) Epitaxial lift-off with selective wet etching[56,74] iii) Laser assisted layer separation[75], etc. The wet etching of sacrificial layer beneath the epitaxial material is the most common approach. For instance, a thin (few tens of nanometers) AlAs between the wafer and the active GaAs epi-layer can be etched by HF with a selectivity in the range of 10^7! The lateral etching rate of AlAs is typically around few tens of mm per hour. It is possible to realize a stack of multiple devices separated by sacrificial AlAs layer in one single epitaxial run, and separate them during one wet etching step. With this approach Yoon et al.[71] could demonstrate the fabrication and separation of a stack of several near infrared imaging and photovoltaic devices (see Fig.5.15-a)). Large area lift-off has been achieved: as an example, the Fig.5.15-b) shows a 1 μm thick and 2 inch. diameter GaAs layer reported on flexible plastic substrate[54]. The GaAs solar cells have been extensively studied by a team from Radboud University[76,77], and the actual record cell has been achieved by Alta Devices, who has pushed the record up to 28.8% for 1 sun illumination[8,66]; the EQE curve of such record cell reaches 100% on a large spectral band, as shown in Fig.5.15-c). The same company also holds the GaAs module efficiency record of 24.1% [8,78]. Finally, the ability to reuse the substrate, after some chemical/mechanical polishing steps, without any decrease in solar cells performances has also been demonstrated[58,59]; this is illustrated in Fig.5.15-d).

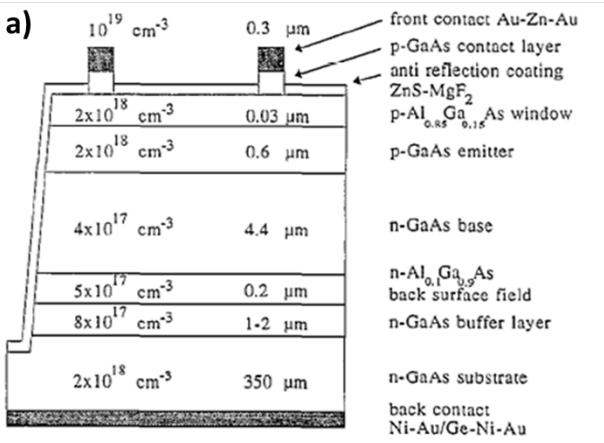
5.4.2 GaAs solar cells

We decided to start with the simplest configuration, which is GaAs cells on wafer, and to validate separately the lift-off process. The depositions were done in a MOCVD reactor at III-VLab, thanks to the expertise of J. Decobert, L. Dornelas and M. Pires. The first tested GaAs solar cell was inspired from design published in the late 90's[57]: the 23.9% efficiency GaAs cells layer stack, with doping and thicknesses, is shown in Fig.5.16-a). The layer stack of the first batch of solar cells we have deposited is shown in Fig.5.16-b). It features an $Al_{0.15}Ga_{0.85}As$ BSF doped at $7.10^{17}cm^{-3}$, a 4μm base GaAs n type doped at $4.10^{17}cm^{-3}$, a 600 nm thick p-type $2.10^{18}cm^{-3}$ GaAs emitter, a window layer made of $Al_{0.85}Ga_{0.15}As$, on top of which we deposited a TiO_2/SiO_2 double layer anti-reflection coating. The solar cell processing, which includes photo-lithography to define front contact, metal contact evaporation, annealing, chemical etching of the contact layer around the metal fingers, anti-reflection coating deposition, solar cell separation by diamond saw, report of the device on conductive handling substrate. Thus, the results presented here could not have been done without the precious help of the III-VLab team members: K. Louarn, C. Fortin, D. Make, H. Gariah, Y. Robert, J.-P. Truffer and A. Accard.

Based on literature considerations and the targeted 1 sun application, we have designed[79] a lithography mask to define cell area and contact scheme. The designed mask was composed of three different cell sizes: 3×3.6mm, 5×5mm and 10×10mm. More details about bus bar and fingers dimensions are

[72] D. Shahrjerdi et al., Advanced Energy Materials, **3**: 566–571, 2013.
[73] S.W. Bedell et al., IEEE Journal of Photovoltaics, **2**: 141 –147, 2012.
[56] C.-W. Cheng et al., Nature Communications, **4**: 1577, 2013.
[74] E. Yablonovitch et al., Applied Physics Letters, **51**: 2222–2224, 1987.
[75] G.J. Hayes et al., arXiv:1408.1977, 2014,
[71] J. Yoon et al., Nature, **465**: 329–333, 2010.
[54] J.J. Schermer et al., Thin Solid Films, **511-512**: 645–653, 2006.
[76] G.J. Bauhuis et al., Solar Energy Materials and Solar Cells, **93**: 1488–1491, 2009.
[77] J.J. Schermer et al., physica status solidi (a), **202**: 501–508, 2005.
[8] M.A. Green et al., Progress in Photovoltaics: Research and Applications, **22**: 1–9, 2014.
[66] B.M. Kayes et al., 37th IEEE Photovoltaic Specialists Conference (PVSC), 000004 –000008, 2011.
[78] L.S. Mattos et al., 38th IEEE Photovoltaic Specialists Conference (PVSC), 003187 –003190, 2012.
[58] G.J. Bauhuis et al., Progress in Photovoltaics: Research and Applications, **18**: 155–159, 2010.
[59] K. Lee et al., Journal of Applied Physics, **111**: 033527–033527–6, 2012.
[79] M. Steiner et al., Progress in Photovoltaics: Research and Applications, **19**: 73–83, 2011.

a)



Parameter	GaAs reference	ELO normal	ELO reversed
η (%)	23.9	9.0	9.9
A (cm^2)	1.00	1.00	1.00
V_{oc} (V)	1.038	0.965	1.016
I_{sc} (mA/cm^2)	27.15	24.66	24.20
FF	0.846	0.379	0.402

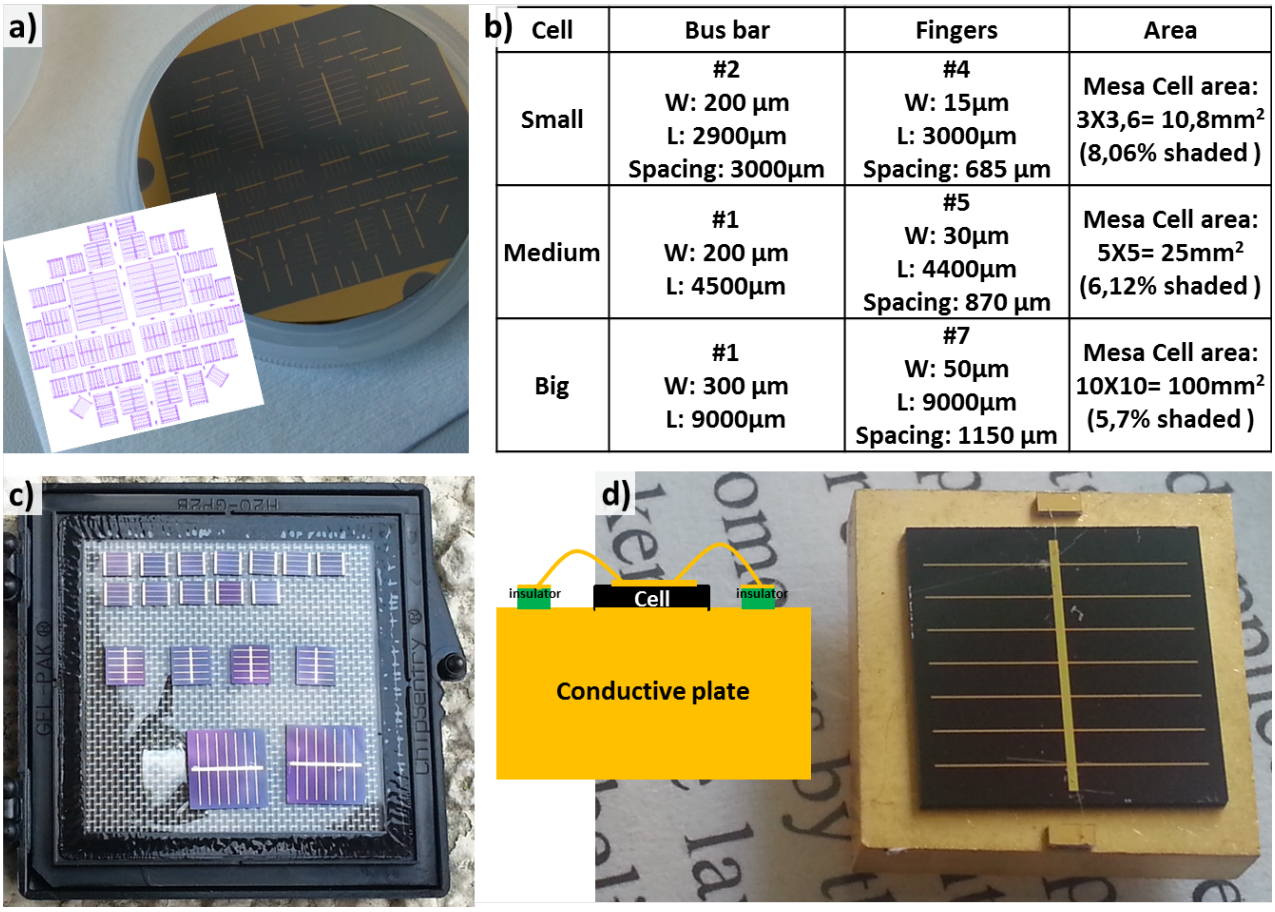
b)

Description	Material	Doping (cm^{-3})	thickness (µm)
Back contact	AuGe/Ni/Au		0.02/0.007/0.2
2inch (100) GaAs 2° miscut toward [110]	GaAs	n:Si 2.10^{18}	350
buffer layer	GaAs	n:Si 9.10^{17}	0.5
BSF	Al0.15Ga0.85As	n:Si 7.10^{17}	0.2
Base	GaAs	n:Si 4.10^{17}	4
Emitter	GaAs	p:Zn 2.10^{18}	0.6
Window	Al0.85Ga0.15As	p:Zn 2.10^{18}	0.03
Contact layer	GaAs	p:Zn 1.10^{19}	0.3
Double layer ARC	*TiO2/SiO2*		0.053/0.09
Contact grid	Pt/Au		0.15/0.25

Fig. 5.16 – a) Example of GaAs solar cell on wafer reaching 23.9% efficiency[57]. b) Details of the first batch of GaAs cell deposited in this thesis.

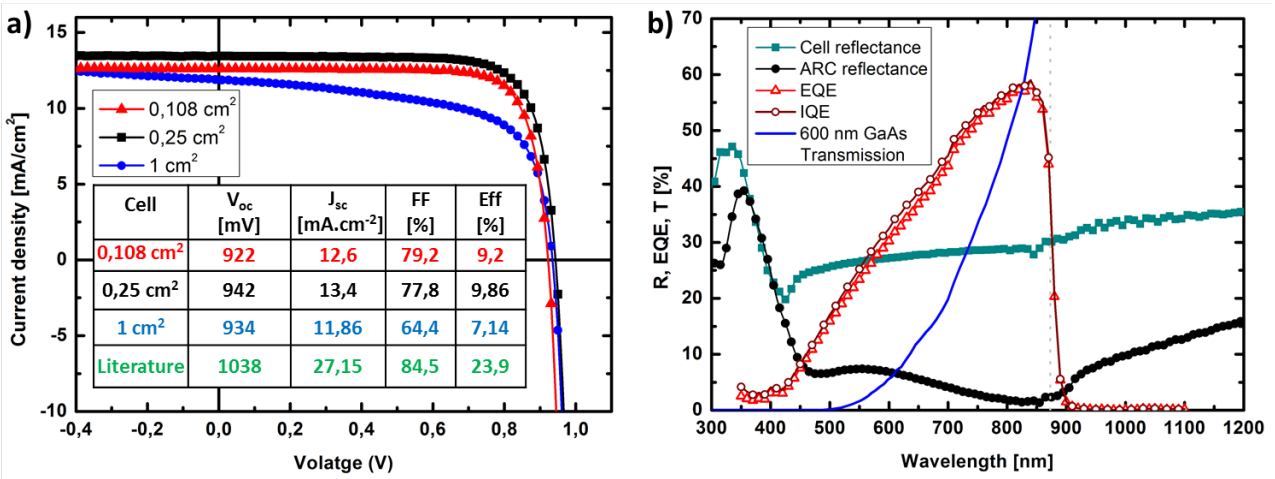
listed in Fig.5.17-b). Throughout this thesis we have been working on 2 inch. GaAs wafer size. The picture of front contact fingers are shown in Fig.5.17-a); cells distribution over the wafer surface is visible on the mask represented in the inset. After completing all fabrication processes, the cells are separated by diamond sawing, and the resulting devices are shown in Fig.5.17-c): from top to bottom one can see the 10.8mm^2, 25mm^2 and 1cm^2 GaAs cells. To facilitate handling and electrical characterizations, devices are glued to a conductive base and bus bar contacts are moved to the side of the device using wire contacts. A top view picture and cross section schematic of the final device, ready to be characterized under solar simulator and EQE set-up, is shown in Fig.5.17-d).

The J-V curve under 1 sun illumination of a single junction GaAs cells corresponding to the stack detailed in Fig.5.16-b) is displayed in Fig.5.18-a). The devices performances were unexpectedly low, to say the least. Indeed, the best performances of the three different cell sizes are listed in the inset, where the solar cells parameters of the corresponding literature device are shown. The 1cm^2 cell is the weakest one, with only $\sim$ 7% efficiency and a current density of 11.8 mA/cm^2; the V_{oc} is not too low, with 934 mV compared to the 1038 mV for the reference cell. But the current is more than 2 times less than the expected value. The two other cell sizes perform slightly better, with the "best" being the 0.25cm^2 reaching 9.8% efficiency. However the current was still stuck at 13.4 mA/cm^2 for this device, despite a relatively correct fill factor of $\sim$ 78 %. To identify the origin of the problem, we have measured reflectivity and EQE on the device; indeed a strong reflection of the front surface can lower significantly the J_{sc}. The total reflectance measured with an integration sphere is shown in Fig.5.18-b): the square symbols correspond to the measurement before depositing the TiO_2/SiO_2 anti-reflection coating (ARC), and the curve with circle symbols is measured on the final device with the double layer ARC. One can see that the reflectivity remains very low, between 5 and 10% on a large spectral range, and thus we could not attribute the low J_{sc} of the device to a reflection problem. Both EQE and IQE measured on the best 0.25cm^2 device are shown on the same graph: the sharp drop around 875 nm, corresponding to GaAs band gap energy, is characteristic of direct band gap semiconductors. However, the poor cell performance is clearly confirmed by a peak EQE value lower than 60% and by very low EQE values in the 400-600 nm range.



Cell	Bus bar	Fingers	Area
Small	#2 W: 200 µm L: 2900µm Spacing: 3000µm	#4 W: 15µm L: 3000µm Spacing: 685 µm	Mesa Cell area: 3X3,6= 10,8mm² (8,06% shaded)
Medium	#1 W: 200 µm L: 4500µm	#5 W: 30µm L: 4400µm Spacing: 870 µm	Mesa Cell area: 5X5= 25mm² (6,12% shaded)
Big	#1 W: 300 µm L: 9000µm	#7 W: 50µm L: 9000µm Spacing: 1150 µm	Mesa Cell area: 10X10= 100mm² (5,7% shaded)

Fig. 5.17 – a) Picture of front metal fingers defined by lithography on a 2 GaAs inch. wafer. The mask defining solar cells areas is shown in the inset. b) Bus bar and finger dimensions for the three tested cells sizes. c) Picture of finished GaAs cell after sawing. d) Schematic and picture of a 1cm^2 GaAs cell glued on a conductive base.



Cell	V_{oc} [mV]	J_{sc} [mA.cm^{-2}]	FF [%]	Eff [%]
0,108 cm²	922	12,6	79,2	9,2
0,25 cm²	942	13,4	77,8	9,86
1 cm²	934	11,86	64,4	7,14
Literature	1038	27,15	84,5	23,9

Fig. 5.18 – a) J-V curve and solar cell parameters of the first batch of GaAs cell corresponding to the layer stack described in Fig.5.16-b). b) Total reflectance measured before (squares) and after (circles) the deposition of double layer ARC. EQE (triangles) and IQE of the 0.25cm^2. The transmission of a 600 nm GaAs layer is shown as an indicative basis.

From this EQE analysis, we could infer that the problem was happening in the front side of the cell; this could be linked the material itself or something wrong during solar cell processing steps. We were first suspecting that the emitter layer was too thick and with a too high doping level. Indeed, the emitter layers used in our devices were 600 nm thick, and thus should the doping be too high, very few minority carriers created in this part of the cell would then be collected. The emitter layer would in this case act as a filtering layer for the solar spectrum, and as shown in Fig.5.18-b), the transmission of a 600 nm GaAs is very poor for wavelength below 800 nm.

To investigate further this problem, we have performed both PC1D simulations. Using the material data base provided with PC1D, we could model a GaAs cell with various front emitter doping levels. The influence of the emitter doping (from 2.10^{18}cm^{-3} to 8.10^{19}cm^{-3}) on the solar cell internal quantum efficiency (IQE) is shown in Fig.5.19-a). One can see that an emitter doping in the range of few 10^{19}cm^{-3} results in a similar quantum efficiency profile, at least qualitatively. Thus, we decided to perform secondary ion mass spectroscopy (SIMS) to get quantitative information of chemical element concentration as a function of depth inside the cell[1]. While no significant deviation from the expected emitter doping level was detected, another important information could be found with this technique. The SIMS profile of oxygen (triangles), gallium (circles) and aluminium (squares), in atom per cm^{-3} plotted as a function of depth from GaAs cell surface, are shown in fig.5.19-b).

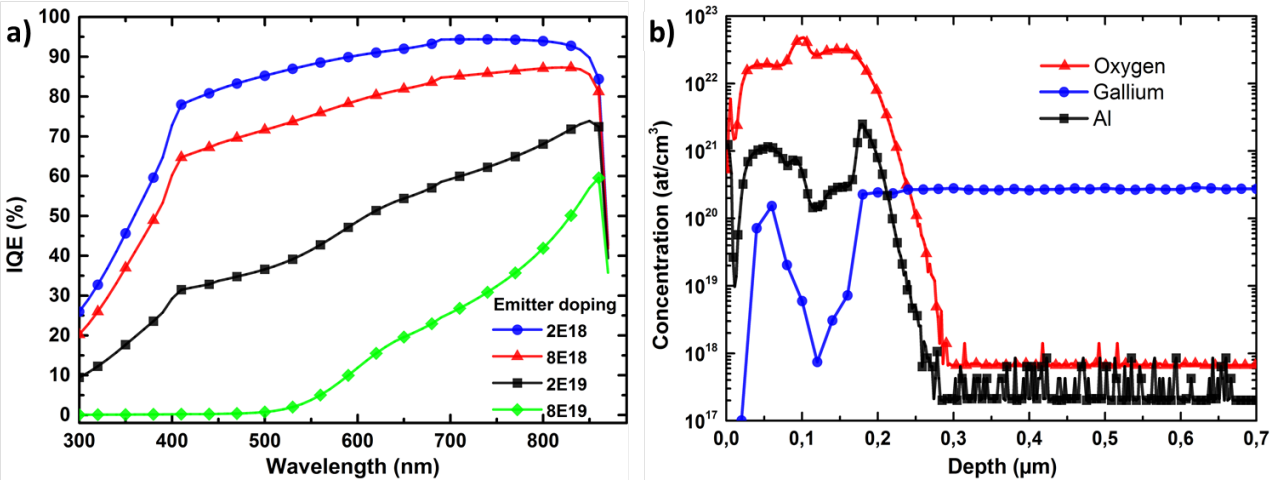


Fig. 5.19 – a) Influence of emitter doping (from 2.10^{18}cm^{-3} to 8.10^{19}cm^{-3}) on GaAs solar cell IQE, for the design shown in Fig.5.16-b), as modeled by PC1D software. b) SIMS profile of oxygen (triangles), gallium (circles) and aluminium (squares) in the first hundreds of nanometers of GaAs cell surface.

The cell surface layers consists in SiO_2(90nm)/TiO_2(55nm) antireflection coating deposited on $Al_{0.85}Ga_{0.15}As$(30nm)/GaAs(600nm) (see Fig.5.16-b)). The Al peak visible around 200nm depth corresponds to the window layer; the high level of Ga and Al detected in the first 100nm are probably due to mass interferences. But overall the striking feature is the oxygen content in the range of few 10^{22} atoms per cm^{-3}; this is the same order of magnitude than the matrix elements. This analysis has thus revealed a completely oxidized window layer. In fact, the oxidation rate of AlGaAs alloys increases significantly with the aluminium content in the layer; consequently the $Al_{0.85}Ga_{0.15}As$ window layer is very sensitive to the presence of oxygen. In fact two obvious source of oxygen were responsible for this: i) First, during the processing of the solar cell, the window layer was exposed to the air. Indeed, after wet etching of the cap GaAs layer and before deposition of ARC, there was roughly 1 hour during which AlGaAs was air-exposed. ii) Secondly, the direct deposition of dielectric ARC layers, mainly composed of oxygen, on the AlGaAs window was probably not a very wise decision. TiO_2/SiO_2 anti-reflective properties are comparable with that of ZnS/MgF_2, but this latter ARC is the most widely used in III-V based PV, probably also because it suppresses the oxygen related problems.

[1]The SIMS measurement were done by M. Quillec at Probion.

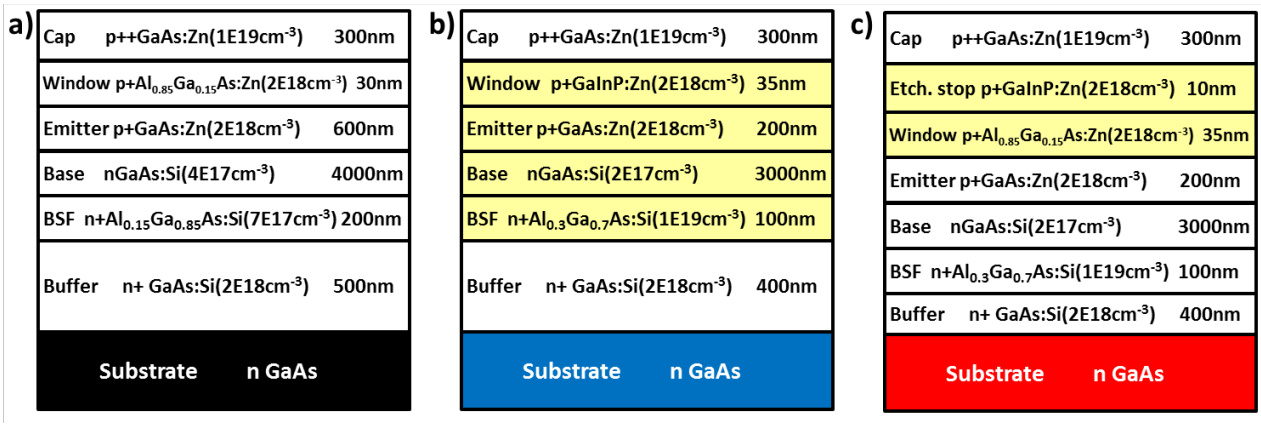


Fig. 5.20 – a) Layer stack used in the first batch of GaAs cells. b) Second tested design; changes with respect to the first design are highlighted in yellow: the thicknesses have been adjusted and a GaInP instead of AlGaAs was chosen for the window. c) Third GaAs design; changes compared to design 2 are highlighted in yellow: the window is made of AlGaAs and a thin GaInP layer is used as an oxidation barrier and etch stop layer.

Unfortunately, deposition tools for ZnS and MgF_2 materials were not available in the III-VLab. Thus we decided to keep the TiO_2/SiO_2 ARC and adapt the front cell design to get rid of oxidation problems. Two new designs were tested; they are described in fig.5.20-b and c). Based on comparison with literature and the above mentioned identified problem, we have changed the following parameters:

- For the second device, the window layer was made of GaInP which is less sensitive to oxidation compared to AlGaAs. The emitter and absorber layers thicknesses were reduced to 200 and 3000 nm respectively. The BSF Al content and doping was increased for better repulsion of minority carriers. Details are shown in Fig.5.20-b).
- For the third design, the same BSF, absorber and emitter layers compared to the second design were used. However, the window was made of an AlGaAs layer protected by 10nm of GaInP. This layer was chosen to act as an oxidation barrier and etch stop layer (when etching the top cap layer). Details are shown in Fig.5.20-c).

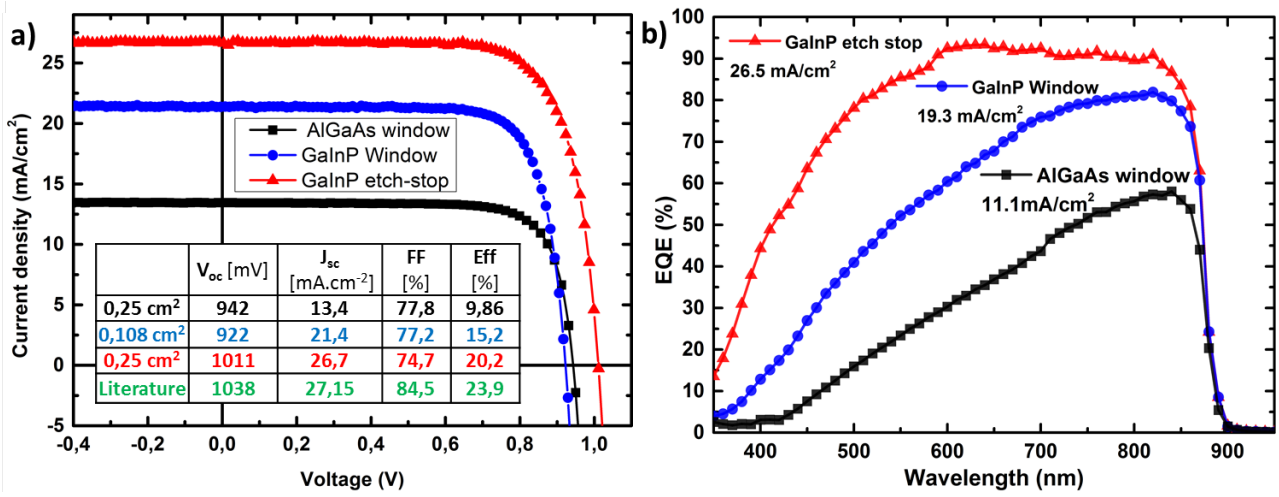


Fig. 5.21 – a) J-V curves measured under 1 sun AM1.5G spectrum for the three GaAs cell design shown in Fig.5.20. The solar cell parameters are listed in the inset. b) Corresponding EQE measurements, with J_{sc} calculated by integration with solar spectrum.

The same process and contacting scheme was used for the second and the third design, and the resulting IV curves are displayed in Fig.5.21-a). A net increase is observed for the two new cells: the GaInP window layer design reaches 21.4 mA/cm^2 and 15.2% efficiency, and the device with AlGaAs window and GaInP barrier layer reaches a 26.7mA/cm^2 J_{sc} and 20.2% efficiency. The best cell has a V_{oc} of 1011 mV which is very close to the 1038 mV reported in literature for similar device. Our best cell is still $\sim$ 4% in term of absolute efficiency behind the reference cell; this is mainly explained by our fill factor being 10% lower. But the improvement paths are clearly identified: series resistance can be reduced significantly by increasing the doping in GaInP barrier layer, and the front grid pattern can be further optimized. The corresponding EQE curves are shown in Fig.5.21-b). The same trend is confirmed by this technique: i) the GaInP/AlGaAs window cell (triangles) has the best EQE, reaching 90% in the range of 600-800 nm. The J_{sc} calculated from integration with solar spectrum is 26.5 mA/cm^2, thus very close to the value measured with the solar simulator. ii) The GaInP window solar cell (circles) has an intermediate EQE, which by integration gives a 19.3 mA/cm^2. iii) The first AlGaAs window cell (squares) has the poorest EQE which corresponds to 11.1 mA/cm^2. This two last cells have a roughly 2mA/cm^2 lower J_{sc} as calculated from EQE compared to the solar simulator value. This may be explained by non-uniform performance of the cell (the EQE beam is probing only 2-3 mm^2). The low value of the GaInP window cell's EQE at short wavelength suggests that there may still be front surface recombination problems for this architecture. Overall, thanks to the complementary expertise of both LPICM and III-VLab, starting from scratch we could go beyond the symbolic 20% efficiency threshold for GaAs cell, within a year.

5.4.3 Tunnel junctions

In monolithic multijunction solar devices, the sub-cells are connected by means of tunnel junctions (TJ), which consist in pn junctions with very high doping levels in order to position the Fermi level in the conduction or the valence band. For this type of degenerated p-n junctions, the classical diode model is no longer valid, since the current can flow as the result of quantum mechanical electron tunneling across a potential barrier.

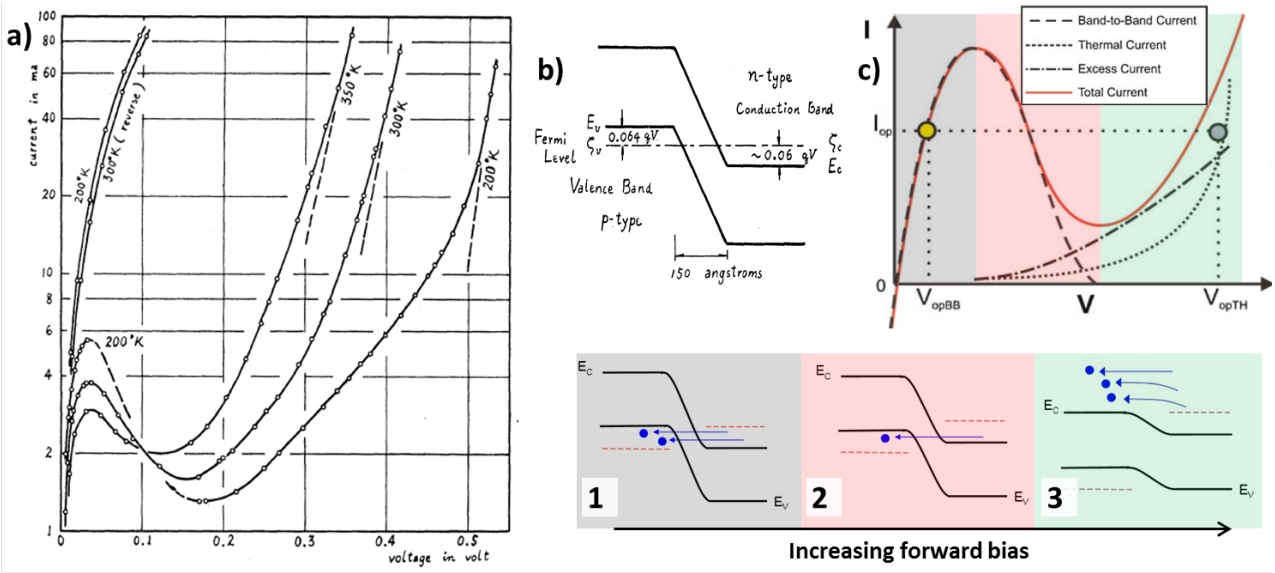


Fig. 5.22 – a) Current-voltage characteristics of the first reported tunnel junction, based on germanium[80]. b) Corresponding schematic of energy band diagram. c) Ideal IV curve[81], and corresponding band diagram, of a tunnel junction showing three regions: 1) At small forward bias, a high tunneling current is obtained, 2) At medium forward bias, the tunnel current decreases (negative differential resistance - NDR). 3) The classic diode current is obtained for higher bias.

The first tunnel diode was reported in 1958 by L. Esaki[80], and the device longevity has been tested recently: half a century later, the same tunnel diode has shown only a 3.3% performance decrease[82] (peak tunneling current)! The IV characteristic of the first TJ, made of germanium layers doped in the 10^{19}cm^{-3} range, and its band diagram are shown in Fig.5.22-a,b). Compared to the classic diode shape, a zigzag is visible in the low bias region. This behavior is indeed explained by the quantum mechanism of electron tunneling. The ideal IV curve of a TJ[81] is shown in Fig.5.22-c), together with the band diagram evolution as a function of the applied forward bias. Three regions can be distinguished:

- 1) The low bias region. Here the resistor like IV shape is due to band to band tunneling: carriers quantum mechanically tunnel through the thin depletion region of the highly doped p-n junction. This behavior is limited by a maximum current density J_{peak} at a voltage V_{peak}. This region is the most important one, since multi-junction solar cells operate in this part of the I-V characteristic, and thus it determines the voltage drop during solar cell operation.

- 2) As forward bias continues to increase, the number of electrons in the n-side facing empty states of similar energy in the valence band decreases (see schematic 2 in Fig.5.22-c)). As a consequence, the tunneling current drops from the peak to the valley: this is the so-called negative differential region (NDR). This region can cause the measurement circuit to become unstable[81,83].

- 3) Beyond the valley, the current comes from the contribution of excess current and thermal current, which is the current normally associated with a p-n junction, that appears at higher forward bias compared to the tunneling current.

The importance of tunneling current can be easily understood by comparing the voltage drop in a classical p-n diode, given by the thermal current, and the voltage drop given by the tunneling mechanism (See yellow an grey points in fig.5.22-c). The initial part of the TJ characteristic is therefore very important since it provides a low resistance path for carriers to bypass thermal current region. TJs are usually characterized by two figures of merit: the peak tunneling current J_{peak} and the equivalent resistance measured in the tunneling part of the IV curve; the peak current should peak as high as possible and the resistance as low as possible. For example, if we take a tandem cell with 21mA/cm^2 under 1 sun illumination, the resulting current density at 400 suns becomes 8.4 A/cm^2 (see Fig.5.23-a)). For a triple junction having 14mA/cm^2 under 1 sun, the current density is pushed to 5.6A/cm^2 at 400 suns. And if the tunnel junction has a lower J_{peak} compared to the device J_{sc}, then the tunnel diode works in the region where the thermal current dominates and thus a high voltage drop occurs over the tunnel diode. In this case the IV curve is affected by a significant valley drop, and the total current rise again at high voltage with J_{peak} being the maximum current density. This is illustrated in Fig.5.23-b), on a triple junction device measured under increasing illumination by Guter et al.[83]. In practice is better to have J_{peak} much higher than J_{sc} to cope for non-uniformities in the illumination intensity and increase the margin for eventual degradation due to thermal load during sub-cells growth. With the IMPETUS approach, this latter problem is suppressed since the sub-cell is grown below 200°C.

[80] L. Esaki., Physical Review, **109**: 603–604, 1958.
[82] L. Esaki et al., Nature, **464**: 31–31, 2010.
[81] J.F. Wheeldon et al., Progress in Photovoltaics: Research and Applications, **19**: 442–452, 2011.
[83] W. Guter et al., IEEE Transactions on Electron Devices, **53**: 2216–2222, 2006.

a)	1 sun	20 suns	250 suns	400 suns
J_{peak} min value (A/cm²) (Tandem J_{sc} 21mA/cm²)	0,021	0,42	5,25	8,4
J_{peak} min value (A/cm²) (Triple J_{sc} 14mA/cm²)	0,014	0,28	3,5	5,6

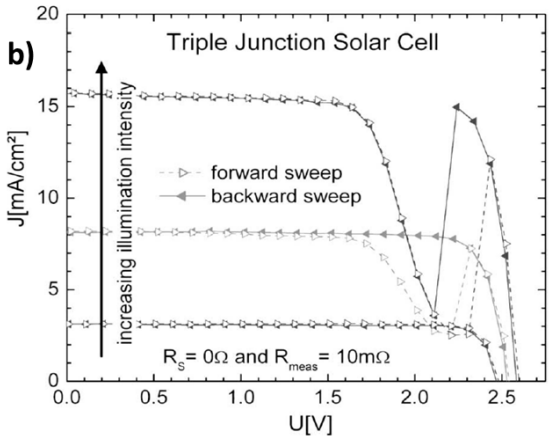


Fig. 5.23 – a) Example of peak current densities (J_{peak}) of a tandem and triple junction device under various concentrations. b) Experimental IV curve of a triple junction with increasing illumination intensity: at high illumination intensity, when J_{sc}>J_{peak}, a significant drop in IV characteristic becomes visible[83].

From an optical point of view, the TJ should be as transparent as possible to transmit the photons potentially absorbable by the sub-cells, and thus have a band gap higher than sub-cells. However, the peak current density is reported to decrease exponentially with the band gap according to[81,84]:

$$J_{peak} \propto exp\left(\frac{-{E_g}^{3/2}}{\sqrt{N_{eff}}}\right) \tag{5.1}$$

where E_g is the TJ semiconductor material band gap and N_{eff} the effective doping defined with the n and p side doping concentrations as follow: $N_{eff} = n.p/(n+p)$. This indicates that for the same effective doping a higher band gap semiconductor used in a TJ will result in a significantly lower tunneling peak current. In addition, for high band gap materials like AlInP, InGaP or $Al_xGa_{1-x}As$ (x>0.45), it is relatively difficult to obtain high carrier concentration (>10^{19}cm^{-3}). Thus a balance should be found between high optical transparency and high peak tunneling current; this balance depends on the targeted operating concentration ratio. A good review and comparative study on the different materials used in TJ has been published by Wheeldon et al.[81]; AlGaAs/GaAs TJs seems to be a good compromise, with extremely high peak tunneling current (>10^4A/cm^2) reported in literature[85].

The contour plot of N_{eff} as a function of p-side and n-side doping concentration is shown in Fig.5.24-a). N_{eff} can be maximized if p=n, but increasing the doping level of one side only will result in marginal N_{eff} improvement. The influence of N_{eff} on the tunneling current is detailed in Fig.5.24-b): using BCBV software[2], which features a simple tunneling model, three GaAs/GaAs TJ were modeled, with effective doping level of 1.5×10^{19} (squares), 2.5×10^{19} (circles), and 5×10^{19}cm^{-3} (triangles), and equal doping on n and p-side. The corresponding band diagrams are shown in Fig.5.24-c). In reality, to get quantitative information, a simulation that includes several tunneling mechanism (local, non-local, trap-assisted, etc.) should be used[86,87]. Here the result produces at least qualitative information: a change in N_{eff} by a factor of two can result in two orders of magnitude higher peak tunneling current. The higher doping on both sides of the TJ produces a higher band bending which facilitates tunneling.

[84] G.J. Bauhuis et al., Progress in Photovoltaics: Research and Applications, **22**: 656–660, 2012.
[85] I. García et al., Journal of Physics D: Applied Physics, **45**: 045101, 2012.
[2] BCBV software is developed internally at III-VLab by J.F. Palmier.
[86] M. Baudrit et al., IEEE Transactions on Electron Devices, **57**: 2564–2571, 2010.
[87] M. Hermle et al., Progress in Photovoltaics: Research and Applications, **16**: 409–418, 2008.

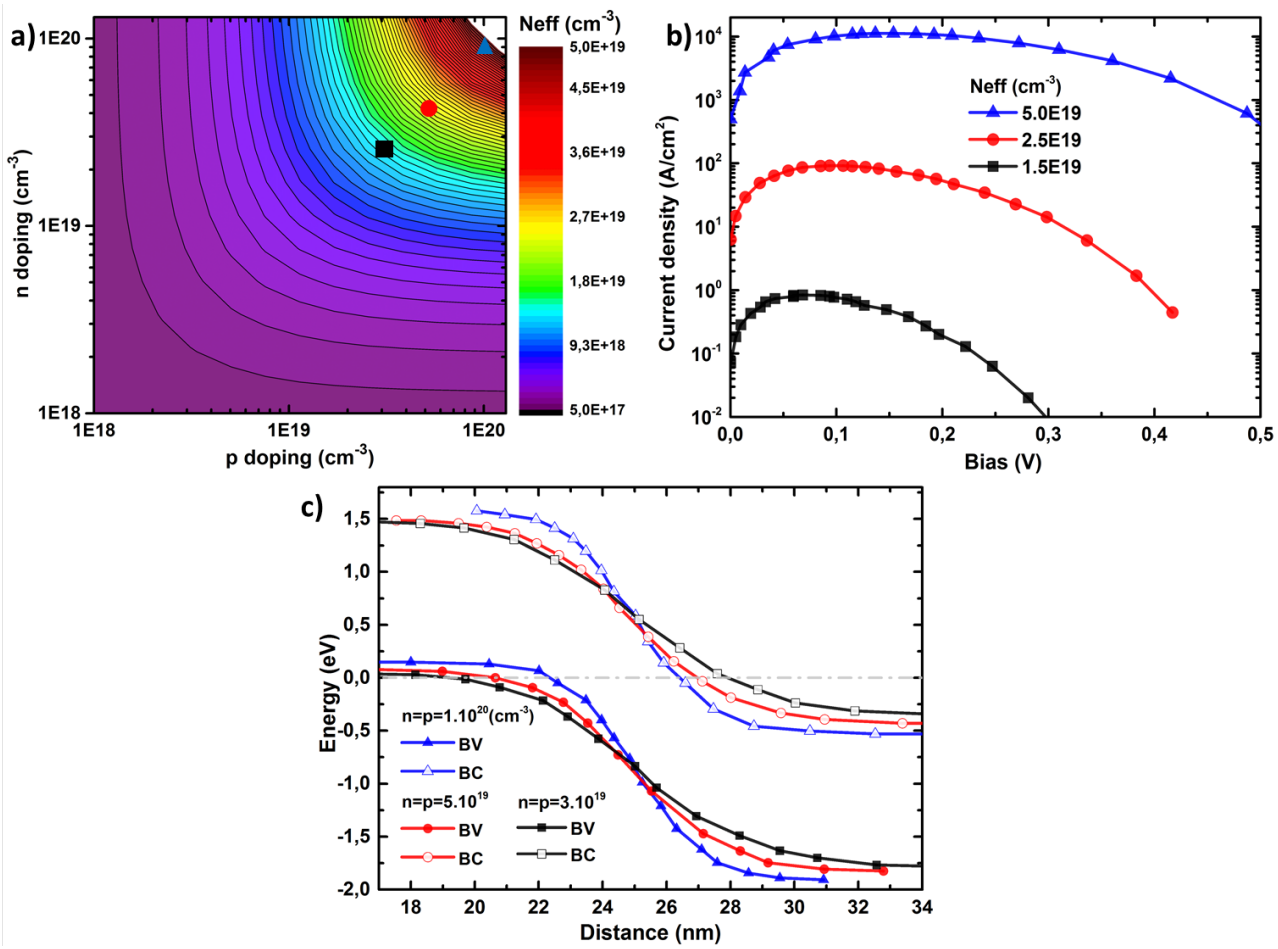


Fig. 5.24 – a) Contour plot of the TJ effective doping, $N_{eff} = n.p/(n+p)$, as a function of n-side and p-side doping concentration. b) Simulations of tunneling current with BCBV software, for a GaAs/GaAs TJ with effective doping of 1.5×10^{19} (squares), 2.5×10^{19} (circles) and 5×10^{19}cm^{-3} (triangles). c) Band diagram for the three values of N_{eff}, as modeled by BCBV.

The first experimental TJ diode we made was a GaAs/GaAs device with p++GaAs(3×10^{19}cm^{-3}) and n++GaAs(8×10^{18}cm^{-3}); this corresponds to a N_{eff} of 6×10^{18}cm^{-3}; in fact achieving higher doping with silicon in GaAs was difficult, probably due to the amphoteric nature of Si dopant in GaAs. More details about the layer stack are shown in Fig.5.26-a). The resulting IV curves are displayed in Fig.5.25: measured with two probes (triangles and pentagons) on the same diode, and four probes configuration (circles and squares) for two diodes at different locations on the wafer. The first comment is that all the curves exhibit the expected TJ IV shape with a peak current at low bias, then a valley and then the classical diode current. The importance of a good contacting scheme is underlined by the measurements with 2 probes: the inferior ohmic contact quality with two probes configuration results in additional series resistances, and thus produces a shifted peak position. The two diodes measured with four probes have reproducible IV curves, with similar features in the tunneling region: low resistance as judged by the slope at the origin, and a peak tunneling current around 7.5 A/cm^2. Those performances are very good, especially given the relatively low level of doping used in this device; this TJ could be used in tandem or triple junction with low to medium concentration.

Thinking about the subsequent PECVD epitaxial growth of silicon, as scheduled in IMPETUS project, this tunnel junction has been exposed to a hydrogen plasma, to track the modifications of its electrical properties. Many works have been done in the eighties about effect of H_2 plasma

exposure of III-V compounds. Hydrogen is known to passivate doping elements in III-V layers[88–90], but also crystalline defects such as dislocations[91] and deep level defects[92,93]. Annealing around 400°C is mentioned to be sufficient for doping recovery, but to suppress the passivation effect on deep levels, annealing around 600°C would be required[92]. However, upon H_2 plasma exposure, III-V layers may also be damaged (e.g. if high power is used); and H_2 plasma-related recombination levels generation has already been reported[94,95]. Given the variability of the effects reported in literature, it was hard to predict in advance the influence of a H_2 plasma on our TJ.

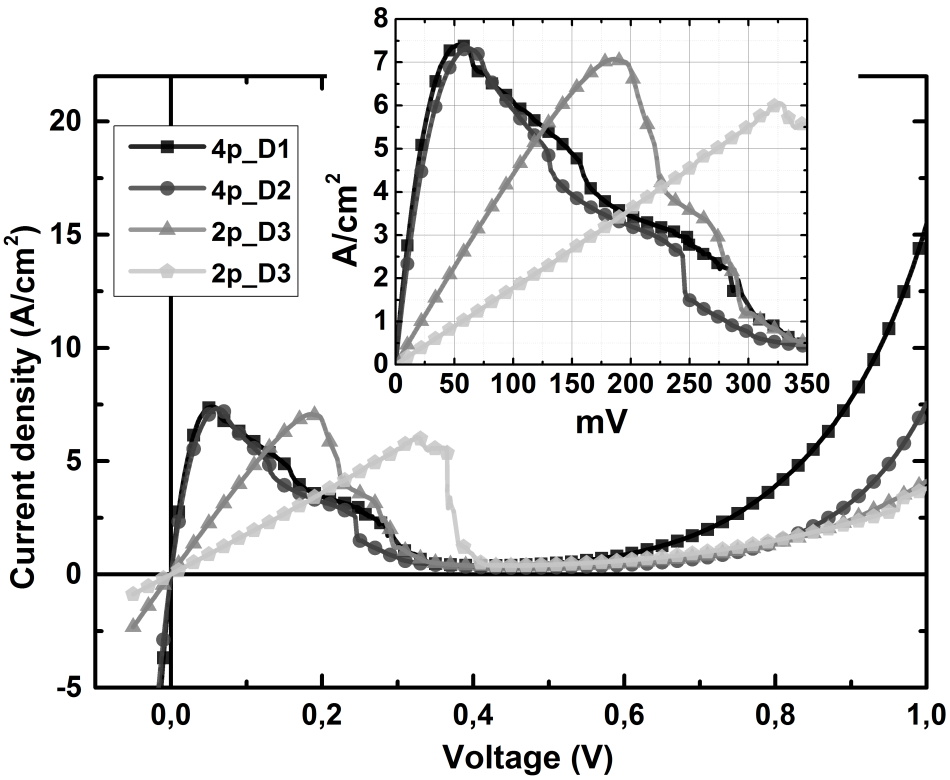


Fig. 5.25 – GaAs/GaAs tunnel junction with $N_{eff} = 6{\times}10^{18}\text{cm}^{-3}$, measured with two probes (triangles and pentagons) and four probes (circles and squares) electrical contacting scheme.

The experimental result, after plasma exposure (2 Torr, 80mW/cm^2, 180°C, 15min), is shown in Fig.5.26-d). The IV curves measured before (triangles) and after (circles) are plotted on the same graph. It should be mentioned that the sample exposed to the H_2 plasma was annealed for 3 min at 400°C in a nitrogen atmosphere, after the plasma step, to get ohmic contact; the other sample received the same treatment. The striking feature is the increase of the peak tunneling current by a factor of 3; similarly, the resistance at J_{peak} decreases by almost three times. Such huge improvement of the tunneling properties may be explained by the generation of defects; such defects could enhance the trap assisted tunneling. This hypothesis is strengthened by the observed strong increase of the valley current. Indeed several studies mention an increase of the valley current in Esaki diode with

[88] J. Chevallier et al., Applied Physics Letters, **47**: 108–110, 1985.
[89] S.J. Pearton et al., Journal of Applied Physics, **59**: 2821–2827, 1986.
[90] B. Theys et al., Journal of Applied Physics, **80**: 2300–2304, 1996.
[91] S.J. Pearton et al., Applied Physics Letters, **51**: 496–498, 1987.
[92] W.C. Dautremont-Smith., MRS Online Proceedings Library, **104**: 313, 1987.
[93] J. Lagowski et al., Applied Physics Letters, **41**: 1078–1080, 1982.
[94] G. Wang et al., Japanese Journal of Applied Physics, **38**: 3504, 1999.
[95] A. Jalil et al., Journal of Applied Physics, **66**: 5854–5861, 1989.

impurity concentration or with recombination centers such as crystalline defects[96,97]. To further assess the link between H_2 plasma and the creation of deep level defects, characterizations such as DLTS (deep level transient spectroscopy) should be performed. Also, it could be useful to test how stable this improvement is under real multijunction working conditions.

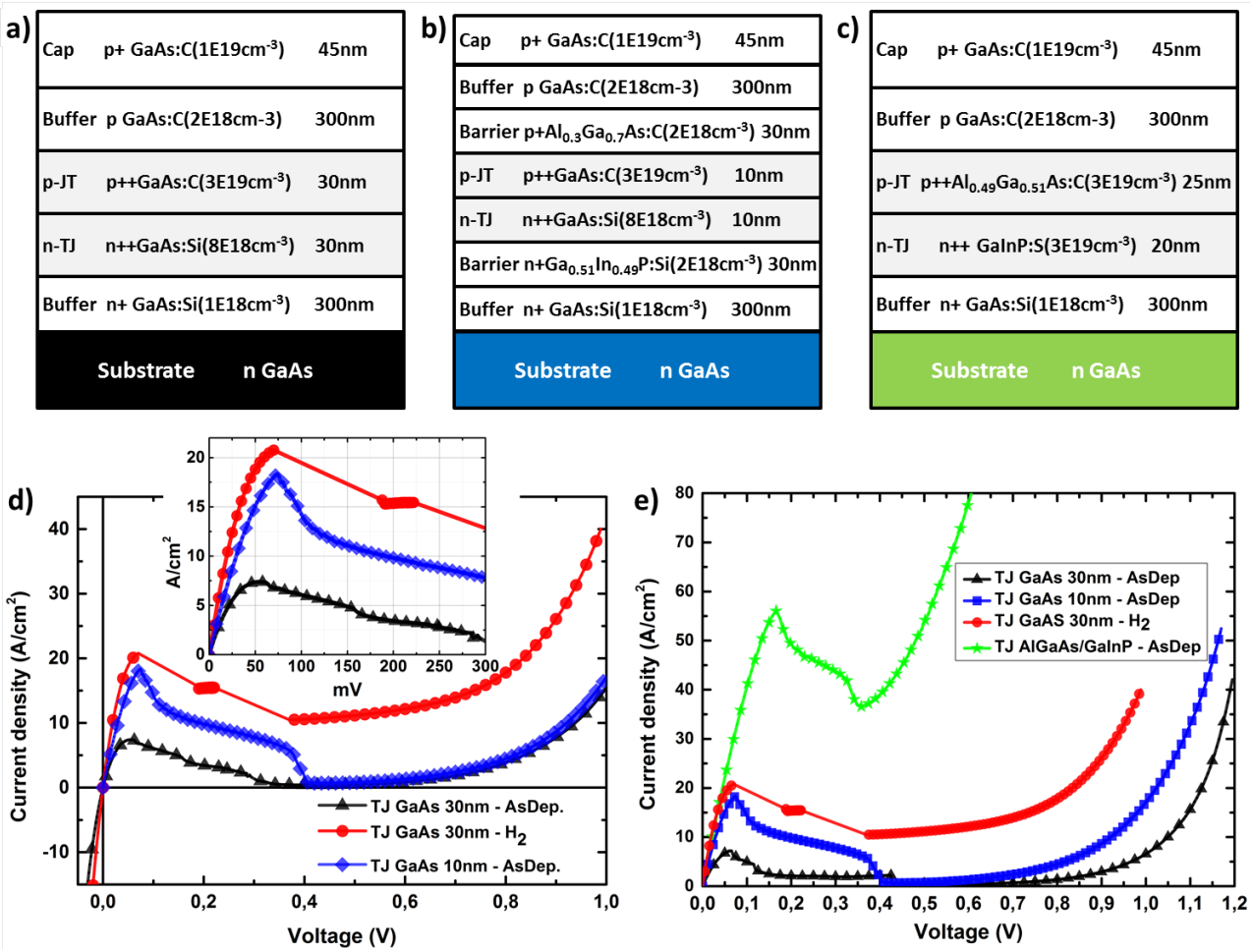


Fig. 5.26 – a) GaAs TJ design with 30nm doped layers, b) GaAs/GaAs TJ design with 10nm doped layers and barrier layers, c) AlGaAs/GaInP TJ. d) IV curve of 30nm TJ (triangles), 30nm TJ exposed to hydrogen plasma (circles) and 10nm TJ (diamond). e) Same IV curves than d) with additional AlGaAs/GaInP characteristic (stars).

Additionally, two other TJ diode designs were tested: one with thinner GaAs layers (10nm) in sandwich between AlGaAs and GaInP layers for minority carriers repulsion (see Fig.5.26-d)), and one with AlGaAs/GaInP being directly the tunnel junction materials (see Fig.5.26-c)). The IV characteristics of the 10 nm TJ is shown in Fig.5.26-d) by diamond symbols; an improved tunneling current (18 A/cm^2) compared to the 30nm GaAs TJ before hydrogenation is observed. Whether this improvement can be linked to the reduced pn junction thickness and/or to the presence of barrier layers is not clear yet. Considering the AlGaAs/GaInP, this TJ is interesting because of a higher transparency (higher gaps); in addition peak tunneling currents around $10^3 A/cm^2$ have been reported in literature[98]. Here we obtain an improvement of the tunneling current up to 56 A/cm^2, and the TJ resistance is similar to the 30 nm thick TJ exposed to H_2. The parameters of the 4 TJ plotted in Fig.5.26-e) are listed in

[96] T.P. Brody., Journal of Applied Physics, **33**: 100–111, 1962.
[97] K. Majumdar et al., IEEE Transactions on Electron Devices, **61**: 2049–2055, 2014.
[98] E. Barrigón et al., Progress in Photovoltaics: Research and Applications, **22**: 399–404, 2014.

Tab.5.1.

	J_{peak} (A/cm^2)	$V_{J_{peak}}$ (mV)	$R_{J_{peak}}$ (mΩ.cm^2)	J(5mV) (A.cm^2)	R(5mV) (mΩ.cm^2)
TJ GaAs 30nm - Asdep.	7.2	70	9.7	1.0	5.1
TJ GaAs 30nm - H_2	20.8	70	3.4	3.0	1.7
TJ GaAs 10nm - Asdep.	18	70	3.9	1.9	2.6
TJ AlGaAs/GaInP - Asdep.	56	166	3.0	2.8	1.8

Tab. 5.1 – Tunnel junction parameters as measured experimentally.

This study has shown that TJ with excellent properties were made, exceeding the requirements for 1 sun or low concentration operation conditions. More importantly, the H_2 plasma exposure (simulating the PECVD epitaxial Si process) does not deteriorate the TJ properties but it rather improves the tunneling properties.

5.5 Heteroepitaxial growth of Si on GaAs

The core idea in IMPETUS research project is to take advantage of the unique capabilities of low temperature PECVD hetero-epitaxial growth. Thus in this section we present a detailed material analysis of LTE silicon on (001)-oriented GaAs wafer: substrate surface preparation, epitaxial growth conditions optimization and crystal quality assessment.

5.5.1 GaAs surface cleaning

GaAs surface cleaning in PECVD reactors is not as simple as using epi-ready wafers in MOCVD reactors (which requires only a small annealing at 600-700°C under group V precursors atmosphere). If GaAs wet chemical cleaning is possible[99], the resulting surface passivation is probably less resistant compared to the H-terminated silicon surface. Indeed, while the short time air exposure between silicon wet oxide removal and reactor pumping does not prevent from good epitaxial growth, in the case of GaAs, we could not obtain a stable passivated surface because of the air exposure before loading into the reactor. Thus, we decided to develop dry plasma GaAs in-situ cleaning, using a similar process as the one established for Si and Ge in the two previous chapters. GaAs surface cleaning has been achieved in both reactors used in this thesis: the 30 years old ARCAM[100] and the new industrial like cluster tool. The best plasma conditions are summarized in Tab.5.2.

PECVD Reactor	Temp. (°C)	Pressure (mTorr)	SiF_4 (sccm)	Power (mW/cm^2)	Time (min)	Electrode gap (mm)
Cluster	175	250	20	140	3	22
Arcam	175	80	30	65 –> 30	3 + 2	17

Tab. 5.2 – Optimized SiF_4 plasma conditions for GaAs surface oxide cleaning in two different PECVD reactors.

[99] V.L. Berkovits et al., Applied Physics Letters, **80**: 3739, 2002.
[100] P. Roca i Cabarrocas., Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, **9**: 2331, 1991.

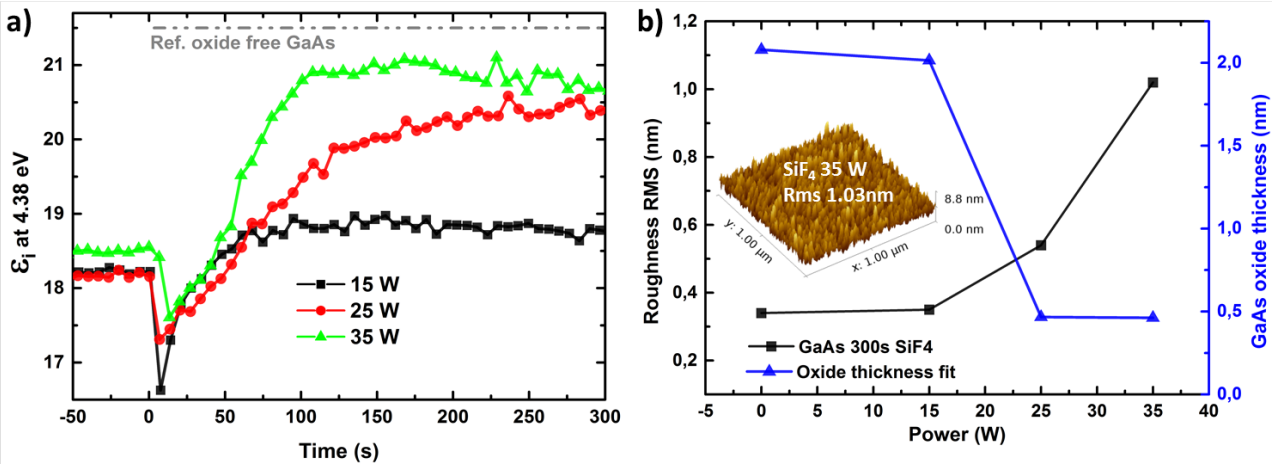


Fig. 5.27 – a) In-situ real time spectroscopic ellipsometry monitoring of GaAs (100) native oxide cleaning by SiF_4 plasma. The plasma starts at t=0s, and ε_i at 4.38 eV is monitored for three values of the RF power: 15W(squares), 25W(circles) and 35W(triangles). b) RMS roughness (squares), measured ex-situ by AFM after 200s plasma treatment, as a function of plasma power. The 35W treatment results in a ∼1nm roughness as shown in the inset. GaAs surface oxide (triangles) thickness deduced from fitting post-deposition ellipsometry measurements.

The evolution of GaAs native surface exposed to a SiF_4 plasma is monitored in real time by in-situ ellipsometry. The time evolution of $\boldsymbol{\varepsilon_i}$ at $\sim$ 4.4 eV[3]for three values of plasma RF-power is shown in fig.5.27-a). As a reference, the reference $\boldsymbol{\varepsilon_i}$ value for GaAs oxide free surface, at the substrate temperature of 180°C is shown by a grey dash line at the top of the graph. The $\mathbf{SiF_4}$ plasma conditions are 20 sccm and a pressure of 250 mTorr, and three power conditions are tested 15W(squares), 25W(circles) and 35W (triangles). The flat curves at t<0s correspond to the GaAs surface with its native oxide, and the plasma ignition is characterized by a drop in $\boldsymbol{\varepsilon_i}$ at t=0s. The presence of such kink is not clearly understood yet. Then, $\boldsymbol{\varepsilon_i}$ is increasing with time, above the initial value, indicating that the surface oxide is being removed. The best recipe turns out to be at 35W, since this curve gets closer to the theoretical value. For the 35W curve, a maximum $\boldsymbol{\varepsilon_i}$ is reached after $\sim$ 3 min of surface cleaning; further plasma exposure results in surface degradation, most likely through roughness creation. The RMS roughness, measured ex-situ by AFM after a 200s $\mathbf{SiF_4}$ plasma cleaning step, is shown in Fig.5.27-b) (square symbols). From an initial value below 0.4nm for the out-of-the-box surface, the 35W treatment creates $\sim$ 1nm roughness (see inset), which remains reasonable for subsequent epitaxial growth. The GaAs oxide thickness, as fitted from post-deposition ellipsometry measurements, is reduced below 0.5nm, as compared to the native oxide thickness being slightly above 2nm. The non-zero value for the oxide thickness after cleaning is probably linked to oxide re-growth since the sample is measured in air. Overall, this is the proof that GaAs oxide can be efficiently removed by in-situ $\mathbf{SiF_4}$ plasma at 175°C. The mechanism involved may be a mix of chemical reaction and sputtering effect.

[3]Absorption depth is in the range of 8nm for this photon energy.

The full spectrum ε_i as measured both in-situ and ex-situ are shown in Fig.5.28. The differences between a standard GaAs (triangles) and an epi-ready surface (circles) is clearly visible on graph a): in the high energy range, the higher amplitude of the epi-ready wafer is linked to lower surface roughness and lower oxide thickness. Thus the cleaning recipe and the SiF_4 cleaning duration should be adapted if a different wafer surface quality is used. The effective oxide removal upon SiF_4 plasma exposure is proven by the good match of the ε_i reference oxide-free curve (in red) and the GaAs wafer measured after cleaning (open triangles). The absorption depth is provided on an indicative basis, on the right axis (blue curve). Fig.5.28-b) shows basically the same information but measured ex-situ: i) the standard GaAs wafer with its native oxide (triangles), ii) the same wafer after SiF_4 plasma etching (open triangles), and iii) the reference ε_i curve for an oxide free GaAs at room temperature (red line). The best GaAs surface plasma cleaning conditions found in two different reactors are listed in Tab.5.2. For the reactor Arcam, more asymmetrical compared to the PECVD cluster configuration, a two-step process with high and low power density has been used.

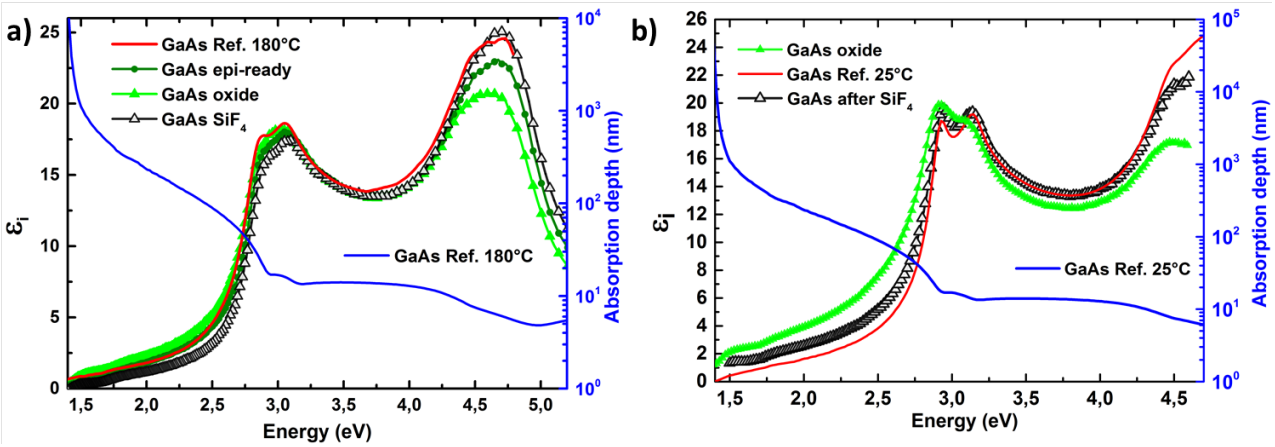


Fig. 5.28 – a) Comparison of GaAs surfaces measured by in-situ ellipsometry for: i) a standard GaAs wafer (triangles), ii) an epi-ready wafer (circles) and iii) a standard GaAs wafer after SiF_4 oxide cleaning (open triangles) and iv) the reference GaAs at 180°C (red line). Absorption depth in GaAs is represented by the blue curve. b) Comparison of GaAs surfaces from ex-situ ellipsometry measurements for: i) a standard GaAs wafer (triangles), ii) a standard GaAs wafer after SiF_4 oxide cleaning (open triangles) and iv) the reference GaAs at room temperature(red line).

The paramount importance of surface oxide cleaning is demonstrated in Fig.5.29. In this graph we show the result of three silicon depositions done with the exact same epitaxial conditions as optimized for epi-Si, but the surface treatment prior epitaxial growth differs between the three samples. The depositions and wafer surface cleaning are done in the same reactor, ARCAM, and the oxide cleaning follows a two steps process (high and low plasma power, see Tab.5.2). In Fig.5.29-a), the ellipsometry spectrum measured ex-situ after deposition are displayed: one sample had a 1min(11W)/4min(5W) SiF_4 plasma (squares), the second a 2.5min(11W)/2.5min(5W) (circles) and the third a 3min(11W)/2min(5W) (triangles), the optimized recipe for this reactor. The difference between the silicon materials deposited on GaAs is striking: for the 1min/4min sample, the material is amorphous (large shoulder with a ε_i max around 20). The 2.5min/2.5min sample shows characteristic peaks of crystalline silicon, thus giving a first proof of epitaxial Si grown on GaAs. The third sample, 3min/2min, shows even higher ε_i peaks: 34.5 and 40.9 at 3.4 and 4.2 eV respectively. Thus the epi-Si quality is strongly correlated to the GaAs effective native oxide removal.

We can draw the same conclusion from the Raman spectra shown in Fig.5.29-b). The amorphous sample has a characteristic shoulder around 480cm^{-1} with a tiny peak centered around 520cm^{-1}: this layer has probably a small fraction of crystalline material. The second sample, 2.5min/2.5min, shows a well-defined c-Si peak centered at 523 cm^{-1} and with a FWHM of 10.2cm^{-1}: this sample seems to be under compressive stress, and the FWHM indicates the presence of crystal defects. The substrate GaAs LO mode is visible at 292 cm^{-1}. For the third epitaxial sample (triangle), the c-Si peak FWHM is lower, 9cm^{-1} and the shift is even larger: 524cm^{-1}. Thus the crystal quality of this sample is higher, but since there are less defects enabling relaxation, the stress is higher in this material. Note that both GaAs TO and LO modes are visible at 268 and 292 cm^{-1}; indeed the high doping of the GaAs substrate results in a coupling of the LO mode with surface plasmons, which explains why this TO mode becomes visible.

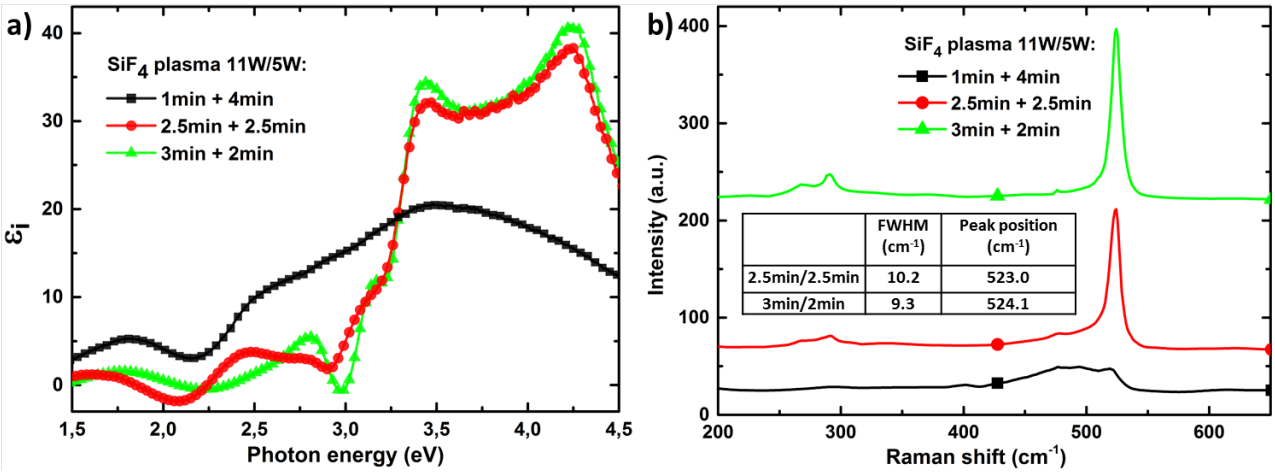


Fig. 5.29 – a) ε_i measured ex-situ after the deposition of silicon on GaAs using the same plasma epitaxial conditions but different SiF_4 oxide cleaning recipe: 1min(11W)/4min(5W) (squares), 2.5min(11W)/2.5min(5W) (circles) and 3min(11W)/2min(5W) (triangles). b) Raman spectra measured on the same samples.

5.5.2 Effect of silane dilution

Once the optimum surface cleaning conditions were established, we decided to optimize the silane dilution in H_2, since, as presented in chapter 3, the precursor dilution is linked to the microcrystalline, epitaxial or amorphous structure of the deposited layer. Thus, we have deposited a series Si on GaAs samples, for which the SiF_4 plasma cleaning step was identical, but during the following SiH_4/H_2 plasma epitaxial conditions, the silane flow rate was changed while keeping all the other parameters constant. The samples were analyzed by ellipsometry and Raman spectroscopy after deposition, as shown in Fig.5.30. The ε_i is displayed in Fig.5.30-a) for 4 different silane flow rates: 14 (stars), 34 (triangles), 36 (circles) and 40 sccm (squares). The same material transition is found compared to the epitaxial Si on c-Si case: i) at high silane flow rate (40sccm), the material is amorphous, ii) at moderate flow rate (34-36 sccm), the material is epitaxial (as judged by ε_i characteristic peaks at 3.4 and 4.2 eV) and iii) at low silane flow rate, thus high dilution in H_2, the sample is microcrystalline (lower ε_i 4.2 eV peak compared to 34-36 sccm curve). When comparing the ε_i curve, one should also keep in mind that the material is changing with thickness and deposition rates are lower for lower silane flux. Thus the 14 sccm sample corresponds only here to 18 nm of Si on GaAs, while the 36 sccm sample consists of 126 nm of Si on GaAs. It is in fact expected that the ε_i peaks amplitude would decrease for the 14 sccm conditions if longer deposition were performed. Indeed the highest ε_i peaks amplitude for the thickest depositions are good criteria for finding the optimum epitaxial conditions.

This trend in Si on GaAs material changes with silane dilution during epitaxy is further confirmed

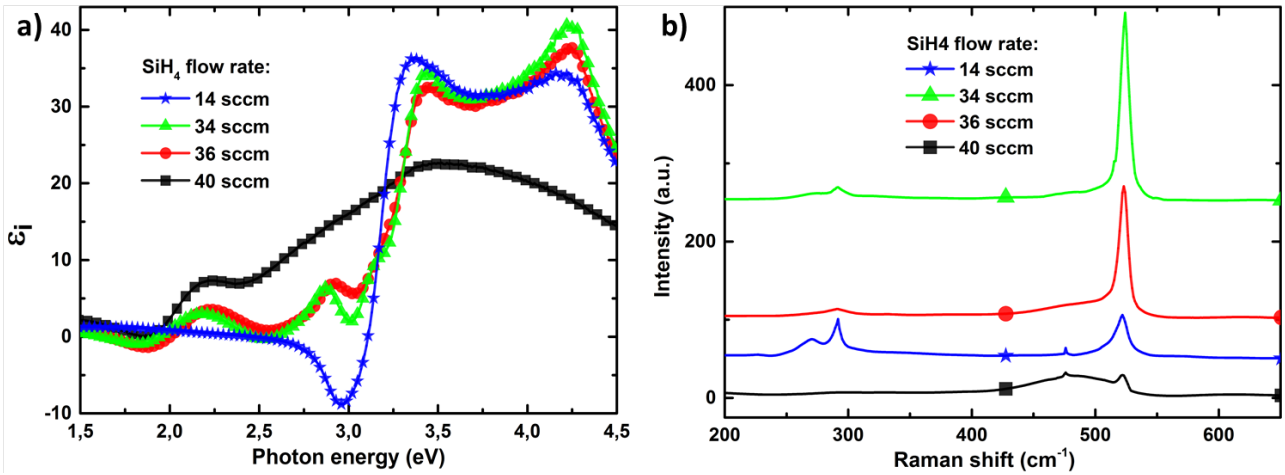


Fig. 5.30 – a) Ellipsometry measurements on silicon deposited on cleaned GaAs wafer from a SiH_4/H_2 plasma, with various silane flow rates: 14 (stars), 34 (triangles), 36 (circles) and 40 sccm (squares). b) Corresponding Raman spectra.

by Raman spectroscopy analysis. The spectra measured on the same series of samples are shown in fig.5.30-b). The c-Si peak around 520 cm^{-1} is very tiny for the 40 sccm sample, betraying the large a-Si:H fraction in this material; for the 14 sccm sample, no broad a-Si:H shoulder is detected, but the peak seems to be larger. The TO and LO modes are well detected at 268 and 292 cm^{-1}, since this sample is very thin. The 34 and 36 sccm samples have a well-defined sharp c-Si peak, with 34 sccm exhibiting the smallest FWHM.

These results are summarized in the Fig.5.31 where the ε_i peak amplitude at 3.4 eV (triangles) and 4.2 eV (circles) are plotted as a function of silane flow rate (or silane dilution with top x-axis). The right y-axis shows the Raman c-Si peak FWHM for the different silane flow rates (squares). The maximum of ε_i, around 34.5 at 3.4 eV and 41 at 4.2 eV, happens for the same silane flow rate, namely ∼34 sccm, than the minimum Raman FWHM (8.4 cm^{-1}). Moreover, looking at deposition rates (see diamond symbols, second y-axis on the right) the highest value, 1.3 Å/s, corresponds also to 34 sccm of SiH_4. Thus the two techniques confirm the existence of an optimum silane dilution for epitaxial growth. This optimum corresponds to a $SiH_4/(SiH_4+H_2)$ of ∼0.14%, in this reactor. Interestingly enough, this optimum is exactly the same than in the silicon homoepitaxial case.

5.5.3 Assessment of the crystal quality

The successful epitaxial growth at 175°C of silicon on GaAs has been confirmed by both Raman and ellipsometry. To gain more insight into such heteroepitaxial layers crystal quality, we have performed cross section TEM analysis of the epi-Si/GaAs samples. These analysis were performed thanks to the help of TEM experts R. Ruggeri, J.-L. Maurice and G. Patriarche, on both LPICM TEM and LPN STEM set-ups.

The TEM analysis of a 650nm epi-Si sample observed in cross section along the [110] axis is detailed in Fig.5.32. The whole layer is visible on the low magnification picture Fig.5.32-b); the characteristic dark spots already observed in the case of low temperature PECVD epi-Si on c-Si are also present here. Such pattern is linked to the presence of defects, such as H-platelets, point defects and strain in the epi-Si layer. A high resolution zoom on this epi-Si interface is presented in a): i) the interface appears sharp and well defined ii) Excellent atomic order can be distinguished in epi-Si layer. Despite the ∼4% lattice mismatched between the two materials, we couldn't detect threading dislocations; this first observation validates the benefice of a low temperature growth approach and its reduced thermal expansion related problems. The Fourier transform image of this high resolution picture is shown in Fig.5.32-c): a two points spot can be distinguished, which in fact corresponds to the contribution

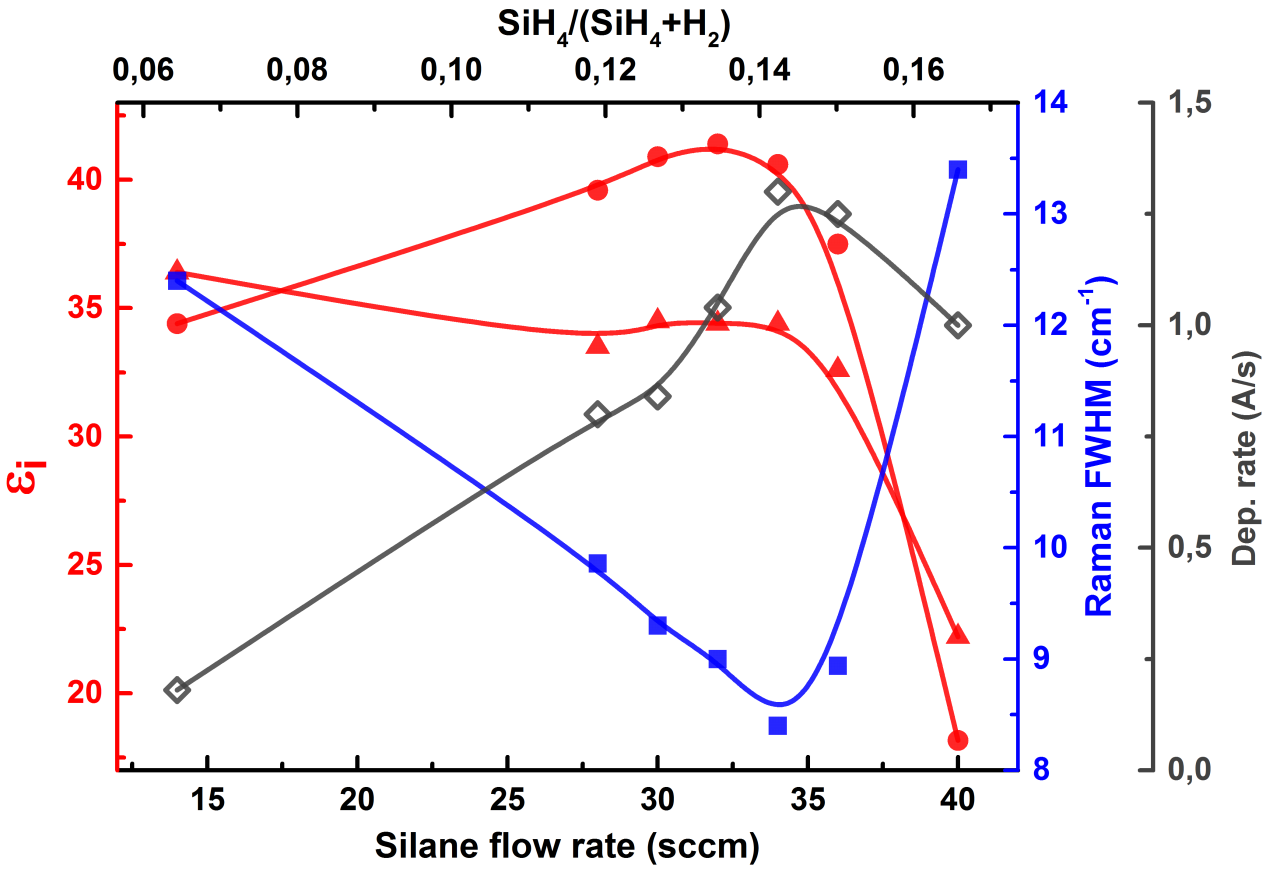


Fig. 5.31 – Left: ε_i amplitude values at 3.4 eV (triangles) and 4.2 eV (circles) as a function of silane flow rate. Right: Raman c-Si peak FWHM as a function of silane flow rate (squares). The top x-axis shows the silane dilution. The second y-axis on the right scales the deposition rate (diamonds).

of Si and GaAs having different lattice parameters. This is confirmed on the electronic diffraction picture taken at the interface, as presented in Fig.5.32-d); zoom on (004) and (440) planes in e) and f) clearly show the distinct diffraction points. This double pattern confirms that the epi-Si growth is not pseudomorphic: the silicon is growing with a lattice parameter at least partially relaxed, which differs from the one of GaAs. From those first images, the epi-Si layer crystal quality seems to be comparable to the one obtained in the case of PECVD epi-si grown on lattice matched c-Si.

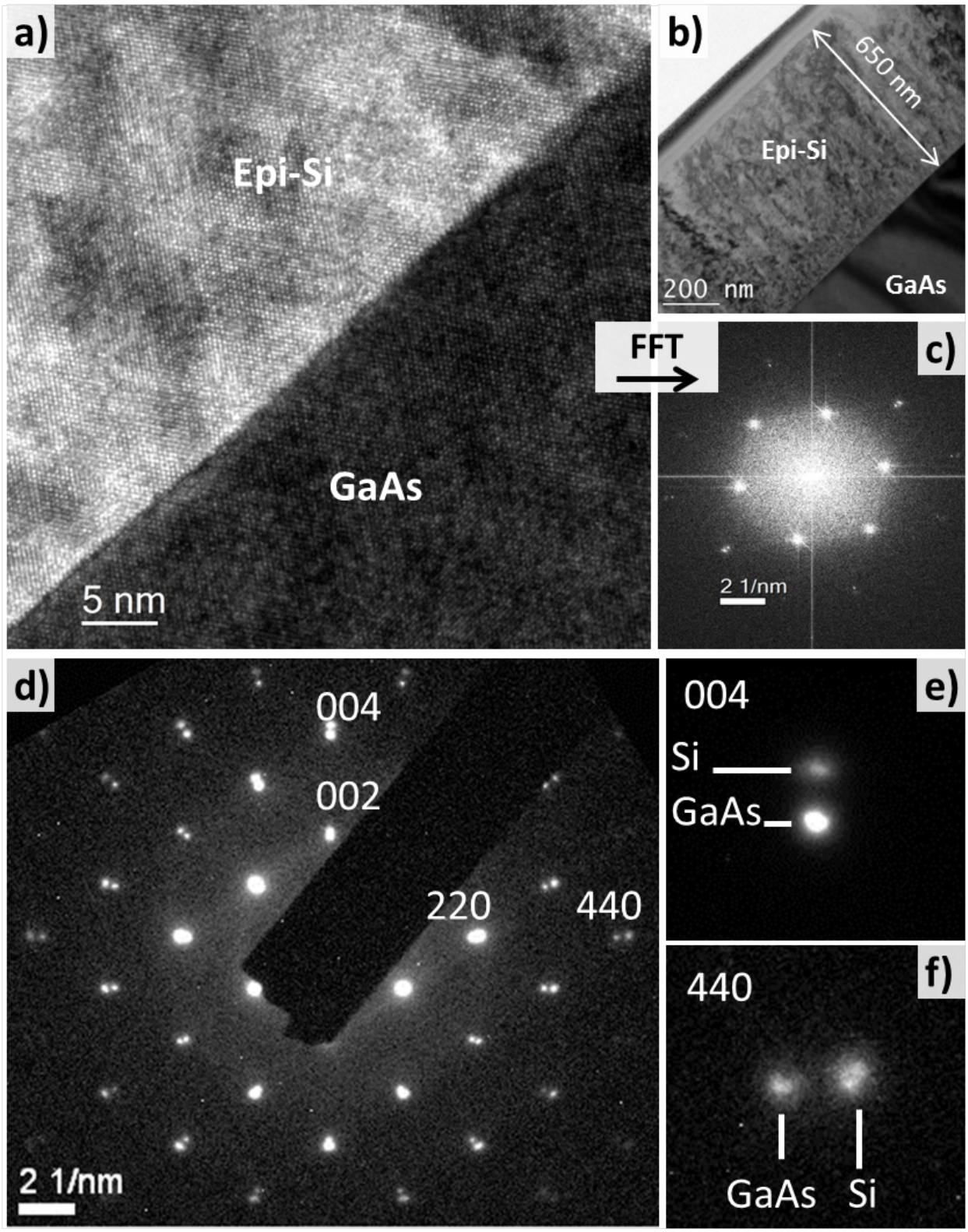


Fig. 5.32 – a) HRTEM image along [110] axis of epi-Si/GaAs interface. b) Low magnification cross section picture of the whole 650nm thick epi-Si layer on GaAs. c) Fourier transform image of picture a). d) Diffraction pattern of epi-Si/GaAs interface: the double points visible in each family planes (e.g. see e) and f)) are the signature of both Si and GaAs lattices.

The epi-Si/GaAs interface has been analyzed by SIMS and HAADF to get detailed information on its chemical composition. The SIMS Si, F and As profiles are shown in Fig.5.33. As visible on graph a) and b), when no annealing is performed (squares symbols) the transition between Si and GaAs is very sharp, no diffusion is detected. The same sample has been analyzed after 15min (circles), 60min (triangles) and 140min (stars) annealing steps in air at 390°C. With these latter two annealing conditions, a diffusion profile starts to be visible for As inside silicon and for F inside GaAs. The fluorine detected at the interface are residual atoms left from the SiF_4 cleaning step; it should be possible to decrease F content at the interface by appropriate H/Ar plasma treatment after the cleaning step. The diffusion of As in silicon may result in n-type doping since As is a donor impurity for silicon. In any case, if annealing steps are required during solar cell processing (e.g. to get ohmic metal contacts) this is usually a 2-5 min step. Consequently, as expected for this low temperature approach, the diffusion across the interface should not be a problem if annealing at T∼400°C does not last more than a few minutes.

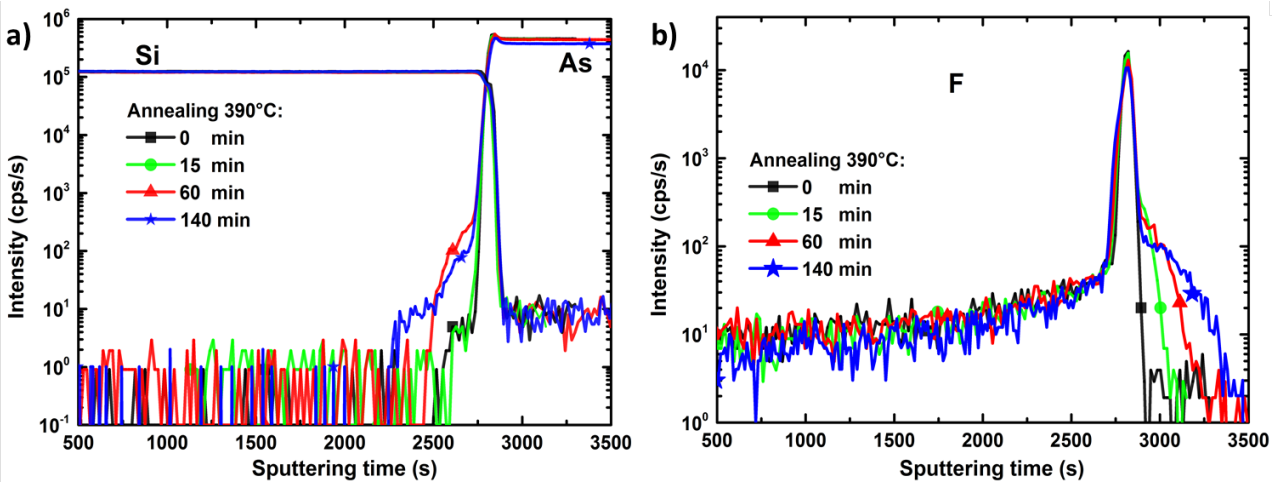


Fig. 5.33 – SIMS profiles of a) Si and As and b) F for epi-Si/GaAs interface. The profiles are measured for the same sample annealed at 390°C in air for 3 durations: 0min (squares), 15min(circles), 60min (triangles) and 140min (stars).

Additionally, STEM-HAADF analysis has been performed on the cross section of epi-Si/GaAs samples prepared by FIB. HAADF images are formed by collecting high-angle scattered electrons with an annular dark-field detector in scanning TEM. Using this imaging method, there is a strong dependence of STEM image intensity on average atomic numbers of the scatterer elements encountered by the incident probe. Thus, a region with lighter elements or simply less atoms will appear darker on a HAADF image; if the sample thickness is uniform, the HAADF contrast is a function of the material density/chemical composition. A 152 nm epi-Si on GaAs low magnification picture is shown both in bright field a) and HAADF b) in Fig.5.34. In HAADF image, the Si appears darker as a consequence of its smaller atomic number. At this scale, the interface looks again sharp and well defined. By zooming on the interface, the crystalline network becomes clearly visible as well as some crystalline defects such as stacking fault. The high resolution HAADF pictures of the interface, Fig.5.34-c,d), and the intensity profile in the inset, confirms the chemically sharp transition as expected from SIMS analysis.

To get more insight into the crystalline defects found in such low temperature epitaxial silicon on GaAs, we have done TEM image treatment. Starting from a HR-STEM image of the interface (see Fig.5.35-a), we could highlight defects lying in the 111 planes. First we have used a fast Fourier transform algorithm (FFT) to process the interface real-space image. The result, as shown in Fig.5.35, is conceptually equivalent to an electronic diffraction pattern, and thus reveals well defined spots corresponding to the contribution of crystallographic planes. In the case of epitaxial growth on (001) oriented substrates, many defects are lying in the 111 planes. Thus by applying a mask on the specific

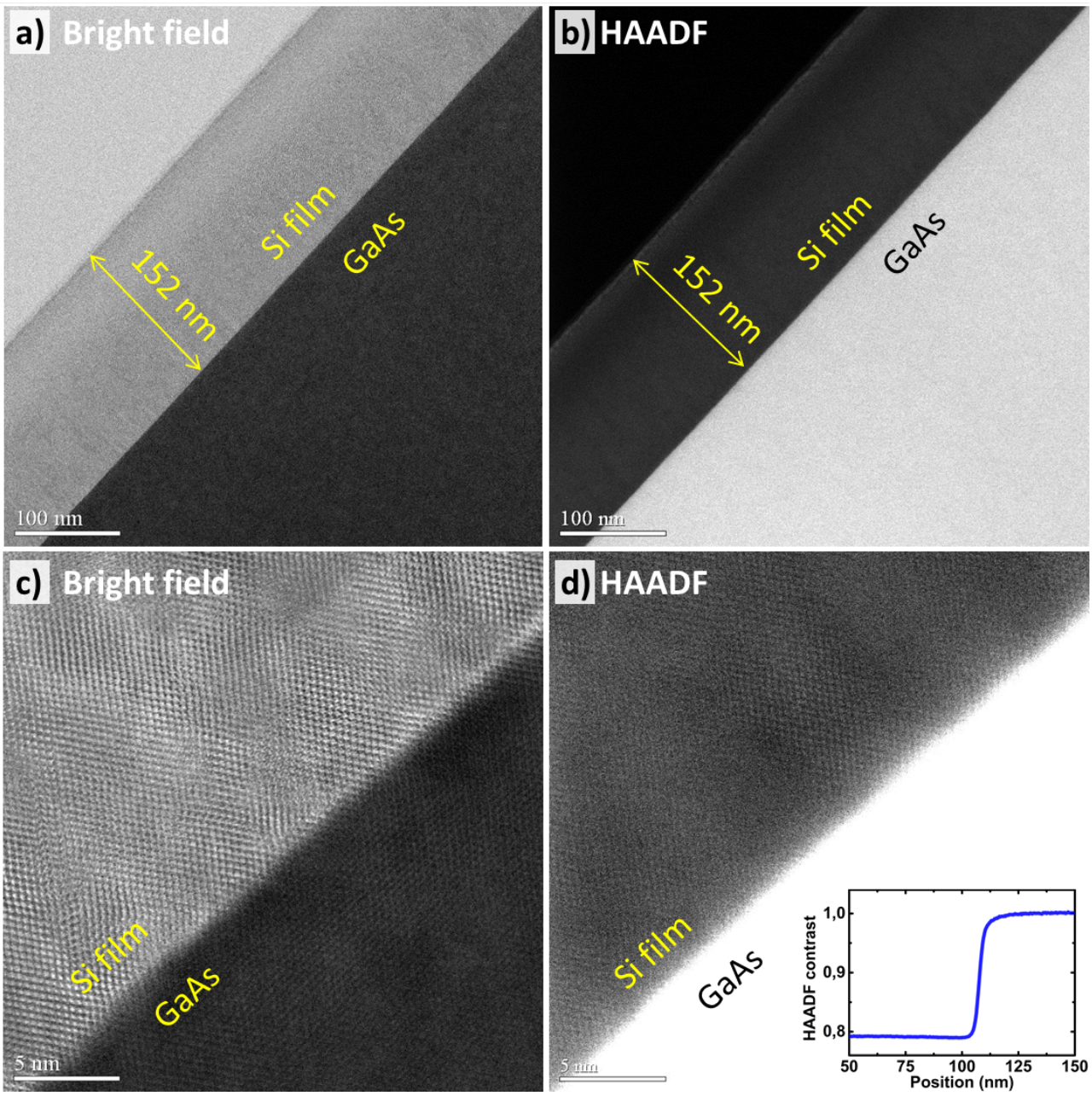


Fig. 5.34 – Low magnification a) STEM bright field (BF) and b) HAADF image of cross section epi-Si(150nm)/GaAs interface. High resolution BF c) and HAADF d) zoom on the interface, with inset showing intensity profile.

(111) spots in the FFT image, and then performing inverse FFT algorithm, we could reconstruct the high resolution real-space image of the interface, but keeping only the contribution of the selected (111) planes. Additionally, we have used color instead of grey scale for this reconstructed image, to better highlight planes. Like so, images Fig.5.35-a) and b) correspond to the exact same interface area. The inset 1, 2 and 3 correspond to zooms on three different zones were defects were detected: lattice distortions and edge dislocations can be recognized. In fact, as shown in the chapter 3, similar defects are detected with this technique in the case of epi-Si on c-Si. Thus from this analysis, we could be tempted to say that similar crystal quality is achieved for both PECVD homo and heteroepitaxial case. Yet, one should remember that Raman FWHM is a good statistical quantity to probe crystal disorder, and around 8 cm^{-1} has been found for epi-Si on GaAs whereas epi-Si on c-Si FWHM are in the range of 5 to 6 cm^{-1}. In any case, this epi-Si on GaAs material is also full of hydrogen, and a large fraction of the crystalline defects should not have electrical activity.

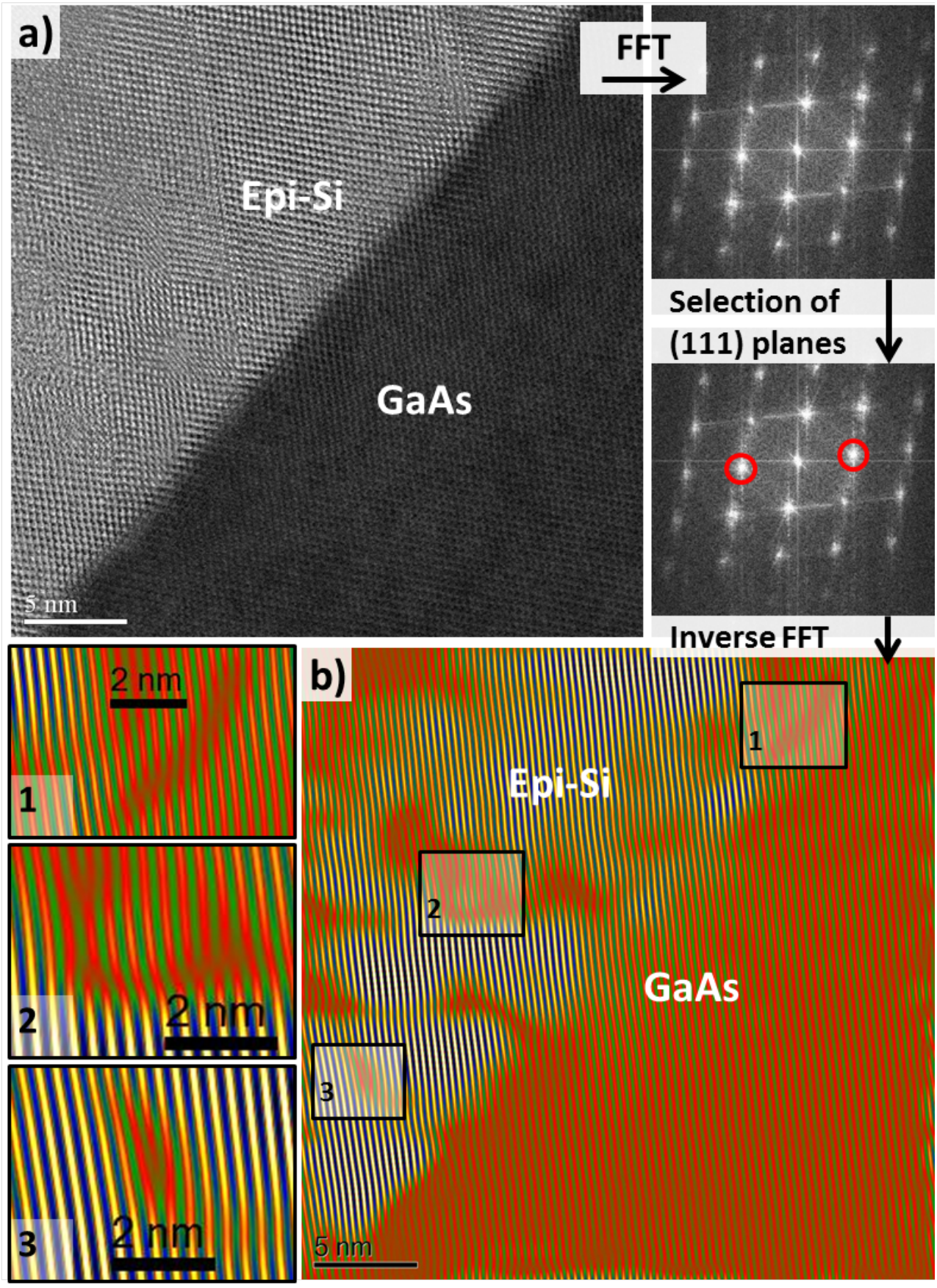


Fig. 5.35 – a) High resolution STEM cross section picture along [110] axis of epi-Si/GaAs interface. b) Corresponding Fourier transformation. c) Selection of (111) planes by applying specific mask. d) Reconstructed TEM image, in temperature color scale, by inverse Fourier transform, keeping only the selected (111) planes contribution. 1, 2 and 3 are zooming on defective areas.

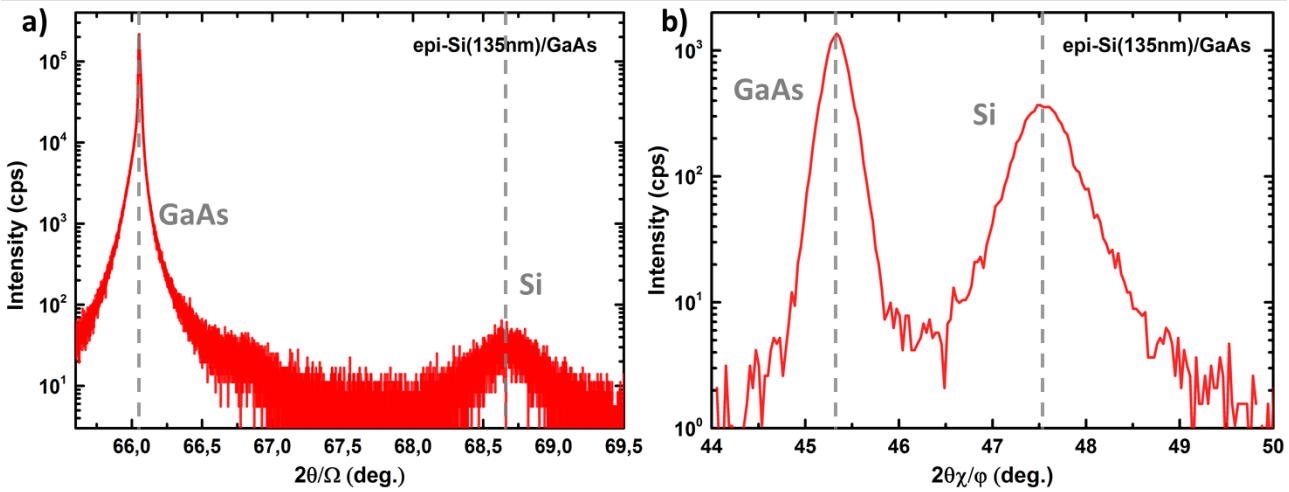


Fig. 5.36 – a) High resolution XRD measurement of the {004} planes parallel to the surface of epi-Si film grown on (100) GaAs. b) Grazing incidence XRD measurement of the {220} planes perpendicular to the surface, for the same sample.

In addition to the TEM analysis, we coupled high angle $2\theta/\omega$ X-ray diffraction and grazing incidence X-ray diffraction (GIXRD) measurements on a epi-Si(135nm)/GaAs, grown by low temperature PECVD epitaxy, to get information about the crystallinity of the films and get their lattice parameters. These analysis were performed by XRD experts L. Largeau and O. Mauguin with the Rigaku Smartlab diffractometer based in the LPN laboratory. This set-up allowed us to study the diffraction from the {004} crystallographic planes parallel to the surface (lattice parameter:$a_\perp$), with $2\theta/\omega$ scan, and the diffraction from the {220} crystallographic planes perpendicular to the surface (lattice parameter:$a_\parallel$), with $2\theta\,\chi/\phi$ scan. The Ω and 2θ grazing angles were both 0.28°. Additionally, 4 scans were performed along the {220} planes to check the epitaxy relaxation; the absence of twins in epi-Si was also confirmed by large angular scans revealing no peak from {114} planes perpendicular to the sample surface.

Fig.5.36-a) shows the $2\theta/\omega$ scan with diffraction from the {004} planes, and Fig.5.36-b) shows the GIXRD scan with diffraction from the {220} planes. In both cases, the peaks of GaAs substrate and Si epi-layers appears at distinct angular positions; thus confirming the difference in lattice parameters (metamorphic growth). For the $2\theta/\omega$ scan, the Si peak intensity is much lower than GaAs, this is attributed to the lower crystal quality of Si and its limited thickness; in GIXRD, the peak of Si is well-defined and has an intensity closer to the one of GaAs. Knowing the distances of {004} and {220} GaAs substrate planes, we could deduce from the peak position the in-plane $a_\parallel$ and out-of-plane $a_\perp$ lattice parameters of epi-Si; we found: $a_\parallel$= 5.4049Å and $a_\perp$=5.4537Å . Using the equations listed in chapter 3 (eq.3.4, eq.3.5 and eq.3.6) a bulk equivalent lattice parameter of 5.4325Å for epi-Si on GaAs is found. Thus, the mismatch between Si and GaAs is so high that Si relaxes almost immediately (few nm after the interface), and the epi-layer is growing with its own lattice parameter. Therefore, in the case of epi-Si on GaAs, the in plane compressive stress detected both in Raman and XRD is more linked to epi-Si impurity content (such as hydrogen platelets) than to the lattice mismatch with GaAs.

Finally, the evolution of epi-Si on GaAs with thickness has been studied. The ε_i curves measured by ex-situ ellipsometry are shown in Fig.5.37-a) for three different epitaxial thicknesses: 215 nm (triangles), 640 nm (circles) and 1450 nm (squares). The thickness change between the three samples is visible in the 1.5-3 eV range, with Si/GaAs interface related oscillations. The characteristic peaks of c-Si in the three samples are visible, however the thickest sample shows a net decrease of the peak amplitude. This could be related to an increase of surface roughness or a deterioration of the epi-Si quality. To further investigate this thickness changes, we have performed Raman measurements on the same three samples, as shown in Fig.5.37-b). The two thickest samples have a lower peak FWHM,

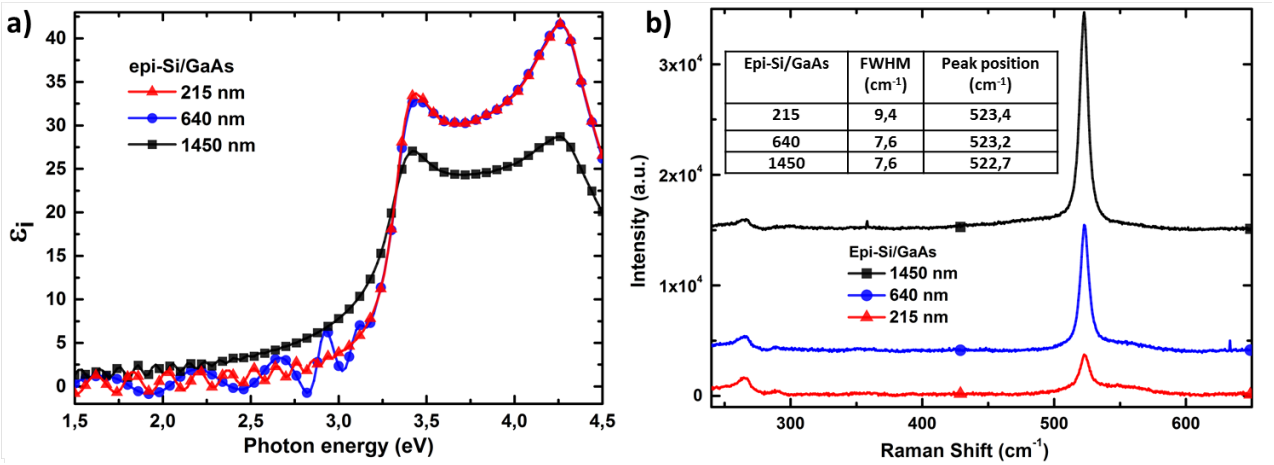


Fig. 5.37 – a) Ellipsometry spectra for epi-Si on GaAs samples with three different thicknesses: 215 nm (triangles), 640 nm (circles) and 1450 nm (squares). b) Corresponding Raman spectra.

namely 7.6 cm^{-1}, compared to the 9.4 cm^{-1} found for the 215 nm sample; the peak position is also decreasing from 523.4 to 522.7 cm^{-1} with increasing thickness. Thus the epi-Si material is relaxing with increasing thickness; while the crystal quality, as measured by this technique, seems to improve. To resolve this apparent contradiction between ellipsometry and Raman analysis, more samples should be analyzed. The question of the existence of a potential critical thickness, or whether epitaxial quality may improves with thickness, in this epi-Si on GaAs scenario remains open.

Using the design presented in the chapter 4 (the so-called wafer equivalent approach) we have built test diodes made of epi-Si on GaAs. The stack consists of GaAs(n+)/epi-Si(i)/(p)a-Si:H, as shown in Fig.5.38. Two diodes were made one with 123nm epitaxial absorber (circles) and a second one with 426 nm epi-Si absorber (triangles). The corresponding IV curves under 1 sun and solar cell parameters are shown in Fig.5.38. These solar cells have in fact a very poor diode behavior, but, obviously, such absorber thicknesses are way too small to have significant absorption. The trend of V_{oc} and J_{sc} increase with absorber thickness reveals that much better diode characteristics can be expected for epi-Si absorber in the range of few microns. Overall, these devices are proof of concept that epi-Si grown on GaAs by PECVD have suitable electronic quality for solar cells.

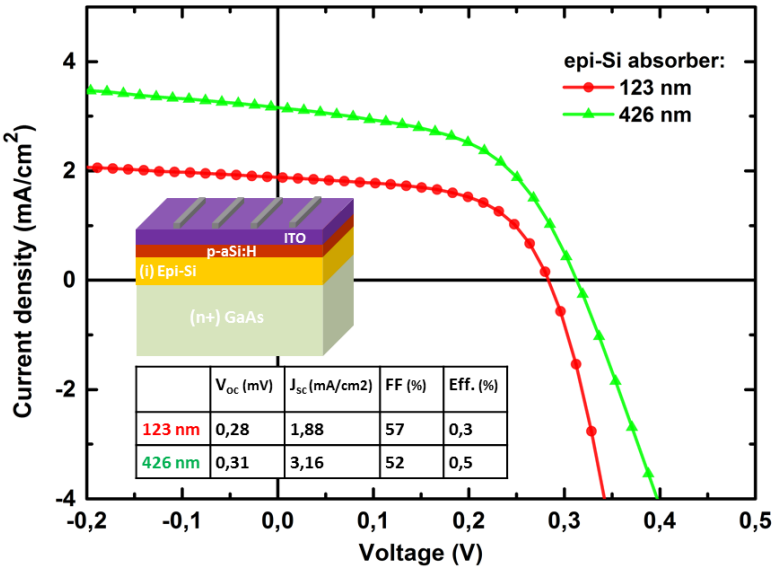


Fig. 5.38 – Test diodes consisting of GaAs(n+)/epi-Si(i)/(p)a-Si:H with two different absorber thicknesses: 123 nm (circles) and 426 nm (triangles).

5.6 Summary and perspectives

Takeaway Message - Integration of Si on III-V: towards tandem devices

- The integration of III-V compounds, dominant materials in LED and optoelectronics, with the mainstream Si technology is a long sought after goal for the semiconductor industry. However, the associated material challenges for growing planar III-V on silicon substrate (polar III-V ***vs*** covalent Si structure, lattice and thermal mismatch) make the task difficult.
- Theoretical detailed balanced efficiency calculations confirm that Si band gap is well adapted for multijunctions: i) 2 junctions can reach ∼42% for 1.74/1.12 eV or 1.64/0.96 eV at 1 sun or ii) 3 junctions (1.87/1.44/1.12) eV can reach ∼ 47% or ∼45% for 1.74/1.12/0.53 eV under 1 sun iii) 4 junctions can reach 57% under 100 suns with 2.0/1.49/1.12/0.67 band gaps.
- For solar cells, direct heteroepitaxy of III-V on GaAs is limited by dislocations and maximum efficiencies are in the 20% range. Using buffer layers, the defects are reduced, but such III-V/Si tandem device remains in the 15% range. Wafer bonding III-V/Si cells are leading the race with efficiency around 25% reported.
- Our innovative inverted metamorphic approach, as studied in IMPETUS project, targets a low cost ∼30% efficient device: i) a top AlGaAs cell is grown lattice matched on sacrificial III-V layers ii) a bottom Si(Ge) cell is grown by LTE on the top III-V cell iii) The whole stack is lifted-off and flipped over to process the top cell front side. This approach minimizes the thermal mismatch, suppresses the polarity problems, and enables wafer re-use.
- GaAs solar cells on wafer reaching more than 20% efficiency and a $\boldsymbol{V_{oc}}$ of 1011 mV have been achieved using AlGaAs window layer, protected from the oxygen of $\mathbf{TiO_2/SiO_2}$ double ARC by a thin GaInP layer.
- GaAs/GaAs and AlGaAs/GaInP tunnel junctions with $\boldsymbol{J_{peak}}$ of respectively 7.2 and 56 $\mathrm{A/cm^2}$ have been realized. Unexpectedly, a ×3 improvement of the GaAs/GaAs TJ $\boldsymbol{J_{peak}}$, up to 20.8 $\mathrm{A/cm^2}$, was observed upon $\mathbf{H_2}$ plasma exposure. This effect is beneficial for integration of III-V top cell with a PECVD bottom cell deposited from $\mathbf{H_2/SiH_4}$ plasma.
- Proper native oxide removal is crucial for Si LTE on GaAs wafer. Using $\mathbf{SiF_4}$ plasma treatment at 175°C, the GaAs wafer native oxide can be efficiently removed while keeping a surface roughness low enough to be compatible with subsequent epitaxial growth (RMS ∼1nm).
- Similarly to epi-Si on c-Si, when changing the silane dilution in $\mathbf{H_2}$, low temperature PECVD heteroepitaxial growth happens at the transition between micro-crystalline and amorphous conditions. The best epi-Si on GaAs has a Raman FWHM of $7.6\mathrm{cm^{-1}}$.
- The monocrystal quality of epi-Si on GaAs is confirmed by TEM cross section analysis and XRD. Similar point defects and stacking faults than epi-Si on c-Si are observed. Diffusion related problems are suppressed in our low temperature approach, as confirmed by the chemically sharp interface found by SIMS and STEM-HAADF. XRD scans confirm that epi-Si epitaxial growth is metamorphic. The small detected compressive stress in epi-Si is probably linked to H-platelets.

References

[1] J.A. del Alamo. Nanometre-scale electronics with III-V compound semiconductors. *Nature*, **479**: 317–323, 2011. doi: 10.1038/nature10677 (see p. 174)

[2] A.W. Fang, H. Park, O. Cohen, R. Jones, M.J. Paniccia, and J.E. Bowers. Electrically pumped hybrid AlGaInAs-silicon evanescent laser. *Optics Express*, **14**: 9203–9210, 2006. doi: 10.1364/OE.14.009203 (see p. 174)

[3] G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, and J. Bowers. III-V/silicon photonics for on-chip and intra-chip optical interconnects. *Laser & Photonics Reviews*, **4**: 751–779, 2010. doi: 10.1002/lpor.200900033 (see p. 174)

[4] A. Le Liepvre, A. Accard, F. Poingt, C. Jany, M. Lamponi, D. Make, F. Lelarge, J.-M. Fedeli, S. Messaoudene, D. Bordel, and G.-H. Duan. Wavelength Selectable Hybrid III-V/Si Laser Fabricated by Wafer Bonding. *IEEE Photonics Technology Letters*, **25**: 1582–1585, 2013. doi: 10.1109/LPT.2013.2271322 (see p. 174)

[5] M. Lamponi, S. Keyvaninia, C. Jany, F. Poingt, F. Lelarge, G. de Valicourt, G. Roelkens, D. Van Thourhout, S. Messaoudene, J.-M. Fedeli, and G.-H. Duan. Low-Threshold Heterogeneously Integrated InP/SOI Lasers With a Double Adiabatic Taper Coupler. *IEEE Photonics Technology Letters*, **24**: 76–78, 2012. doi: 10.1109/LPT.2011.2172791 (see p. 174)

[6] S. Keyvaninia, G. Roelkens, D. Van Thourhout, C. Jany, M. Lamponi, A. Le Liepvre, F. Lelarge, D. Make, G.-H. Duan, D. Bordel, and J.-M. Fedeli. Demonstration of a heterogeneously integrated III-V/SOI single wavelength tunable laser. *Optics Express*, **21**: 3784–3792, 2013. doi: 10.1364/OE.21.003784 (see p. 174)

[7] G.-H. Duan, C. Jany, A. Le Liepvre, A. Accard, M. Lamponi, D. Make, P. Kaspar, G. Levaufre, N. Girard, F. Lelarge, J.-M. Fedeli, S. Messaoudene, D. Bordel, and S. Olivier. Hybrid III-V on silicon lasers for photonic integrated circuits on silicon. *SPIE Novel In-Plane Semiconductor Lasers XIII*, **9002**: 90020X–90020X–6, 2014. doi: 10.1117/12.2044258 (see p. 174)

[8] M.A. Green, K. Emery, Y. Hishikawa, W. Warta, and E.D. Dunlop. Solar cell efficiency tables (version 43). *Progress in Photovoltaics: Research and Applications*, **22**: 1–9, 2014. doi: 10.1002/pip.2452 (see pp. 175, 188–190)

[9] W. Shockley and H.J. Queisser. Detailed Balance Limit of Efficiency of p-n Junction Solar Cells. *Journal of Applied Physics*, **32**: 510, 1961. doi: 10.1063/1.1736034 (see p. 175)

[10] H. Cotal, C. Fetzer, J. Boisvert, G. Kinsey, R. King, P. Hebert, H. Yoon, and N. Karam. III-V multijunction solar cells for concentrating photovoltaics. *Energy & Environmental Science*, **2**: 174–192, 2009. doi: 10.1039/B809257E (see p. 175)

[11] F. Dimroth, M. Grave, P. Beutel, U. Fiedeler, C. Karcher, T.N.D. Tibbits, E. Oliva, G. Siefer, M. Schachtner, A. Wekkeli, A.W. Bett, R. Krause, M. Piccin, N. Blanc, C. Drazek, E. Guiot, B. Ghyselen, T. Salvetat, A. Tauzin, T. Signamarcheix, A. Dobrich, T. Hannappel, and K. Schwarzburg. Wafer bonded four-junction GaInP/GaAs//GaInAsP/GaInAs concentrator solar cells with 44.7% efficiency. *Progress in Photovoltaics: Research and Applications*, **22**: 277–282, 2014. doi: 10.1002/pip.2475 (see pp. 175, 184)

[12] T. Tiedje, E. Yablonovitch, G.D. Cody, and B.G. Brooks. Limiting efficiency of silicon solar cells. *IEEE Transactions on Electron Devices*, **31**: 711–716, 1984. doi: 10.1109/T-ED.1984.21594 (see p. 175)

[13] C.H. Henry. Limiting efficiencies of ideal single and multiple energy gap terrestrial solar cells. *Journal of Applied Physics*, **51**: 4494–4500, 1980. doi: 10.1063/1.328272 (see p. 175)

[14] A. De Vos. Detailed balance limit of the efficiency of tandem solar cells. *Journal of Physics D: Applied Physics*, **13**: 839, 1980. doi: 10.1088/0022-3727/13/5/018 (see p. 175)

[15] S.P. Bremner, M.Y. Levy, and C.B. Honsberg. Analysis of tandem solar cell efficiencies under AM1.5G spectrum using a rapid flux calculation method. *Progress in Photovoltaics: Research and Applications*, **16**: 225–233, 2008. doi: 10.1002/pip.799 (see pp. 176, 178)

[16] J.P. Connolly, D. Mencaraglia, C. Renard, and D. Bouchier. Designing III-V multi-junction solar cells on silicon. *Progress in Photovoltaics: Research and Applications*, 2014. doi: 10.1002/pip.2463 (see pp. 176–178, 186)

[17] W. Guter, J. Schoone, S.P. Philipps, M. Steiner, G. Siefer, A. Wekkeli, E. Welser, E. Oliva, A.W. Bett, and F. Dimroth. Current-matched triple-junction solar cell reaching 41.1% conversion efficiency under concentrated sunlight. *Applied Physics Letters*, **94**: 223504, 2009. doi: 10.1063/1.3148341 (see p. 177)

[18] K. Derendorf, S. Essig, E. Oliva, V. Klinger, T. Roesener, S.P. Philipps, J. Benick, M. Hermle, M. Schachtner, G. Siefer, W. Jager, and F. Dimroth. Fabrication of GaInP/GaAs//Si Solar Cells by Surface Activated Direct Wafer Bonding. *IEEE Journal of Photovoltaics*, **3**: 1423–1428, 2013. doi: 10.1109/JPHOTOV.2013.2273097 (see pp. 177, 183)

[19] I. Mathews, D. O'Mahony, B. Corbett, and A.P. Morrison. Theoretical performance of multi-junction solar cells combining III-V and Si materials. *Optics Express*, **20**: A754–A764, 2012. doi: 10.1364/OE.20.00A754 (see p. 178)

[20] J.M. Zahler. *Materials integration for high-performance photovoltaics by wafer bonding*. PhD thesis. California Institute of Technology, 2005. (see p. 178)

[21] Pchelyakov O.P. Bolkhovityanov Y.B. GaAs epitaxy on Si substrates: modern status of research and engineering. *Physics-Uspekhi*, **51**: 437, 2008. doi: 10.1070/PU2008v051n05ABEH006529 (see p. 179)

[22] H. Kawanami. Heteroepitaxial technologies of III-V on Si. *Solar Energy Materials and Solar Cells*, **66**: 479–486, 2001. doi: 10.1016/S0927-0248(00)00209-9 (see p. 179)

[23] H. Kroemer, T.-Y. Liu, and P.M. Petroff. GaAs on Si and related systems: Problems and prospects. *Journal of Crystal Growth*, **95**: 96–102, 1989. doi: 10.1016/0022-0248(89)90359-X (see p. 179)

[24] M. Kawabe and T. Ueda. Self-Annihilation of Antiphase Boundary in GaAs on Si(100) Grown by Molecular Beam Epitaxy. *Japanese Journal of Applied Physics*, **26**: L944, 1987. doi: 10.1143/JJAP.26.L944 (see p. 179)

[25] R. Fischer, N. Chand, W. Kopp, H. Morkoc, L. P. Erickson, and R. Youngman. GaAs bipolar transistors grown on (100) Si substrates by molecular beam epitaxy. *Applied Physics Letters*, **47**: 397–399, 1985. doi: 10.1063/1.96179 (see p. 180)

[26] A. Georgakilas, Ch. Papavassiliou, G. Constantinidis, K. Tsagaraki, H. Krasny, E. Löchtermann, and P. Panayotatos. Effects of Si(100) tilting angle and prelayer conditions on GaAs/Si heterostructures. *Applied Surface Science*, **102**: 67–72, 1996. doi: 10.1016/0169-4332(96)00022-0 (see p. 180)

[27] I.J. Luxmoore, R. Toro, O.D. Pozo-Zamudio, N.A. Wasley, E.A. Chekhovich, A.M. Sanchez, R. Beanland, A.M. Fox, M.S. Skolnick, H.Y. Liu, and A.I. Tartakovskii. III-V quantum light source and cavity-QED on Silicon. *Scientific Reports*, **3**: 2013. doi: 10.1038/srep01239 (see pp. 180, 182)

[28] P.J. McNally. Techniques: 3D imaging of crystal defects. *Nature*, **496**: 37–38, 2013. doi: 10.1038/nature12089 (see p. 180)

[29] M. Yamaguchi and C. Amano. Efficiency calculations of thin-film GaAs solar cells on Si substrates. *Journal of Applied Physics*, **58**: 3601–3606, 1985. doi: 10.1063/1.335737 (see pp. 180, 181)

[30] S.A. Ringel, J.A. Carlin, C.L. Andre, M.K. Hudait, M. Gonzalez, D.M. Wilt, E.B. Clark, P. Jenkins, D. Scheiman, A. Allerman, E.A. Fitzgerald, and C.W. Leitz. Single-junction InGaP/GaAs solar cells grown on Si substrates with SiGe buffer layers. *Progress in Photovoltaics: Research and Applications*, **10**: 417–426, 2002. doi: 10.1002/pip.448 (see pp. 180, 181, 183)

[31] T. Jimbo, T. Soga, and Y. Hayashi. Development of new materials for solar cells in Nagoya Institute of Technology. *Sci. Technol. Adv. Mater.*, **6**: 27, 2005. doi: 10.1016/j.stam.2004.07.002 (see p. 181)

[32] M. Umeno, T. Kato, T. Egawa, T. Soga, and T. Jimbo. High efficiency AlGaAs/Si tandem solar cell over 20%. *Solar Energy Materials and Solar Cells*, **41-42**: 395–403, 1996. doi: 10.1016/0927-0248(95)00123-9 (see p. 181)

[33] M. Kaya and Y. Atici. Studies of lattice mismatch and threading dislocations in GaAs/Si grown by MBE. *Superlattices and Microstructures*, **35**: 35–44, 2004. doi: 10.1016/j.spmi.2004.04.003 (see p. 182)

[34] M. A. Putyato, B. R. Semyagin, E. A. Emel'yanov, N. A. Pakhanov, and V. V. Preobrazhenskii. Molecular-beam epitaxy of GaAs/Si(001) structures for high-performance tandem A III B V/Si-solar energy converters on an active silicon substrate. *Russian Physics Journal*, **53**: 906–913, 2011. doi: 10.1007/s11182-011-9509-3 (see p. 182)

[35] J. Geisz. III-V/Silicon Lattice-Matched Tandem Solar Cells. *NREL Conference paper*, 520–36991, 2004. (see p. 182)

[36] T. Roesener, V. Klinger, C. Weuffen, D. Lackner, and F. Dimroth. Determination of heteroepitaxial layer relaxation at growth temperature from room temperature X-ray reciprocal space maps. *Journal of Crystal Growth*, **368**: 21–28, 2013. doi: 10.1016/j.jcrysgro.2013.01.007 (see p. 182)

[37] J.R. Lang, J. Faucher, S. Tomasulo, K.N. Yaung, and M.L. Lee. Comparison of GaAsP solar cells on GaP and GaP/Si. *Applied Physics Letters*, **103**: 092102, 2013. doi: 10.1063/1.4819456 (see p. 182)

[38] T. Nguyen Thanh, C. Robert, W. Guo, A. Létoublon, C. Cornet, G. Elias, A. Ponchet, T. Rohel, N. Bertru, A. Balocchi, O. Durand, J. S. Micha, M. Perrin, S. Loualiche, X. Marie, and A. Le Corre. Structural and optical analyses of GaP/Si and (GaAsPN/GaPN)/GaP/Si nanolayers for integrated photonics on silicon. *Journal of Applied Physics*, **112**: 053521–053521–8, 2012. doi: doi:10.1063/1.4751024 (see p. 182)

[39] T.J. Grassman, J.A. Carlin, B. Galiana, F. Yang, M.J. Mills, and S.A. Ringel. MOCVD-Grown GaP/Si Subcells for Integrated IIIâĂŞV/Si Multijunction Photovoltaics. *IEEE Journal of Photovoltaics*, **Early Access Online**: 2014. doi: 10.1109/JPHOTOV.2014.2308727 (see p. 182)

[40] Tyler J. Grassman, Andrew M. Carlin, Javier Grandal, Chris Ratcliff, Limei Yang, Michael J. Mills, and Steven A. Ringel. Spectrum-optimized Si-based III-V multijunction photovoltaics. 82560R–82560R, 2012. doi: 10.1117/12.909658 (see p. 182)

[41] F. Dimroth, T. Roesener, S. Essig, C. Weuffen, A. Wekkeli, E. Oliva, G. Siefer, K. Volz, T. Hannappel, D. Haussler, W. Jager, and A.W. Bett. Comparison of Direct Growth and Wafer Bonding for the Fabrication of GaInP/GaAs Dual-Junction Solar Cells on Silicon. *IEEE Journal of Photovoltaics*, **4**: 620–625, 2014. doi: 10.1109/JPHOTOV.2014.2299406 (see pp. 182, 183)

[42] C.L. Andre, J.A. Carlin, J.J. Boeckl, D.M. Wilt, M.A. Smith, A.J. Pitera, M.L. Lee, E.A. Fitzgerald, and S.A. Ringel. Investigations of high-performance GaAs solar cells grown on Ge-Si1-xGex-Si substrates. *IEEE Transactions on Electron Devices*, **52**: 1055–1060, 2005. doi: 10.1109/TED.2005.848117 (see p. 183)

[43] J. Faucher, A. Gerger, S. Tomasulo, C. Ebert, A. Lochtefeld, A. Barnett, and M. L. Lee. Single-junction GaAsP solar cells grown on SiGe graded buffers on Si. *Applied Physics Letters*, **103**: 191901, 2013. doi: 10.1063/1.4828879 (see p. 183)

[44] H. Uchida, T. Soga, H. Nishikawa, T. Jimbo, and M. Umeno. Reduction of dislocation density by thermal annealing for GaAs/GaSb/Si heterostructure. *Journal of Crystal Growth*, **150, Part 1**: 681–684, 1995. doi: 10.1016/0022-0248(95)80295-N (see p. 183)

[45] D. Huffaker. Novel monolithic integration of Ill-Sb materials on Si substrates. *SPIE Newsroom*, **Available online**: 2008. doi: 10.1117/2.1200801.1002 (see p. 183)

[46] Y. Alaskar, S. Arafin, D. Wickramaratne, M.A. Zurbuchen, L. He, J. McKay, Q. Lin, M.S. Goorsky, R.K. Lake, and K.L. Wang. Towards van der Waals Epitaxial Growth of GaAs on Si using a Graphene Buffer Layer. *Advanced Functional Materials*, n/a–n/a, 2014. doi: 10.1002/adfm.201400960 (see p. 183)

[47] J.M. Zahler, K. Tanabe, C. Ladous, T. Pinnington, F.D. Newman, and H.A. Atwater. InGaAs Solar Cells Grown on Wafer-Bonded InP/Si Epitaxial Templates. *MRS Online Proceedings Library*, **1012**: 2007. doi: 10.1557/PROC-1012-Y01-09 (see p. 183)

[48] K. Tanabe, A. Fontcuberta i Morral, H.A. Atwater, D.J. Aiken, and M.W. Wanlass. Direct-bonded GaAsâĹŢInGaAs tandem solar cell. *Applied Physics Letters*, **89**: 102106, 2006. doi: 10.1063/1.2347280 (see p. 183)

[49] P. Ramm, J.J.-Q. Lu, and M.M.V. Taklo. *Handbook of wafer bonding*. English Weinheim: Wiley-VCH, 2012. (see p. 183)

[50] C.Y. Yeo, D.W. Xu, S.F. Yoon, and E.A. Fitzgerald. Low temperature direct wafer bonding of GaAs to Si via plasma activation. *Applied Physics Letters*, **102**: 054107–054107–4, 2013. doi: doi:10.1063/1.4791584 (see p. 183)

[51] K. Tanabe, K. Watanabe, and Y. Arakawa. III-V/Si hybrid photonic devices by direct fusion bonding. *Scientific Reports*, **2**: 2012. doi: 10.1038/srep00349 (see p. 183)

[52] I. Mathews, D. O'Mahony, K. Thomas, E. Pelucchi, B. Corbett, and A.P. Morrison. Adhesive bonding for mechanically stacked solar cells. *Progress in Photovoltaics: Research and Applications*, n/a–n/a, 2014. doi: 10.1002/pip.2517 (see p. 184)

[53] X. Sheng, C.A. Bower, S. Bonafede, J.W. Wilson, B. Fisher, M. Meitl, H. Yuen, S. Wang, L. Shen, A.R. Banks, C.J. Corcoran, R.G. Nuzzo, S. Burroughs, and J.A. Rogers. Printing-based assembly of quadruple-junction four-terminal microscale solar cells and their use in high-efficiency modules. *Nature Materials*, **13**: 593–598, 2014. doi: 10.1038/nmat3946 (see p. 184)

[54] J.J. Schermer, G.J. Bauhuis, P. Mulder, E.J. Haverkamp, J. van Deelen, A.T.J. van Niftrik, and P.K. Larsen. Photon confinement in high-efficiency, thin-film III-V solar cells obtained by epitaxial lift-off. *Thin Solid Films*, **511-512**: 645–653, 2006. doi: 10.1016/j.tsf.2005.12.135 (see pp. 184, 189, 190)

[55] A.T.J. Van Niftrik. *The epitaxial lift-off method : III/V materials and HF etch process studies*. PhD thesis. Radboud University, Netherlands, 2008. (see p. 184)

[56] C.-W. Cheng, K.-T. Shiu, N. Li, S.-J. Han, L. Shi, and D.K. Sadana. Epitaxial lift-off process for gallium arsenide substrate reuse and flexible electronics. *Nature Communications*, **4**: 1577, 2013. doi: 10.1038/ncomms2583 (see pp. 184, 190)

[57] A. van Geelen, P.R. Hageman, G.J. Bauhuis, P.C. van Rijsingen, P. Schmidt, and L.J. Giling. Epitaxial lift-off GaAs solar cell from a reusable GaAs substrate. *Materials Science and Engineering: B*, **45**: 162–171, 1997. doi: 10.1016/S0921-5107(96)02029-6 (see pp. 185, 189–191)

[58] G.J. BAUHUIS, P. MULDER, E.J. HAVERKAMP, J.J. SCHERMER, E. BONGERS, G. OOMEN, W. KOSTLER, and G. STROBL. Wafer reuse for repeated growth of III-V solar cells. *Progress in Photovoltaics: Research and Applications*, **18**: 155–159, 2010. DOI: 10.1002/pip.930 (see pp. 185, 190)

[59] K. LEE, J.D. ZIMMERMAN, X. XIAO, K. SUN, and S.R. FORREST. Reuse of GaAs substrates for epitaxial lift-off by employing protection layers. *Journal of Applied Physics*, **111**: 033527–033527–6, 2012. DOI: doi:10.1063/1.3684555 (see pp. 185, 189, 190)

[60] I. YONENAGA. Hardness, Yield Strength, and Dislocation Velocity in Elemental and Compound Semiconductors. *Materials Transactions*, **46**: 1979–1985, 2005. DOI: 10.2320/matertrans.46.1979 (see p. 186)

[61] S. OBERG, P.K. SITCH, R. JONES, and M.I. HEGGIE. First-principles calculations of the energy barrier to dislocation motion in Si and GaAs. *Physical Review B*, **51**: 13138–13145, 1995. DOI: 10.1103/PhysRevB.51.13138 (see p. 186)

[62] J. YANG, Z. PENG, D. CHEONG, and R.N. KLEIMAN. III-V on Silicon Multi-Junction Solar Cell with 25% 1-Sun Efficiency via Direct Metal Interconnect and Areal Current Matching. *27th EU PVSEC Proceedings*, **1BO.12.6**: 160 –163, 2012. DOI: 10.4229/27thEUPVSEC2012-1BO.12.6 (see p. 186)

[63] H.J. SNAITH. Perovskites: The Emergence of a New Era for Low-Cost, High-Efficiency Solar Cells. *The Journal of Physical Chemistry Letters*, **4**: 3623–3630, 2013. DOI: 10.1021/jz4020162 (see p. 188)

[64] R.R. KING, D. BHUSARI, A. BOCA, D. LARRABEE, X.-Q. LIU, W. HONG, C.M. FETZER, D.C. LAW, and N.H. KARAM. Band gap-voltage offset and energy production in next-generation multijunction solar cells. *Progress in Photovoltaics: Research and Applications*, **19**: 797–812, 2011. DOI: 10.1002/pip.1044 (see p. 188)

[65] J.F. GEISZ, M.A. STEINER, I. GARCIA, S.R. KURTZ, and D.J. FRIEDMAN. Enhanced external radiative efficiency for 20.8% efficient single-junction GaInP solar cells. *Applied Physics Letters*, **103**: 041118, 2013. DOI: 10.1063/1.4816837 (see p. 188)

[66] B.M. KAYES, HUI NIE, R. TWIST, S.G. SPRUYTTE, F. REINHARDT, I.C. KIZILYALLI, and G.S. HIGASHI. 27.6% Conversion efficiency, a new record for single-junction solar cells under 1 sun illumination. *37th IEEE Photovoltaic Specialists Conference (PVSC)*, 000004 –000008, 2011. DOI: 10.1109/PVSC.2011.6185831 (see pp. 188–190)

[67] G.F. VIRSHUP, C.W. FORD, and J.G. WERTHEN. A 19% efficient AlGaAs solar cell with graded band gap. *Applied Physics Letters*, **47**: 1319–1321, 1985. DOI: 10.1063/1.96266 (see p. 188)

[68] M. TAGUCHI, A YANO, S. TOHODA, K. MATSUYAMA, Y. NAKAMURA, T. NISHIWAKI, K. FUJITA, and E. MARUYAMA. 24.7 % Record Efficiency HIT Solar Cell on Thin Silicon Wafer. *IEEE Journal of Photovoltaics*, **4**: 96–99, 2014. DOI: 10.1109/JPHOTOV.2013.2282737 (see p. 188)

[69] N.E. POSTHUMA, J. VAN DER HEIDE, G. FLAMAND, and J. POORTMANS. Emitter Formation and Contact Realization by Diffusion for Germanium Photovoltaic Devices. *IEEE Transactions on Electron Devices*, **54**: 1210–1215, 2007. DOI: 10.1109/TED.2007.894610 (see p. 188)

[70] O.D. MILLER, E. YABLONOVITCH, and S.R. KURTZ. Intense Internal and External Fluorescence as Solar Cells Approach the Shockley-Queisser Efficiency Limit. *IEEE Journal of Photovoltaics*, **2**: arXiv: 1106.1603, 303–311, 2012. DOI: 10.1109/JPHOTOV.2012.2198434 (see p. 189)

[71] J. Yoon, S. Jo, I.S. Chun, I. Jung, H.-S. Kim, M. Meitl, E. Menard, X. Li, J.J. Coleman, U. Paik, and J.A. Rogers. GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies. *Nature*, **465**: 329–333, 2010. doi: 10.1038/nature09054 (see pp. 189, 190)

[72] D. Shahrjerdi, S.W. Bedell, C. Bayram, C.C. Lubguban, K. Fogel, P. Lauro, J.A. Ott, M. Hopstaken, M. Gayness, and D. Sadana. Ultralight High-Efficiency Flexible InGaP/(In)GaAs Tandem Solar Cells on Plastic. *Advanced Energy Materials*, **3**: 566–571, 2013. doi: 10.1002/aenm.201200827 (see p. 190)

[73] S.W. Bedell, D. Shahrjerdi, B. Hekmatshoar, K. Fogel, P.A. Lauro, J.A. Ott, N. Sosa, and D. Sadana. Kerf-Less Removal of Si, Ge, and III-V Layers by Controlled Spalling to Enable Low-Cost PV Technologies. *IEEE Journal of Photovoltaics*, **2**: 141 –147, 2012. doi: 10.1109/JPHOTOV.2012.2184267 (see p. 190)

[74] E. Yablonovitch, T. Gmitter, J.P. Harbison, and R. Bhat. Extreme selectivity in the lift-off of epitaxial GaAs films. *Applied Physics Letters*, **51**: 2222–2224, 1987. doi: 10.1063/1.98946 (see p. 190)

[75] G.J. Hayes and B.M. Clemens. Laser Liftoff of GaAs Thin Films. arXiv:1408.1977, 2014. (see p. 190)

[76] G.J. Bauhuis, P. Mulder, E.J. Haverkamp, J.C.C.M. Huijben, and J.J. Schermer. 26.1% thin-film GaAs solar cell using epitaxial lift-off. *Solar Energy Materials and Solar Cells*, **93**: 1488–1491, 2009. doi: 10.1016/j.solmat.2009.03.027 (see p. 190)

[77] J.J. Schermer, P. Mulder, G.J. Bauhuis, M.M.A.J. Voncken, J. van Deelen, E. Haverkamp, and P.K. Larsen. Epitaxial Lift-Off for large area thin film III/V devices. *physica status solidi (a)*, **202**: 501–508, 2005. doi: 10.1002/pssa.200460410 (see p. 190)

[78] L.S. Mattos, S.R. Scully, M. Syfu, E. Olson, L. Yang, C. Ling, B.M. Kayes, and G. He. New module efficiency record: 23.5% under 1-sun illumination using thin-film single-junction GaAs solar cells. *38th IEEE Photovoltaic Specialists Conference (PVSC)*, 003187 – 003190, 2012. doi: 10.1109/PVSC.2012.6318255 (see p. 190)

[79] M. Steiner, S.P. Philipps, M. Hermle, A.W. Bett, and F. Dimroth. Validated front contact grid simulation for GaAs solar cells under concentrated sunlight. *Progress in Photovoltaics: Research and Applications*, **19**: 73–83, 2011. doi: 10.1002/pip.989 (see p. 190)

[80] L. Esaki. New Phenomenon in Narrow Germanium p-n Junctions. *Physical Review*, **109**: 603–604, 1958. doi: 10.1103/PhysRev.109.603 (see pp. 195, 196)

[81] J.F. Wheeldon, C.E. Valdivia, A.W. Walker, G. Kolhatkar, A. Jaouad, A. Turala, B. Riel, D. Masson, N. Puetz, S. Fafard, R. ArÃĹs, V. Aimez, T.J. Hall, and K. Hinzer. Performance comparison of AlGaAs, GaAs and InGaP tunnel junctions for concentrated multijunction solar cells. *Progress in Photovoltaics: Research and Applications*, **19**: 442–452, 2011. doi: 10.1002/pip.1056 (see pp. 195–197)

[82] L. Esaki, Y. Arakawa, and M. Kitamura. Esaki diode is still a radio star, half a century on. *Nature*, **464**: 31–31, 2010. doi: 10.1038/464031b (see p. 196)

[83] W. Guter and A.W. Bett. I-V Characterization of Tunnel Diodes and Multijunction Solar Cells. *IEEE Transactions on Electron Devices*, **53**: 2216–2222, 2006. doi: 10.1109/TED.2006.881051 (see pp. 196, 197)

[84] G.J. Bauhuis, P. Mulder, and J.J. Schermer. Ultra-thin, high performance tunnel junctions for III-V multijunction cells. *Progress in Photovoltaics: Research and Applications*, **22**: 656–660, 2012. doi: 10.1002/pip.2333 (see p. 197)

[85] I. García, I. Rey-Stolle, and C. Algora. Performance analysis of AlGaAs/GaAs tunnel junctions for ultra-high concentration photovoltaics. *Journal of Physics D: Applied Physics*, **45**: 045101, 2012. doi: 10.1088/0022-3727/45/4/045101 (see p. 197)

[86] M. Baudrit and C. Algora. Tunnel Diode Modeling, Including Nonlocal Trap-Assisted Tunneling: A Focus on III #x2013;V Multijunction Solar Cell Simulation. *IEEE Transactions on Electron Devices*, **57**: 2564–2571, 2010. doi: 10.1109/TED.2010.2061771 (see p. 197)

[87] M. Hermle, G. Letay, S.P. Philipps, and A.W. Bett. Numerical simulation of tunnel diodes for multi-junction solar cells. *Progress in Photovoltaics: Research and Applications*, **16**: 409–418, 2008. doi: 10.1002/pip.824 (see p. 197)

[88] J. Chevallier, W.C. Dautremont-Smith, C.W. Tu, and S.J. Pearton. Donor neutralization in GaAs(Si) by atomic hydrogen. *Applied Physics Letters*, **47**: 108–110, 1985. doi: 10.1063/1.96284 (see p. 199)

[89] S.J. Pearton, W.C. Dautremont-Smith, J. Chevallier, C.W. Tu, and K.D. Cummings. Hydrogenation of shallow-donor levels in GaAs. *Journal of Applied Physics*, **59**: 2821–2827, 1986. doi: 10.1063/1.336964 (see p. 199)

[90] B. Theys, F. Bourgeois, J. Chevallier, L. Svob, M. Miloche, R. Driad, and J.L. Benchimol. Transport properties of hydrogenated p-GaInAs doped with carbon. *Journal of Applied Physics*, **80**: 2300–2304, 1996. doi: 10.1063/1.363060 (see p. 199)

[91] S.J. Pearton, C.S. Wu, M.l Stavola, F. Ren, J. Lopata, W.C. Dautremont-Smith, S.M. Vernon, and V.E. Haven. Hydrogenation of GaAs on Si: Effects on diode reverse leakage current. *Applied Physics Letters*, **51**: 496–498, 1987. doi: 10.1063/1.98378 (see p. 199)

[92] W.C. Dautremont-Smith. Hydrogen in III-V Semiconductors. *MRS Online Proceedings Library*, **104**: 313, 1987. doi: 10.1557/PROC-104-313 (see p. 199)

[93] J. Lagowski, M. Kaminska, J. M. Parsey Jr, H. C. Gatos, and M. Lichtensteiger. Passivation of the dominant deep level (EL2) in GaAs by hydrogen. *Applied Physics Letters*, **41**: 1078–1080, 1982. doi: 10.1063/1.93407 (see p. 199)

[94] G. Wang, K. Ohtsuka, T. Soga, T. Jimbo, and M.i Umeno. Hydrogen Plasma Passivation and Improvement of the Photovoltaic Properties of a GaAs Solar Cell Grown on Si Substrate. *Japanese Journal of Applied Physics*, **38**: 3504, 1999. doi: 10.1143/JJAP.38.3504 (see p. 199)

[95] A. Jalil, A. Heurtel, Y. Marfaing, and J. Chevallier. Passivation and generation of deep level defects in hydrogenated n-GaAs (Si). *Journal of Applied Physics*, **66**: 5854–5861, 1989. doi: 10.1063/1.343607 (see p. 199)

[96] T.P. Brody. Nature of the Valley Current in Tunnel Diodes. *Journal of Applied Physics*, **33**: 100–111, 1962. doi: 10.1063/1.1728464 (see p. 200)

[97] K. Majumdar, P. Thomas, W. Loh, P. Hung, K. Matthews, D. Pawlik, B. Romanczyk, M. Filmer, A. Gaur, R. Droopad, S.L. Rommel, C. Hobbs, and P.D. Kirsch. Mapping Defect Density in MBE Grown $In_{0.53}Ga_{0.47}As$ Epitaxial Layers on Si Substrate Using Esaki Diode Valley Characteristics. *IEEE Transactions on Electron Devices*, **61**: 2049–2055, 2014. doi: 10.1109/TED.2014.2318597 (see p. 200)

[98] E. Barrigón, I. García, L. Barrutia, I. Rey-Stolle, and C. Algora. Highly conductive p++AlGaAs/n++-GaInP tunnel junctions for ultra-high concentrator solar cells. *Progress in Photovoltaics: Research and Applications*, **22**: 399–404, 2014. doi: 10.1002/pip.2476 (see p. 200)

[99] V.L. Berkovits, V.P. Ulin, M. Losurdo, P. Capezzuto, G. Bruno, G. Perna, and V. Capozzi. Wet chemical nitridation of GaAs (100) by hydrazine solution for surface passivation. *Applied Physics Letters*, **80**: 3739, 2002. doi: 10.1063/1.1479212 (see p. 201)

[100] P. Roca i Cabarrocas. A fully automated hot-wall multiplasma-monochamber reactor for thin film deposition. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, **9**: 2331, 1991. doi: 10.1116/1.577318 (see p. 201)

Conclusion

The growth of monocrystalline material is usually performed with high temperature techniques (∼700°C and beyond) and/or ultra-high vacuum set-ups (10^{-9}mb and below). However during this PhD thesis we have focused on a completely unusual way of epitaxial growth: low temperature plasma enhanced chemical vapor deposition - PECVD. As a matter of fact, this technique, widely used by the semiconductor industry for large area depositions of amorphous and nanocrystalline materials, enables the growth of monocrystalline material without high vacuum at temperatures in the 200°C range. Our goal was to gain insight into this low temperature epitaxial (LTE) process, applied to Si and SiGe crystals, as well as to investigate the potential of such low temperature deposited materials for single and multijunction solar cells.

Contributions to the research field

Three main research axis were investigated during this doctoral work: i) the silicon low temperature homoepitaxial process itself, from SiH_4/H_2 plasma ii) thin film crystalline Si and SiGe solar cells having a photo-active epitaxial layer of few microns thick, and iii) the combination of III-V and silicon for tandem devices using LTE.

First, using ellipsometry, Raman, TEM and XRD, we have confirmed that monocrystal silicon layers can be grown on c-Si substrates in a standard PECVD reactor from SiH_4/H_2 gas precursors; thicknesses up to 8μm were obtained (dep. rate of 1-3 Å/s). As an alternative to the classical wet HF dipping used to remove silicon native oxide from the crystalline substrate prior to epitaxial growth, a dry process has been demonstrated. Using a SiF_4 etching plasma at 175°C, the c-Si native oxide removal has been precisely monitored by in-situ ellipsometry, and excellent epitaxial growth quality has been achieved subsequently in the same plasma chamber. We have shown that the silane dilution in H_2, namely $SiH_4/(H_2+SiH_4)$, is an important parameter that controls the material crystallinity. A small dilution results in microcrystalline layers, a high dilution results in a-Si:H material and the epitaxial growth happens at the transition between these two regimes. The low temperature epitaxial silicon is a highly hydrogenated material, H content can be as high as few 10^{20}cm^{-3}; thus this material could be labeled epi-Si:H. By TEM, the main crystal defects identified were point defects, stacking faults and H-platelets; Secco etching has revealed a dislocation density $< 1\times10^5$cm^2. However, since they are passivated by hydrogen, most of crystal defects do not behave as recombination centers. This hydrogen in the epitaxial layer is responsible for a compressive stress ($a_{epi-Si:H} > a_{c-Si}$); XRD has confirmed the pseudomorphic growth of epi-Si:H on c-Si. In addition, a hydrogen plasma treatment of the wafer surface before epitaxy has been shown to be another efficient way to control the stress in the epi-layer. The best electron(hole) mobilities reported in this work was 400(125) cm^2/(V.s). Using cross section epi-Si Raman mapping and in-situ ellipsometry, we could demonstrate the epitaxial quality improvement with increasing layer thickness. And finally, the existence of an energy upper bond, for incoming charged particles, above which epitaxial growth is lost has been experimentally proven. Below this threshold, the impinging ions on the growing film may provide additional surface energy enabling epitaxial growth at such low temperature.

Thin epitaxial solar cells on wafer reaching a record 8.8% in 4.2μm thick absorber have been

demonstrated. The excellent fill factor of 80.5% obtained confirms the excellent quality of epi-Si:H. Diffusion length up to 20μm were estimated for these solar cells. Compared to wafer based solar cells, high impurity concentration and defect density are acceptable in thin film crystalline solar cells: the rule of thumb is to keep the diffusion length roughly 3 times higher than the absorber thickness for efficient carriers collection. The classic ray optics light trapping is not suited for ultra-thin c-Si films of few microns, but nanostructures can instead efficiently enhance absorption by impedance matching and mode coupling effects. Experimental epitaxial solar cells including nanostructures were found to be very challenging: the absorption gain is often counterbalanced by surface passivation issues. Among the different techniques/patterns tested, the inverted pyramids produced by wet etching was identified as the most promising solution. Furthermore, we have demonstrated that epi-Si:H layers can be easily lifted-of by a rapid annealing step around 400°C. Transfer of few cm^2 PECVD epi-Si layers on PDMS/glass or directly on glass by anodic bonding was successfully achieved. The low density (porous) epi-Si/c-Si interface, as confirmed by STEM-HAADF, offers an easy cleavage direction for detachment. This weak interface is caused partially by H-platelets parallel to the interface. A good quality c-Si/epi-Si interface (high quality surface cleaning and vacuum level) will increase the epitaxial cell V_{oc} but prevents from layer lift-off. We have also shown that the low temperature PECVD process was well suited for heteroepitaxial growth: epi-Ge layers grown on c-Si and epi-SiGe layers grown on c-Si were obtained for the first time. A record SiGe epitaxial cell with 27% Ge reaching 18.8 mA/cm^2 for 1.9μm, 77.5% fill factor and 6.1% efficiency has been demonstrated.

III-V and silicon offer a great combination of band gap: more than 40% and 45% are predicted for tandem and triple junctions featuring a Si bottom cell. The classic approach consists in growing growing GaAs on Si substrate, but the lattice and thermal mismatches remain a big challenge. Thus, unlike the general trend of growing III-V on silicon, we have shown that growing silicon on III-V is a very interesting alternative approach. Indeed, it suppresses the problem of anti-phase domains encountered with the GaAs/Si polar/non-polar interface. By using low temperature PECVD epitaxy, the thermal mismatch and diffusion related problems (as proven by SIMS) are also drastically reduced. Very good Si crystal quality was achieved by direct PECVD epitaxial growth of Si on GaAs at 175°C, as confirmed by ellipsometry, Raman, TEM and XRD. A one pump down and low temperature process was demonstrated using SiF_4 etching plasma to remove GaAs oxide, followed by epitaxy from SiH_4/H_2 gas precursors. The epi-Si material grown on GaAs exhibits similar crystal quality compared to the one grown on c-Si; in addition, similar growth rates and effects of silane dilution were observed. The lattice mismatch between GaAs and Si is relaxed immediately at the interface, and no threading dislocations were observed by TEM. The best epi-Si on GaAs has a Raman FWHM of $7.6cm^{-1}$. Within the IMPETUS research project, we have proposed an inverted metamorphic tandem device with AlGaAs MOCVD-grown top cell and SiGe PECVD grown bottom cell. Building blocks towards this multijunction were demonstrated: GaAs cells with more than 20% efficiency, and performant AlGaAs/GaInP tunnel junction reaching 56 A/cm^2 peak current. Moreover, we could show a striking improvement of the TJ characteristics upon a H_2 plasma exposure; this effect was attributed to the enhancement of trap assisted tunneling mechanism. This provides a further proof of the validity of this approach.

Open questions and futur work

Luckily for the next PhD students, there are still plenty of interesting things to study in the field of low temperature PECVD epitaxy. Indeed, the question of how hydrogen is incorporated into the c-Si lattice remains open: in addition to H-platelets, hydrogen could also be present as interstitial or molecular impurities. Since this low temperature epi-Si contains a lot of hydrogen, one can wonder if there would be some light induced degradation effects. The electronic properties should be studied in more details, as well as their evolution with deposition temperature (and H-content): can we match microelectronic grade electronic properties for epi-Si layers grown by PECVD in the 150-350°

temperature range? In addition the effect of lift-off and transfer process on the epi-layer should be studied in more details. From an industrial point of view, the deposition rate affects strongly the cost, and the upper limit for PECVD epi-Si:H remains to be found. Another intersting point would be to study more precisely the main physical reason which hinders epitaxial growth on (111) oriented c-Si substrate as compared to (100). More generally the growth mechanism should be studied in details, especially the contribution of plasma borned nanoparticles.

With very little room for efficiency improvement, c-Si technology can further drive the cost down by reducing absorber thickness to few tens of microns. The c-Si cell of tomorrow will most likely be $<40\mu$m and >20% and potentially on flexible substrate. Thin film epitaxial Si solar cells are thus building the bridge between the world of thin film and crystalline solar cells. PECVD lifted-off epi-Si cells with absorber in the 10-15μm range, can pass the 15% efficiency threshold using wet etched inverted pyramids as a front light trapping feature, and may even reach 20% if excellent light trapping and passivation are achieved. This would be a great result to achieve. Using higher growth temperature ($\sim$300°C) and appropriate in-situ wafer surface cleaning, better interface quality and electronic properties are expected; this should improve epi-cells performances. Efficient lifted-off nano-structured PECVD epi-Si cells still need to be fabricated.

We have demonstrated that PECVD is a suitable technique for the growth of mono-crystalline Si, Ge and SiGe layers. It seems also very likely that this technique would enable epitaxial growth of III-V materials, and thus offer potentially significant cost reduction compared to MOCVD or MBE approach. Since the epitaxy itself is a significant fraction of the III-V cell cost, this option is worth being explored. Many aspects of the Si growth on GaAs require detailed study: - material quality evolution with thickness - interface electrical properties - doped epi-Si(Ge) layers. In addition, detailed efficiency calculations of the proposed tandem device, by taking into account the incomplete absorption in the SiGe bottom cell should be performed. Before the tandem device itself, a tunnel junction made of GaAs/Si would be an important milestone. Finally, the best technological process to transfer and contact the inverted III-V/Si stack should be found.

List of publications

Peer reviewed publications

- R. Cariou, J. Tang, N. Ramay, R. Ruggeri, and P. Roca i Cabarrocas. Low temperature epitaxial growth of SiGe absorber for thin film heterojunction solar cells. *Solar Energy Materials and Solar Cells*, **134**: 15-21, 2015. doi: 10.1016/j.solmat.2014.11.018

- I. Cosme, R. Cariou, W. Chen, M. Foldyna, R. Boukhicha, P. Roca i Cabarrocas, K.D. Lee, C. Trompoukis, and V. Depauw, Lifetime assessment in crystalline silicon: From nanopatterned wafer to ultra-thin crystalline films for solar cells, *Solar Energy Materials and Solar Cells*, **in press**, 2014. doi: 10.1016/j.solmat.2014.10.019.

- B. Bruneau, R. Cariou, J. Dornstetter, M. Lepecq, J.-L. Maurice, P. Roca i Cabarrocas, and E.V. Johnson. Ion Energy Threshold in Low-Temperature Silicon Epitaxy for Thin-Film Crystalline Photovoltaics. *IEEE Journal of Photovoltaics*, **4**: 1361-1367, 2014. doi: 10.1109/JPHOTOV.2014.2357256

- R. Cariou, R. Ruggeri, X. Tan, G. Mannino, J. Nassar, and P. Roca i Cabarrocas. Structural properties of relaxed thin film germanium layers grown by low temperature RF-PECVD epitaxy on Si and Ge (100) substrates. *AIP Advances*, **4**: 077103, 2014. doi: 10.1063/1.4886774

- C. Trompoukis, I. Abdo, R. Cariou, I. Cosme, W. Chen, O. Deparis, A. Dmitriev, E. Drouard, M. Foldyna, E.G. Caurel, I. Gordon, et al. Photonic nanostructures for advanced light trapping in thin crystalline silicon solar cells. *Physica Status Solidi A*, 2014. doi: 10.1002/pssa.201431180

- S. Chakraborty, R. Cariou, M. Labrune, P. Roca i Cabarrocas, and P. Chatterjee. Feasibility of using thin crystalline silicon films epitaxially grown at 165°C in solar cells: A computer simulation study. *EPJ Photovoltaics*, **4**: 45103, 2013. doi: 10.1051/epjpv/2013014

- P. Roca i Cabarrocas, R. Cariou, and M. Labrune. Low temperature plasma deposition of silicon thin films: From amorphous to crystalline. *Journal of Non-Crystalline Solids*, **358**: 2000-2003, 2012. doi: 10.1016/j.jnoncrysol.2011.12.113

- R. Cariou, M. Labrune, and P. Roca i Cabarrocas. Thin crystalline silicon solar cells based on epitaxial films grown at 165°C by RF-PECVD. *Solar Energy Materials and Solar Cells*, **95**: 2260-2263, 2011. doi: 10.1016/j.solmat.2011.03.038

Conference proceedings

- S.N. Granata, L. Tous, T. Bearda, J. Nassar, R. Cariou, C. Trompoukis, K. Van Nieuwenhuysen, Y. Abdulraheem, I. Gordon, J. Szlufcik, P. Roca i Cabarrocas, et al. Optical and Electrical Improvement of Rear Side ITO for Heterojunction Back Contact Solar Cells. *29th EU PVSEC Proceedings*, **2AV.3.23**: 1024 - 1027, 2014. doi: 10.4229/EUPVSEC20142014-2AV.3.23

- R. Leal, J.-C. Dornstetter, F. Haddad, B. Bruneau, R. Cariou, W. Chen, I. Cosme Bolanos, G. Poulain, J.-L. Maurice and P. Roca i Cabarrocas. Epitaxial Growth of Silicon Thin Films by Low Temperature RF-PECVD from $SiF_4/H_2/Ar$. *29th EU PVSEC Proceedings*, **3DV.4.41**: 1959 - 1962, 2014. doi: 10.4229/EUPVSEC20142014-3DV.4.41

- V. Depauw, I. Abdo, R. Boukhicha, R. Cariou, W. Chen, I. Cosme Bolanos, O. Deparis, He Ding, A. Dmitriev,E. Drouard, O. El Daif, et al. Nanophotonics for ultra-thin crystalline silicon photovoltaics: when photons (actually) meet electrons. *29th EU PVSEC Proceedings*, **3BO.6.5**: 1461-1469, 2014. doi: 10.4229/EUPVSEC20142014-3BO.6.5

- R. Cariou, J.-L. Maurice, J. Decobert and P. Roca I Cabarrocas. Direct Epitaxial Growth of Silicon on GaAs by Low Temperature Epitaxy. *40th IEEE PVSC*, 2014.

- R. Cariou, I. Massiot, R. Ruggeri, N. Ramay, J. Tang, A. Cattoni, S. Collin, J. Nassar, and P. Roca i Cabarrocas. Low Temperature Epitaxial Growth of Si and SiGe and Their Transfer to Foreign Substrate. *28th EU PVSEC Proceedings*, **3DO.7.5**: 2225-2227, 2013. doi: 10.4229/28thEUPVSEC2013-3DO.7.5

- R. Cariou, I. Massiot, R. Ruggeri, N. Ramay, J. Tang, A. Cattoni, S. Collin, J. Nassar, and P. Roca i Cabarrocas. Low-temperature SiGe PECVD epitaxy: From wafer equivalent to ultra-thin crystalline solar cells on inexpensive substrates. *39th IEEE PVSC*, 0921-0926, 2013. doi: 10.1109/PVSC.2013.6744294

- M. Khenkin, A. Kazanskii, A. Emelyanov, P. Forsh, K.H. Kim, R. Cariou, and P. Roca i Cabarrocas. Structural, optical and photoelectric properties of hydrogenated polymorphous silicon. *39th IEEE PVSC*, 0563-0567, 2013. doi: 10.1109/PVSC.2013. 6744214

- R. Cariou, R. Ruggeri, P. Chatterjee, J.-L. Gentner, and P. Roca i Cabarrocas. Silicon epitaxy below 200°C: towards thin crystalline solar cells. *SPIE proceedings*, 84700B, 2012. doi: 10.1117/12.929741

- P. Roca i Cabarrocas, K.H. Kim, R. Cariou, M. Labrune, E.V. Johnson, M. Moreno, A.T. Rios, S. Abolmasov, and S. Kasouit. Low Temperature Plasma Synthesis of Nanocrystals and their Application to the Growth of Crystalline Silicon and Germanium Thin Films. *MRS Proceedings*, **1426**: 319-329, 2012. doi: 10.1557/opl.2012.1094

Patent pending

- J.-L. Gentner, R. Cariou and P. Roca i Cabarrocas, Procédé de fabrication d'un dispositif photovoltaïque multi-jonctions et dispositif photovoltaïque multi-jonctions ainsi obtenu, *European procedure*, Filling number EP13305344.

Abstract:

This thesis focuses on epitaxial growth of Si and SiGe at low temperature (∼200°C) by Plasma Enhanced Chemical Vapor Deposition (PECVD), and its application in thin film crystalline solar cells. Our goal is to gain insight into this unusual growth process, as well as to investigate the potential of such low temperature-deposited material for single and multi-junction solar cells.

First, we have proposed a one pump-down plasma process to clean out-of-the-box c-Si wafer surface and grow epitaxial layers of up to 8μm thick, without ultra-high vacuum, in a standard RF-PECVD reactor. By exploring the experimental parameters space, the link between layer quality and important physical variables, such as silane dilution, ion energy, or deposition pressure, has been confirmed. Both material and electrical properties were analyzed, and we found that epitaxial quality improves with film thickness. Furthermore, we could bring evidence of SiGe and Ge epitaxial growth under similar conditions. Then, with the whole process steps <200°C, we have achieved PIN heterojunction solar cells on highly doped substrates with 1-4μm epitaxial absorber, reaching 8.8% efficiency (without light trapping) and 80.5% FF. Replacing Si absorber by epitaxial $Si_{0.73}Ge_{0.27}$ resulted in 11% boost in Jsc. The use of an engineered wafer/epitaxial layer interface and stress enables easy lift off: e.g. we successfully bonded 1.5μm thick 10cm^2 epi-Si to glass. Additionally, we have considered the impact of photonic nanostructures on device properties. Together, the control of growth, transfer and advanced light trapping are paving the way toward highly efficient, ultrathin (<10μm) and low cost c-Si cells. Finally, in contrast with general trend of growing III-V semiconductors on Si, we have studied the hetero-epitaxial growth of Si on III-V. Good crystal quality was achieved by direct Si deposition on GaAs, thanks to reduced thermal load and suppressed polarity issues in this approach. Using MOCVD, we could build GaAs cells with 20% efficiency and III-V tunnel junctions reaching 55A/cm^2. Tunneling improvement upon H-plasma exposure was shown. Those results, combined with III-V layer lift off, validate milestones toward high efficiency tandem AlGaAs(MOVD)/SiGe(PECVD) metamorphic solar cells.

Keywords: PECVD epitaxial growth, Low temperature, Photovoltaic, Silicon, SiGe, Ultra-thin crystalline solar cells, Lift-off and transfer, Photonic nanostructures, Silicon on III-V, GaAs solar cells, Tunnel junctions.

Résumé:

Cette thèse s'intéresse à la croissance épitaxiale de Si et SiGe à basse température (∼200°C) par dépôt chimique en phase vapeur assisté par plasma (PECVD), et à l'utilisation de ces matériaux cristallins dans les cellules solaires en couches minces. L'objectif était de mieux comprendre cette croissance inattendue et d'étudier le potentiel de ces matériaux pour les cellules simples et multijonctions.

Nous avons d'abord démontré qu'il est possible d'effectuer, avec un réacteur PECVD standard, un nettoyage efficace de la surface du c-Si et de poursuivre par une croissance épitaxiale de couches de Si jusqu'à 8μm d'épaisseur. L'impact des paramètres du procédé tels que la dilution du SiH_4 dans l'H_2, l'énergie des ions ou encore la pression totale, sur la qualité des couches a été mis en évidence. Les propriétés électriques et structurelles des couches ont été analysées, et nous avons démontré une amélioration de la qualité cristalline avec l'épaisseur de la couche. La croissance épitaxiale de Ge et SiGe sur c-Si dans des conditions similaires a également été établie. Ensuite, par une séquence d'étapes à moins de 200°C, des hétérojonctions PIN sur substrats très dopés, avec une couche absorbante épitaxiée de 1-4μm ont été réalisées, atteignant 8.8% de rendement (sans piégeage optique) et 80% de FF. Le remplacement du Si par du $Si_{0.73}Ge_{0.27}$ a permis un gain de 11% sur le J_{sc}. Le contrôle de l'interface wafer/épi et des contraintes permet de favoriser le décollement : des couches epi-Si de 1.5μm/10cm^2 ont été reportées sur verre avec succès. Nous avons également analysé l'influence de nanostructures photoniques sur les propriétés des dispositifs. L'étude conjointe de la croissance, du transfert et du piégeage optique ouvre la voie aux cellules c-Si ultra-minces (<10μm) bas côut. Enfin, contrairement au scénario classique de dépôt des matériaux III-V sur Si, nous avons étudié l'hétéroépitaxie de Si sur III-V. Avec cette approche, une bonne qualité cristalline de Si déposé directement sur GaAs est obtenue grâce aux faibles contraintes thermiques et à l'absence de problèmes de polarité à l'interface. Nous avons fabriqué des cellules GaAs avec 20% d'efficacité et des jonctions tunnel atteignant 55A/cm^2 par dépôt MOVPE. Une augmentation du courant tunnel par exposition au plasma d'hydrogène a aussi été démontrée. Ces résultats de croissance, cellule et jonction tunnel, couplés aux techniques de report, valident les briques élémentaires pour atteindre une cellule tandem AlGaAs(MOVPE)/SiGe(PECVD) à haut rendement.

Mots clés : Epitaxie par PECVD, Basse température, Photovoltaique, Silicium, SiGe, Cellules solaires en cristallin ultra-mince, Détachement, Transfert, Nanostructures photoniques, Silicium sur III-V, Cellules GaAs, Jonctions tunnel.