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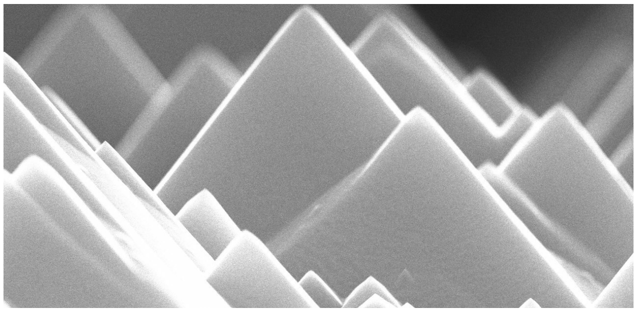
Igor Paul SOBKOWICZ

Study and optimization of the growth of a-Si:H on wet chemically-textured c-Si substrates for the enhancement of a-Si:H/c-Si heterojunction solar cells

Doctoral thesis in Materials Science



Thèse

présentée en vue d'obtenir le grade de

Docteur de l'Ecole Polytechnique

Spécialité Physique/Science des Matériaux
par

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Cette thèse a été soutenue le 9 décembre 2014 à 14h00
Amphithéâtre Becquerel – Ecole Polytechnique
devant le jury composé de:

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Dr.	Erwann Fourmond	Rapporteur
Prof.	Christophe Longeaud	Examinateur
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Dr.	Thierry Mélin	Invité
M.	Mathieu Rouquié	Invité
Prof.	Pere Roca i Cabarrocas	Directeur de thèse

When I saw the pyramids of Giza, it dawned on me that these could not have been made out of (111) planes solely...

A mes chers parents,

Acknowledgements

It's hard to know where to start...3 years at LPICM, constantly meeting new people, gathering new ideas, getting inspired...Let's start from the top.

This Ph.D. thesis has been carried out at the LPICM lab of Ecole Polytechnique within the framework of the Joint-Research Team with the New Energy branch of the TOTAL group. Therefore I would like to thank Bernard Drévillon who was at the head of the LPICM lab in 2011, for allowing me to spend these last 3 years within its walls. I am thankful to Pere Roca i Cabarrocas the LPICM new director who accepted to supervise my Ph.D. thesis. I am especially thankful for his constant optimism (which sometimes needs to be balanced by a French or Russian scientist) that definitely pulls you up to the utmost and eventually leads you to better results. I am very much impressed and thankful for his incredible flexibility, for correcting my presentation and talks on Sundays, vacations, sometimes even at UTC-9, for all the 8 A.M and 8 P.M. meetings, for loading the ARCAM reactor to allow me to efficiently start on Monday morning and for many other things. On the TOTAL side, I would like to thank Fabrice of course, but also Jérôme for allowing me to be part of this joint-research project in 2011. Thank you Antoine for being my mentor: thank you for pushing me into scientific and technical multitasking, thank you for encouraging me to present my results and to get trained when opportunities showed up. Thank you for training me on the ARCAM reactor, thank you for the many HF dips that I could not perform. Thank you for your investment when launching the PECVD Cluster Tool and for your help maintaining it. I'll stop here but just know that I feel lucky to have had you around.

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Rym a.k.a. “Sputtering-Reem” for the positive impact you’ve had on all Ph.D. students including me. It was nice learning a few words in Arabic here and there, between two reactor pumpings. Now, my notebook is full of declensions and verbal forms. Thank you Nada and Ludo: it is in your office that we found how to double my solar cell production instantly (do the same for CAL next time and you’ll become filthy rich). I would like to also thank all the newcomers: competent and fun people like Gilles a.k.a. “Jillz”, Sergej, Jara and Martin. I would also like to thank Pavel for healing my tongue, which I found to be corrupt with 20 years of junk-food. Now, I can boldly say that wine tastes better than sodas. More importantly, thank you for giving me a real taste for stripping down all my results down to a point where I can proudly and undoubtedly present them in front of a crowd of ferocious scientists. Speaking of which, I take the opportunity to thank Jean-Christophe, a.k.a. “Jeanjean” or “Jeanjean Cri” or “Jeanjean Cricri” or “JC”. While he obviously started on the wrong foot by putting his in my office and claiming that his desk should be there, it got much better (with time). Plasma processes and the Clusty reactor helped bringing some barriers down. More seriously, he was the best colleague ever and our workplace quickly became a very pleasant place to be. Conferences were always quite risky and usually involved some near-death experiences such as shooting, rafting and so on. Although scientific discussions often led to quite depressing conclusions, they allowed me to refine my results down to their very core and to present them in the best way. He really had a positive impact on the way I work and I’m sure many other scientists at LPICM could say the same. Thank you for your Bulgarian-nurse strategy. Although sometimes annoying, it is clearly efficient and this is how Clusty became very quickly user-friendly. Thank you for being so innovative and for repairing so many machines (that you weren’t even using sometimes!). I do not forget about our third coworker either, i.e., Ka-Hyun a.k.a. “James” with his incredible knowledge on a-Si:H and inimitable “so-British” style.

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Finally, even during a Ph.D. thesis, life goes on. This is why family is so important, even though they discovered my topic of research only during my defense. Having had you around was precious and knowing it has been helpful on many occasions.

Contents

Introduction

According to the *BP statistical Review of World Energy*[1] published in June 2014, the total consumption of primary energy reached 12,730.4 Mtoe[2] in 2013. This approximately equals 147,668 TWh, i.e., the equivalent of 16,857 1GW power plants running at full capacity throughout a whole year. The three dominant fossil fuels, i.e., oil, natural gas and coal are the main energy sources to meet this need. Indeed, they together represent 86.7 % of this value. 87 mln barils of crude oil, 9.23 bln m^3 of natural gas and 16.0 Mton of coal were produced daily in 2013 to cope with the growing demand. If we follow the estimation of the world documented reserves, at this production rate only 53, 55 and 153 years of oil natural gas and coal remain on the planet, respectively. Moreover, according to the *ALCEN foundation for the energy knowledge*, between 1971 and 2009, the world energy consumption experienced a 40 % increase. This evolution is due to the combination of a stable consumption by industrialized countries (usually also members of OCDE) with the increasing demand in energy by fast-growing newly-industrialized countries[3]. Today's energy consumption landscape brings complex challenges in the short term as well as in the longer term. The world demographic growth has an almost mechanical impact on energy consumption (+1.5% per year). Then, the increasing level of life in developed countries has direct consequences on the energy production per inhabitant (1.5% per year). However, this picture is far from frozen at this stage. Advances made in the energy production, distribution and consumption have managed to lower the energy consumption by 1% per year. Furthermore, political decisions surrounding energy production and consumption, which aim at acting against a predicted global warming in the world, will definitely shape tomorrow's landscape. The main leverages world governments intend to use are the optimization of energy consumption behaviors and efficiencies, as well as the development of renewable energies (hydroelectricity, wind power, biomass, geothermal, solar power…).

In 2010, the world production of renewable energies reached 11,392 GWh per day on average. This represents a very impressive 19.6% share of the electricity world production. Moreover, between 2000 and 2010, the electricity produced from renewable sources experienced a 43% growth. However, solar power represents only 91 GWh per day, which is a little less than 1% of the daily production of

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[1] http://www.bp.com/content/dam/bp/pdf/Energy-economics/statistical-review-2014/BP-statistical-review-of-world-energy-2014-full-report.pdf

[2] 1 toe represents the amount of energy released by burning one ton of crude oil. It approximately equals 42 GJ or 11.63 MWh. However, one has to take into account that different crude oils have different calorific values.

[3] China for example, has seen its energy consumption triple from 1990 to 2008. Its share in the world consumption went from 7.5% to 16.4% and the consumption per inhabitant in China is now equal to the consumption per inhabitant in the world. During the same period, the consumption in Africa increased by 50% but remains quite a small part of the total world consumption (5.7% for more than 15% of the world population).

renewable energies. Indeed, among these renewable energies, hydroelectricity plays the biggest role by providing 83% of the renewable energy produced, thanks to the recent developments in China and Brazil notably. Nevertheless, one should keep in mind that the use of solar power for electricity generation is quite recent. Moreover, between 2000 and 2010, solar power has been the fastest growing renewable energy with a spectacular average increase of 38% per year. The main contributor to this growth is solar photovoltaics (84 GWh per day). Photovoltaics allows for the direct transformation of the energy contained in a beam of light into electricity. This conversion is made possible through the photoelectric effect which was discovered in 1839 by Antoine and Edmond Becquerel and explained for the first time by Albert Einstein in 1905. In the meantime, in 1883, the first solid state photovoltaic cell was built out of selenium and reached a little less than 1% conversion efficiency[1]. The "switch" to silicon was made when Bell Labs managed to fabricate the first silicon solar cells which exhibited a more significant conversion efficiency exceeding 6%[2][3]. As a result, 90% of the PV market today is silicon-based. Indeed, silicon is an abundant earth element and cell efficiencies have been improved up to 25% on an industrial production line by the SunPower corporation in 2014[4]. Since the sun is an infinite source of energy – it provides 10,000 times the amount of energy that the humans currently consume – it has the potential to be used as a source of energy if efficiently converted, namely via PV systems. Electricity generation by solar cells remained quite expensive for many years in comparison with grid electricity. It is however becoming more and more competitive today, reaching prices as low as 0.10-0.20 €/kWh. We therefore have today a great opportunity to make solar power part of the world energy mix. The energy company TOTAL S.A. for example, is one of the six supermajor oil companies in the world with an oil and gas production of 2,299 kboe/day in 2013[4]. With nearly 99,000 employees in over 130 countries, it is however dedicated to rethink the energy mix of the future. In April 2011, Total bought 60% of the photovoltaic Silicon Valley company SunPower for US$1.38 billion. They now own approximately 66% of the company[5]. As a result, the world's biggest solar power plant is now under construction. It is known as the Solar Star Project (formerly Antelope Valley Solar Project) and represents a 579-megawatt solar installation. When completed, the Solar Star Project should deliver enough electricity to power the equivalent of approximately 255,000 homes[6]. One of the greatest challenges photovoltaics needs to address today in order to be more attractive on the energy market is, therefore, to increase the cell efficiencies while reducing its production costs. Silicon heterojunction solar cells are a good candidate to achieve this goal. Indeed, as we will see later, these combine the attractive features of requiring low-cost process steps, for example by using process temperatures below 200°C, and yielding very high efficiencies, namely 24.7% in 2014[5]. The generation of photocurrent by a SHJ was first demonstrated by *Fuhs et al.* in 1974[6], while the first solar device was fabricated in 1983 by *Hamakawa and coworkers*[7] using polycrystalline silicon and a-Si:H to create the so-called *Honeymoon cell*. In the meantime, the outstanding passivating properties of a-Si:H in its intrinsic (undoped) form was demonstrated by *Pankove et al.*[8] and Sanyo improved the SHJ structure by adding a thin intrinsic buffer

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[4] 1 boe=barrel of oil equivalent, i.e., the approximate energy released by burning one barrel (42 U.S. gallons or ~159 litres) of crude oil.

[5] http://investors.sunpower.com/

[6] http://us.sunpower.com/solar-star/about/

layer at the (p)a-Si:H/(n)c-Si interface, leading to the famous HiT structure[7][9]. It may be surprising however, for the reader to see the involvement of the TOTAL Company in the field of SHJ since the company produces solar panels made of silicon homojunction solar cells. In this Ph.D. thesis though, stress was not put on improving existing SHJ solar cells for direct industrial applications. SHJ solar cell performance highly relies on the quality of the interface between two materials: the crystalline silicon (c-Si) substrate and the hydrogenated amorphous silicon (a-Si:H) layer of opposite doping types deposited by PECVD. Hence, by studying SHJ solar cells one can actually study the passivating properties of a-Si:H for c-Si substrates. Results obtained through such a study can then be used to understand how the c-Si substrate interacts with its passivating layer. Therefore, passivation topics are of great interest for the TOTAL company and can perhaps lead to applications to homojunction solar cells using a low-thermal budget and low-cost a-Si:H instead of the usual SiO_2 and a-SiN_x:H materials that are deposited at much higher temperatures. As a matter of fact, Panasonic reported in 2014 a 25.6% solar cell by combining the SHJ concept with the Interdigitated Back-Contact or IBC architecture[10]. This shows well that records can be beaten by combining different technologies.

For these reasons, SHJ solar cells have been studied at LPICM since 2007. Jérôme Damon-Lacoste was the first Ph.D. student to tackle the topic of passivation of c-Si by a-Si:H deposited by PECVD at low-temperature. He bequeathed us with important insights on the a-Si:H/c-Si interface and developed the know-how on passivation at LPICM. His work resulted in the fabrication of a 17.0% champion SHJ solar cell on a 5x5 cm^2 p-type substrate[11]. In 2011, Martin Labrune continued this work by studying the passivation of flat n-type substrates using the same technique and the same reactor. His work resulted in the fabrication of a 17.2% champion SHJ solar cell on 2x2 cm^2 n-type substrate[12]. All of these results were obtained on flat 280-µm thick high-quality TOPSIL wafers. At this point, considering the high reflectance of a flat silicon substrate, i.e., ~37% and the high levels of passivation obtained under our conditions, i.e., high effective lifetimes above 10 ms and implied V_{OC}s close to 725 mV, the main path to higher efficiencies obviously had to go through the improvement of the device's optical properties. Indeed, as can be seen in Figure 1-1, by fostering light-trapping the reflectance can be lowered and the transmission of the light into the device bulk enhanced. Thanks to this, more photons can be absorbed by the c-Si substrate and, thus, more electron-hole pairs generated. As a result, we can potentially witness an improvement of the final short-circuit current (J_{SC}). It may sound easy at this stage: all we would have to do was swap the flat c-Si substrates for textured ones and fabricate higher-efficiency SHJ solar cells. The increase in J_{SC} however, and resulting increase in the final conversion efficiency are only possible if the introduction of a textured c-Si substrate does not induce new recombination processes and extra electron-hole pairs generated through light-trapping are not lost. Moreover, the fact that we are no longer dealing with a flat substrate implies that the deposition times must be adapted to fit the newly obtained micrometer-high random pyramid landscape.

The challenges arising when swapping flat c-Si wafer for textured ones were partly unveiled at the end of Martin Labrune's Ph.D. thesis in 2011 ([12] pp. 123-127). Textured monocrystalline c-Si wafers were provided by the CEA INES within the frame of the HETSI European project.

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[7] Heterojunction with Intrinsic Thin layer.

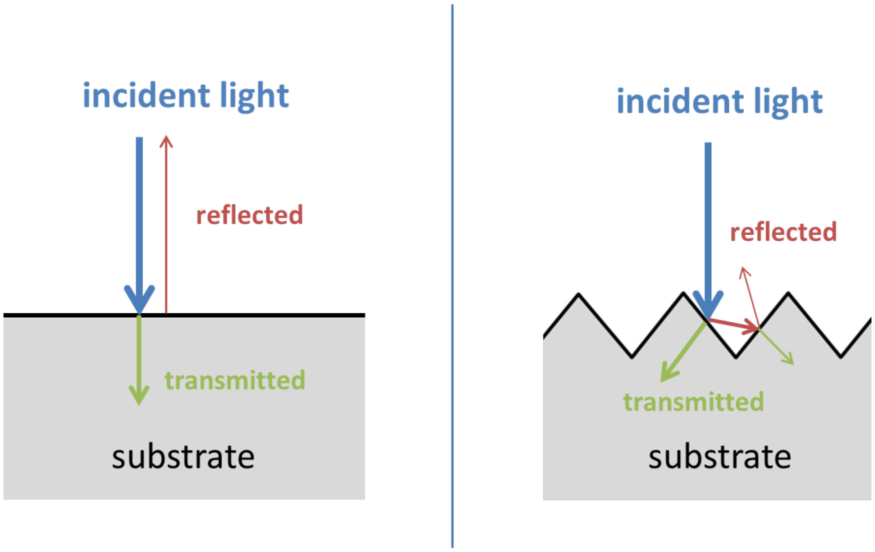

Figure 1-1 – Schematic representation of the impact of surface texturing on the substrate light-trapping properties: the part transmitted to the substrate (green beam) is enhanced while the reflected part (red beam) is reduced.

In this case, n-type substrates of various quality and surface states were tested, and they all led to quite low effective lifetimes, i.e., below $2{\cdot}10^{-5}$ s. Higher passivation levels could be reached by using textured multicrystalline substrates obtained within the framework of the French ANR project MULTIXEN, i.e., close to $3{\cdot}10^{-4}$ s. However, these remained one order of magnitude lower than what could be obtained on flat monocrystalline c-Si substrates (~3 ms). These low effective lifetimes induced significant drops in the finalized device V_{OC}s that was also observed by other labs[13] while, in our case, almost no increase in J_{SC} could be observed despite the lower reflection of our textured substrates. As a result, the efficiencies obtained on textured wafers were much lower than those obtained on their flat counterparts, i.e., between 9.4 and 12.8% instead of the usual 15-17%, thus leading to what could seem like a pointless effort. Since Martin Labrune's thesis mainly focused on the passivation and epitaxial growth on flat c-Si wafers, the study of textured c-Si substrates did not go any further. Therefore, many open questions remained unanswered:

- How can we optimize the light-trapping properties of our c-Si substrates and increase the J_{SC} of our finalized SHJ devices?
- What are the origins of the passivation drops observed at LPICM and by other labs while swapping flat wafers for textured ones?
- How can we compensate these passivation losses adequately to reach passivation levels comparable to what can be obtained on flat c-Si substrates?
- How can we increase the V_{OC} of our textured finalized SHJ solar cells towards reaching efficiencies greater than 19%?

These are the challenges that I was facing when I started this Ph.D. thesis. **Chapter I** is dedicated to the introduction to basic concepts of solar power and semiconductor physics: the solar spectrum, pn junction and diode equation, recombination mechanisms within the c-Si bulk… It also presents an important material: hydrogenated amorphous silicon (a-Si:H). Its main properties are unveiled, as well as its growth mechanism. This chapter also introduces the deposition technique used throughout this thesis. **Chapter II** introduces the concept of passivation of the c-Si surface: the a-Si:H/c-Si heterojunction the interface and band offsets. It also describes the (100) and the (111) c-Si crystallographic orientations are described as it is crucial to understand texturing mechanisms. Finally, the recombination mechanisms described earlier for the c-Si bulk are adapted to surface studies to yield the effective lifetime formalism. **Chapter III** brings us to the heart of my study. I imagined that the best way to understand the impact of the c-Si surface states on the effective lifetimes of our textured samples would be to go deeper into the micromachining of c-Si by studying the different ways to texture crystalline silicon. Not only did I want to choose the texturing technique, but I also wanted to monitor the texturing process from the industrial as-cut wafer down to its loading into the PECVD reactor. This is why this chapter starts with a literature study coupled with the experimental results that allowed me to choose the best texturing process according to very precise criteria. This part is followed by a thorough study that combines PCD measurements and HR-TEM/STEM analysis to understand the impact of texturation on a-Si:H growth and passivation. It results in a new paradigm for textured c-Si surface and leads us to use a very specific technique to improve the a-Si:H/c-Si interface. This technique is then applied to SHJ solar cells in **Chapter IV**. Indeed, passivation of textured c-Si wafers is greatly improved thereby. Making this improvement applicable to enhance the conversion efficiency of SHJ solar cells takes us a step further. The third chapter's conclusions are examined on SHJ solar cell precursors made out both of flat (111) and textured c-Si wafers. This study is first carried out with effective lifetime measurements whereupon SHJ solar cells are finalized and the improvements in terms of performance are analyzed. To underscore our observations, two types of texturing recipes are used for this study. This last chapter ends with a prospective but quite interesting study on the degradation of the passivation upon the deposition of TCO by PVD. It unveils the very particular role of the p-layer in the degradation of the a-Si:H/c-Si interface.

1 Basics of photovoltaics

1.1 Solar energy

The sun does emit light with a specific spectrum, and its intensity varies as a function of the wavelength. It will more or less match the radiation of a blackbody brought to a temperature of 5,800 K. However, as light travels through the atmosphere, it is attenuated by scattering and absorption. Thus, the characteristics of the sun's light impinging the Earth will vary depending on:

- scattering and absorption effects in the atmosphere
- atmosphere feature variation (thickness, chemical content...)
- data collecting latitudes
- earth's relative position with respect to the sun (seasons and time of the day)

These effects will modify the intensity, spectrum and angle of incidence of light reaching the Earth. Indeed, solar radiation has to travel through the molecules contained in the atmosphere. Ozone (O_3), carbon dioxide (CO_2) and water vapor (H_2O). These gases absorb photons of energy close to their molecule bond energy. As a result, most of the far IR light above 2 µm is absorbed by carbon dioxide and water vapor, whereas ozone absorbs the main part of the light below 300 nm. For these reasons, solar cells need to be designed not for a single wavelength but for the *energy distribution* that comes from the sun and manages to get through to the Earth.

1.1.1 Air Mass

Huge amounts of data have been collected by laboratories, governments, the PV industry and aerospace community to build extraterrestrial and terrestrial standards for the solar spectral irradiance distributions. These standards are defined using the notion of Air Mass. It is the path length of light travelling through the atmosphere normalized by the shortest possible path, i.e., when the sun is overhead (zenith angle equals to zero). As can be seen in Figure 1-1, d<D and an angle θ separates the two different paths.

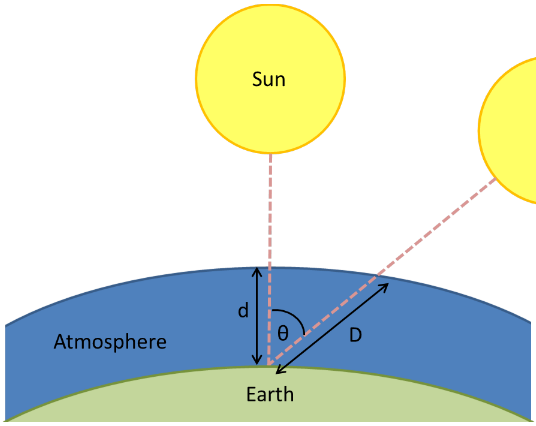

Figure 1-1 – Sunlight impiging the surface of the Earth at a zenith angle equal to 0 travels a distance d. When at an angle θ, the distance is D with d<D. We can define the so-called Air Mass by taking the inverse of the cosine of θ.

Air Mass can be expressed using the following relation:

$$AM = \frac{1}{\cos(\theta)} = \frac{d}{D} \qquad (1)$$

Thus, Air Mass 1 or AM1 corresponds to an angle θ equal to 0°, i.e., when the sun is overhead. The range AM1 to AM1.1 (θ=0° to θ=25°) is useful when testing solar cell performances in equatorial and tropical regions. Likewise, the AM2 (θ=60°) to AM3 (θ=70°) range is useful at high latitudes such as in northern Europe. Nevertheless, most of the biggest population hubs and, hence, their solar installation and industry lie in temperate latitudes, i.e., on either sides of the Earth's 38th parallels. As a result, AM1.5 representing the spectrum at mid-latitudes (θ=48.2°) has been commonly used as an international standard for the research community and the PV industry since the 1970s[14]. Moreover, it stands for a good average value of the yearly variations induced by season-related periodic angle changes[8]. Finally AM0 is used by the aerospace community and represents the spectral solar irradiance received from the sun before it crosses the atmosphere, i.e., before absorption effects become significant. It should be noted that silicon solar cells are not very sensitive to the parts of the spectrum lost in the atmosphere. The crystalline silicon bandgap makes silicon solar cells more efficient at AM1 than AM0 because they cannot make much use of the very high and very low energy radiation. The efficiency can be lower at AM0 but the total output power is still higher because there is still an additional and useful range of energy. Likewise, the shape of the spectrum does not significantly change with further increases in atmosphere thickness. As a result, cell efficiencies do not vary a lot for AM numbers above 1.

1.1.2 Solar spectrum

In Figure 1-2 are plotted the AM0 and AM1.5 spectra together with the crystalline silicon (c-Si) and hydrogenated amorphous silicon (a-Si:H) maximum irradiance fraction utilized. Here, we clearly see the losses induced by atmospheric absorption since AM0's irradiance is much higher than AM1.5, especially in the visible range.

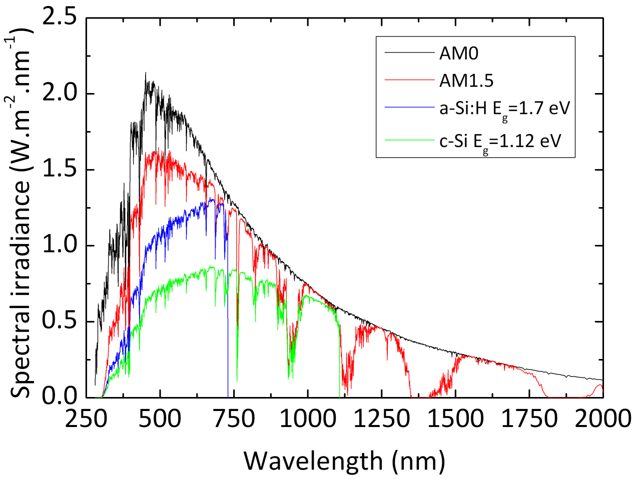

Figure 1-2 – AM0 and AM1.5 solar irradiance spectra together with the maximum utilized energies for a-Si:H and c-Si.

Moreover, we can see that c-Si and a-Si:H are both semiconductors which cannot take full advantage of the sun's irradiance since their maximum utilized irradiance fractions are lower than the AM1.5 spectrum. This is due to the impossibility to collect the so-called *hot electrons*.

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[8] Wintertime performance in temperate latitudes correspond to an AM coefficient greater than 2 at all times of the day, even for latitudes close to the subtropical limit, i.e., 38°.

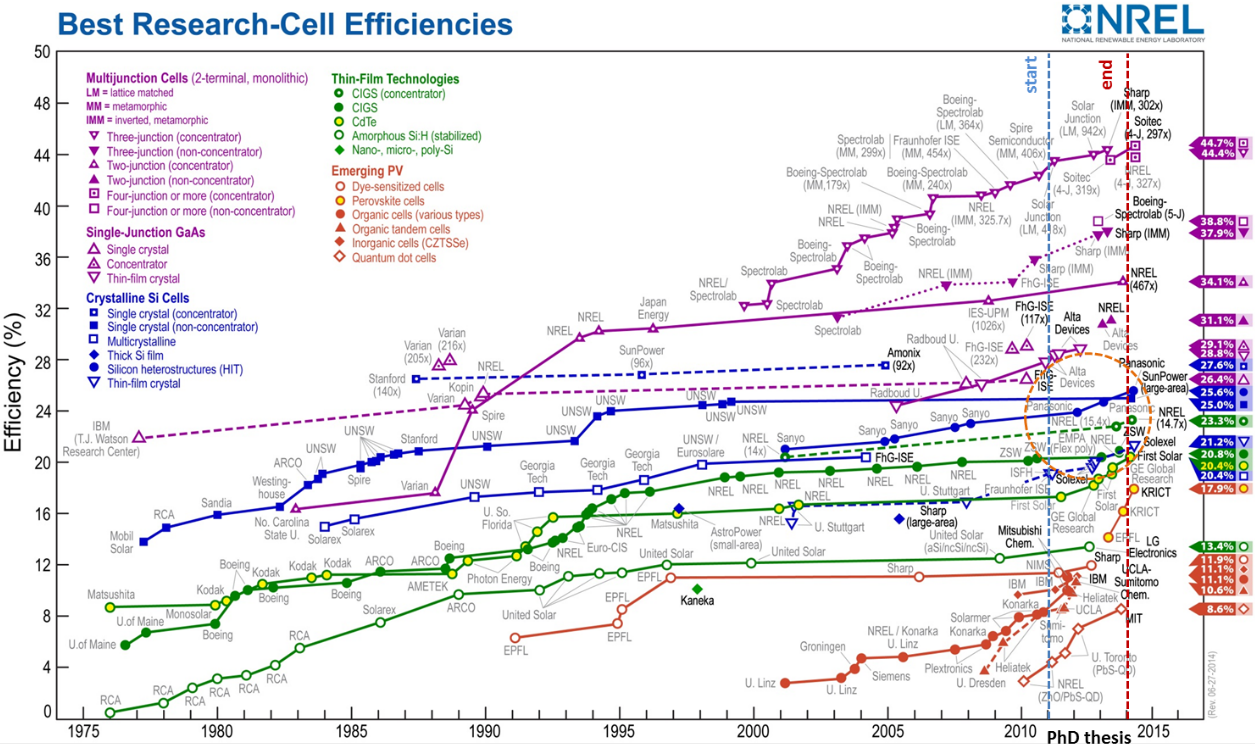


Figure 1-3 – Evolution of research-cell efficiencies in time for different PV technologies. The blue and red dashed vertical lines indicate the starting (2011) and ending (2014) years of my Ph.D. thesis, respectively.

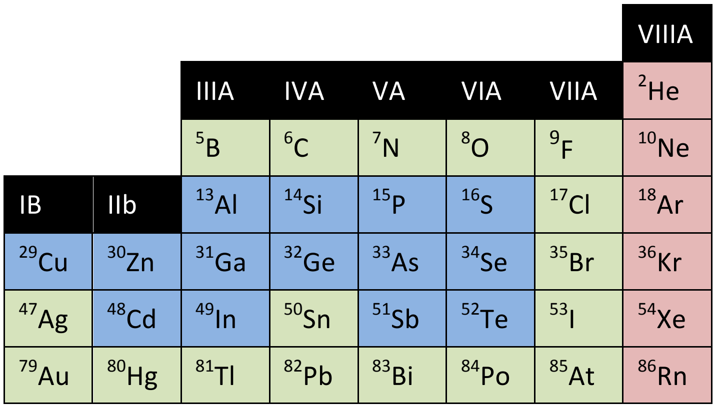
Indeed, when light of energy higher than the semiconductor energy bandgap E_g promotes an electron from the valence band to the conduction band, the electron is transferred to a state that is higher than the conduction band edge by δE. As a result, instead of just recombining by giving back an energy corresponding to E_g+δE, the electron will first release the extra energy δE via thermalization. As a result, the most efficient use of light occurs around the very value of E_g. All higher energy light is absorbed but δE will always be lost, resulting in the spectra shown in Figure 1-2 for c-Si and a-Si:H. One has also to keep in mind that c-Si has an energy bandgap of 1.12 eV (~1110 nm) and a-Si:H of roughly 1.7 eV (~730 nm). This means that these semiconductors will not be able to absorb any of the light of lower energy (higher wavelength). All light above 1110 nm is therefore intrinsically lost for c-Si-based solar cells. The same goes for a-Si:H with all sunlight beyond 730 nm. Increasing the semiconductor bandgap should therefore solve the thermalization-related losses whereas decreasing its value should widen the absorbed sun spectral range. An optimum has been suggested by Shockley and Queisser in 1961. It implies an “ideal” energy bandgap of 1.4 eV and would get us to conversion efficiencies of 30%[15]. To overcome this limit, multi-junction architectures have been proposed by other PV branches. These include several absorbers of various energy bandgaps which, in turn, allow for covering a wider range of the AM1.5 spectrum while keeping the aforementioned thermalization losses as low as possible. These are mainly made out of III-V materials but some include cheaper and simpler materials and alloys, made out of a-Si:H, microcrystalline silicon (μc-Si) or polymorphous silicon (pm-Si:H)[16]. Other new hybrid structures have been reported, combining organic and inorganic materials[17]. Namely, an innovative visible-light sensitizer made out of organometal halide perovskites[18] has allowed the KRICT [9]to reach an impressive conversion efficiency of 17.9% in 2013[19] and to catalyze research within this branch[20]. Figure 1-3 shows a chart that is very popular in the PV community. It shows the evolution of the best research-cell efficiencies with time since 1975 until 2014. It is taken from the NREL[10] website[11] and is commonly used to situate one's work context. From this curve we can see for all kinds of cell architecture, their history and latest efficiency records. In particular, we can situate the context in which this Ph.D. work was carried out between 2011 and 2014 (blue and red dashed lines). Sanyo was the record holder at that time[12] for the best silicon heterojunction solar cell with an efficiency of 23%[21]. However, in three years, advances have been made in this particular field, leading to the impressive 24.7% record efficiency in 2014 by the same company (now owned by Panasonic)[5].

1.2 Semiconductor physics applied to solar devices

1.2.1 Basics of semiconductor physics

1.2.1.a Semiconductor materials

A semiconductor is a material with specific conductivity properties. Indeed, they can neither be completely considered as conductors nor as insulators. They have enough electrons to fill their valence bonds but no free electrons to make them conductive.



							VIIIA
		IIIA	IVA	VA	VIA	VIIA	^{2}He
		^{5}B	^{6}C	^{7}N	^{8}O	^{9}F	^{10}Ne
IB	IIb	^{13}Al	^{14}Si	^{15}P	^{16}S	^{17}Cl	^{18}Ar
^{29}Cu	^{30}Zn	^{31}Ga	^{32}Ge	^{33}As	^{34}Se	^{35}Br	^{36}Kr
^{47}Ag	^{48}Cd	^{49}In	^{50}Sn	^{51}Sb	^{52}Te	^{53}I	^{54}Xe
^{79}Au	^{80}Hg	^{81}Tl	^{82}Pb	^{83}Bi	^{84}Po	^{85}At	^{86}Rn

Table 1-1 – Selected part of the periodic table of elements. The blue portion shows the most common semiconductors. They can either be intrinsically semiconducting or their combination can result in useful semiconductor materials.

As a result, they are insulating when no energy is provided to their system but can become conductive otherwise, by raising the temperature, applying an electric field or under light excitation for example. They can either come from the column IV of the periodic table or from a combination of two different

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[9] Korean Research Institute of Chemical Technology

[10] National Renewable Energy Laboratory

[11] www.nrel.gov

[12] In December 2009, Sanyo became a subsidiary of Panasonic when a $4.5 bln acquisition of a 50.2% stake was completed. In July 2010, Panasonic announced that they would acquire the remaining shares of Sanyo. More information on http://panasonic.net/sanyo/news/2012/12/

columns (III-V or II-VI), as shown in Table 1-1. For example, Si or Ge are intrinsically semiconductor materials whereas compounds such as GaAs (a binary compound), InGaAs (a ternary compound) or AlInGaP (a quarternary compound) can result in the creation of useful semiconductors.Silicon exhibits an electronic structure of $3s^23p^2$. As can be seen in Figure 1-4a), each silicon atom has 4 valence electrons on their external orbital. Therefore, each Si atom can share an electron with its neighboring atom to form chemical bonds. This results in the crystalline lattice described in Figure 1-4b) where all the individual atoms are linked together by covalent bonds. The electrons in these covalent bonds are held in place by these bonds and hence, they are localized and must stay in the region surrounding the atom. These electrons cannot move or jump to a higher energy level and therefore are not considered free. Thus, they cannot participate in conduction at absolute zero, i.e., when no energy is provided to the system. The minimum energy required is called the *energy bandgap*. It is also called the *forbidden* energy bandgap since any lower energy value does not allow such a transfer from a lower state of energy to a higher state of energy to take place, i.e., there is no intermediate state. When an electron leaves a lower state of energy to a higher one, it leaves an empty space behind. A negative charge is therefore missing at this level and can be considered a positive charge. This introduces the very important notion of *holes*. In solar cells, free electrons and holes as well as their number and energy are crucial for their operation.

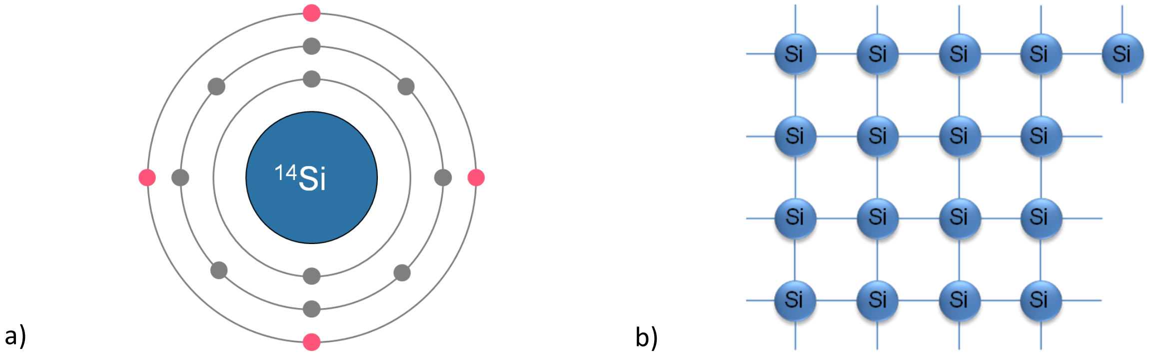

Figure 1-4 – Core shell structure of silicon (a). Pink circles represent valence electrons as opposed to grey circles which are closer to the nucleus. Schematic representation of covalent bonds in a silicon crystal lattice (b). Each line represents two electrons that are shared to form a covalent bond.

1.2.1.b Photon energy and bandgap

When a photon hits the surface of a semiconductor, it can be reflected, absorbed or transmitted. Obviously, reflection and transmission are here considered losses since in solar devices we need to absorb the photons in order to transform them into an electrical current. To determine if light will be efficiently utilized by the semiconductor one needs to consider two parameters: the photon energy and the semiconductor bandgap. When $E_{ph}<E_g$, the photon is not absorbed. In some cases where the semiconducting material contains some localized states within the bandgap, the photon can be absorbed, otherwise not. When $E_{ph}>E_g$, the photon is absorbed by the semiconductor but the excess energy δE with respect to E_g will be lost via thermalization, as mentioned in 1.1.2. When $E_{ph}=E_g$, we find ourselves in the most efficient case of absorption since the energy is completely used for the generation of an electron-hole pair. Now, for $E_{ph}\geq E_g$ the absorption coefficient is not constant but strongly dependent on E_{ph}. Indeed, a photon will be absorbed depending on its ability to interact with an electron. With increasing E_{ph} the absorption will become more efficient, but not the photon energy utilization.

One can simply express the absorption coefficient α by:

$$\alpha = \frac{4\pi k}{\lambda} \tag{2}$$

where λ is the wavelength in nm[13] and k the extinction coefficient. This in turn will get us to the absorption depth 1/α or α^{-1}. It is a useful parameter as it gives the distance into the material at which the light intensity drops by a factor 1/e. Indeed, as can be seen in Figure 1-5, when E_{ph} is high or λ short (UV/blue) α will be large and, therefore, the light will be absorbed close to the semiconductor surface. Likewise, when E_{ph} is low or λ long (red/IR) α will be small and, therefore, the light will go deeper inside the material.

Figure 1-5 – Schematic representation of the evolution of the absorption depths as a function of the incident energy photon E_{ph}.

Figure 1-6 shows the absorption coefficient of c-Si (taken from [22]) and a-Si:H (taken from [23]). The data presented show that crystalline silicon "cuts" right after crossing 1,100 nm, which corresponds to its energy bandgap. Likewise, right above 700 nm light absorption inside a-Si:H vanishes. Again, this corresponds approximately to an energy bandgap of 1.7 eV, which is typical for intrinsic a-Si:H.

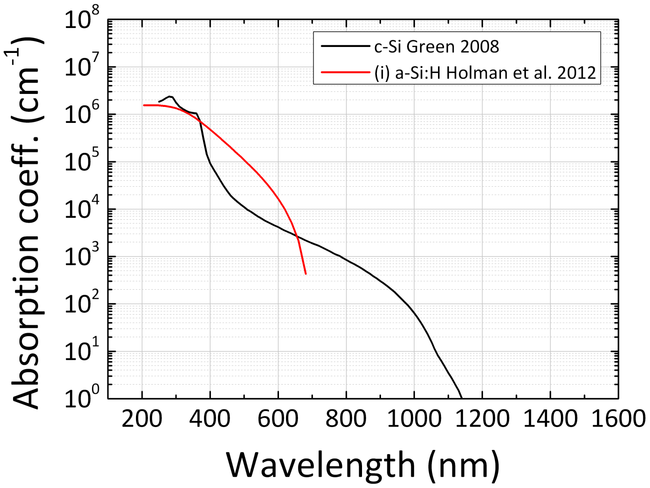

Figure 1-6 – Absorption coefficient *α* of c-Si and a-Si:H as a function of the wavelength at 300K.

This is crucial for solar cell performance analyses since this will determine where the charge carriers are generated and, hence, their recombination probability. As a result, their extraction efficiency as a useful current will be impacted. With zero reflection, the intensity of the light after impinging the semiconductor surface will depend exponentially on α through the relation:

$$I = I_0 e^{-\alpha x} \tag{3}$$

---

[13] To get the result in cm^{-1}, one needs multiply k by 10^7.

Where α is in cm^{-1}, x is the depth at which the intensity is calculated and I_0 is the incident light intensity before it hits the semiconductor surface. Thanks to this, we can calculate the generation rate of electron-hole pairs G:

$$G = \alpha N_0 e^{-\alpha x} \tag{4}$$

where N_0 is the photon flux hitting the surface in photons·cm^{-2}·s^{-1}. Indeed, if we assume that 1 photon is responsible for the creation of 1 electron-hole pair, then the change of intensity can be directly used to express G. Thus, deriving Eq. 3 will result in Eq. 4, which tells us that the generation is at its highest rate close to the semiconductor surface whilst decreasing exponentially further away.

1.2.1.c Doped semiconductors

A significant feature of semiconductors is their ability to be doped. Indeed, by inserting specific atoms called *dopants* inside their crystal lattice an excess (n-type doping) or a deficiency (p-type) of electrons can be created, leading to a much enhanced conductivity of the material[14]. These tuned semiconductors are called *extrinsic* or *doped*. The conductivity will now depend on the amount of dopant inserted inside their lattices. A 1cm^3 sample of silicon contains approximately $5 \cdot 10^{22}$ atoms. While in metals each atom provides at least one free electron for conductivity, here the silicon atoms will provide approximately 10^{10} free electron and 10^{10} free holes. The addition of very small amounts of a doping impurity such as phosphorus will enhance the conductivity of silicon greatly by a factor of 10,000. This is made possible because it simply adds extra electrons, which become available for conduction. When adding extra electrons (n-type doping) or extra holes (p-type doping) to the semiconductor, we introduce impurities to the crystal lattice in the form of atoms that are foreign to the original material. This introduces states within the forbidden bandgap. If these are localized near the midgap, i.e., close to the Fermi level, they do not make the charge carrier transfer from the valence band to the conduction band any easier. However, if these states are closer to the valence and conduction band edges, they make the jump of the carriers from the doping states possible. Indeed, with n-doping will arise a donor level called E_D whereas p-type doping will create an acceptor level called E_A. These two types of doping are crucial to solar cells since they are actually built with a combination of both. To go further into details, one is referred to textbooks written by Stephen Fonash[24] or Jenny Nelson[25]. A few parameters will nevertheless be expressed in the following sections as they are key to solar cell operations.

1.2.1.d Semiconductors at thermal equilibrium

At thermal equilibrium, the distribution function of the electrons at an energy E is defined by Fermi-Dirac statistics. It states that the number of electrons present within the conduction band is equal to:

$$n = \int f_{F-D}(E) \rho_C(E) dE \tag{5}$$

where f_{F-D} represents the occupation probability and ρ_C the number of possible states for the electrons.

---

[14] In fact, conductivity is the most widely spread parameter in physics. Glass has a conductivity close to 10^{-11}-10^{-15} S/m whereas silver yields the very high conductivity value of $6.30 \cdot 10^{7}$ S/m.

As a result we have:

$$n = N_C \exp\left(-\frac{E_C - E_F}{kT}\right) \tag{6}$$

where N_C is the effective density of state within the conduction band[15]. The same statistics allow estimating also the number of holes present within the valence band through the relation:

$$p = \int (1 - f_{F-D}(E))\rho_V(E)dE \tag{7}$$

Where 1- f_{F-D} represents the hole occupancy probability[16] and ρ_V the number of possible states for the holes. As a result we have:

$$p = N_V \exp\left(\frac{E_V - E_F}{kT}\right) \tag{8}$$

where N_V is the effective density of state within the valence band[17]. A condition arises for the product of Eq. 6 by Eq. 8:

$$np = N_C N_V \exp\left(-\frac{E_C - E_F}{kT}\right) = N_C N_V \exp\left(-\frac{E_g}{kT}\right) = n_i^2 \tag{9}$$

Where E_g=E_c-E_v and n_i is the intrinsic carrier concentration[18]. Note that this relation is always true as long as there is a Fermi level, i.e., as long as there is thermal equilibrium. This is no longer the case when we introduce a perturbation to the system. As we will be dealing with solar cells, it is of great importance to study the behavior of semiconductors under the most common perturbation they will be exposed to: light.

1.2.1.e Semiconductors under light excitation

When a semiconductor is exposed to a perturbation such as a pulse of light, the electron populations in the valence and conduction band change. Because their relaxation time in each band is much lower than their relaxation time across the bandgap, they all stabilize momentarily in a quasi-thermal equilibrium within their respective bands. The Fermi level cannot be used anymore to define the electron occupancy. However, we can define a so-called *quasi-Fermi level for the conduction band* E_{Fn} and a *quasi-Fermi level for the valence band* E_{Fp}. As a result, the density of electron from Eq. 6 becomes:

$$n_{light} = N_C \exp\left(-\frac{E_C - E_{Fn}}{kT}\right) \tag{10}$$

---

[15] Given a state density effective mass in the conduction band m_C=1.18, N_C=3.11·10^{19} cm^{-3} for crystalline silicon.

[16] The sum of the electron and hole occupancy probabilities must be equal to 1.

[17] Given a state density effective mass in the conduction band m_V=0.81, N_V=1.7·10^{19} cm^{-3} for crystalline silicon.

[18] For crystalline silicon, Sproul and Green[26]have determined the value n_i=10^{10} cm^{-3}.

whereas the density of holes from Eq. 8 becomes:

$$p_{light} = N_V \exp\left(\frac{E_V - E_{Fp}}{kT}\right) \tag{11}$$

In consequence, the product given in Eq. 9 becomes:

$$n_{light} p_{light} = n_i^{\,2} \exp\left(\frac{E_{Fn} - E_{Fp}}{kT}\right) \tag{12}$$

where $\mu = E_{Fn} - E_{Fp}$ is the quasi Fermi level splitting. This value is important for solar cell operations since it will define the upper bound of their V_{OC} value.

1.2.2 PN junction

The pn junction is the primary brick of all solar cell devices. In fact, it is the core of all rectifying devices such as diodes. In an electroluminescent diode for example, electrical current flows to produce light. In solar cell devices, the opposite event takes place. Sunlight hits the solar cell device (made of a pn junction in its core) and produces electrical current. We will see in the coming section how a pn junction transforms a photon of a given energy into an electrical current.

1.2.2.a Formation of a pn junction

A pn junction is created whenever joining two semiconductors of opposite doping. This can be done either by depositing a doped layer on a substrate or by diffusing dopants in a substrate that is already doped with a dopant of opposite sign. Whenever doing so, an n-type region with a high electron concentration is joined with a p-type region which has a high hole concentration.

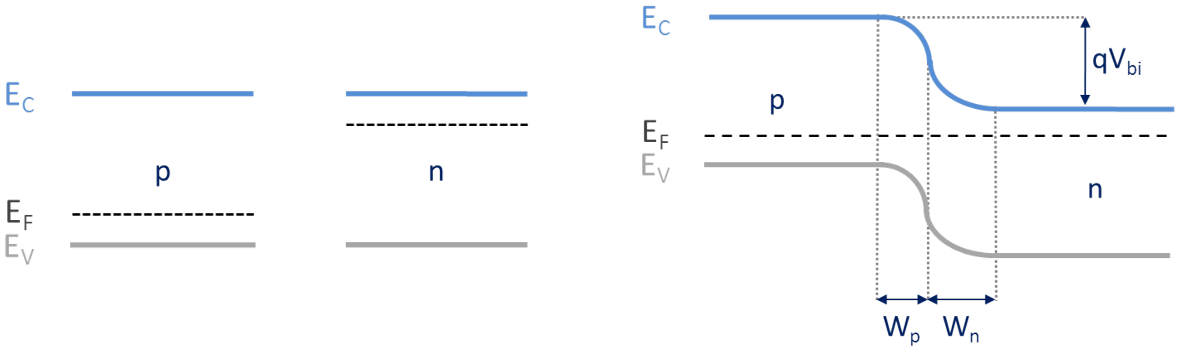

Figure 1-7 – p- and n-type semiconductors before(left) and after (right) joining them to form a pn homojunction.

Therefore, the resulting semiconductor material is inhomogeneous in terms of free carrier concentration. In consequence, free charges start to move in order to reach homogeneity, resulting in a diffusion current. Of course, during this process, n-type dopants, i.e., phosphorus atoms, lose their free electron while p-type dopants, i.e., boron atoms, lose their extra hole. Because their initial number of protons is 15 and 5, for phosphorus and boron respectively, their ionized states will lead to a net charge of opposite sign left behind. Indeed these charges are bound to the crystalline lattice and unable to move. As a result, positive ion cores are exposed on the n side whereas on the p side, negative ion cores appear. An electric field will then arise and counter diffusion. Equilibrium is then reached when there is a current that is equal and opposite to diffusion current. This can be expressed by saying that the overall electronic current is equal to zero or that:

$$n\mu_e\vec{\varepsilon} = -D_e\vec{\nabla}n \tag{13}$$

In other words, electrons simply do not move anymore, because of the electric field generated by the opposite signs now present on either sides of the interface between the n-doped and p-doped semiconductors. Therefore, there is an electrostatic potential such that:

$$\nabla^2\phi(x) = -\frac{\rho(x)}{\varepsilon_0\varepsilon_r} \tag{14}$$

This potential is called the *built-in potential* and is usually noted $V_{bi.}$ This all happens at the interface between the two semiconductors. This region is called the *space-charge region* or *depletion region* since this part of the junction is depleted of free carriers. Its width is equal to the sum of the two components present on each side of the interface W_p and W_n. Their respective width depends on the doping levels on both sides. One should keep in mind that the higher the doping, the thinner the width since with a higher dopant concentration, the same fixed charge can be created on a much shorter length.

1.2.2.b Diffusion and drift

Considering Ohm's law, in presence of an electric field one can write the electronic current density as:

$$\vec{J}_e = ne\mu_e\vec{\varepsilon} \tag{15}$$

where n is the electron density, e is the electronic charge and μ_e the electron mobility. This current which relates to the presence of an electric field is called *drift current*. Likewise, if the material is heterogeneous such that the free electron concentration varies with the position, a *diffusion current* arises which will tend to homogenize the semiconductor:

$$\vec{J}_{d,e} = eD_e\vec{\nabla}n \tag{16}$$

where D_e is the electron diffusion coefficient. Eq. 15 and 16 lead to the overall expression of the electronic current density:

$$\vec{J}_e = ne\mu_e\vec{\varepsilon} + eD_e\vec{\nabla}n \tag{17}$$

The same expression can be written for the holes by considering their density p, mobility μ_h and diffusion coefficient D_h:

$$\vec{J}_h = pe\mu_h\vec{\varepsilon} - eD_h\vec{\nabla}p \tag{18}$$

These are the two most important equations in a pn junction as they determine the movements of all charge carriers through the expression of the overall current density:

$$\vec{J} = \vec{J}_e + \vec{J}_h \tag{19}$$

1.2.2.c Diode equations

In the dark, the current flowing from a diode can be expressed through *Shockley*'s law:

$$J(V) = J_0\left[\exp(\frac{qV}{nkT}) - 1\right] \tag{20}$$

where J_0 is the diode saturation current and n the ideality factor. In the case of a perfect diode, n should be equal to 1. Under light excitation, a photogeneration term J_{ph} is added to Eq. 20. However, under illumination one has to take into account parasitic effects in the form of resistances. As a result, a series (R_S) and shunt (R_{Sh}) resistances are also introduced, resulting in the following equation:

$$J(V) = J_0\left[\exp(\frac{q(V - R_S J)}{nkT}) - 1\right] + \frac{V - R_S J}{R_{Sh}} - J_{ph} \tag{21}$$

JV characteristics are the most powerful tool to assess solar cell performances. It indeed allows for the determining the ideality of the diode in the dark (parameters J_0 and n) as well as the main cell parameters under illumination (V_{OC}, J_{SC} and FF). When extracted under our standard conditions (AM1.5, 25°C), these parameters allow for the estimation of the final conversion efficiency of the solar cell. To perform such measurements during the thesis, an Oriel Sol3A Class AAA solar simulator fabricated by Newport was used. The model we had was a 94083A, which allowed us to carry out measurements under 1 Sun with certified 8"x8" homogeneity. Moreover, a temperature-controlled chuck with a water-cooled hot side, produced by Bentham, delivered a temperature stability of ±1°C during our measurements. Although they can be represented in linear scale, dark JV characteristics are usually plotted using the logarithm of the absolute value of the current. This yields the typical curve shown in Figure 1-8a) in the -1 to 1 V bias range. By linearizing Eq. 20, one obtains:

$$\log J(V) = \log J_0 + \log\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{22}$$

which can be approximated by:

$$\log J(V) \approx \log J_0 + \frac{qV}{nkT}\log e \tag{23}$$

Eq. 23 is now of the form y=Ax+B with:

$$\begin{cases} A = \dfrac{q \log e}{nkT} \\ B = \log J_0 \end{cases} \tag{24}$$

Considering kT=25 meV at RT, A≈17.34/n and that $10^{\log(a)}=a$, we finally have our expressions for the ideality factor n and the dark saturation current J_0:

$$\begin{cases} n \approx \dfrac{17.36}{A} \\ J_0 = 10^B \end{cases} \tag{25}$$

Therefore, by taking the slope A in the linear part of the dark JV characteristics (0.4<V<0.6 V bias range), we find the intercept B. In this case, A=13.8±0.03 while B=-7.78±0.01.

This yields for n and J_0:

$$\begin{cases} n = 1.26 \\ J_0 = 2.31 \cdot 10^{-8}\, mA/cm^2 \end{cases} \tag{26}$$

A typical JV characteristic under illumination is shown in Figure 1-8b). Three points are crucial for the determination of the solar cell performances:

- the point of open-circuit voltage, where no current flows: V_{OC},
- the point of short-circuit, where V=0: J_{SC},
- the point where the product of the voltage times the current reaches its maximum called the *maximum power point* or MPP.

The MPP determines a parameter called fill factor or FF. It is defined as the ratio:

$$FF = \frac{J_{MPP} \cdot V_{MPP}}{J_{sc} \cdot V_{oc}} \tag{27}$$

As can be seen on the curve, two rectangles are drawn. One represents the area determined by the $J_{MPP} \cdot V_{MPP}$ product (dark grey) and the other one by the $J_{SC} \cdot V_{OC}$ product (light grey). Their ratio yields an FF value of 78.7%. The series resistance (R_S) accounts for all the resistive losses that can occur in the finalized device, from a resistive material inside up to the resistive losses induced by the metal contacts. For these reasons, we seek to reduce R_S as much as possible. Contrariwise, the shunt resistance (R_{Sh}) accounts for shunt losses that can occur because of undesirable conduction paths at the pn junction interface for example. For this reason, R_{Sh} should be as high as possible to keep the blocking properties of the diode. These resistances can be estimated by taking the inverse of the slope at V_{OC} and J_{SC}, respectively.

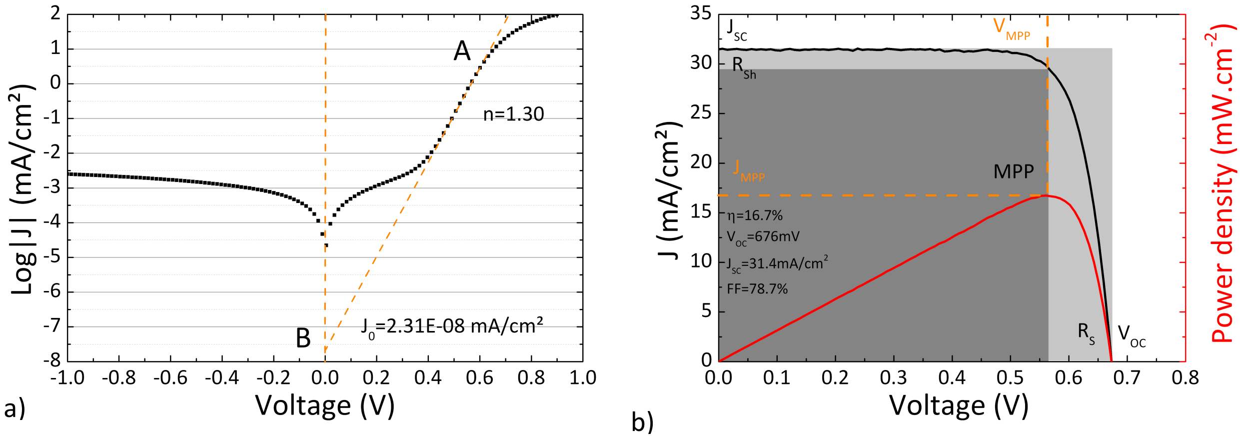

Figure 1-8 – Typical JV characteristics a) in the dark and b) under illumination and the main parameters that can be extracted.

Thanks to the parameters extracted from the JV characteristics taken under illumination, one can estimate the conversion efficiency of the device trough the following relation:

$$\eta = \frac{J_{sc} \cdot V_{oc} \cdot FF}{P_{inc}} \tag{28}$$

where P_{inc} is the power of the incident light.

1.3 Silicon for PV applications

Crystalline silicon is the base of our cell architecture. It is an indirect-bandgap semiconductor with a diamond crystal structure. Its bandgap is 1.12 eV at 300 K. Because it is indirect, absorption is made more difficult than in the case of a direct bandgap materials such as a-Si:H. As a result, the thickness required to fabricate a device with c-Si as the absorber is quite large, i.e., of the order of hundreds of microns (from 98 µm up to 300 µm). For comparison, amorphous pin solar cells made with a-Si:H solely usually reach total thicknesses of the order of hundreds of nanometers. Figure 1-9 shows a crystalline silicon unit cell. As can be seen, the silicon atoms are arranged according to a diamond structure. This particular feature will lead to specific etching properties and very useful orientation selectivity. Table 1-2 displays various parameters for crystalline silicon. On these properties will depend the final performances of the solar device fabricated with this material. Indeed, the density of state, mobility and diffusion will determine how many carriers can be generated, how fast and how far they can travel before being subject to recombination. This will in turn determine the lifetime of the photogenerated carriers inside the device, i.e., how long they actually "live" inside the device. The longer they remain, the higher the chances we will have to collect them as a current. This, among other things, will determine the final conversion efficiency of the solar cell and we want it to be as high as possible.

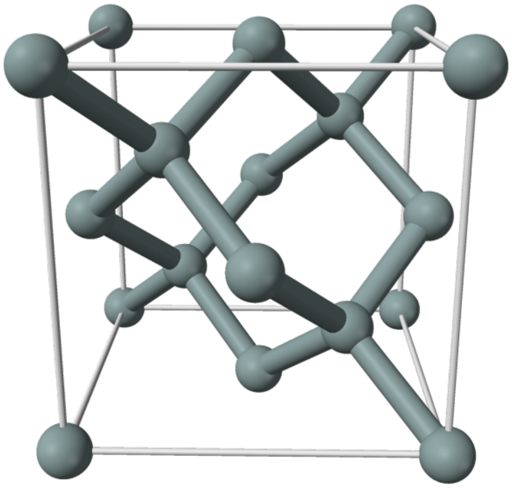

Figure 1-9 – Crystalline silicon unit cell showing a diamond structure arrangement.

Effective density of states N_c	2.8×10^{19} cm^{-3}
Effective density of states N_v	1.04×10^{19} cm^{-3}
Energy bandgap E_g	1.12 eV
Intrinsic carrier concentration	$1\cdot10^{10}$ cm^{-3}
Electron mobility μ_e	≈ 1400 cm^2/(V s)
Hole mobility μ_h	≈ 450 cm^2/(V s)
Electron diffusion coefficient D_e	≈ 36 cm^2/s
Hole diffusion coefficient D_h	≈ 12 cm^2/s
Electron diffusion length $L_{diff\text{-}e}$	1800 µm
Hole diffusion length $L_{diff\text{-}h}$	1050 µm

Table 1-2 – Selected parameters describing the band structure and the electrical properties of crystalline silicon at 300K.

In this section, we will describe the different recombination processes that can occur in a semiconductor material such as crystalline silicon. Indeed, understanding them will help us pushing the photogenerated carrier lifetime limits in order to reach higher conversion efficiencies of finalized solar cell devices.

1.3.1 Bulk recombination and lifetime

At temperature above absolute zero, electron-hole pairs are constantly generated. These carriers eventually recombine through various mechanisms. In the case of solar cells, the electron-hole pairs are generated by an external light excitation. If we assume this excitation to have a constant intensity and steady-state conditions, we witness a situation where the excess carrier density is non-zero. Indeed, there is an excess carrier density, which can be defined through the density of carriers under thermodynamic equilibrium n_0 and their recombination rate U in cm^{-3}·s^{-1}:

$$U = \frac{n - n_0}{\tau} = \frac{\Delta n}{\tau} \tag{29}$$

where τ is the characteristic recombination lifetime of our recombination process and $\Delta n = n - n_0$ the excess carrier density in the c-Si bulk. Under equilibrium though, the thermal generation rate matches the recombination rate and the excess carrier density is equal to zero. Since most of the high-efficiency solar cells work closer to mid- or high-injection levels, we will consider that both excess carrier densities are equal, therefore $\Delta n = \Delta p$. As stated before, carrier recombination in c-Si can occur through different mechanisms, namely three which are independent: radiative recombination, Auger recombination and the so-called SRH (stands for Shockley-Read Hall) recombination n process. The total recombination rate within the c-Si bulk will therefore be a combination of the three recombination rates U_{rad}, U_{Aug} and U_{SRH} as follows:

$$U = U_{rad} + U_{Aug} + U_{SRH} = \frac{\Delta n}{\tau_{rad}} + \frac{\Delta n}{\tau_{Aug}} + \frac{\Delta n}{\tau_{SRH}} = \frac{\Delta n}{\tau_{bulk}} \tag{30}$$

where τ_{rad}, τ_{Aug} and τ_{SRH} are the recombination lifetimes related to their respective recombination rates. These three mechanisms will be described to understand how the overall recombination rate can be influenced.

1.3.1.a Radiative recombination: relaxation by photon emission

Radiative recombination is an unavoidable phenomenon taking place within the c-Si bulk. In this recombination process, the excess of energy confined within crystalline silicon is expelled in the form of a photon when two carriers of opposite charges (an electron and a hole) neutralize each other from the conduction and the valence band, respectively.

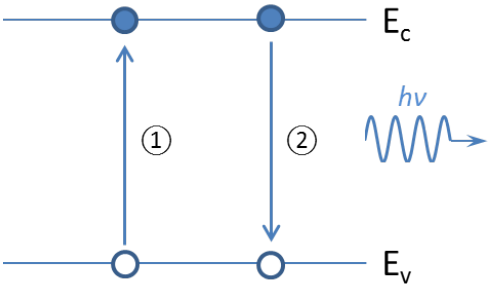

Figure 1-10 — Radiative recombination paths in a semiconductor: (1) hole from the VB recombining with an electron in the CB; (2) electron from the CB recombining with a hole in the VB. Both mechanisms result in the emission of a photon with an energy of hν.

Because of this, the energy of the emitted photon is approximately equal to the energy bandgap of c-Si. If the energy is higher than E_g, the difference is lost by thermalization, until the carriers reach the extremum of their respective band (minimum of the conduction band for an electron or CBM, maximum of the valence band for a hole or VBM).

The recombination rate is proportional to the density of both carriers since one of each is needed in this process[27]:

$$U_{rad} = B_{rad} \cdot \Delta n \cdot \Delta p \tag{31}$$

$$U_{rad} = B_{rad} \cdot \Delta n \cdot (N_D + \Delta n) \tag{32}$$

where B_{rad} is a temperature-dependent parameter and N_D is the donor atom density. Since c-Si is an indirect bandgap semiconductor, one should keep in mind that it requires the participation of at least one phonon to achieve momentum and energy conservation at the same time. This means that four particles should at least be involved instead of just three (if we take into account the electron-hole pair, the incident photon and the latter mentioned phonon) to make radiative recombination possible. This leads to a negligible rate U_{rad} compared to the other recombination processes. Indeed, in c-Si $B_{rad}=1\cdot 10^{-14}$ cm^3/s [28]. Nevertheless, τ_{rad} can be expressed as:

$$\tau_{rad} = \frac{1}{B_{rad} \cdot (N_D + \Delta n)} \tag{33}$$

At this point, we take a moment to notice that at low-injection, i.e., when $\Delta n \ll N_D$, τ_{rad} is constant and limited by $1/Brad \cdot N_D$. At high-injection levels on the other hand, i.e., when $\Delta n \gg N_D$, the minority carrier density dominates τ_{rad} by keeping it proportional to $1/\Delta n$.

1.3.1.b Band-to-band Auger recombination: energy transfer to a charge carrier

Band-to-band Auger recombination is another recombination mechanism we cannot avoid. It is an intrinsic process within the c-Si bulk and it cannot be skirted.

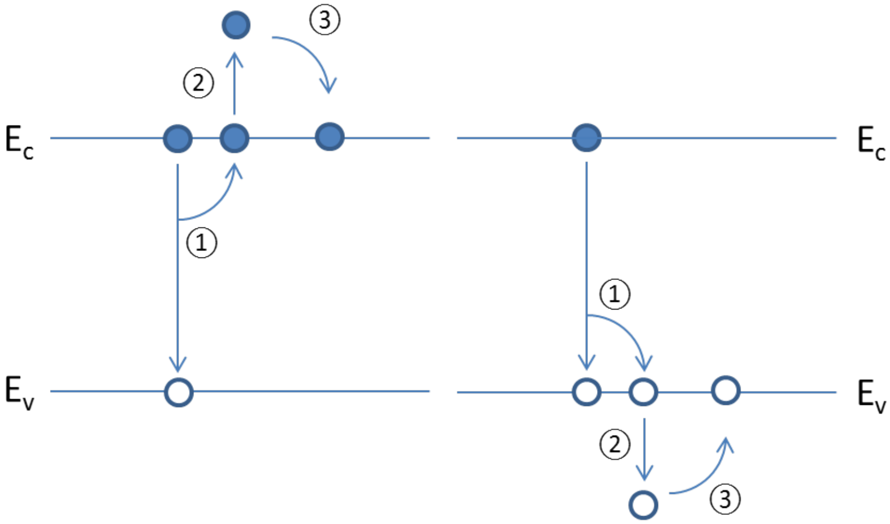

Figure 1-11 — Auger recombination mechanism for electrons (left) and holes (right).

As shown in Figure 1-11, the excess energy generated by the band-to-band recombination of an electron-hole pair is communicated to a third charge carrier. It can either be an electron in the conduction band as well as a hole in the valence band. There is no photon emission here since all the energy is transferred to the latter mentioned third carrier. This extra energy will eventually be lost when this third carrier moves from its excited state to the band edge (minimum of the conduction or maximum of the valence band). If we assume that there is no interaction between the three carriers, the recombination rate will be proportional to the carrier densities involved herein. Since the recombination can occur via either an electron or a hole, two cases are to be considered: a recombination rate $U_{eh\text{-}e}$ and a recombination rate $U_{eh\text{-}h}$. Therefore, we have:

$$U_{eh-e} = C_n \cdot (n^2 p - n_0^{\;2} p_0) \tag{34}$$

$$U_{eh-h} = C_p \cdot (np^2 - n_0 p_0^{\;2}) \tag{35}$$

where C_n and C_p are the Auger coefficients for electrons and holes respectively. U_{Aug} can then be expressed as the sum of these two processes:

$$U_{Aug} = U_{eh-e} + U_{eh-h} = C_n \cdot (n^2 p - n_0^{\;2} p_0) + C_p \cdot (np^2 - n_0 p_0^{\;2}) \tag{36}$$

Many papers have dealt with the determination of these Auger coefficients. In the thesis of Isidro Martin [29], an interesting discussion can be found on that topic. *Altermatt et al.* demonstrated that C_n can be found in the range of $1.7\text{-}2.8\cdot10^{-31}$ $cm^6\cdot s^{-1}$ while C_p $0.99\text{-}1.2\cdot10^{-31}$ $cm^6\cdot s^{-1}$[30], based on the *Hangleite*r and *Häcker* theory[19][31]. Kerr and Cuevas on the other hand made the most complete parametrization of Auger coefficients in 2002 all the while including some Coulomb interactions between particles in c-Si[32]. As stated before, Auger recombination cannot be avoided just like radiative recombination as those are intrinsic processes within the c-Si bulk. Nevertheless, unlike radiative recombination, Auger recombination is far from being negligible and has a noticeable influence on the overall bulk lifetime, at high-injection levels especially or when dealing with highly doped semiconductors.

1.3.1.c Shockley-Read-Hall recombination: defect-assisted recombination

The Shockley-Read-Hall recombination is also commonly known as the SRH recombination. This phenomenon was first described and formalized by *Hall*[33] and *Shockley* and *Read*[34] in the 1950s. This recombination mechanism takes place in the c-Si bulk (or surface as we will see later) through the assistance of defects, whose energies are located within the forbidden energy bandgap of the semiconductor. Although direct band-to-band recombination with multi-phonon emission is unlikely to happen, the presence of this defect as a localized state, strongly coupled to the crystalline lattice, makes it more probable. Hence, a phenomenon that was supposed to be negligible becomes actually dominant in the overall recombination process in indirect bandgap semiconductors. The origin of the defects can be manifold: they can indeed correspond to dislocations, vacancies, impurities or even dopants, etc. Therefore, unlike radiative or Auger recombination, SRH recombination is not an intrinsic process within the c-Si bulk. Should we be able to produce a perfect flawless crystal, we would completely be free from this contribution to the overall recombination rate. However, defects exist and are efficient SRH recombination centers, dominating the overall c-Si bulk lifetime τ_{bulk}. Figure 1-12 shows all the possible interactions of an electron-hole pair with a defect situated at an energy level E_t: i) an electron from the conduction band gets trapped by the defect at an energy level of E_t; ii) an electron trapped by a defect at an energy level of E_t is released into the conduction band; iii) a hole from the valence band gets trapped

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[19] This work takes into account Coulomb interaction between carriers and shows that these forces enhance the carrier density of one type close to a charge carrier of the opposite sign. This phenomenon results in an increase of the recombination rate.

by the defect at an energy level E_t; iv) a hole trapped by the defect at an energy level of E_t is released into the valence band.

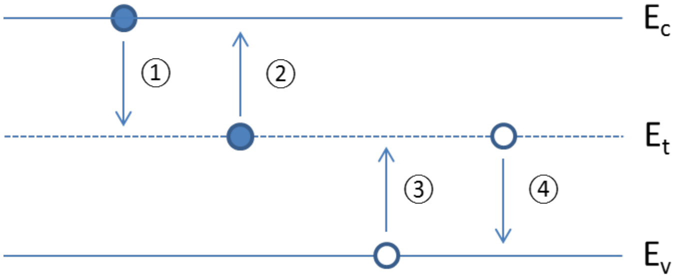

Figure 1-12: Interactions of an electron-hole pair with a defect located at an energy level E_t: (1) capture of an electron from the conduction band, (2) emission of an electron from E_t, (3) capture of a hole from the valence band and (4) emission of a hole from E_t.

When an electron and a hole simultaneously get trapped at a given energy level E_t, there is an increased probability that they might meet and thus recombine. Given some assumptions, the net recombination rate can be expressed in $cm^{-3} \cdot s^{-1}$ as:

$$U_{SRH} = \frac{n \cdot p - n_i^2}{\tau_{n,SRH}(p + p_t) + \tau_{p,SRH}(n + n_t)} \tag{37}$$

where $\tau_{n,SRH}$ and $\tau_{p,SRH}$ are the electron and hole capture lifetimes and n_t and p_t the density of trapped electrons and holes, respectively. These can in turn be expressed as:

$$\tau_{n,SRH} = \frac{1}{N_t \cdot \sigma_n \cdot v_{th,n}} \tag{38}$$

$$\tau_{p,SRH} = \frac{1}{N_t \cdot \sigma_p \cdot v_{th,p}} \tag{39}$$

where N_t is the trap density, σ_n and σ_p the capture cross sections of the trap for electrons and holes respectively, $v_{th,n}$ and $v_{th,p}$ the thermal velocity of the charge carriers. If we consider a trap density N_t at an energy level of E_t, the densities of electrons and holes that are trapped, respectively, can be defined as:

$$n_t = n_i e^{\frac{E_t - E_i}{k_B T}} \tag{40}$$

$$p_t = n_i e^{\frac{E_i - E_t}{k_B T}} \tag{41}$$

Where E_i and n_i are the energy level and the carrier density in the intrinsic case respectively. Taking into account expressions 38 and 39, and by considering $v_{th,n} \approx v_{th,p}$ in c-Si at 300K (~$2.05 \cdot 10^7$ and $1.69 \cdot 10^7$ for electrons and holes respectively), Eq. 37 can then be rewritten as follows:

$$U_{SRH} = \frac{v_{th} \cdot N_t \cdot (n \cdot p - n_i^2)}{\frac{(p + p_t)}{\sigma_n} + \frac{(n + n_t)}{\sigma_p}} \tag{42}$$

As stated earlier, it is important to keep in mind that the description of SRH recombination is based on some assumptions. These assumptions imply that: i) there is no recombination mechanism taking place other than defect-assisted, ii) the Fermi level lies within the bandgap, i.e., the semiconductor is not degenerated, iii) the position of E_t does not change depending on its charge state, iv) $N_{defects} << N_D$, v) there is no interaction between the defects, vi) the relaxation time of the charge carriers is negligibly small compared to the average time between two emission. Moreover, Eq. 40 and 41 imply that SRH recombination processes take place in an environment where Fermi-Dirac statistics rule. Under these conditions, two cases can be considered, depending on the location of the E_t in the forbidden energy bandgap: i) E_t is close to either the VB or CB; ii) E_t is close to midgap. In the first case, the carriers that get trapped at E_t are more likely to be reemitted again to their original energy band because the energy difference is low. The probability of capturing a carrier of opposite sign to allow recombination is therefore much lower than the probability to see the first carrier escaping from E_t. As a consequence, the contribution of these so-called “shallow defects” to the net recombination is very low. On the contrary, if E_t is located around midgap, the probability of capture of an electron and a hole is much higher: this allows them to meet and thus recombine. As a consequence, defects located near midgap are more active to assist recombination. Hence, the contribution of these so-called “deep defects” to the net recombination is very high. Moreover, dopants are “impurities” to the crystalline lattice. Because of this, they will act as trapping centers for charge carriers flowing through the device. The more doped the c-Si, the more trapping centers within the forbidden energy bandgap.

1.3.1.d Bulk lifetime

Based on Eq. 30 we can express the recombination lifetimes which characterizes all recombination occurring within the c-Si bulk τ_{bulk}. It can be written as follows:

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} \tag{43}$$

As can be seen in Eq. 43, the shortest lifetime will dominate this sum by yielding the highest recombination contribution. $1/\tau_{bulk}$ will thus be limited by the shortest lifetime, i.e., by the most efficient recombination mechanism. In Figure 1-13 are plotted the three contributions to the overall bulk lifetime as a function of the excess carrier density for a 2.6 Ω.cm n-type wafer. For SRH recombination, E_t was taken at midgap so that $E_t=E_i$ whereas a value of 10 ms was chosen for $\tau_{n,SRH}$ and $\tau_{p,SRH,}$ τ_{SRH}. As stated before, we see that the overall bulk lifetime is limited by the SRH recombination at low-injection levels whereas Auger recombination becomes dominant at high-injection levels. Moreover, we witness the negligible influence of radiative recombination on the overall bulk lifetime, regardless of how low or how high the injection level is. Notice also that the SRH lifetime is constant at low and high injection levels.

1.3.2 Hydrogenated amorphous silicon

Silicon was presented earlier in its crystalline form. However, this material can exist in non-crystalline structures, such as amorphous silicon[20]. This material was first synthesized in the late 1960s. Before that,

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[20] Even if the word “hydrogenated” is not always mentioned, amorphous silicon always contains hydrogen when deposited by RF PECVD from gases such as silane. From now on, amorphous silicon will always refer to a-Si:H.

unhydrogenated amorphous silicon (a-Si) could be prepared by sputtering or thermal evaporation. As will be stated later, we will mainly focus on a-Si:H, which is a device-grade material compared to a-Si. Although a-Si:H was first deposited in 1969 in the UK by *Chittick and coworkers*, it was abandoned quite quickly. Fortunately, Spear from the University of Dundee had some interest in this material and managed to transfer *Chittick*'s reactor to Dundee. The research carried out in Scotland allowed to demonstrate the qualities of a-Si:H deposited by this technique. Later, the substitutional doping that was thought impossible in this material was reported in 1975 by *Spear and Le Comber*[35], when phosphine and diborane were added to the silane gas. This in fact launched a wave of interest in this material that would allow its thorough study by laboratories such as RCA, IBM, the Carnegie Laboratory of Physics, Xerox Palo Alto Research Center and others. *R.A. Street*'s textbook is a short but dense, easy-to-read manual describing the main properties of amorphous silicon, its doping and deposition mechanisms[36]. *T. Searle*'s textbook is also a reference in that matter[37]. This material is extensively described in these textbooks and we'll go through the main differences between the crystalline and the amorphous forms of silicon to understand the challenges that arise when trying to join these two materials to form a heterojunction.

1.3.2.a The a-Si:H network and its consequences on the density of states

The first striking feature of amorphous silicon is its atomic arrangement. Whereas crystalline silicon has its constituting atoms nicely sitting along a defined crystalline network, amorphous silicon loses very quickly its ordering, i.e., after a couple of interatomic distances. In other words, it does not have a long-range order.

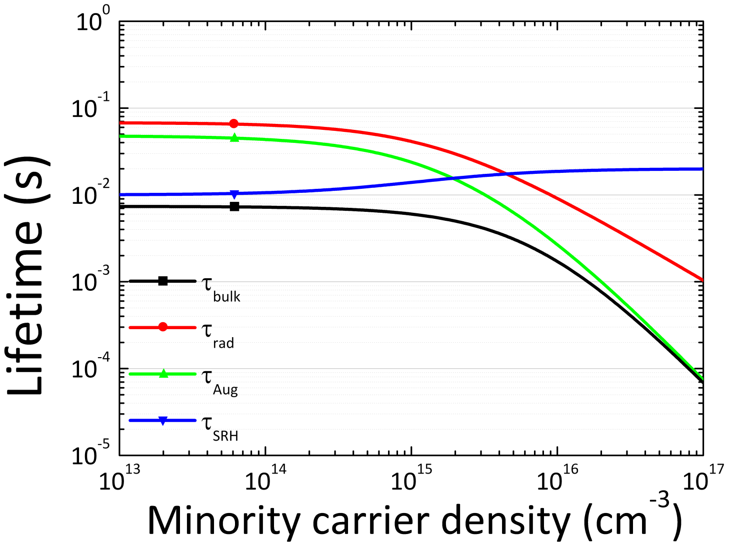

Figure 1-13 — Radiative, Auger and SRH contribution to the overall bulk recombination lifetime as a function of the minority carrier density.

Figure 1-14 depicts a typical network of the a-Si:H material. We see that:

- the bonds do not have the same lengths,
- the angles between bonds vary,
- defects are present in the form of missing silicon atoms.

The covalent bonds between silicon atoms are quite similar actually with the ones found in crystalline silicon. They indeed involve the same number of neighbors and the same average bond lengths and bond angles.

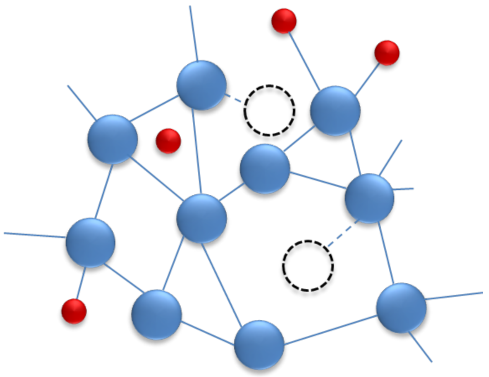

Figure 1-14 — Typical representation of the a-Si:H network.

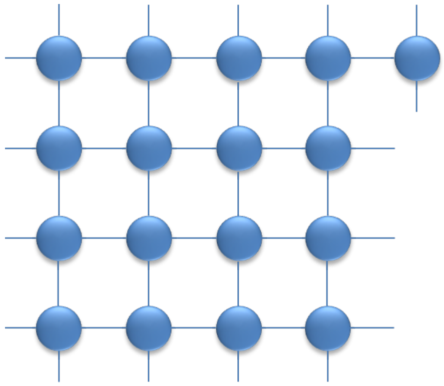

Figure 1-15 — Crystalline network of c-Si.

In fine, the amorphous version of silicon has the same short range order as the crystalline one but becomes less and less organized in the longer range. These differences all result in a particular electron distribution of states. As can be seen in Figure 1-16, the energy bandgap, usually "forbidden" and devoid of states, contains a broad peak. This peak is caused by defects present in the amorphous silicon material in the form of unsaturated dangling bonds. In a crystalline network, defects can be in the form of missing atoms, dislocation of an atom in an interstitial position. This definition does not apply to a disordered network with a short-range order solely. Therefore, a defect in an amorphous matrix will be a coordination defect, i.e., an atom which has too many of too few bonds. The density of these defect states can easily reach 10^{19} cm^{-3}. If not for these "missing" silicon atoms, all the bonds would be saturated and the forbidden bandgap would remain empty. Likewise, increasing the hydrogen content in the network will eventually lead to dangling bond saturation and a decrease in the defect state density down to approximately 10^{15} cm^{-3}. This is the kind of device-grade material we're interested in. Indeed, the high defect density of nonhydrogenated amorphous silicon prevents it from being doped and photoconductive. Also, these defects control some important electronic properties by changing the trapping efficiency and carrier recombination within the bulk. Apart from the "not-so forbidden" bandgap, the electron distribution of states is broader. In Figure 1-16 again, we see that the band edges are not very sharp as is usually the case for crystalline semiconductors such as crystalline silicon. The abrupt edges are replaced by tails of states, which extends into the forbidden bandgap. This is due to the deviations of the bond length and angle, which originates from the long range structural disorder. Even though this difference may look quite negligible it is of great importance, since electronic transport occurs at the band edge. By inducing scattering, the carrier mobility will be reduced above the mobility edges. For these reasons, it was hard at first to use the notion of bandgap for such a material.

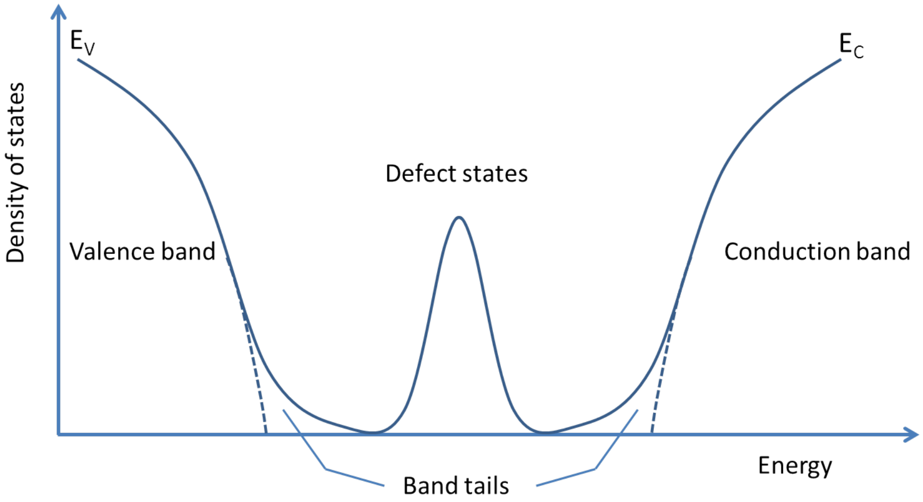

Figure 1-16 — Schematic density of states of a-Si:H as a function of energy. Unsaturated dangling bonds foster the emergence of defect states within the forbidden energy bandgap while bond distortion (length and angle) leads to tail states at the conduction (valence) band minimum (maximum).

The solution is to use the mobility bandgap of a-Si:H:

$$E_\mu = E_c - E_v \tag{44}$$

since here, the mobility bandgap differs from the optical bandgap. Localized states in the band tails take part in the absorption process. Therefore, the optical bandgap will always be smaller than the mobility bandgap. Another useful definition is the E_{04} bandgap, which corresponds to the photon energy for which the absorption coefficient α is 10^4 cm^{-1}. The most widely used definition though is the Tauc bandgap defined by the following expression:

$$\alpha(E) = \frac{(E - E_{g,Tauc})^2}{E} \tag{45}$$

All these definitions are valid, however, if we keep in mind that they all differ by very little (up to 0.1eV at the most) and that we can approximate the relationship between E_μ and E_g by stating that:

$$E_\mu \approx E_g + 0.15\,\mathrm{eV} \tag{46}$$

Apart from the impact of localized states and tail states within the energy bandgap, with the possibility of getting different configurations between atoms and defects within the a-Si:H network arises the phenomenon of metastability. This can be caused by introducing energy into the system: light, current or voltage, ion bombardment, etc. This energy will indeed trigger changes that will affect the quality of the a-Si:H material. The most important phenomenon of this type is known as the Staebler-Wronski effect, or SWE discovered in 1977[38]. This causes the slow degradation of solar cells made with a-Si:H since they are highly exposed to sunlight. Indeed, under prolonged illumination an increase of the defect density from 10^{15} up to 10^{17} cm^{-3} is experienced, mainly due to the apparition of dangling bonds[39]. *Staebler and Wronski* suggested that these defects might come from a nonradiative recombination process of excess charge carrier within the a-Si:H bulk[40]. *Stutzmann et al*. proposed that these dangling bonds originate from broken weak Si-Si bonds that remain unpassivated by a hydrogen atom[41]. However, *Fritzsche* suggested in a review that apart from the creation of defects, changes in the structural network must occur[42]. Indeed, a metastable expansion phenomenon of the a-Si:H lattice was observed upon light-soaking thereby confirming this possibility[43]. Despite intensive research on this topic over the last decades, the exact mechanisms are still under debate[44]. However, in the case of SHJ solar cells, even though their architecture contains layers of a-Si:H, we are less subject to this degradation effect. Indeed, since our absorber is the c-Si wafer, we only use very thin layers of a-Si:H. *Olibet et al.* have shown that the SWE was highly-dependent on the a-Si:H layer thickness[45]. Furthermore, the dependence on such degradation was actually found to be opposite than that of fully amorphous solar cells wherein the thicker the a-Si:H layer is, the more it is sensitive to degradation.

Substitutional doping of this material was not obvious at all at first. In 1975, *Spear and Le Comber* reported that a-Si:H could be doped by the addition of boron and phosphorus[35]. This represented a major turning point for this material and in the development of amorphous semiconductor devices. Indeed, theory predicted that substitutional doping of this material was impossible because of the 8-N rule for chemical bonding. This famous rule states that all elements in a random amorphous network bond while respecting their optimal valency, irrespective of the neighboring atoms. In this way, a maximum of electrons are paired in bonding orbitals while the remaining are paired in non-bonding states while leaving the anti-bonding states empty. In its crystalline counterpart, the periodicity of the lattice forces the impurity to have the same coordination as silicon, promoting boron and phosphorus atoms to dopant states. A variation of this coordination is exceptional and would result only from a defect within the crystalline structure. This type of constraint is absent in the a-Si:H network, therefore, there is no reason why substitutional doping should be possible. Only a modification of the 8-N rule makes it possible. Otherwise, phosphorus for example should be three-fold coordinated, thus inactive as a dopant. This is fortunately not the case and amorphous silicon can be n- or p-doped and used to fabricate devices. For more details on the metastability and doping of the a-Si:H material, the reader is referred to the very thorough review published by *Street* in 1991[36].

1.3.2.b Plasma-Enhanced Chemical Vapor Deposition (PECVD)

The deposition of a-Si:H by the dissociation of silane was first reported by *Ogier* in 1879[46]. However, the interest for this material was quite limited at the time. Only in 1969 did a team composed of *Chittick*, *Alexander and Sterling* synthesize amorphous silicon in the UK. In order to do so, they dissociated silane molecules (SiH_4) by creating a plasma and depositing these molecules on a heated substrate. While the reactors' geometry and the setup designs have much evolved since then, the concept remains identical: SiH_4 is the most widely used gas and is dissociated between two parallel electrodes in a stainless steel chamber which is pumped down to a pressure below 10^{-6} mbar, as Figure 1-17 shows. A plasma can be defined as an ionized gas that is macroscopically neutral. Ionization can be achieved by providing energy to the system in the form of a thermal, optical or electrical excitation. The first a-Si:H deposition system developed by *Chittick et al.* in 1969 was an RF inductive system. Most subsequent systems were designed so that a capacitive discharge would dissociate the gases. Using RF PECVD at a 13.56 MHz frequency is today to most common way to deposit a-Si:H thin films, although other techniques have been developed by researchers, such as very-high frequency CVD (VH-CVD)[47], expanding thermal plasma[48], hot-wire CVD (HWCVD)[49], microwave CVD (µW-CVD)[50], atmospheric pressure CVD (APCVD)[51], ionized cluster beam deposition[52].

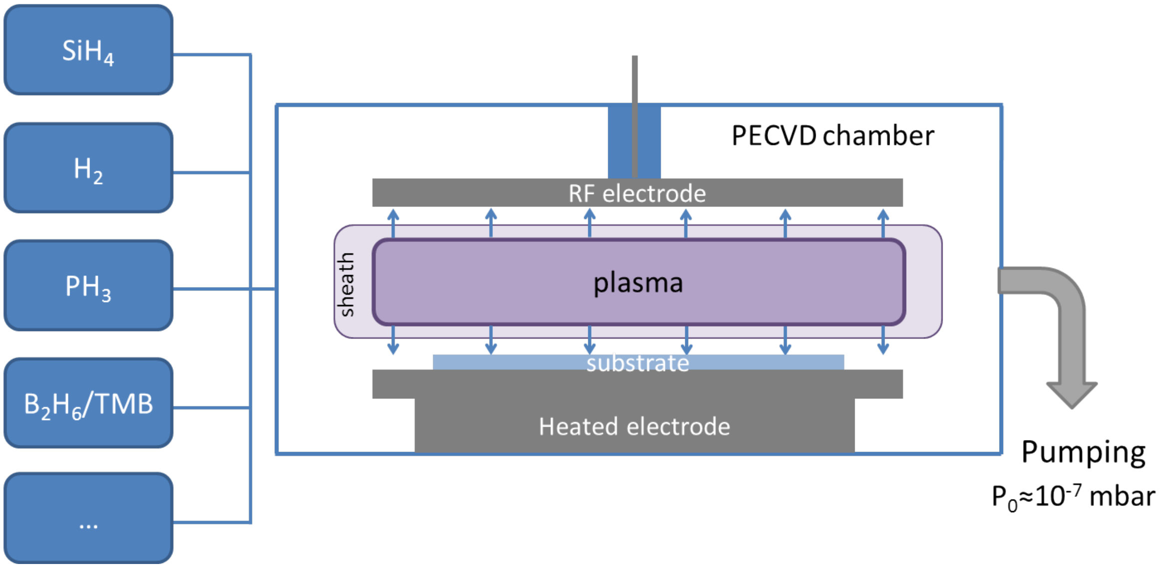

Figure 1-17 — Schematic diagram of basic PECVD deposition reactor. It consists of a gas injection system, a vacuum chamber and of a parallel plate system (RF power electrode + grounded and heated substrate holder). This system has allowed for uniform a-Si:H deposition on substrate sizes up to 5.7 m².

RF PECVD reactors benefit from several advantages, which are intrinsically related to plasma processes:

- the dissociation of gas precursors occurs through collisions with high-energy electrons, thus allowing for deposition even at RT,
- parts of the species present in the plasma are charged (ions) and therefore can be accelerated towards the sample and bring energy to the growing film, thus allowing for a monitoring of the deposited material quality,
- by adding other gases, amorphous silicon can easily be transformed into an alloy (a-SiC:H, a-SiOx:H, etc.) or even doped (p- and n-type),
- stacks can easily be deposited by varying instantly the gas content and other plasma parameters (RF power, pressures, etc.).

On the diagram shown in Figure 1-17 one can see that the PECVD chamber is firstly pumped down to a pressure below 10^{-6} mbars, usually around $6 \cdot 10^{-7}$ mbars. The reactor being heated up to a temperature close to 200°C for most a-Si:H depositions, vacuum allows for the chamber to be free from any remnant humidity or oxygen molecules that could be present on the walls, the electrodes or the substrate. After reaching such a vacuum level, gases are introduced. In order to understand the processes taking place within the plasma and at the substrate surface, we will focus on the example of silane. Indeed, even though other gases can be used (Si_2H_6, SiF_4, $SiCl_3H$, etc.), it has been and is still the most widely studied gas precursor for a-Si:H deposition. Once SiH_4 is in the PECVD chamber, the pressure can usually be monitored via a throttle valve located downstream in the exhaust line. The gas temperature is determined by the temperature of the heated electrode and by the gas properties. Then, when the system is stabilized (constant pressure and temperature), the power is applied on the RF electrode. As a result, electrons are accelerated by the electric field and gain enough energy to dissociate SiH4 molecules. This, in turn, results in the potential distribution depicted in Figure 1-18. Indeed, thanks to the lower mass of the electrons, the energy they gain can heat the electrons up to a few tens of eV[21]. Contrariwise, bigger species such as ions, radicals, molecules are thermalized and their energy remains close to the reactor's wall temperature (~300 K). As stated before, plasma is an ionized gas which is macroscopically neutral. Because of this, a transition region arises (sheath) between the plasma and the reactor walls. If it were not for this sheath, the energy of the electrons would allow them to leave the plasma. This applies for all negatively-charged species inside the plasma. Contrariwise, positively-charged particles, such as ions, will be accelerated towards the walls and the substrate, leading to ion bombardment effects. In many reactors, especially in R&D, the two electrode areas are different and usually the RF electrode area is smaller than the grounded surface. As a result of this asymmetry, a self-bias (V_{DC}) arises on the RF electrode and its value will depend on the area law [53]:

$$\frac{V_1}{V_2} = \left(\frac{A_1}{A_2}\right)^n \quad 2 < n < 4 \tag{47}$$

where n is experimentally close to 5/2. In the industry, reactors are much larger and the area ratio is close to 1, thus reducing V_{DC}. In the perfectly symmetrical case, $V_1=V_2=V_P$. In our case however, the system is not symmetric, $V_1 \neq V_2$ and the plasma potential is given by the following equation:

$$V_P = \frac{1}{2}(V_{RF} + V_{DC}) \tag{48}$$

It is of great importance since the energy of the ions will depend on the difference between the plasma and substrate potentials. As stated before, the electrons provide the larger part of the energy for the dissociation of silane.

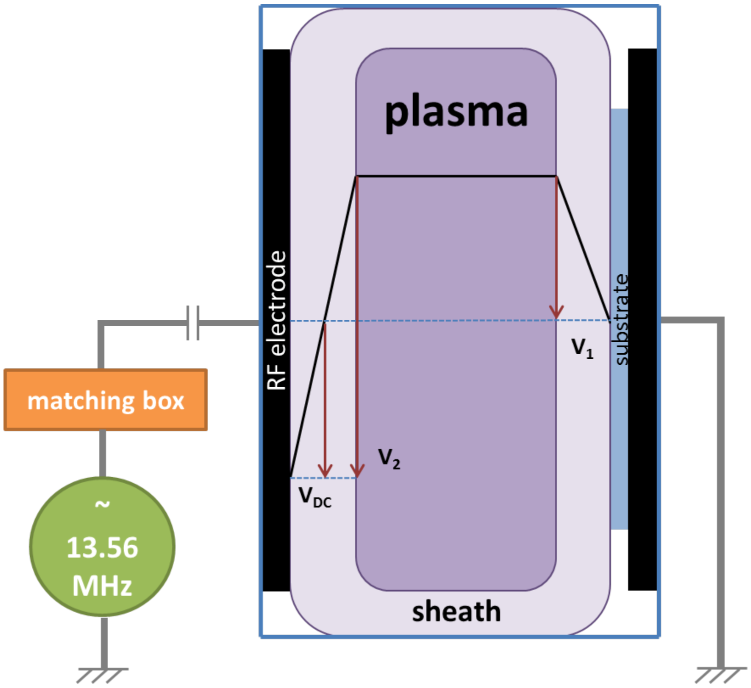

Figure 1-18 — DC potential distribution in a capacitively coupled RF glow discharge reactor.

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[21] 1 eV is equivalent to 11,600 K.

The different types of specie present in the plasma will then highly depend on the energy of the electrons. It is a function of the electric field (determined by the RF power) and of their mean free path (determined by the total pressure inside the reactor). However, besides these primary reactions secondary reactions occurring between the products of primary reactions with silane molecules must be taken into account in most cases. This is because the typical degree of dissociation in silane plasma usually does not go beyond 10%. It can be increased by increasing the RF power coupled to the plasma and this will, in turn, enhance secondary reactions, which can actually start dominating the plasma chemistry[54][55]. The wide variety of species present after the dissociation of a silane molecule upon the impact of a 70 eV electron has been studied by *Schmitt* in 1983 with the help of mass spectroscopy measurements. A schematic drawing sums up the species produced in Figure 1-19[56]. As can be seen, 58% of the species are radicals (SiH_3, SiH_2, SiH, Si). As they have no charge, their interaction with the substrate will be determined by diffusion processes and by the temperature. The other main products are positive ions (SiH_3^+, SiH_2^+, SiH^+, Si^+). Since they have a net positive charge, while arriving to the plasma limits (sheath boundary), they will be accelerated towards the substrate with an energy of the order of the plasma potential (V_p). Of course, depending on their mean-free path, they might reach the substrate with a lower energy due to collisions within the sheath. Apart from these products, other species can be present and interact with the growing film on the substrate:

- high energy electrons. Even though most of the electrons are confined within the plasma because of the higher potential of the plasma with respect to the substrate potential, some have enough energy to reach the substrate and promote chemical reactions[57],
- negatively charged ions and the large powders they produce[58],
- clusters and nanocrystals formed in the plasma. Their charge will determine whether they will be able to cross the sheath and reach the substrate. This is thought to be related to their sizes[58][59].

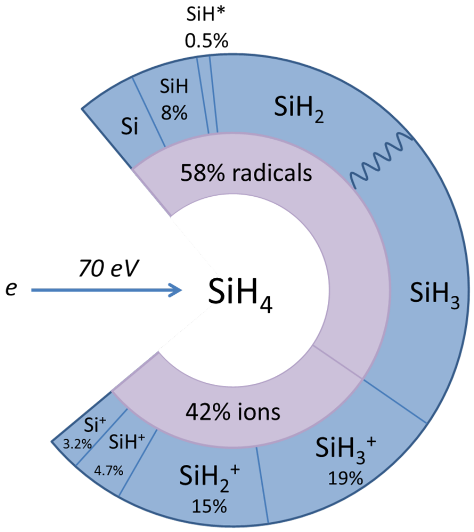

Figure 1-19 — Schematic representation of the products generated upon the impact of a 70 eV electron on a silane molecule as deduced from mass spectroscopy measurements. Adapted from reference [56].

It is important to understand the mechanisms that govern a-Si:H growth because it is a highly tunable material. Indeed, hydrogen content may vary from 8 to 40 at. % and most of the features of the a-Si:H network are defined during the growth[60]. The quality of the material obtained will then greatly depend on the deposition process. However, the role of each of these products in the a-Si:H growth will not be discussed here. For this, the reader is referred to the literature on the topic[61][62][63].

1.3.2.c a-Si:H growth mechanism model

Although the a-Si:H growth have been widely studied since the 1970s, its growth mechanisms are still under debate. However, a model has emerged, based on the SiH_3 radical called the *MGP model*. It is named after three scientists: *Matsuda*, *Gallagher* and *Perrin*. Their assumption was that since SiH_3 was predicted[64] and reported experimentally[56][65] to be the most dominant product of the dissociation of SiH_4 by plasma, it should govern the a-Si:H growth. The interactions between an SiH_3 radical and the growing a-Si:H layer is depicted schematically in Figure 1-20. A SiH_3 radical derived from the SiH_4 plasma after diffusing through the sheath can land at the surface of the growing layer and undergo physisorption with a probability β. This phenomenon is made possible by the creation of a weak SiH_3-H-Si bond between the radical and a hydrogen atom bonded to a silicon atom from the a-Si:H layer.

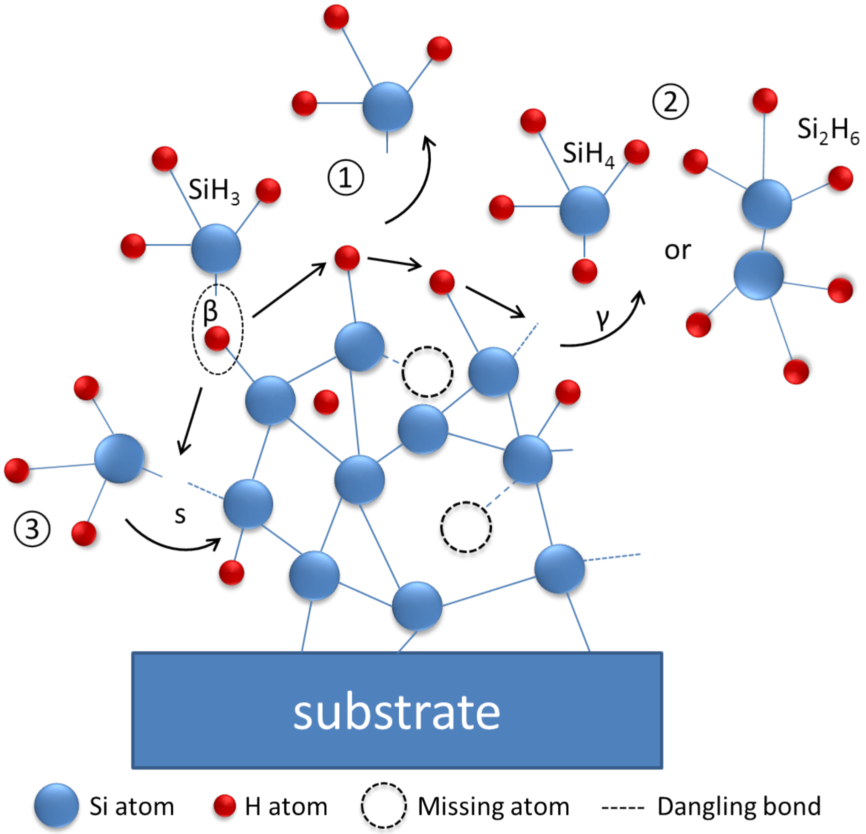

Figure 1-20 — Schematic representation the possible interactions between a SiH_3 radical produced from the dissociation of SiH_4 in a plasma and the surface of the growing a-Si:H layer.

Then, the physisorbed radical can diffuse on the surface from H atom to H atom, until one of the following events occurs:

- the SiH_3 radical desorbs from the surface and goes back to the gas phase. This is highly probable since its sticking coefficient was measured to be quite low (~0.1)[66],

- the SiH_3 radical removes a hydrogen atom (probability γ) or recombines with a SiH_3 radical from the growing a-Si:H layer and goes back to the gas phase as a SiH_4 or Si_2H_6 molecule, respectively,
- the SiH_3 radical finds an empty site (dangling bond) and creates a SiH_3-Si covalent bond with a sticking probability s, resulting in further growth of the a-Si:H material.

As a result, we have $\beta=\gamma+s$. It is to be noted that the fact that SiH_3 is the most abundant radical does not necessarily means it rules the a-Si:H growth. This is all the more true than SiH_3 radicals have a very low sticking coefficient (~0.1) and therefore, the chances of bouncing back to the gas phase are much greater than in the case of SiH_2 or SiH radicals (sticking coefficient of ~0.9)[66]. Nevertheless, it has been found that the presence of SiH_3 is widely related to device-grade a-Si:H materials. It is easy to guess that the more the SiH_3 radical diffuses, the more it has the chance to find a dangling bond and thus, to contribute to the layer growth. This seems to agree with its low sticking coefficient. It has been shown however, that the diffusion of radicals can occur on a distance of 32 Å (molecular-dynamics simulation[67]) and sometimes on a few lattice spacings only (kinetic Monte Carlo simulations based on *ab initio* activation energies [68]). Nevertheless, the growth model depicted in Figure 1-20 is the most widely used to explain the a-Si:H growth. Even if it is pertinent for low pressure and low RF power conditions, it is not valid any longer at high deposition rates. Indeed, increasing the RF power, the pressure or changing the gas dilution will induce secondary reactions and the generation of nanoparticles in the plasma[58][69][70]. These could indeed be directly incorporated and affect the material growth. Moreover, simulations have shown that the physisorption of SiH_3 radicals as depicted in Figure 1-20 would be replaced by the displacement of a hydrogen atom and by the direct binding of the radical to the free site on the Si atom[71]. Nevertheless, these studies do not always concur and, despite many flaws, the MGP model provides an interesting basic understanding of the plasma/surface interactions. Moreover, as we shall see, passivation is often conducted under soft conditions (low RF power, low pressure) and therefore, we could be closer to this model than we actually think.

1.3.2.d ARCAM reactor

The PECVD reactor mainly used for this thesis was the ARCAM[22] reactor, built in the 1980s. A full description of its design can be found in *Roca i Cabarrocas et al*[72]. As can be seen in Figure 1-21, it is a monochamber reactor. However, three electrodes are present inside and thanks to the particular shape of the counter-electrodes (which are in fact plasma boxes) three distinct zones coexist. This allows for the reactive species to stay confined within each plasma box despite the fact that the gases can diffuse inside the whole vessel. Therefore, it is possible to deposit very different materials during the same reactor run without causing any cross-contamination effects. This is indeed crucial when dealing with doped layers. Thanks to this specific design, the ARCAM is in fact what we would call a *monochamber multiplasma* PECVD reactor. To fabricate SHJ solar cells, three plasma boxes are used, one for each doping: intrinsic, n-type and p-type a-Si:H. This design has proved efficient in the fabrication of device grade materials and high-quality a-Si:H/c-Si interfaces, allowing for conversion efficiencies as high as 17.2%[12]. The entire vessel is pumped down to pressures below 10^{-6} mbar (~$5\cdot10^{-7}$ mbar).

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[22] *Action de Recherche Coordonnée sur les Matériaux Amorphes* or *Coordinated Research Project on Amorphous Materials (CRPAM).*

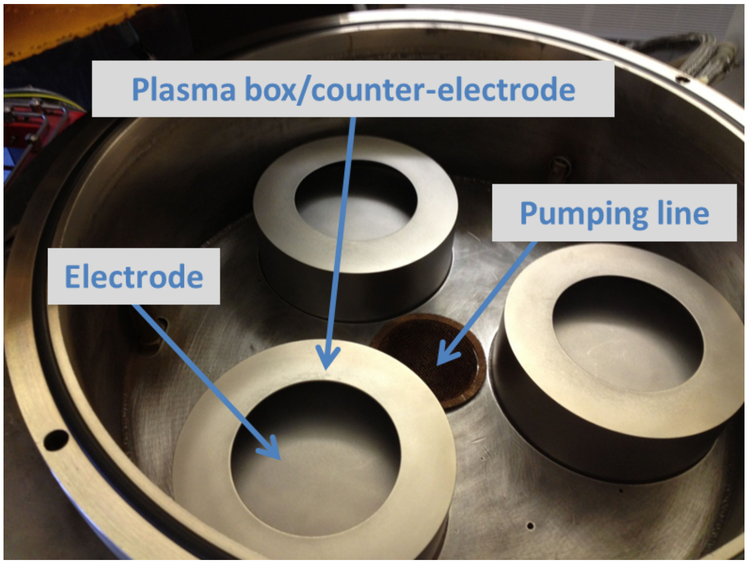

Figure 1-21 — Inside view of the ARCAM reactor. Three plasma confinement boxes can be seen with their RF electrode.

At 200°C, it requires approximately 45 minutes to reach this pressure when the wafers are at RT. The specific design of this reactor (no load-lock) requires its opening to flip the sample after depositing on the first side. This means exposure to air and a second pumping cycle (this time shorter, i.e., 20 minutes). Fortunately, it is still possible to obtain good passivation levels as the second side remains clean despite two pumping cycles and exposure air. The whole chamber is kept at a constant temperature thanks to three Thermocoax wires at three different levels inside the vessel. In Figure 1-22 is shown a detailed cross-section of one of the plasma “chamber” of the ARCAM reactor. Despite many similarities with the classical PECVD reactor architecture shown in Figure 1-17, we can see how the plasma box confines the reactive species. Moreover, the substrate is facing down, preventing any contamination from powders or any macro impurity from falling on it during the introduction of the gases or during the material growth by plasma.

It is worth noting that since we were using quite conductive wafers throughout this Ph.D. thesis , i.e., 2.6 Ω·cm n-type crystalline silicon wafers, the substrate was grounded together with the substrate-holder, itself being in contact with the counter-electrode (plasma box).Since the plasma behaves similarly to a variable load, a matching box is required between the RF voltage source and the plasma. It allows adapting the impedance of the plasma to that of a 50 Ω load for the generator. This way, the applied RF power (at a 13.56 MHz frequency) can be effectively used, thus minimizing the reflected power. As we will later see, when fabricating samples with only one doping type (symmetrical stacks), the plasma box aperture did not need to be fully covered. As a result, quarters of wafer could be used for the fabrication of certain test samples. Most of the time however, 4-inch whole wafers were used when fabricating solar cells in order to completely cover the round aperture of the plasma box and thus avoid cross-contamination when depositing layers of different doping types. For the deposition of device-grade a-Si:H and thus for passivation experiments, the power needs to be kept low, in order to reduce ion bombardment by a decrease of the plasma potential V_P. This kind of conditions have been reported by several groups[73][74]. In our case, it translates into applying an RF power of 1 to 2 W, which corresponds to a power density of 15-30 mW·cm^{-2} approximately. However, by doing so, the dissociation of silane into the species described in Figure 1-19 of section 1.3.2.b is reduced, thus producing less SiH_3

radicals which are essential for a-Si:H growth. One of the ways to circumvent this issue is to increase the gas residence time defined by the number of molecule N within a given volume and the pumping speed as follows:

$$\tau_{res} = \frac{N}{\left(\frac{dN}{dt}\right)_{pump}} \tag{49}$$

This can be done by increasing the distance between the RF electrode and the sample surface (interelectrode distance d). This way, despite the lower RF power, the average number of collisions of a given molecule before it gets pumped is increased.

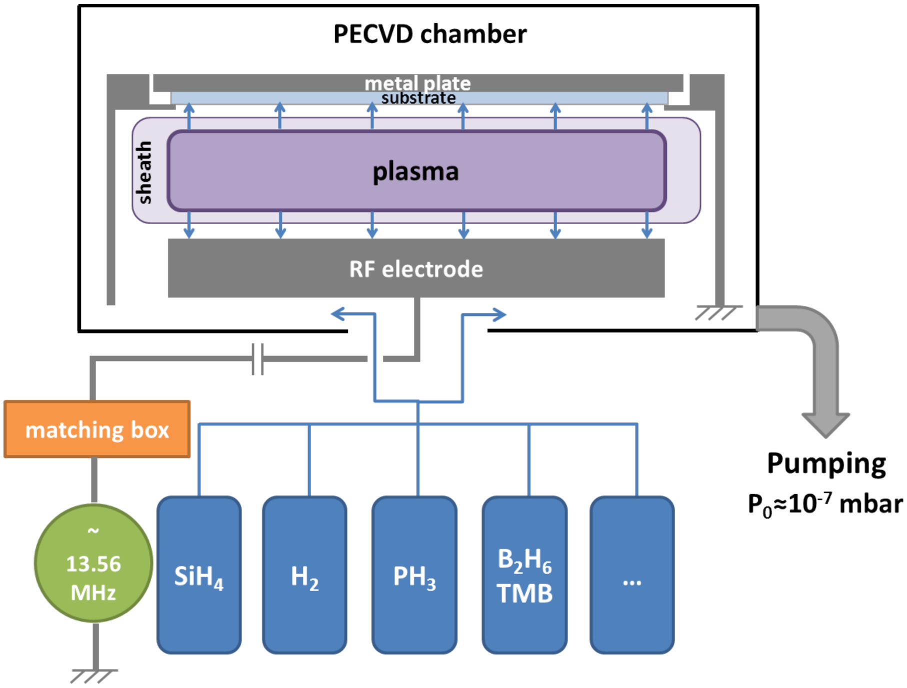

Figure 1-22 — Cross-section of one plasma chamber of the ARCAM reactor.

This can lead to dusty conditions however and to plasma instabilities (V_{dc} fluctuations, extinctions,…). For these reasons, the pressure is also kept low and ranges from 40 up to a few hundreds mTorr at the most. The goal is therefore to use the minimum power to keep the plasma stable. In the ARCAM reactor, the interelectrode distance could be varied by choosing the RF electrode height while the general pressure was controlled by a throttle valve located downstream in the exhaust line. For all of our passivation experiments, an interelectrode distance of 28 mm was chosen.

Chapter Key Facts

After an introduction that was meant to present the solar energy industry as a fast-growing industry that is becoming more and more part of a world energy mix, Chapter I sets a scientific and technical backdrop for the basic physical concepts involved in PV. This allows us to move forward to a very important part of silicon heterojunction solar cells: the crystalline silicon substrate, which plays the role of the absorber. Additionally, the concepts of recombination and lifetimes have been introduced. Finally, hydrogenated amorphous silicon was presented. Its main features have been unveiled and the technique used in this thesis for its deposition described, i.e., plasma-enhanced chemical vapor deposition or PECVD. We are now ready to move forward towards the understanding of the combination of c-Si and a-Si:H by tackling the central concept of this thesis: surface passivation.

2 Crystalline silicon surface passivation by a-Si:H

In the previous chapter we have presented the global energy context in which the solar cell R&D is now evolving, as well as the basics of semiconductor physics. In this section, we propose to go through the state of the art of silicon heterojunction (SHJ) solar cells and passivation. Also, the particularities of the silicon substrate crystalline orientations will be detailed, as they will be at the center of the challenges we meet while passivating with a-Si:H. Finally, the tool used throughout this thesis for the estimation of the passivation quality will be presented.

2.1 Passivation and heterojunction solar cells

The concept of heterojunction begins when joining two materials of different energy bandgaps together. This structure offers many possibilities of applications to devices such as wide band-gap emitters[75], majority carrier rectifiers[76], high-speed wide bandpass photodetectors[77], solar cells[76], transistors[78] and even lasers[79]. As a result of this junction however, band offsets arise in both the conduction and valence bands. This leads to band-diagram specificities, which will later translate into particular solar cell output parameters.

2.1.1 a-Si:H/c-Si heterojunction solar cells and the HiT structure

If we look at the thermodynamic aspect of conversion of solar energy into electrical current, we can distinguish two major steps. First, the beam lights absorbed in the semiconductor material is converted into chemical energy, whose amount will depend on the density of photogenerated carriers. Then, the chemical energy is transformed into electrical energy by separating negatively- and positively-charged carriers, i.e., electron-hole pairs, and by ensuring their collection at the device terminals with minimal recombination losses on their way. In crystalline silicon solar cells, the c-Si wafer plays the role of the absorber. Its thickness must be large enough to absorb efficiently but lower than the diffusion lengths of the charge carriers of both types. Then, the separation of charge carriers can be achieved by adding a surface-passivating layer on the absorber which will act as “semi-permeable” membrane, allowing some charges to pass through and repelling others of opposite sign. Over the years, a large number of surface-passivating materials were designed for this purpose. Among these, the best known is thermally-grown SiO_2. For a long time, the highest conversion efficiency ever reported (25% at AM1.5) featured such a layer[80]. It indeed allows reaching very low effective surface recombination velocities (below $10\ cm\cdot s^{-1}$) for low-resistivity ($1\ \Omega\cdot cm$) n-type c-Si wafers (around $40\ cm\cdot s^{-1}$ for p-type wafers)[81][82][83]. However, despite its high passivating qualities, its growth requires processing temperatures that are too high (~1000°C) to be cost-effective as well as sometimes even compatible with the materials involved. Indeed, at such high temperatures, low-quality c-Si (Czochralski for example) which is widely used in the PV industry, undergoes severe degradation [84][85]. This material is also an effective passivating material for emitter-diffused surfaces. Other PV-suitable passivating materials include a-SiN_x:H [86][87] and its stacking with SiO_2 [88][89]. This material, commonly called SiN_x, is deposited by PECVD at T<500°C using silane (SiH_4) and ammonia (NH_3) while nitrogen (N_2) can be added to reach an optimal stoichiometry and obtain surface recombination velocities below $10\ cm\cdot s^{-1}$[90]. Likewise, it can be used for emitter-diffused surfaces [91]. The advantage of using a SiO_2/SiN_x stack is to obtain the high-quality passivation level provided by SiO_2 all the while incorporating hydrogen upon the SiN_x deposition and post-processing annealing steps, which will diffuse down to the SiO_2/c-Si interface and thus reduce the density of dangling bonds[92]. However, this type of stack brings up the issue of temperature again. On the other hand aluminum-oxide (Al_2O_3) can be grown to passivate crystalline silicon[93][94] and obtain very-low recombination velocities (2 cm·s^{-1} on n-type c-Si)[95]. The deposition rate however, often close to 1 Å/cycle, is a limiting factor for cost-reductions in the PV industry. Nevertheless, it is worth noting that among all the passivating materials described above, all are high-bandgap materials. In fact, they all are insulating dielectric materials. As a result, contacts to the absorber need to be made by "spiking" the metal through the passivating layer to create a direct contact and collect the photogenerated carriers [96][97]. High-efficiency diffused solar cells now very often feature a passivated layer at the back in order to reduce the recombination and selectively enhance collection at the rear. Again, this dielectric layer must be spiked for the rear terminal to contact with the electronically active absorber where the carriers are generated.

One way to combine passivation and collection at the same time is to use a passivating contact. Instead of diffusing dopants and creating a standard homojunction, the dopants can be introduced upon deposition of the passivating layer, thus doping it and creating a pn heterojunction. This is exactly what a-Si:H offers, thanks to its wider bandgap (~1.7 eV)[98], hydrogen content and doping properties[35]. This passivating layer can thus play the role of the semi-permeable membrane for carrier extraction. *Fuhs et al.* were the first to study the a-Si:H/c-Si heterostructure and to demonstrate that such a structure could generate a photocurrent[6]. However, the first solar device was fabricated in 1983 by *Hamakawa and coworkers*[7] using polycrystalline silicon and a-Si:H: the *Honeymoon cell* was born. Later on (p)a-Si:H/(n)c-Si structures were studied and efficiencies close to 12% were reported. Their large dark reverse current revealed a large interface defect density. The remarkable passivating qualities of a-Si:H were demonstrated [8] and Sanyo improved the SHJ structure by adding a thin intrinsic buffer layer at the (p)a-Si:H/(n)c-Si interface, leading to the famous HiT structure[23][9]. As a result, the efficiency was brought up to 14.5%. Not only was the collection improved but also the V_{OC}, thanks to the much lower interface defect density. This very thin layer (~5 nm) allows for keeping a high electric field while reducing the number of defects at the interface. Indeed, having a doped layer contacting directly the c-Si surface means having dopant atoms at the a-Si:H/c-Si interface, which act as recombination centers for charge carriers. By texturing the c-Si substrate[99], by adding a semi-permeable membrane at the rear (this time n-doped) to separate carriers of opposite signs and extract them selectively[100], efficiencies over 18% were reached. By 2000, an efficiency of 20.1% was reported on a 101 cm² surface with a V_{OC} of 700 mV[101]. Then, by reducing the wafer thickness down to 85 µm, an efficiency of 21.4% with an extremely high V_{OC} of 739 mV was reported. This was made possible by improving the a-Si:H/c-Si interface up to a point where the actual limitations started coming from the recombination within the c-Si bulk rather than from the surface. Further optimization of the ITO and silver paste used for the contacts led to the impressive 23.7% conversion efficiency in 2011 on a 98 µm-thick wafer[21]. This is at least 40-50 µm if not 100 µm thinner than most of the industrial standard thickness used in diffused-junction solar cells. Recently, a 24.7% SHJ solar cell with a 750 mV V_{OC}, a J_{SC} of 39.5 mA/cm² and a FF value of 83.2% was reported[5], approaching the 25.0% record of the PERL cell[80][24]. Figure 2-1

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[23] Heterojunction with Intrinsic Thin layer.

[24] In fact, the legendary 25.0% conversion efficiency record of the 4 cm² PERL cell was recently beaten by Sanyo (now Panasonic) with a 25.6% efficiency and a V_{OC} of 740 mV on a 143 cm² surface. However this time, even if the structure remains

shows the HiT structure as developed by Sanyo, both on a flat and textured c-Si wafer. SHJ solar cells cumulate multiple advantages, which explain why the research and the industry both have put so much effort into developing them over the past decades:

i) the V_{OC} can reach extremely high values thanks to the excellent passivating properties of amorphous silicon up to 750 mV, resulting in very-high efficiencies[5]. Even higher V_{OC} values are predicted to be possible by reducing the thickness of the c-Si absorber down to thicknesses close to 50µm[102]. This opens doors to even higher efficiencies in the future when the different challenges related to such thin wafer handling and processing are met,

ii) because the highest a-Si:H material quality is met at temperatures ranging 180-220°C[36], all fabrication steps are usually carried out at temperatures below 250°C. Apart from the obvious cost-reduction related to this, it can also be beneficial for sensitive fabrication process steps, such as the handling of ultra-thin wafers which can be subject to bending and stress,

iii) compared to classical homojunction solar cells, the temperature coefficient of SHJ solar cell is lower. Indeed, with temperature, the conversion efficiency degrades less rapidly than their fully crystalline counterparts. Standard cells exhibit temperature coefficient close to 0.4 $\%\cdot K^{-1}$ whereas these can be as low as 0.3 $\%\cdot K^{-1}$ in the case of SHJ solar cells[103][104][105]. Indeed, their very high V_{OC} makes the temperature coefficient more determined by the a-Si:H material than by the c-Si base, and these are known to be excellent in the case of fully amorphous pin solar cells.

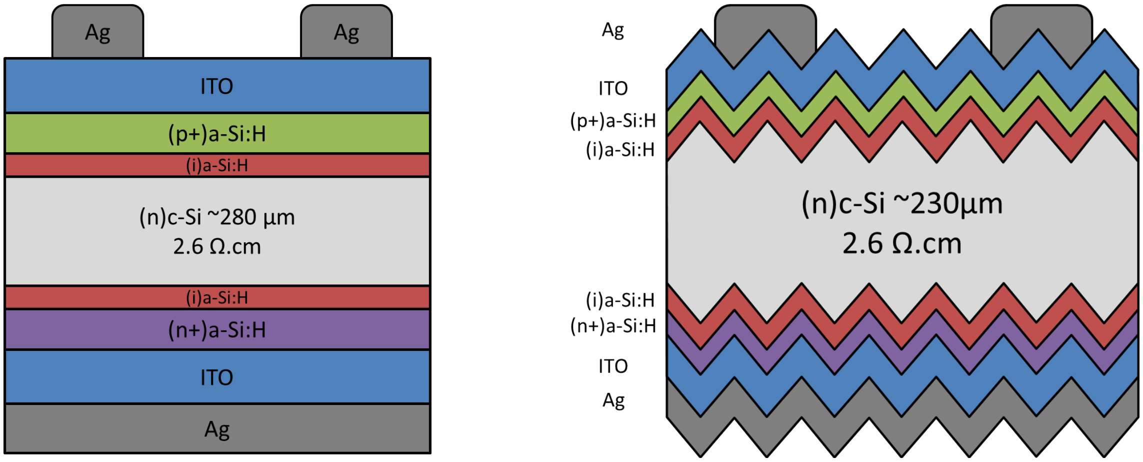

Figure 2-1 — Sketch of the HiT solar cell structure as developed by Sayno on a) flat and b) textured c-Si wafers. Structures are not drawn to scale.

In order to obtain SHJ solar cells with high efficiencies, the c-Si absorber needs to be chosen carefully. However, special attention must be paid to the a-Si:H/c-Si interface and to the a-Si:H material. Indeed, the V_{OC} will highly depend on these two aspects.

HiT-like (combination of a-Si:H and c-Si) it was adapted to the *Interdigitated Back Contact* (IBC) architecture to reduce the optical losses on the front side and thus increase the J_{SC} up to the impressive value of 41.8 mA/cm²[10].

2.1.2 The a-Si:H/c-Si interface

2.1.2.a Band offsets – inversion layer at the a-Si:H/c-Si interfaces

Crystalline silicon heterojunction solar cells are based on a heterojunction made of crystalline silicon (c-Si) for the low-energy bandgap material (1.12 eV) and on hydrogenated amorphous silicon (a-Si:H) for the high-energy bandgap material (~1.7 eV). This combination results in a band mismatch. The conduction and valence band edges levels cannot remain continuous through the junction. As a results, what we call band offsets arise. Figure 2-2 shows a schematic band diagram of a SHJ solar cell build on an n-type c-Si wafer. As can be seen, the wafer is sketched in the central part of the diagram. Its bandgap is 1.12 eV since it is made of crystalline silicon. Moreover, its doping level is characterized by its activation energy $\delta^{(n)c\text{-}Si}$, which is the energy that carriers must overcome to access the conduction band. On the left side we have the emitter ((p)a-Si:H layer) which forms, together with the n-type c-Si absorber, our pn junction. Its bandgap is approximately 1.7 eV but can be tuned to be larger by adding some impurities (carbon, oxygen...)[106]. Its activation energy is noted $\delta^{(p)a\text{-}Si:H}$. On the right-hand side we have our back-surface field or BSF. Its energy bangap is also 1.7 eV, since it is made of amorphous silicon. Sometimes this value can vary, depending on the doping and on the addition of impurities, although it is not as crucial as in the case of the (p)a-Si:H on which sunlight impinges. The band offsets are represented by the ΔE_C and ΔE_V values for the conduction and valence bands, respectively.

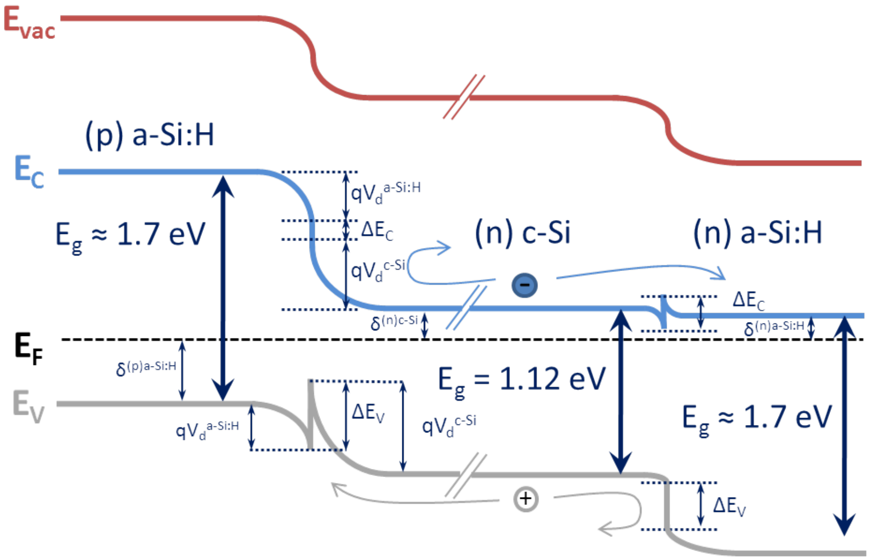

Figure 2-2 — Schematic representation of the band diagram for a (p)a-Si:H/(n)c-Si SHJ solar cell.

As stated before, these band offsets originate from the energy bandgap difference. *Anderson*'s rule[76] allows for their determination by using the junction built-in potential V_{bi}, the energy bandgaps as well as the doping levels $\delta^{(n)c\text{-}Si}$ and $\delta^{(p)a\text{-}Si:H}$:

$$\Delta E_V = \delta^{(n)c-Si} + \delta^{(p)a-Si:H} - E_g^{c-Si} + qV_{bi} \tag{50}$$

As can be seen, these have an impact on the potential barriers on either side of the emitter/absorber (pn junction) and of the absorber/BSF interface, denoted by $V_d^{a\text{-}Si:H}$ and $V_d^{c\text{-}Si}$. Theoretically, they allow the overall built-in potential V_{bi} to be higher than a standard homojunction solar cell since

$V_{bi}=V_d^{c\text{-}Si}+V_d^{a\text{-}Si:H}$. However, the presence of the band offsets ΔE_C and ΔE_V impact the transport of charge carriers through the device. Indeed, as can be seen, two charge carriers are drawn on the diagram: an electron in the conduction band and a hole in the valence band. In the conduction band the electron will be beneficially repelled by the potential barrier imposed by the the pn heterojunction. However, when selectively extracted on the BSF side, it will have to cross the small barrier imposed by ΔE_C. Likewise, in the valence band, the hole will face a potential mostly determined by ΔE_V and be repelled towards the selective (p)a-Si:H contact. However, while travelling through the pn hererojunction, it will face a potential barrier imposed by ΔE_V this time. For *Fantoni et al.*[107] the band offset in the valence band is much larger and hinders hole collection whereas *van Cleef et al.*[108] reported that a sufficient doping of the p-amorphous layer ($>10^{19}$ cm^{-3}) compensates for such effects while measuring cell performance under standard conditions. ΔE_V could be measured and a value of 0.46 eV was reported by *Schmidt et al.* in 2007[109]. Similar values were found by *Korte and Schmidt*[110] and by *Kleider et al.* [111] in 2011. Moreover, it was shown by *Maslova et al.*[112] that holes tend to accumulate as a two-dimensional hole gas (2DHG), leading to highly-conductive lateral channel. This lateral channel, which has also been studied by several other groups[113][114][115], was even thought to be conductive enough to replace the TCO on the front side as a collection "booster"[116]. Recently, *Emmer et al.* suggested that such a lateral carrier flow near the heterointerface could be the reason why SHJ solar cells are so sensitive the defect density[117]. During this thesis, we proposed that the conductivity of this 2D hole gas could be impacted by the interface density. Based on modeling, we reported that this was the case over a certain interface defect density range ($3\cdot10^{11}$-$5\cdot10^{12}$ cm^{-2}). Consequently, coplanar conductivity measurements could be used to assess the passivation quality of (p)a-Si:H/(n)c-Si heterostructures, without having to passivate the second side of the wafer[118]. This is impossible in standard effective lifetime measurements based on photoconductance decay.

2.1.2.b The a-Si:H/c-Si heterointerface and the intrinsic layer

The combination of a-Si:H and c-Si to form a heterostructure raises many challenges. On the one hand, we have a crystal with a very well-defined atomic structure. On the other hand, we have an amorphous material, which loses its periodic ordering after 2 or 3 atomic lengths. The interface is by nature unlikely to be abrupt and suitable for an electronic device. This interface is of great importance because it will be "dividing" the finalized junction. Through this interface, charge carriers will have to flow to be collected at a terminal. Therefore, the final device properties will heavily depend on the quality on the heterojunction interface. However, the combination of the a-Si:H higher bandgap and hydrogen content allows for lowering the interface defect density to a device-grade level. As stated before, introducing a thin intrinsic buffer layer at the (p)a-Si:H/(n)c-Si interface was a major breakthrough for the increase of the efficiency of SHJ solar cell[9]. Compared to homojunction solar cells where diffusion processes lead to a Gaussian or error function-like depth distribution of dopants, the interface in SHJ solar cells is abrupt on the monolayer length scale. By optimizing the wafer cleaning and the doped layers, it is possible to obtain high efficiencies by increasing the J_{SC}.[109] despite the absence of the (i)a-Si:H layer. The V_{OC} however will remain low compared to the HiT-like SHJ solar cells, since the interface defect density cannot be reduced enough because of the presence of dopants, which act as recombination centers.

The quality of the heterointerface will then depend on two parameters:

i) the quality of the a-Si:H layer,
ii) the local network structure at the interface.

These parameters are tunable by varying the PECVD deposition conditions (RF power, temperature, pressure, inter-electrode distance...). Moreover, having a high-quality a-Si:H material and a neat interface at the same time is not at all obvious. Indeed, the interface comprises a particular local network which might not always be in equilibrium with the a-Si:H bulk[74]. Very often, post-deposition annealing brings equilibrium between these two distinct regions. Only afterwards can we consider the interface defect density to be determined by the a-Si:H bulk defects. The next section will deal with the crystalline surface and how its crystalline orientation impacts the abruptness of the a-Si:H/c-Si heterointerface.

2.1.3 Surface passivation of crystalline silicon by a-Si:H

In solid-state physics, every solid (crystal) is built on its periodicity and symmetry. In reality though, this symmetry is broken at the solid's edges because no crystal is infinite. The surface will indeed contain atoms of the crystal but some bonds will be broken and unsaturated. These free bonds are eager to react physically and chemically to stabilize their energy at a lower level. These broken bonds can be identified since they give rise to a precise number of half-filled surface dangling bond orbitals (T_3^0) per surface atom. According to *Adler et al.,* the T_a^b notation describes these surface dangling bond orbitals where T points at the tetrahedrally coordinated site, *a* is the charge state and *b* the coordination number. Due to the bond-breaking, these orbitals are half-filled and feature a single band of states within the bandgap, in the case of intrinsic crystalline silicon. A passivating layer will take part in their neutralization by saturating these dangling bonds and making the surface of the solid "passive", i.e., physically and chemically neutral to reactions that could occur with the environment.

The density and the reactivity of surface dangling bonds at the crystalline silicon surface vary with the crystalline orientation. (100) and (111) silicon will obviously not share the same surface configuration and dangling bond density. Since the surface will be the heart of all passivation challenges, it is therefore important to understand how the Si surface is impacted by the bulk orientation of the ingot upon its processing into wafers.

2.1.3.a The (100) surface

By cutting an ingot in the (100) direction, we end up with a surface covered with two broken bonds (T_2^0) per atom. These are tilted with respect to each other, yielding the unreconstructed Si(100)-(1x1) surface, as shown in Figure 2-3. This is an ideal case though, since this structure is very instable because of the high interaction present between the dangling bonds. These interactions will cause the dehybridization of the neighboring dangling-bonds, resulting in a Si(100)-(2x1) dimer structure[119] as shown in Figure 2-4. This time, two neighboring Si atoms will tend to dimerize by forming a σ-bond between two dangling bonds. The other dangling bonds will overlap in a weaker π-bond yielding an unoccupied dimer structure[120].

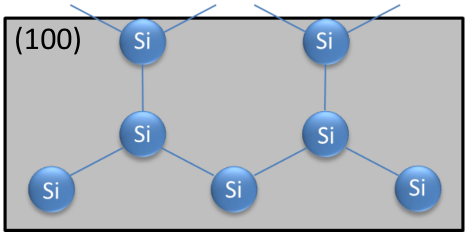

Figure 2-3 – Schematic representation of the unreconstructed Si(100)-(1x1) surface. The truncation in this direction gives rise to two surface dangling bonds per atom.

This dimer can become occupied as soon as the atmosphere surrounding the sample contains atoms that foster the opening of the dimer π-bond. This is particularly true in the case of hydrogen, for which it is energetically favorable to occupy the dimer. As a result, we obtain the doubly-occupied Si(100)-(2x1):H dimer structure shown in Figure 2-5.

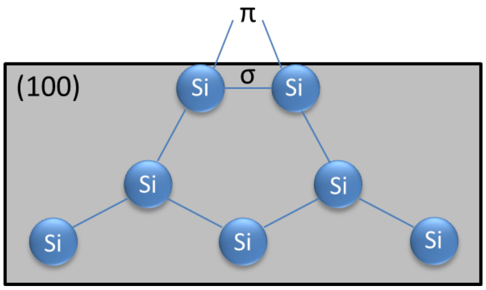

Figure 2-4 – Schematic representation of the Si(100)-(2x1) dimer structures as a result of the interaction between two T_2^0 dangling bond orbitals.

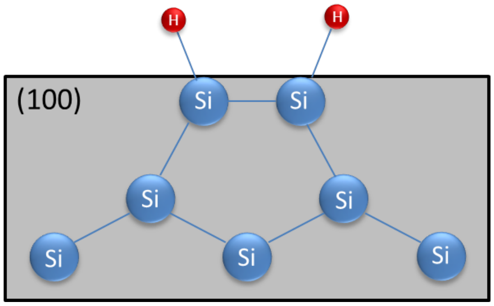

Figure 2-5 – Schematic representation of the doubly-occupied Si(100)-(2x1):H structure.

More generally, the c-Si wafer is usually exposed to air upon fabrication, cleaning and polishing. On its surface, a thin layer of oxide starts to grow to satisfy the unoccupied dimer. This layer of oxide will naturally stop growing after a few angstroms (usually around 1.5-3 nm). In this self-saturating growth process, the wafer surface becomes chemically passive so to speak. Despite this natural "passivating" layer, the wafer is not well passivated. This oxide layer, also known as native oxide, is indeed of poor quality, containing voids and leaving many surface dangling bonds unpassivated. As a result, localized surface states still remain, thus contributing to a higher defect density within the bandgap. This is not the case for thermally grown SiO_2, which has a higher quality and which leads to the passivation of crystalline silicon[81][82].

2.1.3.b The (111) surface

On the other hand, truncating crystalline silicon in the (111) orientation generates broken bonds, which stick out perpendicular from the surface. As a result, we obtain the structure shown in Figure 2-6.

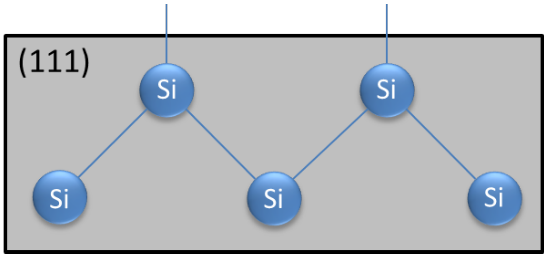

Figure 2-6 – Schematic representation of the dangling bonds at the ideally truncated (111) surface.

These dangling bonds are denoted (T_3^0) since the atom surfaces are back bonded to three Si atoms from the bulk (in 3D). Because of this, as opposed to the (100) orientation, they will not be able to lose energy to form bonds[119]. Generally, the (100) surface has gained a lot of interest in the semiconductor industry because its surface-state density is lower than in the case of other Si surface orientations, such as the (111) orientation[121]. Indeed, the (100) surface exhibits a density of surface atoms of 6.78 10^{14} cm^{-2} as opposed to $7.83 \cdot 10^{14}$ cm^{-2} for the (111). If we take the example of the (100) surface, having a surface defect density of 10^{11} cm^{-2} (good passivation level) would mean to leave only about 1 active defect for 1000 silicon atoms at the interface. For the solar cell industry, these two orientations are of great importance since textured c-Si wafers are usually fabricated from the anisotropic etching of (100)-oriented substrates. As we will see later, texturation is indeed essential to lower the external optical reflectivity and increase the internal reflection[122][25]. It will however increase the surface dangling bond density and the surface to be passivated. This will raise challenges that will be addressed in Chapter 3.

2.2 Assessing the passivating properties of the a-Si:H capping layer

Since the role of passivation is to enhance the charge carrier lifetime within the solar cell structure, we need to understand how to take into account the recombination mechanisms occurring at the edges. Also, it is important to find a way to measure this lifetime in order to choose and optimize the material used to passivate the c-Si substrate. In this section, the formalism of recombination within the c-Si bulk will be applied to its surface and the measurement of passivated sample lifetime will be presented together with the most widely-used measurement method: photoconductance decay or PCD.

2.2.1 Effective lifetime formalism applied to surface recombination

2.2.1.a Surface recombination

In 1.3.1, we have seen what recombination mechanisms rule the bulk lifetime: i) radiative recombination ii) Band-to-band Auger recombination and iii) defect-assisted recombination (SRH). All these recombination mechanisms take place within the c-Si wafer bulk. However, c-Si wafers used in the industry are not edgeless, infinite crystals. Their thicknesses range from 150 µm up to 500 µm very often, depending on their application. For heterojunction solar cells very thin wafers are now used by the main record holders. Indeed, Sanyo (now Panasonic) implemented a 58 µm-thin wafers in their famous HiT architecture to reach a V_{OC} of 745 mV in 2009[123]. Thinner wafers are currently being developed to

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[25] This will in turn increase the J_{SC} of the final solar device.

allow for cost reduction through the reduction of the material used. *Herasimenka et al*. managed to produce 50 µm-thick heterojunction solar cells with an implied V_{OC} above 753 mV[102], raising of course new challenges related to process temperatures which do not lead to any substrate bending and degradation. No matter how thin they can be, the use of c-Si wafers implies that the crystalline network symmetry is completely lost at the substrate edges, thus leading to a higher defect density. Moreover, additional defects can be created during their fabrication (sawing, polishing, etc.) As a consequence, we experience an increased density of defects within the forbidden energy bandgap of the semiconductor. Recombination mechanisms are fostered if not neutralized, i.e., if these surface states are not made *passive*. Since the recombination is increased through a larger amount of defects at the surface, it can still be described by the *Shockley-Read-Hall* theory. However, this leads us to a modified expression of the overall recombination rate (Eq. 42) as follows:

$$U_s = \frac{v_{th} \cdot N_{st} \cdot (n_s \cdot p_s - n_i^2)}{\frac{(p_s + p_t)}{\sigma_n} + \frac{(n_s + n_t)}{\sigma_p}} \tag{51}$$

where N_{st} is the number of traps per unit area and n_s and p_s the carrier concentrations at the surface. Now, instead of the bulk recombination rate, we are dealing with the recombination rate per unit area expressed in $cm^{-2} \cdot s^{-1}$. Moreover, introducing S_n and S_p the surface recombination velocity of electrons and holes, we can write the recombination rate per unit area as:

$$U_s = \frac{n_s \cdot p_s - n_i^2}{\frac{(p_s + p_t)}{S_n} + \frac{(n_s + n_t)}{S_p}} \tag{52}$$

If we consider that the excess carriers are photogenerated homogeneously within the crystalline silicon volume, this new contribution can be taken into account in the general expression of τ_{eff} by adding a term for the semiconductor surface $\tau_{surface}$. Eq. 43 then becomes:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{surface}} \tag{53}$$

2.2.1.b Effective lifetime

In articles and literature related to passivation topics, we often read about a so-called minority carrier "effective lifetime" instead of just a "lifetime". This is simply because the lifetime is what theory gives us whereas the "effective lifetime" is what we can actually measure. The measured lifetime will then be related to all the recombination processes occurring throughout the whole thickness of the sample by an average population density of excess carrier Δn_{ave} as follows:

$$\sum_i U_i = \frac{\Delta n_{ave}}{\tau_{eff}} \tag{54}$$

where the average excess carrier density within the whole wafer thickness W can be expressed as:

$$\Delta n_{ave} = \frac{1}{W}\int_{-W/2}^{W/2}\Delta n(x)dx \tag{55}$$

Of course, different profiles of Δn(x) can be found throughout the wafer, depending on the wavelength of excitation. We will consider a constant generation rate within the substrate. It is then only true for a monochromatic light with a wavelength close to let's say 1120 nm for c-Si. Because of the c-Si bandgap, any higher wavelength would be lost by transparency whereas a lower wavelength would get us further away from a homogeneous carrier generation. In reality, measurements are made with a white flash light as will be explained later. This will have consequences on the carrier generation homogeneity. Eq. 55 helps us define the overall recombination rate by taking into account both surfaces:

$$\sum_i U_i = \frac{\int_{-W/2}^{W/2}\Delta n(x)dx}{\tau_{bulk}} + S_{eff,front}\cdot\Delta n(W/2) + S_{eff,back}\cdot\Delta n(-W/2) \tag{56}$$

If we consider a perfectly symmetrically passivated wafer, i.e., with the same recombination velocities at both surfaces, we then can keep only one effective recombination velocity S_{eff} since $S_{eff,front}$=$S_{eff,\ back}$. If we assume the generation to be constant, we also have the same excess carrier density generated throughout the whole wafer so that Δn(W/2)=Δn(-W/2). We then have from Eq. 54 and 56:

$$\frac{\Delta n_{ave}\cdot W}{\tau_{eff}} = \frac{\Delta n_{ave}\cdot W}{\tau_{bulk}} + 2S_{eff}\cdot\Delta n(W/2) \tag{57}$$

Hence the following expression for τ_{eff}:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + 2\frac{S_{eff}}{W}\cdot\frac{\Delta n(W/2)}{\Delta n_{ave}} \tag{58}$$

Moreover, after simplification and when considering τ_{bulk} very high (we mainly used FZ wafer), Eq. 58 reduces to:

$$\frac{1}{\tau_{eff}} = 2\frac{S_{eff}}{W} \tag{59}$$

In view of Eq. 59, we can now relate —given some assumptions— the measured effective lifetime of the photogenerated minority carriers to their recombination velocity.

We have seen so far how the c-Si network is organized and how recombination can occur within its bulk and also at its surface. In the next section, we will see how we can measure the effective lifetime of a passivated sample.

2.2.1.c Effective lifetime enhancement strategies

Since the bulk lifetime of our c-Si substrate is very high, our limitation of the overall effective lifetime comes mainly from the surface, according to Eq. 43. The goal of passivation is to reduce the defect density at the substrate surface in order to reduce the impact from the surface on the overall effective lifetime as much as possible. This involves avoiding minority carrier recombination at both interfaces or at least, reducing it. If we consider Eq. 52, there are two possible ways to lower the surface recombination rate. We can either try to lower the electron and hole recombination velocities S_n and S_p by reducing the interface defect density or decrease the amount of carriers n_s and p_s at the surface in order to reduce the $n_s p_s$ product. These two methods are experimentally achievable and are not incompatible.

In order to reduce S_n and S_p, we need to improve the chemical passivation by monitoring the passivating properties of the material deposited on our substrate. To do so, dangling bonds present at the c-Si surface need to be more efficiently saturated by atoms present in the passivating material (Si and H in the case of a-Si:H). Also, all contaminants need to be eliminated thoroughly from the wafer surface upon its wet-chemical preparation. On the other hand, it is possible to reduce the n_s and p_s population at the substrate surface by increasing the so-called *field-effect passivation*. This method although less intuitive, is extremely useful to lower R_s. It consists in the implementation of an internal electric field that will repel only one type of carriers from the interface. By doing so, in this region where trap-assisted recombination mechanisms are more efficient because of the increased defect density, keeping the electrons away from the holes will lead to a decrease in their number of encounters and thus lower their recombining probability. This electric field can be the result of doping profile near the interface. If the dopant used is the same as the substrate's doping type, we obtain a high-low junction. This structure is called *Front Surface Field* or *Back Surface Field*, depending on where it is used in the solar cell architecture[26]. It can also be obtained by using electrostatic charges (SiO_2 or SiN_x) that will act in the same way as explained in 2.1.1, depending on the sign of the charge they generate. One also has to keep in mind that even without these additional charge effects, heterojunction band offsets are by nature dipoles and, thus, create an electric field that contribute to the overall passivating effect of a layer. Therefore, a-Si:H/c-Si heterojunction cumulates several advantages in being able to:

- reduce the interface defect density by saturation of the dangling bonds at the c-Si surface thanks to the a-Si:H material properties,
- separate carriers of opposite signs at the interface because of the band offsets generated by the energy bandgap difference between a-Si:H and c-Si,
- separate even more carriers of opposite signs at the interface thanks to the doping properties of a-Si:H, thus reducing their encountering and recombination all the more.

One has to keep in mind though, that the spatial impact of the electrical fields induced by the band offsets and by field-effect passivation are quite different. Indeed, in the case of a junction, the field will extend over a few hundred nanometers as opposed to a few Angstroms in the case of band offsets. Nevertheless, the effect is not negligible either way since the recombination reduction varies exponentially with the potential induced by the band banding.

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[26] Depending on whether the surface field is implemented on the illuminated side or the back side of the solar cell.

2.2.2 Photoconductance decay measurements

In order to choose the right material to passivate our c-Si substrate and to determine the best process conditions to improve its quality, we need a characterization technique to assess the recombination rate in our sample. The idea of extracting the effective lifetime from contactless photoconductance measurements originated from Albert Rose in 1978[124]. The short light pulses were adequate to measure very low lifetimes. In 1996 however, *Sinton et al*. reported a more flexible technique called Quasi-Steady-State Photoconductance (QSSPC)[125]. The photoconductance decay method can be used to measure the charge carrier effective lifetime. A WCT-120 Sinton lifetime tester was used in this thesis. The experimental setup was placed in a black box to attenuate the impact of the light present in the room. This section will present this method and the assumptions whereon it relies.

2.2.2.a WCT-120 PCD setup and its different operating modes

A thorough description of the setup can be found in [125] by *Sinton and Cuevas* but this is basically how it works: the lamp generates a flash over a semiconducting sample and generates excess carriers within it. The decay constant of the flash is slower than the carrier lifetime. This means that excess carriers can always be considered to be in steady-state, or at least, very close to it: generation and recombination rates are in balance. Simultaneously, the setup measures a voltage, which relates to the sheet conductivity of the sample, all the while monitoring the intensity of the flash in time. This is made possible thanks to an RF coil inductively coupled to the sample and a calibrated light sensor placed in the substrate holder. This measured voltage will indeed vary in time and be proportional to the difference in the conductance induced in our sample by the flash and its decay, as expressed by Eq. 60.

$$\Delta\sigma = q \cdot W \cdot \Delta p_{average} \cdot (\mu_e + \mu_h) \tag{60}$$

where q is the elementary charge, W the wafer thickness, $\Delta p_{average}$ the excess hole density in the wafer and μ_e and μ_h the electron and hole mobilities, respectively. This sheet conductivity is then converted into an average excess carrier density Δn at each stage of the measurement. On the other hand, the measured flash intensity is converted into the generation rate of carriers G(t) in $cm^{-3} \cdot s^{-1}$ in the sample. The expression of τ_{eff} as a function of σ and G is given by Eq. 61:

$$\tau_{eff} = \frac{\Delta p}{G - \frac{d\Delta p}{dt}} \tag{61}$$

Three operating modes arise from this equation:

i) $$G >> \left| \frac{d\Delta p}{dt} \right| \tag{62}$$

In this case the illumination decay is much longer than the effective lifetime of the sample and Eq. 61 becomes:

$$\boxed{\tau_{eff} = \frac{\Delta p}{G}} \tag{63}$$

Mode i) is called the ***Quasi-Steady-State*** regime (QSS) and we have $\tau_{flash} >> \tau_{eff}$. This mode is adequate for short lifetimes, i.e., <200µs since the pulse of light is much longer (~1 ms). Of course, in this case, illumination must be measured at all times and an optical factor (f_{opt}) must be defined to account for the reflectivity of the sample surface. [29]. Mode ii) is defined by:

$$\text{ii)} \qquad G << \left| \frac{d\Delta p}{dt} \right| \tag{64}$$

In this case, the illumination decay time is much shorter than τ_{eff}. Eq. 61 then becomes:

$$\boxed{\tau_{eff} = -\frac{\Delta p}{\frac{d\Delta p}{dt}}} \tag{65}$$

Mode ii) is called the ***Quasi-Transient*** regime (QT) and we have $\tau_{flash} << \tau_{eff}$. This mode uses very short light pulses (~1 µs). Finally, mode iii) is defined by

$$\text{iii)} \qquad G \approx \left| \frac{d\Delta p}{dt} \right| \tag{66}$$

In this case, the illumination decay time is of the same order as τ_{eff}. As a result, Eq. 61 then becomes:

$$\boxed{\tau_{eff} = \frac{\Delta p}{G - \frac{d\Delta p}{dt}}} \tag{67}$$

Mode iii) is called the ***Generalized*** regime (G) and we have $\tau_{flash} \approx \tau_{eff}$. In most cases, the Sinton tester was used in the *generalize* mode which do not rely on any approximation of the expression in Eq. 61. After checking that the approximation of case ii) did not affect the measurement, the transient mode was used to carry out fast averages over 10 measurements to minimize the noise. The optical constant was set to 0.7 for double-side polished (DSP) substrates while for textured wafers, the latter was increased to a value of 0.8. For more details on the effective lifetime formalism, the reader is referred to a more complete study by *Brody et al.* [126].

2.2.2.b Extraction of the implied open-circuit voltage (iV$_{OC}$) from PCD measurements

From the effective lifetime measurements, we can also extract a value called implicit open-circuit voltage or iV$_{OC}$. Indeed, since the V_{OC} should be equal to the Fermi level splitting under an illumination of 1 Sun, it can be expressed as:

$$Voc = \frac{E_{Fn} - E_{Fp}}{q} = \frac{kT}{q} \ln\left(\frac{n_e \cdot n_h}{n_i^2} \right) \tag{68}$$

For an n-doped wafer of donor density N_D, we have $n_h = \Delta p$ and $n_e = N_D + \Delta p$. The V_{OC} then becomes:

$$Voc = \frac{kT}{q} \ln\left[\frac{(N_D + \Delta p) \cdot \Delta p}{n_i^2} \right] \tag{69}$$

Thus, from the measurement of Δp at 1 Sun, it is possible to assess the maximum theoretical value of the V_{OC} of the future device. This is very practical since, when fabricating a SHJ solar cell, apart from assessing the effective lifetime of the unfinalized device, we will be able to know the upper limit of the device final V_{OC}. Indeed, this estimate should give the best theoretical V_{OC} value our solar cell could reach if the remaining fabrication steps (antireflective coating deposition, metallization) had no impact on the cell performance and if there were no losses associated with resistances and transport. This is obviously never true but the iV_{OC} will however indicates our upper limit of the final V_{OC} and help us determine which solar cell precursor is more likely to give the highest final V_{OC} value. Actually, we usually noticed a -15 mV difference with the iV_{OC}. However, this allows us to filter the precursors before finalization thereby saving a lot of time and effort.

Chapter Key facts

In this chapter, we had the opportunity to tackle the concept of passivation. This led us to review the materials that could be used to passivate the crystalline silicon surface and how they were implemented in solar cell architectures. As a result, we could understand how innovative the a-Si:H/c-Si heterojunction structure is because of the doping properties of a-Si:H, which allows for surface passivation and contacting at the same time. The (100) and (111) orientation of c-Si were described to prepare for the challenges related to the transfer from flat to textured substrates. Finally, the effective lifetime formalism was adjusted to describe surface recombination while the different operating modes of the Sinton setup were presented. We are now ready to move forward to our main goal: c-Si texturing and passivation by a-Si:H.

3 Passivation of chemically wet-textured crystalline n-type wafers using hydrogenated amorphous silicon deposited by low-temperature PECVD

3.1 Texturation of crystalline silicon

In solar cells, there are two main types of losses that can lower conversion efficiency: electrical and optical losses. Optical losses can be reduced by the use of antireflective coatings as it is already the case in most solar cell architectures. These can also be reduced by surface texturing. Indeed, as can be seen in Figure 3-1, between 400 nm and 1100 nm, more than 35% of the light is reflected by the c-Si surface, on average.

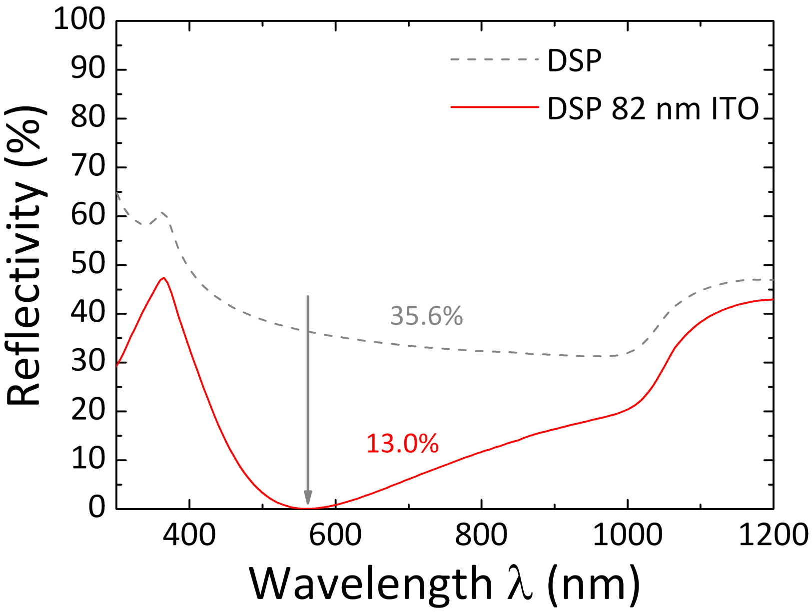

Figure 3-1 – Reflectivity of a DSP c-Si wafer, with and without an antireflective layer (ITO).

Even when adding a standard antireflective coating like ITO, the average reflectivity remains quite high, i.e., close to 13%. By texturing the surface of c-Si wafers, light absorption into the device is enhanced. The light impinging on a randomly textured surface experiences multiple reflections on the surface and is partially absorbed upon each reflection. This generates a mechanism known as *light-trapping*. This effect is shown schematically in Figure 3-2. Thanks to this, the hemispherical reflectance, i.e., the total reflectance on half of the solid angle is minimized. As a result, the reflectivity of a c-Si wafer is decreased to values close to 10% prior to adding an antireflective coating, as further study will show. It is presently a generalized technique in c-Si solar cell processing both to increase coupling of the light into the cell and to decrease the surface reflectivity [127][128] of the light that usually escapes[129][130]. In the case of silicon-based solar cells, the light absorption increase will enhance the photogeneration, since more photons can be used to excite electron-hole pairs. As a result, the EQE will increase and so will the J_{SC}. There are several ways of obtaining a textured c-Si surface. This chapter will go into more details on how we can texture crystalline silicon and on the different techniques used by the PV industry. This study will conclude on the definition of adequate texturation recipes to lower the reflectivity of our c-Si wafers. The impact of this newly textured surface on passivation will be examined by different characterization techniques and will lead to a new paradigm for anisotropically-etched c-Si wafers. However, we will see that in order to optimize c-Si HJ solar cells, we rely on reflectivity measurements solely.

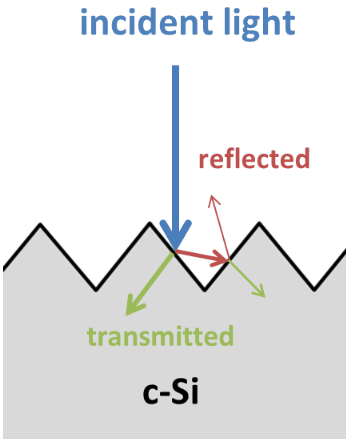

Figure 3-2 – Schematic representation of the impact of c-Si texturing on the trapping of a light beam.

Indeed, advances made by texturing c-Si wafers will have to be put in perspective of surface passivation by a-Si:H. In this way only will we be able to get high effective lifetimes and VOC values, and eventually achieve higher conversion efficiencies.

3.1.1 Bulk etching of crystalline silicon

Texturing of silicon is obtained by removing significant amounts of material in a selective fashion. This is sometimes done for undercut-etching of Si structures[131] or to pattern the Si surface with trenches, holes, or other micrometer-scale structures[132][133][134]. Even though etching processes for silicon very often require a quite aggressive chemistry, they can be compatible with on-chip circuitry and microelectronic devices when designed accordingly. This has actually allowed the fabrication of CMOS circuits[135]. Silicon bulk *etching* or *micromachining* can either be *isotropic*, i.e., yielding rounded shapes due to equal etch rates in every crystallographic direction, or *anisotropic*, i.e., exhibiting sharp angles and flat surfaces due to crystallographic direction-dependent etch rates. The isotropic or anisotropic nature of an etchant is determined by the chemical interactions it will have with the crystalline silicon lattice. Indeed, the nature of the etchant, the diffusion of the reactants and products in the medium, as well as the shapes and size of the masks that are used have huge impacts on the final patterning schemes of the silicon surface. Another way to classify etching techniques is by the physical phase in which the reactants are when operating the etching process. Indeed, etching of crystalline silicon can be carried out in a liquid phase (*wet etching*), in plasma-less gaseous phase (*vapor dry etching*) and in plasma phases (*plasma dry etching*). The chemistries involved in all of these etching processes are quite different, even for one phase. However, all silicon etching reactions include one crucial element: a change in the oxidation state of silicon through redox reactions. This indeed, will lead to the formation of compounds that can then be removed away from the substrate surface. These reactions can be modulated by *internal* (Si doping level) as well as *external* parameters (electrochemical biasing). In plasma-less-gas phase or vapor phase, chemical reactions are made possible by the adsorption of halogen reactants which will dissociate into reactive species. As a result, these will react with the silicon surface and form volatile silicon compounds[136]. These kinds of etchants are usually isotropic and their rate will be determined by the diffusion of the species from site to site and in the gas phase. As in the case of wet etching, etching in vapor phase can be modulated by an external source of energy, even optically. In the gas phase, one can also break halogen gas molecules by applying a bias under vacuum. This will ignite a plasma, which will sustain the creation of highly reactive halogen radicals within the vacuum chamber. These will in turn be able to react with the silicon surface to form volatile silicon compounds and, thus, lead to the etching of silicon. One of the main advantages of plasma etching is that it uses fresh chemicals for each etch. Indeed, the vacuum chamber is constantly being pumped down via a process pump, while gases keep on entering the chamber. Moreover, plasma etching can be enhanced by tuning bombardment effects induced by energetic ions. It can also be isotropic as well as vertically anisotropic, allowing for the patterning of narrow lines in a very specific way. Another distinguishable feature of plasma etching is the tunability of the chemistry during the etching process. This allows for in-situ control of the anisotropy. Among all these etching techniques, different wet-chemical etching techniques were explored. They will be described more thoroughly in the following sections.

3.1.2 Wet etching

As stated earlier, wet chemical etching of silicon can be isotropic or anisotropic. In both cases, it is an electrochemical process. Therefore, it involves electron transfer processes as part of the reactions taking place at the silicon surface. In electrochemistry, oxidation describes the process leading to the loss of an electron. As a result, the net positive charge of the species will increase (higher oxidation number). Contrariwise, reduction describes the process of electron gain, i.e., a decrease in the net positive charge (lower oxidation number). Wet etching is governed by oxidoreduction (or redox) reactions, i.e., by simultaneous oxidation and reduction reactions of species. For wet etching processes, which rely almost exclusively on aqueous chemistry, oxidation of silicon is usually done using acids and bases, which are highly reactive. In the case of isotropic and anisotropic etching, the process typically involves i) the transport of reactants to the surface, ii) surface reactions and iii) the transport of products from the surface. To generate the reactions necessary for the etching of the silicon material, several chemicals are needed in the etching chemical bath. Typically, there are three main ingredients in such a process. An oxidizer is needed to oxidize the silicon surface. It can be hydrogen peroxide (H_2O_2) or nitric acid (HNO_3) for example. An acid or a base is then needed to dissolve the oxidized surface. For this, sulfuric acid (H_2SO_4) or ammonium hydroxide (NH_4OH) for example can be used. To transport the reaction products from the surface, a diluting medium is then needed. Water or some other diluent such as acetic acid (CH_3COOH) can play this role[137]. This section is dedicated to the study of texturing techniques which will lead us to define adequate recipes for the passivation of textured c-Si wafers by a-Si:H deposited by PECVD.

3.1.2.a Isotropic wet etching of silicon

A classical recipe to etch silicon istropically is HNA, containing hydrofluoric acid (HF), nitric acid (HNO_3) and acetic acid (CH_3COOH)[138][139][137][140][141]. A redox reaction occurs, which leads to the formation of an oxide. The latter is dissolved by hydrofluoric acid (HF), the same acting as a complexing agent. The overall chemical reaction taking place is[142]:

$$3Si + 4HNO_3 + 18HF \rightarrow 3H_2SiF_6 + 4NO_{(g)} + 8H_2O \tag{70}$$

In fact, during the reaction, the Si surface becomes randomly covered with oxidation and reduction sites.

On anode sites, silicon atoms get promoted to a higher oxidation state, following the "hole-injection" reaction:

$$Si^0 + 2H^+ \rightarrow Si^{2+} \tag{71}$$

On cathode sites on the other hand, NO_2 from nitric acid is reduced, thus producing free holes, as per the reaction:

$$2NO_2 \rightarrow 2NO_2^- + 2H^+ \tag{72}$$

Naturally, HNO_3 will dissociate in water following a classical deprotonation reaction. However, NO_2 is effectively the oxidizing factor since HNO_2 and protons are produced in an autocatalytic cycle:

$$\begin{aligned} &HNO_2 + HNO_3 \rightarrow N_2O_4 + H_2O \\ &N_2O_4 \leftrightarrow 2NO_2 \leftrightarrow 2NO_2^- + 2H^+ \\ &2NO_2^- + 2H^+ \leftrightarrow 2HNO_2 \end{aligned} \tag{73}$$

In this way, HNO_2 is constantly regenerated allowing for constant production of protons for the oxidation of Si as shown in Eq. 71. Oxidation will thus be controlled by the amount of undissociated HNO_3. At this point, Si^{2+} ions can react with OH^- ions to form silicon oxide SiO_2, as per the reactions:

$$Si^{2+} + 2OH^- \rightarrow Si(OH)_2 \tag{74}$$

$$Si(OH)_2 \rightarrow SiO_2 + H_2O \tag{75}$$

Hydrofluoric acid can then dissolve the silicon oxide and complexify into H_2SiF_6, as per the reaction:

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \tag{76}$$

Acetic acid is present in the HNA etching recipe as a diluent to replace water. Acetic acid has a lower dielectric constant than water (6.15 versus 81 for H_2O in the liquid phase) and this particular feature will allow for a weaker dissociation of HNO_3 into NO_3^- and NO_2^-. As we will later see, the oxidation step is controlled by the amount of undissociated HNO_3, hence the importance of replacing water by acetic acid. Moreover, acetic acid is less polar than water, enhancing the wetting of silicon which tends to be slightly hydrophobic. To sum-up, all oxidation and reduction sites will act as localized electrochemical cells with quite high corrosion currents, i.e., close to 100 A/cm². Eventually, each one of these sites turns into anode and cathode sites over time, alternatively. Isotropic etching is obtained when each point on the surface goes through the etching process as an anode and a cathode, equally in time. Otherwise, anisotropic etching will take place instead. Three cases of isotropic etching can be considered however, depending on the respective concentration of the bath's three ingredients: i) if the HF concentration is high, the etch rate will be controlled by the HNO_3 and limited by the oxidation process, ii) if the HNO_3 concentration is high, the etch rate will be controlled by the HF, leaving a residual SiO_2 layer, iii) if we are in excess of H_2O, then the etch rate will not be impacted unless the HF and HNO_3 are in 1:1 proportions. A typical formulation for HNA comprises 250 ml HF, 500 ml HNO_3 and 800 ml CH_3COOH, yielding an etch rate of 4-20 µm/min at RT. Figure 3-3 shows the typical patterns obtained after isotropic texturing of c-Si, with and without stirring. As can be seen, even if the mask prevents the surface from being etched homogeneously, the round features show that etching occurs in every direction.

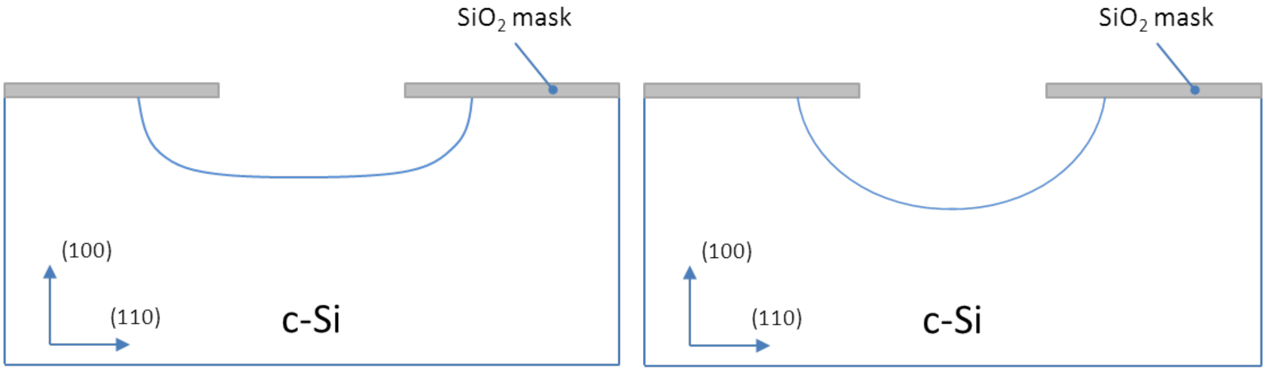

Figure 3-3 – Schematic representation of isotropic wet etching of c-Si masked with SiO2, without agitation (left) and with agitation (right).

To summarize, in order to etch isotropically, we need a source of OH- ions and a complexing agent. Since the etching process relies on oxidoreduction reactions, one can easily see that the same can be modulated by the doping level of the c-Si substrate as well as by external biases.

3.1.2.b Anisotropic wet etching of silicon

Anisotropic etching of silicon started in the 60s, whilst looking for a method to lower the reflection losses of photovoltaic devices and of semiconductors in general[143][144][145]. Etching rates are very sensitive the crystalline orientation. This difference stems from the fact that silicon atoms, having four electrons which repel each other, form in a tetrahedral configuration, known as sp^3 hybridization. Because of the diamond structure of the silicon lattice, the (100) surface will exhibit two DBs from each silicon atom, as explained in 2.1.3.a. These surface atoms will be bonded to two Si atoms in the bulk. On the other hand, the (111) surface exhibits one DB from each silicon atom as shown in 2.1.3.b. As a result, each silicon atom at the surface is bonded to 3 silicon atoms in the bulk. Because of this, it will be much harder for hydroxyl ions to attack the silicon surface if 3 bonds need to be broken. Consequently, the etch rate is greater for (100) than for (111) wafers and we observe a general (111)<(100)<(110) trend.

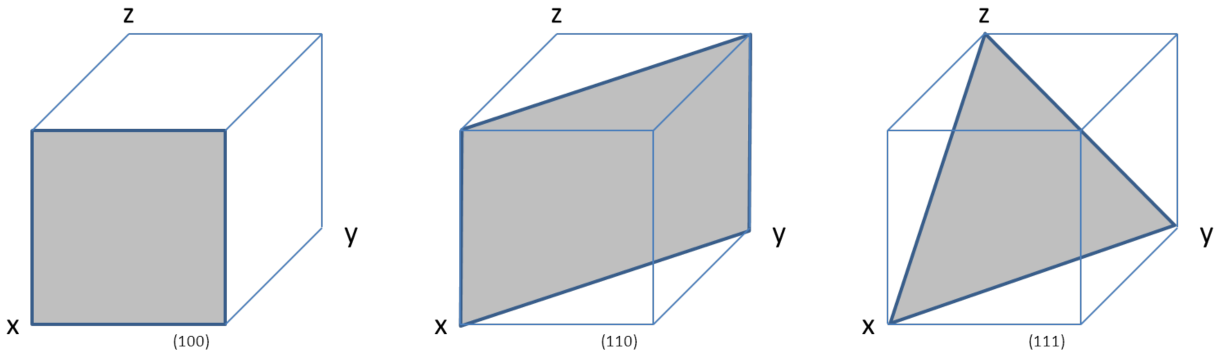

Figure 3-4 – (100), (110) and (111) crystallographic planes of silicon.

In fact, the etching rate along the (111) orientation is so low that it can sometimes be considered as negligible when texturing c-Si wafers, especially for short texturing times. Table 3-1 shows the dependence of the silicon etch rate in different KOH solutions at 70°C, as a function of its crystalline orientation. In parentheses are given the values normalized by the etch rate along the (100) orientation. As can be seen, the etching rates vary substantially and almost independently from the alkaline solution concentration, the etch rate along the (111) direction is very slow.

Crystallographic orientation	Etching rate [$\mu m \cdot min^{-1}$]		
	30%	40%	50%
(100)	0.797 (159)	0.599 (66)	0.539 (60)
(110)	1.455 (291)	1.294 (144)	0.870 (97)
(111)	0.005 (1)	0.009 (1)	0.009 (1)

Table 3-1 – Silicon etch rates at 70°C as a function of the crystalline orientation and KOH concentration. Taken from [146].

This allows for obtaining very well-defined landscapes. In particular, when intersecting the 8 (111) planes present along the ±x ±y ±z unit vectors (Figure 3-5), we generate pyramids and grooves between these, and, as a result, the surface becomes covered with pyramids of randomly distributed sizes but of identical shape, as seen in Figure 3-6.

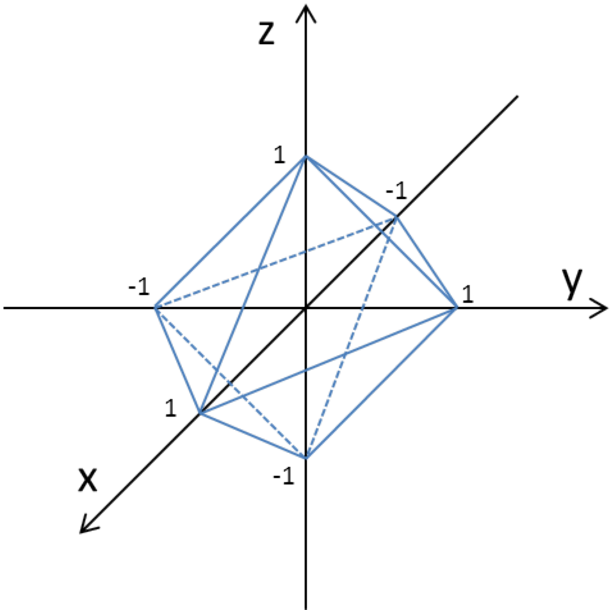

Figure 3-5 – All 8 {111}-oriented planes of c-Si.

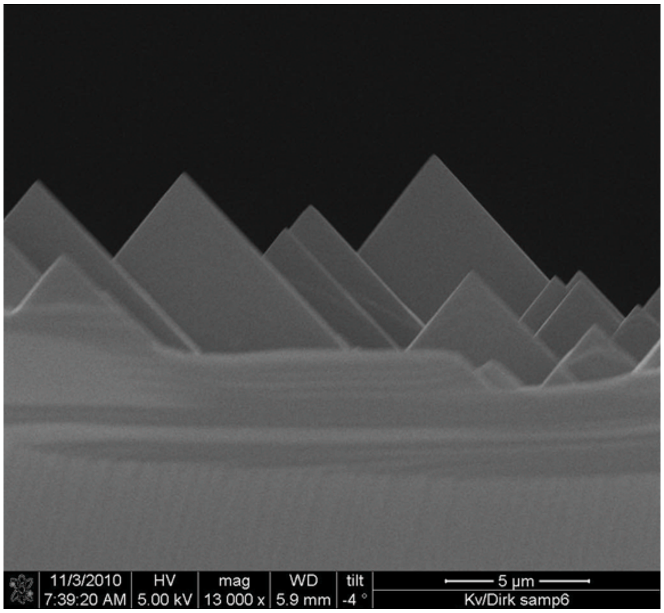

Figure 3-6 – SEM image of c-Si surface landscape after texturation in a KOH-IPA solution.

Figure 3-7 shows in detail how anisotropic etching operates. Etching a (100)-oriented silicon surface through the rectangular hole of a masking material such as SiO_2 results in a pit surrounded by {111}-oriented sidewalls and a flat (100)-oriented plane (Figure 3-7a)). The sidewalls are at 54.7° angle to the wafer surface. Etching will continue on the flat (100) plane at the same pace whereas etching will also take place on the {111}-oriented sidewalls but at a much lower rate. Etching virtually "stops" when the flat (100) plane disappears, resulting in a V-shaped section on the c-Si wafer, as shown in Figure 3-7b). Because of the non-zero etch rate in the (111) direction, the silicon wafer needs to be taken out of the solution to effectively suppress all etching process. In the meantime however, a thin part of the {111}-oriented sidewalls are etched, yielding an undercut δ defined by:

$$\delta = \frac{\sqrt{6}D}{S} \qquad (77)$$

where D is the etching depth and S the anisotropy ratio.

Considering D=R_{100}·t and S=R_{100}/R_{111}, where R_{xyz} and t are the etch rates in the <xyz> direction and in time, respectively, we can rewrite Eq. 77 as:

$$\delta = \frac{\sqrt{6} R_{100} t}{R_{100} / R_{111}} = \sqrt{6} R_{111} t \qquad (78)$$

For example, for 30%-dilute KOH at 70°C, the data taken from Table 3-1 yield a δ value of δ=√6·0.005·t≈0.01·t µm. Even though reaction mechanisms are well-known today, anisotropic etching along crystal planes cannot be explained. Indeed, it was thought that the etch rate was directly dependent on the density of atoms on the surface. However, in some cases as the diamond structure for example, the surface density of atoms does not vary substantially with the crystallographic orientation. H_2O molecules could be responsible for part of the anisotropy that we experience by screening some part of the surface, thus preventing the etchant from reaching the crystalline silicon bulk. As shown earlier in Table 3-1, etch rate for the (111), (110) and (100) crystalline orientations varies markedly. Indeed, relative etch rates with regard to the (111) orientation range from 60 to 159 and from 97 to 291 for the (100) and (110) orientations, respectively, while decreasing the KOH concentration. Moreover, etch rates vary a lot with other parameters, such as temperature. (111)-relative etch rate values as high as 400[147] and 600[148] have been reported for the (100) and (110)-oriented surfaces, respectively. As a result, it is hard to predict the behavior of an etchant with absolute certainty. Even if some models have been developed[149], most of the time research groups prefer to define their own conditions by measuring the etch rate and other useful parameters through experimental studies and by relying on literature data. For example, one can perfectly refer to the data published by *Williams and Muller* in 1996. They indeed have studied thoroughly 317 combinations of 16 materials that are used in the fabrication of microelectromechanical systems (MEMS) and integrated circuits and the interaction thereof with 28 different etching recipes (wet, plasma, plasmaless-gas-phase)[142]. Today, surface texturation of (100)-oriented crystalline silicon wafers is a commonly used technique in the solar cell industry to reduce optical losses induced by reflection. The most successful approaches are based on the use of alkaline solutions[150][151]. Other techniques however contain completely different chemical compounds, as we will see.

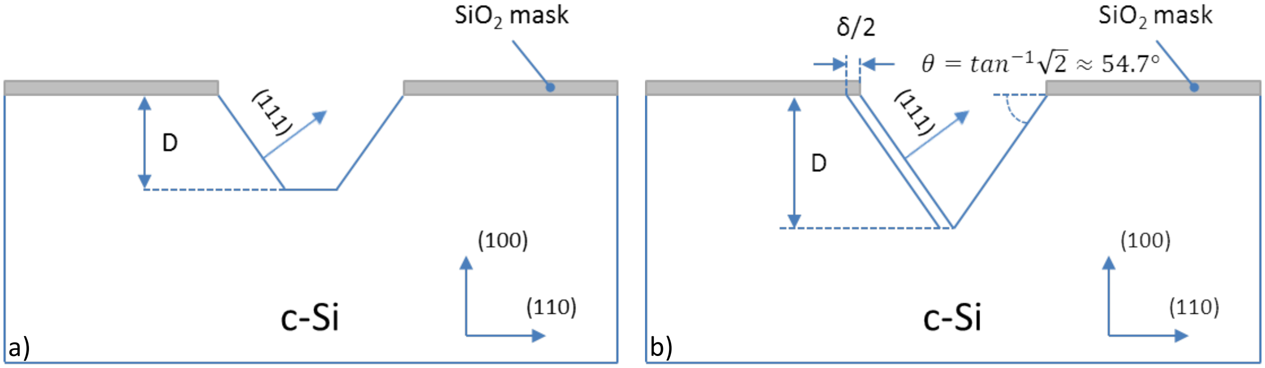

Figure 3-7 – Schematic representation of anisotropic etching of c-Si covered with an SiO_2 mask.

Hydrazine

Among these, hydrazine (N_2H_4) mixed with water was a pioneer in the late 60s. By mixing such in 1:1 proportions, etching rates close to 2µm/min could be obtained at a temperature of 100°C. However, a replacement was needed since this solution is very hazardous. Indeed, hydrazine is a very powerful reducing agent used for rocket fuel. Thus, it is a very flammable liquid (flashpoint at 52°C in air) and has pyrophoric[27] and hypergolic[28] properties, which make it not very easy to handle.

EDP

Likewise, Ethylene Diamine Pyrocatechol (EDP), also known as Ethylene diamine – Pyrocatechol – Water (EPW) can be used to etch silicon since it displays a <100>/<111> selectivity of 17 and can be masked by many materials like SiO_2, Si_3N_4, Au, Cr, Ag, Cu and Ta. It also displays a high selectivity between lightly-doped and heavily boron-doped (p-type) silicon[152]. Despite its typical (100) oriented silicon etch rate of 0.5 µm/min at 110°C[144], it requires a reflux condenser to keep volatile compounds from evaporating. Hence, a fume collecting bench is required for this process alone. This has prevented this process from being more widely used in microelectronics. Moreover, it is very corrosive and will cause any metal in the solution vicinity to rust. It also often induces in the formation of silicon hydroxide ($Si(OH)_4$) which is quite unstable and may rapidly polymerizes to form more complex molecules such as $Si_2O(OH)_6$ or $Si_3O_2(OH)_8$. Even if there is a way to avoid this effect by using additional chemical baths, its high carcinogenic action has made this compound quite unpopular for silicon etching.

Amine Gallates

A much safer solution consisting of gallic acid ($C_6H_2(OH)_3COOH$), ethanolamine (C_2H_7NO), water, pyrazine ($C_4H_4N_2$) and a surfactant was developed, yielding a <100>/<111> selectivity of 50-100 with an etch rate up to 2.3 1.7 µm/min on (100) Si[153]. The etchants have the distinctive characteristics of being stable for at least six months at RT. On the contrary, a slight etch rate increase is experienced and this is thought to be due to the slow formation of gallotannin catalysts. Similarly to EDP, it is also sensitive to high boron concentrations (>3E19 atoms/cm^2). Moreover, it yields good uniformity and the gallate etch product does not precipitate, a major problem for the disposal of EDP. It is quite similar to EDP in terms of etching and masking, but much safer. It is possible to increase the etch rate with the help of some additives like pyrazine. However, this will also induce the surface roughness to increase.

Alkaline-based etchants

In general, hydroxides of all alkali metals can be used as anisotropic etchants for bulk silicon. Indeed, they usually exhibit an etch rate dependence with respect to the crystalline orientation. Among the KOH, NaOH, CsOH[154][155], RbOH[156], etc. etchants, the most commonly retained is KOH. Other alkali-free etchants such as NH_4OH or $(CH_3)_4NOH$ (TMAH) are also used to avoid alkali contamination in clean-rooms during the fabrication of transistors, for example. While the precise mechanisms taking place during

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[27] Ignites spontaneously in O_2.

[28] Ignites spontaneously in hydrogen peroxide.

etching in alkaline solutions are not entirely known, it is commonly accepted that the etching occurs in three main reactions., The process of KOH etching in particular has been described by *Seidel et al.*[157]. Since all anisotropic etchants for silicon are basic, we can refer to this example. Firstly, the silicon surface is oxidized by OH^- ions to produce Si^{2+} ions, as per the reaction:

$$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^- \tag{79}$$

The four electrons produced move into the silicon crystal, where they stay in the conduction band. These can then participate in the water reduction, thus producing molecular hydrogen, which moves away from the surface in the form of bubbles:

$$4H_2O + 4e^- \rightarrow 4H_2O^- \tag{80}$$

$$4H_2O^- \rightarrow 4OH^- + 2H_2 \tag{81}$$

OH^- ions are regenerated. In this way, the process described in Eq. 79 can start again and the etching can continue. This is all the more true than the doping of c-Si remains low. Indeed, in such cases, electrons will be able to have a high lifetime before recombining, resulting in a higher probability of participating in the reaction described by Eq. 80. At this point, we can clearly understand the electrochemical aspect of the process. By doping the c-Si substrate even more, recombination processes can be increased, thus preventing reaction 80 from taking place. This is, in fact, how one can stop the etching process, i.e., by increasing the electron recombination (*p+ etch stop*). Another way to control the etching is to remove the electrons from the c-Si surface by applying an electrical bias (*electrochemical etch stop*). After the oxidation of silicon (reaction described in Eq. 79), silicon is no longer part of the crystalline bulk but is attracted to the c-Si surface (negatively charged by the electrons stored at the interface) in the form of $Si(OH)_2^{2+}$ cations, because of the latter's positive charge. They further react with OH^- anions to form a water-soluble silicon complex as per the reaction:

$$Si(OH)_2^{2+} + 4OH^- \rightarrow SiO_2(OH)_2^{2-} + 2H_2O \tag{82}$$

The $SiO_2(OH)_2^{2-}$ ions produced being negatively charged, they are naturally repelled from the c-Si surface since they are soluble in the etchant. As a result, the overall redox reaction is:

$$Si + 2OH^- + 2H_2O \rightarrow Si(OH)_2^{2-} + 2H_2 \tag{83}$$

Generally, concentrations of KOH in the range of 40-50 wt% are used to minimize the surface roughness and to avoid the formation of insoluble precipitates. However, many proportions can be used at different temperatures to obtain either slow or fast etching. Also, the smoothness of the resulting silicon surface can be controlled by adjusting the proportions to obtain higher or lower (100):(110):(111) relative etch rates. Table 3-2 shows the etch rate of (100)-oriented silicon surfaces as a function of the KOH concentration and of temperature. Even though high etch rates can be achieved at a low KOH concentration, it is recommended to use higher concentrations to minimize the surface roughness. The typical recipe is the one reported by *Williams and Muller*: 50 wt% KOH at 80°C with an etch rate of 1.4 µm/min[142]. It is possible, however, to tune the etching properties of KOH solution with adequate additives. *Price* showed that adding isopropyl alcohol (IPA) was beneficial for the etchant selectivity[158]. Indeed, IPA is far less polar than water, allowing for an enhanced wettability of the silicon surface.

Etching recipe	Temperature [°C]	Etch rate [$\mu m \cdot min^{-1}$]	Reference
15%KOH:85%H_2O	72	0.9	[149]
20% KOH:80% H_2O	20	0.025	[159]
	40	0.188	
	60	0.45	
	80	1.4	
	100	4.1	
30% KOH:70% H_2O	20	0.024	[159]
	40	0.108	
	60	0.41	
	80	1.3	
	100	3.8	
40% KOH:60% H_2O	20	0.020	[159]
	40	0.088	
	60	0.33	
	80	1.1	
	100	3.1	
44% KOH:56% H_2O	120	5.8	[160]
50% KOH:50% H_2O	70	0.5	[146]
	80	1.4	[142]

Table 3-2 – (100) c-Si etch rates in KOH solutions as a function of concentration and temperature.

As a result, the hydrogen bubbles formed during reaction 81 and which could be sticking onto the silicon surface, move away. This is why stirring and high temperature are often required during texturing in KOH[161]. Although IPA decreases the etch rate[162], it improves the texturing uniformity required in the case of silicon-based solar cells. Under typical texturing conditions, a high IPA concentration is required to obtain a high uniformity[163]. However, IPA is volatile and must be used very often above or at least close to its boiling point (~82°C) to achieve reasonable etching rates, as seen in Table 3-3. As a result, IPA, which is already an expensive product, must be constantly added to the solution to compensate for the losses and to keep the same reactant proportions throughout the whole etching process. Low-cost alternatives are under investigation to reduce the amount of IPA in texturing solutions using chemical compounds such as tetramethyl ammonium hydroxide (TMAH)[164], tribasic sodium phosphate[165], sodium phosphate (Na_3PO_4). *Nishimoto et al.* even demonstrated the IPA-free texturation of silicon surfaces using sodium carbonate (Na_2CO_3)[166]. In the next section, we will discuss the case of ammonium hydroxides.

Etching recipe	Temperature [°C]	Etch rate [$\mu m \cdot min^{-1}$]	Reference
20% KOH: 80% 4 H2O:1 IPA	120	5.8	[160]
23.4% KOH:63.3% H2O:13.3% IPA	80	1	[158]

Table 3-3 – KOH-IPA solution etch rates as a function of concentration and temperature.

Ammonium hydroxides

The main advantage of replacing alkali-based etchants is the simple fact that they do not contain alkali ions. Potassium and sodium in particular are extremely detrimental for the electronic properties of materials used in microelectronic devices such as transistors. As a result, they have been banned from clean-rooms. However, even if a KOH-treated wafer cannot be processed in a CMOS line, it is possible to organize the process in such a way that KOH etching takes place at the end of the fabrication chain. Using other etchants such as ammonium hydroxides can also be a solution. In 1978, the first use of NH_4OH for the etching of (100)-oriented silicon was demonstrated by *Kern*[167]. Later, *Schnakenberg et al.* published a more thorough study on this etchant[168]. A maximum etch rate of 0.5 µm/min, an important surface roughness (hillocks) and the evaporation of ammonia gas were reported. Indeed, the etch rate remains quite low compared to what can be obtained with conventional alkali-based etching solutions. This is one of the reasons why ammonium hydroxide has not replaced those. However, by combining ammonium hydroxide with less volatile compounds we can lower its evaporating effect. A quaternary ammonium hydroxide, $(CH_3)_4NOH$ or tetramethyl ammonium hydroxide (TMAH) has become essential to the fabrication of MOS transistors. It can be manipulated in clean-rooms since it does not contain sodium or potassium. But we are far from the 200-600 (111)-relative etch rate selectivity presented earlier in Table 3-1. For 10-40% TMAH it is in the range of 10-35, corresponding to etch rates between 0.5 and 1.5 µm/min at 90°C[135]. Just as in the case of KOH, low concentrations tend to increase the surface roughness, which is why concentrations above 20 wt% are usually chosen. The advantages of TMAH must be sought in its compatibility with the fabrication of microelectronic devices. Indeed, apart from its alkaline-free feature, typical masking materials such as silicon dioxide or silicon nitride are quite stable in the presence of TMAH and exhibit very low etch rates[168][169][170]. Moreover, TMAH exhibits boron-doping dependent stop-etch properties[171] which can yet be enhanced by adding IPA[172]. Finally, the pH of TMAH can be tuned by adding silicon[173] or even silicic acid (H_4SiO_4)[174] to the etching solution. Lowering the solution pH enhances the selectivity toward aluminum. TMAH seems like a good candidate for c-Si texturation, although its main advantages are directed towards microelectronic devices. One of the possible benefits of using TMAH for silicon HJ solar cells would be to avoid the possible contamination of the a-Si:H/c-Si interface by alkaline metals like potassium or sodium[175][164]. We will see, however, that an adequate cleaning recipe allows for the use of KOH solutions without any contamination problems.

From this review of c-Si texturing, we conclude that the texturing of our c-Si wafers to decrease their reflectivity requires anisotropic texturing. This can be achieved either via dry or wet etch processes. Texturing of c-Si could be obtained by RIE to decrease the reflectivity. However, the same remained too high, i.e., close to 20%, compared to what could potentially be obtained by wet-texturing, i.e., closer to 10-13%. Moreover, this resulted in quite porous Si materials. As a result, we could not obtain good passivation on such samples. Indeed, the effective lifetimes were never found to be greater than 50 µs. Wet-chemical texturing on the other hand has already been successfully applied to solar cell fabrication[176][4][177][13]. Moreover, as we will see, their reflectivity can effectively be decreased and high effective lifetimes can be reached using such a technique.

3.1.3 Wet-texturing recipes for a-Si:H/c-Si heterojunction solar cells

As stated earlier, alkali-based texturing solutions became our first choice to obtain textured c-Si wafers. The goal of this thesis being the optimization of passivation of textured c-Si silicon, we decided to go for the classical KOH etchant solution. Since the use of IPA was the main drawback of the KOH etchant, two types of etch solutions were studied: a classical KOH-IPA solution and a KOH/surfactant solution wherein an industrial surfactant (RenaTex) replaces IPA. For the sake of simplicity, wafers processed in KOH-IPA solutions with no additional processing (chemical rounding for example) were denoted **KIno**, where *'K'* and *'I'* stand for *'KOH'* and *'IPA'*, respectively, whereas 'no' shows explicitly that no further processing was carried out on the substrate. Similarly, wafers that underwent KOH/RenaTex texturing with no additional processing were denoted **RTno**, where *'RT'* stands for RenaTex.

3.1.3.a Saw-damage removal

In research and in the PV industry, texturation can be done on different initial surfaces: polished, etched or as-cut (after ingot wire-cutting). Many laboratories actually use polished (100)-oriented c-Si wafers. However, very often an increase in roughness is required as a first step, which can be accomplished via ultra-sonic (US) waves. *Papet et al.* reported the need for a 20-min treatment prior to texturation, mentioning also that for as-cut wafers, stirring in US waves was useless[164]. Indeed, as can be seen in Figure 3-8, the manufacture of wafers by multi-wire sawing of silicon ingots generates a mechanically damaged surface, which appears from the top as a naturally homogeneous roughness. Its mean height was measured by Laser-Scanning Microscopy (LSM) to be 1.98 µm on average with the highest points just below 4 µm.

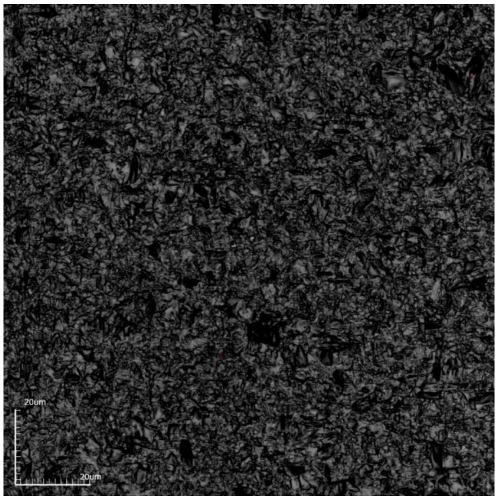


Figure 3-8 – SEM image (top view) of an as-cut silicon wafer.

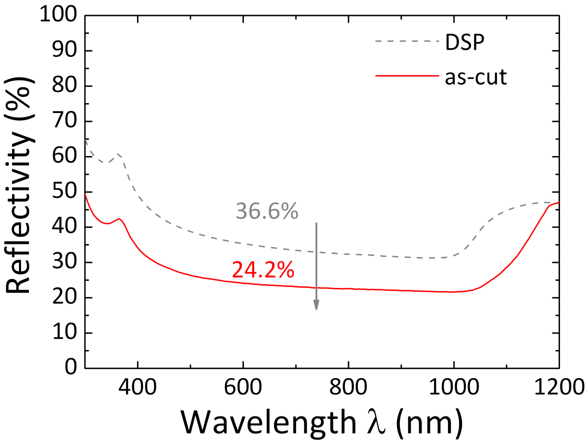
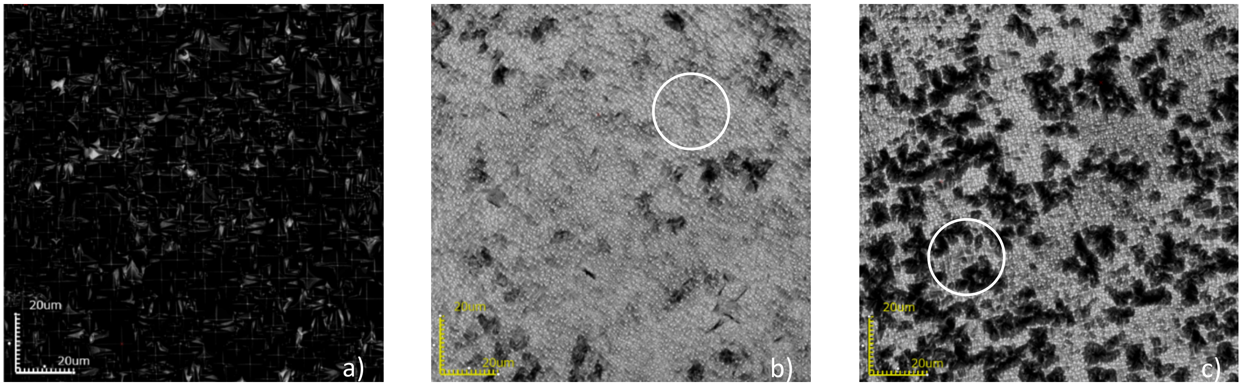


Figure 3-9 – Reflectivity of an as-cut wafer. The DSP reference is shown in the background (dotted grey line).

Thanks to this roughness, etching uniformity should be ensured by a more homogeneous attack by the OH^- ions. Thus, texturing was carried out using a 1.7%-dilute KOH both for the KOH-IPA and KOH-RenaTex solutions on as-cut wafers. For the latter, 0.6L of RenaTex additive was added to a 42L solution. One sample underwent 30 min of texturing in KOH-IPA while two wafers underwent 13-min and 45-min texturing in a KOH-RenaTex bath, respectively. For all the solutions, a similar etch rate of $0.29\ \mu m\cdot min^{-1}$ was measured. SEM images of the c-Si surfaces after texturing are shown in Figure 3-10. Figure 3-10a) shows an attack that was quite homogeneous since almost all parts of the wafer contain revealed pyramids. However, they are quite small, of varying sizes and do not look very well-defined, i.e., with no sharp edges. Figure 3-10b) shows an as-cut wafer textured for 13 min in the KOH-RenaTex solution. On the image, small white dots can be seen. These are the tips of pyramids that are being revealed by the texturing. The black parts are the regions that remain from the original as-cut roughness (white circle). The small size of the pyramids as well as the overall heterogeneity of the texturation led us to try a longer texturing time.



30’ KIno **13’ RTno** **45’ RTno**

Figure 3-10 – SEM images (top view) of KOH/IPA and KOH/RenaTex textured c-Si surfaces.

However, leaving the wafer in the same bath for 30 more minutes did not significantly improve the landscape as can be seen in Figure 3-10c). Moreover, for some reason, the texturing is even less homogeneous. This showed us that the roughness, which comes naturally after the ingot wire cutting, even if beneficial for a faster and more homogeneous attack by the etchant comparatively to polished substrates, seems to prevent the texturing to occur on every part of the silicon surface. This could be due to local porosity or to a less efficient wetting of the sharpest parts of the roughness. Figure 3-11 shows the height profile of an as-cut wafer. As can be seen, the landscape is very heterogeneous contrary to what can be seen on the SEM image shown in Figure 3-10. Moreover, the profile sometimes exhibits sharp parts, which made us suspect that some capillary effects could occur in some regions (at L=39 µm for example in Figure 3-11). These two features certainly affect the distribution of the etchant over the silicon surface. Figure 3-12 shows the reflectivity of the three samples after texturing.

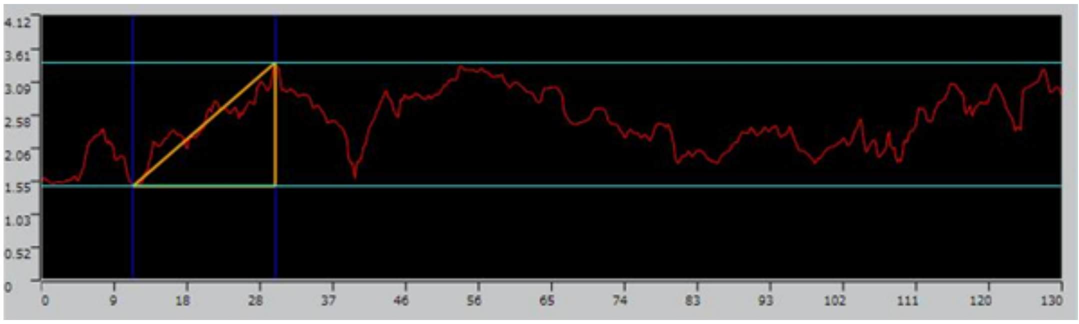


Figure 3-11 – Height profile (in µm) of a 130 µm-long region of a TOPSIL as-cut wafer made by LSM.

As can be seen, the reflectivity is much lower than in the case of a flat DSP wafer. However, only the KOH/IPA sample exhibits a value close to the ones we are expecting after wet-chemical texturing, i.e., 10-13%. This shows an interesting feature of IPA. IPA is thought to reduce the surface tension between the silicon surface and the etchant. This is the main reason why substitutes are often chosen among surfactants. These actually influence anisotropic etching processes by enhancing the wettability of the silicon surface in the case of alkaline-based etchants like KOH [178][179][180], as well as in the case of TMAH for example[181][182]. Indeed, some KOH/surfactant systems have already been used, showing mean reflectivities below 12%, ranging 400-1100 nm[183]. However, we see that the presence of the RenaTex surfactant obviously does not play the same role on as-cut silicon surfaces, yielding the poor homogeneity seen on images b) and c) of Figure 3-10.

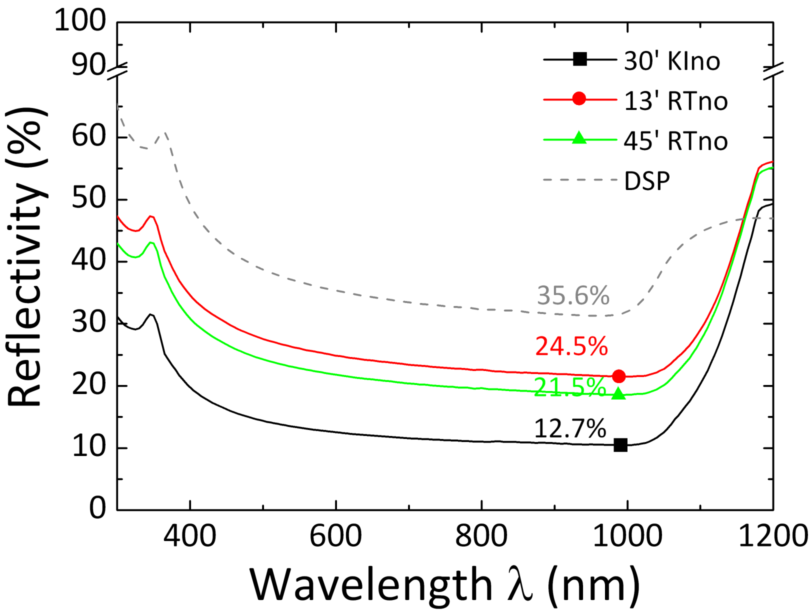
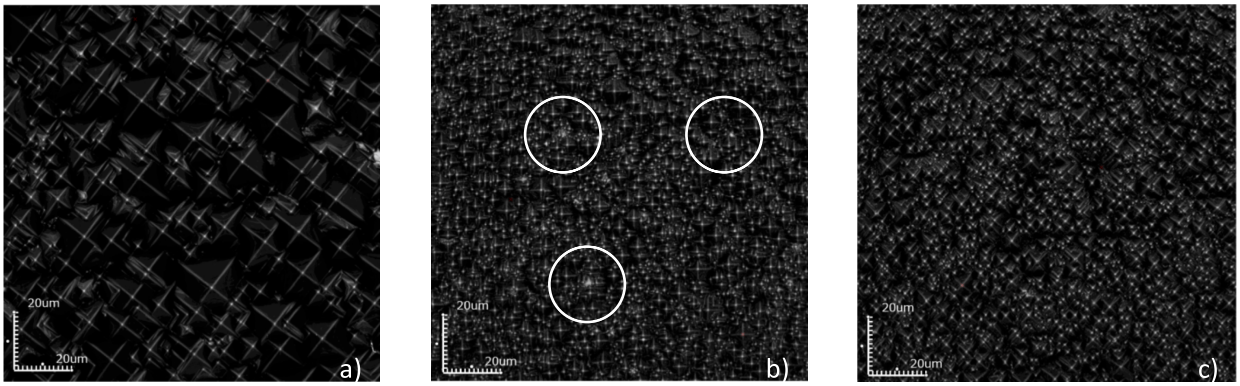


Figure 3-12 – Reflectivity as a function of the light wavelength for 3 different texturing recipes directly carried out on as-cut wafers. The reflectivity values given are averaged between 400 and 1100 nm.

In order to avoid polishing the wafers, which can be expensive and time-consuming, a solution to soften the roughness of as-cut wafers prior to texturing *per se* is needed. The best way to do this would be to combine this step with the subsequent texturing process. In the literature we can find different methods of removing these so-called *saw-damages*. Usually, dilute KOH or NaOH is used to etch from 10 to 30 µm on each side[184][180][185][186]. The etching reaction is similar to the one described by Eq. 83. Subsequently, anisotropic etching can be carried out to form randomly distributed pyramids on the Si surface. In some cases, it is even possible to use an etching mixture that will simultaneously remove the saw-damages and provide surface texturation. This is the case for the hydrofluoric acid and nitric acid mixture (HF/HNO_3). Many studies have been carried out by the *Hochschule Lausitz* group[187][188][189][190][191][192] regarding the mechanisms of wet-chemical etching of silicon using this particular solution. It can indeed remove saw-damages while lowering surface reflectivity by revealing shallow valleys in the micrometer range of monocrystalline silicon. However, it has found its main practical application for multi-crystalline as-cut wafers, due to its isotropic etching behavior[189][193]. In our case, we decided to apply to most commonly used technique in industrial PV, namely alkaline-based saw-damage removal. A 22%-NaOH solution was used to dip the as-cut wafers for 3 minutes at a temperature of 80°C. This step removed the silicon on both sides with a 1.8 µm/side/min etch rate. Consequently, an overall 11-µm thickness of silicon was removed at this stage, approximately. Subsequent texturing was carried out on these wafers in the same KOH/IPA and KOH/RenaTex solutions as previously. The resulting silicon surfaces obtained after the same texturing times as before are shown in Figure 3-13. The surfaces were incomparably more homogeneously attacked by the etchant this time. As a result, randomly distributed pyramids were revealed on the whole wafer surface, especially in the case of 30 min KOH/IPA (Figure 3-13a)) and 45 min KOH/RenaTex (Figure 3-13c)) texturing. However, in part b) of Figure 3-13 we noticed some areas (white circles) where the etchants did not seem to have had the desired effect. Indeed, when comparing with image c), we suspect that the 13-min texturing time was not sufficient to ensure a silicon surface homogeneously covered by random pyramids.



Saw-damage removal+30’ KIno **Saw-damage removal+13’ RTno** **Saw-damage removal+45’ RTno**

Figure 3-13 – SEM images of KOH-IPA and KOH-RenaTex textured c-Si surfaces.

Figure 3-14 shows the reflectivity of three as-cut wafers textured after a 3-min NaOH pre-treatment. As can be seen, in the case of KIno texturing, reflectivity increased only slightly, by 1 point, in the 400 to 1100 nm range. Contrariwise, the improvements seen by SEM in Figure 3-13 are confirmed by the much lower reflectivities obtained in the case of KOH/RenaTex texturing. Indeed, instead of the 24.5 and 21.5% reflectivities evidenced before for a 13-min and a 45-min texturing, respectively, these samples are now reflecting approximately 11 % of the light only, i.e., between 400 and 1100 nm. From the results shown above, we concluded that the easiest way to texture c-Si wafers was to use as-cut samples. However, in order to texture as-cut c-Si wafers with an alkaline etchant such as KOH, we need to carry-out a saw-damage removal step.

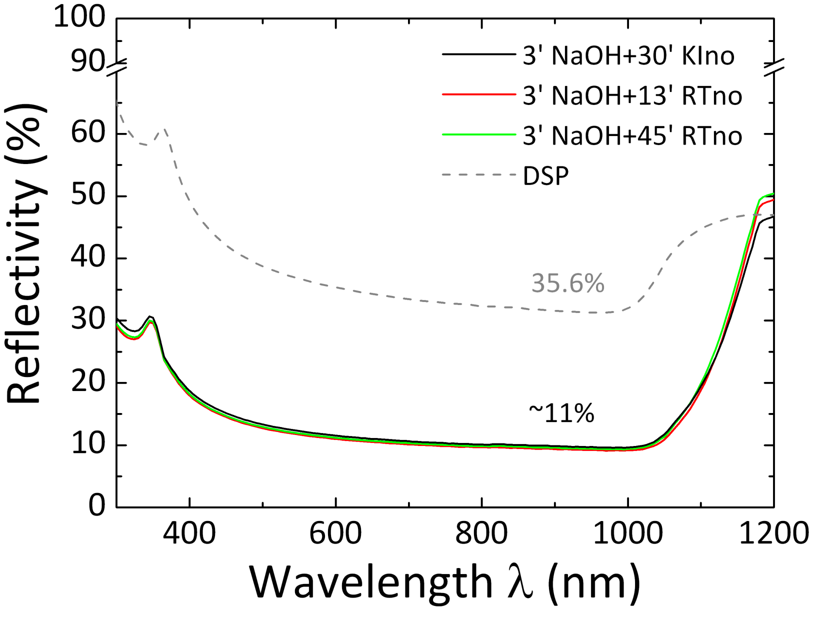


Figure 3-14 – Reflectivity as a function of the light wavelength for 3 different texturing recipes carried out on as-cut wafers after a 3 min NaOH surface pre-treatment. The reflectivity values given are averaged between 400 and 1100 nm.

Even if it does not seem necessary “optically” in the case of KOH/IPA texturing, the homogeneity and sharpness of the randomly distributed pyramids were much enhanced by a 3-min NaOH pre-treatment in both texturing recipes (IPA and RenaTex surfactant).

3.1.3.b KIno and RTno texturing recipes

As a consequence, we decided to keep two recipes for our investigation on the passivation of textured n-type c-Si wafers. Basically, all wafers underwent a 3-min NaOH pre-treatment to remove damages related to wire cutting of silicon ingots upon wafer production. Next, wafers were divided in two batches. One batch was textured using a KOH/IPA mixture for 30 minutes, yielding *KIno* wafers, whereas the second one was textured using a KOH/RenaTex mixture for 45 minutes, yielding *RTno* wafers. The reason why we did not keep the 13-min KOH/RenaTex texturing is that despite its slightly better optical properties between 400 and 1100nm and in the near-IR, some texturing imperfections were noticed by SEM in Figure 3-13b). This led us to think that passivation could be impacted or that at least, passivation trends would be randomized because of the intrinsically unpredictable occurrence of these imperfections. After cleaning the wafers following a precise routine that we will later described, passivation tests were carried out using SiN_x deposited by PECVD on the three types of samples. It was determined that 13 minutes of texturing in a KOH/RenaTex mixture would lead to a slightly lower iV_{OC} than in the case of a 45-min texturing (680 mV versus 685 mV), as shown in Table 3-4.

Saw-damage removal	Texturing	ε [µm]	iV_{OC}@1 Sun [mV]	J_{oe} [A/cm^2]	τ_{eff}@1E15 cm^{-3}
3' NaOH	13' RTno	242	680	9.97-14	591
	45' RTno	230	685	8.50-14	652
	30' KIno	228	671	8.50-14	353

Table 3-4 – Effective lifetime, iV_{OC} and J_{0e} of textured c-Si wafers passivated by a thin layer of SiN_x deposited by PECVD.

Of course, passivation using PECVD-deposited a-Si:H is quite different since it is also based on chemical passivation and not solely on charges that create a field effect. However, it is a good indicator of the defect density at the a-SiN_x:H/c-Si interface. Moreover, the fact that the reflectivity of the 13-min KOH/RenaTex sample was slightly higher in the blue, the most important region for us, confirmed that 45 min would be the texturing time to retain. Even with KIno recipe leading to lower iV_{OC}s, it will be retained in order to study the impact of the pyramid size on passivation. Indeed, even if the reflectivities of both texturing recipes are quite similar, Figure 3-13 clearly demonstrates that KIno samples have larger pyramids featuring 10-µm large square bases sometimes.

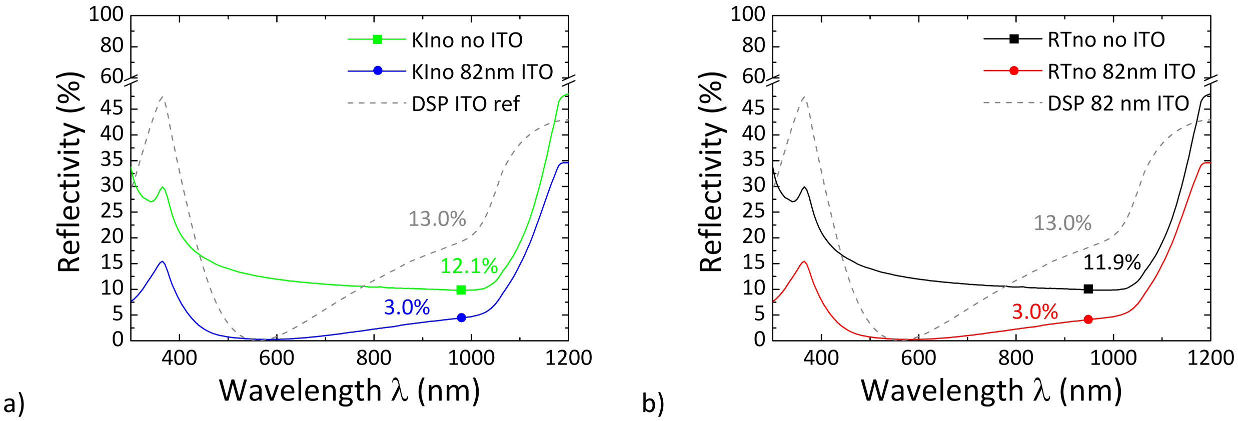


Figure 3-15 – Reflectivity as a function of the light wavelength for KIno (part a)) and RTno (part b)) wafers, with and without ITO.

Contrariwise, RTno samples exhibit pyramids with smaller bases, reaching 4-5 µm at most. Figure 3-15a) and b) show the reflectivity of KIno and RTno wafers before and after the sputtering of a thin ITO layer

(~82 nm) by PVD using our standard conditions. As expected, ITO decreases the reflectivity of both samples down to the identical mean value of 3.0%. These results appear promising in the perspective of the fabrication of HJ solar cells with such substrates. Indeed, these being identical in the 400-1100 nm range, it will be easier to compare their potential for passivation purposes and to draw conclusions based on the pyramid size distribution. It is noteworthy that the amount of silicon etched upon all kinds of texturing is quite significant. Indeed, our as-cut wafers were 280-µm thick, initially. After texturing, the measured thicknesses ranged 230-240 µm. This represents a loss of 20 to 25 µm on each side of the wafer.

3.2 Passivation of wet-textured c-Si n-type wafers using a-Si:H

Passivation of crystalline silicon (c-Si) is a process commonly used in microelectronics and in the PV industry. It allows for the fabrication of electronic devices such as transistors and photovoltaic solar cells. It is all about depositing a material which will neutralize chemically and physically the unsaturated dangling bonds at the crystalline silicon surface level. To do so, different materials can be used, which are amorphous most of the time, such as thermally-grown silicon dioxide (SiO_2)[81][82][194], silicon nitride (SiN_x)[195][196][87][90] or hydrogenated amorphous silicon (a-Si:H)[197][198]. A-Si:H is of interest since it can be doped to generate p-n heterojunctions with n-type and p-type c-Si wafers. In this section, the passivation of textured n-type silicon surfaces will be studied with regard to their flat (100) and (111) counterparts, and challenges relating to the quality of the texturing will be addressed. A solution to compensate the surface imperfections arisen upon texturing will be explored under the prism of undesirable epitaxial growth and a method to impede such will be proposed.

3.2.1 Defining a cleaning procedure for our textured c-Si wafers

When exposed to air, a freshly cleaved c-Si surface, whether it be (100) or (111) oriented, will quickly start oxidizing. Then, Si-Si bonds under the Si surface layer are broken to produce Si-O bonds. As a result, the overlayer structure becomes amorphous, leading to a layer-by-layer oxide growth. This oxide, also called *native oxide*, usually saturates starting at a certain thickness depending on the ambient conditions and time[199]. In our case, we were able to measure thicknesses of about 13 Å with a very high accuracy, as can be seen in Figure 3-17. Even if thermally-grown SiO_2 is known to passivate crystalline silicon very well, with recombination velocities (S_{eff}) lower than 10 $cm \cdot s^{-1}$ for high and low-resistivity n-type wafers[81][82][83], this is not the case with native oxide. Moreover, native is an insulator which hinders the collection of charge carriers flowing through the a-Si:H/c-Si interface. As a result, this oxide has to be removed prior to any passivation process. The most effective procedure to remove this native oxide is the so-called RCA standard clean developed by *William Kern* while working for the *Radio Corporation of America*[200][201]. This procedure requires, however, constant monitoring of the temperature and of other parameters, which was not possible within the LPICM facilities. For this reason, a simplified procedure was created based on the literature as well as on experimental results. Indeed, for polished c-Si wafers, the usual way to remove the native oxide is through wet-chemical treatment of the surface by a low-concentration HF solution[202]. This procedure is extremely efficient and, in the case of industrially-produced DSP wafers, there is obviously no need to track organic or metallic contaminants. This is reported by some research labs working on passivation and on topics related to the fabrication of a-Si:H/c-Si heterojunction solar cells[203][204].

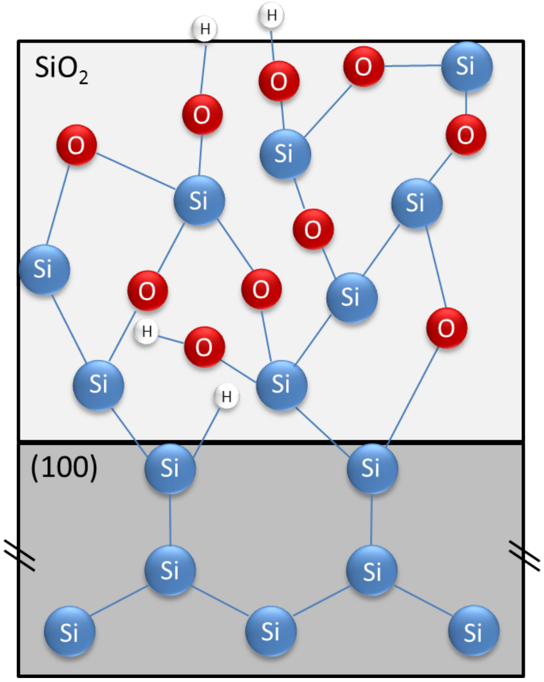


Figure 3-16 – Model of native oxide growth as reported by *Morita et al.*[199].

Some other labs prefer to still integrate a contaminant removal step directly taken from the RCA procedure or slightly modified[205][206]. In our laboratory, our standard procedure includes a 30-sec dip in a 5%-dilute solution solely. Thanks to this, a record effective lifetime value of 17.3 ms with an iV_{OC} of 734 mV was obtained during this Ph.D. thesis, with an in/in symmetrical stack deposited on a DSP (100) n-type wafer. Moreover, a 17.2% 2x2 cm² n-type heterojunction solar cell was reported in 2011. It used the same kind of substrate with this simple cleaning procedure[12][176]. In the case of textured wafers however, a simple HF dip was not sufficient. Indeed, our wafers are textured from their as-cut state. Possible contaminants are organic compounds such as *slurry* from multi-wire cutting, glue, synthetics or etch resist and metals. Since the texturing ends up to by being efficient and homogeneous when the right recipe is applied, it seems that there is not much contaminant left on the c-Si surface[185]. However, cleaning our textured wafers in a dilute HF solution was not sufficient to obtain high effective lifetimes[29]. Therefore, we used a three-step cleaning procedure consisting in: i) a cleaning in acidic baths (HCl to remove metallic impurities, then HF to remove the native oxide), ii) a cleaning in a 3:1 H_2SO_4/H_2O_2 solution (Piranha bath) to remove all organic impurities from the c-Si surface (boiling mixture because of the exothermal reaction) which results in the growth of a thin oxide layer, and iii) a final HF dip to remove the oxide grown during step ii). The procedure is described in more detail in Table 3-5. As stated earlier, the facilities at LPICM did not allow for texturing and cleaning in the best conditions. For this reason, all textured wafers underwent the cleaning procedure immediately after texturing at *ISC Konstanz* facilities, up to step iii).

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[29] This would be later confirmed by the random trends obtained while passivating textured c-Si wafers after in-situ removal of the native oxide using SiF_4/H_2 plasma chemistry[207][208]. Indeed, contaminants act as recombination centers and their distribution is randomized by the wafer fabrication process, leading to low as well as sometimes, high effective lifetimes.

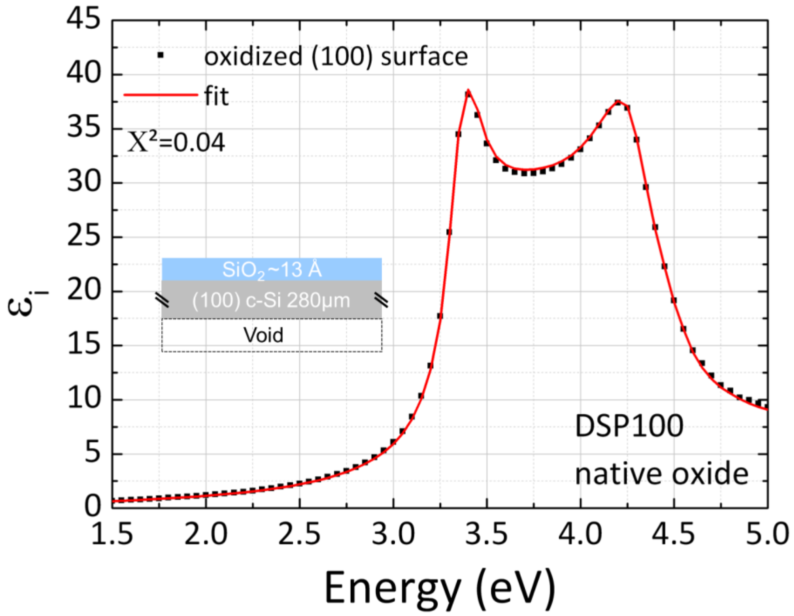

Figure 3-17 – Imaginary part and fit of the pseudo-dielectric function of mirror-polished 100 c-Si surface covered with its natural native oxide.

	Post-texturing cleaning recipe	
i)	DI water rinsing until	1.5 MΩ
	HCl (3%)	300 sec
	DI-water rinsing until	1.5 MΩ
	HF (2%)	120 sec
	DI-water rinsing	Dip
ii)	Piranha-bath (H_2SO_4/H_2O_2 3:1)	600 sec
	DI-water rinsing until	2.0 MΩ
iii)	HF (5%)	45 sec

Table 3-5 – Standard cleaning procedure for all of our c-Si textured wafers. Step iii) was carried out in our facilities.

In this way, we would ensure that the c-Si surface would be cleaned from any metallic and organic impurities and protected from any further ambient contamination by the thin oxide layer while shipped and stored. Step iii) would be done at LPICM just before loading the samples in the PECVD reactor. Since we do not know the exact thickness of this oxide layer, in order to determine the adequate HF dip time for step iii) the effective lifetime of textured wafers cleaned after steps i) and ii) was measured. As can be seen in Figure 3-18, the native oxide grown in the Piranha bath (step ii) does not yield good passivation properties prior to step iii). This is probably due to the poor quality[30] and small thickness of the native oxide. After dipping the wafer for 30 seconds in 5%-dilute HF, the passivation increases due to partial native oxide removal as well as to the newly and temporarily acquired H-termination of the c-Si surface broken bonds. A second 30-sec dip further increases the effective lifetime to a maximum value of about 100 µs at a 2E15 cm^{-3} injection level. An additional 30-sec dip time leads to a passivation decrease. This shows that we had probably removed all the native oxide after 60 seconds of HF dip.

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[30] Indeed, thermally grown SiO2 is grown by thermal oxidation at higher temperatures (~1000°C).

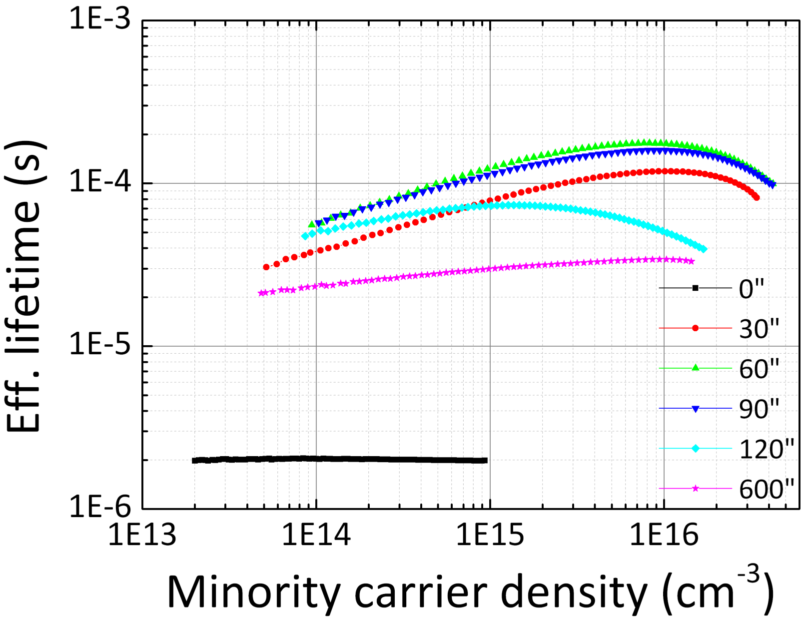

Figure 3-18 – Effective lifetime of an textured KIno c-Si wafer measured after various 2nd HF dip times.

Moreover, the decrease in lifetime beyond 90 seconds of HF dip testifies to an attack of the c-Si surface by the HF, inducing the creation of defects and possibly a nano-roughness, thus increasing the recombination of photogenerated carriers. As can be seen in Figure 3-19, after a 60-sec HF dip, the effective lifetime reaches its highest value. After an additional 30-sec HF dip, the lifetime starts decreasing. The effective lifetime was then measured on a regular basis until t=600”. A clear decay was observed that could be fitted by an exponential function, confirming the high sensitivity of the cleaned wafer to ambient air. Indeed, the H-termination seems to be quickly converted into Si-O-Si or Si-OH bonds.

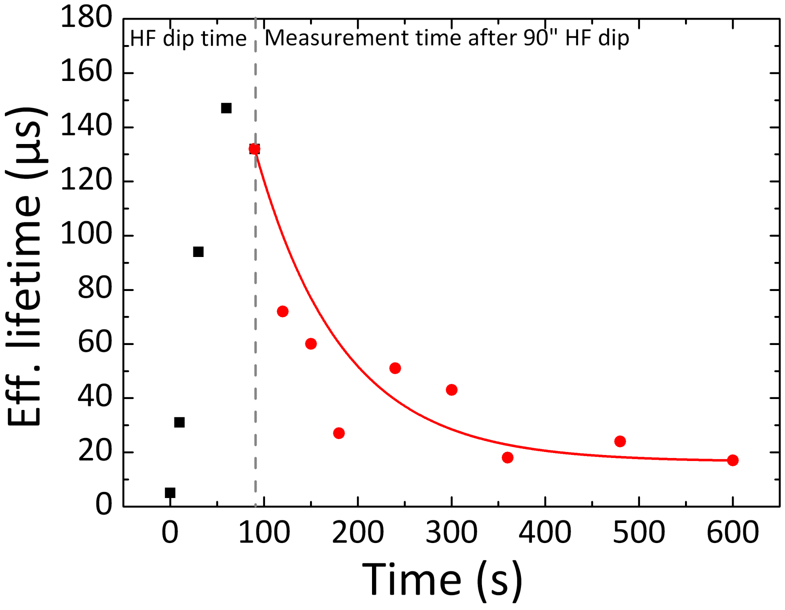

Figure 3-19 – Decay of the effective lifetime of a KIno c-Si wafer after a 90 sec 2nd HF dip.

It has been reported by *Morita et al.* [209][199], *Ohmi et al.*[210] and *Morita*[211] that the native oxide growth on a silicon surface requires the presence of both O_2 and H_2O. This was confirmed later by the work referenced[212]. Since we did no operate under clean-room conditions, our wafers would undergo the last HF dip (step iii) of the cleaning procedure) right before loading into the PECVD reactor. It is also possible to remove the native oxide by a dry process using in-situ plasma etching, as mentioned earlier. Such will not be used throughout this thesis as a standard cleaning procedure since the effective lifetimes obtained through wet-chemical treatment were much higher.

3.2.2 Passivation enhancement on textured (n)c-Si wafers

After having defined our standard cleaning procedures for DSP and textured wafers, our samples could be loaded in our PECVD reactor for a-Si:H deposition. Prior to passivating textured c-Si surfaces, however, we decided to make a comparative study of the passivation of (100) versus (111) c-Si flat surfaces. Indeed, given the latter's specific crystallographic orientation and surface dangling bond organization, the a-Si:H growth happened to be quite orientation-dependent. This led us to study epitaxial growth impediment on (100) flat surface, which proved to be very useful for enhanced passivation of textured (n)c-Si wafers.

3.2.2.a Passivation of flat 100 and 111-oriented (n)c-Si wafers

Although heterojunction solar cells rely on the deposition of amorphous silicon on crystalline silicon, under certain plasma conditions epitaxial growth can occur, especially on (100)-oriented c-Si wafers. This effect has been reported by *Tsai et al.*[213] when getting close to µc-Si deposition conditions, i.e., when silane is highly diluted in hydrogen and for temperatures ranging from 150 to 350°C. Since we usually deposit a-Si:H at temperatures close to 200°C, epitaxial growth is very likely to happen when passivating (100) flat substrates. The epitaxial layer is unfortunately not simply a continuation of the c-Si wafer, as the network incorporates about 30-100 times more hydrogen than the c-Si substrate. Demonstrably, the material grown close to 200°C contains more defects, usually in the form of clustered H platelets. In heterojunction solar cells, we are interested in lowering the a-Si:H/c-Si defect density, therefore epitaxial growth must be avoided when passivating c-Si surfaces[214]. This was confirmed by the studies of *Kondo et al.*[205] and *Gielis et al.*[215], in which plasma conditions were chosen carefully, so that the passivating layers were completely amorphous. This is because usually the epitaxial layer is not purely crystalline but exhibits a mixed-phase. Whether the epi-Si/c-Si interface be sharp, the epitaxial layer could be incorporated in a heterojunction solar cell as *Damon-Lacoste et al.* have reported[216]. However, their performances were lower than their counterparts containing an abrupt a-Si:H/c-Si interface. Figure 3-20 illustrates this phenomenon. A thin intrinsic a-Si:H layer is codeposited using our standard conditions on a flat (100) c-Si wafer and on its (111) counterpart. As can be seen, the (100) sample exhibits the very poor effective lifetime of 16 µs with a iV_{OC} of 552 mV. This value is actually very close to the value we typically get when measuring a wafer before dipping it into HF, i.e., with its native oxide on both sides (5 µs). Needless to say, with such passivating properties any finalized device would perform very poorly. On the other hand, our standard conditions yield a 3.6 ms lifetime and a 724 mV iV_{OC} on a (111)-oriented c-Si surface. Figure 3-21 shows that with increasing thicknesses we can lower the interface defect density even more while increasing the field-effect in the low-injection range.

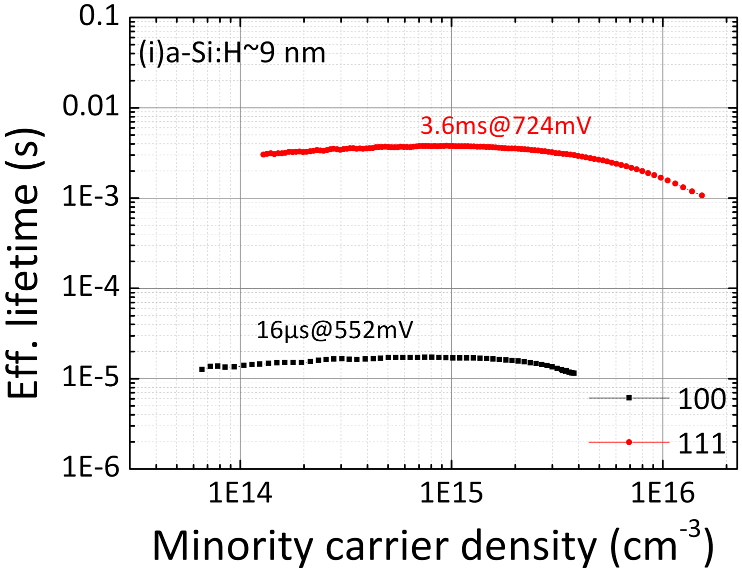

Figure 3-20 – Effective lifetime curves of two mirror-polished (100) (black squares) and (111) (red dots) c-Si wafers symmetrically passivated by a 10 nm thin (i)a-Si:H layer. The (100) sample exhibits a very low passivation level.

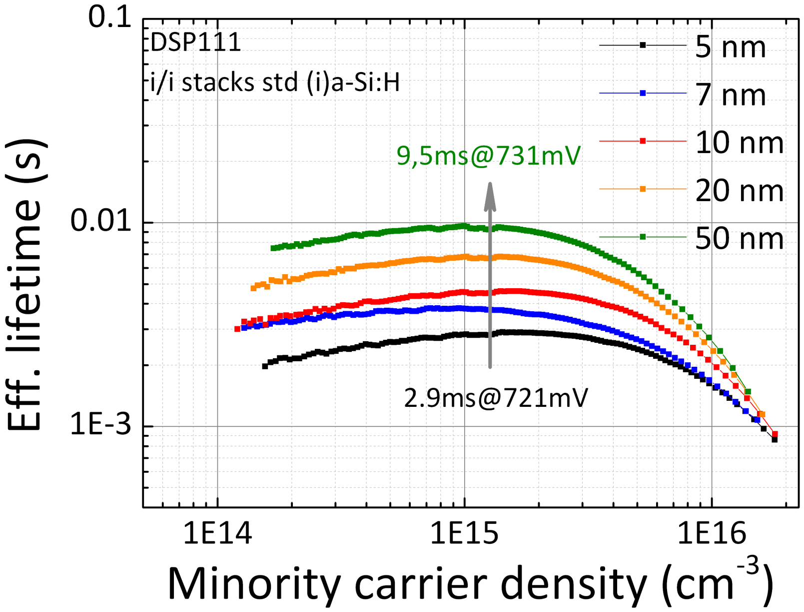

Figure 3-21 – Dependence of the effective lifetime of i/i passivated (111) wafers on the a-Si:H layer thickness.

It also shows that our standard a-Si:H deposition process is very reliable, yielding a clear trend between 2.9 ms and 721 mV up to almost 10 ms and above 731 mV, as Figure 3-21 shows. It is worth noting that both the (100) and (111) samples were fabricated together in the same substrate holder. In order to study the characteristics of the material deposited, spectroscopic ellipsometry was performed on these samples. Results are shown in Figure 3-22. As can be seen, the (111) sample shows a typical amorphous signal for a thin a-Si:H layer deposited on a c-Si substrate. Obviously, although the a-Si:H layer is very thin the peak at 4.2 eV has decreased. In the case of the (100) sample however, the signal is very near the c-Si reference. In the case of (111)-oriented c-Si surfaces, epitaxial growth is less likely to happen, although it is possible in some cases[205].

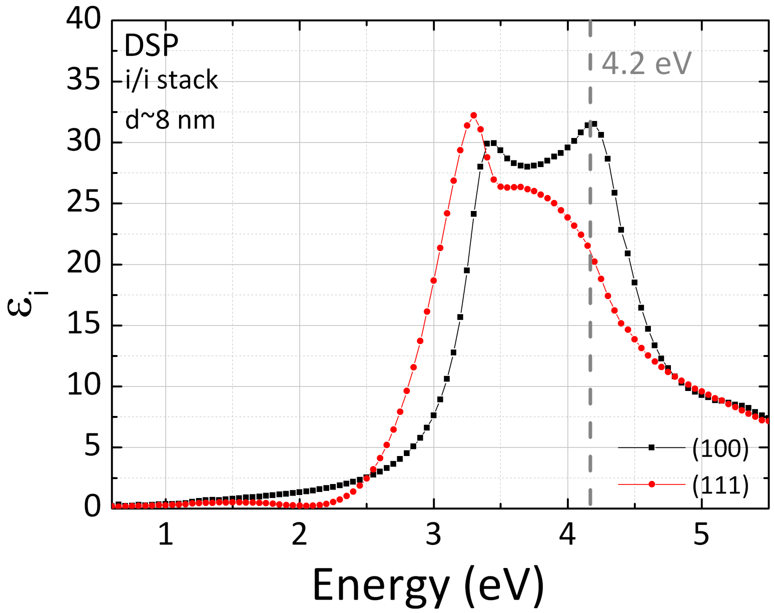

Figure 3-22 – Imaginary part of the pseudo-dielectric functions of a 10nm-thick a-Si:H layer deposited on two mirror-polished 100 (black squares) and 111 (red dots) c-Si wafers. We can clearly see that the layer deposited on the 100 sample is epitaxial.

Therefore, we should not witness this phenomenon on textured c-Si substrates. Nonetheless, as we will see in the following sections, a-Si:H growth on textured c-Si substrates is not so straightforward and challenges will arise when transferring passivating recipes. To understand how epitaxy can occur during a-Si:H growth, we will now review the different options at our disposal to circumvent this issue on (100)-oriented c-Si substrates.

High power, high pressure and high dilution conditions

One of the ways of avoiding epitaxial growth on (100)-oriented c-Si substrates is to change the plasma conditions. Characteristically, epitaxial growth occurs on (100) surfaces at higher temperatures and parameters such as pressure, RF power, etc. can modify the organization of SiH_3 radicals at the c-Si surface. When epitaxial growth is fostered it is however lost after a few Angstroms or nanometers, breaking down to a-Si:H growth eventually. A simple solution would be to change the surface/radical interactions in order to avoid the organization thereof into a crystalline lattice. A typical example is shown in Figure 3-23, where two (100) c-Si wafers passivated with a thin intrinsic a-Si:H layer under two different conditions (described in Table 3-6) lead to radically different results. As can be seen, the epitaxial growth at the interface seems to be inhibited by the new conditions since the passivation level is now much higher, yielding an effective lifetime of 2.2 ms and a 708 mV iV_{OC}.

	H2	SiH4	Pressure	Power	Dep. Time
Units	[sccm]	[sccm]	[mTorr]	[W]	[s]
Std conditions (pure silane)	0	50	50	1	103
Non-epi conditions	500	50	2600	2600	600

Table 3-6 – Deposition conditions of a-Si:H on two (100) c-Si wafers.

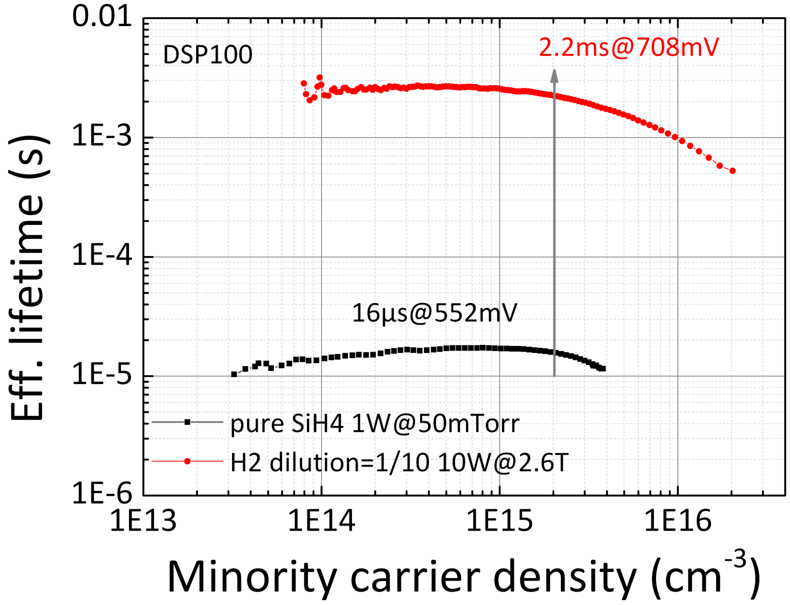

Figure 3-23 – Effective lifetime of two mirror-polished 100. One the first one is deposited a thin (i)a-Si:H layer in our standard pure silane conditions (black squares) and on the second one is deposited a thin (i)a-Si:H layer at high pressure, high power and in H_2 dilution 1/10.

It should be noted that the short deposition time in the case of the sample deposited under pure silane conditions does not affect the interpretation of this finding. Indeed, the same low passivation level has been observed when growing thicker layers under pure silane conditions on 100 c-Si wafers.

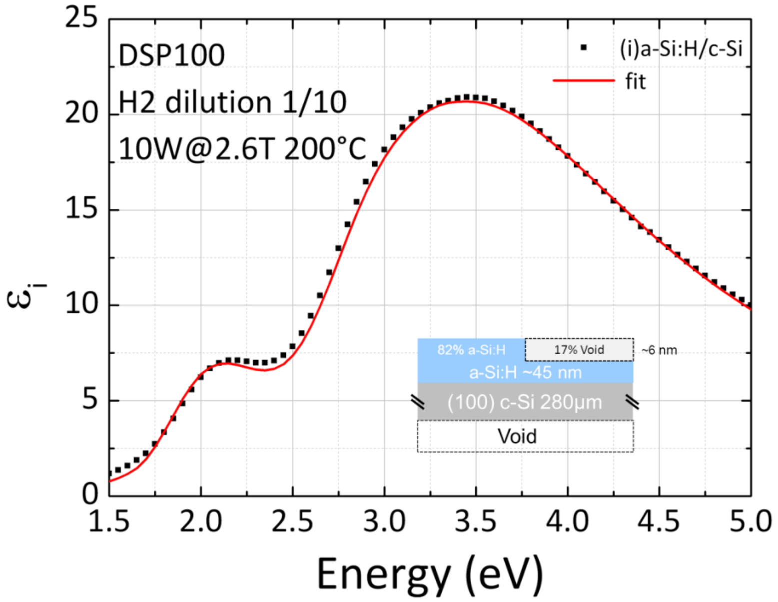

Figure 3-24 – Imaginary part of the pseudo-dielectric functions of an a-Si:H layer deposited on a mirror-polished 100 c-Si wafer under high pressure, high power and highly H_2-diluted conditions. We can clearly see that the layer deposited on the 100 sample is amorphous.

This result is confirmed by the clear amorphous signal detected by spectroscopic ellipsometry, as shown in Figure 3-24. This acquisition could be fitted with a low χ^2 using a simple Tauc-Lorentz model as shown below. The optical bandgap was estimated at 1.64 eV and the layer was indeed amorphous. We found this approach interesting because it does not require any additional processing step. However, the conditions in which we could obtain amorphous growth on (100) wafers were really close to powder formation and were, therefore, not reproducible. Sometimes we would get high lifetimes but the presence of powder due to the high pressure/high power conditions would lower the effective lifetime by contaminating the surface of our freshly cleaned c-Si wafer. We therefore decided to find another way to prevent epitaxial growth.

Low-temperature deposition conditions

Another way of avoiding epitaxial growth on (100)-oriented c-Si surfaces is to lower the deposition temperature. Indeed, it has been shown that the substrate temperature is an important parameter for epitaxial growth. Reducing it could lead to more amorphous growth[217][215][205]. However, a-Si:H layers deposited at low temperature are more defective[36] in their as-deposited state, as can be seen in Figure 3-25 extracted from *R.A. Street*'s textbook. Incorporating such a film in a passivated structure would imply a post-deposition annealing at a relatively low temperature, i.e., below 250°C, in order to reduce the defect density. Indeed, these layers do not provide good passivation properties in their as-deposited state and several groups have demonstrated that it was possible to increase the effective lifetime of symmetrically-passivated samples by 2 or even 3 orders of magnitude[204][218]. *Pysch et al.* even showed that this technique could be implemented to increase the V_{OC} of finalized solar cell devices[219]. There was an attempt made to explain this phenomenon by stressing the fact that in the as-deposited state, not only the a-Si:H material *per se* but also the interface between the a-Si:H layer and the c-Si substrate was not at equilibrium. Therefore, performing an annealing on a passivated sample would lead to a lower defect density in the a-Si:H bulk but also at the a-Si:H/c-Si interface[74].

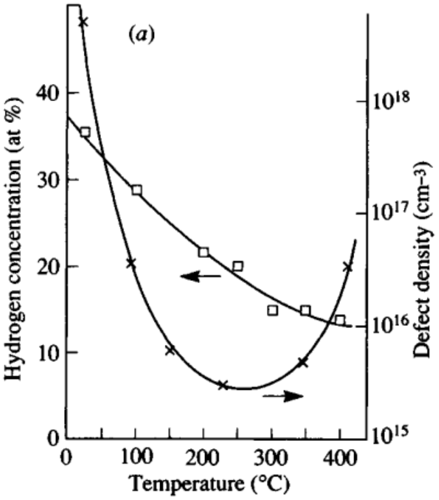

Figure 3-25 – Variation of the hydrogen content (left axis) and defect density (right axis) of an intrinsic a-Si:H layer as a function of its deposition temperature[36].

However, in *Martin Labrune's* Ph.D. thesis([12] pp. 88-89), annealing studies were performed on different stacks and cells, whereby he concluded that lifetimes above 1.2 ms would in fact be obtained when depositing at 125°C and subsequently annealing between 200 and 250°C in the case of intrinsic capping layers.

However, when dealing with doped a-Si:H layers or even in/in and ip/ip stacks, i.e., when protecting the interface with an intrinsic buffer layer, no lifetime would increase above 750 µs (in/in stacks) or 200 µs (ip/ip stacks). Therefore, the conclusion was that no solar cells with a high V_{OC} could be obtained by depositing at such a low temperature, despite the amorphous characteristics and the excellent passivating properties of the (i)a-Si:H layers. Hence, this is not the direction we chose for our experiments.

Incorporation of impurities at the interface

Even though it is possible to avoid epitaxial growth by lowering the deposition temperature, effective lifetimes are not high enough to provide solar cells with a high iV_{OC}. Moreover, other options such as argon plasma treatments have been explored in *J. Damon-Lacoste's*[11] and *M. Labrune*'s[12] Ph.D. theses to avoid epitaxial growth. Results have shown that in fact, epitaxial growth occurs only on the (100) wafers which did not undergo an argon plasma treatment. This is mainly due to the ion bombardment from the Ar plasma, which induces the creation of defects or the amorphization of a few angstroms at the c-Si surface. This, in turn, makes epitaxial growth impossible, since defects disrupt crystalline organization quite efficiently. However, there was a delicate balance to find between the amorphization of the first atomic layers of the c-Si wafer and the creation of too high a number of defects. Obviously, for passivation purposes, we need to keep the a-Si:H/c-Si interface defect density as low as possible. For these reasons, neither of these options were retained. Instead, we decided to focus on epitaxial growth breaking by controlled addition of impurities at the interface. Several types of impurities can be considered since their mere presence prevents the layer from organizing in a crystalline lattice. Actually, any atom that is not necessary to the a-Si:H layer growth can be considered an impurity, even boron and phosphorus when dealing with an intrinsic a-Si:H layer deposition. Carbon seems like a good candidate for this purpose. Several groups, namely *Pysch*'s team[220][221], have studied the impact of carbon incorporation in a-Si:H layers[222][223] on the implementation thereof for passivation purposes and even for heterojunction solar cell applications[224][225][226][227]. However, these involved the deposition of an actual a-SiC alloy. In *M. Labrune's* thesis, CH_4 was chosen as an additional gas during the intrinsic a-Si:H layer deposition to solve the epitaxial growth problem on flat (100) wafers.

T=200°C	SiH4	CH4	Pressure	Power	Dep. Time
Units	[sccm]	[sccm]	[mTorr]	[W]	[s]
a-SiC:H	25	50	40	1	30
a-Si:H	50	0	50	1	–

Table 3-7 – Deposition conditions of an a-SiC:H/a-Si:H stack designed to impede epitaxial growth on (100) c-Si wafers.

Plasma conditions and deposition time were chosen such that carbon was incorporated only during the first seconds of the deposition in very small proportions, resulting in the growth of a thin (~2nm) a-SiC:H layer at the a-Si:H/c-Si interface. This buffer layer was then covered by a standard intrinsic (i)a-Si:H layer for passivation purposes, as shown in Figure 3-26. The standard deposition conditions of the a-SiC:H buffer layer are shown below, together with the deposition conditions of the capping a-Si:H layer. As can be seen in Figure 3-27, the presence of this thin a-SiC:H layer at both a-Si:H/c-Si interfaces allows to reach much higher effective lifetimes than with a standard a-Si:H layer solely. These lifetimes are actually very close to those of their (111) counterparts. Actually, at high injection levels the (100) with a thin a-SiC:H buffer layer overlaps quite well with the (111) sample, showing an almost identical interface defect density. At low-injection levels however, where the field-effect passivation is dominant, we notice a lower lifetime in the (100) case. This shows that even though carbon allows for amorphous growth on (100) c-Si wafers, its presence affects the passivation by lowering the field-effect contribution to the overall passivation.

Figure 3-26 – Schematic representation of a passivated c-Si wafer with (right) and without (left) a thin a-SiC:H layer at the a-Si:H/c-Si interface.

It should also be stressed that our standard a-SiC:H layer does not possess good passivating properties in itself. Indeed, high lifetimes such as the ones presented in Figure 3-27 have never been reported in the literature when capping with an amorphous silicon carbide layer alone. The best value reported so far reached 1650 µs on a p-type wafer, but phosphine was added to the gas mix[228]. Under our standard conditions, the lifetimes were close to identical in the case of (100) and (111) wafers when depositing a 20-nm thick a-SiC:H layer, and reached 805 and 768 µs with an iV_{OC} of 682 and 681 mV, respectively. Results of the PCD measurements are shown in Figure 3-28, wherein the two lifetime curves overlap quite nicely, especially at high injection.

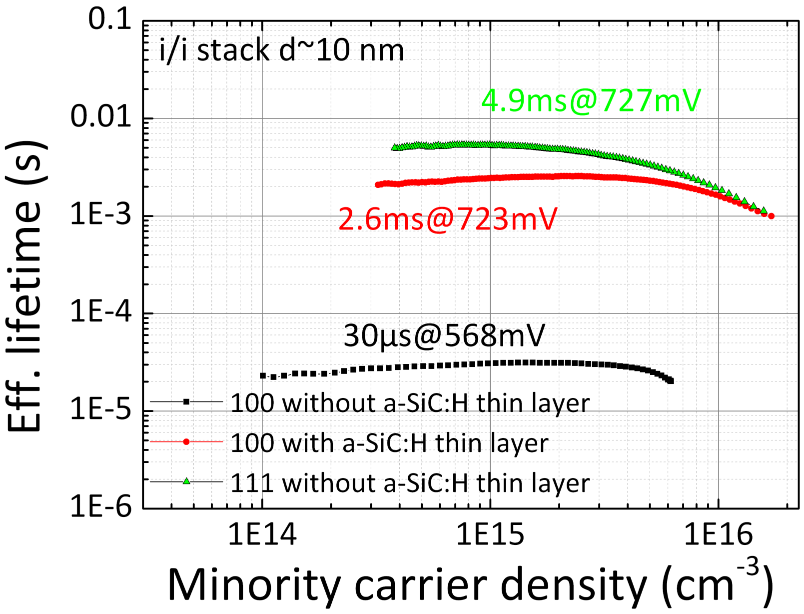

Figure 3-27 – Effective lifetimes of three passivated samples. The first one (black squares) is a (100) capped with a standard 10 nm a-Si:H layer whereas the second one (red dots) has a thin a-SiC:H buffer layer at both a-Si:H/c-Si interfaces. Their (111) counterpart is shown in green triangles.

At low-injection, there seems to be a stronger field-effect in the case of the (100) wafer, but this is quite negligible given the accuracy of the measurement. Therefore, the increase in lifetime evidenced in

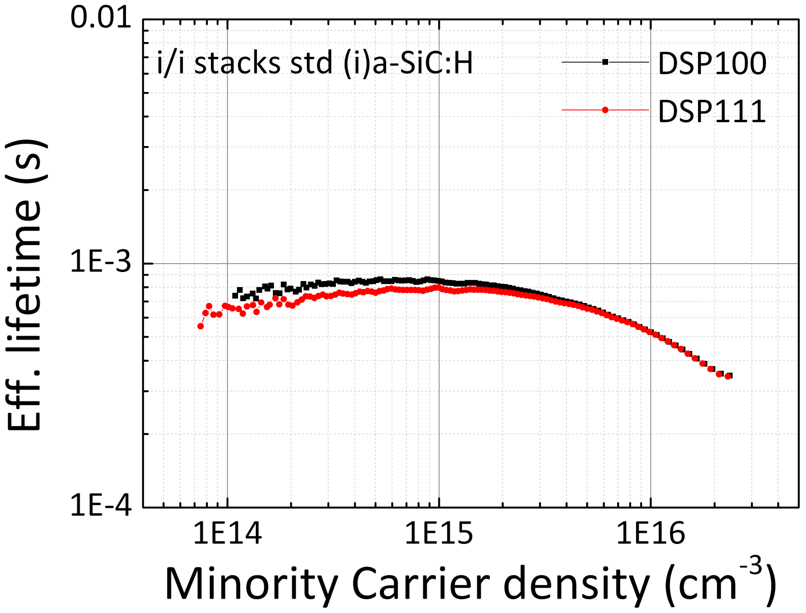

Figure 3-28 – Effective lifetime curves of two c-Si wafers passivated with ~20 nm of a-SiC:H under our standard conditions.

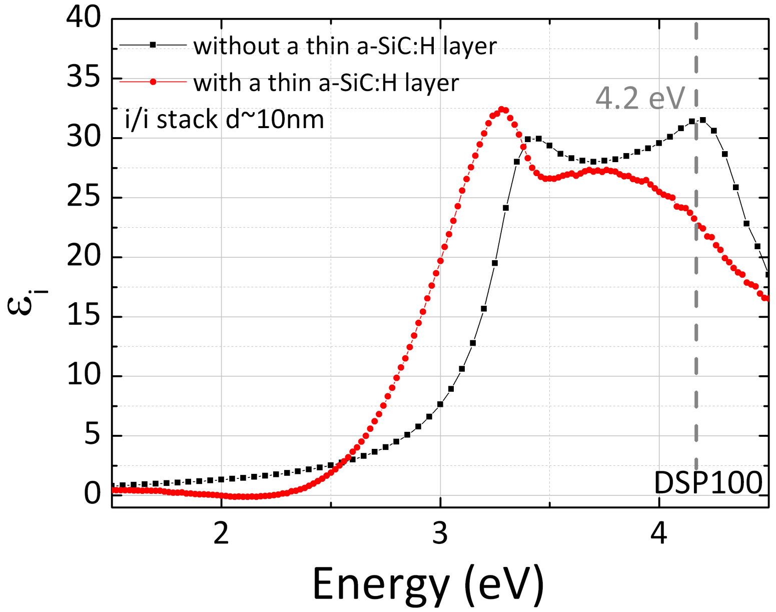

Figure 3-29 – Imaginary part of the pseudo-dielectric functions of an a-Si:H layer deposited on a mirror-polished 100 c-Si wafer with (red dots) and without (black squares) a thin a-SiC:H buffer layer at both a-Si:H/c-Si interfaces.

Figure 3-27 is really due to the subsequent deposition of an intrinsic a-Si:H layer. The role of the a-SiC:H layer is only to provide for an amorphous growth of silicon on (100) wafers. This can be understood in terms of an increase in the a-SiC:H bulk defect density. Indeed, it has been demonstrated by *Mahan et al.* that alloying silicon with carbon induces an increase in the microstructure content, which in turn increases the Urbach energy E_u[222]. It was actually found that there is a correlation between the bulk defect density of a-Si:H films and their Urbach energy[229].

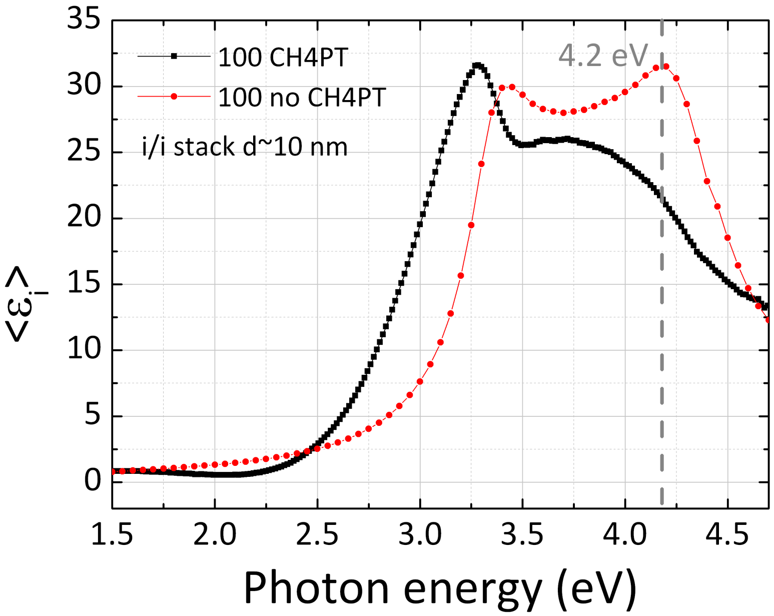

Figure 3-30 – Imaginary part of the pseudo-dielectric functions of an a-Si:H layer deposited on two mirror-polished 100 c-Si wafers with (red dots) and without (black squares) a short CH4 plasma treatment at both a-Si:H/c-Si interfaces.

A higher defect density in the bulk does not seem to impact the a-Si:H/c-Si interface quality at first sight. However, it was demonstrated by *Schulze et al.* that the bulk defect density of a a-Si:H capping layer is, in fact, in equilibrium with the interface defect density[74]. This may explain why our effective lifetime remains quite low when passivating with a-SiC:H solely, despite the obvious benefit of avoiding epitaxial growth. The amorphous feature of the a-Si:H layer deposited over the a-SiC:H buffer layer can be seen in Figure 3-29. Just as in (111) case shown in Figure 3-22, the signal is typical of amorphous silicon measured on crystalline silicon as measured for such thin layers. Interestingly enough, amorphous growth could also be obtained by applying a CH_4 plasma treatment (CH4PT) prior to a-Si:H deposition. As can be seen in Figure 3-30, applying a short CH_4 plasma treatment prevents the subsequent a-Si:H layer to grow epitaxially. The conditions used during the CH4PT are shown in Table 3-8.

T=200°C	CH4	SiH4	Pressure	Power	Dep. Time
Units	[sccm]	[sccm]	[mTorr]	[W]	[s]
CH4PT	50	0	50	2	30
a-Si:H	0	50	50	1	143

Table 3-8 – Plasma conditions for a CH4PT and a subsequent deposition of a thin a-Si:H passivating layer.

However, even if the layers are amorphous, the effective lifetime remains very low as shown in Figure 3-31. There might be two reasons for this. First, the CH_4 plasma treatment generates only carbonated radicals, mainly CH_3 radicals. Therefore, there are no SiH_3 radicals to dilute the carbon concentration in the gas phase. This will in turn increase the carbon concentration on the c-Si surface. The presence of carbon atoms can indeed be detrimental if the carbon atom density on the surface overwhelms the interface defect densities typically found at the interface of well-passivated wafers, i.e., ~10^{10}-10^{11} cm^{-3}. The second reason is that CH_4 plasmas can also lead to the growth of carbon films since methyl radicals (CH_3) are generally considered the most effective species for carbon thin film deposition[230].

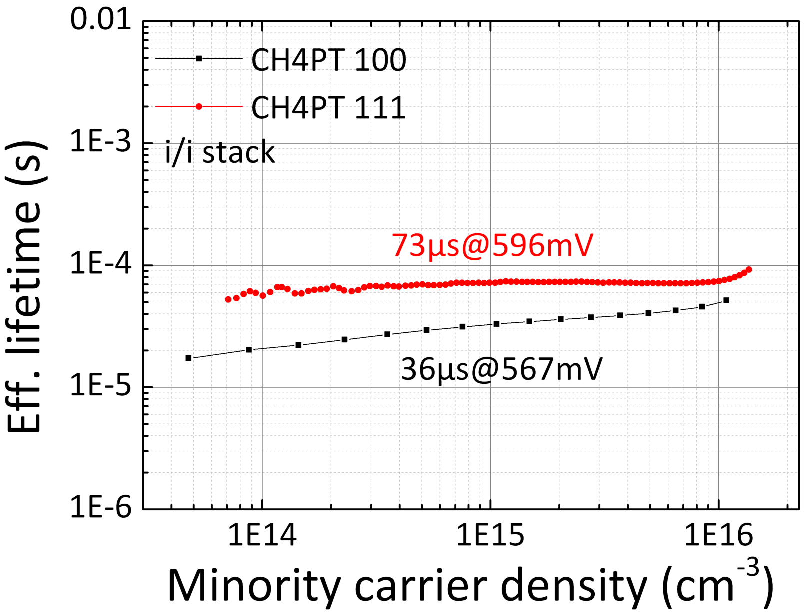

Figure 3-31 – Effective lifetime of two passivated samples after a CH4PT.

Incidentally, our conditions are very close to *Naito et al.*'s experiments in their paper dealing with the impact of H_2 dilution on the growth of carbon thin films in RF discharge CH_4 plasmas[231]. They have shown that diluting CH_4 in H_2 causes the deposition rate of the carbon thin film to decrease while keeping the CH_3 radical density constant. According to the authors, this is due to the decrease in the sticking probability of CH_3 radicals when the layer is growing, and also by the enhancement of etching mechanisms due to the presence of H_2. Therefore, our standard a-SiC:H layer deposition conditions can incorporate a much smaller amount of carbon at the interface, thus breaking the epitaxy while keeping the interface defect density low enough to achieve good passivation levels.

3.2.2.b Textured c-Si wafer passivation enhancement

Now, one might wonder how all these findings can be relevant to the passivation of textured c-Si. At first glance, texturation will lead to (111)-oriented c-Si surfaces in the form of pyramid facets.

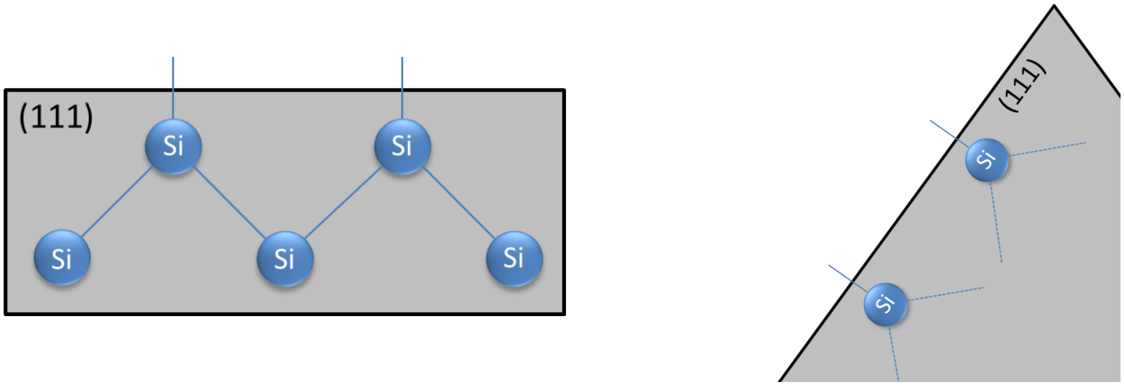

Figure 3-32 – Schematic representation of the 111 c-Si surface and its corresponding counterpart on a anisotropically wet-etched c-Si surface.

As was shown earlier in Figure 3-20 and Figure 3-21, our standard a-Si:H layer yields high effective lifetimes on (111) wafers, and one of the reason is that it grows completely amorphous on this kind of substrate.

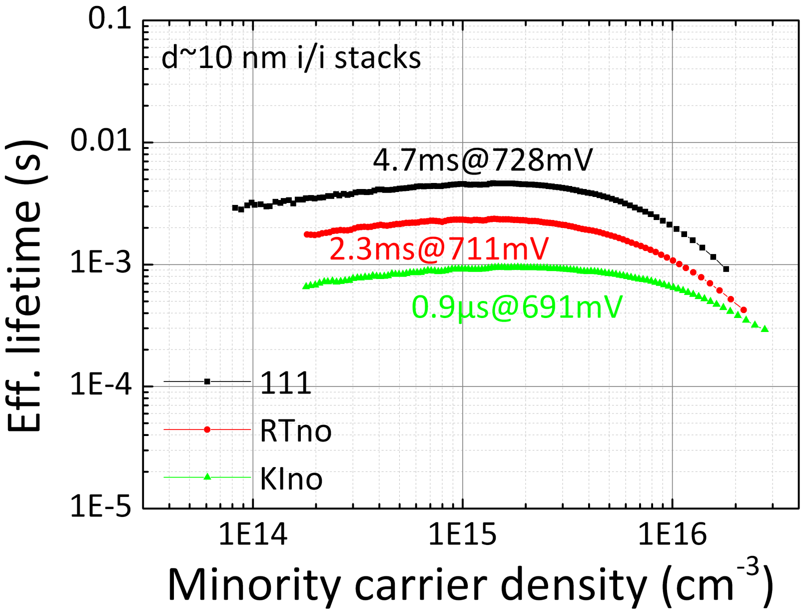

Figure 3-33 – Effective lifetimes of three passivated samples, a flat (111), an IPA-free textured (RTno) and a conventional KOH-IPA textured wafer.

However, when attempting passivation on textured substrates for the first time, we experienced a significant difference with flat (111) wafers. This can easily be understood when looking at the (111) surface that was presented in 2.1.3.b p.60. It is presented together with the schematic representation of a (111)-oriented facet of a typical pyramid obtained after anisotropic wet etching of (100) in Figure 3-32. As can be observed, the 3D landscape that arises upon texturing generates an increase in the effective surface (by a factor of √3 in fact). Therefore, the number of dangling bonds will also increase, resulting in a more challenging minimization of the interface defect density upon passivation. This effect is illustrated in Figure 3-33. For the same thickness of a standard a-Si:H layer, the passivation level differs significantly. In the case of (111) wafers, we usually reach lifetimes close to 5 ms with an iV_{OC} close to 730 mV. When passivating textured c-Si wafers, we witness an impact of the higher defect density at the a-Si:H/c-Si interface in the high-injection range. On the RTno wafer, the lifetime decreases to 50% of its initial value. For the KIno sample, the passivation level is even lower and we could not go beyond 1 ms, whereas the iV_{OC} stayed below 700 mV at 691 mV. This represents a decrease down to 25% of the initial value. The difference between the two types of texturing could be explained by the presence of contaminants at the interface of the KIno sample. Since we are using NaOH and KOH for texturation, the probability to find Na or K atoms at the c-Si surface despite the wet-chemical cleaning is not negligible. However, GDOES was performed on a KIno wafer capped with a thin SiO_2 layer and no trace of Na or K atoms was found. In Figure 3-34, the signal detected by the equipment starts by a sharp decrease for every signal but silicon. This is due to the fact that the surface naturally collects contaminants, even when stored in a nitrogen box. Then, the Si signal appears and stabilizes quickly, showing that we have started to etch the bulk of the wafer. Throughout the whole measurement however, Na and K signals remain below the detection limit, showing that there is no Na or K atoms at the c-Si surface. At least, there is no variation of Na and K atom content between the native oxide, SiO_2/c-Si interface and the c-Si bulk; which is already an important piece of information.

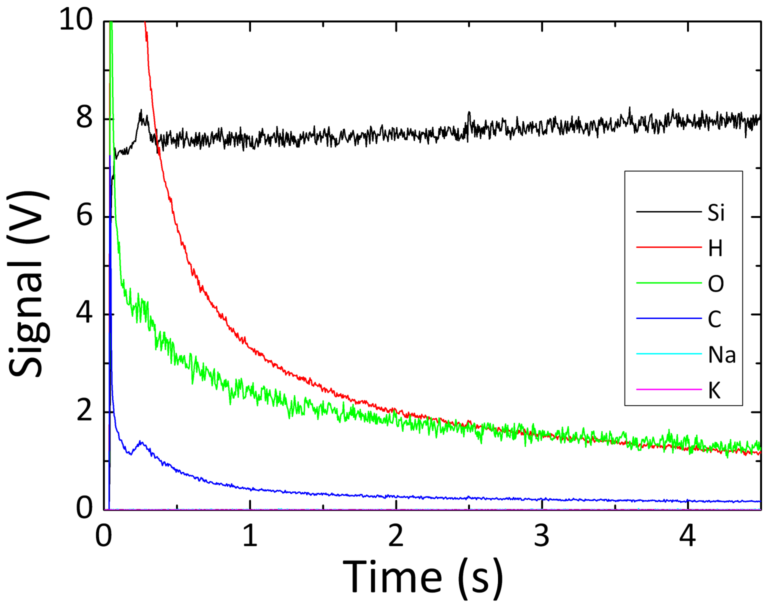

Figure 3-34 – Detected signals upon GDOES measurements for various atoms on a KIno wafer.

A second and more plausible explanation for such a discrepancy in the passivation results shown in Figure 3-33 could be that the RTno and KIno texturation recipes yield quite different pyramid landscapes. In particular, as shown earlier, KIno wafers exhibit higher pyramids, yielding much larger facet areas and thus increasing the number of dangling bonds to saturate at the c-Si surface upon a-Si:H passivation. This in turn naturally increases the defect density at the a-Si:H/c-Si interface. Besides, the two texturation recipes do not yield identical textured surfaces in terms of size homogeneity and texturing imperfections. In fact, *Stegemann et al.*[232][233] have shown that a large fraction of small pyramids will limit the effective lifetime by increasing the influence of the valleys and edges. *Deligiannis et al.* reported that the direct transfer from flat to textured is not necessarily obvious, and that an optimization of texturing and cleaning recipes can lead to higher passivation levels[234].

3.2.2.c Looking for epitaxial growth on textured c-Si wafers

Another explanation for the drop in effective lifetime with regard to the flat (111) reference that we wanted to explore though, was the possibility that despite the (111) orientation that anisotropically-etched (100) wafers exhibit, epitaxial growth could occur at the a-Si:H/c-Si interface. At first glance, we should not expect any epitaxial growth on textured c-Si surfaces. However, epitaxial growth has been reported on textured c-Si wafers by *Olibet et al.* [13][235]. Indeed, their experiments showed that in the pyramid valleys constituted by the intersection of two (111) planes, additional stress can occur leading to epitaxial growth. This is all the more true when these valleys are filled with small imperfections, such as nano-pyramids. In fact, they reported the existence of a distribution of crystalline orientations comprised between the (100) and the (111) orientation. In their study however, epitaxial growth occurred in the valleys when capping the thin a-Si:H passivating layer by a doped microcrystalline layer. The conditions therefore, were quite harsh, i.e., high H_2-dilution and high power. This is clearly not our case. However, we decided to take into account this possibility. The best way to validate this hypothesis was to consider that the pyramid bottoms of our textured samples could contain (100)-oriented imperfections. If this were really the case, depositing a-Si:H using our standard conditions should generate epitaxial growth on these (100)-oriented regions just as in the case of flat (100) wafers. To verify this assertion, we decided to fabricate test stacks by using the same technique as for (100) c-Si wafers, i.e. deposit a thin a-SiC:H layer at the a-Si:H/c-Si interface as schematically shown in Figure 3-35 and Figure 3-36. This was carried out on our two types of texturing recipes, i.e., RTno and KIno. The result is indeed striking and the corresponding PCD measurements are shown in Figure 3-37. As can be seen, for both texturing recipes, adding CH_4 during the first seconds of the a-Si:H deposition increased the effective lifetime.

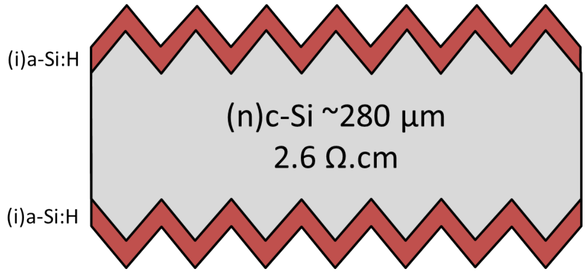

Figure 3-35 – Schematic representation of a randomly textured n-type crystalline silicon wafer capped by a pure a-Si :H layer at both a-Si:H/c-Si interfaces.

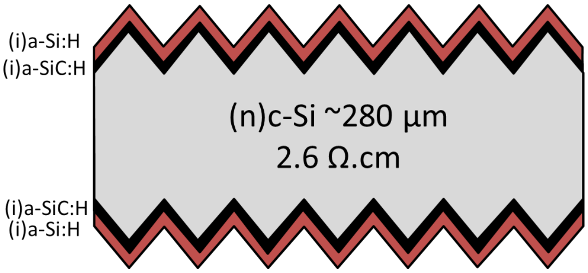

Figure 3-36 – Schematic representation of a randomly textured n-type crystalline silicon wafer capped by an a-SiC :H layer at both a-Si:H/c-Si interfaces.

In the case of our KIno sample, a 34% increase of the effective lifetime was found, whereas the iV_{OC} gained +6 mV. In the case of our RTno sample, the increase was even more striking, with a 60% increase for the effective lifetime and a iV_{OC} gain of +8 mV. Deposition conditions are shown in Table 3-9.

T=200°C	SiH4	CH4	Pressure	Power	Dep. Time
Units	[sccm]	[sccm]	[mTorr]	[W]	[s]
a-SiC:H	25	50	40	1	0 or 30
a-Si:H	50	0	50	1	254

Table 3-9 – Deposition conditions of an a-SiC:H/a-Si:H stack on the textured c-Si wafers described in Figure 3-36.

These measurements were obtained at 2E15 cm^{-3} for the effective lifetime and at 1 Sun for the iV_{OC}. However, we can see that these two samples evidenced an increase in the effective lifetime over the whole injection range. At very high-injection only, can we see the curves overlap in the RTno case, whereas in the case of KIno texturing, the two curves seem still separated, indicating an improved interface by a lowering of the defect density. At low-injection, we also see a major improvement as the signal is shifted by a constant. Indeed, the curves are parallel for both types of texturing, indicating no loss in the field-effect upon the introduction of carbon at the a-Si:H/c-Si interface. From these results we conclude that introducing a thin a-SiC:H layer at the a-Si:H/c-Si interface improves the passivation over the whole injection range and for different texturing recipes. This means that independently of the pyramid size distribution and sizes, there is a benefit to be gained by introducing this carbide layer. We must be cautious though and consider the possibility that this thin a-SiC:H layer can improve the passivation of the 111-oriented c-Si surface by other mechanisms than just breaking epitaxial growth.

T=200°C	SiH4	CH4	Pressure	Power	Dep. time
Units	[sccm]	[sccm]	[mTorr]	[W]	[s]
a-SiC:H	25	50	40	1	0 or 30
a-Si:H	50	0	50	1	254

Table 3-10 – Deposition conditions used on textured c-Si wafers described in Figure 3-37.

For this reason, two i/i stacks were fabricated on flat (111) wafers. One with a thin a-SiC:H layer at both a-Si:H/c-Si interfaces and the second sample without the latter-mentioned carbide buffer layer.

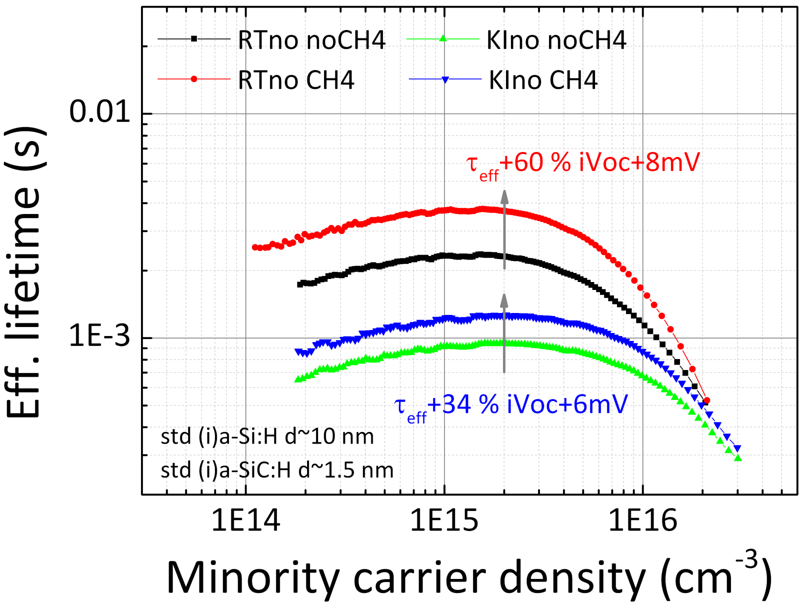

Figure 3-37 – Effective lifetime of RTno and KIno textured wafer passivated by a 10 nm-thick (i)a-Si:H layer with and without a thin a-SiC:H layer at the interface.

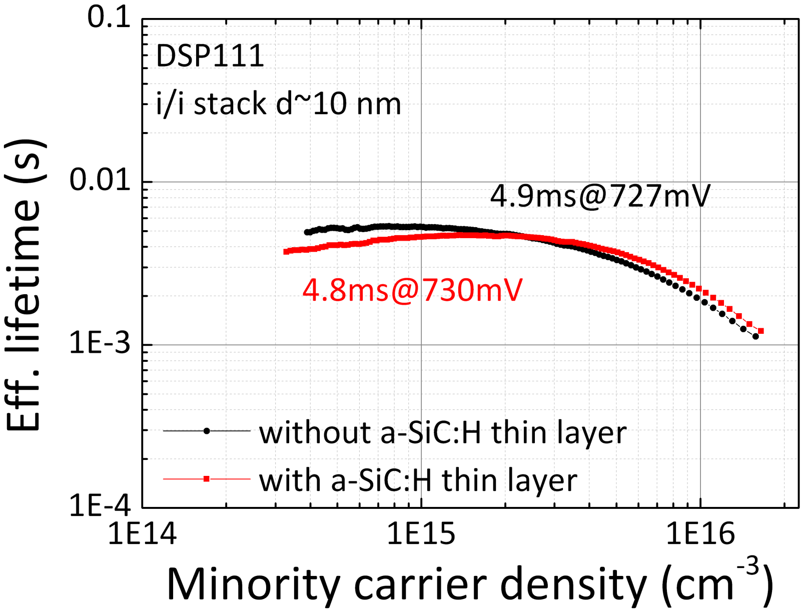

Figure 3-38 – Effective lifetimes of two i/i stacks on flat (111) wafers. One has a thin a-SiC:H layer at the a-Si:H/c-Si interface, the second does not.

Deposition conditions are shown in Table 3-10. If we are correct, adding carbon at the a-Si:H/c-Si layer should not improve the passivation of (111) wafers. If anything, it should lower it by introducing impurities at the a-Si:H/c-Si interface, but in no case should it improve it, since we do not experience epitaxial growth on (111) wafers under our standard conditions. PCD measurements were performed on both samples and results are shown in Figure 3-38. As expected, the two samples exhibit close-to-identical lifetime curves, and the effective lifetime at 2E15 cm^{-3} is actually a bit lower when introducing the thin a-SiC:H buffer layer. The iV_{OC} on the other hand seems a bit higher (+3 mV), but we believe that this small difference rather stems from the small reproducibility error that can occur when passivating samples in a PECVD reactor[31]. As a consequence, Figure 3-38 combined with Figure 3-27 demonstrate that the thin a-SiC:H layer at the interface has no other role than breaking epitaxial growth on the (100)-oriented c-Si surface. Therefore, all improvements that we experienced upon introduction of a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface of passivated textured c-Si wafers can be attributed to epitaxial growth impediment and not to any other passivation enhancement mechanism. To confirm the positive results obtained on KIno and RTno textured wafers, passivated in/in stacks were deposited using different c-Si substrates. A third kind of textured wafer, a 20 Ω·cm 140 µm-thick n-type wafer, was used. AFM mapping experiments were carried out on these wafers for comparison. Results are shown in Figure 3-39.

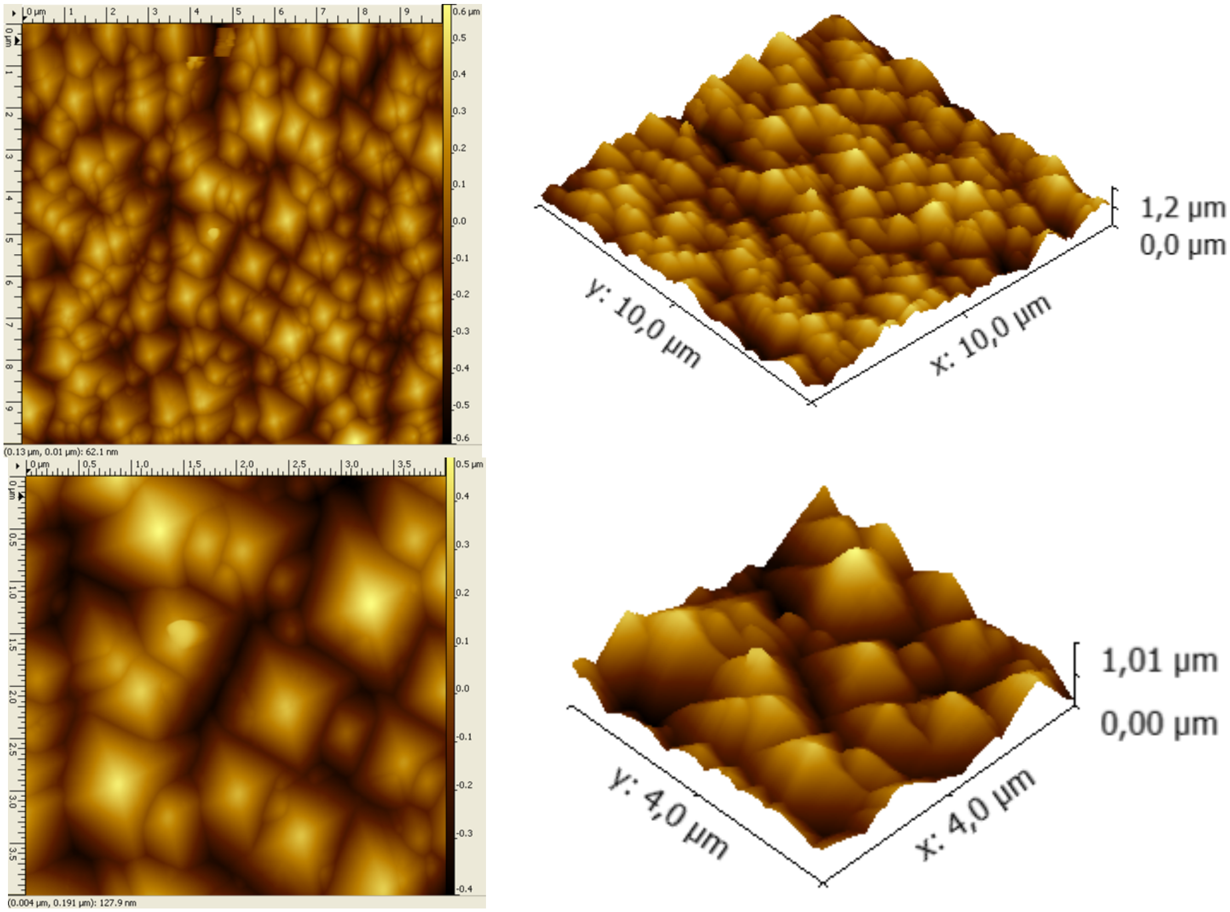

Figure 3-39 – AFM mapping of a 10x10 and 4x4 µm² region on a CAL textured wafer.

Here, we see that the landscape is very different with respect to our textured wafers. Indeed, the pyramids do not reach heights beyond 1 µm and their distribution looks quite homogeneous in comparison. Also, even if nanopyramids can be found in the valleys, there seems to be fewer imperfections present at the c-Si surface and between the crystalline planes. One could expect epitaxial growth to be less effective in this case, and the thin a-SiC:H layer at the interface to be less useful. Deposition conditions are shown in Table 3-11. The overall (i)a-Si:H has a thickness of about 5 nm and

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[31] Many things can impact the iV_{OC} of a sample: HF cleaning, cleanliness of the tweezers, substrate holder conditioning and last but not least, wafer positioning during PCD measurement.

half if it is made of a-SiC:H. The (n+)a-Si:H layer is quite thick to ensure a strong field-effect and its deposition time corresponds approximately to a 32-nm thickness. Results from the PCD measurements are striking. As can be seen in Figure 3-40, by adding a thin a-SiC:H layer at the a-Si:H/c-Si interface, we were able to enhance the passivation of our in/in stack on an industrially textured c-Si wafer. Indeed, the lifetime of our in/in stack goes from about 3.5 ms up to more than 5 ms! This represents a 60% increase. Likewise, by using this technique our iV_{OC} gains an additional +8 mV.

T=180°C	SiH4	CH4	PH3 (1%)	Pressure	Power	Dep. Time
Units	[sccm]			[mTorr]	[W]	[s]
(i)a-SiC:H	25	50	0	40	1	0 or 48
(i)a-Si:H	50	0	0	50	1	48
(n+)a-Si:H	50	0	1	60	1	579

Table 3-11 – Deposition conditions used on textured c-Si wafers described in Figure 3-40.

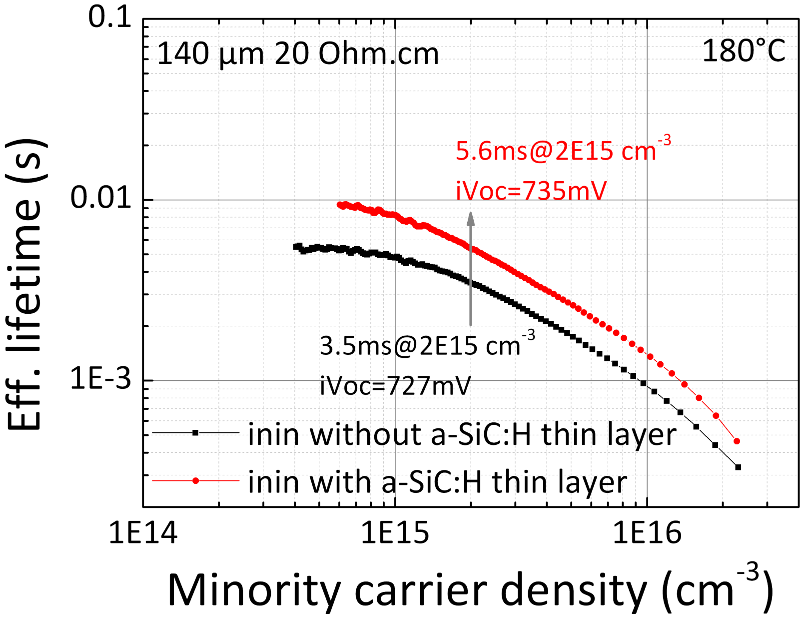

Figure 3-40 – Effective lifetime of an in/in stack deposited on a CAL textured wafer, with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface.

This means that even for very well-defined texturing recipes there is room for improvement, as epitaxial growth seems to be neutralized also on high-quality industrially-textured wafers. Moreover, it shows that the introduction of a thin a-SiC:H layer can be used in the case of very different types of n-type wafers (texturing, thickness, doping level,…). Finally, we see that this technique can be used at different deposition temperatures and that it does not screen the strong field-effect generated by the (n+)a-Si:H capping layer. This was already known for flat c-Si surfaces but was not at all obvious in the case of textured wafers. This open doors to the implementation of this technique in ip/ip stacks and, eventually, in HJ solar cell precursors with an a-SiC:H thin layer at the a-Si:H/c-Si interface. Having said that, we propose to study the a-Si:H/c-Si interface in more details to cross-check the results obtained so far.

3.2.2.d HR-TEM and STEM analyses on passivated KIno wafers

In order to carry out HR-TEM and STEM analyses, two KIno wafers were used. These underwent a cleaning procedure at LPICM consisting in a preliminary HF dip followed by a step in a Piranha bath whence all organic contaminants could be removed, and thin oxide layer was grown. Right before loading inside the PECVD reactor, the wafers underwent a 45 sec HF dip to remove the oxide. Two recipes were used so as to obtain the two structures described in Figure 3-35 and Figure 3-36, i.e., i/i stacks without and with a thin a-SiC:H layer at the a-Si:H/c-Si interface, yielding samples that we will henceforth refer to as *A* and *B*, respectively. PCD measurements were carried out prior to any further analysis. As shown in Figure 3-41, the sample with a thin a-SiC:H at the interface exhibits a higher effective lifetime (+70%) and the iV_{OC} yields a positive gain of +15 mV. In order to eliminate the possibility that contaminants could be present at the a-Si:H/c-Si interface of the sample with a lower effective lifetime, GDOES analyses were performed on both samples. Results showed that the Na and K signals remain below the detection limit. Based on these preliminary results and on the conclusions that were drawn earlier, we expected to find some structural differences at the a-Si:H/c-Si interface. More specifically, based on the results shown earlier, we could expect these to be in the form of epitaxial growth in the regions most submitted to stress, such as c-Si imperfections and V-shaped valley grooves.

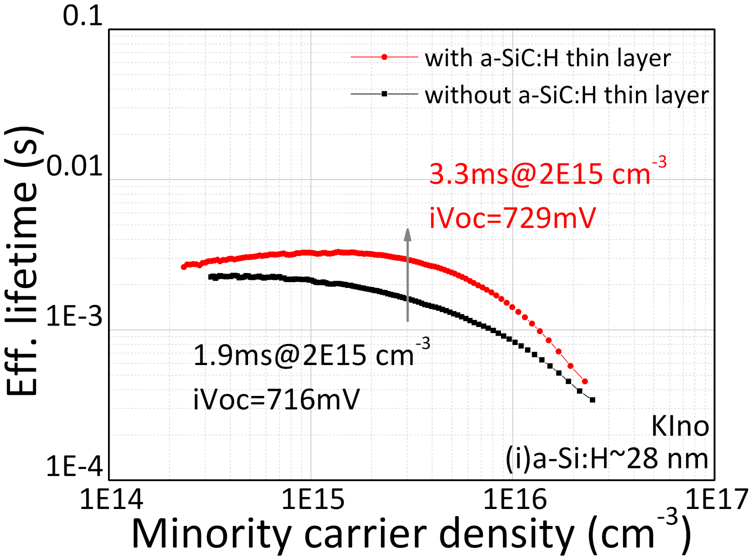

Figure 3-41 – Effective lifetime of two passivated KIno samples. One has a thin a-SiC:H layer at both a-Si:H/c-Si interfaces (black squares), the other one does not (red dots).

HR-TEM and STEM analyses of a KIno wafer passivated with our standard (i)a-Si:H layer (sample A)

HR-TEM analyses were performed on a KIno substrate passivated by a 28 nm-thick a-Si:H layer deposited under our standard conditions (sample A). It is worth mentioning again that it does not contain a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface, as shown in Figure 3-35. The lamella was prepared by ionic thinning on a Focused Ion Beam (FIB) using an Omniprobe-equipped Strata DB400. The sample was placed on a Cu grid and the thinning of the TEM lamella was controlled by SEM. The region on the textured c-Si wafer was selected in such a way that observations could be later made on the flanks and at the bottom of the pyramids, as shown in Figure 3-42. The lamella obtained after milling is shown in

Figure 3-43. TEM analyses were performed on a TEM JEOL 2200FS aberration-corrected microscope. In the STEM mode, all the electrons are concentrated in a probe (with an effective size of about 1 Angstrom thanks to the aberration probe corrector). This probe was scanning along the sample and we collected the electrons transmitted by the sample. There are two imaging modes of the electron microscope available: the bright field (BF) and the high-angle annular dark field (HAADF). In the BF geometry, we collected the electrons very close to the optical axis.

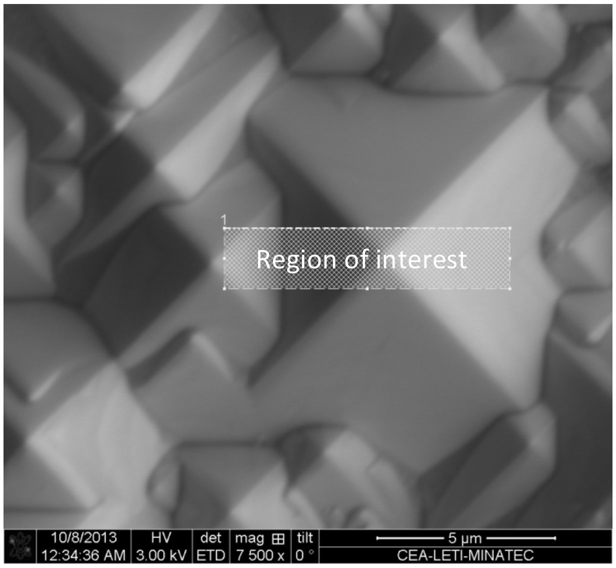

Figure 3-42 – Sample A observed by SEM from the top. The white section shows the region chosen for the preparation of lamella A.

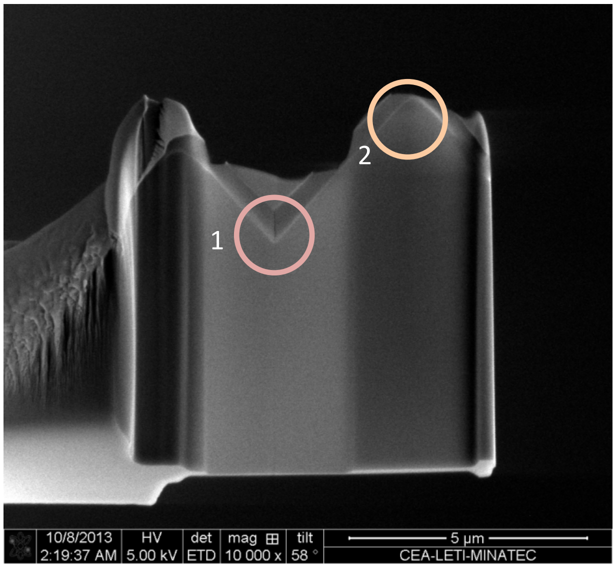

Figure 3-43 – SEM image of lamella A after coating, extraction and milling.

Therefore, we are more sensitive to the diffraction and to the deformation of the crystalline lattices. In this respect, the images acquired are very similar to HR-TEM images. In the HAADF geometry however, we collect the electrons that are elastically scattered by the atomic columns of the sample. This signal is comparable to a Rutherford scattering and the intensity of each atomic column varies with the square of their atomic number (Z^2). Therefore, we are more sensitive to the chemical composition of the nanostructure. The heavier the component, the higher the Z number (and thus Z^2) and the brighter it appears in the HAADF imaging mode.

HR-TEM and STEM analyses of the pyramid flanks

The goal of this study was to look for potential epitaxial growth at the a-Si:H/c-Si interface on a wafer that was found to yield a lower effective lifetime than if a thin a-SiC:H buffer layer were inserted (sample B). Figure 3-44 shows an HR-TEM image of our sample in region 1 (pyramid groove), whereas Figure 3-45 is a magnification of region 2 (pyramid tip). For each region, higher resolution images were made and are shown in Figure 3-46 and Figure 3-47, for regions 1 and 2, respectively. One can clearly distinguish the stack formed by the c-Si substrate and the a-Si:H layer. The protective SiO_x and platinum layers, needed for the preparation of the lamella can also be seen. More particularly, one can see platinum which penetrated in the a-Si:H layer over a few nanometers. When looking at the magnification of the valley (region1) in Figure 3-46, on the left-hand side flank close to the bottom of the pyramid, we can see two disruptions in the abruptness of the a-Si:H/c-Si interface. The first disruption i) (blue circle) is approximately 50 nm long and seems to penetrate 5 nm inside the a-Si:H layer. The second disruption ii) (green circle) at the a-Si:H/c-Si interface can be found in the lower part of the flank, closer to the valley bottom. The latter one extends on a slightly longer stretch but does not go beyond 1 or 2 nm within the a-Si:H layer. The two sections i) and ii) might be of interest as we suspect these imperfections at the a-Si:H/c-Si interface to be due to epitaxial growth. Figure 3-47 shows a magnification of the pyramid tip.

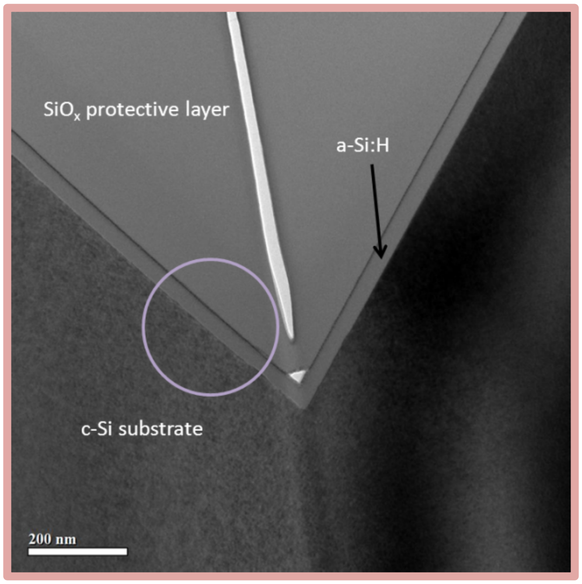

Figure 3-44 – HR-TEM magnification of region 1 (200 nm).

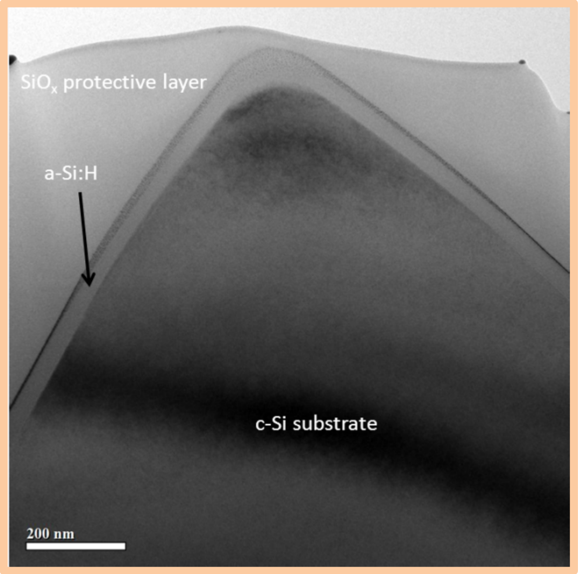

Figure 3-45 – HR-TEM magnification of region (200 nm).

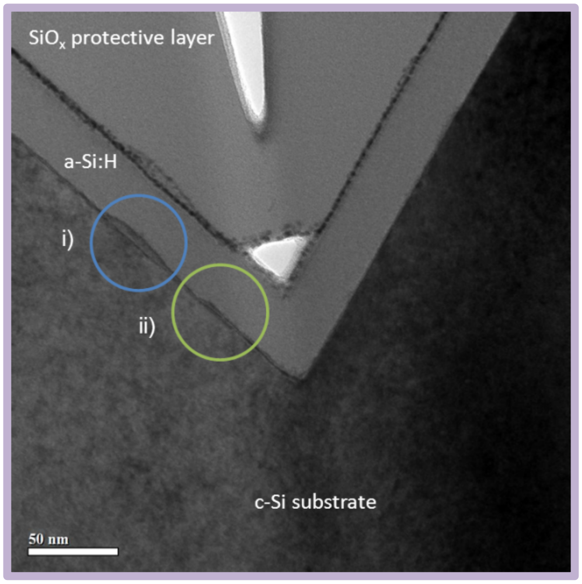

Figure 3-46 – HR-TEM magnification of region 1 (50 nm).

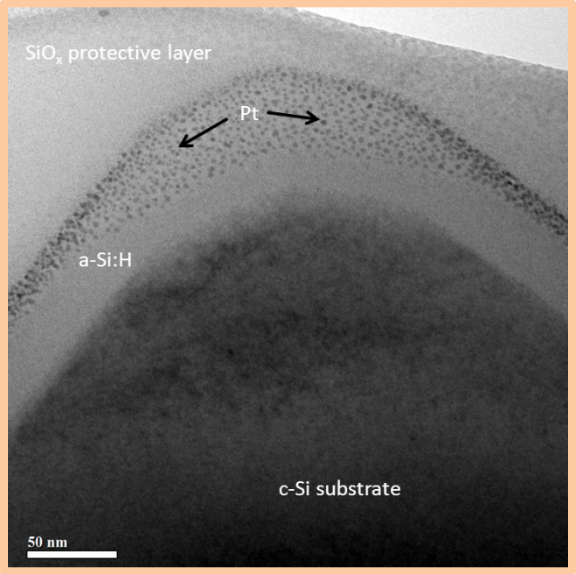

Figure 3-47 – HR-TEM magnification of region 2 (50 nm).

The a-Si:H/c-Si interface here does not seem very abrupt. Instead, we notice that the c-Si material from the wafer fades away until it transitions smoothly into the a-Si:H layer. This is probably due to the preparation of the sample which was done very close to the pyramid tip. As a result, this part of the lamella is very thin and we can expect some optical effects, which translate into extended transitions instead of clear contrast at the interface. This also explains why platinum penetrates so deeply inside the a-Si:H layer in this precise area and nowhere else. Despite the mixed phase observed, it seems that no imperfection, roughness or crystalline silicon plane is present, as opposed to what could be seen in regions i) and ii) of Figure 3-46. Therefore, our attention was focused on region 1, and sections i) and ii) were analyzed at a higher resolution. The HR-TEM images of region i) is shown in Figure 3-48 whereas Figure 3-49 shows region ii). First, the magnification of section i) shows how deeply the protuberance penetrates into the a-Si:H layer, thereby confirming the 5-6 nm value for this section. In the case of section ii) the 1 nm value is also confirmed.

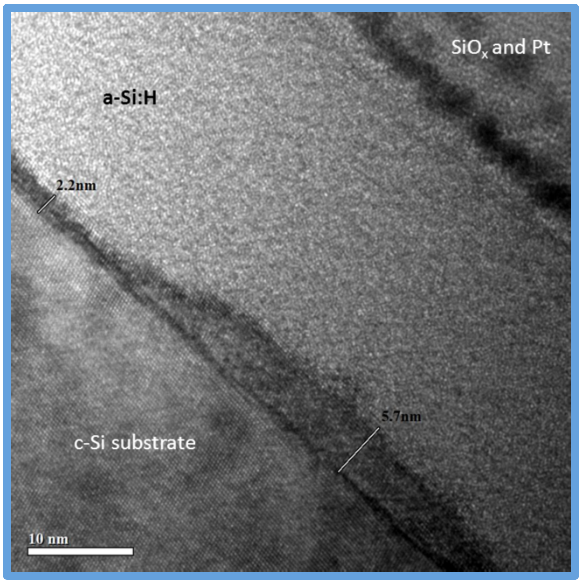

Figure 3-48 – HR-TEM magnification of section i) (10 nm).

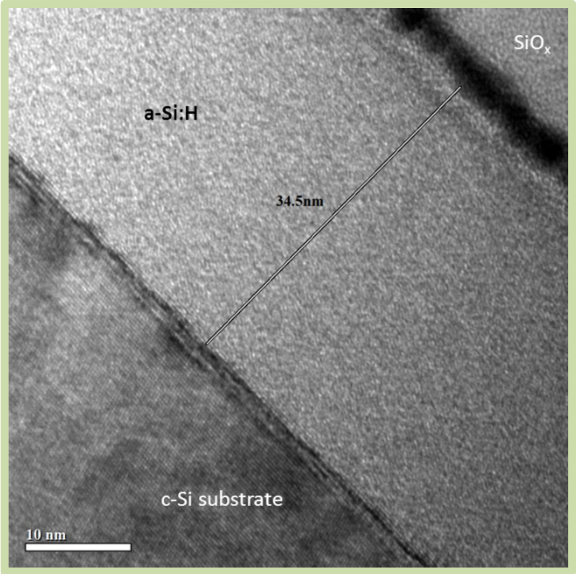

Figure 3-49 – HR-TEM magnification of section ii) (10 nm).

The interface disruptions are clearly crystalline since we can see the crystalline network up to the edge of the imperfections. However, at this point it is hard to tell if the imperfections are part of the c-Si substrate or if they are indicative of the occurrence of epitaxial growth at the a-Si:H/c-Si interface. In order to verify the above, a much higher-resolution image was obtained, as shown in Figure 3-50. Here again, it seems that the imperfection per se, even though it is obviously made of a crystalline network, is an imperfection that is part of the c-Si wafer rather than made of epitaxial layers grown on silicon. Since we were working at HR-TEM resolution limits, we decided to perform Scanning Transmission Electron Microscopy (STEM) analyses to study this region in greater depth. Figure 3-51 shows two high-resolution STEM images obtained in High-Angular Annular Dark-Field (HAADF) and Bright-Field (BF) imaging modes of the electron microscope in parts a) and b), respectively. As stated earlier, the HAADF mode is more sensitive to the density of the film because of its dependence on Z^2. On the image shown in Figure 3-51a), we see that the c-Si imperfection is much darker than the c-Si substrate. This indicates that the imperfection, which penetrates approximately 5 to 8 nm deep into the a-Si:H network, is either not very thick in volume or not fully crystalline. Consequently, this part of the sample should be due to roughness of nanometric size. Since the lamella thicknesses ranges from 50-100 nm, this means that such roughness would extend less than 50-100 nm in the z direction. However, epitaxial growth is not to be excluded, since the crystalline planes appear to have a lower density than the c-Si substrate underneath. Indeed, the same patterns have been observed by *Moreno et al.*[208] at PICM and by other groups like the AIST[217]. Their conditions were slightly different and the epitaxial growth usually extends over a much greater thickness. However, the difference in density could also be observed when comparing the epitaxial layers with the c-Si substrate underneath. Figure 3-51b) shows a STEM-BF image of the same flank. Here, we see that the shape of the crystalline imperfection matches the density contrast seen on the STEM-HAADF image. Indeed, in this mode more sensitive to the shape, we see that beyond this imperfection, no crystalline organization typical of epitaxial growth can be found in the amorphous network. In order to confirm the observation made on the STEM-HAADF image, density profiles were extracted from Figure 3-51a).

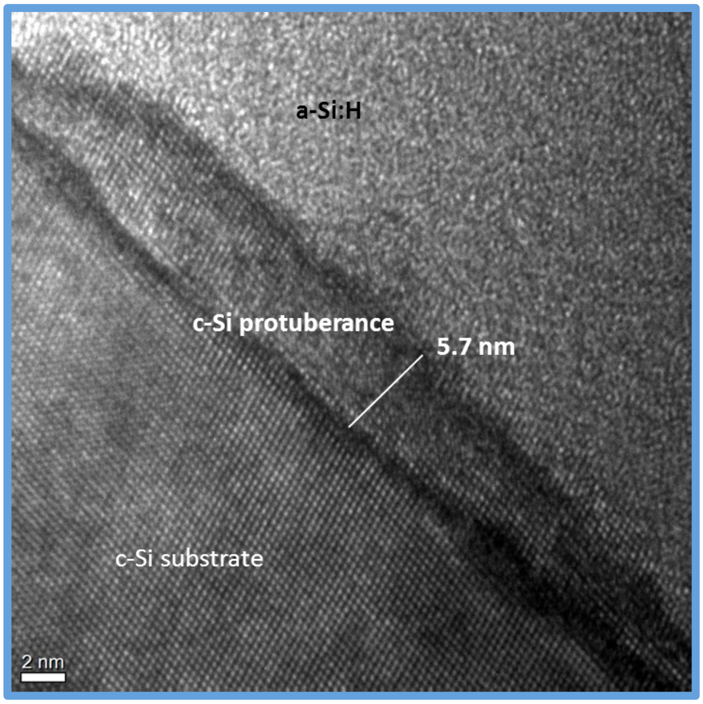

Figure 3-50 – HR-TEM magnification of section i) (2 nm).

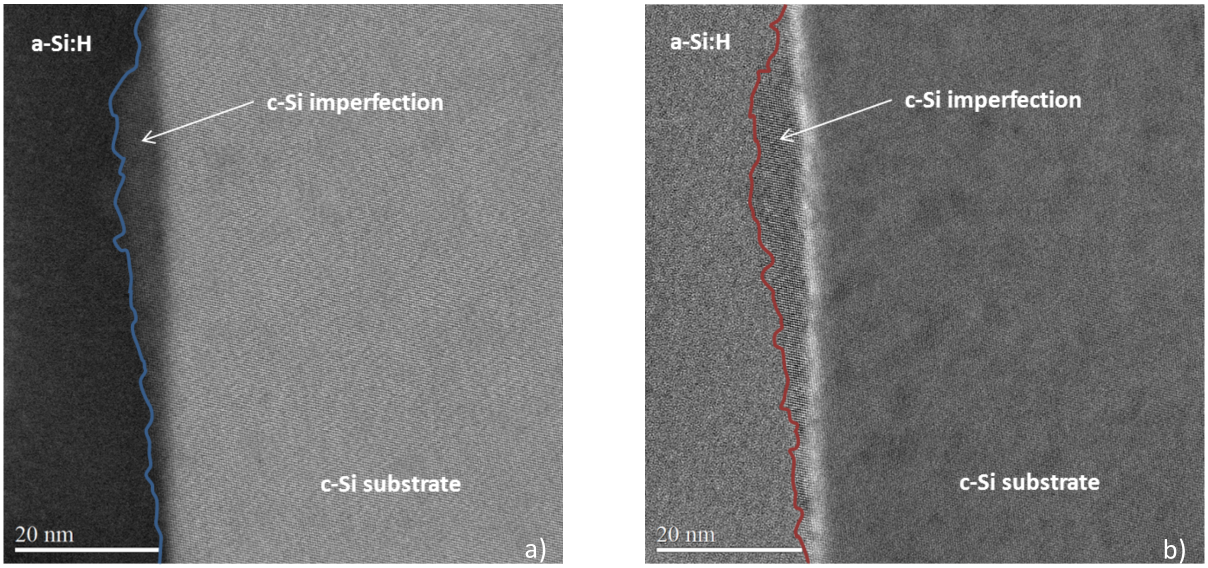

Figure 3-51 – STEM-HAADF (part a) and STEM-BF (part b) images of a pyramid flank of sample A (20 nm).

Two sections of the flank were analyzed. Figure 3-52a) and b) show the density profiles obtained for both sections. Section 2a is situated in the middle of the c-Si imperfection, whereas section 2b is located at its upper edge (inset images). As can be seen, the two density profiles differ. The most striking feature is surely the presence of a plateau in section 2a while the transition at the a-Si:H/c-Si interface in section 2b is very smooth. Indeed, Figure 3-52a) shows that at the a-Si:H/c-Si interface, the density stabilizes at a value that is lower than that of c-Si but higher than that of a-Si:H. Such a constant intensity is only possible if the density does not vary throughout the sample thickness, in the z direction. Since the density is much lower than c-Si, and since this kind of profile could be found on different parts of the flank under study, the presence of local epitaxial growth on the flank of Figure 3-51 was confirmed.

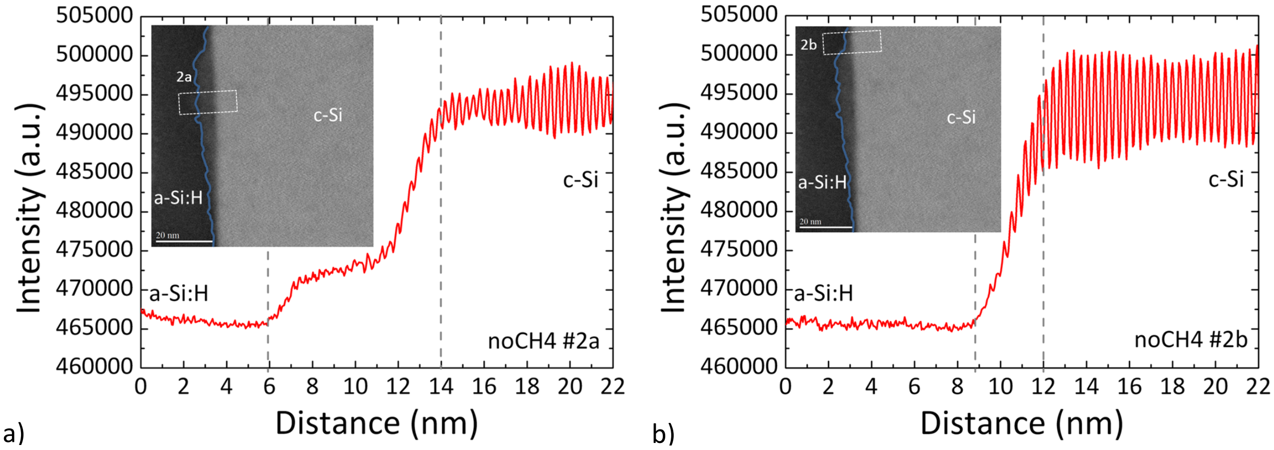

Figure 3-52 – Density profiles extracted from the STEM-HAADF image shown in Figure 3-57. Two sections are analyzed: 2a (left) and 2b (right).

For comparison purposes, two other sections from different pyramid flanks are shown in Figure 3-54 and Figure 3-55. Figure 3-53 helps situate both flanks on the lamella, wherein sections iii) and iv) are defined by a grey and blue circle, respectively. In both sections, the interface is very straight and abrupt when compared to what could be seen in sections i) and ii) of Figure 3-46.

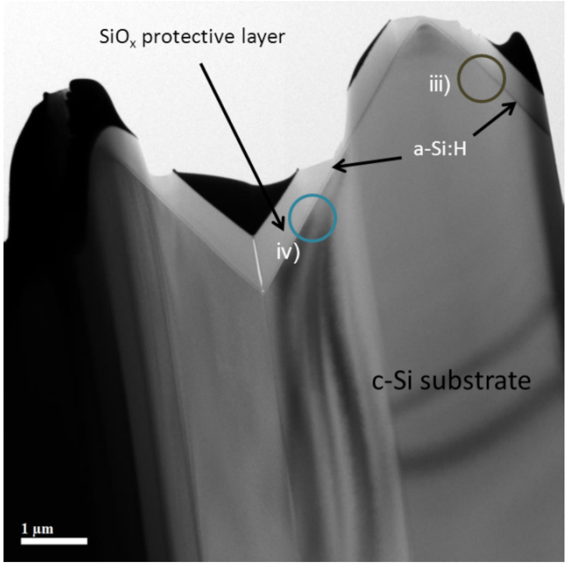

Figure 3-53 – General view of lamella A with the two regions of interest circled.

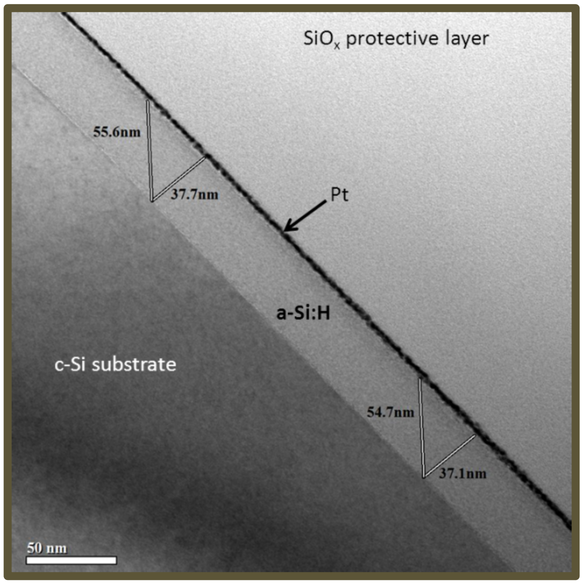

Figure 3-54 – Magnification of section iii).

Indeed, no disruption or visible imperfection is observed, at least at this resolution. To confirm this, a magnification is shown in Figure 3-55b). As can be seen, the a-Si:H/c-Si interface is very neat and abrupt and no signs of epitaxial growth can be seen.

So far, we have analyzed several sections of the flanks of a pyramid defined by two (111) c-Si crystallographic planes of an anisotropically-etched (100) wafer. Thanks to HR-TEM analyses, the presence of crystalline planes at the a-Si:H/c-Si interface was confirmed. STEM analyses on the other hand allowed for the detection of a variation of the material density across the interface. Density profiles were carried out on STEM-HAADF images and, the presence of an intensity plateau at the a-Si:H/c-Si interface confirmed the epitaxial nature of the crystalline planes observed. We then decided to explore the bottom of the pyramid valleys, since this section had already been reported as more prone to epitaxial growth[13][235].

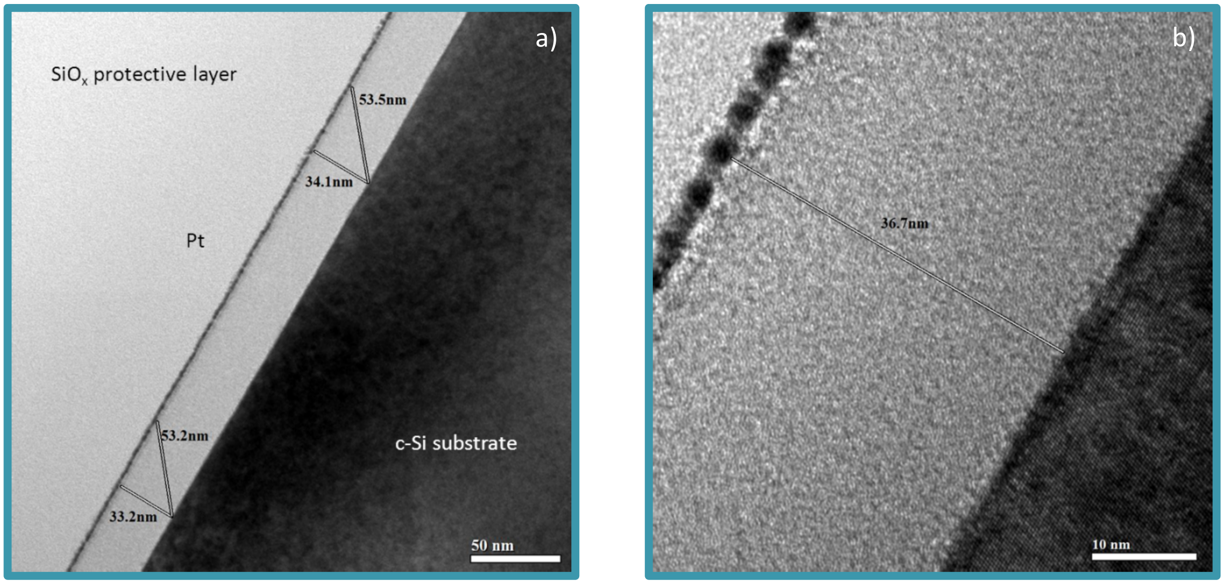

Figure 3-55 – HR-TEM images of lamella A shown in two different magnifications.

HR-TEM and STEM analyses in the pyramid groove

As stated earlier, we expected imperfections, such as local (100) regions, to foster epitaxial growth. As demonstrated above, we could confirm epitaxial growth on the pyramid flanks. However, it is still unclear what could foster such a phenomenon. Figure 3-56 shows the HR-TEM images taken at the bottom of the pyramid in region 1 of Figure 3-43 at two resolution levels. In Figure 3-56a), we can see some roughness and imperfections in this region, which actually are a continuation of the long imperfection found on the pyramid flank and shown in Figure 3-46. A magnification thereof is shown in Figure 3-56b) on which we can clearly see that these affect the shape of the valley. Instead of the expected V-shaped valley, the interface exhibits a U-shaped valley with a transition region that is clearly crystalline. It is difficult at such resolution however to dissociate the imperfections of the c-Si surface from any potential epitaxial growth. Part of these crystalline planes seems to belong to the c-Si wafer. However, on top of these imperfections of the c-Si substrate, the a-Si:H deposition seems to have generated the apparition of crystalline planes. Since we were reaching the resolution limits of the HR-TEM equipment, STEM analyses were carried out to study the a-Si:H/c-Si interface in this region with greater accuracy. The results of this analysis are shown in Figure 3-57. In part a) the HAADF imaging mode of the electron microscope, which is more sensitive to material density, shows the limits (blue line) of the c-Si wafer (brighter parts). Darker regions containing crystalline planes can be distinguished at the a-Si:H/c-Si interface. These could belong to the substrate and testify to some roughness at its surface. From the STEM-BF image shown in part b), more sensitive to diffraction and therefore to the shape of the interface, epitaxial growth can potentially be deduced from the crystalline planes that appear beyond the c-Si wafer limits detected on the STEM-HAADF image. It is hard to say with certainty if these crystalline planes are the result of epitaxial growth or not since these could be the result of the detection of some parts of the c-Si substrate in the background.

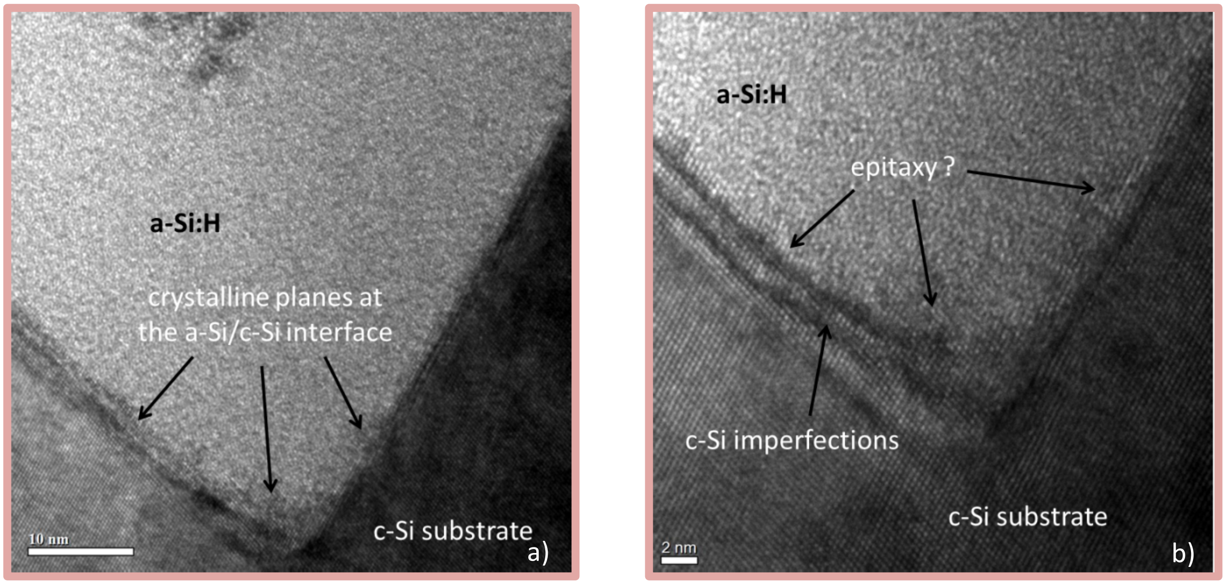

Figure 3-56 – HR-TEM images of the bottom of the pyramid valley of region 1 presented in Figure 3-43.

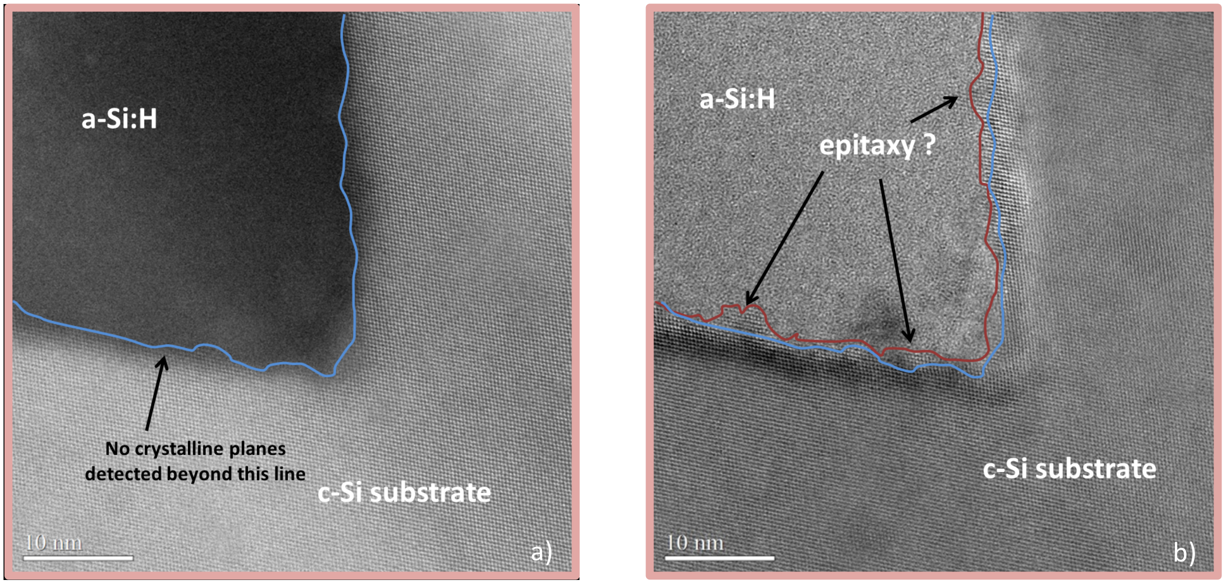

Figure 3-57 – STEM-HAADF (part a) and STEM-BF (part b) images of a valley of our textured sample passivated with a 27 nm-thick a-Si:H layer.

In other words, we would be detecting roughness of the c-Si substrate only. These crystalline planes could also be due to silicon redeposition phenomena sometimes associated with FIB preparation. This could be verified by comparing with another sample that underwent FIB preparation together with sample A. However, density profiles could yield interesting information, just as in the case of the pyramid flank previously analyzed. Consequently, density profiles were extracted from STEM-HAADF images. Figure 3-58a) and b) show the profile density across the a-Si:H/c-Si interface in two distinct regions close to the bottom of the pyramid valley. As can be seen, despite the crystalline planes observable beyond the interface defined in Figure 3-57b) by the atom density variation, both analyses yield very similar density profiles. Indeed, the oscillations differ between these two sections, probably because the 1a profile was not made perfectly perpendicularly to the a-Si:H/c-Si interface.

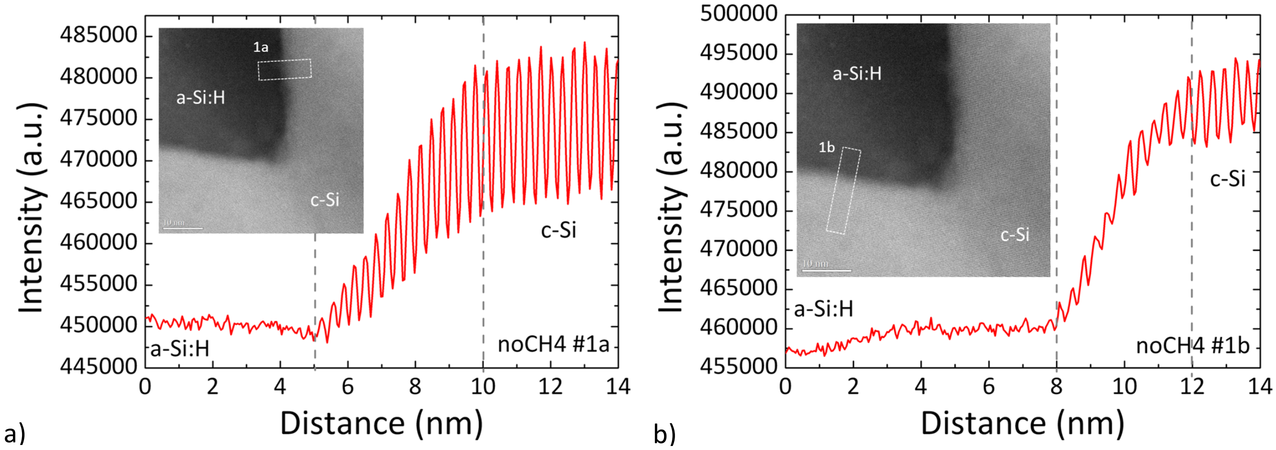

Figure 3-58 – Density profiles extracted from the STEM-HAADF image shown in Figure 3-57a). Two sections are analyzed: 1a (left) and 1b (right).

However, the intensity transition (and thus Z^2) drops, while going from the substrate to the a-Si:H layer at the same pace, over a 2-2.5 nm length. This shows that despite the differences observed in the shape or with the presence of crystalline planes at the interface, sections 1a and 1b are similar. Also, the fact that the mass transition is smooth at the a-Si:H/c-Si shows that the density is never constant. Therefore, it is clear that the crystalline planes that can be observed at the interface are not present throughout the sample, in the z direction. This allowed us to exclude the presence of epitaxy, as opposed to what could be observed on the pyramid flank above.

To conclude with sample A, crystalline planes could be observed by HR-TEM analyses both on the pyramid flanks and in the valley bottoms. STEM analyses allowed us to detect variations in the density and to extract density profiles. As a result, we observed smooth transitions from the c-Si substrate to the a-Si:H layer most of the time. This shows that the crystalline planes are rather part of the c-Si substrate and form roughness of nanometric size. However, in one section of a pyramid flank, the stabilization of the density at an intermediate value between those of c-Si and a-Si:H points at an epitaxially-grown crystalline lattice. Moreover, in regions where epitaxy was thought to be fostered, such as valley bottoms, density profiles resulted in smooth a-Si:H/c-Si interfaces, despite the lack of apparent abruptness on HR-TEM images. To verify this, a comparison with sample B could prove useful inasmuch as the presence of a thin a-SiC:H layer at the a-Si:H/c-Si interface must have impeded all epitaxial growth, both at smooth and rough parts of the c-Si substrate. We should then be able to see the abruptness of the a-Si:H/c-Si interface in regions comparable to the ones previously studied. Moreover, the detection of any potential silicon redeposition phenomenon possibly occurring upon FIB lamella preparation should become obvious.

HR-TEM and STEM analyses of a KIno wafer passivated by a a-SiC:H/a-Si:H stack (sample B)

The second sample (sample B) was deposited on the same kind of textured wafers (KIno), during the same PECVD pump-down, and underwent the same cleaning procedure as sample A. On both a-Si:H/c-Si interfaces a thin a-SiC:H layer was deposited to prevent any epitaxial growth upon a-Si:H deposition on potential (100)-oriented surface imperfections. The same thickness was used as in the case of the previous sample (sample A with no a-SiC:H at the a-Si:H/c-Si interface). For more details, one is referred to the passivated structure described in Figure 3-36. This sample underwent FIB preparation together with sample A. This allowed for a more thorough comparison. The sample was placed on a Cu grid and the thinning of the TEM lamella was controlled by SEM. The region on the textured c-Si wafer was chosen in such a way as to provide for observations to be made later on the flanks and at the bottom of the pyramid groove, as shown in Figure 3-59. It is noteworthy that there seems to be a higher local density of imperfections than in the case of sample A. Indeed, nanopyramids and surface anomalies can be observed in several sections of the landscape. This could make the comparison by microscopy more challenging since we do not know how efficient a-SiC:H deposition was on all of these particular regions. However, the region of interest shown in Figure 3-59 was chosen so that the section would be comparable with that of sample A, i.e., removed from such texturing imperfections. Moreover, PCD measurements carried out on both samples have clearly demonstrated that the passivation level was superior on sample B than on sample A, despite the higher imperfection density. The lamella obtained after milling is shown in Figure 3-60. On this image, color circles indicate the 5 different sections where HR-TEM and/or STEM analyses were carried out. As can be seen, different flanks are analyzed in the lower and higher parts of the pyramid, as well as at the pyramid tip and groove levels.

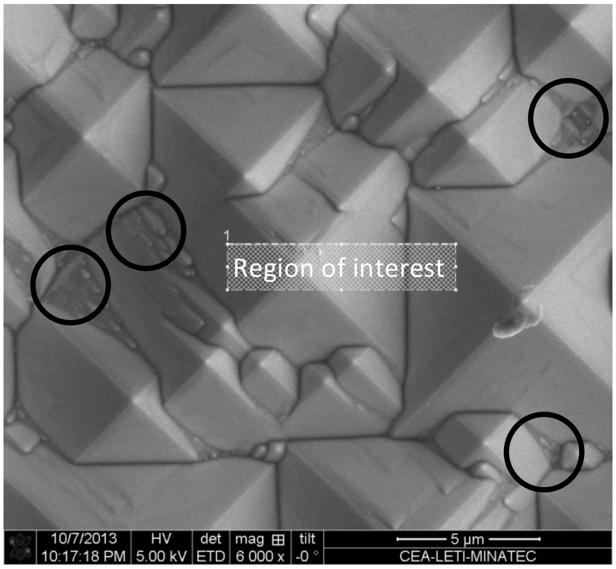

Figure 3-59 – Sample B, as observed by SEM from the top. The white section shows the region chosen for lamella preparation whereas circled sections point at local texturing imperfections.

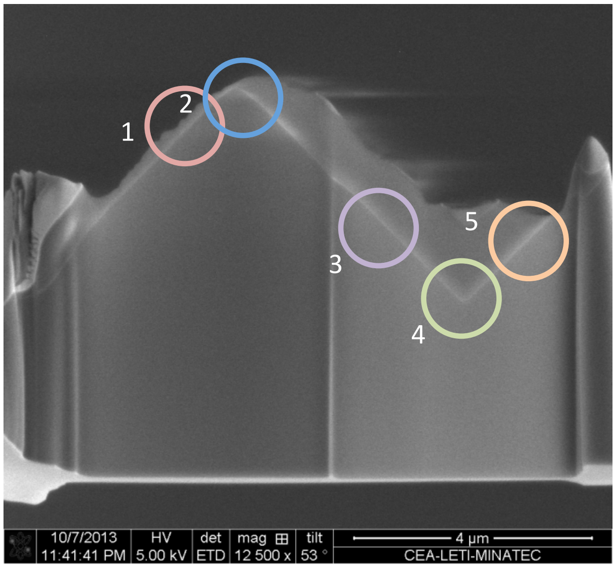

Figure 3-60 – SEM image of lamella B following coating, extraction and milling.

HR-TEM and STEM analyses at the pyramid flanks

As in the case of sample A, we started by analyzing the a-Si:H/c-Si interface on pyramid flanks selected in various regions of the lamella. Figure 3-61a) shows region 1 situated on a flank of a pyramid, closer to its tip than to its lower part.

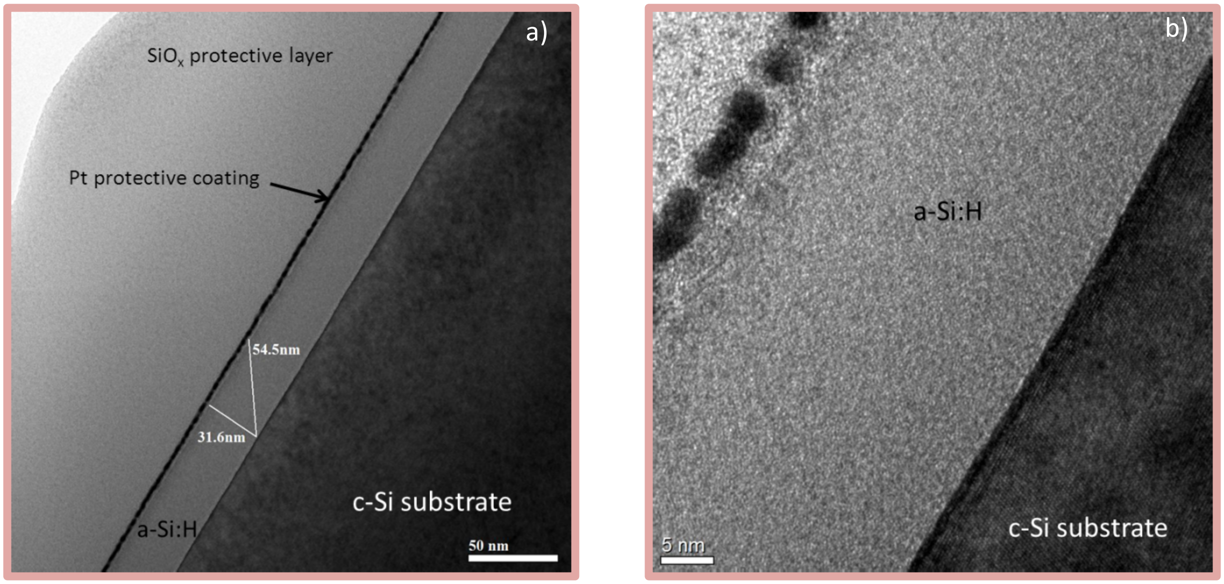

Figure 3-61 – HR-TEM images of region 1 presented in Figure 3-60.

Again, the nice contrasts help us distinguish the three main parts of the sample: the c-Si substrate (darker area) and the a-Si:H layer (lighter area), which are separated from the protective SiO$_x$ layer by a thin Pt coating (black line).

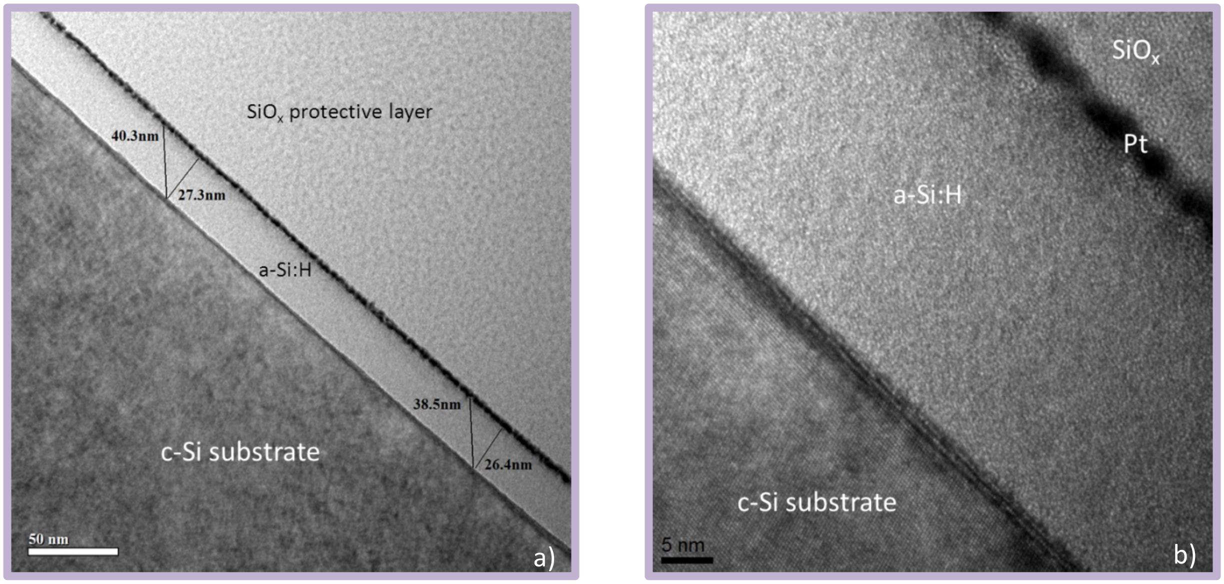

Figure 3-62 – HR-TEM images of region 3 presented in Figure 3-60.

On this image we already can notice the abruptness of the a-Si:H/c-Si interface. This is confirmed on the magnification shown in Figure 3-61b). Indeed, in this particular part, the sharpness of the a-Si:H/c-Si interface is quite comparable to the one that can be observed when depositing a-Si:H on a flat

(111)-oriented wafer, as we shall see later. However, in region 3, we can distinguish some roughness on some parts of the pyramid flank, as shown in Figure 3-62a). A magnification of this section is shown in Figure 3-62b). However, the roughness detected at the a-Si:H/c-Si transition seems quite small. This image can be considered a reference for a smooth interface compared to sample A, since no epitaxial growth can possibly occur thanks to both to (111) orientation and the presence of the thin a-SiC:H layer. Figure 3-63 shows a STEM-HAADF image of a pyramid flank (region 5). As can be seen, the sensitivity of this mode to the material density allows us to define the three different regions involved in the passivated structure.

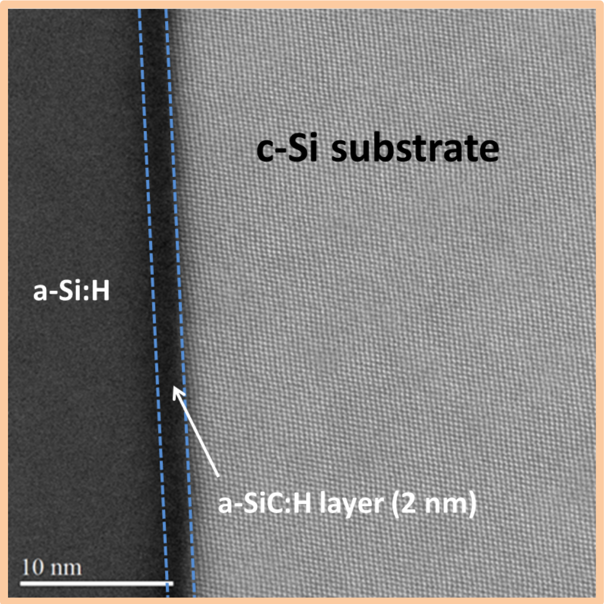

Figure 3-63 – STEM-HAADF image of region 5 shown in Figure 3-60.

The densest part is, of course, the c-Si substrate, which has a low defect density and hydrogen content. The a-Si:H layer is then easily recognizable since it appears darker (less dense) and is quite thick at this scale.

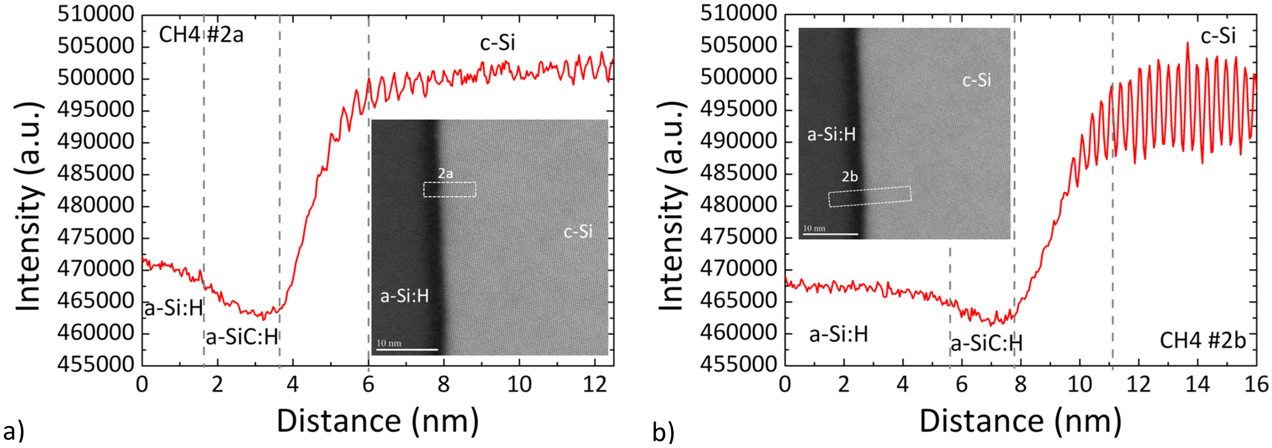

Figure 3-64 – Density profiles extracted from the STEM-HAADF image shown in Figure 3-63. Two sections are analyzed: 2a (left) and 2b (right).

The 2-nm thick a-SiC:H layer is the darkest part in the picture however, and therefore the less dense material of the passivated stack. Density profiles conducted in this region confirm this trend.

Figure 3-64a) and b) shows the density profile across the a-Si:H/c-Si interface shown in Figure 3-63. As can be seen, sections 2a and 2b exhibit similar density profiles. The stronger oscillations in Figure 3-64b) stems from an analysis carried out slightly off the normal at the a-Si:H/c-Si interface compared to Figure 3-64a). The slopes are comparable in both sections and we experience a small drop in density (between 1.8 and 3.8 nm in section 2a and between 5.6 and 7.8 nm in section 2b due to the presence of carbon at the interface. It is noteworthy that this slight drop occurs after the density transition. Therefore, the regions between 4 and 6 nm in section 2a and between 8 and 11 nm in section 2b are indeed part of the substrate. This confirms our conclusions drawn earlier on sample A.

HR-TEM and STEM analyses at the pyramid tip

Region 2, namely the pyramid tip, was analyzed, yielding the HR-TEM images shown in Figure 3-65. Just as in the case of sample A, the a-Si:H/c-Si interface does not seem very abrupt and we notice again, that the c-Si material from the wafer fades away, until it transitions smoothly into the a-Si:H layer. This confirms our earlier observations on sample As this effect being due to the preparation of the sample as well as to the small thickness of the lamella in this region. In the high-resolution magnification of Figure 3-66, we can observe how the crystalline planes smoothly vanish, leading to a fully amorphous phase.

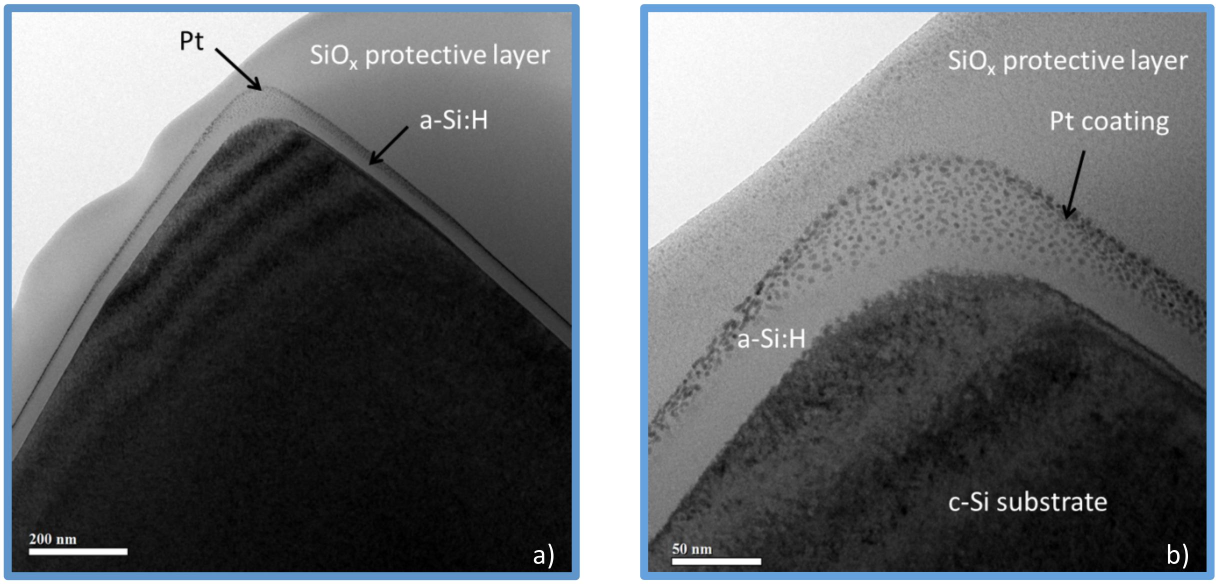

Figure 3-65 – Two HR-TEM magnifications of region 1 of sample B.

Again, platinum is quite present in this part, pointing to a deeper penetration into the a-Si:H material than in other parts of the lamella. Despite the mixed phase observed, it seems that no imperfection, roughness or crystalline silicon plane is present. Indeed, because of the particularity of the region (lamella thickness, cutting edge), the irregularities observed at the pyramid tip cannot be interpreted as roughness. Owing to the presence of carbon however, we can again use this image as a reference for a typical and abrupt a-Si:H/c-Si interface in this specific part of the pyramid.

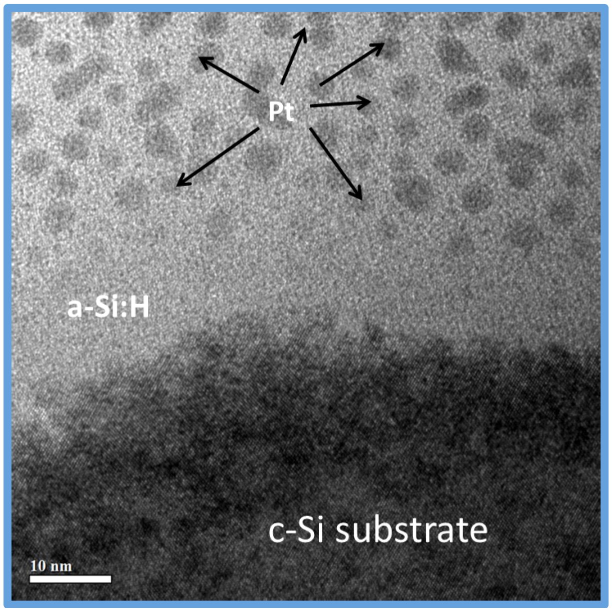

Figure 3-66 – HR-TEM magnification of the pyramid tip (region 2).

HR-TEM and STEM analyses in the pyramid groove

Finally, region 4, which stands for the pyramid groove, was analyzed. HR-TEM images of this region are shown in Figure 3-67. On the first magnification (Figure 3-67a), the a-Si:H/c-Si interface looks perfectly smooth and abrupt on both sides of the valley, from the upper part down to the bottom. On the second magnification however (Figure 3-67b), some roughness can be detected at the bottom of the valley. On this image it looks quite significant, similarly to what we observed in the pyramid groove on sample A. However, when looking at a higher resolution, as opposed to sample A, the interface looks quite abrupt despite the observed roughness at the bottom, as shown in Figure 3-68.

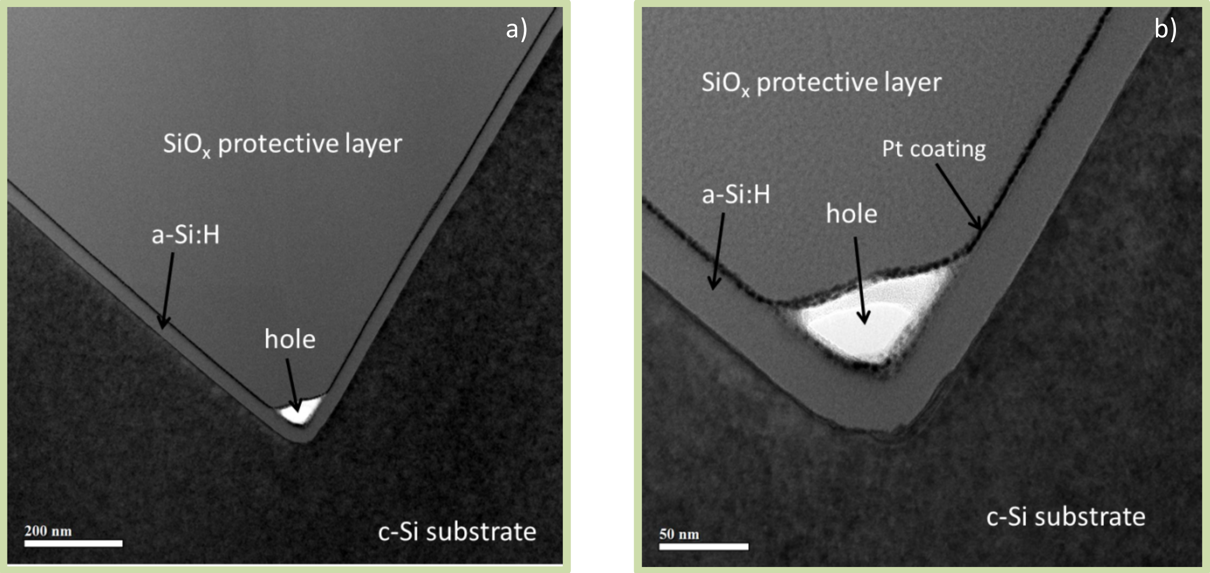

Figure 3-67 – Two HR-TEM magnifications of region 4 of sample B.

Indeed, epitaxial growth is made impossible on this sample by the presence of carbon. Therefore, the crystalline silicon parts penetrating within the a-Si:H materials must come from the substrate and such patterns are optical artifacts detected on the analysis. This image can be considered as a reference, especially to draw conclusions from the previous analyses conducted on sample A. In order to study this region in more details, STEM analyses were carried out. Figure 3-69a) shows a STEM-HAADF image on which we can detect the contrast between the different parts of the sample.

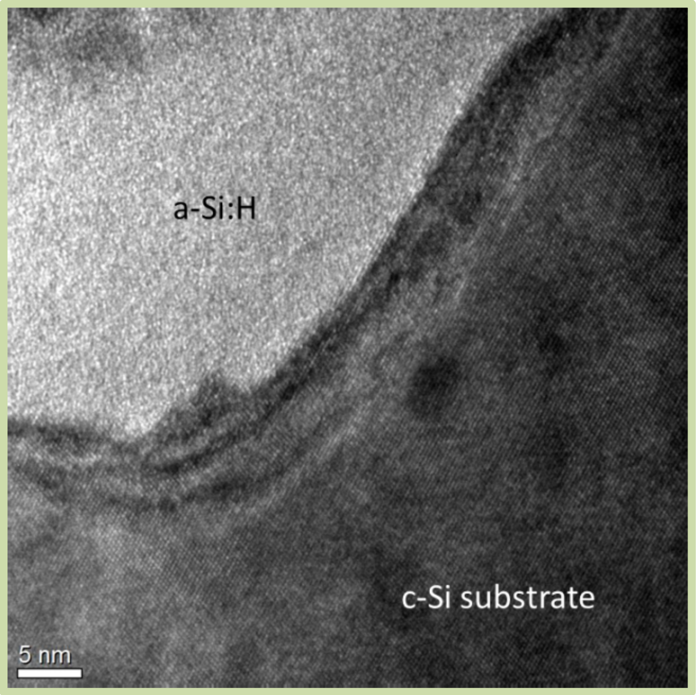

Figure 3-68 – HR-TEM image of the pyramid groove, showing an abrupt a-Si:H/c-Si interface despite the roughness observed.

The brightest area is the densest element, namely platinum. Then, the c-Si substrate is the second-densest material and a-Si:H is the less dense, thus the darkest.

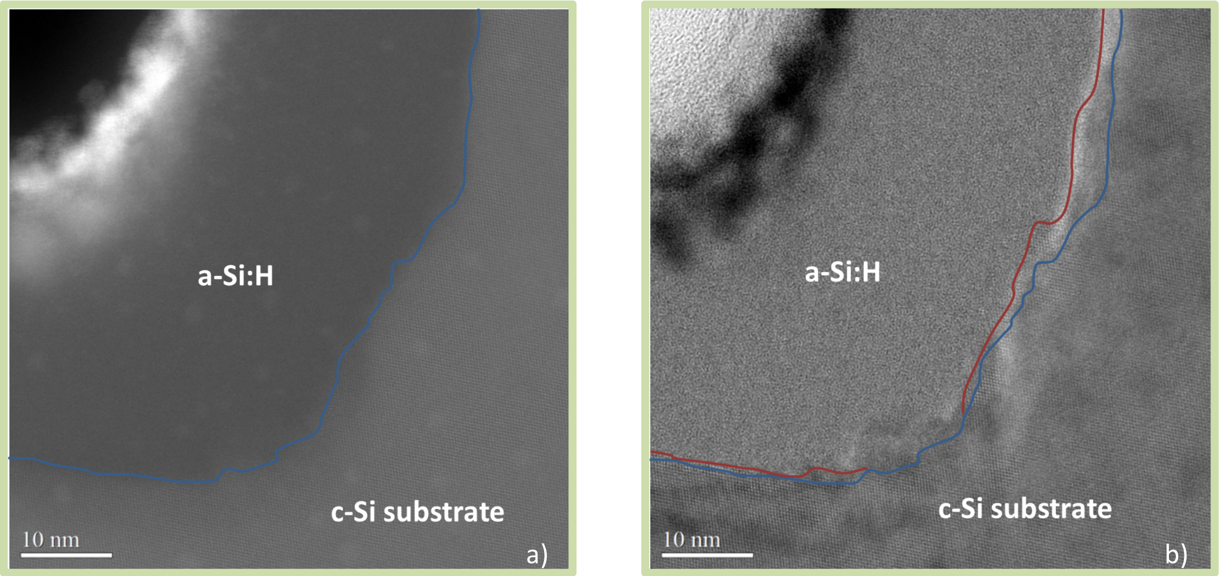

Figure 3-69 – STEM-HAADF (part a) and STEM-BF (part b) images of the pyramid groove.

Despite the fact that the contrast does not allow us to directly see the darker a-SiC:H thin layer on this image, the a-Si:H/c-Si interface can still be tracked (blue line). Figure 3-69b) shows a STEM image taken in the BF imaging mode of the electron microscope. Here, we can detect another limit of the a-Si:H/c-Si interface (red line). In fact, it follows the line that was defined in Figure 3-68 by HR-TEM quite well.

There are some crystalline planes that can be observed between the blue and red lines. Since a thin a-SiC:H layer was deposited prior to a-Si:H deposition on sample B, we know for a fact that these planes are not the result of epitaxial growth. They must therefore correspond to rough parts of the c-Si surface.

From the analyses conducted on sample B, where a thin a-SiC:H layer was deposited, we have a clearer vision of how rough the textured c-Si surface actually is, and how it impacts the interpretation of HR-TEM and STEM images. In particular we saw how abrupt the a-Si:H/c-Si is despite some crystalline planes that could be seen as though stemming from epitaxial growth, especially at the bottom of the valley grooves.

Density profiles

Just as in the case of the pyramid flank, density profiles were extracted from STEM-HAADF images of the valley groove. Figure 3-70 shows the density profile of sections 1a and 1b selected in the pyramid groove previously observed in Figure 3-69a). As can be seen, the transition from c-Si to a-Si:H at the interface is smooth and both slopes are comparable, despite the shape and contrast observed between each of the sections. It is also worth noting that the presence of carbon at the a-Si:H/c-Si clearly induces a slight drop in density at the interface throughout a 2-nm length, approximately. This is less clear in the case of section 1b but is confirmed on profiles extracted earlier from the flank analysis.

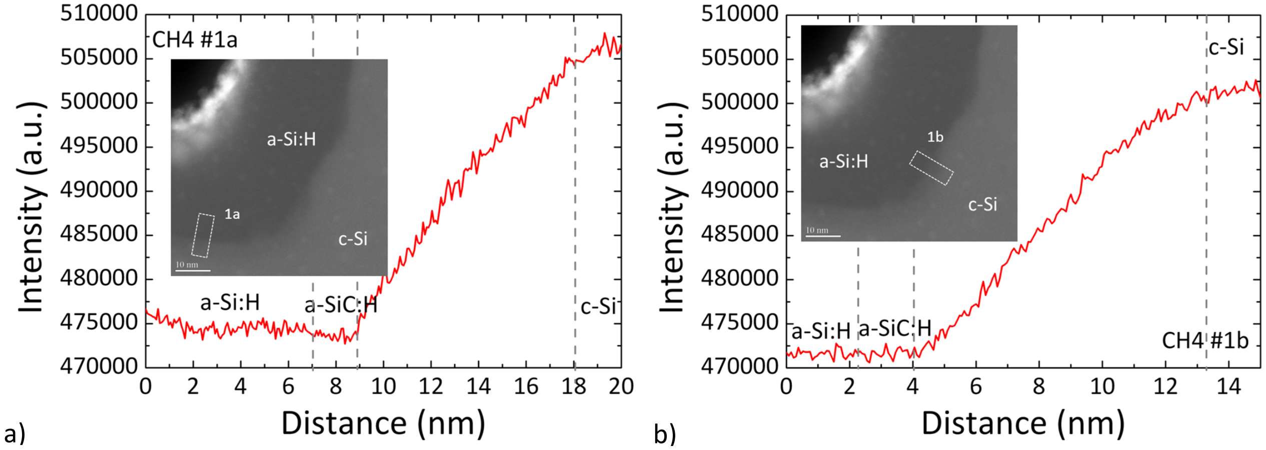

Figure 3-70 – Density profiles extracted from the STEM-HAADF image shown in Figure 3-69a). Two sections are analyzed: 2a (left) and 2b (right).

There is a clear difference in the profiles between the pyramid bottom and flank. Indeed, the evolution of the density was much steeper on the pyramid flank. This can be explained only by the difference in the roughness. Indeed, since we have carbon present at the interface and since there is no plateau detected on any of the profile density that were carried out on sample B, we are sure that no epitaxial growth is present. Thus, the difference detected between the pyramid groove and flank must come from the roughness. The steeper slope detected in the smoothest area, i.e., on the flank (Figure 3-64) confirms this hypothesis, since no apparent roughness is present. On the contrary, analyzing the valley bottom yields a less steep slope, showing that the contrast in density is less abrupt because of the roughness.

To conclude with sample B, HR-TEM analyses allowed us to locate a disruption at the a-Si:H/c-Si interface in various regions of the lamella. Hence, we were able to select sections on which to conduct STEM analyses. As a result, the abruptness of the a-Si:H/c-Si interface was evidenced in comparison with sample A. Moreover, density profiles allowed us to demonstrate that the density variation across it was smooth, as opposed to what could be seen on sample A. Finally, the presence of carbon could be detected after the density transition, thereby confirming the conclusions drawn from the analyses previously conducted on sample A which stated that a smooth transition was the signature of an abrupt interface. Contrariwise, the occurrence of a density plateau is the signature of epitaxial growth at the a-Si:H/c-Si interface.

Comparison with images taken at the a-Si:H/c-Si interface on a flat (111) wafer

In order to validate the results obtained on sample A and B, HR-TEM and STEM analyses were carried out at the a-Si:H/c-Si interface of a polished (111) wafer on which a 20 nm-thick a-Si:H layer was deposited. A smooth section was selected, as shown in Figure 3-71. As can be seen, the interface is perfectly abrupt, although some roughness is present. This roughness expands 2-3 monolayers maximum into the a-Si:H material.

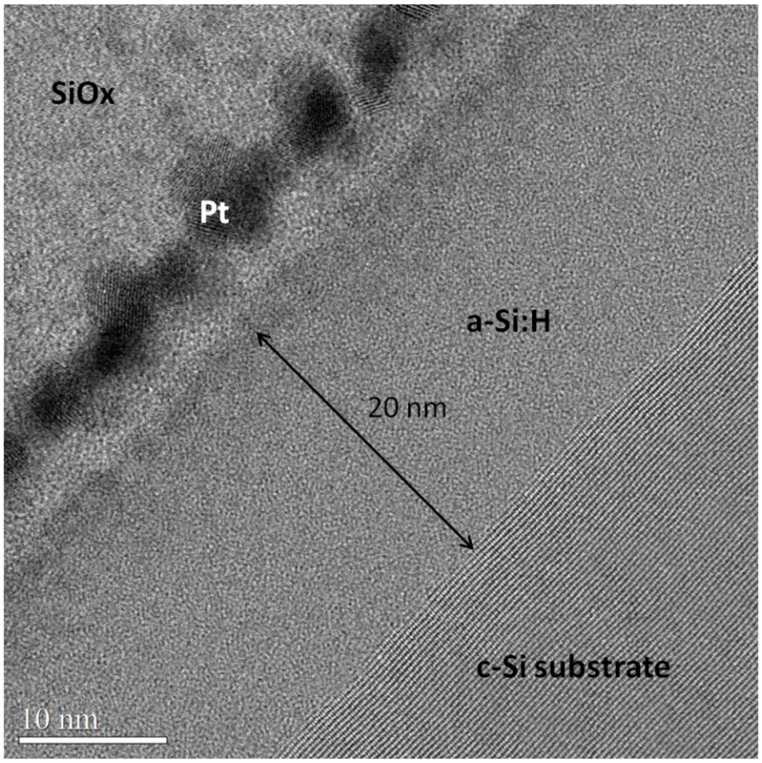

Figure 3-71 – STEM image of the a-Si:H/c-Si interface on a flat (111) c-Si wafer.

For comparison, HR-TEM and STEM images of a rough section of an a-Si:H/c-Si interface on a flat (111) substrate are shown in Figure 3-72. This time, the roughness expands up to 6 monolayers within the a-Si:H material. Of course, under our standard conditions, epitaxial growth is to be excluded on such substrates. Moreover, the high effective lifetime and the amorphous signal obtained upon analysis of this flat sample both testify for the abruptness of its a-Si:H/c-Si interface.

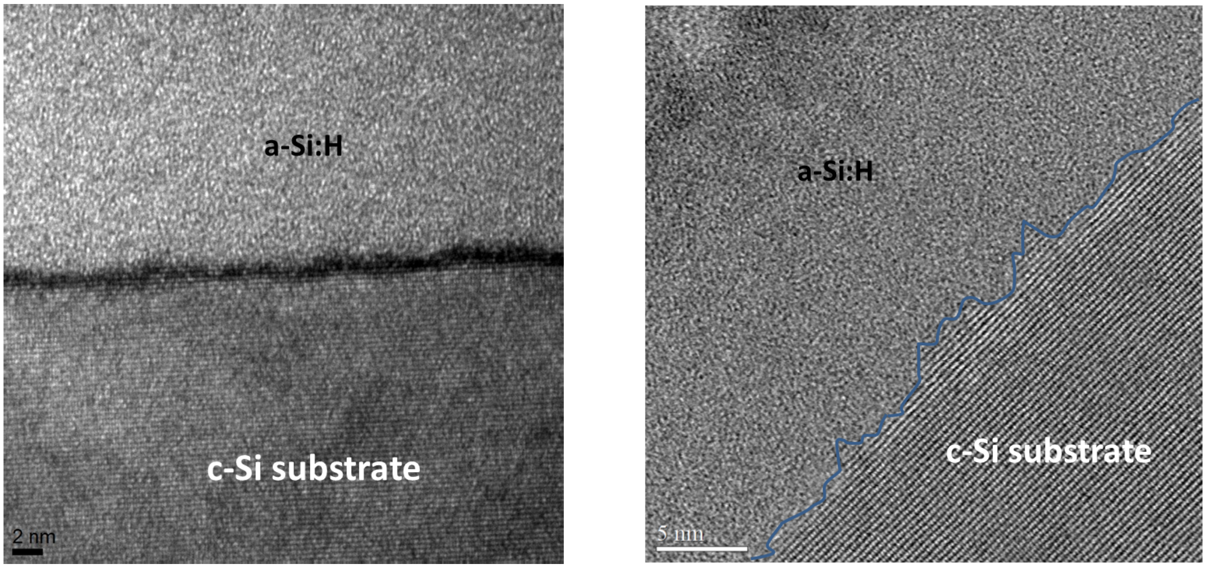

Figure 3-72 – HR-TEM and STEM images of a rough section of an a-Si:H/c-Si interface on a flat (111) c-Si wafer.

Therefore, by comparison we conclude that the roughness observed on the pyramid flanks of samples A and B is quite common at the junction between c-Si and a-Si:H, despite the several crystalline planes that protrude within the amorphous layer in some parts.

To conclude on these HR-TEM and STEM analyses, we studied two samples consisting of textured KIno wafers passivated with 28 nm of a-Si:H, one of which had a thin a-SiC:H layer at the a-Si:H/c-Si interface. By comparison with a flat (111) sample, it was possible to isolate the effect of roughness on the shape and abruptness of the interface. With and without a thin a-SiC:H layer, the interface appeared rough. In the case of sample B, a more abrupt transition could be observed, pointing at possible local epitaxial growth impediment. Density profiles carried out on STEM-HAADF images confirmed that crystalline planes with an intermediate density were grown on the pyramid flanks. In order to validate these results, further studies needed to be carried out since HR-TEM and STEM, even if very powerful, remain quite local experimental tools.

3.2.2.e Detection of epitaxial growth at the a-Si:H/c-Si interface of passivated textured c-Si wafers via annealing studies

The previous results showed that epitaxial growth could be suspected in some regions of the anisotropically textured c-Si wafer surface. However, HR-TEM and STEM analyses remain quite local. It has been reported that improvement of the intrinsic a-Si:H/c-Si interface upon annealing was highly dependent on its abruptness[217]. Indeed, annealing can be detrimental to the passivation quality if there is a low-hydrogen content at the interface. This is in fact the case of epi-c-Si layers, which contain about 30 to 100 times less hydrogen that a-Si:H[213]. Upon thermal annealing, hydrogen atoms are extracted at higher hydride states from the bulk but also from the interface. Fortunately, a-Si:H contains enough hydrogen to ensure re-passivation of these states. Given the difference in hydrogen content, it is probable that the epi-c-Si layer cannot fulfill the same role of being a hydrogen source. As a result, more dangling bonds are likely to emerge from such a post-deposition treatment. Therefore, the evolution of passivation upon thermal annealing could be a way of further confirming the presence of epi-c-Si at the a-Si:H/c-Si interface. For this purpose, symmetrically passivated i/i stacks were fabricated on both types of textured wafers: KIno and RTno. For each texturing recipe, a counterpart was fabricated with a thin a-SiC:H layer at the a-Si:H/c-Si interface. The four samples underwent 30-minute thermal annealing steps in a temperature-controlled oven, and in H_2/N_2 atmosphere at temperatures ranging from 180°C to 300°C, following which PCD measurements were taken to assess the changes in effective lifetime. While the ramp to reach the nominal temperature was quite steep, the decrease in temperature back to RT was conducted in a 30-minute period to avoid any quenching phenomenon from taking place, which could have left the a-Si:H bulk and the a-Si:H/c-Si interface more defective than in their as-deposited states. In Figure 3-73 and Figure 3-74 we report the evolution of the measured effective lifetime τ_{eff}, as normalized by the initial effective lifetime value τ_0 of the KIno and RTno samples, respectively.

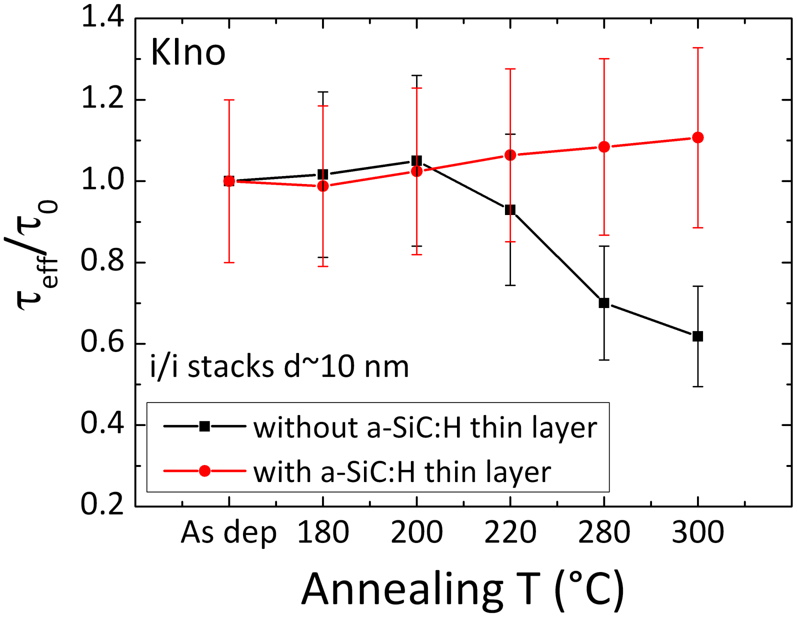

Figure 3-73 – Evolution of the effective lifetime of a “buffered” and “unbuffered” KIno wafer passivated with a 10-nm thick intrinsic a-Si:H layer.

As can be seen, annealing our KIno samples up to 200°C did not lead to any difference in the evolution of passivation. However, annealing beyond 200°C led to the degradation of the “unbuffered” KIno sample. Indeed, at 220°C, the evolutions of the a-SiC:H-buffered sample versus the a-SiC:H layer-free sample start to mark off. While the buffered-sample improves its initial lifetime slightly, the unbuffered sample drops to 90% of the initial value. Afterwards, the evolutions of the two samples are significantly diverging. Annealing at 280°C and 300°C induces a degradation that is quite severe for the unbuffered sample, i.e., down to 70 and 60% of the initial effective lifetime value. Meanwhile, the sample containing the thin a-SiC:H layer at the a-Si:H/c-Si interface keeps improving up to 1.1 time the initial lifetime value. This is quite surprising since these temperatures usually degrade passivation down to a very low effective lifetime value.

In the case of the two RTno samples, the trend is not so obvious. Indeed, up to 250°C, the two samples seem to evolve quite similarly, by degrading by 20% of the initial effective lifetime value. However, at higher temperatures, starting from 280°C, the two trends definitely start to mark off. While the buffered sample keeps a level of passivation corresponding to more than 60% of the initial effective lifetime value, the sample with no thin a-SiC:H buffer layer at the a-Si:H/c-Si interface degrades severely, until it reaches a little more than 40% of the initial value. While the experiment could be carried out for higher temperatures, it was decided that the trends were clear enough for both texturation recipes. Moreover, other effects such as hydrogen desorption could have started to blur these trends.

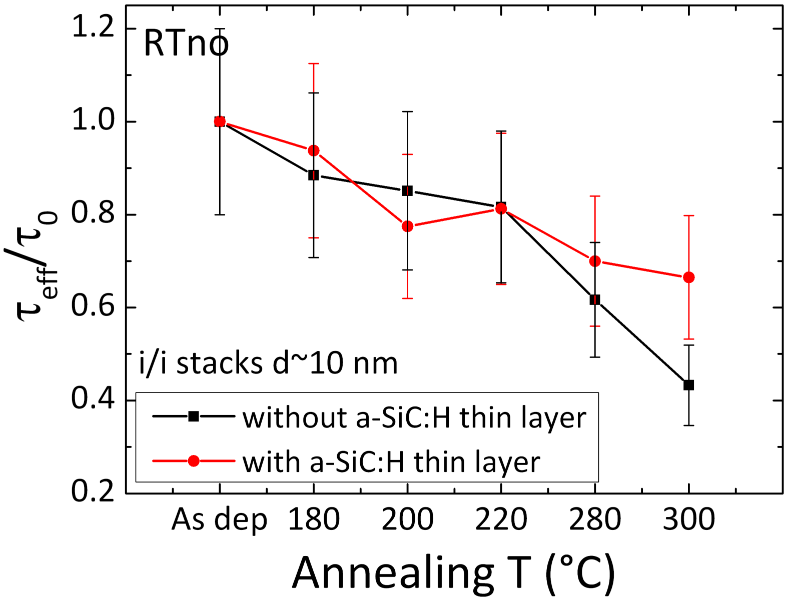

Figure 3-74 – Evolution of the effective lifetime of a “buffered” and “unbuffered” RTno wafers passivated with a 10-nm thick intrinsic a-Si:H layer.

To conclude on this experiment, it has been shown that it was clearly beneficial to have a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface when conducting thermal annealing on passivated textured (n)c-Si samples with a thin intrinsic a-Si:H layer.

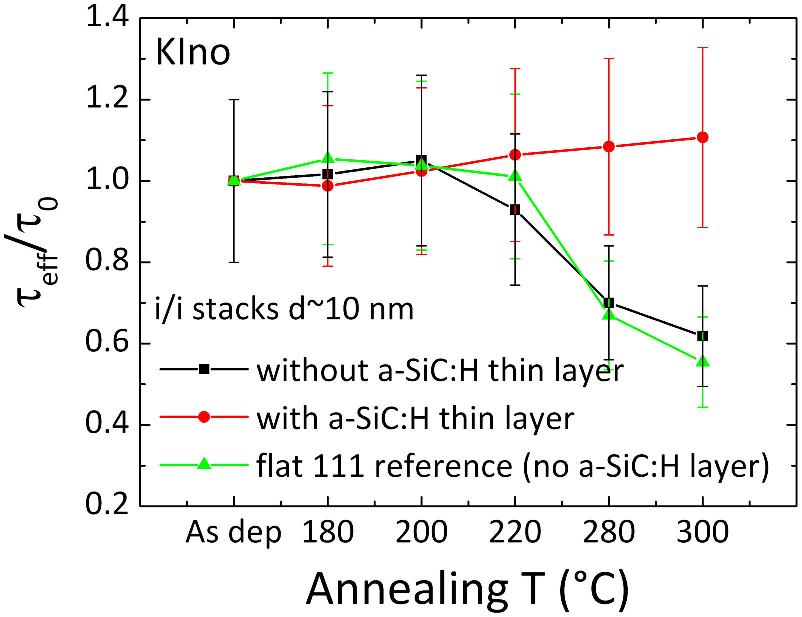

Figure 3-75 – Evolution of the effective lifetime of a “buffered” and “unbuffered” KIno wafers passivated with a 10-nm thick intrinsic a-Si:H layer.

This tends to confirm that unbuffered samples may contain epitaxial regions locally, which prevent the interface from being efficiently hydrogenated while raising the temperature. However, this cannot explain how all samples containing an a-SiC:H layer at the interface can keep a good level of passivation at temperatures higher than 220°C, i.e., already 20°C above the initial PECVD process temperature. Indeed, Figure 3-75 replicates the results of Figure 3-75 while comparing them with a flat (111) reference on which a 10-nm thick layer of a-Si:H has been deposited, without an a-SiC:H layer at the interface. It is striking to see that the latter-mentioned flat reference follows the exact same pattern as the unbuffered KIno wafer. This result clearly shows that apart from impeding local epitaxial growth, the presence of a thin a-SiC:H layer provides the passivated sample with an interface that can sustain very high temperatures. This is quite unusual for a-Si:H-passivated samples since this material is deposited at 200°C and hydrogen can start to desorb or at least move from the interface, leading to very poor effective lifetime values.

3.2.2.f Detection of epitaxial growth at the a-Si:H/c-Si interface of passivated textured c-Si wafers by spectroscopic ellipsometry

All results shown so far tend to demonstrate the presence of epitaxial growth on textured c-Si wafers, despite the global (111) orientation they exhibit. Since we had used spectroscopic ellipsometry to detect such undesirable growth on DSP wafers, we thought that the same could be done on textured substrates. As we were working on making such measurement possible at LPICM, we decided to carry-out some test-acquisition. By tilting the sample adequately, we were indeed able to detect a signal strong enough to measure the optical properties of a 28 nm-thick a-Si:H layer deposited on a KIno textured c-Si wafer. In Figure 3-76, the acquired imaginary part of the pseudo-dielectric function of a bare KIno wafer is shown in grey triangles.

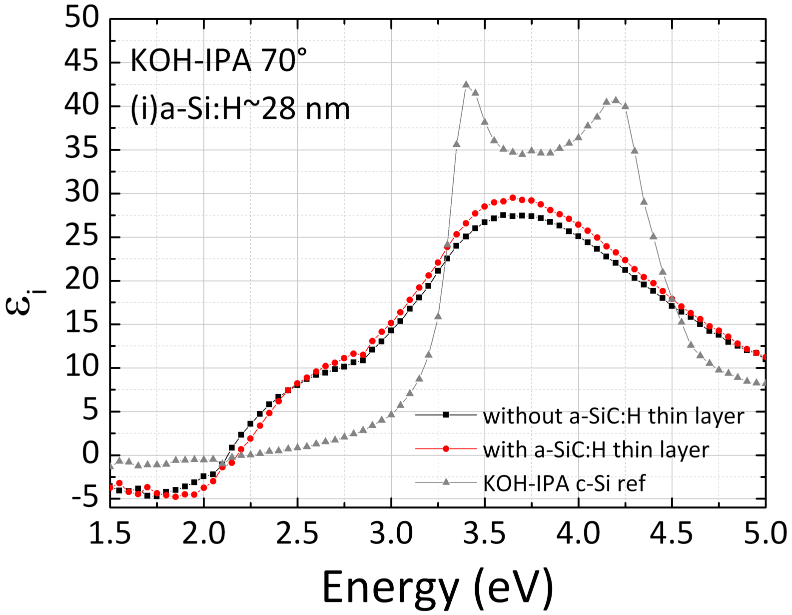

Figure 3-76 – Imaginary part of the pseudo-dieletric functions of films deposited on KIno susbtrates with (red dots) and without (black squares) a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface. A reference of a bare KIno wafer is shown in the background (grey triangles).

The collected signal is typical of crystalline silicon. On the other hand, the passivated samples exhibited a signal that is typical of amorphous silicon on a c-Si substrate. Moreover, there is no difference in the shape or intensity of the signal, whether there is a thin a-SiC:H layer at the a-Si:H/c-Si interface or not. Since the lifetimes of both samples were quite high (3.3 ms and 729 mV versus 1.9 ms and 716 mV) we did not expect to see any characteristic peak at 4.2 eV as in the case of the bare crystalline silicon reference. However, it is interesting to see how this interface quality is hard to detect optically, as opposed to what we experienced on flat (100) wafers (please refer to Figure 3-22). We suggest that this is due to the fact that epitaxial growth must occur in limited and specific regions and not in a homogeneous fashion over the whole wafer, as it is the case for flat (100)-oriented c-Si wafers. This explains why the lifetime obtained with a thin a-SiC:H layer at the a-Si:H/c-Si interface remains quite high.

To conclude on this experimental part, there is no significant difference in the optical characteristics between a buffered and an unbuffered i/i passivated textured wafer, despite the fact that all of our results point at the presence of local epitaxy. However, it does not mean that there is no epitaxial growth, given the previous passivation results combined with HR-TEM/STEM imaging and the annealing study. It simply means that if there is epitaxial growth, it is undetectable by spectroscopic ellipsometry, probably because it must be quite spread out and strongly localized, as opposed to what occurs on flat (100)-oriented c-Si wafers.

3.2.2.g Chemical smoothing

CP133 KIshort and KIlong

In an attempt to minimize the impact of surface imperfections on textured c-Si wafers, we turned to another solution. Indeed, it has been reported in the literature that an adequate chemical polishing of the random pyramids of a textured wafer could improve the a-Si:H/c-Si interface by decreasing the probability of experiencing local epitaxial growth[236]. The idea is to transform the sharp V-shaped surface morphology of the valley bottom into a smoother U-shaped valley. To do so, we chose to use a CP133 solution consisting of a mixture of HF (50% in H_2O DI), HNO_3 (65%) and CH_3COOH (100%) in 1:3:3 proportions (volume ratio). It actually is a HNA mixture used for isotropic etching of silicon, as described in 3.1.2.a. The chemical bath was cooled at temperatures ranging 14-22°C[32]. Etching times varied and two batches were selected for KIno substrates. A first batch called *KIshort* underwent 70 seconds of rounding (30 seconds only had a minor effect, hence an additional etching time of 40 seconds), inducing an etch depth of 2.5 µm and yielding the surface morphology shown in Figure 3-77b) and Figure 3-77b'). A second batch called *KIlong* was prepared with a 180-second chemical treatment, inducing an etch depth of 7 µm and yielding the surface morphology shown in Figure 3-77c) and Figure 3-77c'). The CP133 attack can be seen in the valley grooves essentially, which change from sharply V-shaped to rounded smooth U-shaped grooves. One can also see its impact on the pyramid edges, which turn much smoother than after KOH/IPA texturing. However, the reflectivity increased accordingly due to the highly reflective, almost flat parts in the U-shaped valleys.

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[32] Strong exothermic reaction, hence the temperature rise during the etching.

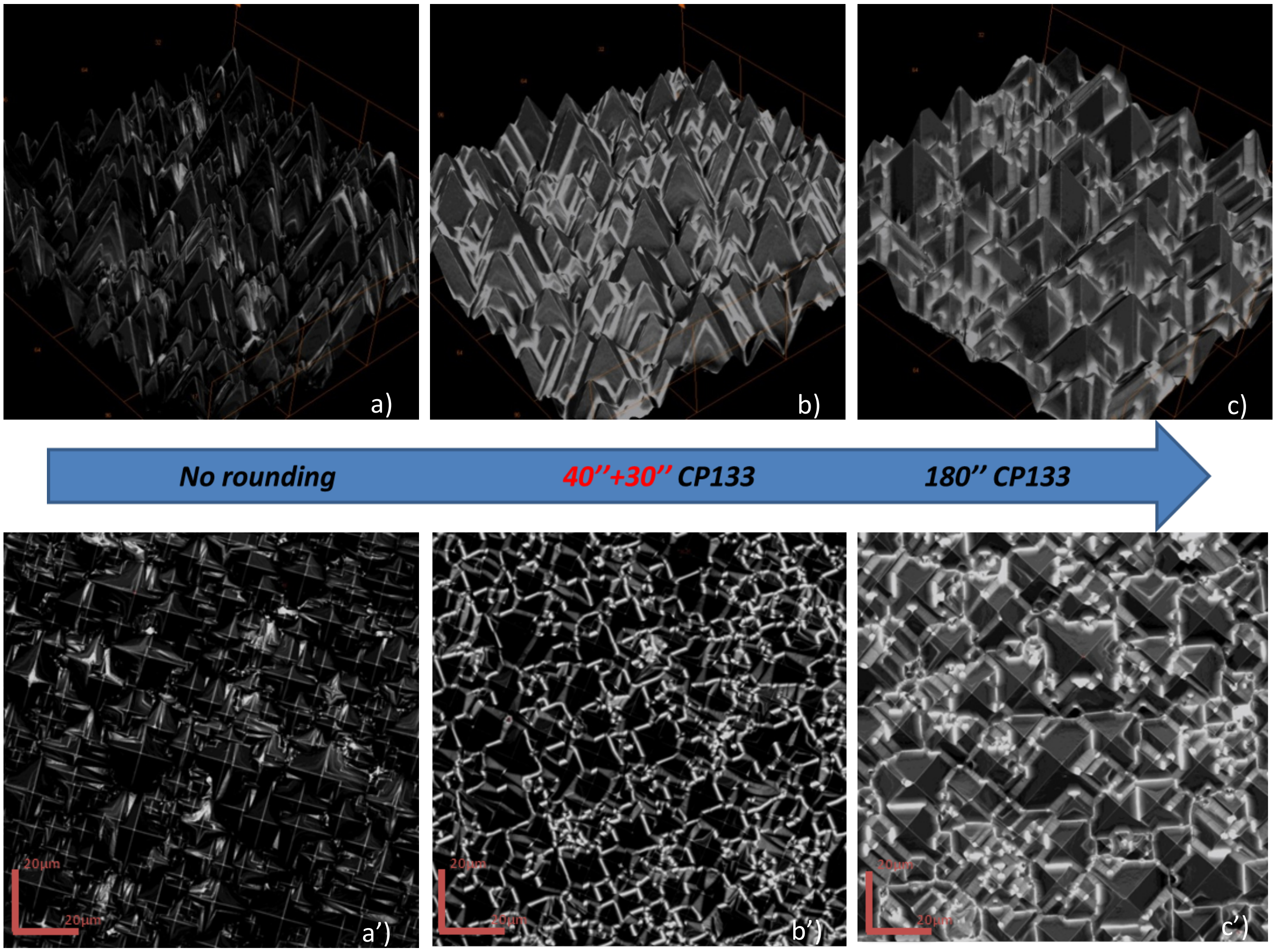

Figure 3-77 – LSM(upper part) and SEM(lower part) images of KOH-IPA before and after chemical polishing in CP133.

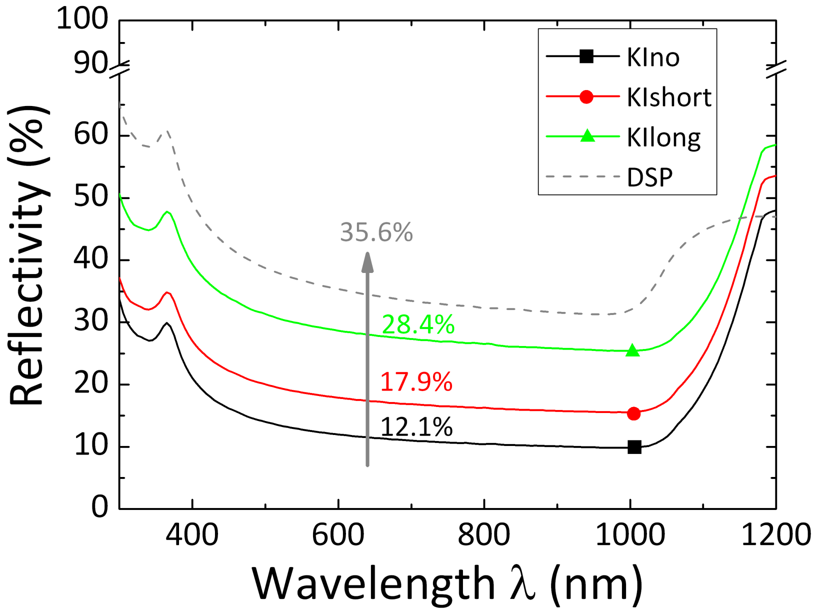

Figure 3-78 – Reflectivity as a function of the light wavelength for a KIno wafer, before and after chemical polishing in a CP133 chemical bath.

As can be seen in Figure 3-78, the KIshort sample keeps a relatively low reflectivity, around 17%. If this type of rounding could allow us to gain a few mV in V_{OC}, the higher reflectivity could still be interesting for a solar cell. Contrariwise, the KIlong sample exhibits a mean reflectivity very close to its flat counterpart, so that part of the gain in V_{OC} should be lost in J_{SC}.

CP133 RTshort and RTlong

The same experiment was conducted on RTno wafers. In this particular case, the CP133 etching was more efficient. A first batch called *RTshort* underwent a 40-second rounding process, inducing an etch depth of 1.4 µm and yielding the surface morphology shown in Figure 3-79b) and Figure 3-79b').

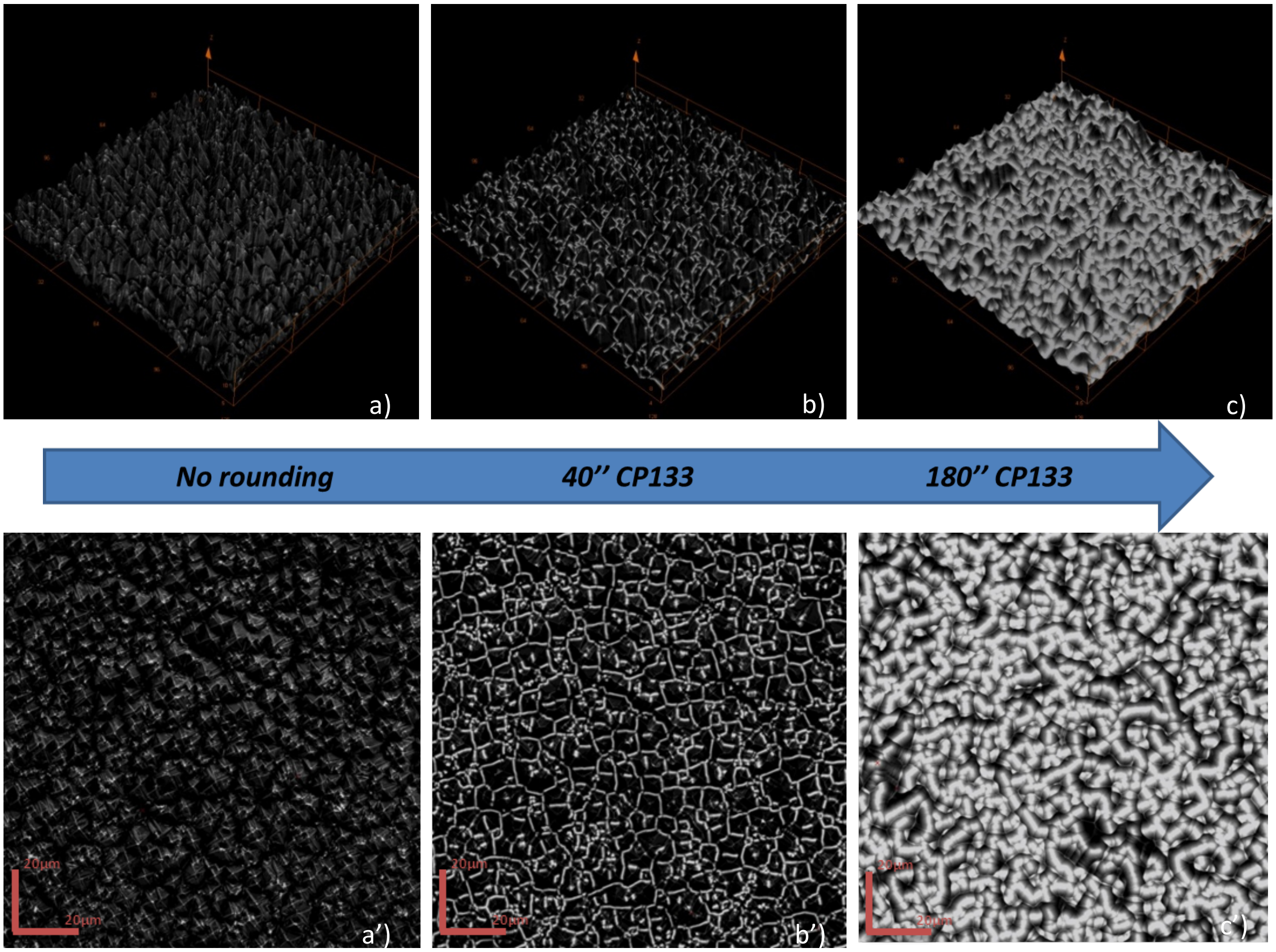

Figure 3-79 –LSM(upper part) and SEM(lower part) images of KOH/RenaTex textured wafers, before and after chemical polishing in CP133.

A second batch called *RTlong* was prepared with a 180-sec chemical treatment, inducing and etch depth of 6 µm and yielding the surface morphology shown in Figure 3-79c) and Figure 3-79c'). As in the case of KIno wafers, the sharp V-shaped valleys turned into U-shaped grooves. The 180-second treatment is the most striking. Indeed, in Figure 3-79c) we hardly recognize the initial landscape made of randomly distributed pyramids. Again here, the reflectivity increased accordingly, due to the highly reflective – almost flat– parts in the U-shaped valleys. As can be seen in Figure 3-80, the RTshort sample keeps a relatively low reflectivity, around 17%.

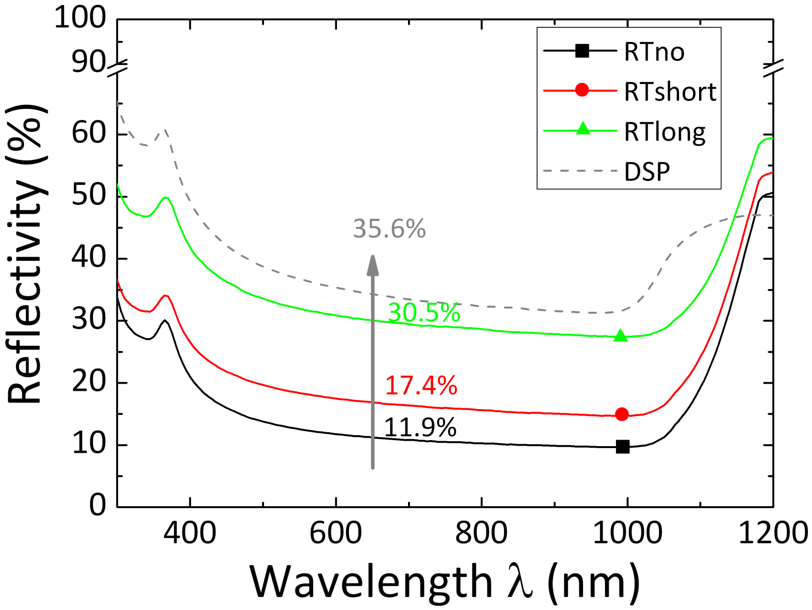

Figure 3-80 – Reflectivity as a function of the light wavelength for an RTno wafer, before and after chemical polishing in CP133.

Again, this type of rounding could allow us to gain a few mV in V_{OC}, without losing too much in J_{SC}. Similarly to KIlong, the RTlong sample exhibits a mean reflectivity almost identical to its flat counterpart between 400 and 1100 nm. Therefore, part of the gain in V_{OC} should be lost in J_{SC}.

Passivation tests

Passivation tests were carried out to assess the gains in V_{OC}, which were made possible by chemical smoothing. These tests were made under our standard a-Si:H deposition conditions, i.e., 50 sccm, 50 mTorr at 200°C substrate temperature. The resulting effective lifetimes and iV_{OC} are shown in Table 3-12. As can be seen, using our standard (i)a-Si:H layer, it was impossible to reach effective lifetimes comparable to those obtained on KIno and RTno wafers. For a 254”(30”)[33] deposition time on an RTno wafer, we would usually get a value above 3 ms for an iV_{OC} of 720 mV. Even without a thin a-SiC:H buffer layer at the interface, we could reach lifetimes as high as 2.3 ms with an iV_{OC} of 711 mV. In this case, we do not go beyond 185 µs with a layer twice as thick (sample 140317-4). Increasing the a-SiC:H deposition time (in case the flat parts from the U-shaped valleys required so) (sample 140324-2) or the RF power did not help us reach any higher lifetime values. Oddly enough, using an HF/Piranha/HF routine instead of just a 2nd HF dip seemed to improve the passivation level notably (sample 140321-8). Indeed, for the same deposition time, i.e., 254”(30”), the effective lifetime markedly exceeds that of sample 140317-4, which has a much thicker layer. The same phenomenon was observed on KIlong wafers, where a 254”(30’) a-Si:H deposition time led to a much higher lifetime after a complete HF/Piranah/HF routine. This made us question the CP133 process in terms of contaminants. Since the lifetimes are higher after a complete HF/Piranha/HF cleaning, this means that organic contaminants must have been present at the c-Si surface. This does not however explain why lifetimes are not comparable to those obtained on RTno

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[33] The time in parentheses indicates the deposition time of the thin a-SiC :H layer at the a-Si:H/c-Si interface over the overall (i)a-Si:H deposition time.

and KIno wafers. Indeed, there is no real source of contaminants in such a mixture, apart from carbon that must have been removed in the Piranha bath. A more plausible option would have been that CP133 being an isotropic etchant, the c-Si surface became rough during the chemical rounding up to a point where porosity may have been produced. This would explain the poor passivation obtained on all the rounded wafers. A solution would consist in carrying out another texturing routine in our KOH/IPA and KOH/RenaTex baths. However, since we had managed to achieve device-grade lifetimes and iV_{OC}s on KIno and RTno wafers – using the thin a-SiC:H buffer layer at the a-Si:H/c-Si interface – and because of the much higher reflectivity of the rounded samples, we decided to focus on further developments of the textured substrates with no chemical rounding.

Cleaning	Sample#	Substrate	Deposition time	τ_{eff} [µs]	iV_{OC} [mV]
HF DCSO	140317-4	RTshort	i=510"(30")	185	630
HF-P-HF ARCAM	140321-8	RTshort	i=254"(30")	488	667
HF ARCAM	140324-2	RTshort	i=254"(60")	172	631
HF ARCAM	140324-5	RTshort	i=127"(30")@2W	51	579
HF ARCAM	140324-9	RTshort	i=51"(15")@5W	31	545
HF-P-HF ARCAM	140321-5	RTlong	i=254"(30")@1W	202	631
HF DCSO	140319-4	KIshort	i=254"(30")	81	597
HF-P-HF ARCAM	140321-7	KIshort	i=254"(30")	253	641
HF-P-HF ARCAM	140321-13	KIlong	i=254"(30")	480	666

Table 3-12 – Effective lifetimes and iV_{OC} of RTshort, RTlong, KIshort and KIlong samples passivated with a thin (i)a-Si:H layer. HF DCSO refers to a classical HF dip carried out in a laboratory nearby. HF ARCAM refers to a classical HF dip in the reactor room. HF-P-HF refers to a HF-Piranha-HF routine. (t'') refers to the (i)a-SiC:H deposition time over the overall (i)a-Si:H deposition time.

Chapter Key Results

To conclude this chapter, we have reviewed how texturation of c-Si can be carried out. In particular, wet-texturing recipes were studied with a focus on KOH-based texturing of as-cut (100)-oriented 280 µm-thick c-Si wafers. This allowed us to define two texturing recipes. Both included a preliminary 3 min NaOH etching step in a highly concentrated bath to remove the saw-induced damages. The solution had a wt.22% concentration and was kept at 80°C. Subsequently, based on reflectivity measurements and on passivation tests, two texturing recipes were selected: a KOH-IPA recipe which gave us large pyramids (12-15 µm high) and an IPA-free recipe, which yielded much smaller pyramids (6-8 µm). Both types of pyramids were cleaned right after etching in several chemical baths (DI water rinsing, HCl, HF and Piranha). Upon the final part of this cleaning, a thin SiO_2 layer was grown in the Piranha bath. This allowed us to protect the c-Si surface until the use of the wafer for passivation tests. Based on PCD measurements after a 2nd HF dip, a 45-sec HF dip was selected to remove the protective SiO_2 layer prior a-Si:H deposition in the reactor.

Our first passivation tests showed how much textured c-Si differs from its flat counterpart:

- the effective lifetimes and implied open-circuit voltages of passivated textured c-Si wafers were much lower than in the case of flat wafers. Several explanations were suggested, such as the surface increase that occurs upon texturing, for example,
- by studying the a-Si:H growth on (100) and (111) c-Si wafer, we explored the possibility of local epitaxial growth on textured c-Si wafers,
- adding CH_4 during the first seconds of the a-Si:H layer deposition improved the effective lifetimes and iV_{OC}s of passivated textured c-Si wafers noticeably, just as in the case of (100) wafers. This could not be explained by a passivation enhancement mechanism due to the presence of carbon in the a-Si:H bulk since we demonstrated that this material had poor passivating properties *per se* and that flat (111) wafers were not sensitive to this additive. Therefore, we suspected epitaxial growth on textured c-Si surfaces despite its theoretical pure (111) orientation. In consequence,
- HR-TEM and STEM analyses were carried out on two samples: one with a standard (i)a-Si:H passivating layer and the other one with an (i)a-SiC:H/(i)a-Si:H passivating stack. Results showed that:
    - i) the c-Si textured surface is rough and contains many imperfections on the flanks as well as in the pyramid grooves,
    - ii) on imperfections found on the flanks, crystalline planes are more likely to develop than on neat parts of the surface and STEM-HAADF images confirmed their epitaxial nature on some parts of the flanks,
    - iii) in pyramid grooves where epitaxial growth was thought to be fostered, the a-Si:H/c-Si interface was found to be abrupt and density profiles carried out on STEM-HAADF images confirmed this abruptness,
    - iv) with the use of a thin a-SiC:H layer, the a-Si:H/c-Si interface looks more abrupt and no crystalline planes can be found beyond the interface, even on c-Si imperfections.

Moreover, annealing studies were performed:

- a thin a-SiC:H buffer layer is beneficial to keep a high level of passivation for annealing temperatures up to 300°C while samples with no a-SiC:H buffer layer degraded if $T_{ann.}>220°C$. This not only tends to confirm the presence of epi-c-Si at the a-Si:H/c-Si interface as suggested by PCD measurements and HR-TEM/STEM analyses, but also shows that the presence of carbon allows for the interface to sustain temperatures that are usually highly detrimental for the passivation of c-Si by a-Si:H,
- in an attempt to detect these epitaxial regions, spectroscopic ellipsometry measurements were conducted on passivated textured substrates with and without a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface. They showed that no difference could be detected optically and that the deposited layers were perfectly amorphous in both cases.

As a result, we concluded that, indeed, local epitaxial growth occurs whilst being undetectable by HR-TEM/STEM analyses (local) or by spectroscopic ellipsometry (too averaged). This opens doors to the use of thin a-SiC:H layers not only to improve the passivation of textured c-Si wafers by a-Si:H, but also to assess the quality of a texturing recipe. Indeed, if we consider the drop in passivation $\Delta\tau_{eff}$ experienced when going from a flat (111) to a textured wafer, it could theoretically be expressed as the sum of a contribution induced by the increased surface plus a contribution coming from (100)-oriented imperfections, thus generating epitaxial growth locally. In other words, $\Delta\tau_{eff}$ could be expressed as:

$$\boxed{\frac{1}{\Delta\tau_{eff}}=\frac{1}{\Delta\tau_{text}}+\frac{1}{\Delta\tau_{epi}}} \tag{84}$$

Therefore, introducing an adequate a-SiC:H layer would virtually reduce to zero the second contribution, leading to the following expression for $\Delta\tau_{eff}$:

$$\boxed{\Delta\tau_{eff}=\Delta\tau_{text}} \tag{85}$$

Optimizing a texturing recipe would no longer mean lowering the c-Si wafer reflectivity solely, but also lowering the remaining $\Delta\tau_{text}$ contribution to the overall drop in effective lifetime, when transferring from flat to textured c-Si substrates. This could be done by optimizing the size distribution, the size homogeneity, the pyramid edge sharpness, the shape of the valley grooves, etc. and, above all, the density of (100)-oriented imperfections. This could help improving texturing recipes to meet the results obtained on their flat (111) counterparts.

In an attempt to lower the impact of the c-Si surface imperfections, a chemical rounding mixture was used:

- as a result, the V-shaped valleys were rounded into U-shaped grooves, thereby increasing the reflectivity. However, the shortest rounding time yielded quite acceptable reflectivities (~17%),
- passivation tests carried out afterwards led to very poor effective lifetimes, ranging 80-500 µs. This is thought to be due to the roughness and porosity induced by the isotropic HNA etchant. This could be corrected by using again a texturing recipe like KOH to eliminate the porous sections.

Nonetheless, we preferred to continue with our KIno and RTno c-Si wafers since device-grade lifetimes and iV_{OC}s could be obtained, while passivating these with intrinsic a-Si:H. Naturally, we felt ready to try incorporating doped layers to the structure and move towards the fabrication of textured (n)c-Si heterojunction solar cells. Namely, it would be interesting to try implementing a thin a-SiC:H buffer layer in a cell structure to see if this leads to a combined increase in the passivation level and conversion efficiency.

4 Optimization of a-Si:H/c-Si SHJ solar cells on n-type textured wafers

4.1 A-SiC:H thin buffer layer at the a-Si:H/c-Si interface to enhance the conversion efficiency of textured SHJ solar cells

4.1.1 SHJ solar cell fabrication chain at LPICM

Throughout this thesis, the fabrication of SHJ solar cells involved the deposition of intrinsic and doped a-Si:H by low-temperature PECVD, the deposition of ITO by PVD at 180°C and the evaporation of silver for metal contacts. PECVD deposition included:

- a standard intrinsic amorphous silicon layer,
- a standard n-type amorphous silicon layer deposited at 200°C. Its conductivity reaches $2\cdot10^{-2}\ \Omega^{-1}\cdot cm^{-1}$, which is optimal considering the negative impact of dopant incorporation beyond the $10^{-2}\ \Omega^{-1}\cdot cm^{-1}$ threshold value found by *Spear and LeComber* for n-doped a-Si:H (see Figure 4-1)[35].

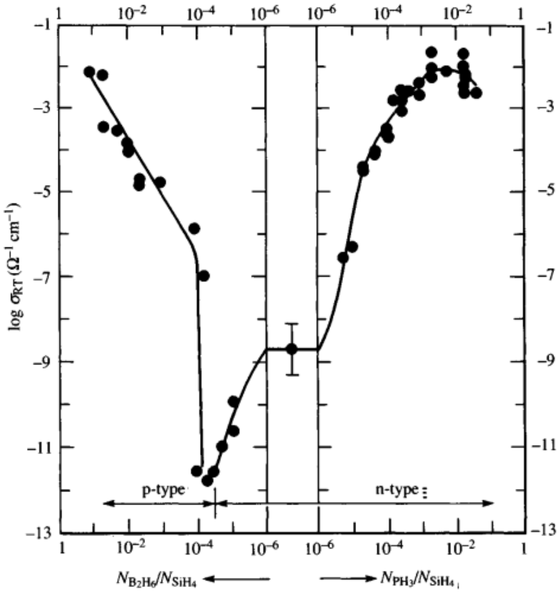

Figure 4-1 – DC conductivity of phosphorus- and boron-doped a-Si:H as a function of the gas dopant concentration at RT. Taken from [35].

Moreover, one should also consider that at high dopant concentrations, the energy bandgap starts to decrease due to an increased absorption effect. This is obviously something we want to avoid. This layer has an optical energy bandgap of 1.65 eV and a deposition rate close to that of intrinsic a-Si:H, i.e., 0.7 Å/s. The deposition conditions are shown in the table below.

SiH_4 [sccm]	PH_3 (1% in H_2) [sccm]	Time [s]	Pressure [mTorr]	Power [W]	Thickness [nm]
50	1	360	60	1	25

- a standard p-type amorphous silicon layer with $1\cdot10^{-4}\ \Omega^{-1}\cdot cm^{-1}$ conductivity. Again, as can be seen in Figure 4-1 on the left-hand side, $10^{-4}\ \Omega^{-1}\cdot cm^{-1}$ was considered optimal to fabricate SHJ solar cells with our reactor[237]. Indeed, despite the higher achievable values for p-type a-Si:H, the impact of boron-capping layers on the intrinsic layer underneath needed to be taken into account. This aspect will be discussed more thoroughly in section 4.2. This layer was developed using 1% TMB in H_2, thus allowing for a higher deposition temperature (200°C) and a wider optical energy bandgap, close to 1.8 eV (owing to the presence of carbon) than in the case of B_2H_6. The deposition conditions are shown in the table below.

SiH_4 [sccm]	TMB (1% in H_2) [sccm]	Ar	Time [s]	Pressure [mTorr]	Power [W]	Thickness [nm]
50	20	yes	200	110	2	16

Three plasma chambers with an interelectrode distance of 28 mm were used to isolate the different types of doping and avoid cross-contamination. The n-side was first deposited in order to prevent the p-layer from spending a double pumping cycle at 200°C for the second-side deposition, since there was no load-lock system in our reactor. No second HF dip was performed when flipping the wafer after the n-layer deposition. Indeed, our experimental results showed that the silicon surface was still H-terminated after depositing on the first side and that a second HF dip actually decreased the passivation level. This is most probably due to a detrimental re-exposure of the surface to HF, thus inducing an increase in the silicon surface atomic roughness.

For the p-side, the intrinsic layer was deposited in a separate plasma chamber, since we observed a stronger impact of the presence of remaining boron despite preliminary precoatings using intrinsic conditions. The gas mix also contained argon to increase the plasma density, thus resulting in a reduction of the growth rate to approximately 0.8 Å/s, and to increase the layer density and boron incorporation. Indeed, dopants (especially boron) are known for their catalytic impact on a-Si:H growth (*Street* p. 140-141 [36]). This can either be due to an increase in silicon radical formation in the gas phase or to a higher sticking coefficient of such radicals on the silicon surface. Another explanation could be that the higher diffusion rate of hydrogen in boron-doped a-Si:H induces a much higher hydrogen atom release rate from the silicon surface, thus allowing for a more efficient silicon radical adsorption. This would indeed, naturally foster the a-Si:H growth. In any case, argon, being present within the gas mix and promoting bombarding action, helped us decrease the (p) a-Si:H growth rate. The argon flow rate was chosen so that its partial pressure would equal that of SiH_4 during the deposition, i.e., 50 mTorr. The changes in density could be directly measured by monitoring the evolution of the A parameter deduced from ellipsometry fits. Under our argon-free standard conditions, A would reach values around 180, whereas under the process conditions described above, A is found to be close to 220. This directly relates to the lower growth rate and subsequent lower hydrogen incorporation. Likewise, the optical energy bandgap of the p-amorphous layer was also found to be lower, closer to 1.7 eV, confirming this trend.

Finally, for all SHJ solar cells fabricated during this Ph.D. thesis, an ITO layer of approximately 82 nm was deposited on both sides of our solar cell precursors. The n-side was fully covered by the TCO, whereas for the p-side the wafer was cleaved to obtain a quarter of wafer, and a 2x2 cm² mask was used to avoid any measurement inaccuracy possibly due to lateral transport beyond the cell limits. To finalize the SHJ solar cells, silver was evaporated on both side of the solar cell precursor, on top of the ITO. On the n-side again, a deposition was made on the whole ITO surface, whereas on the p-side a grid was used such as to fit the 2x2 cm² ITO cell limits. Various 2x2 cm² silver grid patterns were tested during this Ph.D. thesis. However, a grid containing a tapered busbar as shown in Figure 4-2a) was used for most of our samples, since it yielded slightly higher currents due to the reduced cell surface shading while inducing an acceptable increase of series resistance during our IV measurements. Indeed, EL measurements were performed on cells with straight and tapered busbars. A Si CCD camera was used to detect the emitted signal. Because of this, the exposure time was set to 0.25 s. The bias was set at a value such that the current flowing through the SHJ solar cells corresponded approximately to a typical J_{SC} value found on our textured cells, i.e., close to 35-37 mA/cm². Examples of measurements are shown in Figure 4-2b) and c). As can be seen in Figure 4-2b), our reference sample with a straight busbar (Figure 4-2b) leads to a quite homogeneous collection on the whole cell surface. Contrariwise, the collection is made heterogeneous when using a tapered busbar since the brightest area remains close to the thicker part of it, while darker areas can be seen away from this point. Despite this clear detrimental effect, we will see later that the reduction of shading allowed for a higher J_{SC}.

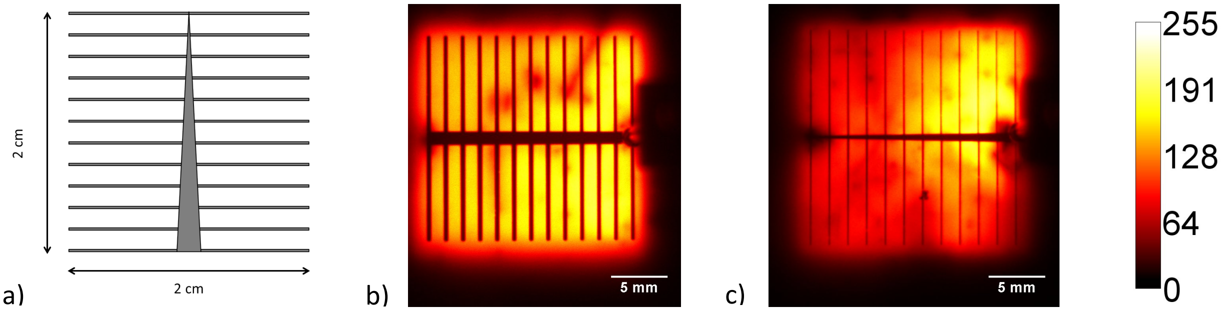

Figure 4-2 – a) Front grid pattern exhibiting a tapered central busbar, b) the homogeneous collection induced by a straight central busbar and c) the heterogeneous collection that can be found when tapering the central busbar (measured by EL).

To sum-up, the SHJ solar cell fabrication chain at LPICM is described in Figure 4-3. These steps were kept as constant as possible in terms of cleanliness and time in order to keep the variables dependent on the deposition conditions only. The cleaning, the PECVD, PVD and Ag deposition times varied depending on the type of substrate used (flat or textured). Using conditions and thicknesses close to these, a record efficiency of 17.2 % was reported by the LPICM in 2011 (*M. Labrune*'s thesis p.120 [12]) on a flat (100) 2.6 Ω·cm n-type c-Si wafer (2x2 cm² cell surface). Based on this result and by making a few upgrades, all of our SHJ solar cells were fabricated following this process chain. Each upgrade will be mentioned when implemented.

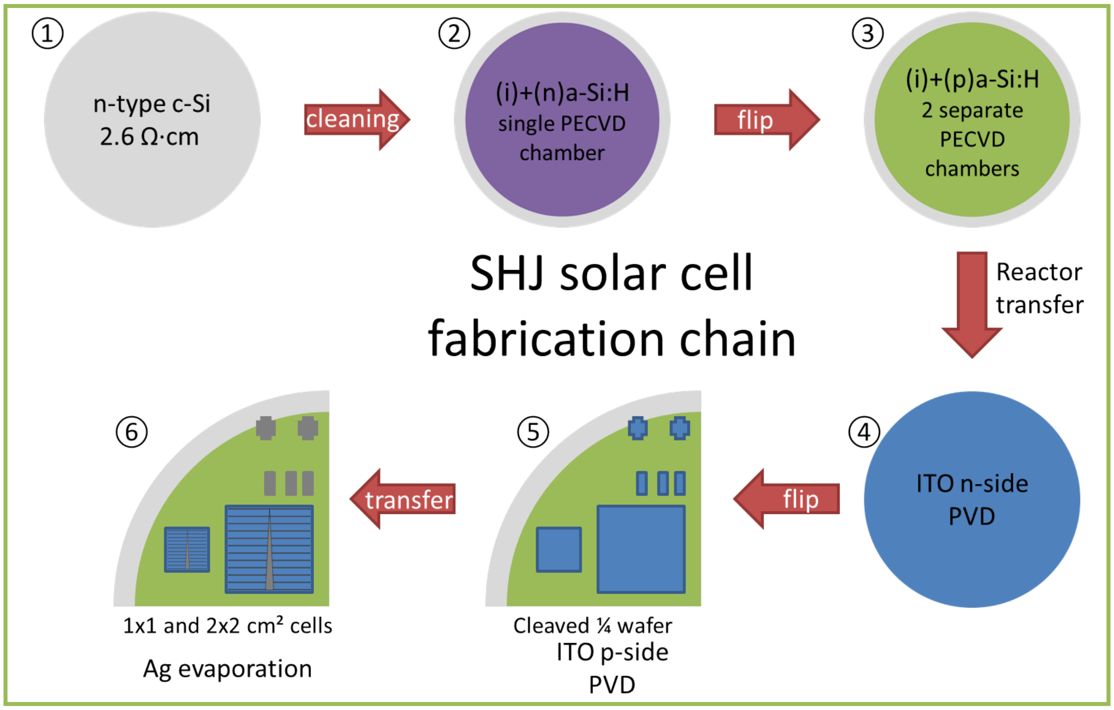

Figure 4-3 – SHJ solar cell fabrication chain at LPICM. The samples are not drawn to scale.

4.1.2 SHJ solar cell performance under our standard conditions

4.1.2.a Flat SHJ solar cells fabricated on DSP (111)-oriented c-Si wafers

Prior to the thin a-SiC:H layer implementation at the a-Si:H/c-Si interface of our textured SHJ solar cells, we carried out some experiments with our standard intrinsic amorphous silicon layer on flat substrates. In this way, reference samples would be available for comparison purposes. Flat DSP (111) c-Si wafers were first used with our standard recipes described previously. The resulting structure of an n-type SHJ solar cell fabricated according to Figure 4-3 on a flat substrate is shown in Figure 4-4. It contains a 5 nm-thick intrinsic layer on both sides, a 25 nm-thick (n+)a-Si:H layer for the BSF and a 16 nm-thick (p++)a-Si:H layer for the emitter.

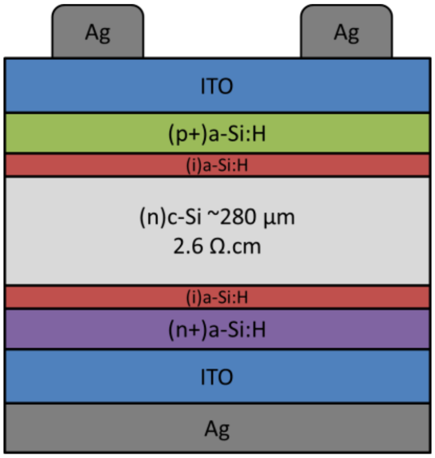

Figure 4-4 – Sketch of an n-type SHJ solar cell fabricated on a flat 2.6 Ω·cm c-Si wafer. The structure is not drawn to scale.

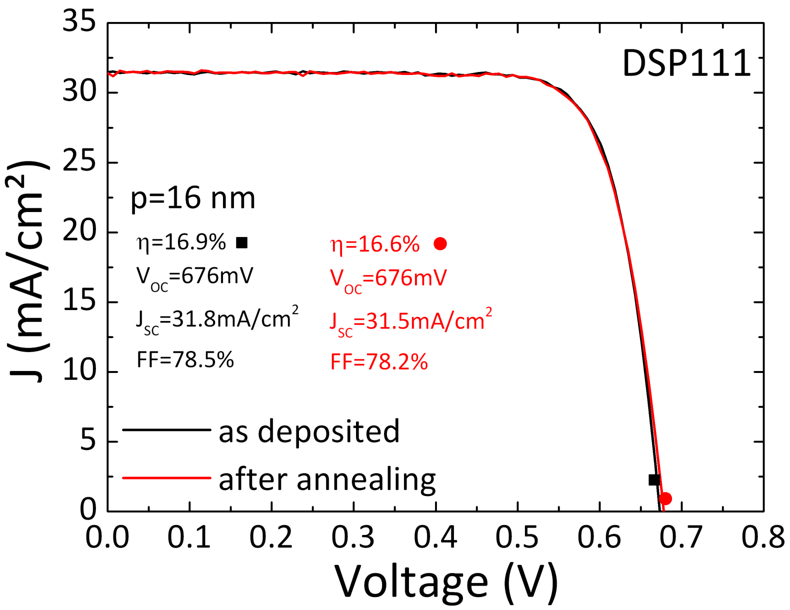

Figure 4-5 – JV characteristics of a SHJ solar cell fabricated with a flat (111) wafer before and after annealing.

The JV characteristics of the cell are shown in Figure 4-5. As can be seen, by using this recipe, a conversion efficiency of 16.9% is achieved. Despite a lower-than-expected V_{OC} the collection stays good with a J_{SC} quite high for a flat c-Si substrate. As can be seen, annealing this cell structure does not lead to any significant improvement, neither in terms of V_{OC} nor in FF. Contrariwise, we witness a slight degradation of the conversion efficiency. Usually, upon annealing, the a-Si:H/c-Si improves in quality leading to a lower recombination velocity, and this was demonstrated using the same annealing conditions with symmetrical i/i stacks. Moreover, the Ag/ITO contact should also improve and provide an enhanced carrier collection reflected by a higher FF. This was not the case here since we experienced a slight FF decrease. This should not be related to a worse Ag/ITO contact but rather to a more significant recombination mechanism within the (p)a-Si:H layer. To confirm this trend, JV measurements were performed in the dark before and after annealing. From these curves shown in Figure 4-6, the diode ideality factors n and the dark saturation currents J_0 were extracted using a linear fit in the 0.4<V<0.6 bias region. As a result, the n factor was found to be approximately equal to 1.30 and J_0 to 2.38E-11 A/cm². To obtain the V_{OC} measured under illumination, n=1.24 needed to be introduced in the following equation:

$$V_{oc} = \frac{nkT}{e}\log\left(\frac{J_{sc}}{J_0}\right) \tag{86}$$

Upon annealing, this cell evidenced an increase in the dark current in the reverse and the forward bias range, up to 0.4 V. At reverse bias, we suspect that since our 2x2 cm² SHJ solar cells were defined upon ITO deposition and not upon p-layer deposition, the dark current is increased by lateral effects. However, at a higher forward bias, i.e., for 0.4<V<0.7, the dark currents are almost perfectly superimposed, especially considering that we are dealing with log values of J. Between 0.65 and 0.7 V, the currents are still equal, confirming the stability of our V_{OC}, as measured under illumination. At V=0.7, i.e., just above our V_{OC}, the series resistance (R_S) kicks in.

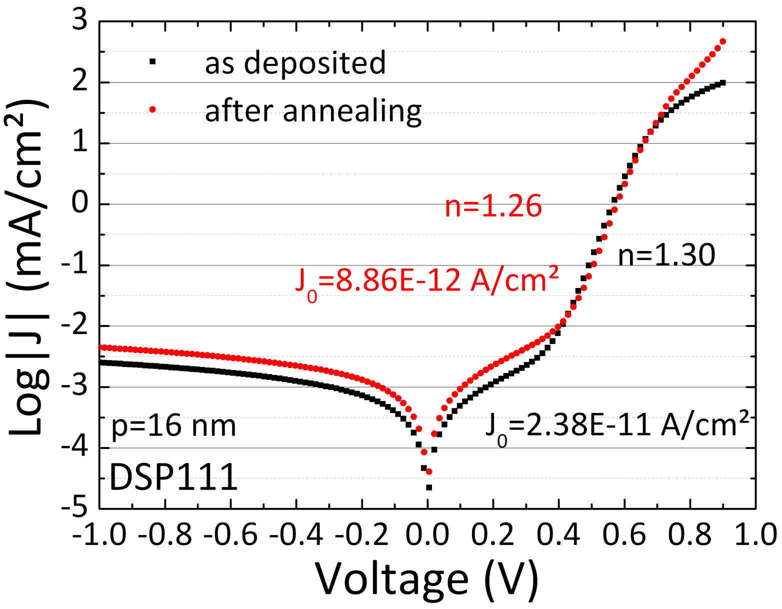

Figure 4-6 – Dark JV characteristics of a SHJ solar cell fabricated with a flat (111) wafer before and after annealing.

However, after annealing, the impact of the R_S becomes much weaker, thereby confirming that the Ag/ITO contact must have improved upon annealing, and that the decrease in FF must come from increased recombination phenomena due to a decrease in the shunt resistance mainly. Finally, after annealing, the ideality factor decreased down to 1.26 and J_0 down to 8.86E-12 A/cm², showing an overall improvement of the pn junction. By using Eq. 86 and choosing n=1.18, a V_{OC} of 675 mV could be obtained, pointing again at a precision of the order of ±0.1 rather than the expected ±0.01 for n. To conclude, our standard recipe allows for the fabrication of SHJ solar cells on flat (111) substrates with conversion efficiencies close to 17%. Upon annealing, we do not witness any V_{OC} increase or efficiency increase upon annealing under conditions where symmetrical i/i stacks would improve. Therefore, we should not expect any improvements upon annealing cells fabricated on textured substrates using our standard recipe either.

4.1.2.b Direct transfer of our standard SHJ recipe to textured c-Si substrates

In order to fabricate SHJ solar cells using textured substrates, we needed to adapt our PECVD deposition recipes. Indeed, when depositing on randomly distributed pyramids, the deposition times used for flat c-Si surfaces have to be adjusted to compensate for the geometrical differences. Usually, the deposition time is multiplied by √3 since the surface is enhanced by such a factor[235], as seen in 3.2.2.b. As a result, the perpendicular thickness d becomes equivalent to that of a flat surface, as shown in Figure 4-7a). In this way, the passivation level is maintained, especially its field-effect component while absorption losses in the a-Si:H are slightly enhanced since light beams impinge the sample perpendicularly and travel over a longer path. Consequently, our deposition times were multiplied by 1.73 for the intrinsic and n-doped a-Si:H layer, yielding the global structure depicted in Figure 4-7b). Throughout all of the experiments presented in this chapter, these would be kept constant while other parameters, e.g., carbon incorporation, p-doped layer thickness, would vary. To start studying the impact of texturation on the SHJ solar cell efficiency, the p-layer was kept identical, i.e., close to 16 nm as in the case of the DSP111 reference shown previously.

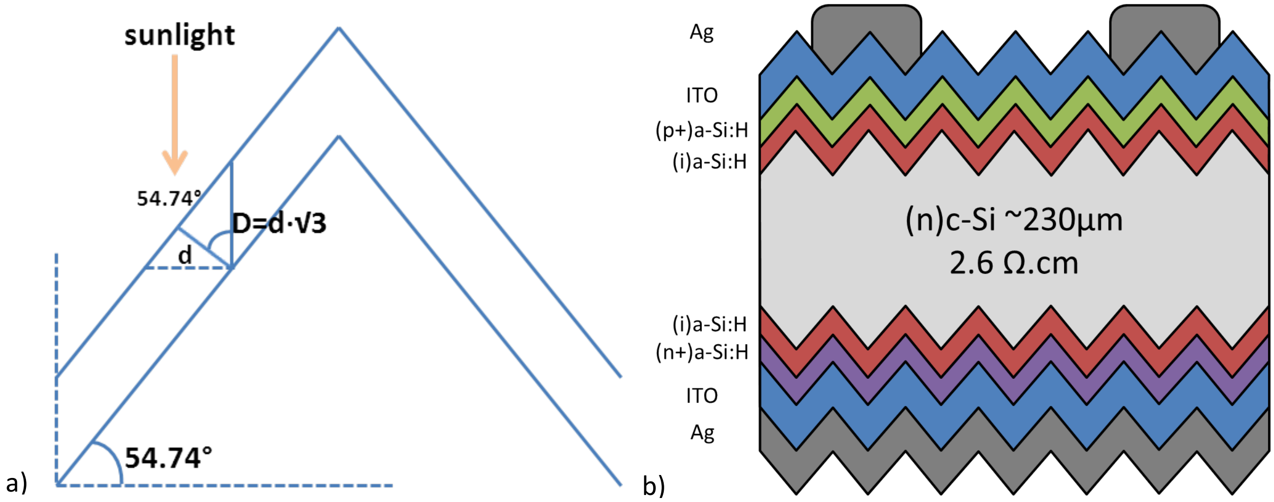

Figure 4-7 – a) schematic representation of the impact of texturation on the deposition time and b) structure of a textured SHJ. The diagrams are not drawn to scale.

The light JV characteristics of such SHJ solar cells are shown in Figure 4-8 in their as-deposited state. As expected, we witness a major increase in current. Indeed, by using textured c-Si substrates, the J_{SC} goes from 31.8 mA/cm² to values closer to 35 mA/cm². However, the most striking feature is the very low V_{OC} that both textured cells exhibit, i.e., around 640 mV. This represents a difference greater than 30 mV with respect to their flat counterpart (dashed grey line), leading to efficiencies actually lower than in the case of a flat wafer. This can be explained by the difference in passivation induced by the larger area and by possible local epitaxial growth on c-Si imperfections, as seen in Chapter 3. Table 4-1 shows the effective lifetimes and iV_{OC}s extracted from PCD measurements on the SHJ solar cell precursors in their as-deposited state.

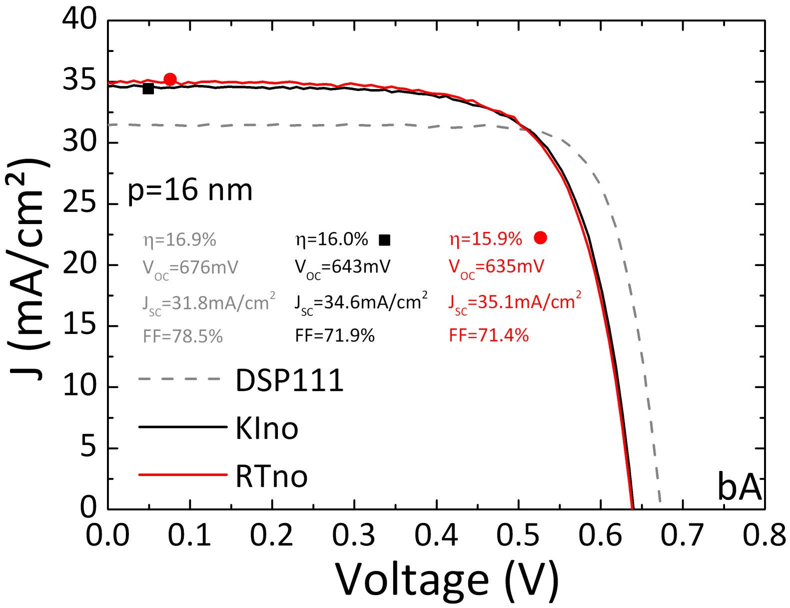

Figure 4-8 – JV characteristics of SHJ solar cells fabricated with textured wafers (as-deposited). A flat (111) reference is also shown (dashed line).

Even though the effective lifetime is much lower in the case of both textured samples, the initial implied V_{OC} remains quite close to that of the flat precursor.

Sample	As deposited		After ITO deposition	
	τ_{eff} [µs]	iV_{OC} [mV]	τ_{eff} [µs]	iV_{OC} [mV]
DSP111	1005	687	762	682
KIno	434	676	255	657
RTno	528	681	236	654

Table 4-1 – Passivation level of the three different cell precursors, before and after ITO sputtering.

The differences in V_{OC} of the three finalized devices are actually due to the fact that by studying the cells in their as-deposited state, we are actually looking at a degraded state. Indeed, as we will see in 4.2, ITO deposition by PVD induces a degradation of the passivation involving complex mechanisms. However, we can already see that by measuring the PCD on the SHJ solar cell precursor after ITO deposition, textured samples degrade much more than the flat cell. Indeed, they experience a loss in iV_{OC} ranging from 19 to 27 mV, whereas the flat precursor decreases by 5 mV only. Figure 4-9 shows the JV characteristics under illumination of the same cells after an annealing process under our standard H_2/N_2 conditions at 180°C. As can be seen, upon annealing, the V_{OC} does not increase substantially, apart from the RTno sample, which experiences an increase from 635 mV up to 643 mV.

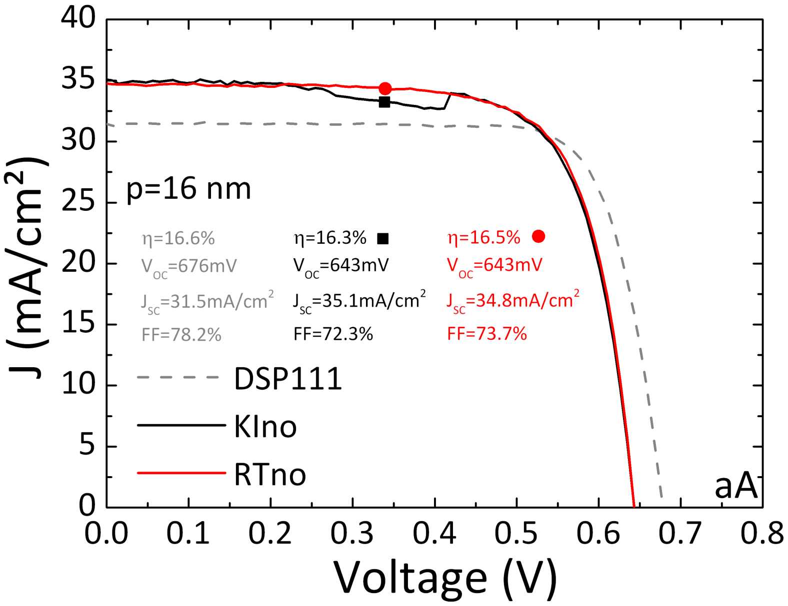

Figure 4-9 – JV characteristics of SHJ solar cells fabricated with textured wafers (after annealing). A flat (111) reference is also shown (dashed line).

While the currents remain unchanged the FF increases in the case of the textured cells, showing an improvement of the Ag/ITO contacts and a decrease of the R_S. All the cell parameters are presented in Table 4-2. Despite the improvements experienced upon annealing, the efficiencies remain quite low, mainly due to a V_{OC}, which does not recover from the degradation upon ITO deposition. Indeed, all values remained lower than those of the flat (111) reference. To further analyze the impact of texturing, JV characteristics were measured in the dark. Results are shown in Figure 4-10. As can be seen, in the best case using a textured c-Si substrate instead of a flat one increases the dark current by one order of magnitude. This is due to enhanced recombination phenomena at the a-Si:H/c-Si interface solely, inasmuch as all other parameters were kept constant.

Cells	state	Eff. [%]	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	R_{OC} [Ω/cm^2]	R_{SC} [Ω/cm^2]
DSP111 std	bA	16.9	676	31.8	78.5	0.352	1011
	aA	16.7	676	31.5	78.5	0.463	1523
KIno std	bA	16.0	643	34.6	71.9	0.351	2472
	aA	16.3	643	35.1	72.3	0.292	1241
RTno std	bA	15.9	635	35.1	71.4	0.402	280
	aA	16.5	643	34.8	73.7	0.370	285

Table 4-2 – Performance parameters of SHJ solar cells fabricated on flat (111) and textured n-type c-Si wafers.

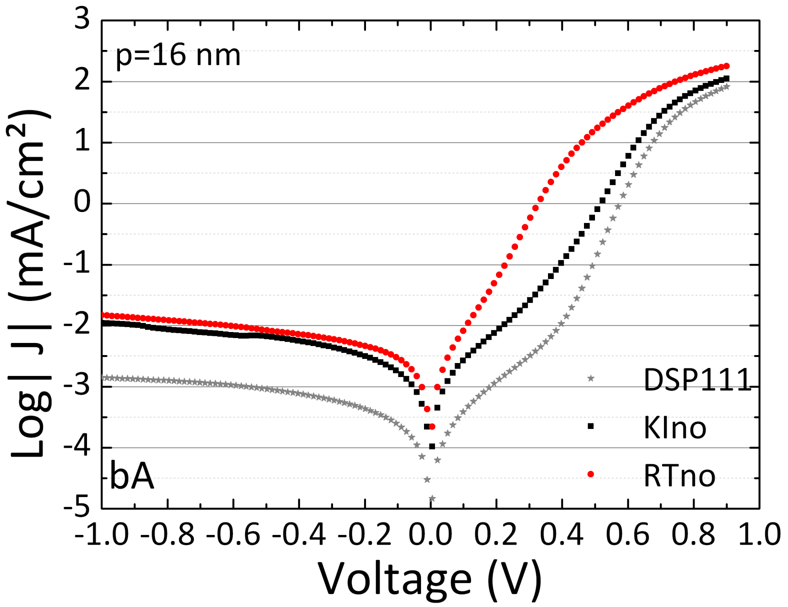

Figure 4-10 – Dark JV characteristics performed on as-deposited textured SHJ solar cells fabricated using our standard recipe. A flat reference is given in grey (dashed line).

It is noteworthy that the impact of R_S seems more important in the case of textured substrates, despite the quite similar R_S values extracted close to V_{OC}. Figure 4-11 shows the dark JV characteristics of the same samples after annealing. Here, the impact of R_S seems to be slightly reduced while we experience a general increase of the dark current in the forward bias region for the KIno cell. The RTno cell on the other hand improves slightly, confirming the increase in V_{OC} experienced under illumination. However, the significant difference with the flat reference testifies to an increase in recombination at the emitter/c-Si interface and in the a-Si:H bulk. Indeed, the shape of the curves for KIno and RTno and thus, their slope, remained almost constant when measured as a function of temperature in the 20-60°C range, pointing at a tunneling-limited current. The tunneling current strongly depends on the density of localized states in the a-Si:H bulk[238]. The role of the intrinsic layer is therefore very important since it has a much lower density of localized states than its doped counterpart, and can reduce the probability of tunneling through them. Between 0.1 and 0.4 V the values of the current are much lower than J_{SC}, thereby minimizing the impact of such a dark current change. However, the discrepancy observed between the performance of Kino and RTno cells with the flat reference and their lack of improvement upon annealing seem to confirm the absence of a perfectly abrupt a-Si:H/c-Si interface.

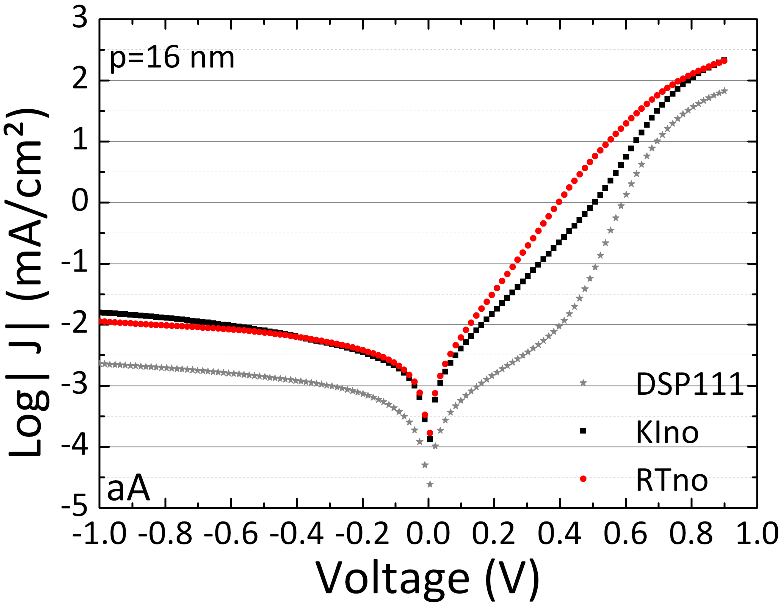

Figure 4-11 – Dark JV characteristics performed on annealed textured SHJ solar cells fabricated using our standard recipe. A flat reference is given in grey (dashed line).

To conclude, transferring our recipes for the fabrication of SHJ solar cells from flat wafers to textured substrates was unsuccessful. Indeed, despite the presence of doped layers, the level of passivation remained quite low, pointing to a higher interface recombination. This resulted in conversion efficiencies lower than those obtained on flat (111) c-Si wafers. Consequently, it was decided that the thin a-SiC:H buffer layer should be implemented within the SHJ solar cell architecture to impede any local epitaxial growth and to obtain a more abrupt a-Si:H/c-Si interface.

4.1.3 Impact of a thin a-SiC:H layer at the a-Si:H/c-Si interface: flat (111) SHJ solar cells

Before trying implementing the thin a-SiC:H buffer layer to improve the passivation and perhaps decrease the dark current on textured SHJ solar cells, its impact on flat (111) SHJ solar cells needed to be studied. Indeed, even if its thickness remains quite small (~2-2.5 nm) and its impact was proven to be non-existent on the effective lifetime and implied V_{OC} of symmetrical i/i stacks (see section 3.2.2.a), one might wonder about the impact of the presence of a thin a-SiC:H layer on the carrier collection. Indeed, the presence of carbon increases the structural and chemical disorder within the intrinsic a-Si:H layer[239]. As a result, the quality of the a-SiC:H/c-Si interface cannot be identical to that of an interface obtained with a pure intrinsic layer in terms of conductivity. However, since this layer is quite thin, the increase in V_{OC} should be able to compensate for the slight collection impediment that could occur. Figure 4-12 shows the imaginary part of the pseudo-dielectric function of a 45 nm-thick a-SiC:H layer grown under our conditions on a flat (100) c-Si substrate. Thanks to this measurement, not only were we able to assess the growth rate of this material to be only slightly lower than pure intrinsic a-Si:H (~0.63 Å/s) but also to extract some interesting information on its structural properties. Indeed, along with a very nice figure of merit (X^2~0.07), we found an amplitude A=202 and a disorder parameter C=2.30. This indicates that this material is quite similar to our standard intrinsic a-Si:H layer in terms of density (A close to 205). However, it is also more disordered since C usually stays close to 2.10 for (i)a-Si:H. This last piece of data confirms what can be found in the literature and possibly points to higher resistivity to be taken into account upon the optimization of SHJ solar cells on textured substrates.

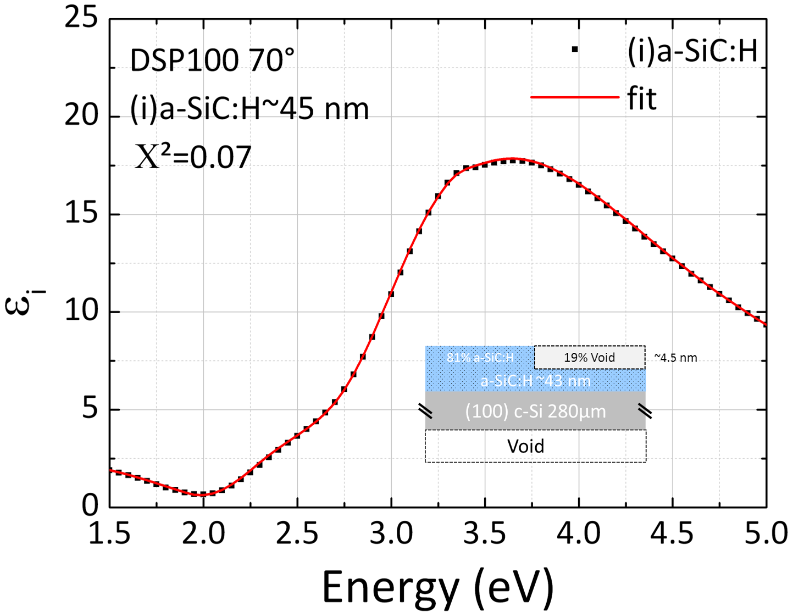

Figure 4-12 – Imaginary part of the pseudo-dielectric function of a 45 nm-thick a-SiC:H layer grown on a flat (100) c-Si wafer.

To this end, flat (111) cells were fabricated with an a-SiC:H buffer layer at both a-Si:H/c-Si interfaces to be compared with our standard SHJ structure. Figure 4-13a) shows the typical structure of a flat SHJ solar cell whereas Figure 4-13b) shows the "improved" structure, wherein a thin a-SiC:H buffer layer was introduced at both a-Si:H/c-Si interfaces. All other parameters were kept constant in terms of thickness and deposition conditions and the p-layer thickness was maintained at 16 nm. The thin a-SiC:H was grown under the same conditions as described in 3.2.2.a and $t_{a\text{-}Si:H}=t_{a\text{-}SiC:H}$, so that approximately half of the intrinsic layer was made of a-SiC:H.

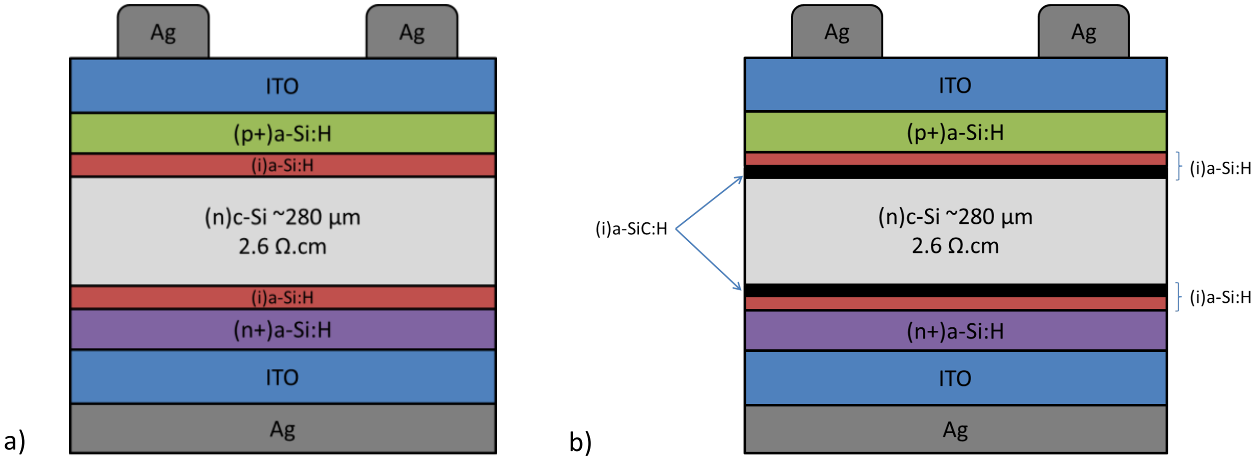

Figure 4-13 – a) Schematic structure of a standard flat SHJ and b) with a thin a-SiC:H buffer layer at the a-Si:H/c-Si interfaces (diagram not drawn to scale).

Prior to cell finalization (ITO sputtering and Ag evaporation), PCD measurements were performed on SHJ solar cell precursors to assess the impact of the a-SiC:H buffer layer at the a-Si:H/c-Si interface. These specific samples contain an improved p-layer as will be discussed later in 4.2. However, they both are identical and only differ by the presence or not of the thin a-SiC:H buffer layer at the a-Si:H/c-Si interface. Therefore, these are very representative of its negligible impact in terms of passivation. As Figure 4-14 shows, its introduction did not impact the level of passivation at all, thereby confirming the results obtained on i/i symmetrical stacks in section 3.2.2.a. Indeed, this time, both the effective lifetimes and the iV_{OC}s are identical (1664 and 1667 µs rounded up to 1.7 ms), showing also the very high reproducibility of our cleaning conditions and PECVD deposition processes.

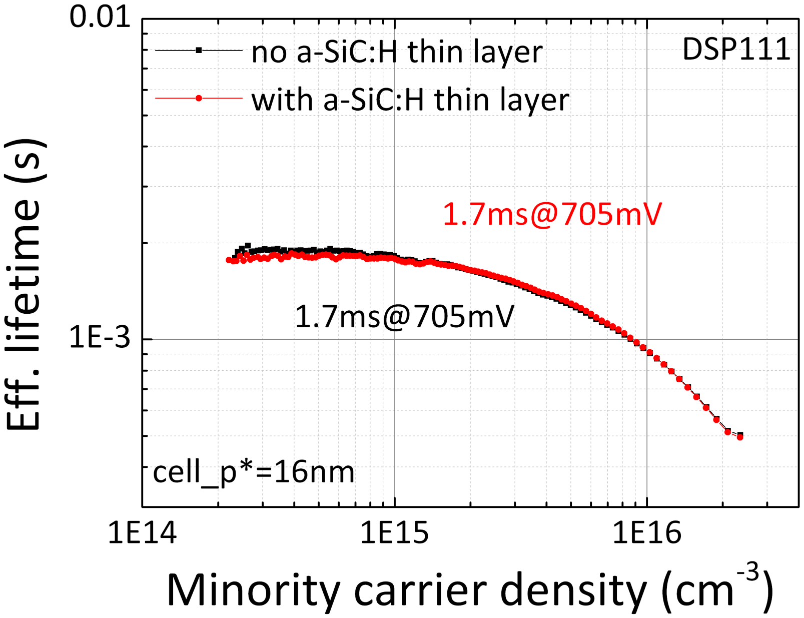

Figure 4-14 – Effective lifetime of two SHJ solar cells deposited on flat (111) c-Si wafers using the exact same conditions, differing only by the presence of a thin a-SiC:H layer at a-Si:H/c-Si interfaces for the second (red dots).

On this graph, one can see a slightly lower field-effect passivation at low injection. However, this difference can be treated as part of the measurement error. After finalization, dark IV measurements were performed on the two cells mentioned earlier (standard p-layer). As can be seen in Figure 4-15, in their as-deposited state, the dark currents of both cells overlap quite nicely in the whole bias range, from -1.0 V up to 0.6 V. This confirms that the introduction of a thin a-SiC:H layer does not change the quality of the interface, either by enhancing, nor by degrading the recombination velocity. It is also noteworthy that the properties of the diode remain unchanged, which is not easily obtained since the presence of carbon could induce some screening effects and reduce the efficiency of the field generated by the pn junction. However, when fitting the $0.4<V<0.6$ bias region, we see that the slopes are not exactly the same. The presence of carbon at the interface induces an increase in the ideality factor, which becomes close to 1.41. Moreover, the dark saturation current increases from 2.38E-11 A/cm² up to 9.00E-11 A/cm², showing a slight degradation of our diode with a possible greater impact of the series resistance. Indeed, after 0.6 V and beyond, the two cells exhibit quite different dark JV characteristics. The presence of the a-SiC:H thin layer makes the R_S kick in much earlier than in the case of our standard cell. This confirms our prediction based on the greater disorder observed by ellipsometry. Even though carbon does not affect our cells in terms of passivation, it seems to have quite an impact on the series resistance.

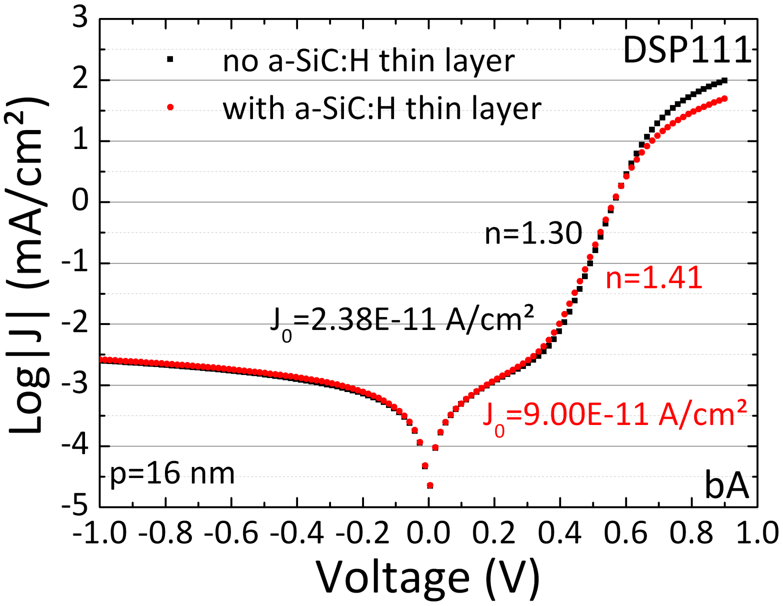

Figure 4-15 – Dark JV characteristics of two SHJ solar cells deposited on flat (111) c-Si wafers using the exact same conditions, differing only by the presence of a thin a-SiC:H layer at a-Si:H/c-Si interfaces for the second one (red dots) (as-deposited).

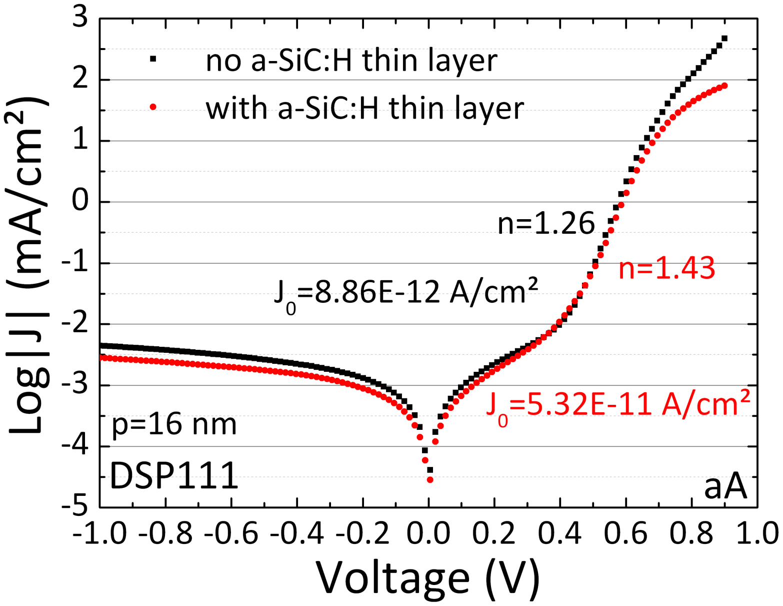

Figure 4-16 – Dark JV characteristics of two SHJ solar cells deposited on flat (111) c-Si wafers using the exact same conditions, differing only by the presence of a thin a-SiC:H layer at a-Si:H/c-Si interfaces for the second one (red dots) (annealed).

In order to verify this assertion, these two samples were annealed. As seen earlier, annealing the standard cell leads to a general improvement of the diode by decreasing the n and J_0 factors. Moreover, it induces improved Ag/ITO contact, thus leading to a lower impact of the R_S at higher biases. Interestingly enough, annealing the “improved” cell, which contains carbon at the a-Si:H/c-Si interface leads, to very few changes. The ideality factor stays around the initial value and even increases slightly, whereas J_0 improves somewhat by decreasing by roughly half an order of magnitude. The most striking feature is perhaps the fact that the impact of the R_S stays quite strong, despite the Ag/ITO contact improvement that presumably occurs upon thermal annealing. This means that we are here limited by something else, which could be related to the presence of carbon at the a-Si:H/c-Si interface. For comparison purposes, the dark JV characteristics of the standard and “improved” SHJ cells before and after annealing are shown in Figure 4-17a) and b), respectively, and the diode parameters extracted therein are presented in Table 4-3.

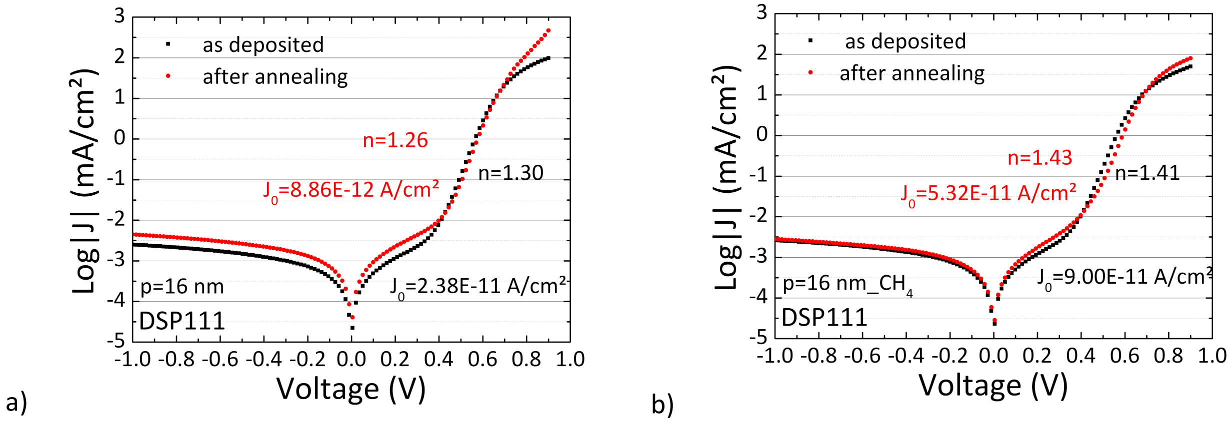

Figure 4-17 – Evolution upon thermal annealing of the a) dark JV characteristics of a standard SHJ solar cell deposited on flat (111) c-Si wafers and b) dark JV characteristics of a SHJ solar cell fabricated using the exact same conditions, differing only by the presence of a thin a-SiC:H layer at a-Si:H/c-Si interfaces.

Cell	state	Ideality factor n	J_0 [A/cm²]
DSP111_noCH_4	bA	1.30	2.31E-08
	aA	1.26	8.86E-09
DSP111_CH_4	bA	1.41	9.00E-08
	aA	1.43	5.32E-08

Table 4-3 – Evolution upon thermal annealing of the diode parameters of a standard and “improved” SHJ solar cell fabricated with flat (111) c-Si wafers.

To further analyze these two samples, JV characteristics were also measured under illumination. Figure 4-18 shows the impact of the a-SiC:H buffer layer on the performance of the flat SHJ solar cell. The most striking features are mainly the drop in current accompanied by a higher series resistance. Indeed, the difference in V_{OC} is consistent with the difference noticed on the PCD measurements of the solar cell precursors. Indeed, as opposed to what could be seen in Figure 3-38 and Figure 4-14, the iV_{OC}s were slightly different (687 mV for the standard cell versus 700 mV for the cell with the a-SiC:H layer). Since it was one of the rare occurrences of such a difference, either on i/i symmetrical stacks or on solar cell precursors, we maintain the statement that the introduction of carbon at the a-Si:H/c-Si interface of a (111)-oriented c-Si wafer does not change the interface defect density, either by a more efficient saturation of dangling bonds or by a short increase in the bandgap on a 2-nm length, that would virtually increase the splitting of the quasi-Fermi levels and thus induce a higher V_{OC}. We will therefore focus on the other parameters while keeping an eye on the evolution of the V_{OC} upon annealing.

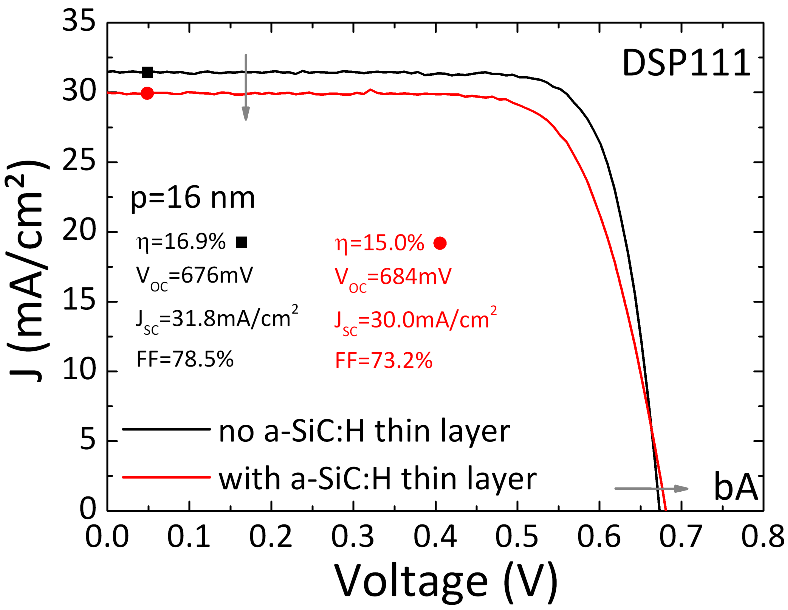

Figure 4-18 – JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on flat (111) c-S wafers (as-deposited).

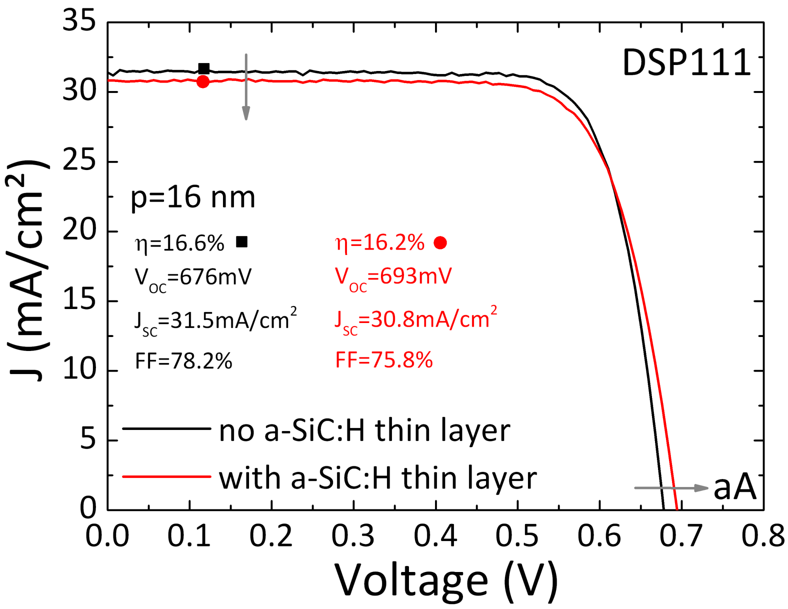

Figure 4-19 – JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on flat (111) c-S wafers (after annealing).

Here, introducing carbon at the a-Si:H/c-Si interface induces a drop in J_{SC} of about 2 mA/cm². As expected, the R_S also increases and the FF drops from above 78 to 73.2%. We are definitely dealing with a collection-related issue induced by the a-SiC:H layer. As a result, the efficiency is lower by almost 2 points, despite a V_{OC} higher by 8 mV. In order to differentiate this phenomenon and poor Ag/ITO contact, the two cells underwent our standard annealing procedure. The resulting JV characteristics are shown in Figure 4-19. Here again, the V_{OC} is higher in the case of the cell with the thin a-SiC:H layer at the a-Si:H/c-Si interface. However, it is worth noting that contrary to our standard cell, it has actually increased by almost 10 mV. In contrast, our standard cell exhibits the exact same V_{OC}, showing a total lack of improvement of the interface quality. Moreover, this annealing step enhanced the charge carrier collection of our “improved” structure. Indeed, the J_{SC} is now very close to that of the standard cell, with a value of 30.8 mA/cm² while the FF has increased by almost 76%, i.e., to only 2 points below the standard cell. The lack of improvement on the standard cell in terms of collection however, shows that some recombination effects must have been enhanced because the Ag/ITO contacts definitely improve under these conditions. For comparison purposes, the evolution of the performance of both solar cells is shown in Figure 4-20.

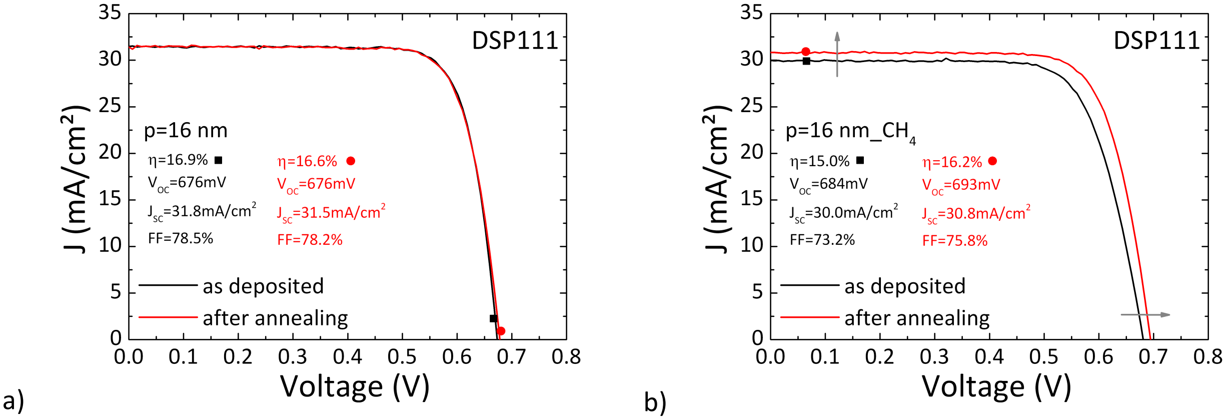

Figure 4-20 – Evolution upon annealing of the performance of SHJ solar cells fabricated a) without and b) with a thin a-SiC:H layer at the a-Si:H/c-Si interface on flat (111) c-S wafers.

In an attempt to understand how the thin a-SiC:H layer could interfere with the collection process, the band diagram of the SHJ structure was simulated using AFORS-HET.

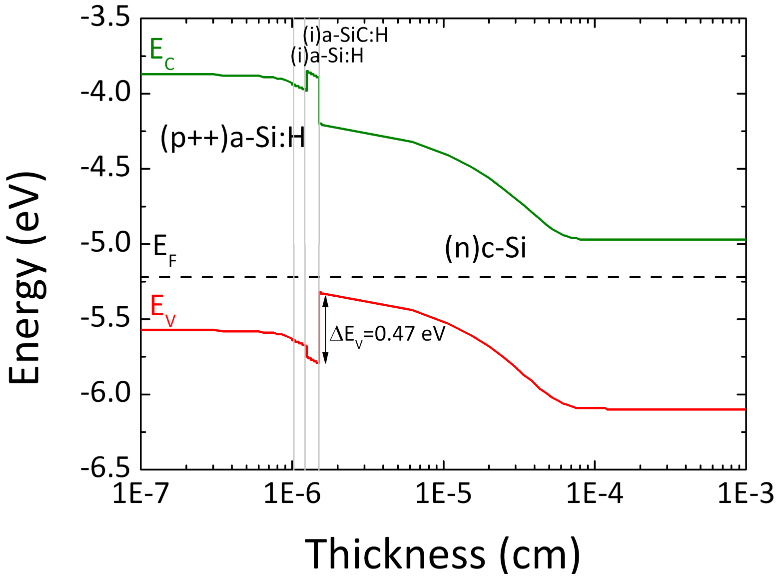

Figure 4-21 – Band diagram of a (i)a-Si:H/(i)a-SiC:H/(n)c-Si heterostructure simulated with AFORS-HET.

By introducing a 1.9 eV thin layer at the a-Si:H/c-Si interface and by merely replacing the 3.88 eV value of the electronic affinity of a-Si:H with a realistic value of 3.75 eV for a-SiC:H, we obtain the band diagram shown in Figure 4-21. Despite the small thickness of the a-SiC:H layer and despite the significant band mismatch in the conduction band, the simulation exhibits a band mismatch of 0.47, i.e., 0.7 eV higher than usual, in the valence band, thus making the hole collection much harder. Therefore, one may think of this layer as a more defective and thus resistive (i)a-Si:H layer, which naturally induces an increase in R_S and a lower FF.

To conclude, adding a thin a-SiC:H layer at the a-Si:H/c-Si interfaces hinders the whole collection process and increases the R_S, resulting in lower J_{SC} and FF values. This eventually leads to a decrease in the conversion efficiency by 2 points, approximately. Fortunately, our standard annealing procedure shows that the a-SiC:H/c-Si is more prone to improvements and can compensate for the losses induced by its higher resistivity by increasing the V_{OC}. Moreover, an improvement of the Ag/ITO contacts is evidenced. This in turn results in an increase of the J_{SC} and FF, leading to an efficiency comparable to that of our standard SHJ cell. The main cell parameters are summarized in Table 4-4.

Cells	state	Eff. [%]	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]	R_{OC} [Ω/cm²]	R_{SC} [Ω/cm²]
DSP111 std	bA	16.9	676	31.8	78.5	0.352	1011
	aA	16.6	676	31.5	78.2	0.454	1115
DSP111 CH_4	bA	15.0	684	30.0	73.2	0.660	946
	aA	16.2	693	30.8	75.8	0.579	410

Table 4-4 – Evolution upon thermal annealing of the conversion efficiencies of a standard and "improved" SHJ solar cell fabricated on flat (111) c-Si wafers.

Of course, this is valid only for this particular sample which exhibits a higher initial V_{OC} (and iV_{OC}). However, when assuming an identical V_{OC} of 676 mV and the same increase of +8 mV after annealing while keeping all the other parameters constant (J_{SC}=30.8 mA/cm² and FF=75.8%), we still obtain an efficiency of 0.676x30.8x0.76~16.0%, i.e., only 0.6 point lower than our standard cell. In Table 4-5 is presented the evolution of the passivation of two symmetrical i/i samples passivated with a standard 20 nm-thick a-Si:H layer deposited under our standard conditions. One of these has a 2-nm thin a-SiC:H layer at the a-Si:H/c-Si interface.

Sample	As-deposited		After annealing	
	τ_{eff}	iV_{OC}	τ_{eff}	iV_{OC}
i/i with no a-SiC:H layer	4.1	726	3.6	720
i/i with a-SiC:H layer	3.6	724	3.9	723

Table 4-5 – Evolution upon thermal annealing of the passivation of a standard and "improved" i/i passivated stack fabricated with flat (111) c-Si wafers.

As can be seen, there is no noticeable difference in the passivation level compared to the effective lifetime or the iV_{OC}. After annealing under our standard H_2/N_2 conditions at 180°C, we do not observe any significant change. This shows that adding carbon at the a-Si:H/c-Si interface does not lead to any improvement or degradation upon annealing on a (111) flat surface. Therefore, the increase in V_{OC} experienced on the DSP111 cell must rather originate from an improvement of the p-layer by dopant activation, for example. The fact that this improvement occurs on the sample with a thin carbonated layer at the a-Si:H/c-Si interface raises the question of a possible protecting effect of carbon on the interface.

From this study we conclude that implementing a thin a-SiC:H layer at the a-Si:H/c-Si interface of SHJ solar cells fabricated with flat (111) wafers does not have any impact in terms of passivation. This was confirmed by the effective lifetimes and implied V_{OC}s of i/i symmetrical stacks and SHJ solar cell precursors, which turned out to be close to identical. Finalized SHJ solar cells exhibited quite different characteristics in their as-deposited state though, with a quite important charge collection impediment due to the presence of carbon at the a-Si:H/c-Si interface. Moreover, the behavior of these SHJ cell precursors upon annealing is quite different, showing a V_{OC} increase solely in the case where a thin a-SiC:H layer was present, despite the fact that this could not be observed on i/i symmetrical stacks. As a result, flat (111) SHJ solar cells exhibit close-to-identical conversion efficiencies thanks to similar J_{SC}s and higher V_{OC} values, thereby compensating for the higher R_S found when adding carbon at the a-Si:H/c-Si interface. Therefore, we should expect the same results on textured substrates. We therefore predict that the V_{OC} should improve when adding carbon at the a-Si:H/c-Si and at least compensate for the higher R_S and lower FF.

4.1.4 Impact of a thin a-SiC:H layer at the a-Si:H/c-Si interface: textured SHJ solar cells

In order to assess the impact of carbon at the a-Si:H/c-Si interface of textured c-Si wafers, two types of SHJ samples were fabricated: with and without a thin a-SiC:H layer at the interface. For both kinds of cells the n-side was kept constant in terms of thickness and a-Si:H/c-Si interface by: i) using the same deposition times for the n-layer, ITO and silver; ii) impeding any local epitaxial growth by adding carbon at the a-Si:H/c-Si interface. On the p-side however, one sample was prepared with a standard intrinsic a-Si:H layer, while the other one had a thin a-SiC:H buffer layer as part of the intrinsic a-Si:H layer. All the remainder was kept constant in terms of thickness and material properties for the p-layer (~16nm), ITO (~82 nm) and silver (~1 µm). These two types of samples are sketched in Figure 4-22.

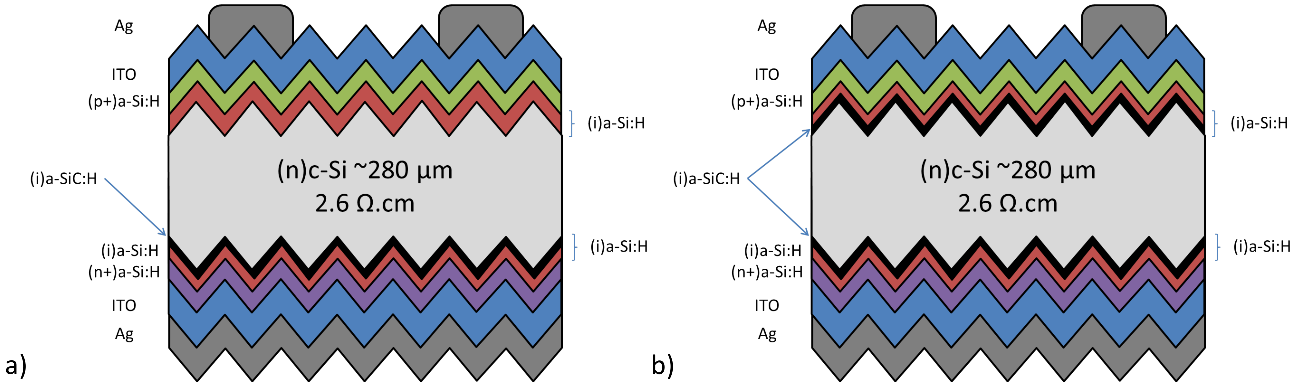

Figure 4-22 – Schematic representation of a classical HiT cell, as developed by Sanyo[240][176] with an additional thin a-SiC :H layer at the back a-Si:H/c-Si interface (left-hand side), and of an “improved” HiT structure containing a thin a-SiC :H layer at the back and at the front a-Si /c-Si interface (right-hand side). These structures are not drawn to scale.

The goal was to compare the passivating properties and cell characteristics and to understand if the presence of carbon at the a-Si:H/c-Si interface could help us reach higher conversion efficiencies. This comparison study was made using the two texturing recipes defined earlier: KIno (KOH/IPA) and RTno (KOH/RenaTex surfactant).

4.1.4.a KIno cells

As expected from the passivation studies carried out in 3.2.2.b, the results were quite striking on KIno wafers. As can be seen in Figure 4-23, adding a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface of SHJ cell precursors doubles the effective lifetime and leads to a +20mV increase of the V_{OC}. It is noteworthy that the improvement occurs at high injection levels, showing a clear decrease in the defect-related recombination at the a-Si:H/c-Si interface (SRH component). Moreover, the enhancement induced at low-injection levels testifies to a more efficient field-effect made possible by the neutralization of all epitaxial growth, which usually results in a strong screening effect.

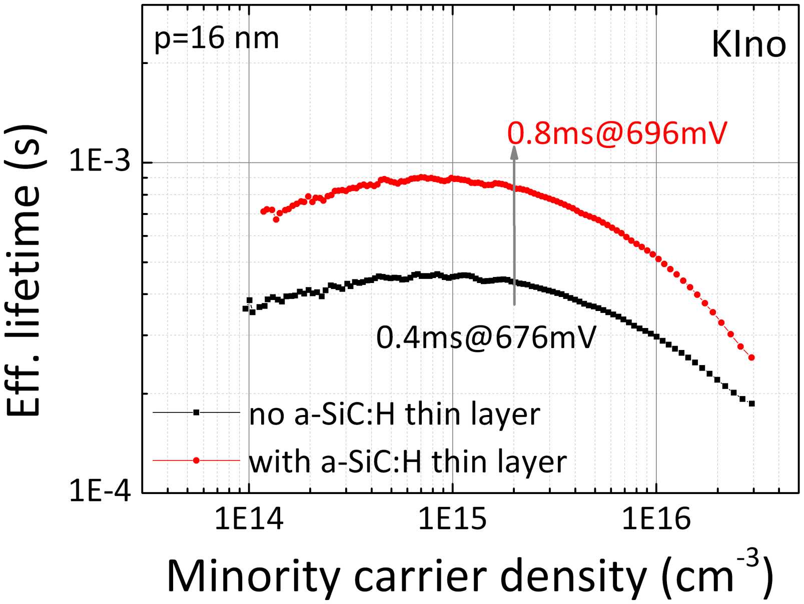

Figure 4-23 – Impact of a thin a-SiC:H layer on the effective lifetime of a SHJ solar cell precursor fabricated on a KIno wafer.

SHJ solar cells were finalized by sputtering ITO and evaporating silver for the contacts. Light JV characteristics of the same samples are shown in Figure 4-24. The impact of carbon at the a-Si:H/c-Si interface is, again, striking.

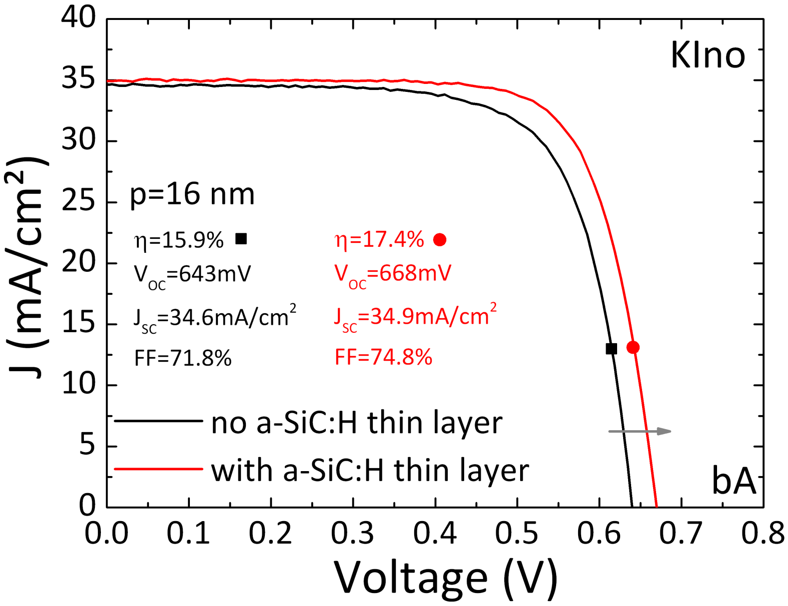

Figure 4-24 – JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on KIno textured c-Si wafers (as-deposited).

Indeed, carbon appears to be highly beneficial for the V_{OC}, which has increased from the very poor 643 mV level up to the quite honorable 668 mV one. Moreover, this time the impact on the charge carrier collection cannot be seen directly on the J_{SC}. However, the quite low FF (71.8%) testifies to a collection that is strongly hindered when using our standard intrinsic a-Si:H layer. When using carbon at the a-Si:H/c-Si though, the FF increases up by almost 75 %. Although we are not close to state-of-the art values, this improvement related to the presence of carbon suggests that local epitaxial growth is suppressed and the thin a-SiC:H layer becomes beneficial despite its high resistivity. Our charge carrier collection is therefore more deteriorated by the local epitaxial phase at the a-Si:H/c-Si interface than by the presence of carbon. As a result, by introducing carbon at the interface on the p-side we were able to increase the conversion efficiency from 15.9 % to 17.4%. Figure 4-25 shows the JV characteristics of the same SHJ solar cells after a standard annealing step in our standard H_2/N_2 conditions at 180°C. Despite the kink experienced while measuring the standard cell (black squares), all the cell parameters could still be extracted at MPP, and a comparison with the enhanced SHJ solar cell was made possible.

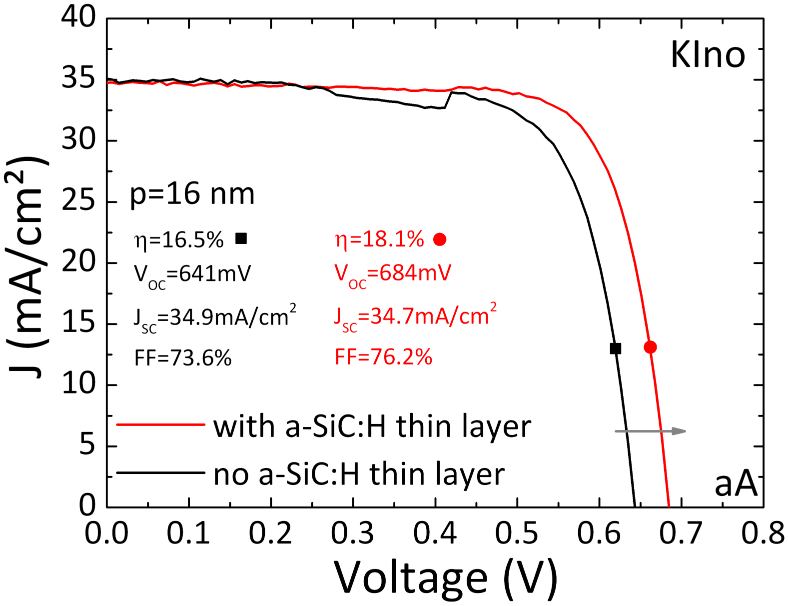

Figure 4-25 – JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on KIno textured c-Si wafers (annealed).

Perhaps the most striking feature is again the V_{OC} and its evolution. With no a-SiC:H layer at the a-Si:H/c-Si interface on the p-side, the V_{OC} does not increase. It actually decreases by 2 mV, suggesting the presence of local epitaxial growth at the interface for the reasons explained in 3.2.2.e. When adding carbon at the a-Si:H/c-Si interface however, improvements in terms of passivation are made possible. As a result, the V_{OC} gains +16 mV, thus reaching 684 mV. Quite interestingly, the FF increases in both cells. This is due to an improved ITO/Ag contact since the collection must still be impacted by the presence of epitaxy or carbon at the interface. Consequently, while the standard cell improves up to 16.5%, the SHJ solar cell with carbon at the interface reaches the value of 18.1%. This represents a difference of 1.6 point and finally, the use of textured wafers leads us to higher conversion efficiencies than those obtained on flat (111) wafers. The cell parameters in their as-deposited and annealed states are presented in Table 4-4 and the evolution of the cell parameters upon annealing is shown in Figure 4-26. As can be seen, by inserting a thin a-SiC:H layer at the a-Si:H/c-Si interface on the p-side, we have enabled a higher passivation level and, hence, a higher V_{OC}. Moreover, because of this, collection is enhanced and the FF is increased. Finally, improvements upon annealing are enabled. Indeed, inasmuch as the lack of local epitaxial growth at the interface allows for the reconfiguration of mobile hydrogen, passivation improves[217]. This in turn fosters an increase of the V_{OC}.

Cells	state	Eff. [%]	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]	R_{OC} [Ω/cm²]	R_{SC} [Ω/cm²]
KIno std	bA	15.9	643	34.6	71.8	0.351	2472
	aA	16.5	641	34.9	73.6	0.292	1241
KIno CH_4	bA	17.4	668	34.9	74.8	0.458	204
	aA	18.1	684	34.7	76.2	0.364	433

Table 4-6 – Evolution upon thermal annealing of the conversion efficiencies of a standard and "improved" SHJ solar cell fabricated with textured KIno c-Si wafers.

As a consequence, due to our interface enhancement, only the second sample experiences increases in the V_{OC} on annealing and, apart from identical J_{SC} values, all of its parameters increase.

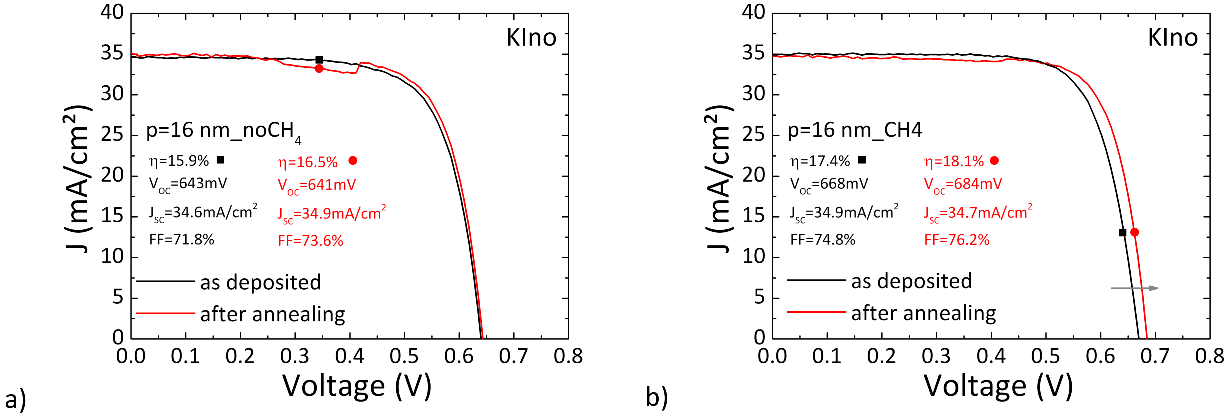

Figure 4-26 – Evolution upon annealing of the performance of SHJ solar cells fabricated a) without and b) with a thin a-SiC:H layer at the a-Si:H/c-Si interface on KIno textured wafers.

In order to assess the impact of carbon on recombination mechanisms at the a-Si:H/c-Si interface, JV measurements were also performed in the dark. Figure 4-27 shows the dark JV characteristics of these two samples in their as-deposited state. The improvements induced by the presence of the a-SiC:H buffer layer are quite significant. Indeed, as can be seen, the dark current is decreased on the whole bias range while the saturation current is reduced by one order of magnitude. This is directly related to the improved abruptness of the a-Si:H/c-Si interface and the neutralization of highly active recombination centers. This was definitely not the case on flat (111) wafers and points to the beneficial epitaxy impediment effect of carbon. This trend is still observed after annealing these samples under our standard H_2/N_2 conditions (Figure 4-28). However, when comparing the as-deposited state with the annealed state for both samples, we see that we witness the same dark current increase. However, for both samples, close to the V_{OC}, the dark currents overlap quite well, showing that the general increase in dark current is not detrimental to the solar cell performance. Therefore, adding carbon at the a-Si:H/c-Si interface on the emitter side of a KIno SHJ solar cell decreases the dark current on the whole bias range before and after annealing. By qualitatively comparing the steepness of the slopes, it is also clear that the addition of carbon improves the diode characteristics.

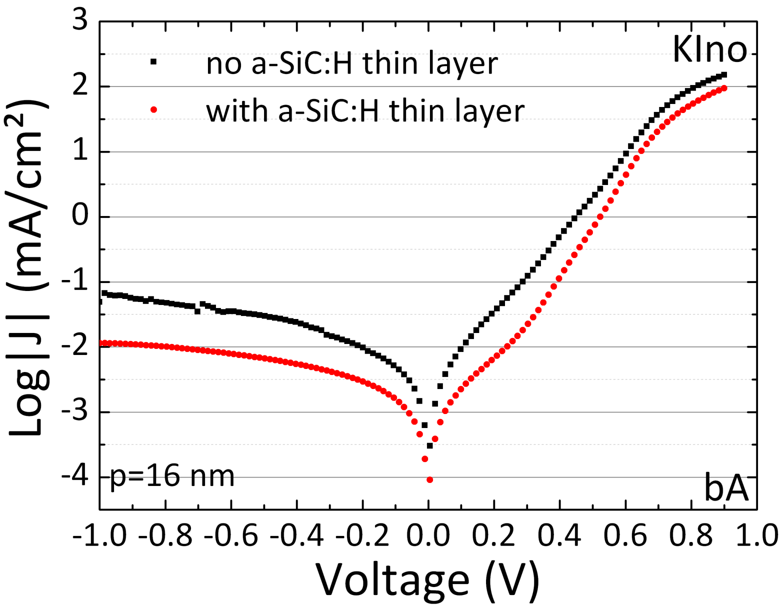

Figure 4-27 – Dark JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on KIno textured c-Si wafers (as-deposited).

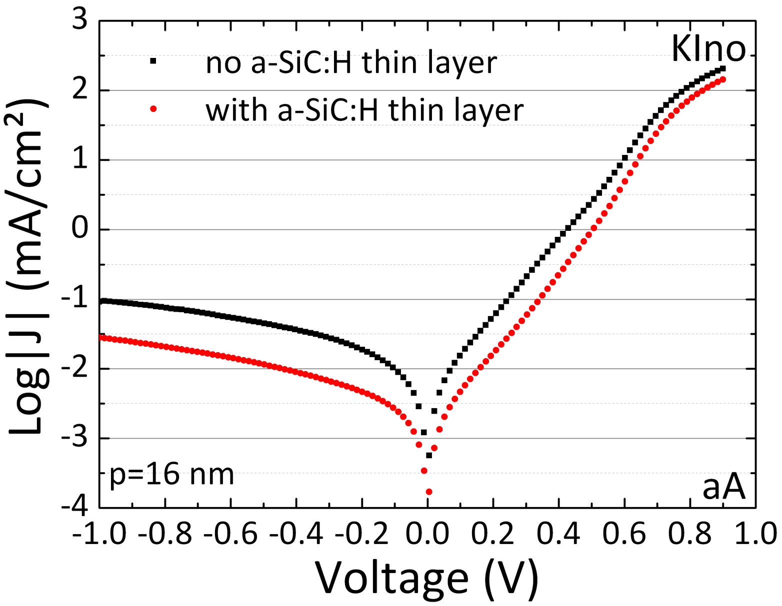

Figure 4-28 – Dark JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on KIno textured c-Si wafers (annealed).

To sum-up, we have seen that adding carbon at the a-Si:H/c-Si interface improves the performance of our textured KIno solar cells by impeding local epitaxial growth. As a result, the dark current is reduced and the V_{OC} is increased. This in turn triggers a stronger collection, as evidenced by a higher FF and, at the end, a higher conversion efficiency. Since the RTno texturation is very different from the KIno one (in terms of pyramid size and homogeneity) and since the preliminary passivation tests carried out on such substrates yielded quite different results, it is interesting to see how the performance of SHJ solar cells on RTno textured wafers can be impacted by the implementation of a thin a-SiC:H layer at the a-Si:H/c-Si interface.

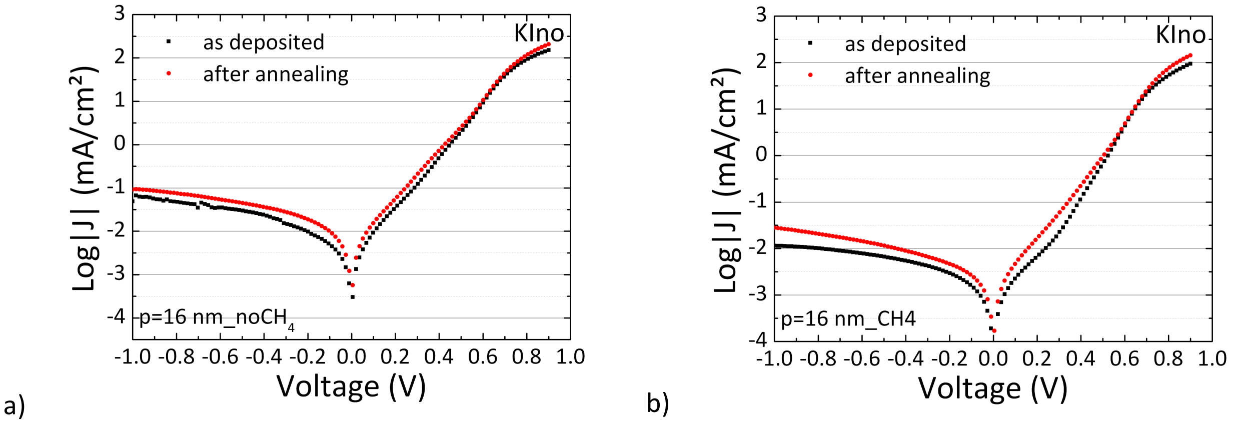

Figure 4-29 – Evolution upon annealing of the dark JV characteristics of SHJ solar cells fabricated a) without and b) with a thin a-SiC:H layer at the a-Si:H/c-Si interface on KTno textured c-Si wafers.

4.1.4.b RTno cells

Two types of RTno cells were prepared for this study just as in the case of KIno wafers: one with a standard intrinsic a-Si:H layer at the a-Si:H/c-Si interface on the emitter side and the other with carbon at this specific interface, as described by Figure 4-22. Again, both of these had an identical BSF side comprising a thin carbide buffer layer followed by a standard intrinsic a-Si:H layer and an n-doped a-Si:H layer. Figure 4-30 shows the effective lifetimes of these two samples as a function of the minority carrier density. The impact of carbon at the a-Si:H/c-Si interface on the emitter side is quite strong. Indeed, thanks to the thin a-SiC:H buffer layer, the effective lifetime more than doubles to reach 1.8 ms, while the iV_{OC} experiences an impressive +35 mV gain. Again, local epitaxial growth deduced from the results presented in 3.2.2 seems efficiently suppressed on RTno substrates, as the effective lifetime has increased over the whole injection range.

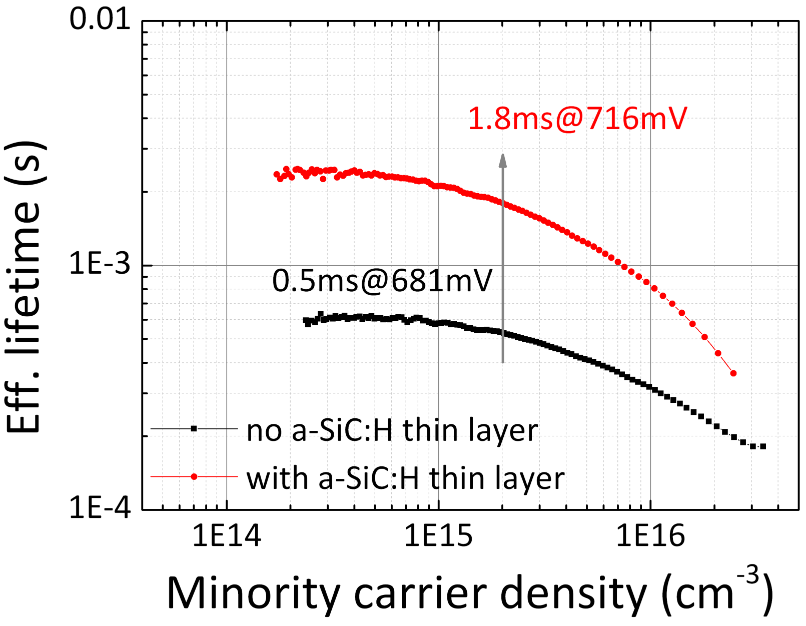

Figure 4-30 – Impact of a thin a-SiC:H layer on the effective lifetime of a SHJ solar cell precursor fabricated on a RTno wafer.

SHJ solar cells were finalized by sputtering ITO and evaporating silver for the contacts. Both light JV characteristics of the same samples are shown in Figure 4-31. The impact of carbon at the a-Si:H/c-Si interface is not so obvious this time. Indeed, the V_{OC} is higher in our enhanced SHJ solar cell (+8 mV) but this time, it remains quite low compared to our KIno cells by reaching only 643 mV. However, the lack of epitaxy at the a-Si:H/c-Si interface enables a stronger charge carrier collection, as reflected by a slightly higher J_{SC} and much higher FF. This time, the carbide layer is less detrimental to the collection than with our KIno cells. Its presence at the interface is beneficial, leading to an overall increase of the conversion efficiency from 15.9% up to 17.2% (+1.3 points). The annealing of these samples was performed under our standard H_2/N_2 conditions at 180°C for 30 minutes. The light JV characteristics measured afterwards are shown in Figure 4-32. This time, the impact of carbon at the interface can be clearly seen. The V_{OC} increases from 643 mV up to 684 mV. This represents a +41 mV increase, not at all present in the other sample which nonetheless yields a +8 mV increase. Contrary to what could be seen on KIno wafers, the FF decreases in our enhanced solar cell whereas the sample with a standard intrinsic a-Si:H layer on the emitter side experiences an increase in the parameter concerned. This could indicate that the charge carrier collection degraded upon annealing when carbon was present at the interface, despite the obvious improvement of the Ag/ITO contacts. This is also reflected by a slight decrease in J_{SC}. However, it is not clear why this occurs only on our RTno SHJ solar cells.

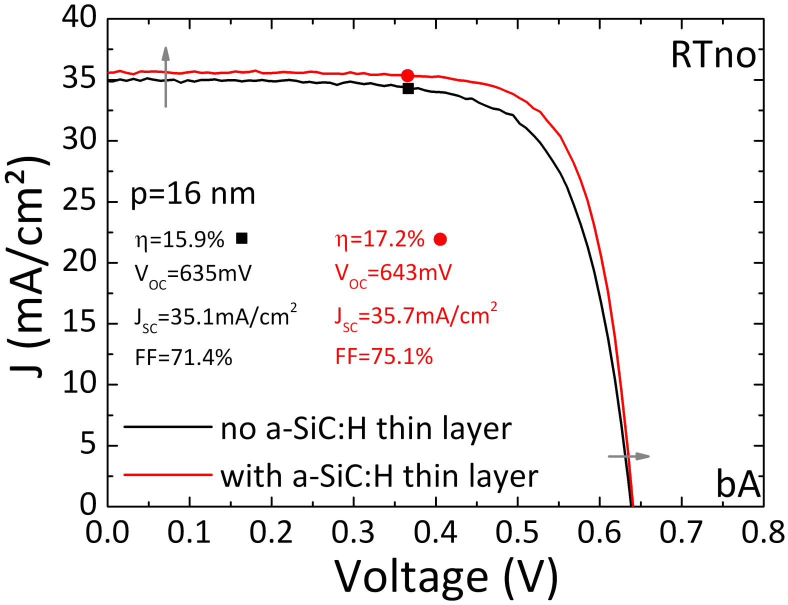

Figure 4-31 – JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on RTno textured c-Si wafers (as-deposited).

Nevertheless, the J_{SC} and FF values remain greater or equal to those of the SHJ solar cell with no a-SiC:H buffer layer at the a-Si:H/c-Si interface on the emitter side. This results in a conversion efficiency of 17.5%, i.e., more than 1 point higher than in a SHJ solar cell with no carbon at the interface. For comparison purposes, the evolution of the JV characteristics upon annealing of both cells is shown in Figure 4-33. All the cell parameters are summarized in Table 4-7. To further understand the impact of carbon at the a-Si:H/c-Si on the performance of SHJ solar cells, JV measurements were performed in the dark. The characteristics obtained are shown in Figure 4-34. As can be seen, just as in the case of KIno substrates, inserting a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface allows for a decrease in the dark current on the whole bias range.

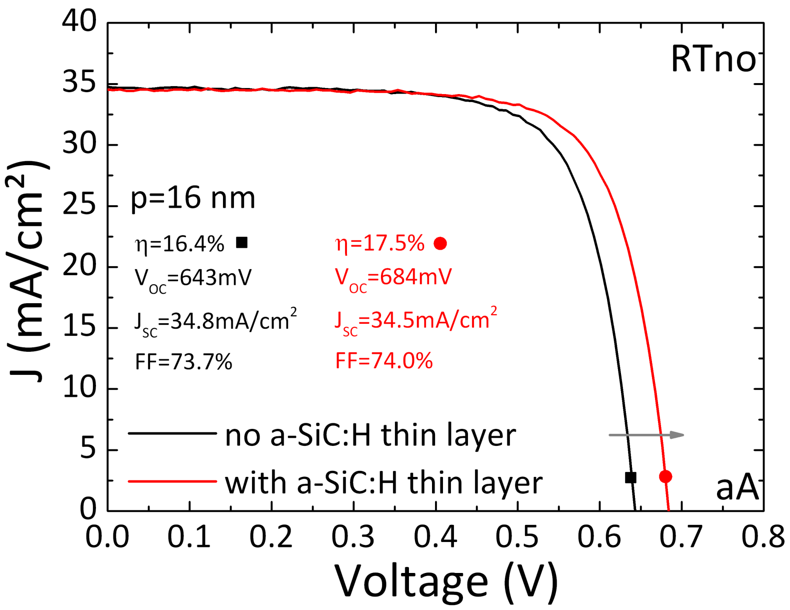

Figure 4-32 – JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on RTno textured c-Si wafers (annealed).

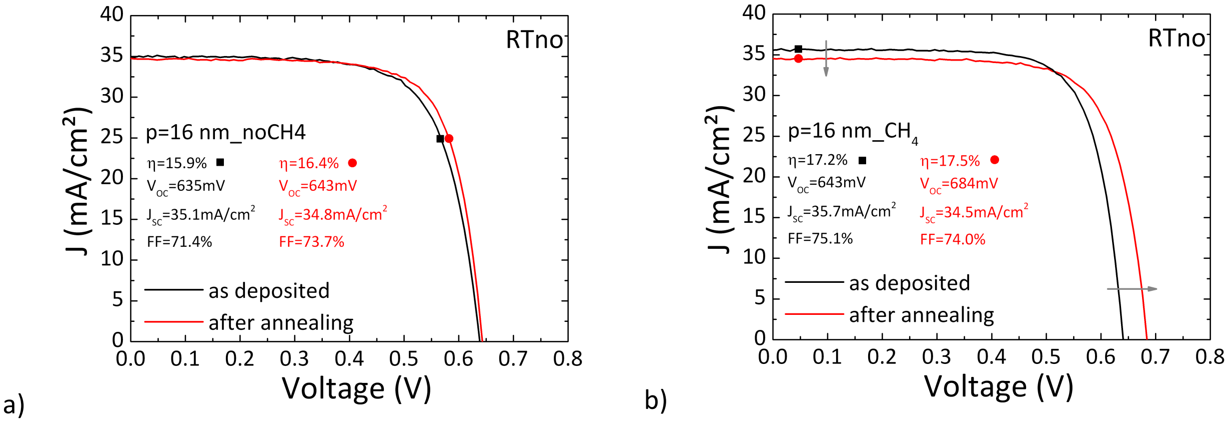

Figure 4-33 – Evolution of the performance upon annealing of SHJ solar cells fabricated a) without and b) with a thin a-SiC:H layer at the a-Si:H/c-Si interface on RTno textured wafers.

RTno cells	state	Eff. [%]	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]	R_{OC} [Ω/cm²]	R_{SC} [Ω/cm²]
noCH$_4$	bA	15.9	635	35.1	71.4	0.402	280
	aA	16.5	643	34.8	73.7	0.370	285
CH$_4$	bA	17.2	643	35.7	75.1	0.321	524
	aA	17.5	684	34.5	74.0	0.276	514

Table 4-7 – Evolution upon thermal annealing of the conversion efficiency of a standard and “improved” SHJ solar cell fabricated with textured RTno c-Si wafers.

The dark saturation current is reduced by almost an order of magnitude. We are dominated by the R_S at high forward bias (0.7 V) and by high recombination currents under the V_{OC}. Despite this fact, it is clear that the enhanced structure enables a steeper slope and thus a lower n and J_0. As can be seen in Figure 4-35, annealing these structures does not change this trend. Having the thin a-SiC:H layer at the a-Si:H/c-Si interface still allows for a lower recombination current. For comparison purposes, the evolution of the samples upon annealing is shown in Figure 4-36a) and b).

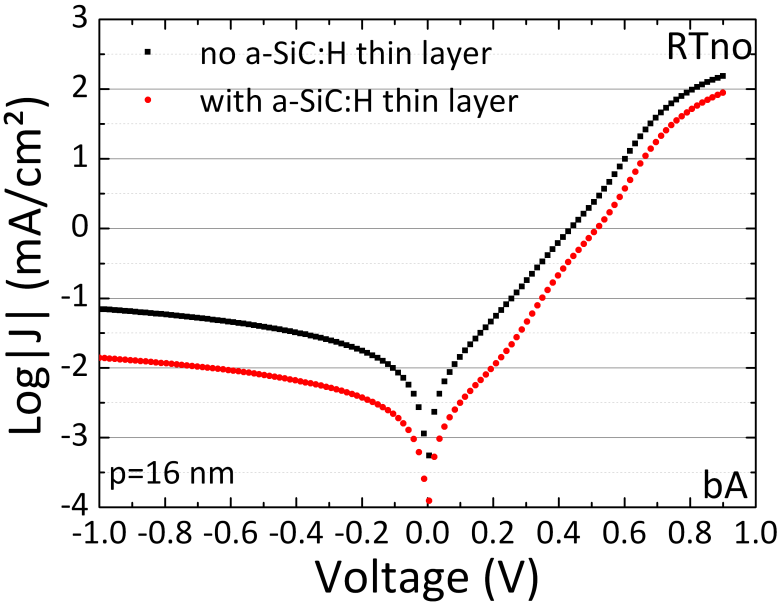

Figure 4-34 – Dark JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on RTno textured c-Si wafers (as-deposited).

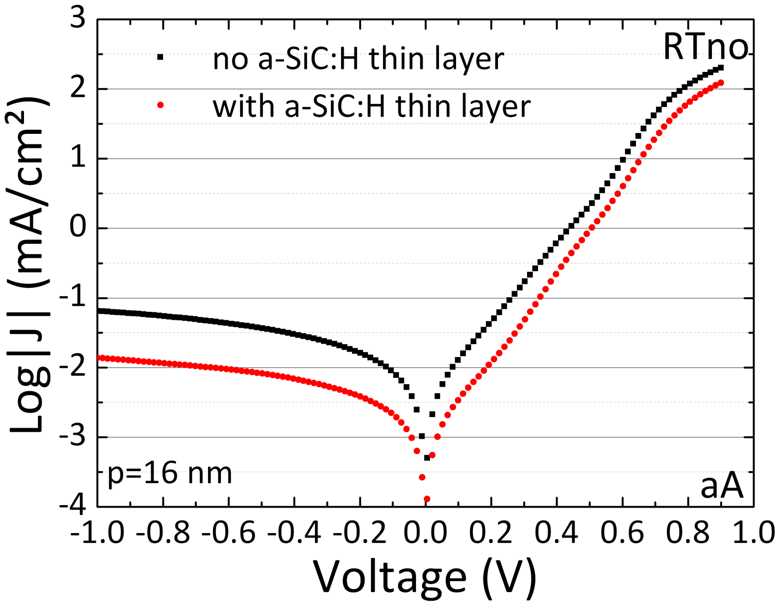

Figure 4-35 – Dark JV characteristics of SHJ solar cells fabricated with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface on RTno textured c-Si wafers (annealed).

As can be seen, unlike the KIno cells previously shown, our standard annealing step does not affect any of the RTno cells. Only close to V_{OC} can we see a reduction of the impact of R_S, which is probably due to an improvement of the Ag/ITO contact.

To summarize, we have seen that implementing a thin a-SiC:H layer at the a-Si:H/c-Si interface on the emitter side of an RTno SHJ solar cell enables to reduce the dark current on the whole bias range. This is a sign that recombination is reduced at the interface. Thanks to this, we experience an increase in the final device V_{OC}, i.e., +41 mV above that of the SHJ cell with no carbon at the interface. This leads to an overall increase of the conversion efficiency by 1.1 point to reach a final yield of 17.5 %. We have shown that just as in the case of the passivation studies carried out in 3.2.2, for two very different types of texturing in terms of pyramid size and chemical process (IPA and IPA-free), the introduction of a thin a-SiC:H layer is beneficial for SHJ solar cell performance. This is mainly due to a strong increase in the V_{OC}, close to 700 mV, induced by a decrease in defect-related recombination at the a-Si:H/c-Si interface. This is confirmed by an overall decrease in the dark current on the whole bias range. Considering these results and those presented in 3.2.2.b, we conclude that only the impediment of local epitaxial growth can lead to such improvements. This is again confirmed by the improvements experienced upon annealing. However, we also witness an improved charge carrier collection, as reflected by a higher FF. This shows that despite the higher resistivity of the interface due to the presence of carbon, it is still more important to ensure that the interface be abrupt to achieve high conversion efficiencies. However, upon finalization of the SHJ solar cells, we noticed a degradation of the passivation taking place upon the ITO sputtering on our samples (see section 4.1.2.b). Moreover, we experienced a difference in the passivation degradation depending on the type of substrate used (flat or textured). In an attempt to understand the underlying mechanisms of such degradation, and in order to increase the final conversion efficiency of our solar cells, we carried out a study of this phenomenon.

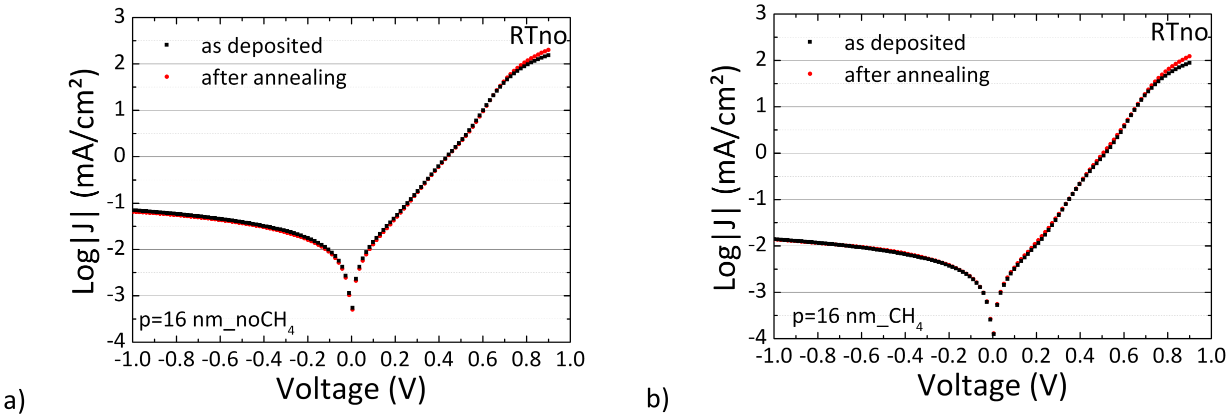

Figure 4-36 – Evolution upon annealing of the dark JV characteristics of SHJ solar cells fabricated a) without and b) with a thin a-SiC:H layer at the a-Si:H/c-Si interface on RTno textured c-Si wafers.

4.2 Degradation of the passivation upon TCO sputtering. Implementation of a p-layer gradient to enhance the conversion efficiency of SHJ solar cells.

4.2.1 Passivation degradation upon ITO sputtering

4.2.1.a Goal of the study

Upon finalization of SHJ solar cells, it is essential to deposit a layer of TCO on both sides of the solar cell precursor. Its role is twofold. On the one hand, contacting directly a-Si:H, even when doped, with the evaporated silver results in a non-ohmic contact. Indeed, the work function of silver (4.26-4.74 eV) is higher than that of n-doped a-Si:H, so that we have $\phi_{Ag}>\phi_{(n+)a\text{-}Si:H}$, resulting in a Schottky barrier. On the other hand, the TCO serves as an antireflective coating. Indeed, despite texturing or nanopatterning, crystalline silicon remains a quite reflective material in some parts of the spectrum. In order to lower this reflectivity and enhance the transmission of light, a thin layer of TCO can be deposited on top of our cell.

Transparent conductive oxides are wide bandgap materials. There are different types of TCOs, such as zinc oxide, tin oxide or indium oxide…, which can be doped with a variety of elements (Al, B, In, Ga, F, Sn), depending on the application. Indium oxide doped with tin or ITO (Indium Tin Oxide) is the most widely known TCO. Indeed, ITO has outstanding optical properties, with a transparency greater than 90% in the visible range. Moreover, as an n-type degenerated semiconductor this material exhibits a very low resistivity, as low as 10^{-4} Ω·cm, with a high electron mobility, close to 50 $cm^2 \cdot V^{-1} \cdot s^{-1}$. These two features allow ITO to serve as a good TCO. It can also be combined with other materials to form stacks. When used with SiO_x for example, one can minimize the ITO layer thickness and thus reduce some of the parasitic absorption due to the important amount of free carriers[241]. For a more thorough review of TCOs, the reader is referred to *C. Charpentier*'s Ph.D. thesis[242].

ITO is usually sputtered by physical vapor deposition (PVD). The process is schematically described in Figure 4-37. The sample is loaded in a vacuum chamber just as in the case of a PECVD deposition process. However this time, it is facing a solid target made of indium, tin and oxygen with a well-defined stoichiometry[34]. When the chamber reaches a pressure ranging from $7 \cdot 10^{-7}$ to $1 \cdot 10^{-6}$ mbar, a mixture of argon and oxygen is introduced inside the chamber. RF power is then used to ignite the plasma between the sample and the target. Unlike PECVD, the power density needs to be quite high since, the ions generated from argon and oxygen atoms must sputter indium, tin and oxygen atoms from the solid target. As a result, the sputtered species impinge the substrate surface, allowing the ITO layer to grow.

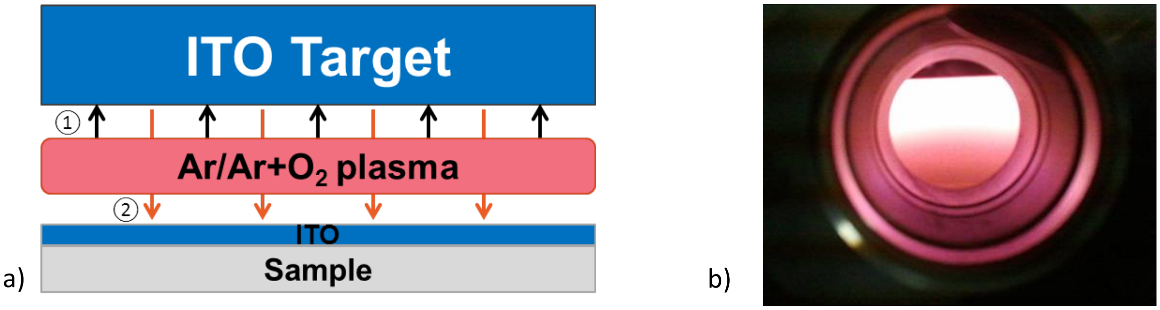

Figure 4-37 – a) Schematical representation of ITO deposition by PVD and b) picture of an argon plasma taken during ITO deposition in a PVD reactor.

As stated above and as shown in 3.1, ITO is vital for finalized SHJ solar cell devices. After finalization of our SHJ solar cells however, metal contacts are evaporated on both sides, making PCD measurements impossible. The effective lifetime is therefore unknown at some point. Nevertheless, while carrying out such measurements right before and after ITO sputtering, we noticed that our solar cell precursors would undergo severe degradation during this process. This caught our attention since very little had been published on this topic thus far. In 1979, *Street et al.*[243] reported how the bombardment of a-Si:H by He^+ ions generated dangling bonds, which acted as recombination centers. Many years later, in 2007, *Lu et al.*[244] observed that ITO deposition by sputtering had a detrimental effect on the front-surface passivation of IBC-SHJ solar cell, while the deposition of MgF_2 by electron beam evaporation did not have the same effect. They explained this degradation by the ion bombardment as originating from the sputtering process and they also noticed that after annealing in air, the effective lifetime could be

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[34] In our case, the In_2O_3 :SnO_2 ratio equaled 9:1.

fully recovered and would even exceed its initial value. In 2011, two Dutch teams from Eindhoven and Delft[245] separated the effects of the ion bombardment and light-induced degradation[246][247] induced by the sputtering plasma process. They observed that the degradation was independent from the ion kinetic energy but rather increased linearly with the ion flux. The same year, in 2011, *Zhang et al.* reported that SHJ solar cell precursors would degrade during ITO sputtering and recover when annealing in air. They also demonstrated that ITO sputtering could be less detrimental when conditions were optimized, namely by reducing the RF power. Finally, *Demaurex et al.*[248] confirmed in 2013 that sputtering degrades the a-Si:H/c-Si interface and that this is due, at least in part, to plasma luminescence, thus explaining the reversibility of this phenomenon by SWE-related mechanisms. However, they noticed irreversible changes in the film microstructure. Moreover, the role of ion bombardment remains unclear when depositing ITO by sputtering. For these reasons, some experiments were conducted on SHJ solar precursors.

Figure 4-38 shows the effective lifetime drop of a SHJ solar cell precursor prepared on a 140 µm-thick, 20 Ω·cm n-doped textured c-Si wafer, before and after ITO sputtering on both sides. The i-layer is 4-nm thick on the BSF side and comprises 2 nm of an a-SiC:H buffer layer, whereas the n-layer is 25-nm thick. On the emitter side, the i-layer is 6-nm thick, comprising 2 nm of an a-SiC:H buffer layer, and is capped by 10 nm of our standard p-layer.

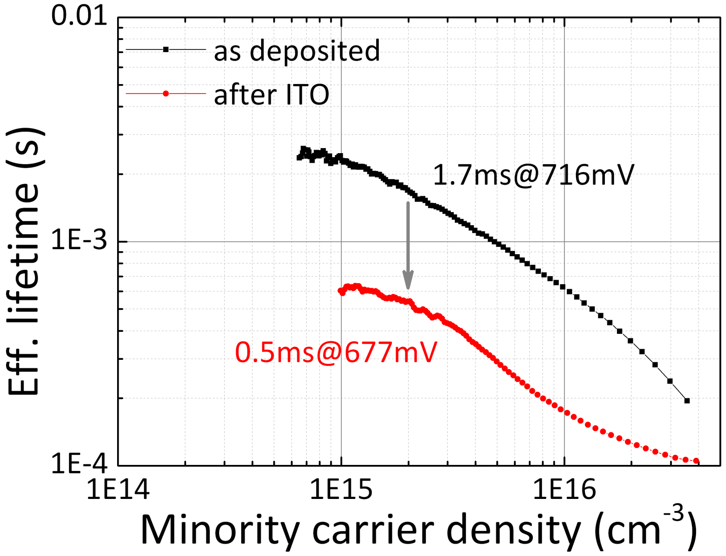

Figure 4-38 – Effective lifetime of a SHJ solar cell precursor before and after sputtering ITO on both of its sides.

As can be seen, ITO deposition on both sides of this solar cell precursor induced a severe degradation of its passivation level, as measured by PCD. Indeed, the effective lifetime drops from 1.7 ms down to 500 µs while the iV_{OC} decreases by almost 40 mV, from 716 mV down to 677 mV. It is worth noting that in the high-injection range, the impact of the ITO sputtering seems stronger. This testifies to an obvious degradation of the a-Si:H/c-Si interface, wherein the defect-assisted recombination mechanisms dominate (SRH component).

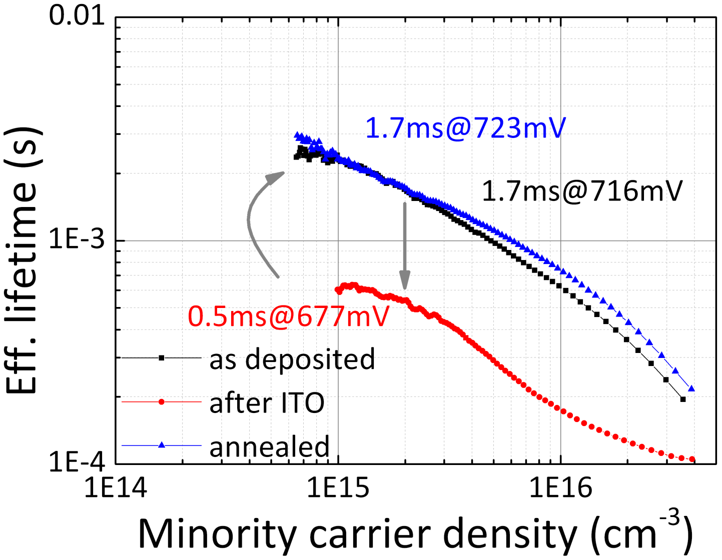

Figure 4-39 – Effective lifetime of a SHJ solar cell precursor before and after sputtering of ITO, and after annealing in air at 180°C.

Although *Zhang et al.* showed that the passivation could be fully recovered only when ITO was sputtered at RT, in our case depositing ITO under our standard conditions, i.e., at 180°C, did not prevent us from fully recovering our passivation level. Figure 4-39 shows the effective lifetime of the latter-mentioned SHJ solar cell precursor before and after ITO sputtering, as well as after annealing in air at 180°C for 30 min. As can be seen, we again measure 1.7 ms of effective lifetime while the iV_{OC} is actually higher, now reaching 723 mV.

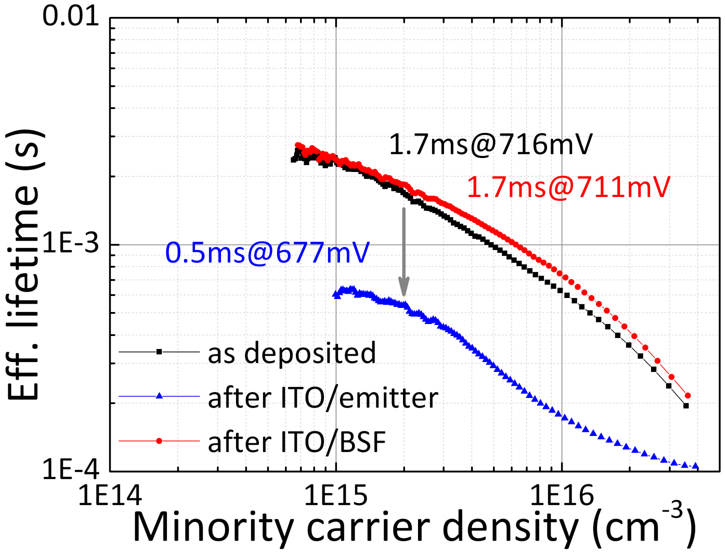

Figure 4-40 – Effective lifetime of a SHJ solar cell precursor before and after sputtering of ITO on both sides.

This is due to the annealing process, which was not calibrated to only recover the initial state of our cell and has provided more thermal energy, thus leading to an actual improvement compared to its as-deposited state. Interestingly enough, when measuring the SHJ solar precursor lifetime at each stage of the ITO deposition, i.e., after sputtering on the BSF and after sputtering on the emitter, we actually noticed that the degradation does not just occur after sputtering on any side, but when depositing on the emitter side where the p-layer is present. Figure 4-40 shows the effective lifetime of the latter-mentioned SHJ solar cell precursor at each stage of the ITO deposition. Sputtering ITO under our standard conditions on the BSF side leads to only a slight change in iV_{OC} (-5 mV) but to no change in the effective lifetime. Contrariwise, sputtering on the emitter side leads to the general degradation observed earlier. Since the 'ip' stack on the p-side was much thinner than the 'in' stack on the n-side, we decided to study the impact of the i- and p-layer thicknesses (on the emitter side) on the passivation degradation.

4.2.1.b Impact of the amorphous layer thicknesses on the passivation degradation

To study the impact of the i- and p-layer thicknesses (on the emitter side) on the passivation degradation, SHJ solar cells with varying p-layer thicknesses were fabricated following the recipes presented in Table 4-8.

SiH_4 [sccm]	CH_4 [sccm]	PH_3 or TMB [sccm]	Pressure [mTorr]	Power [W]	Thickness [nm]
BSF					
25	50	0	40	1	1.5
50	0	0	50	1	3.5
50	0	1	60	1	25
Emitter					
25	50	0	40	1	1.5
50	0	0	50	1	3.5
50	0	20	105 (Ar dilution)	2	variable

Table 4-8 – Deposition conditions for the BSF and emitter sides of KIno and RTno textured SHJ solar cells.

As can be seen, the BSF side was kept constant, whereas only the p-layer thickness varied. The ITO sputtering time was kept at 180 seconds, according to the standard recipe for textured SHJ solar cell finalization. Figure 4-41a) shows the evolution of the effective lifetime of SHJ solar cells fabricated using KIno textured wafers as a function of the p-layer thickness. As can be seen, the effective lifetime remains constant up to a thickness of 13 nm. After that, the effective lifetime drops below 600 µs. However, it increases slightly for a thickness of 19 nm. The iV_{OC} on the other hand, exhibits a clear decrease from the highest value above 690 mV, even though it seems to start increasing again at 19 nm. In part b) of Figure 4-41 is shown the variation of the effective lifetime (in % relatively to the initial value) and of the iV_{OC} (in mV relatively to the initial value) upon ITO sputtering on both sides of the SHJ solar cell precursors. As can be seen, there is no clear relationship between the thickness of the p-layer and the level of degradation of the SHJ solar cell precursors. Indeed, whereas the effective lifetime drop remains close to -40% in most cases (apart from the 16 nm-sample which degrades by 70%), the drop in iV_{OC} remains quite constant, between -25 and -30 mV. It is worth noting that all samples exhibit quite similar initial effective lifetimes. From the two graphs presented in Figure 4-41, we conclude that the effective lifetime drop does not depend on the thickness of the p-layer. This raises the question of a possible impact of the doping, inasmuch as for a p-layer thickness of 19 nm we are quite close to the (i)a-Si:H/(n)a-Si:H stacks in terms of thickness. The lack of degradation on the BSF side would then be due to the type of dopant rather than to its thickness.

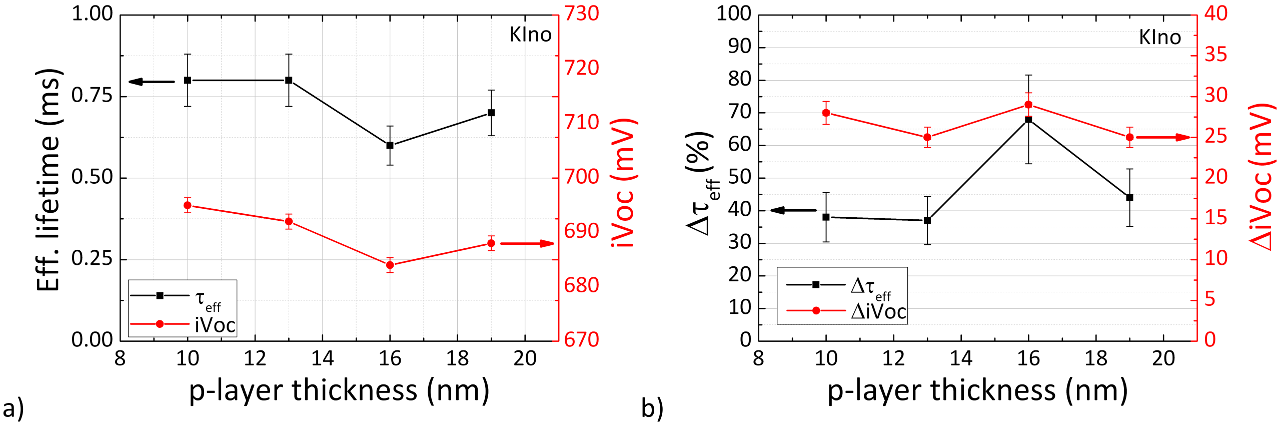

Figure 4-41 – a) Impact of the p-layer thickness on the effective lifetime and iV_{OC} of SHJ solar cell precursors fabricated on KIno wafers and b) evolution of the effective lifetime and iV_{OC} degradation upon ITO sputtering as a function of the p-layer thickness.

In order to confirm the previous results, the same experiments were conducted on RTno wafers. Figure 4-42 shows the evolution of the effective lifetime of SHJ solar cells fabricated using RTno textured wafers as a function of the p-layer thickness. As can be seen, the effective lifetime increases with the thickness of the p-layer. This is due to a stronger field-effect that increases up to a value of 16 nm. However, after this, the effective lifetime starts decreasing slightly, testifying to a possible detrimental impact of the boron-doped layer. Again, the iV_{OC} does not follow the exact same trend as the effective lifetime. Indeed, as can be seen, the highest value is reached for a thickness of 13 nm. After this, the iV_{OC} starts decreasing and stabilizes at a value of 710 mV just as in the case of τ_{eff}. In Figure 4-42b) is shown the evolution of the variation of the effective lifetime (in % relatively to the initial value) and of the implied V_{OC} ΔiV_{OC} (in mV relatively to the initial value) upon ITO sputtering on both sides of the SHJ solar cell precursors.

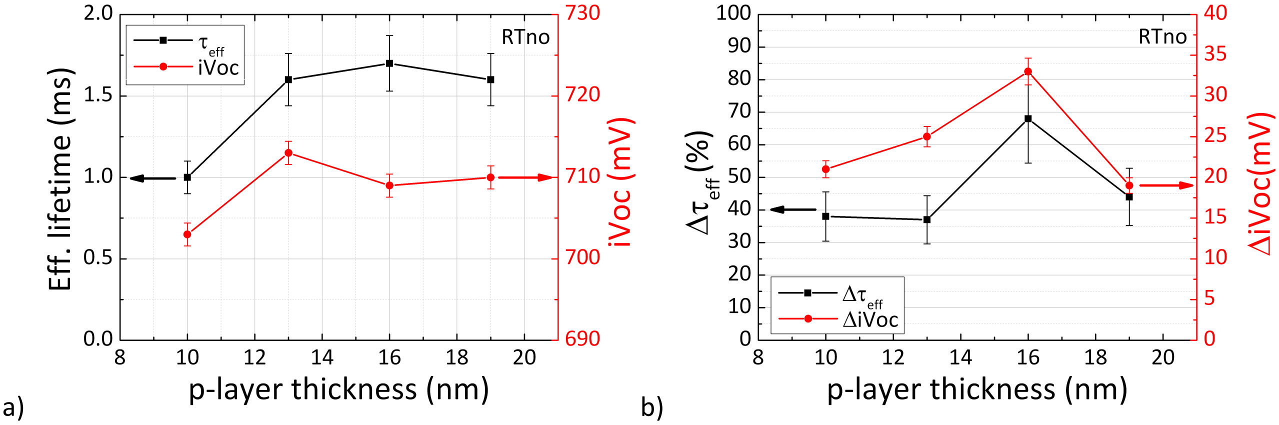

Figure 4-42 – a) Impact of the p-layer thickness on the effective lifetime and iV_{OC} of SHJ solar cell precursors fabricated on RTno wafers and b) evolution of the effective lifetime and iV_{OC} degradation upon ITO sputtering as a function of the p-layer thickness.

As can be seen, there is no evidence that a thicker p-layer prevents SHJ solar cell precursors from being degraded, thereby confirming the results found on the KIno wafers. Indeed, $\Delta\tau_{eff}$ varies in a quite trendless fashion, reaching values as low as 40% for the thinnest p-layer, whereas the largest degradation occurs when the p-layer thickness equals 16 nm. This time, ΔiV_{OC} follows the variation of $\Delta\tau_{eff}$. Indeed, the largest drop in iV_{OC} is reached for a p-layer thickness of 16 nm, with a -33 mV loss.

Moreover, this drop is almost identical as concerns the thinnest p-layer (10nm), i.e., -15 mV, and the thickest one (19 nm). This confirms that the thickness of the p-layer was not responsible for the significant degradation difference when sputtering ITO on the BSF or on the emitter side shown in Figure 4-40. Indeed, it seems that the p-layer is “transparent” to the sputtering-induced damages. For comparison purposes, Figure 4-43 shows the evolution of the effective lifetime of two KIno cells upon a standard ITO sputtering: the first one has a 10 nm-thick p-layer (part a)) and the other one has a 16 nm-thick layer (part b)). As can be seen, despite the 6 nm difference, the passivation drops on ITO sputtering are quite similar in terms of effective lifetime. Indeed, with a quasi-identical initial 0.7-0.8 ms, they both degrade down to the same 0.1 ms value.

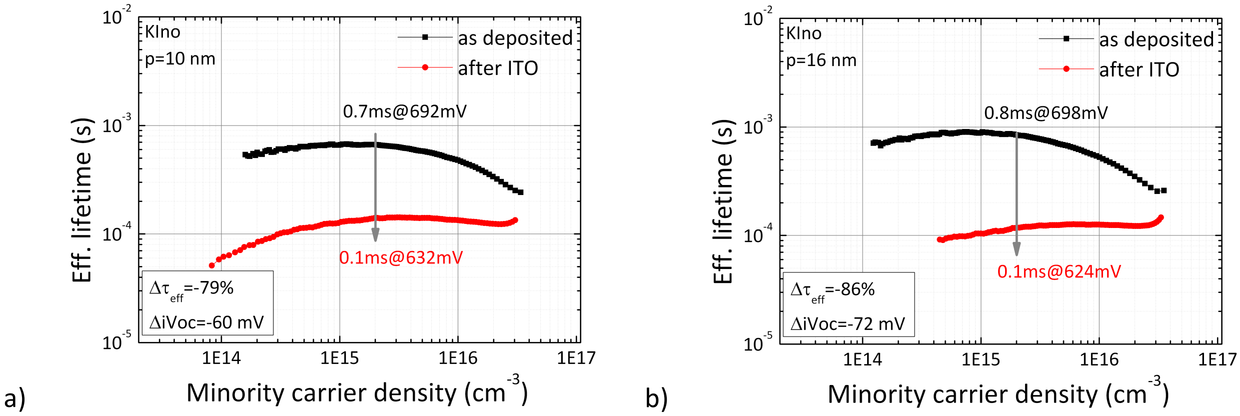

Figure 4-43 – Evolution of the effective lifetime of KIno SHJ solar cell precursors upon ITO deposition for a p-layer thickness of a) 10 nm and b) 16 nm.

This degradation is evidenced throughout the whole injection range, showing that: i) the a-Si:H/c-Si interface is more defective (high-injection range) and ii) the field-effect is weakened by ITO deposition (low-injection range). Despite the higher initial passivation level of RTno counterparts, the same trends could be observed as shown in Figure 4-44. Moreover, these could be obtained on various kinds of samples (flat (100) and (111), various pyramid sizes and wafer doping) and p-layer thicknesses, testifying to a weak correlation between the texturation or the p-layer thickness and the degradation level.

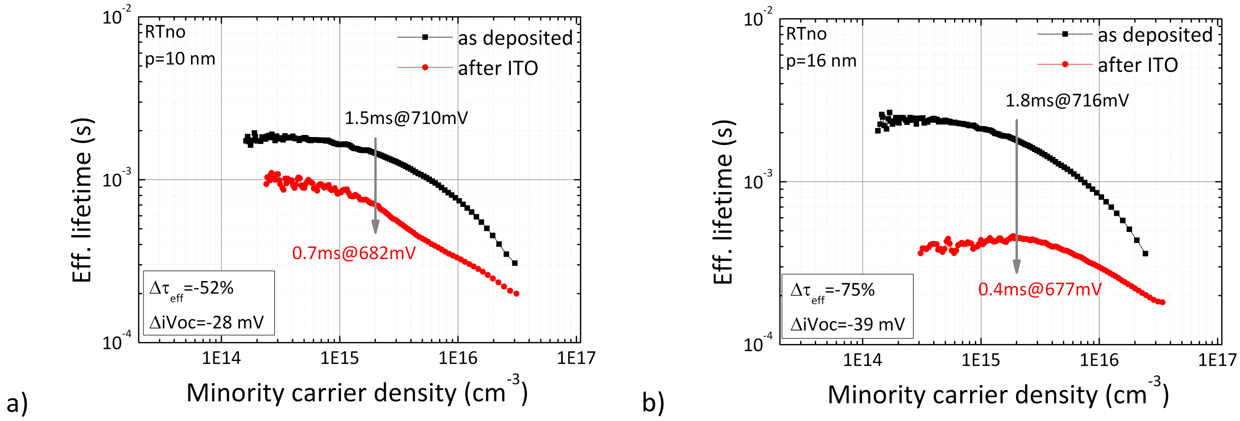

Figure 4-44 – Evolution of the effective lifetime of RTno SHJ solar cell precursors upon ITO deposition for a p-layer thickness of a) 10 nm and b) 16 nm.

In order to gain a deeper understanding of the phenomenon under study, four SHJ solar cells with varying i-layer thicknesses on the emitter side ranging 5-50 nm were fabricated on flat (111) n-type wafers. All other parameters were kept constant: the BSF side was identical for all the samples while a 10-nm thickness was chosen for the (p++)a-Si:H layer. The deposition conditions are shown in Table 4-9.

SiH_4 [sccm]	CH_4 [sccm]	PH_3 or TMB [sccm]	Pressure [mTorr]	Power [W]	Thickness [nm]
BSF					
50	0	0	50	1	5
50	0	1	60	1	25
Emitter					
50	0	0	50	1	5 - 50
50	0	20	105 (Ar dilution)	2	10

Table 4-9 – Deposition conditions for the BSF and emitter sides of (111) flat SHJ solar cells.

A standard 82-nm thick layer of ITO was sputtered on both sides of the samples and the effective lifetime and iV_{OC}s were extracted from PCD measurements at each stage of the fabrication process. Figure 4-45 shows the drop in effective lifetime (%) and in iV_{OC} (mV) as a function of the i-layer thickness. A clear trend can be observed and we can see that the passivation degradation is highly dependent on the thickness of the intrinsic buffer layer. Indeed, when doubling the p-layer thickness would not bring any substantial change in ΔiV_{OC}, switching (i)a-Si:H from 5 to 10 nm induces a reduction in the iV_{OC} drop almost twofold, i.e., from -22 mV down to -12 mV.

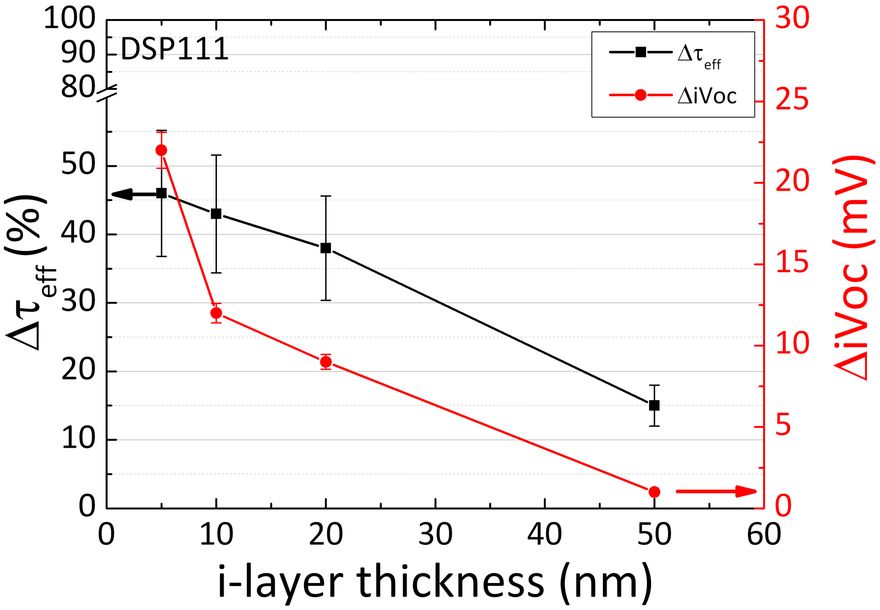

Figure 4-45 – Evolution of the effective lifetime and iV_{OC} degradation as a function of the i-layer thickness in (111) SHJ solar cell precursors.

From the above we conclude that by using a thicker i-layer, the interface is shielded against damages induced by the sputtering process. Since a thicker p-layer could not provide the same protection, one must seek an explanation related to the doping of a-Si:H. Considering the damages induced by the ion bombardment, one explanation for the results presented above could lie in the hydrogen diffusion coefficient differences within the bulk of the intrinsic and doped a-Si:H layers. Indeed, the Ar^+ ions do not penetrate more than a few Angstroms within the a-Si:H subsurface (2-3 Å). Therefore, they cannot be directly responsible for the degradation at the a-Si:H/c-Si interface 20-30 nm below. However, they impinge upon the sample surface with an energy close to 100 eV. This energy can therefore be released within the a-Si:H network, possibly inducing the breaking of weakly bonded Si-Si pairs but also of Si-H bonds. As a result, hydrogen atoms could move towards the interface with a diffusion coefficient, which happens to be determined by their doping environment. Indeed, hydrogen atoms have one electron orbiting around their core. If they find themselves in the presence of donor-like dopants (such as phosphine), they will tend to keep their electron since the a-Si:H network is already negatively charged. As a result, all diffusion mechanisms will be determined by the ability a hydrogen atom accompanied by its electron to move within the a-Si:H network. Contrariwise, if hydrogen atoms find themselves in the presence of acceptor-like dopants (such as boron), they will tend to lose their single charge since the a-Si:H network is positively charged. Therefore, diffusion will be made much easier since the hydrogen atoms can freely move within the a-Si:H network without its electronic surrounding, as a proton. Despite the apparently small "size" difference, this results in a significant increase in the hydrogen diffusion coefficient, i.e., by a factor close to 100 actually[249]. As a result, hydrogen atoms can diffuse through the (p)a-Si:H layer quite easily and penetrate inside the thin (i)a-Si:H layer. Once present, they could induce the breaking of weak Si-Si bonds. They could even foster the breaking of Si-H bonds when weakened by Fermi-level related mechanisms, as we will see later. This could explain why increasing the p-layer thickness does not provide any kind of protection for the a-Si:H/c-Si interface. Indeed, it has been reported that the diffusion coefficient of hydrogen in intrinsic and n-doped a-Si:H are quite close[250]. Therefore, the (n)a-Si:H layer is able to shield the thin a-Si:H layer underneath which, as can be seen in Figure 4-45, could not provide a sufficient protection for the a-Si:H/c-Si interface on the emitter side. In an attempt to understand why the BSF side would not degrade when implemented in a SHJ solar cell structure, in/in symmetrical stacks were fabricated using the standard conditions and thicknesses used in solar cell precursors. A standard ITO layer was deposited on both sides. Then, the sample was dipped for 10 seconds in 5%-dilute HF to remove the ITO. Afterwards, the sample was annealed under our standard forming gas conditions at 180°C for 30 minutes. At each step, the effective lifetime and iV_{OC} were measured by PCD. Results for each step are shown in Figure 4-46. As can be seen, contrary to SHJ solar cells, the initial effective lifetime is much larger. Indeed, instead of the usual 1-2 ms and 700 mV, the effective lifetime reaches the very high value of 17.3 ms with an iV_{OC} of 735 mV. Sputtering ITO on one side induces a degradation of the passivation such that the effective lifetime drops to 5.9 ms and the iV_{OC} to 728 mV. This represents a drop of $\Delta\tau_{eff}$=-66% and ΔiV_{OC}=-7 mV. Logically, depositing on the second side does not impact the level of passivation. Indeed, we are measuring τ_{eff}, which will always be limited by the poorest interface between the front and the back. The lifetime drops to 4.4 ms and the iV_{OC} barely changes by 1 mV, down to 727 mV. The HF dip removes the ITO completely without removing the damages induced by the sputtering process. The lifetime remains constant with a value of 4.3 ms whereas the iV_{OC} drops down to 716 mV. This can be understood in terms of field-effect, since ITO is an n-type degenerated semiconductor with a wide bandgap. Because of this, the separation of charges of opposite signs at the a-Si:H/c-Si interface is enhanced and recombination mechanisms are reduced. Removing this layer results in a loss of this effect. Moreover, the lack of improvement upon ITO removal shows that the material in itself is not responsible for any loss in passivation, thereby confirming the sputtering process as being responsible for the passivation degradation.

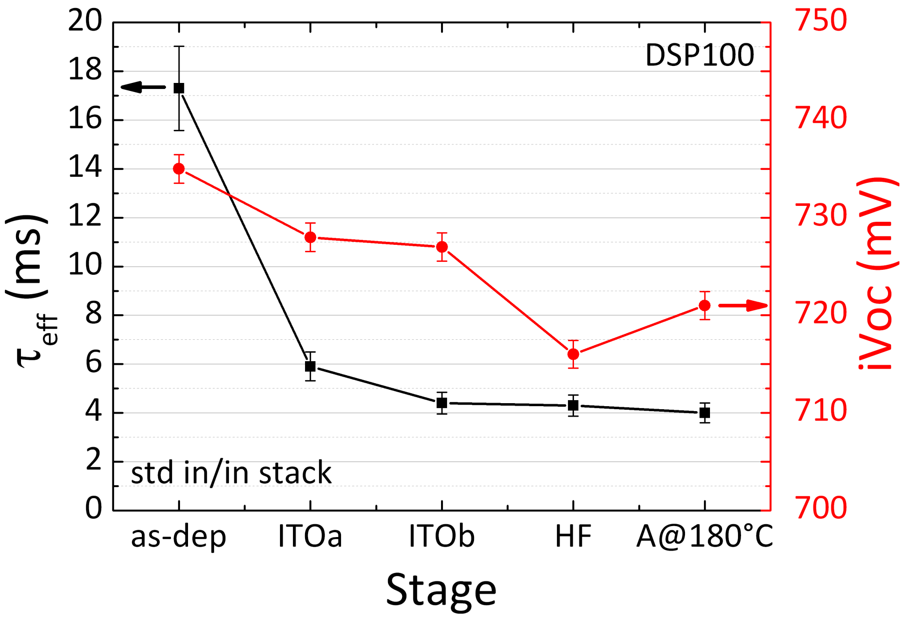

Figure 4-46 – Evolution of the effective lifetime and iV_{OC} of a symmetrical in/in stack deposited on flat (100) c-Si wafer upon bilateral ITO deposition, removal thereof, and annealing.

Finally, annealing the degraded sample does not lead to any increase in effective lifetime and only to a small increase in iV_{OC}. From these results we conclude that:

i) despite the apparent lack of degradation on SHJ solar cell precursors, BSF do degrade when submitted to sputtering processes, just as emitters do,

ii) the recovery that we witness upon the annealing of SHJ solar cell precursors is due to the improvements on the emitter side since the BSF side seems to remain unchanged in terms of passivation.

However, despite the significant losses in passivation experienced on in/in stacks, the effective lifetime, as well as the iV_{OC}, remain quite high in comparison with the values measured on SHJ solar cell precursors. Indeed, on the in/in stack presented above, the final effective lifetime stays above 4 ms whereas the iV_{OC} remains at the high value of 721 mV. Under such conditions, it is impossible to witness the passivation changes on the BSF side when measuring the evolution of a SHJ solar cell precursor submitted to sputtering processes by PCD. Indeed, their usual lifetimes and iV_{OC}s are found to lie between 0.6-2 ms and 650-700 mV. Therefore, the changes presented in Figure 4-40 can be misleading. In short, 'no change' on the BSF side does not necessarily mean 'no degradation'. There is a significant degradation actually, in terms of effective lifetime especially, but since we are limited by the emitter side we simply cannot see it on PCD measurements. However, the resulting passivation level is by no means as low as when sputtering on the emitter side. The reasons why passivation degradation upon ITO sputtering is so detrimental on the p-side remain unclear and this topic would require further studies. However, it seems that the nature of the p-layer is responsible for the significant lifetime drop. This could be related or at least be fostered by the poorer passivating properties of the p-layer. Indeed, we saw in 3.2.2.a that depositing 5 nm of (i)a-Si:H on a flat DSP (n)c-Si wafer provides for a high passivation level with an effective lifetime usually ranging 3-5 ms. Capping this (i)a-Si:H layer with 25 nm of our (n+)a-Si:H under our standard conditions yields effective lifetimes above 10-17 ms. Contrariwise, capping with our standard (p)a-Si:H layer yields effective lifetimes in the 1-2 ms range. It is well-known that (p)a-Si:H layers are more defective than their intrinsic and n-doped counterparts[251]. However, the higher defect density within the p-layer bulk does not provide an explanation for the passivation degradation when capping an intrinsic layer with good passivating properties. Indeed, *De Wolf and Kondo* suggested that not only is the p-layer more defective but also that this very layer induces the formation of defects within the intrinsic layer lying underneath[73][252]. This can be understood by first considering a (p)a-Si:H/(i)a-Si:H/(n)c-Si stack and its resulting band diagram structure. Figure 4-47 shows such a band diagram generated with AFORS-HET using classical properties for all materials, as described in [253]. The doping of the p-layer was chosen such that its activation energy E_A would reach the realistic value of 0.34 eV. Moreover, our structure results in the formation of an inversion layer which exhibits an activation energy of 0.11 eV, i.e., close to standard values[118]. As expected, the band bending occurs mainly within the crystalline silicon. Then, due to the different bandgaps, a band offset arises at the a-Si:H/c-Si interface, followed by the intrinsic and p-doped a-Si:H layers. At equilibrium, the Fermi levels of all materials must align. Due to the difference in the electronic affinities of the (p)a-Si:H and (n)c-Si materials, the band bending induces the Fermi level to cross the (i)a-Si:H buffer layer not at midgap as in the case of any intrinsic material, but close to the valence band.

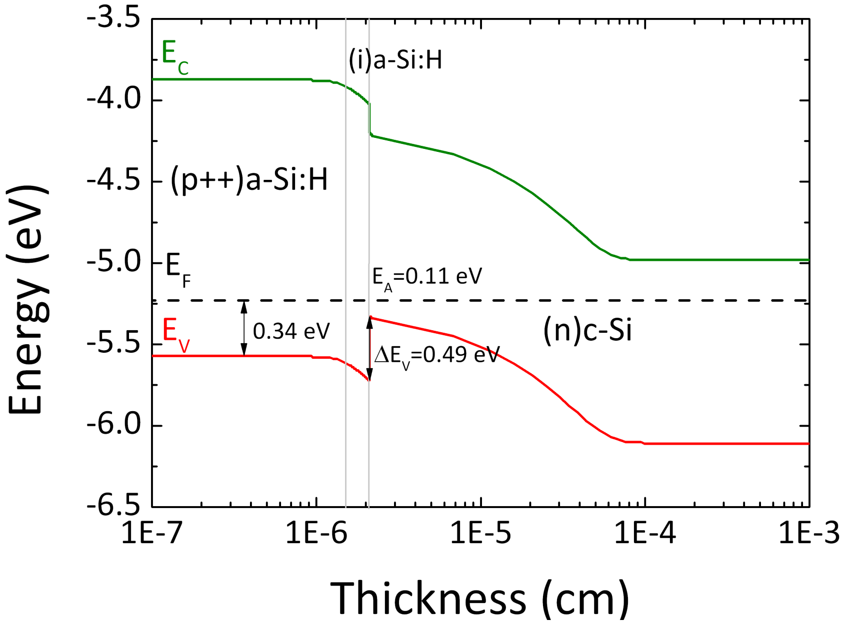

Figure 4-47 – Energy band diagram of an (n+)c-Si/(i)a-Si:H(p++)a-Si:H heterojunction simulated using AFORS-HET.

It has been shown by *Beyer* [254] and *Beyer et al.*[255][256] that the rupture of Si-H bonds and the resulting defect formation depends on the Fermi level position rather than on the physical nature of the dopant. Figure 4-48 shows the activation energy of hydrogen diffusion E_H in a-Si:H (blue dots) and the defect formation enthalpy ΔH (red lines) as a function of the Fermi level shift from midgap. These data have been collected by *Beyer et al.*[257] and *Zunger*[258], respectively. By looking at this schematic but quite explanatory figure, one can see that shifting the Fermi level left or right will not induce the same amount of defects within the a-Si:H bulk. Indeed, by moving it closer to the conduction band minimum or CBM (towards the right-hand side), the diffusion of hydrogen is only slightly enhanced by a small decrease of E_H.

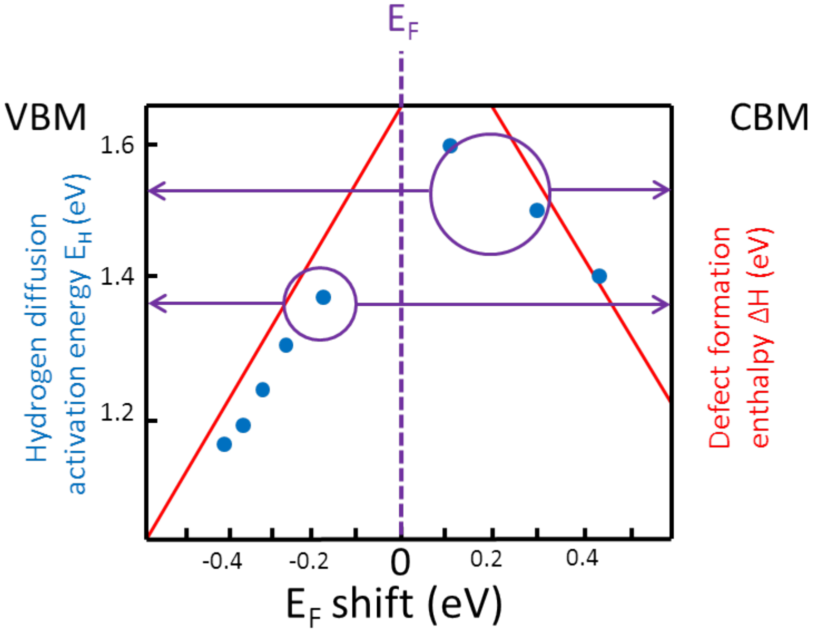

Figure 4-48 – Hydrogen diffusion activation energy in a-Si:H (blue dots) as a function of the E_F position with regard to midgap (data taken from [257]) and dependence of the defect formation enthalpy on the position of E_F (red straight lines) (adapted from [258]).

Likewise, the defect formation enthalpy still remains quite high, i.e., close to 1.4 eV for a 0.4 eV shift from midgap. On the other hand, by shifting E_F from midgap towards the valence band maximum or VBM (towards the left-hand side), the diffusion of hydrogen is greatly enhanced by a significant drop in E_H. This is accompanied by a decrease in the defect formation enthalpy, down below 1.2 eV for a 0.4 eV shift from midgap. This explains why doping a-Si:H with boron results in a more defective material, but also why an intrinsic a-Si:H layer underneath would be more defectful than when not capped with a p-layer. Indeed, upon deposition of the p-doped a-Si:H layer over the intrinsic layer by PECVD (at 180-200°C), hydrogen diffusion must have been enhanced resulting in hydrogen effusion from the (i)a-Si:H layer and, thus, from the a-Si:H/c-Si interface. As a consequence, we obtain a poorer a-Si:H/c-Si interface on the emitter side. When generating the same band diagram as shown in Figure 4-47 for various i-layer thicknesses ranging from 50 down to 5 nm, one can see that the thinner the i-layer the closer E_F will be to the VBM. Figure 4-49a) shows the evolution of the band diagram of a (p++)a-Si:H/(i)a-Si:H/(n)c-Si stack as a function of the i-layer thickness. Part b) of Figure 4-49 shows the evolution of max(E_F-E_V) (taken from within the amorphous layers) and of E_A (measured at the spike of the inversion layer) as a function of the i-layer thickness. As can be seen, the 5 nm intrinsic layer exhibits the smallest E_F-E_V difference, i.e., 0.5 eV from the VBM. This represents a shift of 0.35 eV from the midgap position (for a typical a-Si:H energy bandgap value of 1.7 eV). When considering Figure 4-48 together with the results of the simulation shown in Figure 4-49, one can easily understand that a 5-nm thick (i)a-Si:H layer, when covered with a device-grade (p++)a-Si:H layer, is subject to E_F-induced degradation. This could also explain why sputtering ITO on the emitter side results in a greater degradation than on the BSF side.

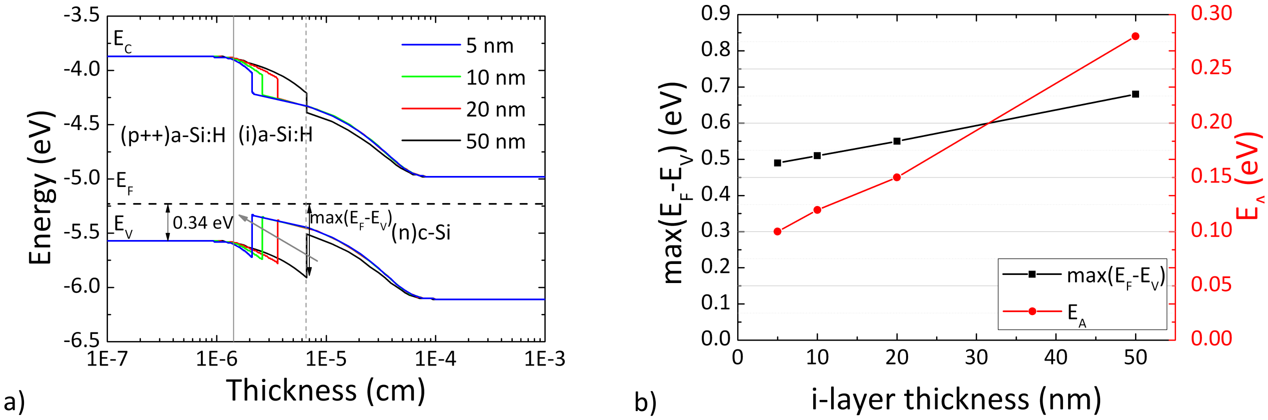

Figure 4-49 – a) Evolution of the energy band diagram of an (n+)c-Si/(i)a-Si:H(p++)a-Si:H heterojunction as a function of the i-layer thickness simulated using AFORS-HET; b) evolution of $max(E_F-E_V)$ and E_A as a function of the i-layer thickness.

However, even if a 50 nm-thick i-layer results in a shift of E_F of only 0.15 eV and in an almost negligible degradation upon ITO sputtering, it is not a viable solution because of the collection issues that start becoming significant (increase of R_S and decrease of FF) beyond 5-10 nm[259]. Therefore, a solution would consist in trying to push E_F farther away from the VBM. This is tricky however, since a lower doping density would induce poorer diode properties and thus poorer solar cell performance. Nevertheless, it was suggested in *J. Damon-Lacoste*'s[11] (p.116) and *M. Labrune*'s[12] (p.106) respective Ph.D. theses that a doping gradient would possibly help overcome this issue. Instead of putting the intrinsic a-Si:H layer directly in contact with our standard heavily doped p-layer, one could imagine depositing a thin transition (p)a-Si:H layer, which would exhibit a much lower doping (and thus conductivity). Its activation energy would be much higher than that of our standard p-layer and therefore, at equilibrium, E_F would cross the (i)a-Si:H farther away from the VBM. As a result, we could expect a less detrimental impact of the p-layer on the overall passivation process. Moreover, by introducing such a gradient, the impact of ITO sputtering might be reduced by a lower concentration of positive charges at the (p)a-Si:H/(i)a-Si:H interface, thus acting as a barrier for hydrogen atoms trying to reach the intrinsic layer. The implementation of such a p-doping gradient and the study of the impact thereof on passivation and on finalized SHJ solar cells will be the heart of next section.

4.2.2 Implementation of a p-layer gradient to lower recombination on the emitter side

In order to simulate the impact of a p-doping gradient on the relative position of E_F with regard to the CBM within the (i)a-Si:H layer, let us consider the (p++)a-Si:H/(i)a-Si:H/(n)c-Si stack previously generated with AFORS-HET. To model our slightly and heavily p-doped a-Si:H layers, we chose to vary the net density N_A of acceptors and monitor the impact of such on the position of E_F therein. As a result, we obtained p-layers with different activation energies: 0.50 eV for the (p)a-Si:H layer and 0.34 eV for the (p++)a-Si:H layer. Figure 4-50a) shows the band diagram of our stack containing a device-grade p-layer solely, whereas Figure 4-50b) shows the band diagram of a (p++)a-Si:H/(p)a-Si:H/(i)a-Si:H/(n)c-Si stack. The thickness of the transition (p)a-Si:H layer was chosen to be 1.5 nm-thick, as in the case of our SHJ solar cell samples.

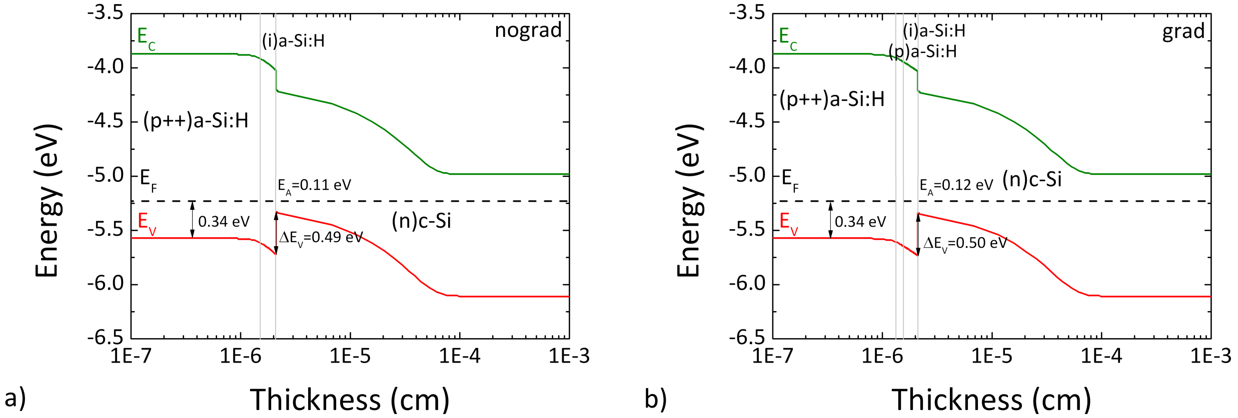

Figure 4-50 – a) Energy band diagram of an (n+)c-Si/(i)a-Si:H(p++)a-Si:H heterojunction and b) Energy band diagram of the same heterostructure with a low-doped (p)a-Si:H transition layer at the (i)a-Si:H/(p++)a-Si:H interface. Both diagrams were simulated using AFORS-HET.

At first glance, both band diagrams look quite similar. Figure 4-51 shows a magnification of the superimposition of Figure 4-50a) and b) in the transition region. As can be seen, the valence bands overlap quite nicely over the whole thickness range however, a shift of the VBM is clearly evidenced in the (i)a-Si:H layer between the inversion layer and the heavily-doped (p++)a-Si:H layer.

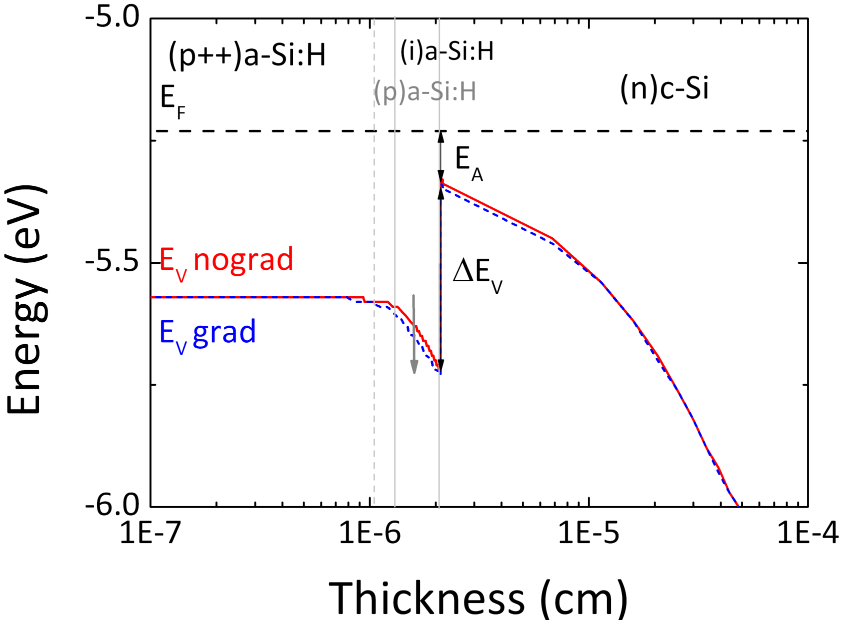

Figure 4-51 – Magnification of the valence band at the a-Si:H/c-Si interfaces presented in Figure 4-50a) and Figure 4-50b).

Indeed, even if quite small, in this very region and throughout the entire thickness of the (i)a-Si:H layer, this shift illustrates well the benefits we could obtain by implementing a p-layer gradient. If we could experimentally reproduce this effect even slightly, this could result in lower E_F-induced defect generation by the defectful, though essential, device-grade (p++)a-Si:H capping layer. This way, recombination would be reduced at the (i)a-Si:H/(p)a-Si:H and the a-Si:H/c-Si interfaces. This could theoretically lead to a V_{OC} increase and to an enhanced carrier collection, as reflected by an increase of the J_{SC} and FF.

4.2.2.a Impact of a p-layer gradient on passivation

If the p-layer gradient helps in reducing the interface defect density by keeping the defect formation enthalpy high within the (i)a-Si:H layer, we should witness an increase of the effective lifetime of SHJ solar cell precursors. For this, we fabricated a series of samples on flat (111) and RTno and KIno textured c-Si wafers, using alternatively a standard ip stack and a p-doping gradient as an emitter. This was done for an overall p-layer thickness of 10 and 16 nm. The low-doping transition layer was kept at a thickness of 1.5 nm and its conductivity was measured to be 9.6E-06 $\Omega^{-1}\cdot cm^{-1}$ at 25°C, i.e., approximately one order of magnitude lower than that of our device-grade (p++)a-Si:H layer. The deposition conditions of the BSF and graded emitters are shown in Table 4-10. As can be seen, the BSF side was kept constant. The (p)a-Si:H layer was deposited using 5 sccm of TMB instead of the 20 sccm we use for the standard (p++)a-Si:H layer. For standard emitters, the usual recipe was used (20 sccm) throughout the whole p-layer deposition process to reach a thickness of 10 or 16 nm.

SiH_4 [sccm]	TMB [sccm]	Pressure [mTorr]	Power [W]	Thickness [nm]
BSF				
50	0	50	1	5
50	1	60	1	25
Emitter (p-gradient)				
50	0	50	1	5
50	5	105 (Ar dilution)	1	1.5
50	20	105 (Ar dilution)	2	8.5 or 14.5

Table 4-10 – Deposition conditions of the BSF and graded emitter for the fabrication of SHJ solar cells.

Figure 4-52 shows the effective lifetime of two SHJ solar cell precursors fabricated out of flat (111) c-Si wafers. One cell has a standard, 16 nm-thick (p++)a-Si:H layer whereas the second cell has a p-layer gradient such that the (p)a-Si:H and (p++)a-Si:H layer thicknesses are 1.5 and 14.5 nm, respectively. As can be seen, the implementation of a p-layer gradient on the emitter side allows for a significant increase in the effective lifetime of the SHJ solar cell precursor. Indeed, starting at 1.0 ms and 687 mV, we now reach 1.7 ms and an iV_{OC} of 705 mV. This is made possible due to passivation improvement over the whole injection range. This seems to indicate that the intrinsic buffer layer underwent weaker degradation thanks to the larger activation energy of the transition (p)a-Si:H layer. In order to confirm these results, PCD measurements were carried out on the different SHJ solar cells fabricated for this study. Table 4-11 sums up the τ_{eff} and iV_{OC} values for these cells. Overall, the implementation of a p-doping gradient is beneficial. This is true especially in the case of flat (111) SHJ solar cells, where the gradient allows for a frank increase in the iV_{OC} with a gain of +6 to 18 mV. In the case of textured wafers, most of our samples exhibit an increase in the effective lifetime as well as in the iV_{OC}. Incidentally, the smallest improvements experienced on flat (111) wafers occur when the thin a-SiC:H buffer layer is inserted. Further studies would be needed to understand why it is so. However, based on these results, we can expect SHJ solar cells fabricated on flat (111) and RTno c-Si wafers to exhibit a higher final V_{OC} when the p-doping gradient is implemented.

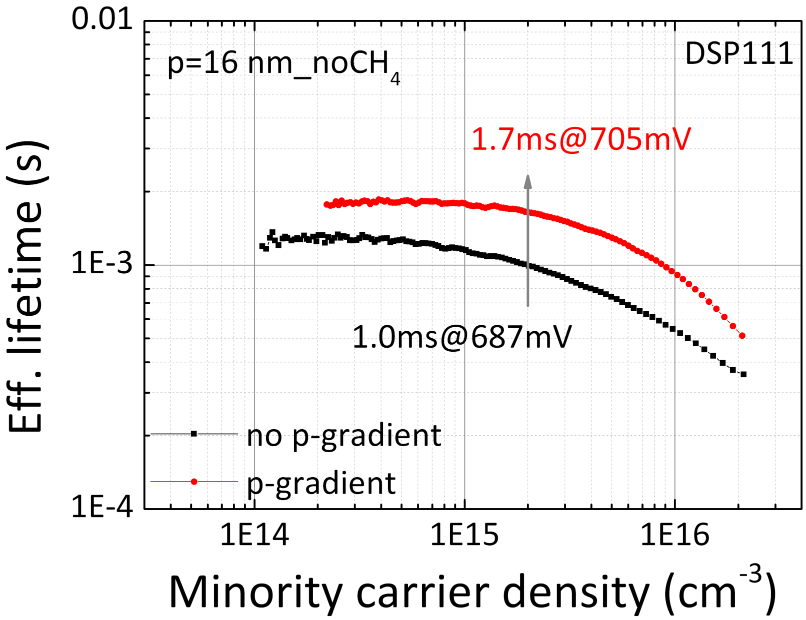

Figure 4-52 – Effective lifetimes of solar cell precursors fabricated on flat (111) c-Si wafer using a) the standard emitter recipe and b) a p-doping gradient.

	i-layer	p-layer [nm]	Gradient	As-deposited	
				τ_{eff} [ms]	iV_{OC} [mV]
Flat (111)	noCH$_4$	16	nograd	1.0	687
			grad	1.7	705
	CH$_4$	16	nograd	1.5	699
			grad	1.7	705
KIno	noCH$_4$	16	no grad	0.4	676
			grad	0.5	679
	CH$_4$	10	no grad	0.7	692
			grad	0.8	695
		16	no grad	0.8	696
			grad	0.6	684
RTno	noCH$_4$	16	no grad	0.5	681
			grad	0.7	689
	CH$_4$	10	no grad	1.5	710
			grad	1.0	703
		16	no grad	1.8	716
			grad	2.1	718

Table 4-11 – Effective lifetimes and implied V_{OC} extracted from PCD measurements done on various SHJ solar cell precursors using standard and graded emitters.

4.2.2.b Impact of a p-layer gradient on the performance of flat SHJ solar cell

Simulation study

In order to validate the results previously obtained on flat solar cell precursors, light JV characteristics were simulated using AFORS-HET. A structure close to our standard SHJ solar cell was used. To model the interface defect density, a 1-nm thick c-Si layer, with a donor-typed Gaussian defect with a 2E15 cm^{-3} net donor density was inserted between the (n)c-Si substrate and the 5-nm thick (i)a-Si:H layer. Its capture cross-sections for both electrons and holes were set at 1E-15 cm^{-2} whereas the trap density value was chosen to be close to 1E19 cm^{-3}·eV^{-1}. The donor and acceptor densities for the (n+)a-Si:H, (p)a-Si:H and (p++)a-Si:H layers were defined in such a way that their respective activation energies reach 0.2, 0.34 and 0.50 eV. Figure 4-53 shows the generated JV curves under a simulated AM1.5 spectrum. As can be seen, the software predicts three major changes when using a p-doping gradient instead of a standard emitter: i) a decrease in the V_{OC}, ii) a higher J_{SC} and iii) a lower FF. The lower V_{OC} can be understood in terms of field-effect. Indeed, by replacing 1.5 nm of the (p++)a-Si:H layer by a simple (p)a-Si:H, the software sees it as a loss in the charge extraction. Moreover, this loss is reflected on a poorer collection and a lower FF. However, by replacing a highly-doped region by a less-doped one, and despite the small 1.5 nm thickness involved, the absorption is reduced, hence the slightly higher J_{SC}. This was confirmed by simulating a JV curve using a (p)a-Si:H/(p++)a-Si:H stack of 17.5 nm, that is (1.5 + 16 nm), resulting in an increase in J_{SC} up to 38.1 mA/cm². However, the V_{OC} is lower (673 mV) and the FF remains greatly impacted (78.4%), resulting in the lower conversion efficiency of 20.1%.

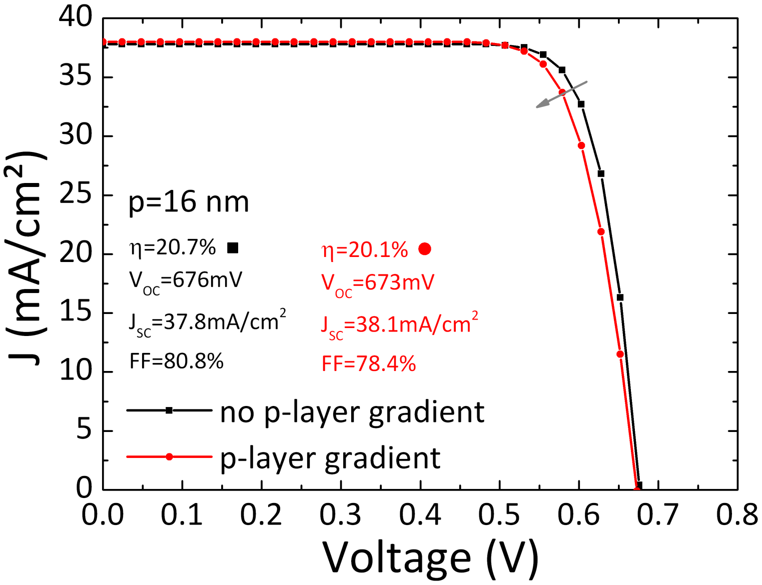

Figure 4-53 – Simulated JV characteristics of SHJ solar cells fabricated with and without a p-doping gradient using AFORS-HET.

Impact of a p-doping gradient on the performance of flat (111) SHJ solar cells

SHJ cells were finalized by sputtering ITO and evaporating silver. Light JV measurements were carried out at 1 Sun at 25°C and the results are shown in Figure 4-54. As can be seen, the trends observed by measuring the effective lifetimes are confirmed, as opposed to the simulation results shown above. Indeed, thanks to the p-doping gradient, the V_{OC} increases by +17 mV. Moreover, the J_{SC} remains constant and the FF increases by 2.7 points, thus reaching the very nice 81.4% value. Annealing these samples does not bring any change to the V_{OC} and only a small one to the J_{SC}. Nevertheless, an increase in FF is reported in the case of the p-doping gradient only, while it decreases when using a standard emitter. Figure 4-46 shows the evolution of both samples upon annealing.

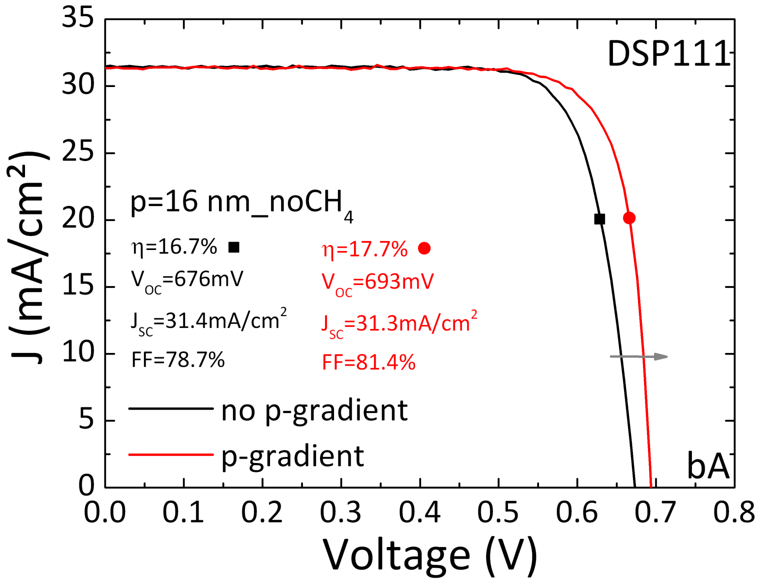

Figure 4-54 – JV characteristics of SHJ solar cells simulated with AFORS-HET for a standard emitter (black squares) and a p-doping gradient (red dots).

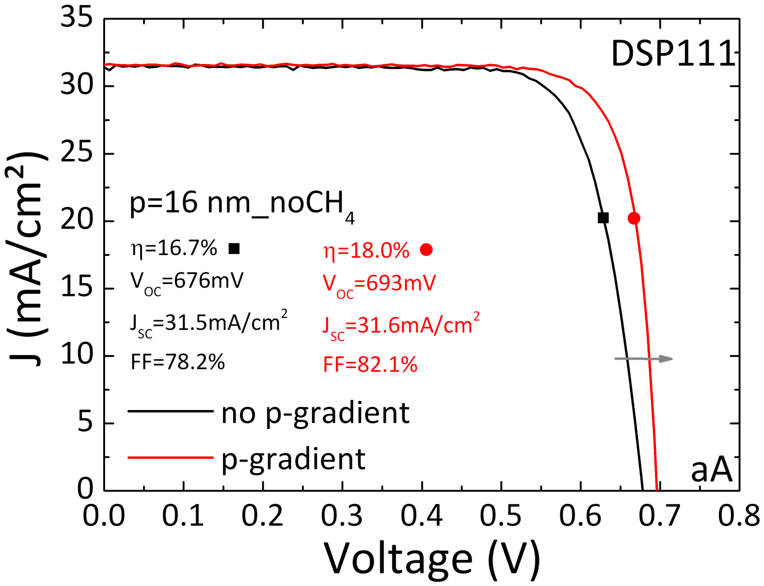

Figure 4-55 –JV characteristics of SHJ solar cells fabricated on flat (111) wafers with and without a p-doping gradient (annealed).

The much more pronounced square shape and the improvement upon annealing which the p-doping gradient generates can be clearly seen. As a result, we obtain a 2x2 cm² cell with a record conversion efficiency of 18.0%. This represents an increase of 1.3 points when compared with our standard emitter SHJ flat cell. In an attempt to understand the underlying mechanisms of this effect, JV characteristics were also performed in the dark. Figure 4-57 shows the dark JV curves of our two samples. As can be seen, by inserting a gradient, the dark current is decreased on almost the entire bias range. Despite this obvious improvement, in the as-deposited state the diode ideality factor is quite high, i.e., 1.45 instead of 1.30 and the J_0 increases by almost one order of magnitude. Upon annealing however, these two samples behave quite differently.

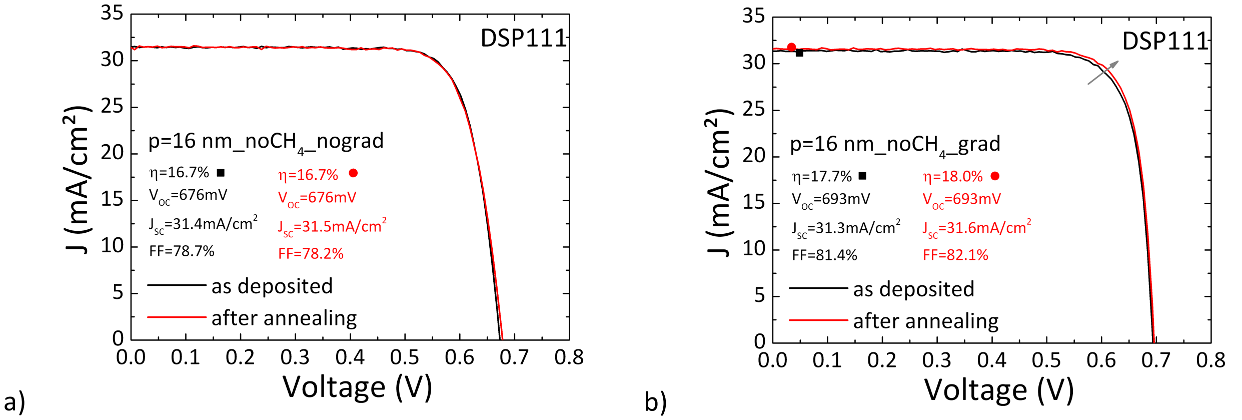

Figure 4-56 – Evolution upon annealing of the JV characteristics of SHJ solar cells fabricated a) without and b) with a p-doping gradient on flat (111) c-Si wafers.

Indeed, as can be seen in Figure 4-58, the sample which has a standard p-layer degrades and its dark current characteristics shifts slightly upwards. Moreover, its diode ideality factor increases from 1.30 up to 1.38 while the J_0 increases slightly. Contrariwise, the sample with a p-doping gradient improves. Indeed, even if its dark current experiences a slight degradation up to 0.4 V, the same decreases afterwards.

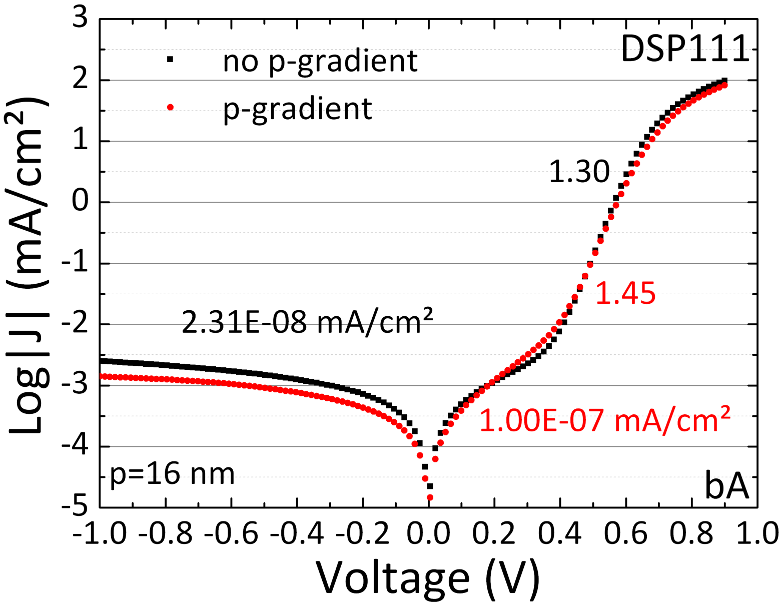

Figure 4-57 – Dark JV characteristics of SHJ solar cells fabricated on flat (111) wafers with and without a p-doping gradient (as-deposited).

As a result, the diode ideality factor of the p-graded cell decreases from a very high 1.45 value down to 1.26. Likewise, its J_0 improves by decreasing by more than one order of magnitude to finally reach 8.86E-06 mA/cm². This confirms what we expected. Figure 4-59 shows the evolution of both samples upon annealing. As can be seen in Figure 4-59b), having a p-doping gradient allows for the reduction of the recombination at the a-Si:H/c-Si interface, eventually leading to a higher V_{OC}.

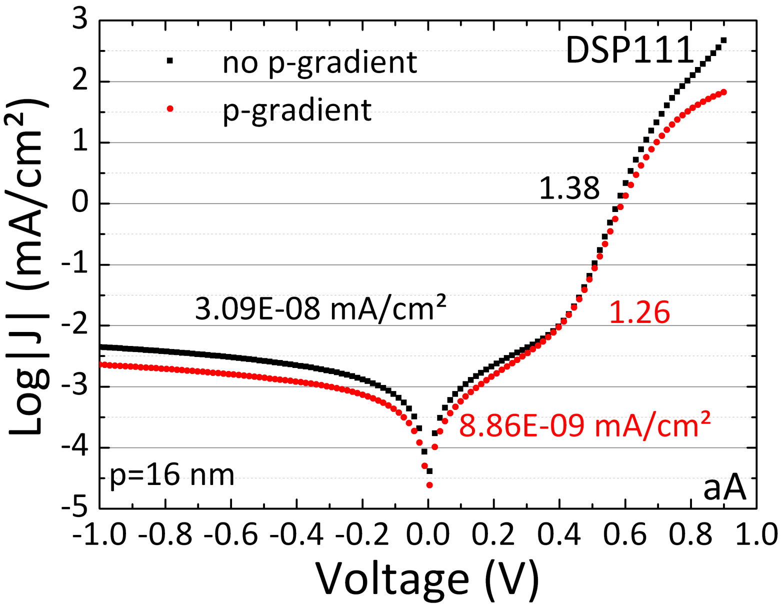

Figure 4-58 – Dark JV characteristics of SHJ solar cells fabricated on flat (111) wafers with and without a p-doping gradient (annealed).

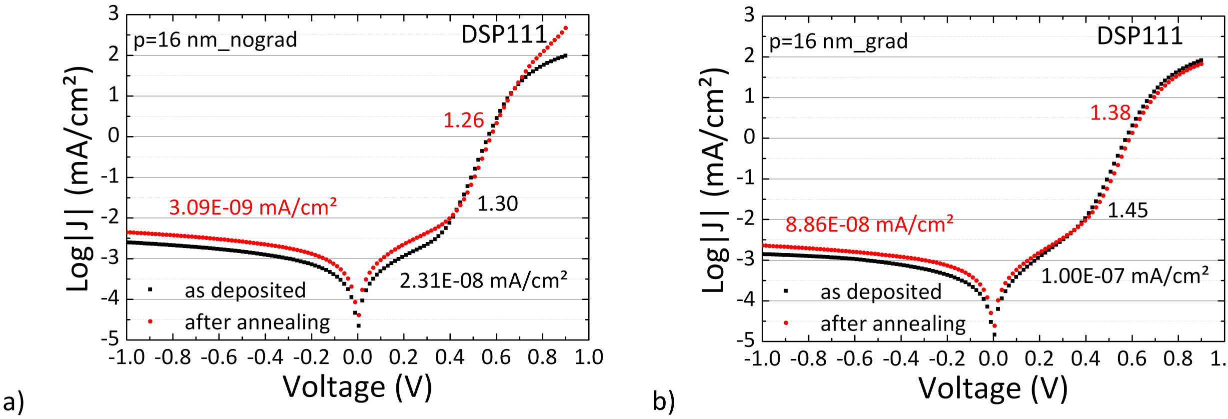

Figure 4-59 – Evolution upon annealing of the dark JV characteristics of SHJ solar cells fabricated a) without and b) with a p-doping gradient on flat (111) c-Si wafers.

Impact of a p-doping gradient on the performance of flat (111) SHJ solar cells containing a thin a-SiC:H layer at the a-Si:H/c-Si interface

Before implementing the p-doping gradient on textured SHJ solar cells, it was important to verify the latter's effect when combined with a thin a-SiC:H layer at the a-Si:H/c-Si interface at the emitter side. Indeed, even if there is no clear relation between these two layers, they are only 2.5 nm away and both participate in the passivation quality. For this purpose, two SHJ solar cells were fabricated using flat (111) c-Si wafers identical to the ones previously studied, but with a thin a-SiC:H layer inserted at both a-Si:H/c-Si interfaces. Figure 4-60 shows the light JV characteristics of both cells.

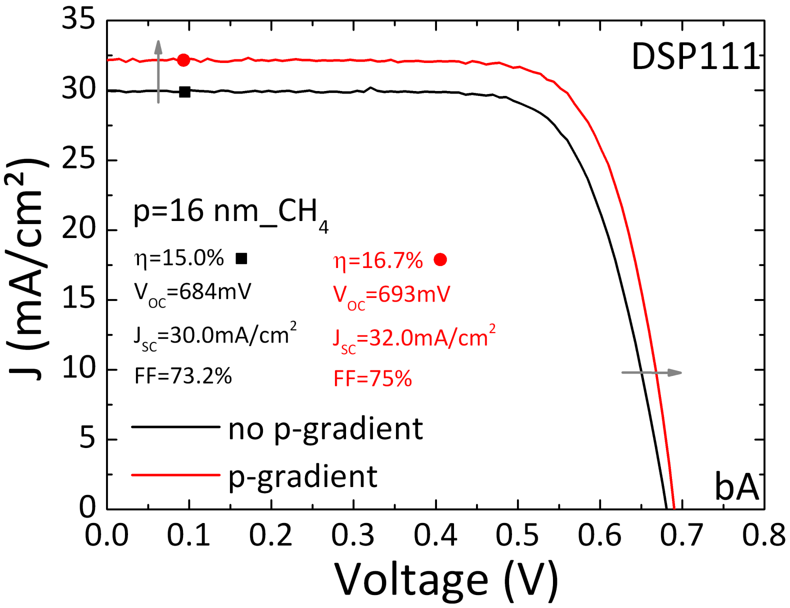

Figure 4-60 – JV characteristics of SHJ solar cells fabricated on flat (111) wafers with and without a p-doping gradient (as-deposited).

As can be seen, the insertion of a p-doping gradient in a SHJ solar cell containing a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface results in improved performances. First, the V_{OC} is higher just as the PCD results were showing (see Table 4-11). It is noteworthy that the V_{OC} of the p-gradient cell is identical to that of its a-SiC:H layer-free counterpart in Figure 4-54, reaching 693 mV in both cases. We also witness a significant enhancement of the charge carrier collection reflected by a higher J_{SC} (+2 mA/cm²) and FF (+1.8 points), thereby confirming the simulation results at this point. The implementation of a p-doping gradient thus results in an overall increase in the conversion efficiency from 15.0% up to 16.7%. This represents a quite impressive increase of 1.7 points despite the obviously higher R_S and lower FF than when omitting the thin a-SiC:H buffer layer. Figure 4-61 shows the JV characteristics performed after annealing under our standard H_2/N_2 conditions at 180°C for 30 minutes. As can be seen, both samples have improved in terms of conversion efficiency. For the standard emitter cell, this is mainly due to an increase in the V_{OC} (+9mV) and the FF (+2.6 points), while the J_{SC} increases only slightly by 0.8 mA/cm². This results in a quite significant increase in the conversion efficiency from 15.0 up to 16.2%. For the p-gradient cell however, the V_{OC} also increases up to a much higher level than its a-SiC:H-free counterpart (see Figure 4-56b)) actually, reaching 701 mV. This raises a question as to the real impact of the thin a-SiC:H layer at the interface of flat (111) cells. Indeed, all the passivation studies carried out on such substrates have shown that it had only a minor (if any) impact on the effective lifetime of symmetrical i/i stacks, as well as on SHJ solar cell precursors. JV results indicate that it is not necessarily the case and deeper annealing studies should be conducted to understand how the a-SiC:H layer helps improve the a-Si:H/c-Si interface or how it can possibly be less prone to E_F-induced degradation than a standard (i)a-Si:H layer. Indeed, since the energy bandgap of our a-SiC:H material is 1.9 eV one could imagine that the position of E_F crossing the overall (i)a-Si:H/(i)a-SiC:H stacks should generate less defects upon p-doped layer deposition.

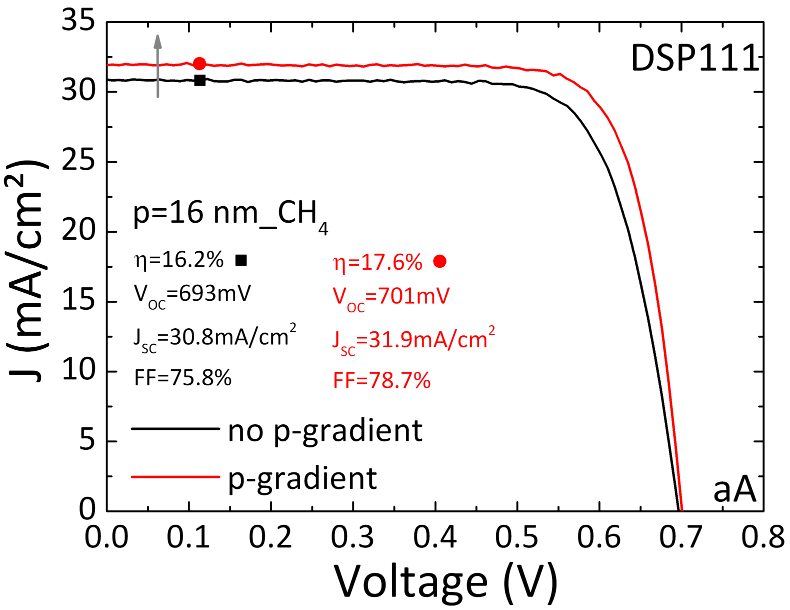

Figure 4-61 – JV characteristics of SHJ solar cells fabricated on flat (111) wafers with and without a p-doping gradient (annealed).

On the other hand, the J_{SC} remains almost constant while the FF again increases to reach the value of 78.7% (+3.7 points). This cannot be explained in terms of Ag/ITO contact improvement solely. Indeed, when looking at the performance of the a-SiC:H-layer-free cells of Figure 4-56, one can clearly see that this improvement must be related to the presence of the p-layer gradient.

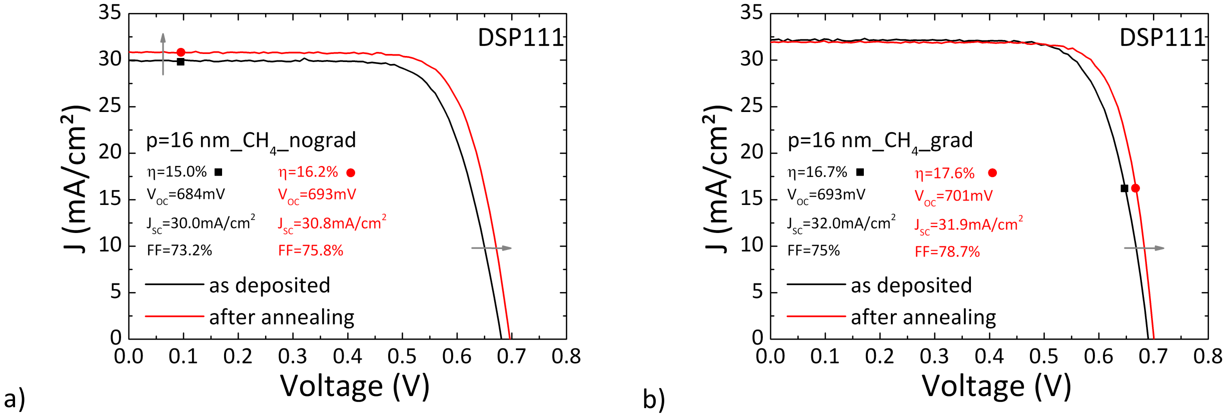
a) b)

Figure 4-62 – Evolution upon annealing of the JV characteristics of SHJ solar cells fabricated a) without and b) with a p-doping gradient on flat (111) c-Si wafers.

Figure 4-62a) and b) show the improvement of both cells under study upon annealing. As can be seen, both cells improve in terms of V_{OC}. However, it is striking to see how the presence of a p-doping gradient helps us reach a V_{OC} above 700 mV and a FF close to 79%. In order to understand these improvements in terms of recombination, JV characteristics were performed in the dark. Figure 4-63 shows the dark JV characteristics of both cells in their as-deposited state. As can be seen, despite the slight shift upwards, the implementation of a p-doping gradient does not bring any change in terms of recombination since the J_0 remains constant, i.e., around 9E-08 mA/cm². Likewise, the diode ideality factor remains constant since the slight variation stays within the measurement and fitting error, reaching a value close to 1.4. Upon annealing, the dark current remains almost unchanged apart from the low forward-bias region.

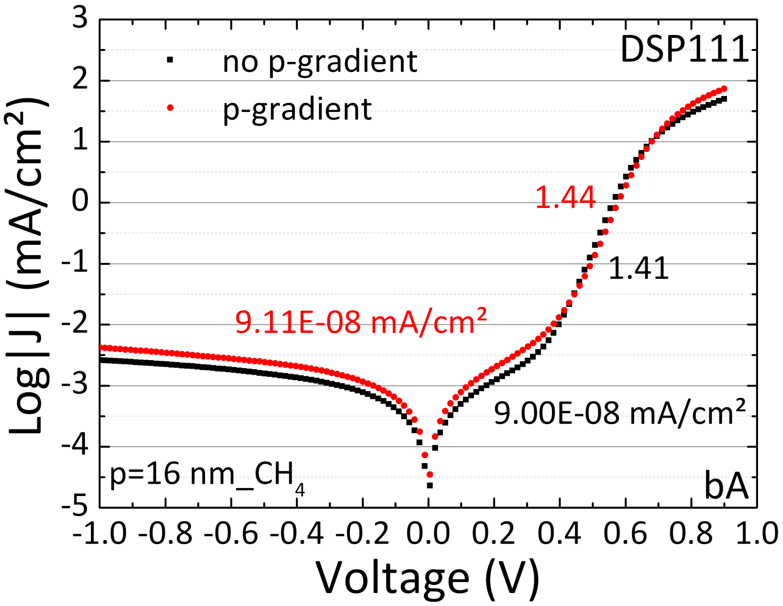

Figure 4-63 – Dark JV characteristics of SHJ solar cells fabricated on flat (111) wafers with and without a p-doping gradient (as-deposited).

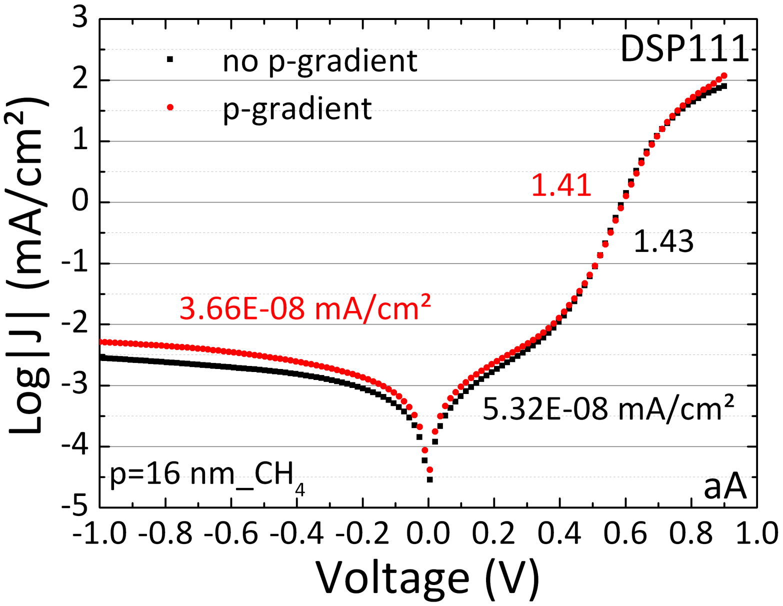

Figure 4-64 – Dark JV characteristics of SHJ solar cells fabricated on flat (111) wafers with and without a p-doping gradient (annealed).

Likewise, the diode ideality factor remains constant. However, recombination mechanisms are obviously reduced since the J_0 decreases significantly. Moreover, the decrease of J_0 is more significant when a p-doping gradient is implemented, thereby confirming the increase of V_{OC} observed under 1 Sun illumination. Figure 4-65 shows the evolution of the dark JV characteristics of both cells upon annealing under our standard conditions.

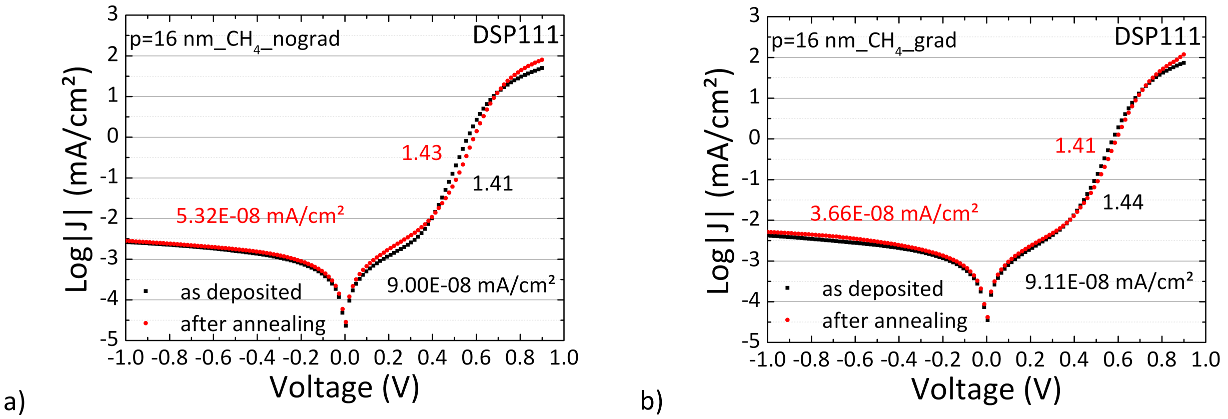

Figure 4-65 – Evolution upon annealing of the dark JV characteristics of SHJ solar cells fabricated a) without and b) with a p-doping gradient on flat (111) c-Si wafers.

As can be seen, implementing a p-doping gradient did not necessarily bring any change at first in terms of recombination. However, this architecture provides a higher potential for improvements upon annealing. Indeed, the gradient allowed the cell to reduce the recombination more effectively than with a standard emitter, resulting in a stronger decrease in the J_0 and a slight decrease in the diode ideality factor. Moreover, when comparing with the cells in Figure 4-59, we see that the benefits of such a gradient are evidenced only when a thin a-SiC:H buffer layer is inserted at the a-Si:H/c-Si interface. Indeed, we are no longer limited by the higher resistivity of the 1.5-nm thick low-doped (p)a-Si:H layer but by the defective 2.5-nm thick a-SiC:H layer.

To conclude, the study on the impact of a p-doping gradient on the performance of flat (111) SHJ solar cells showed us that a gradient is beneficial for the final conversion efficiency, whether a thin a-SiC:H buffer layer is present at the a-Si:H/c-Si interface or not. Indeed, despite the higher resistivity of such a low-doped (p)a-Si:H layer, it helps in reducing the recombination at the a-Si:H/c-Si and (i)a-Si:H/(p++)a-Si:H interfaces, providing significant improvements upon annealing. As a result, the V_{OC} is higher and the collection is enhanced, thus leading to higher FF values. Moreover, when inserting a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface, we are no longer limited by this low-doped region. This leads us to think that when implementing such a gradient on textured substrates, recombination should be reduced and, as a result, higher efficiencies should be reached. This will be developed in the following section.

4.2.2.c Impact of a p-layer gradient on the performance of textured SHJ solar cell

In an attempt to reach higher efficiencies, we decided to keep the enhanced i-layer stack made of (i)a-SiC:H and (i)a-Si:H as discussed in 4.1.4, since this improvement led us to higher V_{OC}s. However, despite the increase in J_{SC} due to the c-Si texturation, we could not obtain efficiencies higher than those obtained on (111) flat substrates. For KIno wafers, we reached 18.1% whereas for RTno wafers, we could not get beyond 17.5%. The detailed results are shown in Table 4-12. However, since the implementation of a p-doping gradient on flat (111) SHJ solar cells (with and without a thin a-SiC: H layer inserted at the a-Si:H/c-Si interface) led to an increase in the V_{OC} and of the FF, textured wafers were used to fabricate SHJ solar cells using the same conditions as described in Table 4-10 and by adapting the deposition times to match the same thicknesses. The resulting SHJ solar cell architecture is described in Figure 4-66.

Cell	Eff. [%]	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]
DSP111 noCH4 nograd	16.9	676	31.8	78.5
DSP111 noCH4 grad	18.0	693	31.6	82.1
DSP111 CH4 nograd	16.2	693	30.8	75.8
DSP111 CH4 grad	17.6	701	31.9	78.7
KIno CH4 nograd	18.1	684	34.7	76.2
RTno CH4 nograd	17.5	684	34.5	74.0

Table 4-12 – Performance of flat and textured SHJ solar cells as a function of the type of substrate and emitter.

Despite the unclear impact of a p-doping gradient on the passivation of textured SHJ solar cell precursors (see Table 4-11), the improvement of their performance is quite striking. Figure 4-67 shows the JV characteristics of two RTno SHJ solar cells. Both have a 16-nm thick emitter, however, the second one contains of a p-doping gradient. As can be seen, despite similar effective lifetimes, i.e., close to 1.8-2 ms, and iV_{OC}s, i.e., within the 716-718 mV range, the two cells exhibit a difference of 41 mV in their final V_{OC}. Indeed, the cell with p-layer gradient yields a V_{OC} of 684 mV, while the standard cell a V_{OC} of 643 mV.

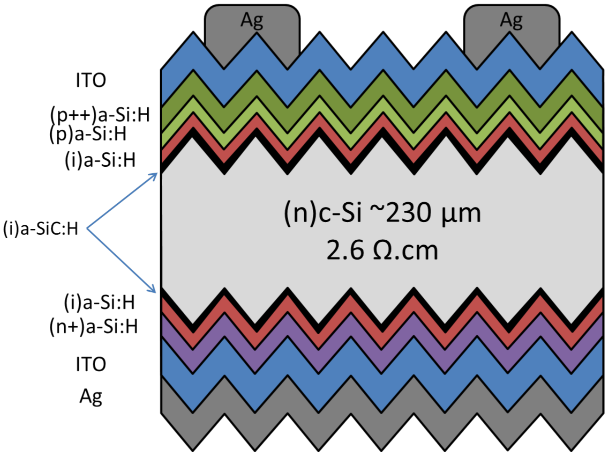

Figure 4-66 – Schematic representation of a textured SHJ solar cell fabricated using a thin a-SiC:H buffer layer at both a-Si:H/c-Si interfaces and a p-doping gradient on the emitter side. The sketch is not drawn to scale.

Likewise, the gradient allows the J_{SC} to gain more than 1 mA/cm², confirming the collection enhancement reflected by an increase of the FF by 1 point, from 75.1 up to 76.1%. As a result, we experience a 2-point gain in efficiency. Indeed, by replacing the standard emitter with a graded one, the conversion efficiency increases from 17.2 to 19.2%. In order to understand the significant difference in V_{OC}, other parts of the two SHJ solar cell precursors were used to study the passivation degradation upon ITO sputtering. Figure 4-68a) shows the effective lifetime of the SHJ solar cell precursor with a standard emitter as a function of the minority carrier density, in its as-deposited state and after ITO sputtering. Figure 4-68b) shows the same measurement obtained from the SHJ solar cell with a graded p-layer. As can be seen, the SHJ solar cell precursor with a standard emitter degrades significantly upon ITO sputtering. Indeed, its effective lifetime drops by 75 %, from 1.8 ms down to 0.4 ms whereas its iV_{OC} experiences a loss of -39 mV, from 716 down to 677 mV. This is not at all the case with the graded precursor. In Figure 4-68b) we see that sputtering ITO under the same conditions induces a loss in effective lifetime by 67 %, which keeps the passivation up, i.e., above 1 ms. Besides, for this sample, we experience a drop in iV_{OC} of -25 mV only, keeping the passivation level high with an iV_{OC} of 693 mV.

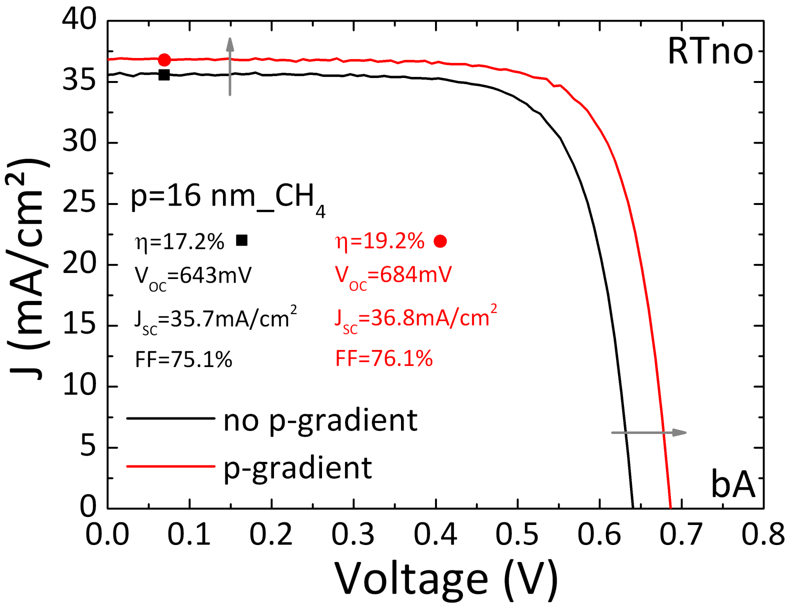

Figure 4-67 – JV characteristics of SHJ solar cells fabricated on RTno textured c-Si wafers with and without a p-doping gradient (as-deposited).

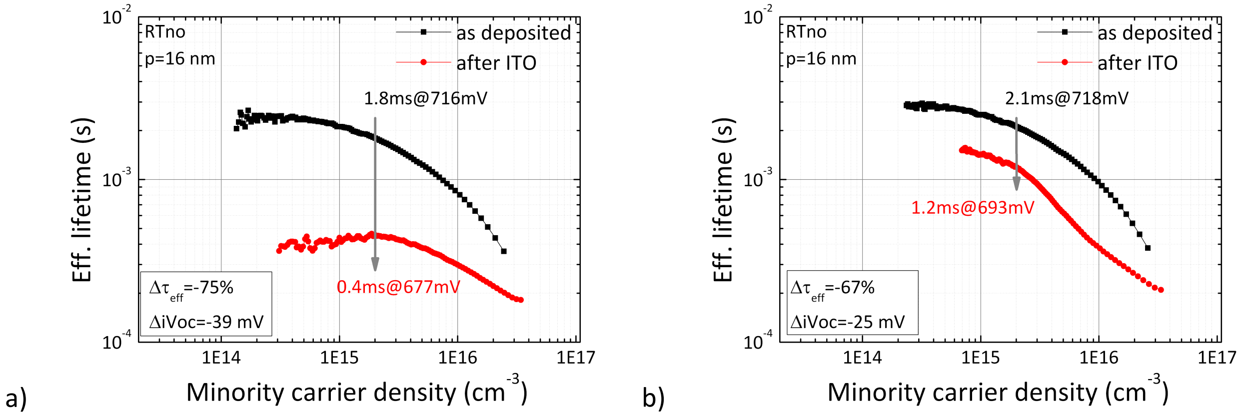

Figure 4-68 – Effective lifetime of SHJ solar cell precursors fabricated on RTno wafers, before and after sputtering of a standard ITO layer a) with a standard p-layer and b) with a p-gradient.

This helps us understand why the V_{OC} of the finalized cells are so different in their as-deposited state, but they also show the higher sensitivity of a passivated cell upon sputtering when the intrinsic and p-doped layers are not separated by a low-doped (p)a-Si:H transition layer. This tends to confirm our previous study on the impact of boron on passivation. Further studies would be needed to confirm such a trend and the benefits of this kind of gradient. However, this opens doors to the codevelopment of optimal ITO/p-layer stacks instead of optimizing these layers separately. Indeed, just as *Zhang et al.* have shown that lowering the RF power used upon ITO sputtering helped reduce the passivation degradation[206], our results show that changing the p-layer structure may also prevent the a-Si:H/c-Si interface from degrading. Annealing the previously studied SHJ cells under our standard conditions yields the performances shown in Figure 4-69.

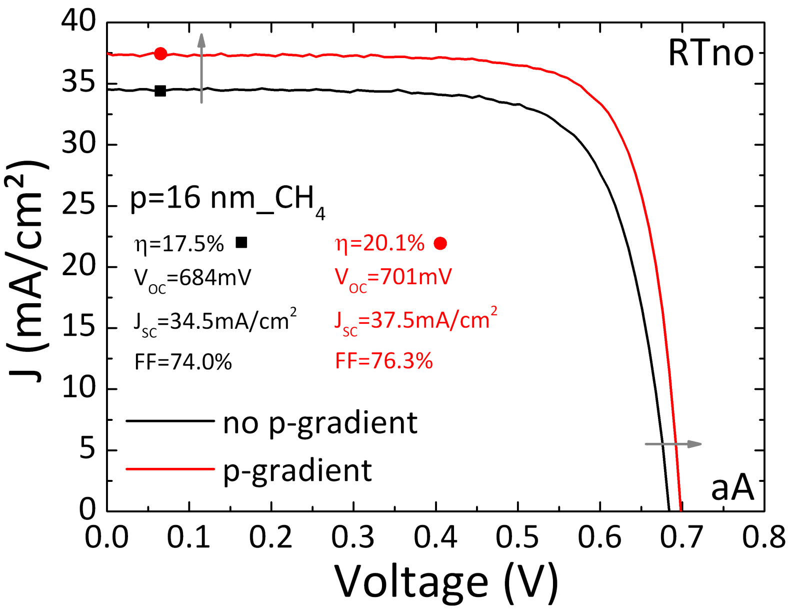

Figure 4-69 – JV characteristics of SHJ solar cells fabricated on RTno textured c-Si wafers with and without a p-doping gradient (annealed).

As can be seen, after annealing the benefits of a graded p-layer are striking. Even though the V_{OC} increases in both cases, the graded cell exhibits the highest V_{OC} value: 701 mV. Moreover, the charge collection is still strongly enhanced by this p-layer gradient. Indeed, the J_{SC} is 2.6 mA/cm² higher and the FF increases by 2.3 points. Thanks to this, the overall conversion efficiency could be increased up to 20.1%, which is 2.6 points more than the SHJ cell with a standard p-layer. To understand such an increase in the J_{SC}, two possibilities are to be taken into account: on the one hand, this could be due to an optical effect which would stem from a lower absorption in the graded p-layer stack due to the lower doping level. On the other hand, this could be due to weakened recombination mechanisms due to a reduced Fermi-level related defect creation effect at the interface between the (p++)a-Si:H layer and the passivating (i)a-Si:H layer underneath. To determine the origin of this J_{SC} increase, reflectance measurements were performed on the emitter side of two KIno cells: one with a standard p-layer and another one with a graded p-layer. The well-known relationship between the absorbance A, the transmittance T and the reflectance R gives us A+T+R=1. For both samples we then have:

$$\begin{cases} A_{nograd} + T_{nograd} + R_{nograd} = 1 \\ A_{grad} + T_{grad} + R_{grad} = 1 \end{cases} \tag{87}$$

After checking that the transmittance T is the same in both cases and that it is equal to zero ($T_{nograd}=T_{grad}=0$) within our measurement range, we notice that measuring R on both cells gives us an estimation of the absorbance A:

$$\begin{cases} A_{nograd} = 1 - R_{nograd} \\ A_{grad} = 1 - R_{grad} \end{cases} \tag{88}$$

Figure 4-70 shows us the reflectance of both samples as a function of the wavelength. As can be seen, the two curves overlap almost completely on the entire wavelength range.

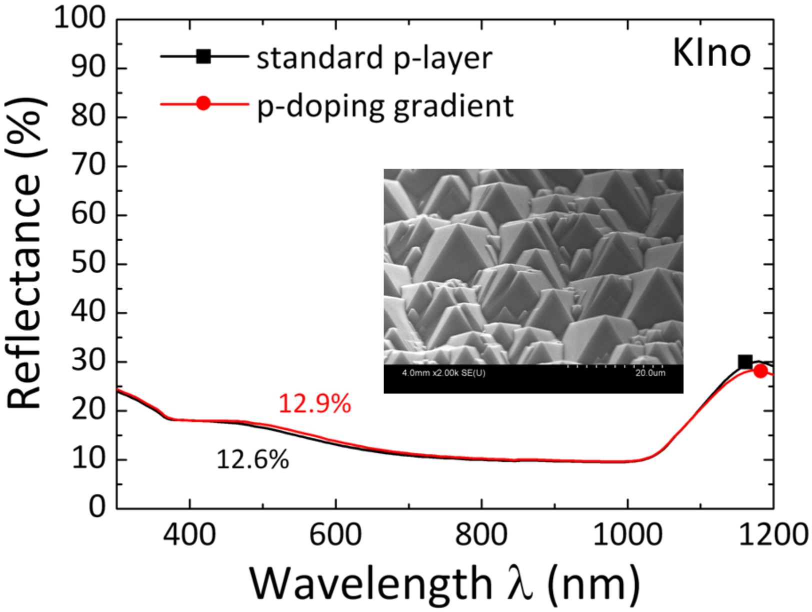

Figure 4-70 – Reflectance as a function of wavelength measured on the emitter side of the KIno cells: with a standard p-layer (black square) and with a graded p-layer (red dot).

This actually shows that by implementing a p-layer gradient, we do not lower the absorption on the front side but we indeed weaken the recombination mechanisms by reducing the amount of Fermi-level related created defects. For comparison purposes, the evolutions of the JV characteristics of these two cells upon annealing are shown separately in Figure 4-71a) and b). As can be seen, the cell with a standard emitter experiences a significant increase of the V_{OC}, from 643 up to 684 mV, confirming the reversibility of sputtering damages demonstrated in 4.2.1. Unexpectedly however, the charge collection seems to be hindered after this annealing step. Indeed, the J_{SC} as well as the FF decrease (-1.2 mA/cm² and -1.1 point), unlike what could be experienced on flat (111) wafers. As a result, despite the significant increase of V_{OC}, this only leads to a minor increase of the conversion efficiency of 0.3 points, from 17.2% up to 17.5%. It is worth noting that despite the quite good V_{OC} and J_{SC}, the low FF prevents us from going beyond the efficiencies that could be reached using flat substrates, making all light-trapping benefits from texturing useless. On the other hand, when using a p-layer gradient, all cell parameters improve. The V_{OC} increases from the already high value of 684 mV up to 701 mV, which represents a +17 mV gain. The charge collection is also improved, reflected by a +0.7 mA/cm² and a +0.2 point increase in J_{SC} and FF, respectively. Consequently, the conversion efficiency increases by almost 1 point, from 19.2% to 20.1%. This time, the highest conversion efficiency obtained on a flat (111) wafer, i.e., 18.0%, is overridden by more than 2 points, making the use of textured wafers sensible. To conclude, we have seen that the use of a p-layer gradient is also beneficial in the case of textured wafers. Thanks to this, we have been able to enhance the conversion efficiencies of SHJ solar cells and go beyond the highest values we had obtained on flat (111) wafers, up to a record value of 20.1% with a V_{OC} of 701 mV on a 2x2 cm² surface. However, there is room for improvement since the maximum value for the FF did not go beyond 76.3%. This represents a significant improvement compared to standard cells with no p-layer gradient.

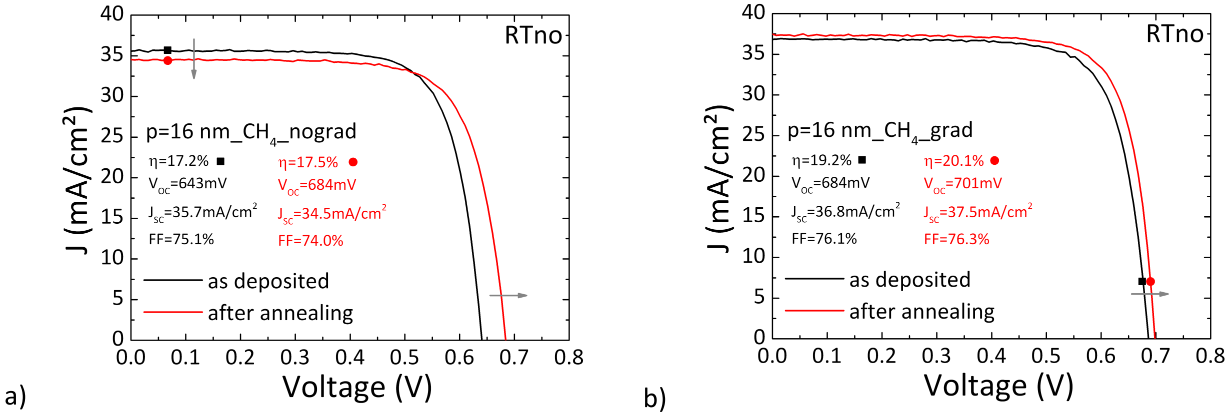

Figure 4-71 – Evolution upon annealing of the JV characteristics of SHJ solar cells fabricated a) without and b) with a p-doping gradient on RTno textured c-Si wafers.

Nevertheless, this is quite far from the 78.7% value we could obtain on flat (111) wafers using the same cell architecture. Therefore, we decided to investigate the impact of the (p++)a-Si:H layer thickness on the SHJ solar cell performance.

4.2.2.d Impact of the (p++)a-Si:H layer thickness on the performance of flat and textured graded SHJ solar cells

In order to study the impact of the (p++)a-Si:H layer thickness on the SHJ solar cell performance, we fabricated a series of 4 cells for each type of substrate. While the whole BSF side and the (p)a-Si:H layer were kept constant in terms of deposition conditions and thickness, the (p++)a-Si:H layer thickness was varied so that the overall p-layer thickness ranged from 10 to 19 nm. Figure 4-73 shows the evolution of the effective lifetime and the iV$_{OC}$ as a function of the overall p-layer thickness for SHJ solar cell precursors fabricated on flat (111) wafers with no a-SiC:H thin layer at either a-Si:H/c-Si interface. As can be seen, the effective lifetime finds its lowest value for the thinnest p-layer. When increasing the p-layer thickness, this increases until it reaches a maximum for p=16nm. Increasing the thickness further results in a decrease in the effective lifetime, showing that the boron starts being detrimental for the a-Si:H/c-Si interface. By looking at the iV$_{OC}$ extracted from the same PCD measurements, we find the same optimum for a p-layer thickness of 16 nm. Despite the fact that the trend is less clear[35] than in the case of the effective lifetime, and the minimum iV$_{OC}$ value is reached for the intermediate 13 nm value, we find that the best efficiency should be reached for a 16 nm value. In order to confirm these results, these four cells were finalized by sputtering an 82 nm-thick layer of our standard ITO and evaporating approximately 1 µm of silver thermally. Figure 4-73 shows the JV characteristics obtained after annealing these cells under our standard conditions. As can be seen, the trend is identical to that of the PCD results. Indeed, the best performance is reached for the 16-nm thick p-layer, with a conversion efficiency of 18.0%. This is partly due to the V$_{OC}$, which also finds its maximum value for such a thickness. However, the PCD trends are not necessarily followed with regard to this parameter. Indeed, the lowest V$_{OC}$ is found for a thickness of 10 nm while it remains constant after reaching its peak at 16 nm.

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[35] This is most certainly due to the fact that τ_{eff} is extracted at 2E15 cm^{-3} whereas the iV$_{OC}$ is calculated at 1 Sun, thus at a slightly different injection level.

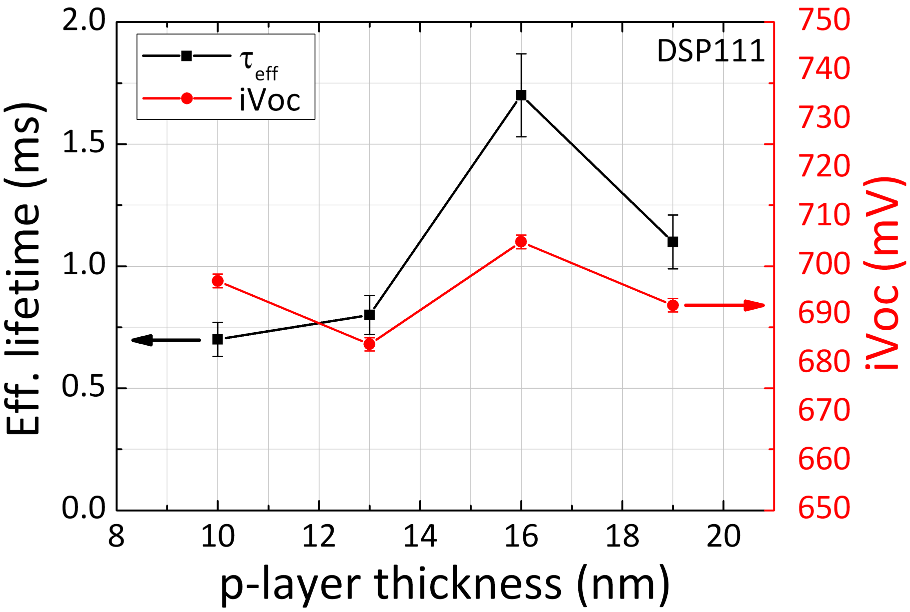

Figure 4-72 – Evolution of the effective lifetime and iV_{OC} of SHJ solar cell precursors fabricated on flat (111) c-Si wafers as a function of the overall p-layer thickness. No a-SiC:H thin layer is present at the a-Si:H/c-Si interfaces.

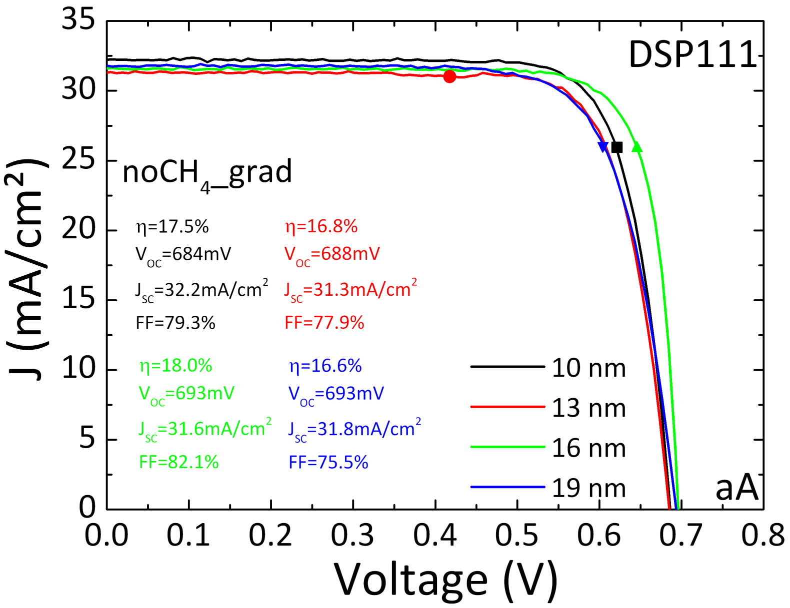

Figure 4-73 – JV characteristics of flat (111) SHJ solar cells with a p-graded emitter as a function of the (p++)a-Si:H layer thickness (annealed).

This shows that adding 3 nm to the optimum thickness is not detrimental to the passivation process but more so to the charge carrier collection. This is confirmed by the FF, which severely degrades at 19 nm. The evolution of the cell parameters with the p-layer thickness is shown in the as-deposited and annealed state in Figure 4-74. The measurement uncertainties were too small to be considered as significant. For this reason, error bars which are not relevant anymore are not shown. As can be seen, the trends extracted from the PCD measurements can be found again on finalized cells, in their as-deposited state. Indeed, there is a clear optimum at 16 nm for the efficiency, FF and V_{OC} parameters.

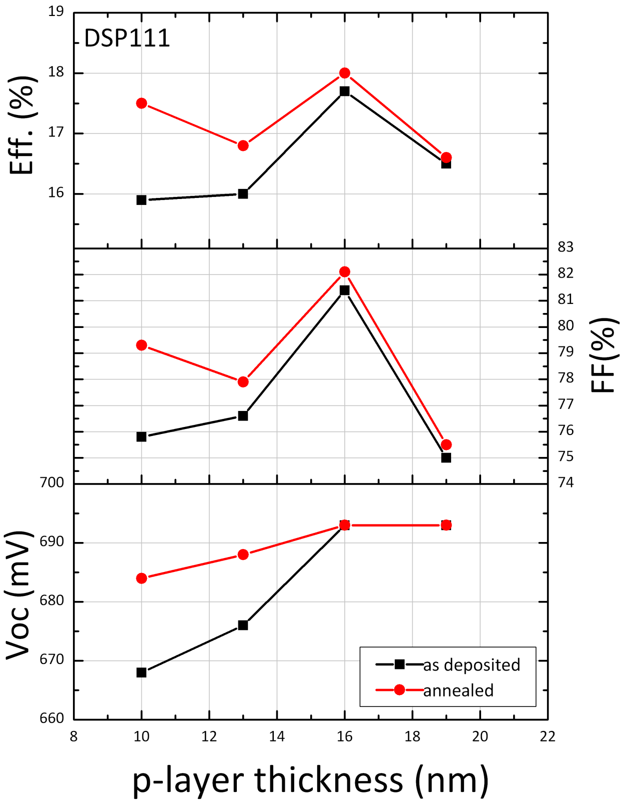

Figure 4-74 – Evolution of the solar cell parameters of flat (111) SHJ solar cells with a p-graded emitter as a function of the (p++)a-Si:H layer thickness, before and after annealing. No a-SiC:H thin buffer layer is present at the a-Si:H/c-Si interface.

The annealing process seems to change this trend by unexpectedly improving substantially the SHJ solar cell with a 10-nm thick emitter. Even if its V_{OC} is still the lowest, the thin p-layer limits the absorption and allows for an enhanced charge collection, as reflected by a higher J_{SC} and FF. Increasing the p-layer thickness increases the absorption, and the length charge carriers must go through, thus lowering the J_{SC} and FF. However, at 16 nm, the V_{OC} is enhanced by the thicker p-layer, allowing for a stronger charge carrier extraction. As a result, the FF is the highest and the J_{SC} can remain quite high, i.e., close to 32 mA/cm². In an attempt to verify if this p-layer thickness is also optimal on textured wafers, SHJ solar cells were fabricated using RTno wafers and by adapting the deposition times to match p-layer thicknesses ranging 10-19 nm. Figure 4-75 shows the evolution of the effective lifetimes and iV_{OC}s of the corresponding SHJ solar cell precursors as a function of the (p++)a-Si:H thickness. As can be seen, the trend obtained on flat (111) wafers is quite closely matched on our RTno textured wafers, despite the presence of a thin a-SiC:H layer at both of their a-Si:H/c-Si interfaces to suppress all local epitaxial growth, and thus increase the V_{OC}. Indeed, even if the optimum is less sharply defined the maximum τ_{eff} value is found at p=16 nm. On the other hand, while the maximum iV_{OC} value is found at p=13 nm, values for p=13 and 19 nm are quite close, i.e., between 709 and 713 mV. These results are confirmed by the light JV characteristics performed on finalized SHJ solar cells. Indeed, in Figure 4-76, we can see that again, a p-layer thickness of 16 nm is optimal to get the maximum conversion efficiency.

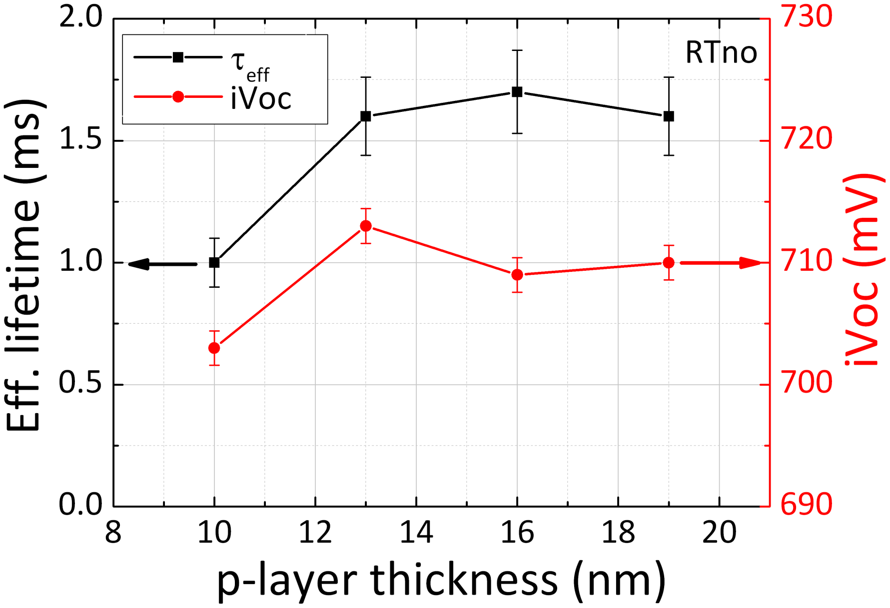

Figure 4-75 – Evolution of the effective lifetime and iV_{OC} of SHJ solar cell precursors fabricated on textured RTno c-Si wafers as a function of the overall p-layer thickness. A thin a-SiC:H layer is present at both a-Si:H/c-Si interfaces.

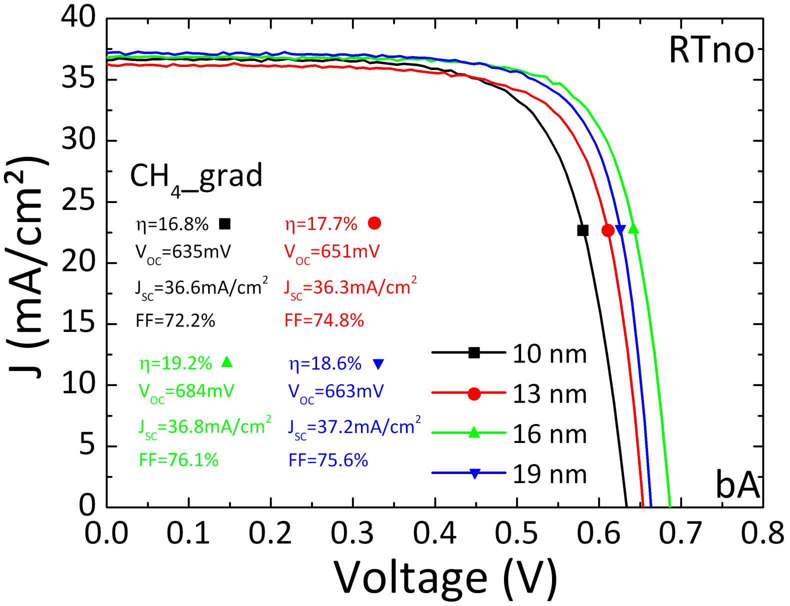

Figure 4-76 – JV characteristics of RTno textured SHJ solar cells with a p-graded emitter as a function of the (p++)a-Si:H layer thickness (as-deposited).

This is made possible partly thanks to the high V_{OC} but also to the enhanced charge collection. Indeed, despite the almost constant J_{SC}, the FF evolves with regard to the p-layer thickness and its maximum value is found to be 76.1% at p=16 nm. However, contrary to what could be seen on flat (111) wafers, this trend is preserved upon annealing. The evolution of the RTno cell parameters with the p-layer thickness are shown in their as-deposited and annealed state in Figure 4-77. As can be seen, the optimum for all cell parameters is found for a p-layer thickness of 16 nm, before and after annealing. Moreover, it is clear that the annealing step shifts the V_{OC} upwards in a quite reproducible fashion.

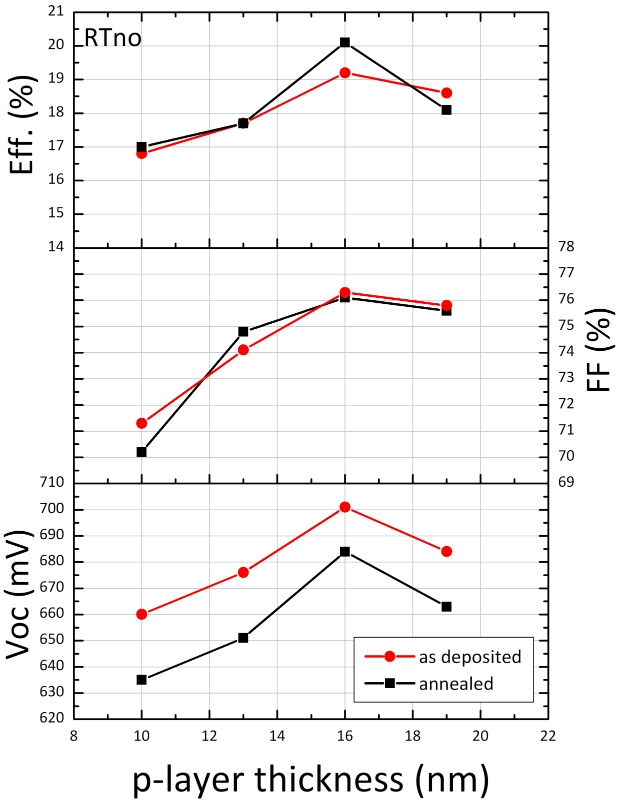

Figure 4-77 – Evolution of the solar cell parameters of RTno textured SHJ solar cells with a p-graded emitter as a function of the (p++)a-Si:H layer thickness, before and after annealing. A thin a-SiC:H buffer layer is present at both a-Si:H/c-Si interfaces.

This is not exactly the case for other cell parameters, such as the FF. Indeed, the fill-factor is very much related to the charge carrier collection and therefore, depends also on the current. As could be seen in Figure 4-76, the J_{SC} first decreased slightly before increasing from p=16 nm. Table 4-13 summarizes all cell parameters extracted by performing the JV measurements on RTno cells in their as-deposited and annealed states.

RTno cells	state	Eff. [%]	V_{OC} [mV]	J_{SC} [mA/cm²]	FF [%]
10 nm	bA	16.8	635	36.6	72.2
	aA	17	660	36.1	71.3
13 nm	bA	17.7	651	36.3	74.8
	aA	17.7	676	35.3	74.1
16 nm	bA	19.2	684	36.8	76.1
	aA	20.1	701	37.5	76.3
19 nm	bA	18.6	663	37.2	75.6
	aA	18.1	684	34.9	75.8

Table 4-13 – Performance of RTno textured SHJ solar cells containing a p-layer gradient on the emitter side.

To conclude, it was found that a thickness of 16 nm for the (p++)a-Si:H layer is optimal. Indeed, on flat (111) with no a-SiC:H buffer layer at the a-Si:H/c-Si interface as well as on RTno textured wafers with a thin a-SiC:H buffer layer at the a-Si:H/c-Si interfaces, PCD measurements yielded the highest effective lifetimes for this value. Moreover, by depositing this thickness for the (p++)a-Si:H layer, the highest V_{OC}

and FF values were obtained, while the J_{SC} approximated the maximum value. This led us to two record conversion efficiencies: 18.0% on flat (111) n-type c-Si wafers and 20.1% on RTno textured n-type c-Si wafers.

Chapter Key Results

To conclude this chapter, we have seen that the introduction of a thin a-SiC:H layer at the a-Si:H/c-Si interface of SHJ solar cells:

- does not impact the passivation of flat (111) SHJ solar cell precursors,
- allows for similar conversion efficiencies of SHJ solar cells, despite a slightly lower FF because of charge carrier collection degradation due to a higher band mismatch,
- increases the V_{OC} of textured SHJ solar cell precursors regardless of the texturing recipe, by impeding local epitaxial growth,
- allows for higher conversion efficiencies on textured SHJ solar cell thanks to a higher V_{OC} and a greater potential for improvement upon thermal annealing (lack of local epitaxy).

Upon finalization of our SHJ solar cells however, we have noticed the detrimental impact of TCO sputtering on the effective lifetime and iV_{OC} of SHJ solar cell precursors:

- ITO sputtering damages both a-Si:H/c-Si interfaces (BSF and emitter sides),
- the effective lifetime and iV_{OC} drops during ITO sputtering on SHJ solar cell precursors are due to the higher sensitivity of the a-Si:H/c-Si interface on the emitter side (p-type a-Si:H),
- this doping-dependence could be verified by demonstrating that the passivation degradation does not depend on the p-layer thickness, unlike the intrinsic or n-type a-Si:H layer,
- it was suggested that the higher hydrogen diffusion coefficient in p-type a-Si:H combined with E_F-related sensitivity to defect creation could explain the higher degradation of the passivation on the p-side. However, further studies would be required to gain a better understanding of this phenomenon.

The latter results led to the replacement of the standard (p++)a-Si:H by a graded (p)a-Si:H/(p++)a-Si:H stack:

- it was shown by simulation that introducing a thin slightly-doped (p)a-Si:H transition layer allowed for the Fermi level to cross through the (i)a-Si:H layer at a slightly larger E_F-E_V distance,
- a p-layer gradient allows for a higher effective lifetime and iV_{OC} on the great majority of our samples, regardless of whether they are flat or textured,
- a p-layer gradient allows for a smaller degradation of the passivation of our samples upon ITO sputtering, compared to our standard p-layer,
- simulation results predicted that the implementation of a p-layer gradient should be detrimental to the V_{OC} and FF of finalized devices, and thus induce slightly lower efficiencies,
- contrary to simulation results, a p-gradient was successfully implemented in the standard SHJ solar cell architecture on flat (111) wafers and allowed for significant gains in the V_{OC} and FF, which translated into higher conversion efficiencies. As a result, a 2x2 cm² SHJ solar cell with a record efficiency of 18.0% with a FF of 82.1% was fabricated on a flat (111) (n)c-Si wafer,
- when replacing the standard emitter by a p-gradient on flat (111) SHJ solar cells with a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface, the conversion efficiency improves due to an increase of the V_{OC} and FF,

- when using a p-gradient on textured samples, both the V_{OC} and the charge carrier collection increase. As a result, we obtained a 2x2 cm² SHJ solar cell with a record efficiency of 20.1% and a V_{OC} of 701 mV,
- by studying the impact of the (p++)a-Si:H layer, it was found that the optimal thickness is 16 nm and that the trends on flat (111) and textured samples are comparable. This shows that the implementation of the thin a-SiC:H layer at the a-Si:H/c-Si interface and of the p-gradient made it possible to overcome the higher interface defect density usually met on textured c-Si wafers, regardless of the texturing recipe used.

5 Conclusion

5.1 Achievements

The aim of this thesis was to reach higher efficiencies on SHJ solar cells by going from flat to textured c-Si substrates. Indeed, previously, in our laboratory, J. Damon-Lacoste and M. Labrune had managed to obtain conversion efficiencies above 17% on flat (100) p- and n-type wafers, respectively. However, while trying a simple transfer of substrates, we noticed that we lacked knowledge and experience with wafer texturing and the passivation thereof with a-Si:H deposited by PECVD. Indeed, under certain conditions, it seemed as if the random pyramid landscape, theoretically made of (111) crystallographic planes, did not respond to a-Si:H deposition as a simple (111) flat substrate. The surface ratio could not explain the significantly lower effective lifetimes and iV_{OC}s we could obtain. This led us to study the impact of the (100) and (111) orientations on the passivation by a-Si:H and crystalline silicon texturing using alkaline wet-etching. While doing so, we noticed that the method we were using to impede local epitaxial growth on flat (100) wafer improved the passivation of anisotropically-etched c-Si wafers, regardless of the texturing recipe or the wafer doping. Indeed, thanks to the addition of a small amount of an impurity (carbon in our case) which resulted in the deposition of an a-SiC:H alloy at the a-Si:H/c-Si interface, the effective lifetime often increased by a factor of 2 while the iV_{OC} could easily gain 20 to 30 mV. A complementary study showed us that this buffer layer had absolutely no impact on the passivation of flat (111) c-Si wafers. Since this method proved to be efficient in the case of (100) flat wafers, this intriguing result was examined under the angle of a possible imperfect (111) post-texturing orientation of the pyramid landscape, which could lead to local epitaxial growth. Consequently HR-TEM and STEM analyses were conducted on textured wafers, passivated with a-Si:H, which had or had not a thin a-SiC:H buffer layer at the a-Si:H/c-Si interface. Crystalline planes could be found at the a-Si:H/c-Si interface in several regions of the pyramid facets and grooves. However, in most cases, we could demonstrate that these belonged to the crystalline substrate and that these were not the result of local epitaxial growth. Moreover, most patterns could be found on buffered and unbuffered passivated samples. Nevertheless, in one particular case, an organization of crystalline planes protruding from the a-Si:H/c-Si into the a-Si:H bulk could be found, and a density profile conducted on STEM images showed that indeed, it is highly likely that these planes were epitaxially grown upon the a-Si:H deposition by PECVD. As a result, a model was proposed to describe the passivation of textured samples by a-Si:H, which takes into account not only the higher dangling bond density due to the larger surface when using textured samples, but also the presence of spread-out (100)-oriented regions on the surface that are not easy to detect. This model can be summarized by the following equation:

$$\boxed{\frac{1}{\Delta\tau_{eff}} = \frac{1}{\Delta\tau_{text}} + \frac{1}{\Delta\tau_{epi}}} \qquad (89)$$

Further annealing studies confirmed that local epitaxial growth must be present on unbuffered samples. However, spectroscopic ellipsometry measurements conducted on textured samples showed no difference in the optical properties of layers deposited with and without a thin a-SiC:H layer at the a-Si:H/c-Si interface. All these results confirm that this epitaxial growth is local and quite well spread out over the whole sample. For this reason, powerful characterization methods used for local analysis such as HR-TEM require a “lucky” sample positioning to be able to detect such subtle variations in the properties of a buffered and unbuffered sample. This led us to conclude that using a thin a-SiC:H layer is a very efficient and complementary method to detect local epitaxial growth on textured substrates. Moreover, it also allows for the assessment of the texturing quality by determining quite accurately $\Delta\tau_{text}$. Thus, one can situate how far a textured sample stands from the flat (111) reference in terms of dangling bond density. *Stegemann et al.*[232][233] have shown that a large fraction of small pyramids limits the effective lifetime by increasing the influence of the valleys and edges. Thus, reducing the fraction of small pyramids should lead to a simple transfer of an intrinsic a-Si:H layer optimized on flat (111) wafers. However, despite the optimization of our intrinsic a-Si:H layer on flat (111) wafers, we report that the transfer to pyramids with {111}-oriented facets is not at all straightforward.

The results obtained on simple symmetrical i/i stacks allowed us to move further. What if the improvement obtained on these could be implemented in SHJ solar cell precursors? Would it also improve their lifetimes and iV_{OC}s? How would it affect their performance once finalized? To answer these questions, the a-SiC:H thin buffer layer was introduced in our SHJ solar cell precursor architecture, occupying half of the usual intrinsic a-Si:H layer at the a-Si:H/c-Si interface. First, a study of its impact on flat (111) wafers showed that we should only expect a slightly worse collection, which would result in a lower FF. This was explained in terms of a higher band mismatch, due to the higher energy bandgap of our a-SiC:H alloy. Nevertheless, as expected, the addition of carbon in the intrinsic layer allowed for higher passivation levels on our textured SHJ solar cell precursors. Moreover, this was true regardless of the texturing recipe or wafer doping. Thanks to this, the final performances of our solar cells were enhanced. Even though the collection could be slightly impeded by the buffer layer, the interface was made much more abrupt. This resulted in an increase of the V_{OC} mainly, but also of the charge carrier collection.

While finalizing SHJ solar cells, ITO sputtering was required. PCD measurements showed that this step induced severe degradation, while being entirely recoverable. Indeed, most of the time, the effective lifetime would experience a 60 to 70 % drop while the iV_{OC} would decrease by a few tens of mV. While repeating these measurements at each stage of the SHJ solar cell precursor fabrication, we discovered that this degradation occurred while sputtering the TCO on the emitter side, where the (p)-a-Si:H layer is present. Indeed, sputtering on the BSF side induced no change in the effective lifetime nor in the iV_{OC}. The study of the impact of the i- and p-layer thickness showed that while the i-layer had a strong screening effect, the p-layer seemed “transparent” to this process. While the exact origin of this degradation remains unknown, this result pointed to a higher sensitivity of the emitter side, which we relate to two things: i) the higher hydrogen diffusion coefficient within the p-doped a-Si:H bulk and ii) Fermi-level related defect creation in the i-layer underneath. This led us to examine the possibility of the implementation of a p-layer gradient to minimize the losses that are naturally induced by the presence of a capping p-layer and those induced by the sputtering process. Simulation showed that this could only lead to a worse charge carrier collection and thus, to lower conversion efficiencies of finalized devices. However, SHJ precursors with a p-doping gradient were fabricated on flat (111) and textured substrates. In both cases, the effective lifetime and the iV_{OC}s improved. Moreover, the degradation upon ITO sputtering was reduced and the performances of the finalized device were enhanced. Consequently, 2x2 cm^2 SHJ solar cells with record efficiencies of 18.0% and 20.1% were fabricated on flat (111) and textured n-type wafers, respectively. These results open doors to a finer optimization of p-doped a-Si:H emitter stacks but also to the codevelopment of the TCO and p-layer to reduce damages induced by the sputtering step, whether these are related to the presence of the TCO or to the sputtering process *per se*.

5.2 Prospects

We believe our results can have an impact of paramount importance on the passivation of textured c-Si substrates with a-Si:H deposited by PECVD. Indeed, we passivated industrially anistropically-textured 20 Ω·cm 140 µm-thick n-type CZ wafers using our thin a-SiC:H thin buffer layer and the improvements obtained were striking. This indeed shows that not only can lab-scale texturing be imperfect in terms of average crystallographic orientation, but also industrial-grade wafers. This motivated us to file a patent based on this innovation, since an industrial application seemed possible. Moreover, an article based on these results will be submitted. When published, it could open new possibilities toward texturing and passivation technology codevelopment, for classical SHJ solar cells but also for IBC SHJ solar cells. However, even if our results pointed to local epitaxial growth on some parts of random pyramid landscapes and if there is little doubt of its existence, there is a need for the understanding of the exact cause of its occurrence. It is indeed likely to be caused by (100)-oriented imperfections of the texturing. However, there is no such evidence yet since the only regions involved yield crystalline planes on perfectly defined (111) facets. HR-TEM and STEM analyses are very local and, because of this it is hard to study the right area. Further studies would then be required on several regions of textured sample: junction between four neighboring pyramids, pyramid grooves with obvious imperfections detected by SEM, etc. Moreover, there is room for improvement of the a-SiC:H layer in terms of stoichiometry and thickness. Studies could be carried out with regard to this since a possible tuning of the bandgap could lead to a lower degradation of the charge carrier collection while ensuring a proper impediment of local epitaxial growth.

Studies on the passivation degradation upon TCO sputtering were carried out while working on obtaining SHJ solar cells with higher efficiencies. Because of this, stress was put more on what the study implied for the p-layer rather than on the phenomenon in itself. Indeed, the degradation being recoverable upon annealing, the main information we gathered from these experiments was that the p-layer was more sensitive and that it required all of our attention to move on to higher efficiencies. However, while obtaining our record efficiencies of 18.0 and 20.1% on flat and textured substrates, respectively, it became clear that just as texturing cannot be optimized without taking into account its impact on passivation, we are not able to choose the best p-layer without considering the impact of the sputtering process and of the TCO presence, as well. As a result, further studies should be carried out on this topic in order to understand the exact origin of the passivation degradation upon TCO sputtering (UV, ion bombardment, …) and the reasons that make the emitter side more sensitive to this process. The first problem was addressed recently by the Californian company SILEVO, as they managed to produce 25%-SHJ solar with great reproducibility. Moreover, *Demaurex et al.* have presented their results in 2014 at the IEEE conference in Denver, on the irreversible impact of the TCO deposition because of the work function mismatch with the p-layer underneath. One way to address the second problem would be to carry out comparative studies on p-type SHJ solar cells to see if there is any relation with the junction itself. Also, a study of the doping dependence on the degradation could be carried out to verify our hypothesis involving the hydrogen diffusion coefficient in doped a-Si:H. Comparing the boron incorporation by SIMS measurements with passivation degradation studies could yield interesting insights on this phenomenon.

In order to reach higher efficiencies, the ITO should be optimized in terms of mobility, transparency and work function, to improve light capture and charge collection. Moreover, we have found out recently a recipe for a (p)a-Si:H layer with a greater conductivity and a smaller boron incorporation. This shows that part of the boron we had so far in our p-layer was inactive and probably generating defects at the a-Si:H/c-Si interface. Using this new recipe should help us reach higher effective lifetimes and iV_{OC}s, while enhancing charge carrier collection. As a result, higher V_{OC}s should be reached with thinner p-layers, leading to lower absorption effects on the front side and thus to a J_{SC} increase. Consequently, higher efficiencies should be within reach.

One of the interesting results of part 3.2.2.e was the higher resilience of the a-Si:H/c-Si interface at high temperature, i.e., 100°C above the initial PECVD process temperature. This phenomenon should be investigated with great interest because it is unusual and opens doors to processes which normally require higher temperatures, such as screen-printing for example. On a more realistic scale, ZnO:Al could easily replace ITO as our TCO. Indeed, its deposition temperature usually exceeds 300°C to reach a sufficient level of crystallization and is found to be ideal at 320°C in terms of optical and electrical properties at LPICM[242]. With a resilience at 300°C, as depicted in Figure 3-73, the use of such a low-cost solution would be of great interest.

The next step would be to replace the doped a-Si:H layers by microcrystalline ones to increase the layer conductivity while lowering the optical absorption. Even though it has been reported that the harsh conditions in which microcrystalline silicon is usually deposited (high power, high H_2 dilution) can generate epitaxial growth in some regions of textured wafers, the presence of our thin a-SiC:H layer should prevent this from happening. As doped and intrinsic amorphous and microcrystalline oxide materials are currently being developed at LPICM, it would be even more interesting to use such materials, as the presence of oxygen could open doors for the transmission of a wider part of the light spectrum and thus to a higher J_{SC}.

Finally, the launching of the new PECVD cluster tool at LPICM allowed us to deposit passivating stacks (BSF and emitter) in separate chambers and with a much shorter pumping time (thanks to the presence of a load-lock). So far, only one SHJ solar cell has been fabricated after optimizing the deposition conditions of the intrinsic, n- and p-doped amorphous silicon layers. This result is quite promising (15.0%) since the thicknesses have not been optimized yet. When done, this would open doors for a transfer to textured substrates toward the fabrication of textured SHJ solar cells under much better conditions than the ones used for our 20.1% record cell, and thus, to higher efficiencies.

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Patent

1 patent filed on the 17th of November, 2014 (not published yet).

List of Acronyms

Acronym	Full name	Unit
a-Si :H	Hydrogenated amorphous silicon	–
a-SiC :H	Hydrogenated amorphous silicon carbide	–
BSF	Back-Surface Field	–
c-Si	Crystalline silicon	–
CBM	Conduction Band Minimum	eV
DSP	Double-Side Polished	–
E_F	Fermi energy	eV
E_{Fn}	Quasi-Fermi level for the conductionband	eV
E_{Fp}	Quasi-Fermi level for the valence band	eV
E_g	Energy bandgap	eV
E_i	Fermi energy at midgap	eV
E_U	Urbach energy	eV
FF	Fill factor	%
GDOES	Glow-Discharge Opical Emission Spectroscopy	–
HAADF	High-Angular Annular Dark Field	–
HR-TEM	High-Resolution Transmission Electron Microscopy	–
HWCVD	Hot-Wire Chemical Vapor Deposition	–
ITO	Indium-Tin Oxide	–
(i)a-Si :H	Intrinsisc hydrogenated amorphous silicon	–
in/in	Symmetrically passivated (n)a-Si :H/(i) a-Si :H/(n)c-Si/(i) a-Si :H/(n) a-Si :H stack	–
ip/ip	Symmetrically passivated (p)a-Si :H/(i) a-Si :H/(n)c-Si/(i) a-Si :H/(p) a-Si :H stack	–
iV_{OC}	Implicit open-circuit voltage	mV
J_{SC}	Short-circuit current	mA/cm^{-2}
LSM	Laser-Scanning Microscopy	–
KIno	3’NaOH+30’ KOH-IPA texturing	–
µc-Si :H	Hydrogenated microcrystalline silicon	–
(n)µc-Si :H	n-doped hydrogenated microcrystalline silicon	–
PCD	PhotoConductance Decay	–
PECVD	Plasma-Enhanced Chemical Vapor Deposition	–
(p)µc-Si :H	p-doped hydrogenated microcrystalline silicon	–
PV	Photovoltaics	–
RIE	Reactive Ion Etching	–
RF	Radio-frequency	–
R_S	Series resistance	Ω·cm^2
R_{Sh}	Shunt resistance	Ω·cm^2

RT	Room Temperature	°C or K
RTno	3’NaOH+45’ KOH/RenaTex texturing	–
sccm	Standard cubic centimeter	cm^{-3}·min^{-1}
SE	Spectroscopic Ellipsometry	–
SEM	Scanning Electron Spectroscopy	–
SRH	Shockley-Read Hall	–
STEM	Scanning Transmission Electron Microscopy	
τ_{eff}	Minority carrier effective lifetime	µs or ms
TEM	Transmission Electron Microscopy	–
V_{OC}	Open-circuit voltage	mV
VBM	Valence Band Maximum	eV

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ABSTRACT

This thesis is the result of the work carried out on the passivation of anisotropically wet-etched crystalline silicon by hydrogenated amorphous silicon deposited by low-temperature RF PECVD. Firstly, the (100) and (111) crystalline orientations were studied to understand the impact thereof on a-Si:H growth. Wet-chemical etching of crystalline silicon was then addressed in order to choose the best recipe to texture silicon wafers and thereby increase their light-trapping properties. Surprisingly, the deposition of a-Si:H on textured wafers was tested and passivation under our standard conditions was not evident at all. Indeed, we experienced huge losses in effective lifetime and implied V_{OC}. We could at first explain this difference by the larger surface and thus larger number of dangling bonds exhibited by textured wafers. However, we imagined that randomly distributed pyramid landscapes could be imperfectly defined in their natural {111} crystallographic orientation and that they rather contained a particular set of specific surface orientations. Such being the case, this would in turn foster particular growth modes locally. Consequently, we decided to use a method that is counter-intuitive for textured c-Si wafers in order to obtain a perfectly abrupt a-Si:H/c-Si interface. The improvements were striking and showed great reproducibility while HR-TEM/STEM analyses clearly indicated that the interface was made more abrupt indeed. This allowed us to procede towards our main goal: improving a-Si:H/c-Si heterojunction (SHJ) solar cell efficiencies on textured c-Si n-type wafers. A proper cleaning routine was defined, the cleanliness of the whole fabrication chain processes (no clean-room conditions) was optimized and adequate layer stacks were developed to enhance SHJ solar cells. As a consequence, a 2x2 cm² (n)c-Si HJ solar cell was fabricated with a conversion efficiency as high as 20.1% with a V_{OC} of 701 mV, a J_{SC} of 37.5 mA/cm² and a FF of 76.3%. This cell contains the two major improvements we have introduced in the conventional HJ solar cell architecture. Implementation of these improvements required a study of their impact on the SHJ solar cell resilience to TCO deposition and on their final J(V) characteristics. A new semi-industrial PECVD cluster tool was installed and new PECVD processes were defined to assess its potential for passivation studies and to check its reproducibility features. As a result, we obtained a 11.3 ms effective lifetime with a 734 mV implied V_{OC} on a symmetrical i/i stack.

Keywords: surface passivation, crystalline silicon, wet-chemical texturing, amorphous silicon, heterojunction, PECVD

RÉSUMÉ

Cette thèse est le résultat de travaux menés sur la passivation du silicium cristallin texturé par voie chimique, par le silicium amorphe hydrogéné déposé par RF PECVD à basse température. Tout d’abord, les orientations cristallines (100) et (111) ont été étudiées pour comprendre leur impact sur la croissance du a-Si:H. Ensuite, la gravure du silicium par voie humide a été explorée pour définir la recette de texturation du silicium cristallin la plus adaptée en vue d’améliorer ses propriétés de piégeage optique. La croissance du a-Si :H sur des wafers texturés a été étudiée et, à notre grand étonnement, leur passivation dans nos conditions standard n’a pas été évidente au premier abord. En effet, cela est passé par des pertes importantes en termes de temps de vie et de V_{OC} implicite. Cela pouvait être tout d’abord expliqué par la surface développée plus importante du substrat de silicium après texturation. Cependant, nous avons imaginé que la surface du silicium cristallin pouvait être imparfaitement définie dans son orientation naturelle faite de plans {111} et qu’elle pouvait au contraire contenir une distribution d’orientations cristallines. Cela aurait pour conséquence de favoriser localement des modes de croissances particuliers. Par conséquent, nous avons décidé d’utiliser une méthode contre-intuitive pour obtenir des interfaces a-Si :H/c-Si abruptes lors de la passivation de wafers c-Si texturés par voie chimique. Les améliorations ont tout de suite été très nettes avec une grande reproductibilité tandis que des analyses HR-TEM/STEM ont démontré l’obtention d’une interface plus abrupte. Cela nous a permis de poursuivre notre objectif principal fixé : augmenter le rendement de cellules solaire à hétérojonction a-Si :H/c-Si (SHJ) sur wafers c-Si texturés de type n. Une procédure de nettoyage chimique des wafers adaptée à notre laboratoire a été définie, la propreté de la chaîne complète de fabrication a été optimisée et des couches de a-Si :H adéquates ont été développées pour améliorer les performances de cellules solaires SHJ. Par la suite, une cellule solaire de 2x2 cm² a pu être fabriquée avec un rendement de 20.1%, un V_{OC} de 701 mV, un J_{SC} of 37.5 mA/cm² et un FF de 76.3%. Cette cellule contient les deux améliorations majeures que nous avons introduites dans l’architecture SHJ. Leur implémentation a requis l’étude de leur résistance aux procédés de dépôts du TCO et de leur impact sur les caractéristiques J(V) finales. Dans cette quête vers les hauts rendements, un nouveau réacteur semi-industriel de type cluster PECVD a été installé. De nouveaux procédés PECVD ont été définis pour à la fois estimer ses capacités pour les études de passivation et également vérifier ses caractéristiques de reproductibilité. Par la suite, un temps de vie de 11.3 ms a pu être obtenu avec un V_{OC} implicite de 734 mV sur un stack symétrique i/i sur substrat lisse (111).

Mots-clés: passivation de surface, silicium cristallin, texturation par voie chimique, silicium amorphe, hétérojonction, PECVD