STUDY OF IN-PLANE SILICON NANOWIRES OBTAINED VIA A SOLID-LIQUID-SOLID GROWTH PROCESS AND THEIR SELF- ORGANIZATION FOR ELECTRONIC APPLICATIONS

Zheng Fan

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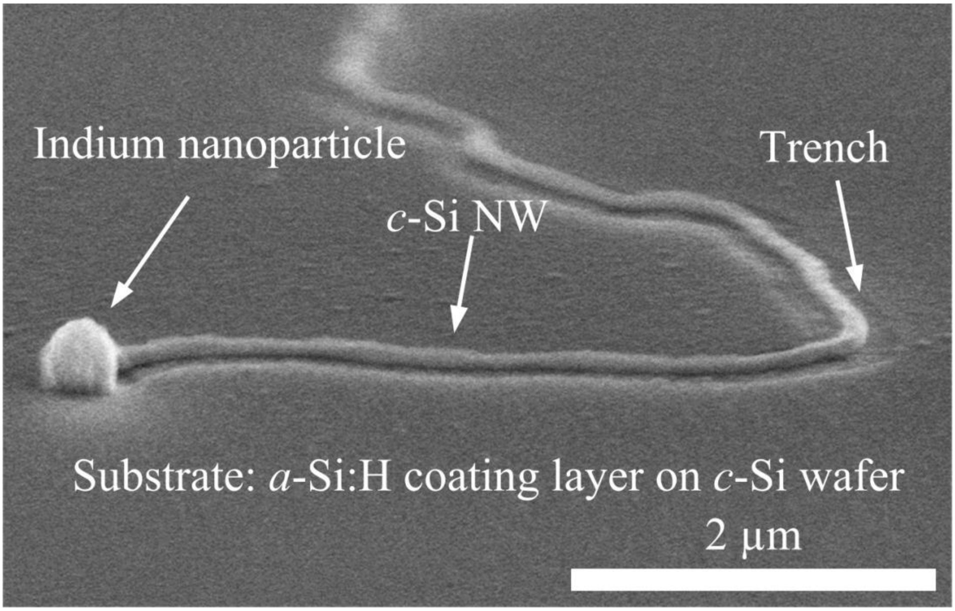
Study of in-plane silicon nanowires obtained via a solid-liquid-solid growth process and their self-organization for electronic applications



FAN Zheng

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Spécialité Physique / Science des Matériaux

par

FAN ZHENG

STUDY OF IN-PLANE SILICON NANOWIRES OBTAINED VIA A SOLID-LIQUID-SOLID GROWTH PROCESS AND THEIR SELF-ORGANIZATION FOR ELECTRONIC APPLICATIONS

Soutenue le 21 décembre 2015 à l'Amphi Becquerel devant le jury composé de :

PROF. PERE ROURA GRABULOSA	UDG	Rapporteur
DR. FRANK GLAS	LPN	Rapporteur
DR. FRANCK FORTUNA	CSNSM	Examinateur
DR. SOPHIE BOUCHOULE	LPN	Examinateur
PROF. PERE ROCA i CABARROCAS	LPICM	Directeur

男兒到死心如鐵
看試手
補天裂

à mes chers parents et Nan

献给我的父亲母亲与楠

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All started from the summer 2012, when my Ph.D. subject of CSC-Groupe d'Ecole Centrale was administratively cancelled and I was busy looking for an alternative one in a French lab. It seemed to be quite late and most of the posted theses were not available anymore at that time. After throwing a large amount of application e-mails into the internet, I received a less negative response from Prof. Pere Roca i Cabarrocas in Laboratoire de Physique des Interfaces et des Couches Minces (LPICM, Ecole Polytechnique). No surprising on the regretting phrases, however, in the attachment there was another Ph.D. proposal on in-plane solid-liquid-solid silicon nanowire™, and one *Phys. Rev. Lett.* . I had never heard of nanowires, neither the *Phys. Rev. Lett.* However, a huge amount of technologies were listed in the proposal: PECVD, sputtering, evaporation, lithography, plasma etching, SEM, as well as transistor fabrication and electrical characterization, etc. So, I decided to come. Thank you Prof. Yu for the phone interview and for introducing such a amazing and chanllenging Ph.D. subject.

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FAN Zheng

à Palaiseau

2016/04/20

Contents

INTRODUCTION

❑ NANO-SCALE SEMICONDUCTORS

❖ MORE MOORE AND MORE-THAN-MOORE

The method of controlling the electric currents by a three-terminal device proposed by J. E. Lilienfeld in 1930 opened the era of solid state semiconductor electronics [1], and J. S. Kilby published the miniaturized electric circuits for the first time in 1964 [2], which is nowadays known as integrated circuits (ICs) for logic devices like central computing units (CPUs) and memories, whose building blocks are based on complementary metal-oxide-semiconductor (CMOS) technology. Since then, great efforts have been made on integrating more CMOS of decreasing dimensions on a single chip, in order to keep low manufacturing cost and meanwhile maintain low power consumption with an increasing device performance, called CMOS scaling or miniaturization. During the past several decades this technology evolution was directed by the Moore's law (the number of transistors on a chip doubles every 18 to 24 months, as shown in Figure 1) and now currently almost approaches its limit. Novel channel materials and gate, dielectrics, supported by substrate engineering, novel device architectures with multi-gate engineering, advanced doping, as well as etching and lithography technologies are being developed for boosting the Moore's law, which is called "More Moore". The evolution of corresponding technologies is summarized in Figure 2.

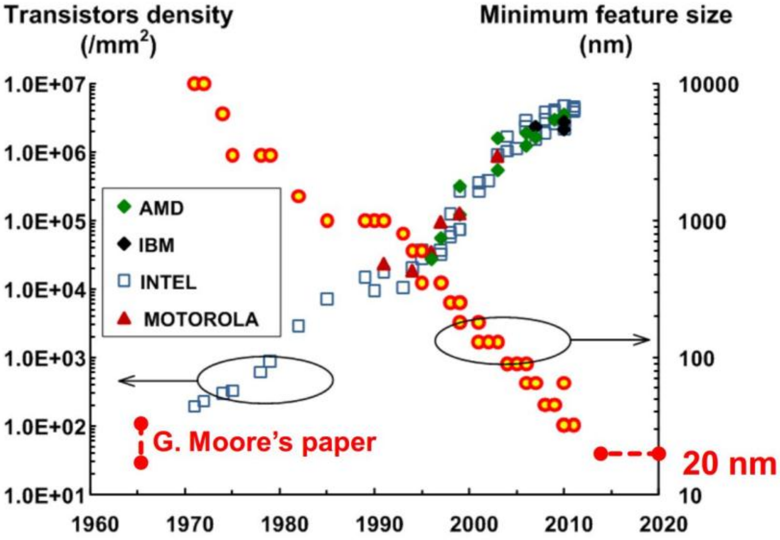


Figure 1 Moore's Law 1965-2011, from [3]

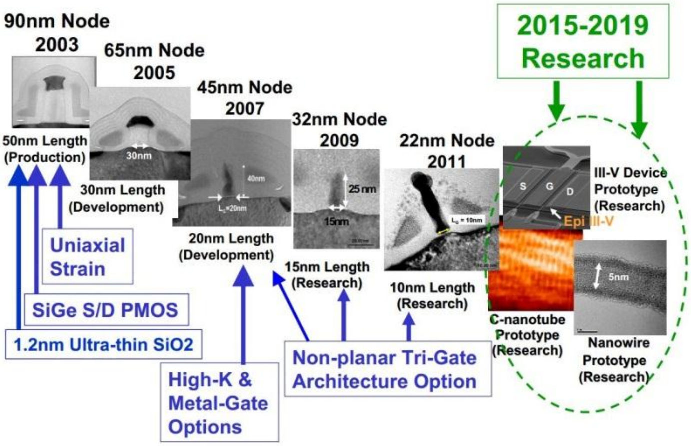


Figure 2 Advanced CMOS technology in the transistor scaling roadmap, source from Robert Chau, Intel Corporation [4].

Moreover, semiconductor industry encounters new challenges, with the requirements of integrating non-digital (e.g. analogue) functions in a multi-functional system based on CMOS technology, including radio frequency (RF) components, power management subsystems, passive components, biochips, sensors, actuators, microelectromechanical systems (MEMS), etc. This developing direction of functional diversification is known as "More-than-Moore". Figure 3 shows the diagram of this dual trend of More Moore (miniaturization of the digital functions) and More-than-Moore (functional diversification) from the International Technology Roadmap for Semiconductors (ITRS) [5].

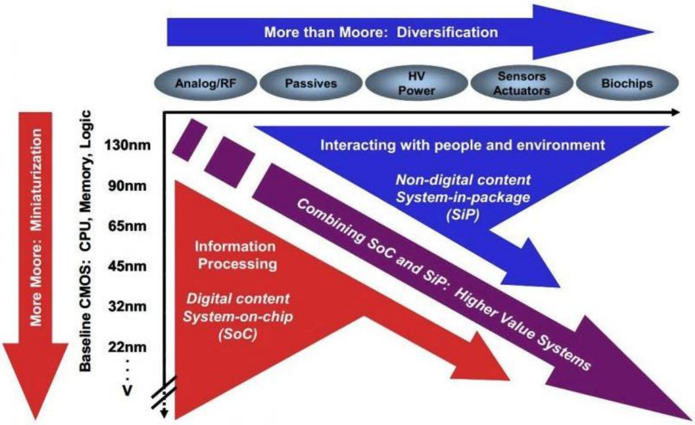


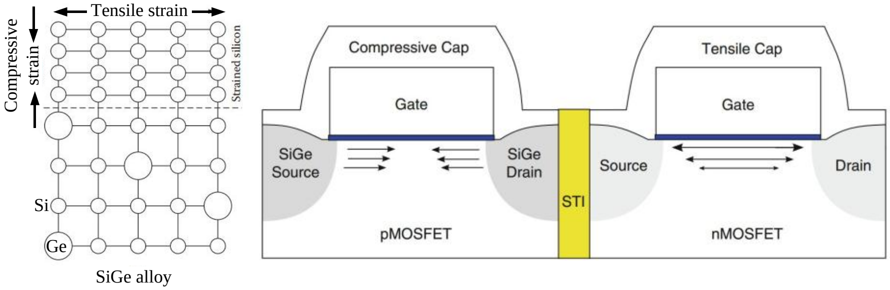
Figure 3 Diagram of a dual trend of More Moore (miniaturization of the digital functions) and More-than-Moore (functional diversification) from International Technology Roadmap for Semiconductors (ITRS), from [5].

❖ STRAIN ENGINEERING

Figure 4 shows the strain engineering technolgoies that scale transistors down to the 90 nm node. Instead of introducing new materials like III-V compounds, strain engineering realizes the enhancement of device performance (electron and hole mobility) by mechanically stressing the channels (Si, Ge or SiGe alloy) of MOSFETs, including substrate-induced (or global) and process-induced (or local) technologies.

Substrate-induced strain engineering describes a process of introducing a $Si_{1-x}Ge_x$ layer between the channel layer and the substrate (normally Si), so that the top channel layer can be stretched due to its lattice mismatch with the $Si_{1-x}Ge_x$ layer. Figure 4.a shows the schematic representation of strained Si thin layer on SiGe alloy.

Another strain engineering technology is derived from the silicidation at the source and drain regions, where the channel region is stressed by the nitrides at the two sides. So it is called local or process-induced strain engineering. Later on, selective epitaxial growth of SiGe alloys embedded in the source and drain region was developed as the main technology in semiconductor industry. The advantage of local strain engineering is that the strains in P- and N- channels can be manipulated independently. Figure 4.b shows the schematic representation of process-induced strain engineering by selective epitaxial growth of SiGe alloy embedded in the source and drain regions, which forms compressive and tensile strains in p- and n- channels, respectively.



(a) Substrate-induced strain engineering

(b) Process-induced strain engineering

Figure 4 Schematic representation of substrate-induced strain engineering (a) [6] and process-induced strain engineering (b) [7].

❖ HIGH-*K* DIELECTRICS AND METAL GATES

For conventional CMOS technology, SiO_2 and heavily doped polycrystalline silicon gate are the standard materials for gate stack engineering. In the transistor scaling roadmap, the standard configuration shifts to metal gate/high-k dielectric, as shown in Figure 5.

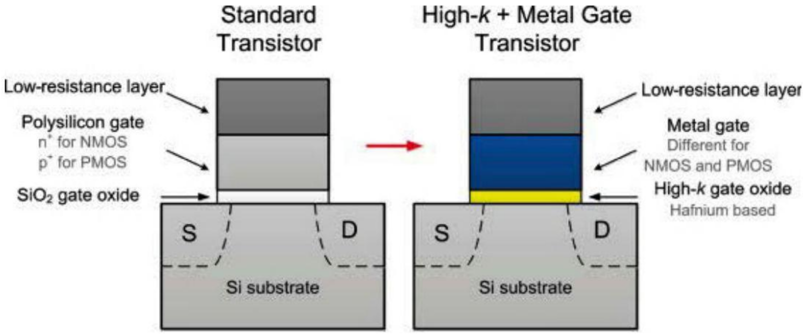


Figure 5 Schematic representation of gate stack configurations of poly-Si/SiO$_2$ (left) and metal gate/high-k dielectric [8].

Continuous thickness reduction of SiO$_2$ dielectrics will cause detrimental gate leakage current. In order to obtain high device performance while maintaining low power consumption, high-*k* dielectrics/metal gates are introduced. High-*k* dielectrics are a group of metal oxides with dielectric constant *k* larger than 7 (the value of Si$_3$N$_4$). Other requirements of high-*k* dielectrics are: (i) large bandgap (>5 eV) in order to establish large band offset with Si to avoid Si-dielectrics conduction due to Schottky emission of electrons and holes into the oxide bands; (ii) thermodynamic stability at the Si/dielectrics interface to avoid interfacial reaction and SiO$_2$ formation; (iii) high thermal stability with high crystallization temperature; (iv) high quality thin film with respect to uniformity, conformal profile and density. Commonly considered high-k dielectrics include Al$_2$O$_3$, HfO$_2$, Ta$_2$O$_5$, etc. The replacement of heavily doped poly-Si is due to the limitations in doping density, which result in the depletion of poly-Si gate when the gate stack is biased in inversion and lowering of the drive currents. Besides, poly-Si is not thermodynamically stable when put in contact with high-*k* dielectrics. Hence, metal or metal compound gates are proposed as new materials in gate stack engineering. As pure metals can react with dielectrics (e.g. Ta, Ti, Hf, etc.), while other inert ones (e.g. Ni, Pd, Pt, etc.) have difficulty in chemical bonding at metal/dielectrics interface, metallic alloys, and metal nitrides turn to be alternative materials. Metallic alloys (e.g. Ta-Pt) provide good thermal stability and adjustable work function by modulating the atomic composition fraction of two metals with different work functions. Metal nitrides, like TiN, WN, HfN, etc., are also considered as gate materials, and their work function can be tuned by the nitrogen composition. However, the range of achievable work function is not broad enough to be adaptable to both p- and n- type channels. Metal silicides are considered as the most suitable gate material as their adjustable work functions can suit both p- and n- type channels and the silicidation process (i.e. metal-Si reaction) is compatible with the CMOS technology, for example Ti silicide, Pt silicide, Ni silicide, etc.

❖ PLANAR VS. NON-PLANAR ARCHITECTURES

In the continuous scaling in CMOS technology, a non-planar architecture is considered as the most possible route in the More Moore roadmap. However, the competition with advanced SOI planar technology is challenging.

Planar transistor technologies can be classified as: (i) conventional bulk technology, where Si channels are formed in bulk Si; (ii) Silicon-On-Insulator (SOI) technology, where Si channels are located in the thin layer of Si (called Body) over a buried oxide insulator (called BOX) on Si substrates. If the Si Body is thicker than its depletion depth, a neutral region will exist between source and drain, called Partially-Depleted SOI (PD-SOI), the normal thickness of Si is around 50~90 nm; if the Si Body is ultra-thin, the entire layer can be depleted, called Fully-Depleted SOI (FD-SOI), the normal thickness is around 10~20 nm. In comparison with bulk Si technology, SOI has advantages like low junction capacitance and leakage, low operating power, better electrostatic control to reduce short channel effects, etc. [9]

Another competing technology, FinFET, relies on non-planar technologies for enabling the multi-gate engineering. A 3-D channel, shaped as a fin, is fabricated on bulk Si substrate, so that the gate stack layers can be coating the top and both sides of the fin channel. This dual gate architecture provides optimized electrostatic control and thus improves the current control of transistor. Besides, variant multi-gate architectures are proposed as gate engineering progresses, such as Π gate, Ω gate and even gate-all-around (GAA) [10]. However, FinFET technology encounters challenges like process complexity (e.g. uniform doping technology) and subsequent performance variation. Figure 6 shows the schematic representation of FinFET transistor (left) and FD-SOI transistor (right).

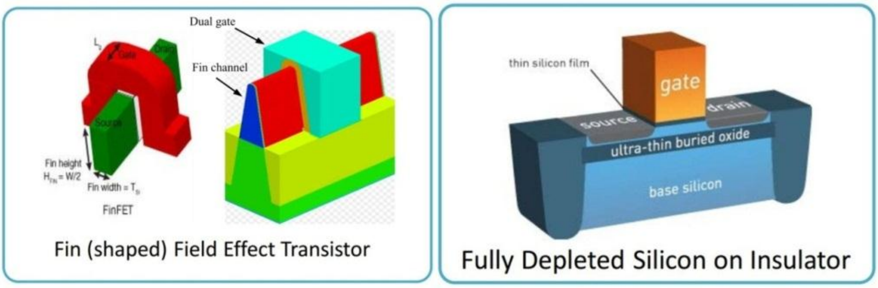


Figure 6 Schematic representation of FinFET transistor (left) and FD-SOI transistor (right) [11].

❖ CONTRIBUTION OF ONE-DIMENSIONAL SEMICONDUCTORS TO MORE MOORE

One solution for future transistors based on CMOS technology is FinFET on SOI, by combining the SOI and FinFET technologies. Silicon nanowires (SiNWs), as a type of one-dimensional (1-D) semiconductor nanostructure, are expected as an available channel candidate in this novel architecture, which can be lying on the substrate, or vertically standing on it. Figure 7 represents selected examples of SiNWFETs: (a, b) show the architecture and SEM image of a SiNW lying on SiO_2 insulator, with highly doped Si substrate as bottom gate [12]; (c, d) show the architecture and cross-sectional TEM image of junctionless SiNWFETs, where lateral flat SiNWs (or nanoribbons) are fabricated by lithography patterning and plasma etching (top-down method) on SOI substrate and highly doped by ion implantation, with a poly-Si Π gate on top [13]; (e, f) show the architecture and SEM image of a lateral SiNW suspended on a SOI substrate fabricated by a top-down method, with poly-Si gate-all-around structure [14]; (g, h) show the architecture and cross-sectional TEM image of a vertically (vapour-solid-liquid-grown) SiNW, with bottom source, top drain and gate-all-around structure [15]. Moreover, NW heterostructures broaden the range of electronic applications, core-shell heterostructures (e.g. SiGe, GaN/AlN, etc.) have been demonstrated for the high performance quantum well (QW) FET [16][17] or optoeletronics [18]. Besides SiNWs, other one-dimensional semiconductors like Ge [19], group III-V [20]-[25], III-nitride (e.g. GaN [26]), oxide (e.g. ZnO [27], SnO_2 [28]) and carbon nanotubes (CNTs) [29][30] are also explored as the channel candidates for future electronics.

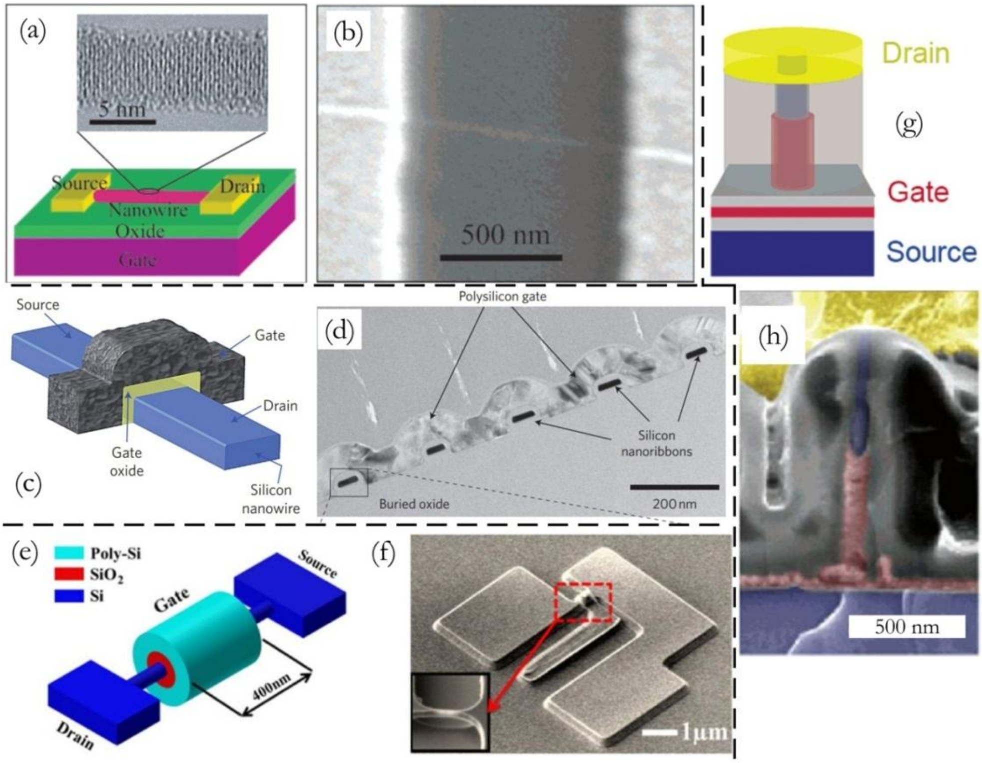


Figure 7 Examples of SiNWFETs: (a) architecture of bottom gate lateral SiNWFET and the top-view SEM image (b); (c) architecture of Π gate lateral SiNWFET and the cross-sectional TEM image (d); (e) architecture of gate-all-around lateral SiNWFET and the top-view SEM image (f); (g) architecture of gate-all-around SiNWFET and the cross-sectional TEM image (h).

❖ CONTRIBUTION OF ONE-DIMENSIONAL SEMICONDUCTORS TO MORE-THAN-MOORE

Besides their applications in logic electronics, 1-D semiconductors have optical, thermal, mechanical and magnetic properties, which allow their applications in photonics, biosensors, piezotronics, energy conversion and storage, etc.

Biosensors based on SiNWFETs have been reported, where the surface of a SiNW is functionalized by modifying the receptors, so that it can be recognized by the target molecules (e.g. gas, ions, proteins, DNA, etc.) through strong binding affinity. As a consequence an electrical signal arises when a biological/chemical event takes place on the surface of the channel [31]. Moreover, SiNWs can also be used in energy conversion and storage applications, like photovoltaics based on radial junction solar cells, SiNW anodes as an electrochemical energy storage material, or in thermoelectric conversion applications [32]-[34]. III-V NWs and their heterostructures have been demonstrated as novel semiconductor materials for nano-scale photodetectors, waveguides, microcavity lasers and light emitting diodes (LEDs), etc. [35][36] Moreover ZnO NWs are applied in nanogenerators, piezotronics and piezo-photonics due to their strain-induced piezopotential property [37].

❖ FABRICATION AND INTEGRATION OF ONE-DIMENSIONAL SEMICONDUCTORS

In general, the methods for producing 1-D semiconductor nanostructures can be classified into two families: i) **Top-down methods**, based on a physical and/or chemical **etching** process of tailoring the bulk substrates into NWs laterally lying or vertically standing on the substrates; (ii) **Bottom-up methods**, which rely on **growing** processes catalysed or self-catalysed by collecting and organizing atomic sources (precursors) from a vapour, liquid or even solid phase, assisted by thin film deposition techniques such as chemical vapour deposition (CVD), plasma-enhanced chemical vapour deposition (PECVD), metalorganic chemical vapour deposition (MOCVD), molecular beam epitaxy (MBE), or via solution-based synthesis methods. The most popular bottom-up method is vapour-solid-liquid (VLS) growth process, based on the interaction of liquid metal droplets and atomic precursors from vapour phase and transforming them to solid crystalline phase. A variant of the VLS method is vapour-solid-solid (VSS) mode, where the metal catalysts are in solid phase. In this thesis, we will introduce another variant growth mode, called in-plane solid-liquid-solid mode [38], where liquid metal droplets (indium) move on substrates with a pre-coated layer of *a*-Si:H on top, absorb Si atoms from the *a*-Si:H layer at their advancing edge, and precipitate *c*-SiNW at their receding edge [39]. Numerous review articles on the growth methods and properties of semiconductor nanostructures have been published before [40]-[46], and a brief review of bottom-up growth techniques related with our growth method is presented in Chapter 2.

In order to integrate 1-D semiconductors into nano-scale systems, it is of prime importance to organise or assemble them in an efficient way. Advanced lithography techniques (e.g. e-beam lithography and nanoimprint lithography) allow the fabrication of ordered lateral and vertical 1-D semiconductor arrays via top-down method, assisted by anisotropic dry etching techniques (e.g. inductively coupled plasma reactive ion etching, reactive ion beam etching, etc.). For vertically grown 1-D semiconductor arrays, selective area epitaxial growth [47] is the most favourable way, in which the catalysts are pre-defined by the same high resolution lithography techniques. On the other hand, challenges still remain on ordering lateral arrays of 1-D semiconductors. As most 1-D semiconductors are vertically standing on the substrates, lying them down on the pre-designed positions was a most common approach in the early days, called "growth-and-place" method. Later on, the alternative "growth-in-place" method started to be considered, where the growth of semiconductor NWs or CNTs can be guided on a structured substrate with features such as nano-facets (atomic steps) or nano-channels. More information can be found in [48]. Also a brief review relating to this thesis is introduced in Chapter 4.

❑ THESIS STRUCTURE

This is the first Ph.D. thesis on systematic study of in-plane silicon nanowires produced via a solid-liquid-solid (SLS) growth mode and of their self-organisation for FET application.

In Chapter 1, we first present the synthesis process of in-plane SiNWs via a solid-liquid-solid mode. Principles of thin film deposition, characterization and micro/nano fabrication technologies are also introduced.

In Chapter 2, we systematically study the formation process of indium catalyst nanoparticles: H_2 plasma treatment of indium catalyst thin films on heated substrates. Two types of catalyst source thin films are studied: (i) evaporated discontinuous In thin films, and (ii) sputtered ITO thin films. A series of experiments are designed, which reveal the different physical and chemical processes taking place on the two types of films under *ex-situ* SEM observation and analysis. The deep understanding of In NPs formation is fundamental for our stratetgy of localizing in-plane SiNWs for self-organisation.

In Chapter 3, we consider the solid-liquid-solid growth mode of in-plane SiNWs from three aspects: (i) metal-induced crystallization of amorphous silicon, (ii) spontaneous motion of liquid droplets, and (iii) heterogeneous nucleation and crystal growth from solution. By decomposing the growth process into three corresponding episodes in loop, we manage to reconstruct the entire scenario of the growth of in-plane SiNWs. Further geometric investigation of the in-plane solid-liquid-solid system under *ex-situ* SEM observation and analysis supports the proposed growth mechanism and reveals the relationship between SiNW diameters, In NPs diameters and *a*-Si:H thickness. This improvement on understanding the growth mechanism provides principles for optimizing the guided growth strategy of in-plane SiNWs. Moreover, in order to further understand the growth mechanism, the structural properties of *a*-Si:H and other metal catalyst candidates (Sn, Au) are investigated. This provides strategies for lowering the growth temperature and selecting metal catalysts for GeNWs, respectively.

In Chapter 4, we propose a strategy for self-organising in-plane SiNWs, which includes two aspects: (i) a guided growth method for aligning in-plane SiNWs, and (ii) a technique of forming In NPs on buried ITO sidewalls required for localizing in-plane SiNWs. Based on the mechanisms of In NPs formation on planar ITO surface and SiNWs growth on planar substrate, we elaborate the guided growth mechanism and sidewall In NPs formation mechanism, which is expected to make this self-organising strategy reproducible and reliable. Besides, the fabrication flow chart and key factors in it are elaborated.

In Appendix A, we provide the heated substrate temperature calibration of the PECVD system for SiNWs growth (PLASFIL).

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1 FUNDAMENTALS AND EXPERIMENTAL TECHNIQUES

CONTENTS

1.1 IN-PLANE SILICON NANOWIRES VIA A SOLID-LIQUID-SOLID GROWTH MODE

Based on thin film techniques, in-plane silicon nanowires are synthesized in PLASFIL, a PECVD system in which the plasma is ignited by applying a RF power (13.56 MHz). Figure 1.1 shows a schematic representation of the PLASFIL system. The bottom electrode is grounded and the upper electrode is connected to the RF power generator through an impedance matching box, which is used to minimize the power reflection from the plasma by equalizing the impedances of the external power source (Z_{RF}) to that of the plasma (Z_{plasma}). The series connected capacitor within the impedance matching box is called blocking capacitor, and this mode of sustaining the plasma is thus named capacitively coupled plasma (CCP). Resistive heaters are integrated with each electrode to heat them up to a nominal temperature of 600°C. The vacuum system consists of a primary oil-sealed mechanical pump for approaching low vacuum background (10^{-5}~10^{-4} mbar) and with a turbomolecular pump for high vacuum (above $5x10^{-6}$ mbar). A Pirani gauge (thermal conductivity gauge) and a Penning gauge (ionization gauge) are integrated in the system for monitoring the low and high vacuum pressure, respectively. During the plasma process, gases are introduced from inlet lines, and non-reacted gases or volatile gaseous reactants are pumped out of the chamber. A butterfly valve is, connected between the chamber and rector pump, for adjusting the total gas pressure thanks to adaptative pressure controller. The spatial distribution of the average DC potential voltage between the two parallel electrodes is also shown in Figure 1.1.

The synthesis of in-plane SiNWs is catalysed by liquid indium nanoparticles (In NPs). The source of indium (In) can be evaporated In or sputtered indium tin oxide (ITO) thin films, which experience the same process steps in PECVD system: (i) H_2 plasma treatment at 300°C, (ii) *a*-Si:H coating at 150°C, (iii) annealing at 450°C in vacuum or in the presence of H_2. Figure 1.3 and Figure 1.4 show the flow charts and the corresponding SEM images of the in-plane SiNWs fabrication process based on evaporated In or sputtered ITO thin films as catalyst source, respectively. The difference between evaporated In and sputtered ITO thin films is detailed in Chapter 2.

The growth of in-plane SiNWs includes the diffusion of Si atoms into liquid In NP from its front side and their precipitatation in the form of a *c*-Si nanowire, as illustrated in Figure 1.2. Therefore, it is a solid-liquid-solid growth process. The growth mechanism is detailed in chapter 3.

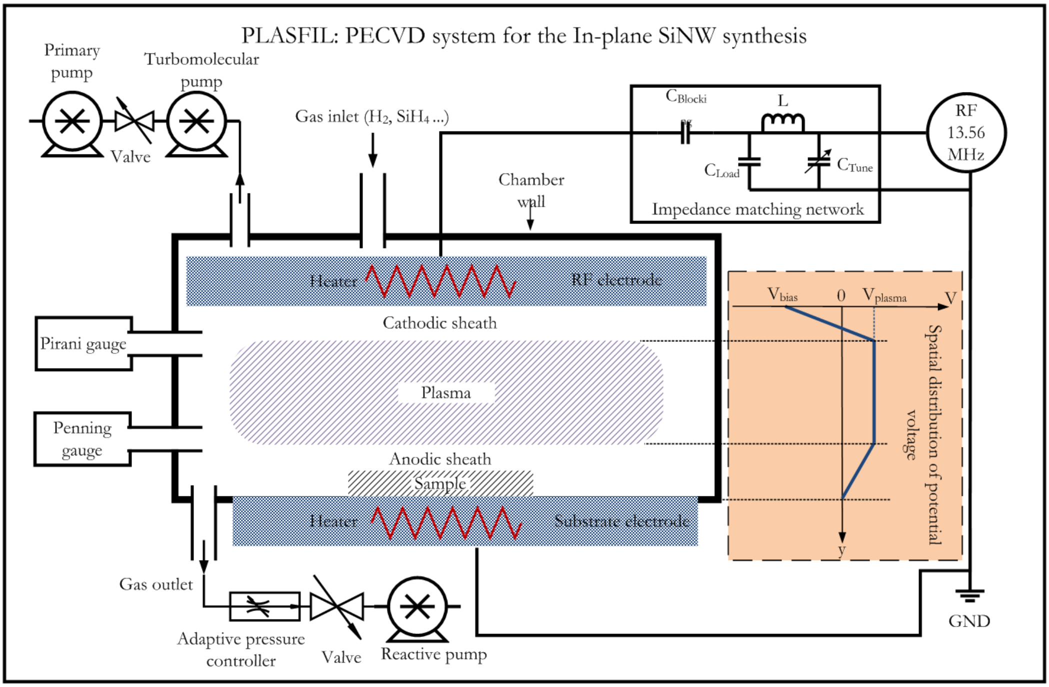


Figure 1.1 Schematic representation of PLASFIL: the PECVD system for in-plane SiNWs synthesis.

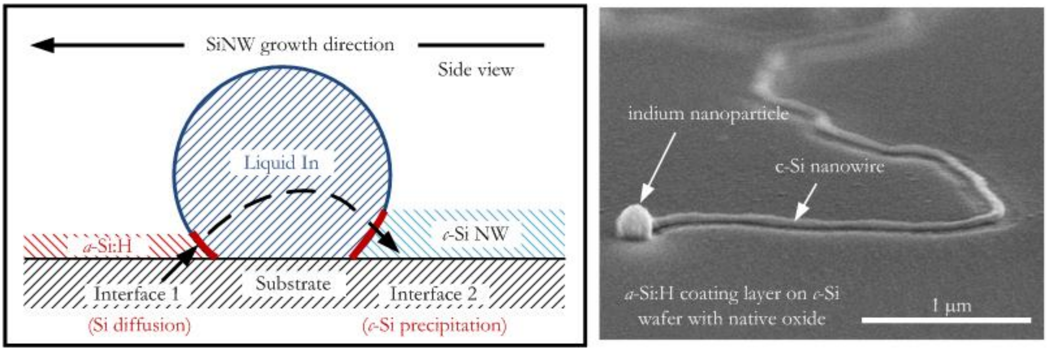


Figure 1.2 Schematic representation and SEM image of in-plane SiNWs obtained via a solid-liquid-solid mode.

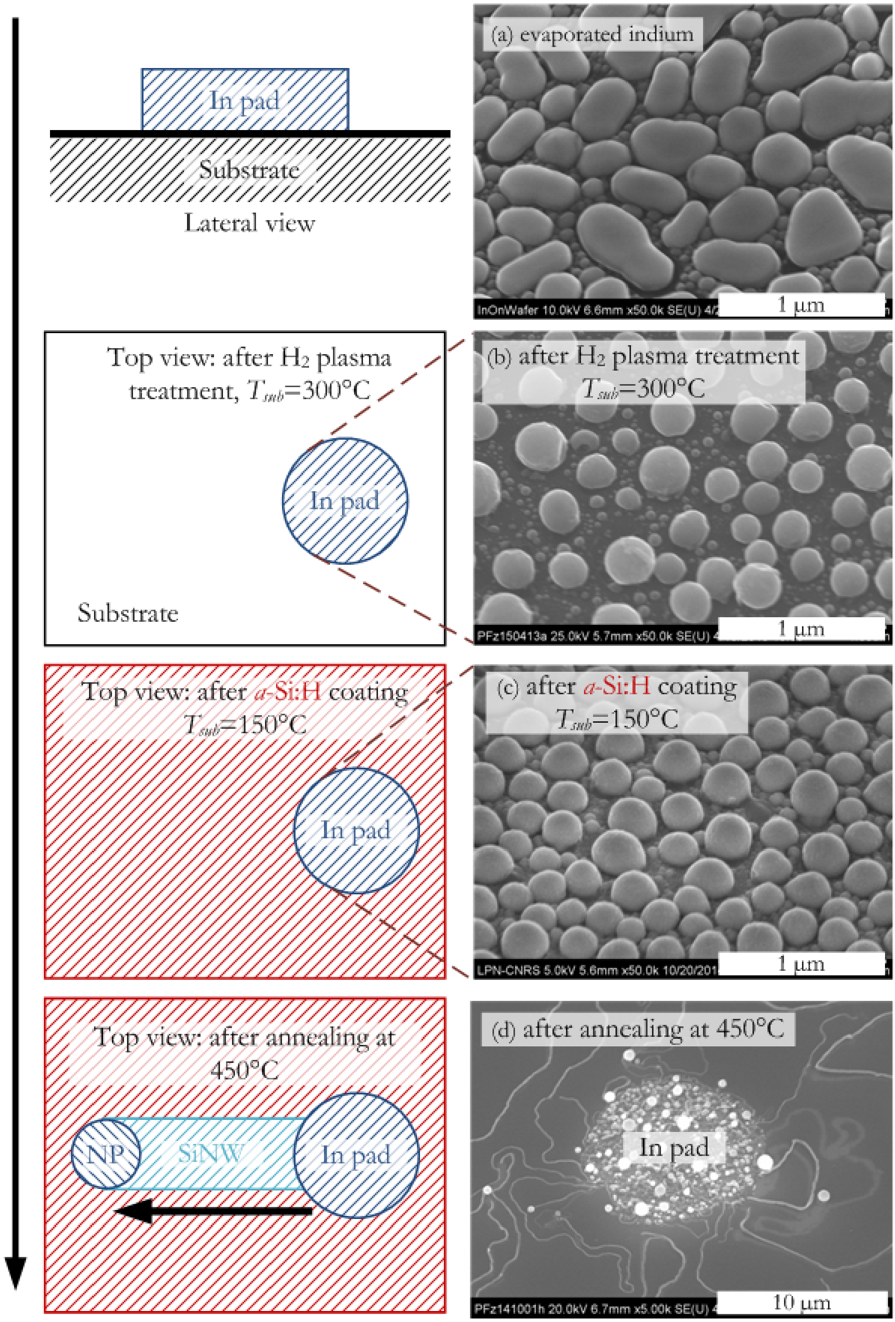


Figure 1.3 Flow chart of in-plane SiNWs synthesis with evaporated In as a catalyst source. Note that the variation of density and size of In NPs in the four images may be due to the fact that they were not taken at the same position on the same sample.

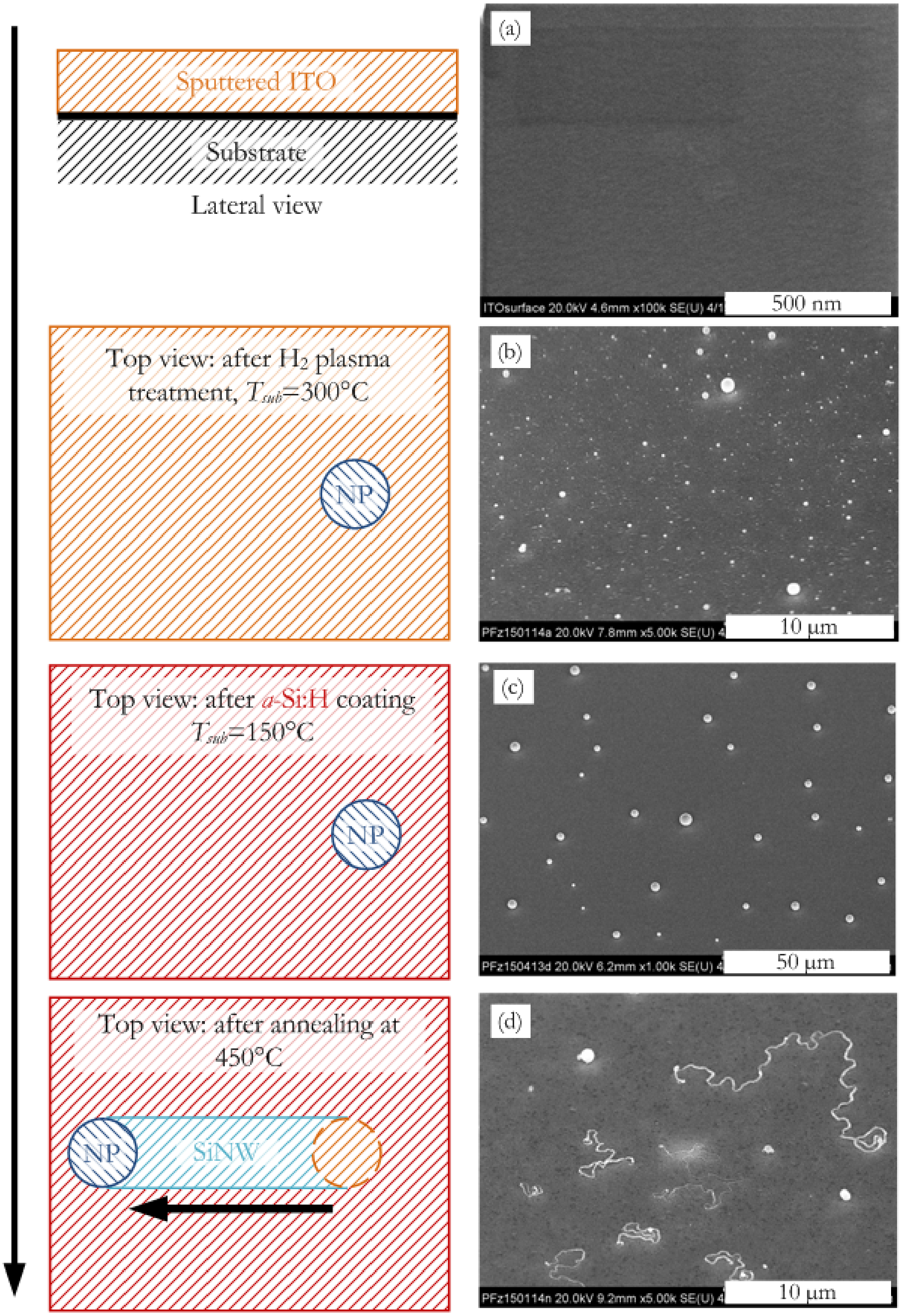


Figure 1.4 Flow chart of in-plane SiNWs synthesis with sputtered ITO as a catalyst source. Note that the variation of density and size of In NPs in the four images may be due to the fact that they were not taken at the same position on the same sample.

1.2 THIN FILM DEPOSITION AND CHARACTERIZATION

As mentioned in 1.1, the synthesis of in-plane SiNWs is based on thin film process. In this section, the thin film deposition and characterization techniques utilized in this thesis are presented.

1.2.1 PLASMA-ENHANCED CHEMICAL VAPOUR DEPOSITION (PECVD)

Plasma-enhanced chemical vapour deposition (PECVD) is widely used for the growth of dielectric films (i.e. Si_3N_4 and SiO_2) [1], *a*-Si:H [2], *μc*-Si:H [3], and *c*-Si epitaxy [4]. The schematic representation of a RF-PECVD system has been shown in Figure 1.1. It is a sort of chemical vapour deposition (CVD) reactor, where single or mixed gaseous compounds are partially dissociated and the dissociation products (called reactive species or radicals) diffuse to the substrate and form a thin film on it due to reactive chemical process.

Take silane (SiH_4) in a PECVD system for instance. Radio-frequency power, as an electrical excitation mode, provides energy to electrons which will partially ionize the SiH_4 gas at a low pressure (a few tens of mTorr to a few Torr). The electrons with low mass are accelerated by the electrical field between the two parallel plate electrodes and gain enough energy to dissociate SiH_4 gas via electron-molecule collisions. The products of the reaction can be various, including positive and negative ions, radicals, electrons, photons, etc. Figure 1.5 shows the probability manifold for the SiH_4 dissociative species due to a 70 eV electron impact, deduced from mass spectrometry measurements.

At the initial stage of plasma establishment, low mass/high energy electrons are rapidly evacuated to the reactor walls leaving behind positively charged ions.This results in the formation of a space charge region where an electrical field confines the negative ions and electrons, while accelerating the positive ions (ion bombardment). The space charge region between the plasma bulk and the chamber wall has a low electron density which results in a low level of gas excitation. As a consequence it appears dark and is called sheath. The type of interaction between plasma species and the substrate depends on the charge of the species, as illustrated in Figure 1.6.

Figure 1.7 depicts the standard model of *a*-Si:H thin film deposition, where SiH_3 radicals, as the dominant precursors at low pressure, arrive on a H-terminated surface, physisorb (as low temperature in PECVD system cannot activate the Si-H bond breaking) and diffuse on the surface to grow the film due to various chemical reactions, such as desorption of SiH_3, recombination with other SiH_3 to produce Si_2H_6 molecules, and abstraction of H atoms to produce SiH_4 molecules, which results in dangling bonds on the surface for the following SiH_3 radicals to form chemical bonds and thin film growth.

Other excitation modes can also provide energy to dissociate the gas precursors and sustain the chemical reactive system for thin film growth, like thermal or photonic activated CVD [5].

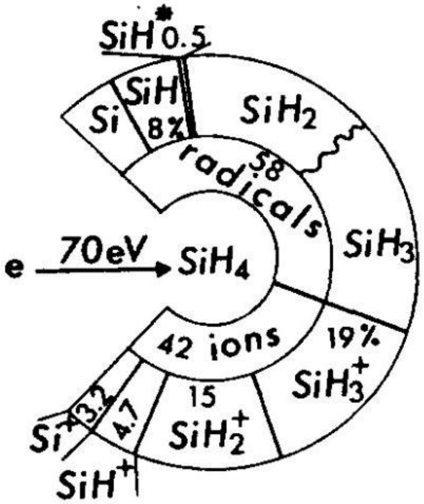


Figure 1.5 Probability manifold for the SiH_4 dissociative species due to a 70 eV electron impact deduced from mass spectrometry measurements [6].

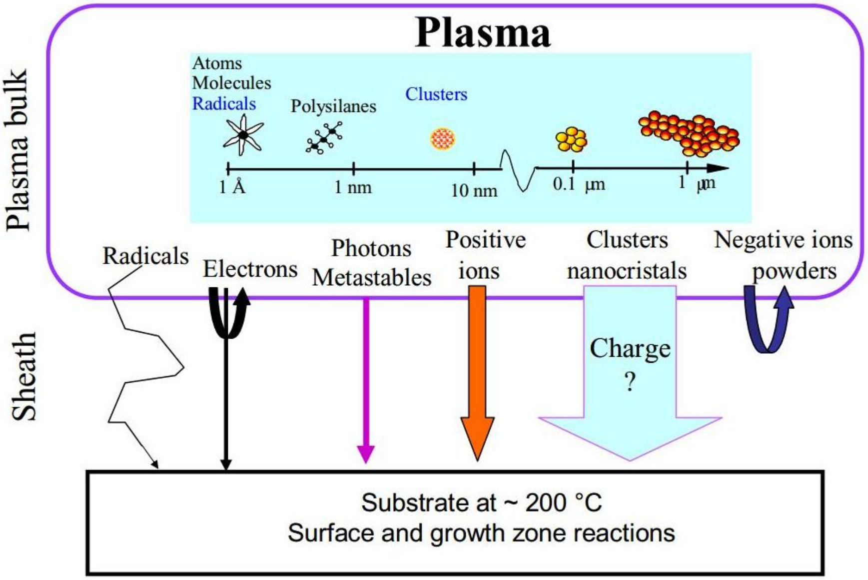


Figure 1.6 The plasma provides the source of reactive species, whose interaction with the substrate depends on their charge due to the presence of a space charge region (sheath) between the plasma and the chamber walls [7].

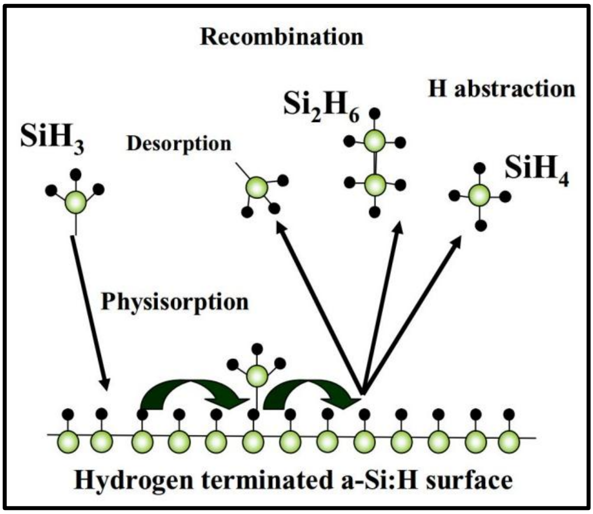


Figure 1.7 Standard model of *a*-Si:H deposition based on the interaction of SiH_3 radicals with a hydrogen terminated silicon surface [7].

1.2.2 SPUTTERING

Sputtering is a physical vapour deposition (PVD) process, where the atoms are ejected from a 'target' due to the collision of energetic ions and diffuse onto the substrate surface for the film growth. Inert gases like Ar are normally used as the sputter source, and the configuration can be glow discharge or ion beam. The glow discharge source is commonly sustained between the two parallel plate electrodes on which a DC or AC power is applied, in a similar way to the PECVD system. Figure 1.8 shows the schematic representation of a sputter coater. Moreover, in order to increase its efficiency, a magnetic field can be applied parallel to the target surface (as shown in Figure 1.9), so that in combination of electrical field, the secondary electrons in the glow discharge can be confined in a closed circuit, therefore the glow discharge bulk is kept in front of the target surface. In addition, oxide and nitride thin films can be formed via a chemical reaction process between the target material and the gas (i.e. O_2 or N_2) introduced in the chamber, which is named reactive sputtering. In this thesis, a RF-magnetron sputter coater is utilized for ITO (ITO as target) and SiO_2 (Si as target and O_2 as reactive gas) deposition. Compared with PECVD deposition, the film deposited via sputtering is less conformal; however, sidewall deposition still takes place, as shown in 4.3.2.2.

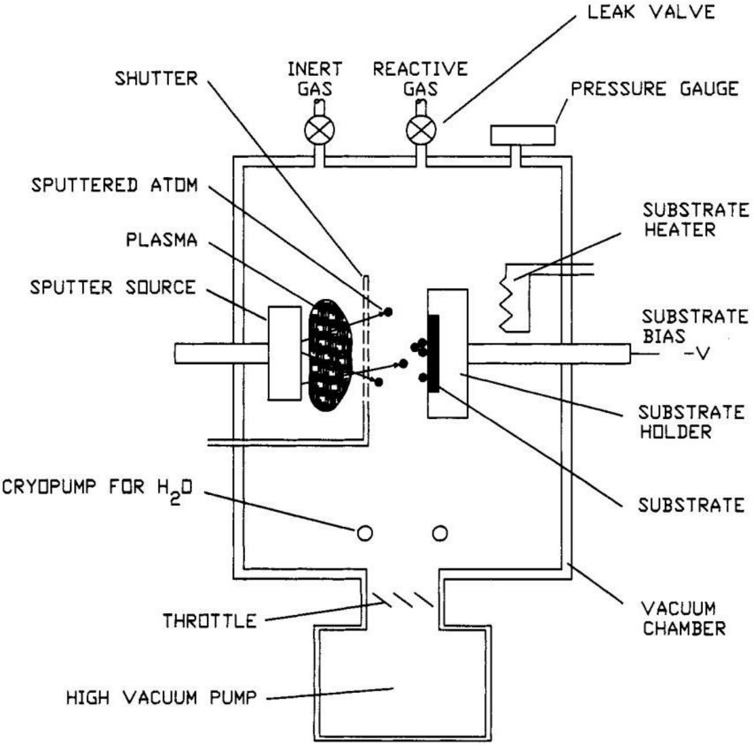


Figure 1.8 Schematic representation of a sputter coater [8].

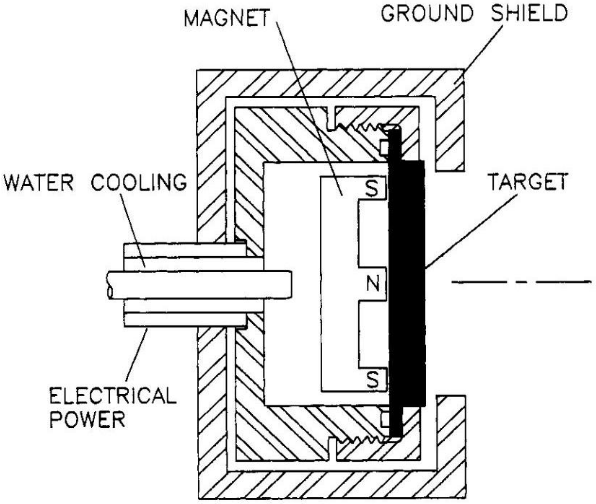


Figure 1.9 Schematic representation of a magnetron sputter source [9].

1.2.3 THERMAL EVAPORATION

Thermal evaporation is another physical vapour deposition process that utilizes Joule-effect to heat the source material (target) thanks to an electrical current passing through the crucible until it melts and evaporates in vacuum; then the material atoms in the vapour phase transport directly to the substrate and condense to form a solid phase on it. Figure 1.10 shows a schematic representation of a Joule-effect thermal evaporator. Different from PECVD and sputtering, thermal evaporation is an anisotropic deposition process, which favours the lift-off method for patterning thin films, as will be detailed in 1.3.1. In this thesis, indium thin films are deposited by thermal evaporation. Their nominal thickness is controlled thanks to a quartz crystal microbalance.

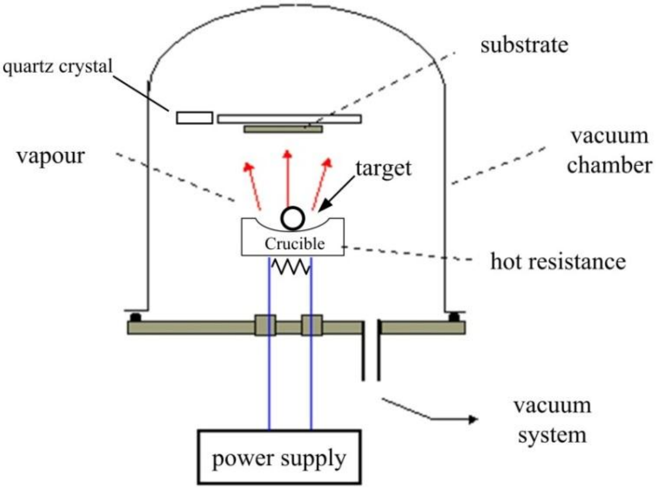


Figure 1.10 Schematic representation of a joule-effect thermal evaporator [10].

1.2.4 RAMAN SPECTROSCOPY

Raman spectroscopy is a spectroscopic technique based on the inelastic scattering of a monochromatic light by a material, which causes wavelength shifts of the light (i.e. Raman shift). The identity and properties of the material are reflected by the Raman shift and Raman spectrum, respectively.

The principle of Raman scattering is the energy change between the absorbed and re-emitted photon upon its interaction with a molecule. Note that the molecule should have polarity so that its bonds can start to vibrate and re-emit a photon after their excitation due to the interaction with incident photons. If the photon energy change is zero, the light scattering is elastic, named Rayleigh scattering, which is the most common light scattering process. If the photon loses or grains energy during this scattering process, it is called Stokes or anti-Stokes Raman scattering. Figure 1.11 illustrates the three forms of scattering of a monochromatic light by a material. Stokes Raman scattering depicts the process by which a molecule is raised from the ground state to a virtual state and drops back to a vibrational state, so the incident photon loses energy with decreased frequency and increased wavelength. Anti-Stokes Raman scattering occurs when a molecule starts from a vibrational state to a virtual state and drops back to the ground state, therefore the incident photon gains energy with increased frequency and decreased wavelength. As the probability of initial state energy of a molecule is determined by Boltzmann distribution:

$$F(state) \propto e^{-\frac{E}{kT}} \tag{1-1}$$

where E represents the state energy, k is the Boltzmann constant and T is the absolute temperature, the amount of molecules at the ground state is much higher than the ones at vibrational states before the photon-molecule interaction, thus Stokes scattering events are more likely to occur than anti-Stokes ones. So normally Raman spectroscopy only uses the Stokes spectrum due to its greater intensity.

Figure 1.12 shows a schematic representation of a conventional Raman spectrometer. The monochromatic light from a laser is focused on the sample surface, then scattered by the sample. Most of the scattering process is Rayleigh scattering, but a small amount results into a Stokes Raman scattering, so the filter discriminates the Rayleigh scattered light and lets Raman scattered light pass. Finally, the spectrograph splits and diffracts the Raman scattered light thanks to grating and records the electrical signal by a CCD.

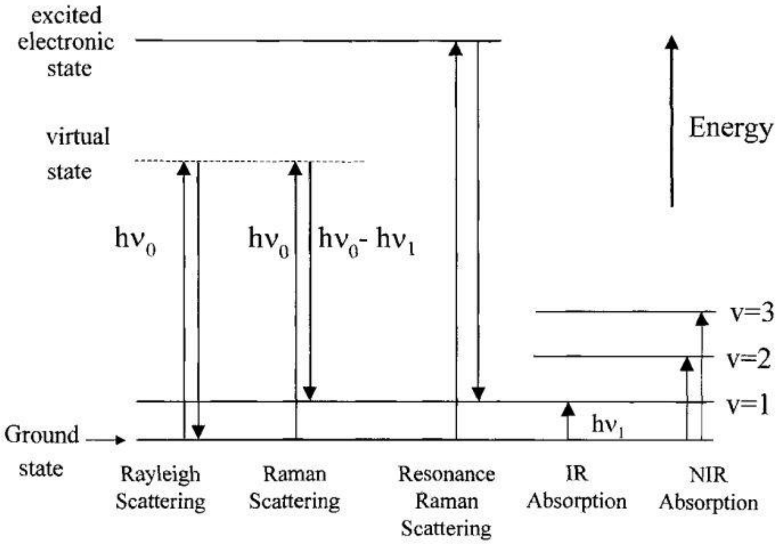


Figure 1.11 Three different forms of scattering [11].

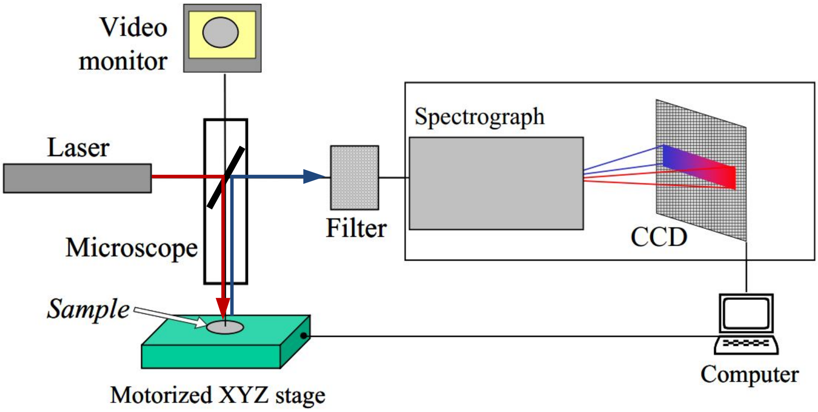


Figure 1.12 Schematic representation of a Raman spectroscopy set up [12].

Figure 1.13 shows the Raman shift of hydrogenated and non-hydrogenated amorphous silicon [13]. Transverse optical (TO) peak with standard wavenumber of 480 cm^{-1} is the main peak of amorphous silicon, whose position and full width at half maximum (FWHM) reflect the structural disorder of the amorphous network. Figure 1.14 shows that the TO peak position of ion-implanted amorphous silicon shifts to higher wavenumbers and the FWHM decreases (i.e. broadening of the Raman spectrum), due to thermal annealing, which implies that the structural disorder degree is reduced [14]. Other peaks like transverse acoustic (TA), longitudinal optic (LO) and acoustic (LA) peaks as shown in Figure 1.13, are also determined by the structure of the amorphous silicon network, but will not be detailed here.

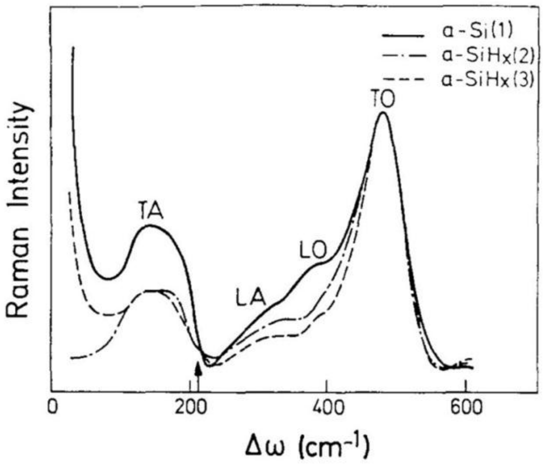


Figure 1.13 Raman shift (Δω) of hydrogenated and non-hydrogenated amorphous silicon [13].

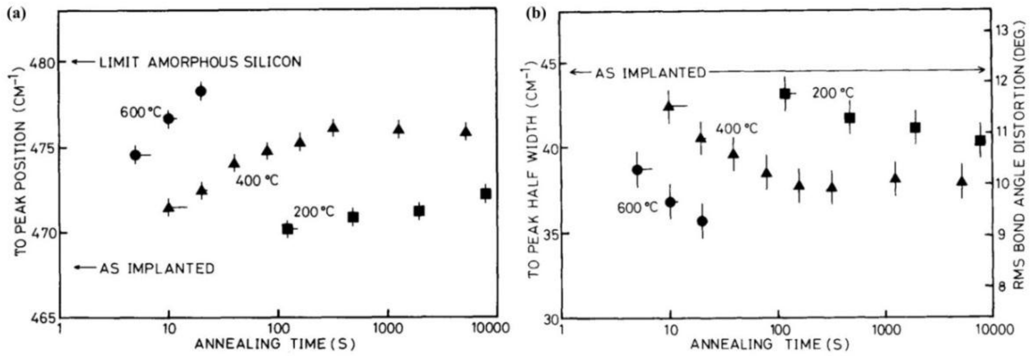


Figure 1.14 Annealing effect on the TO peak position (a) and its FWHM (b), for ion-implanted amorphous silicon [14].

1.2.5 SPECTROSCOPIC ELLIPSOMETRY

Another method for thin film characterization is the UV-visible Spectroscopic Ellipsometry (SE), which is mainly used to determine film thickness and optical constants and also applied to characterize composition, crystallinity, roughness, and other material properties associated with a change in optical response.

In principle, ellipsometry measures the change of polarization of the light transmitted or reflected from a thin film. Light can be depicted as an electromagnetic wave traveling through space. Polarization is a property of wave that can oscillate with more than one orientation. Figure 1.15 illustrates a vertically polarized electromagnetic wave of wavelength λ propagating in direction z with electric field E and magnetic field B components oscillating in orthogonal directions.

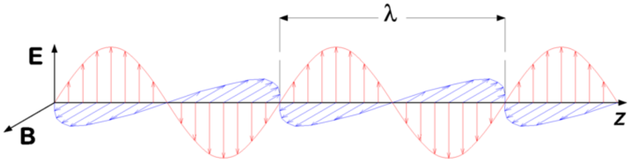


Figure 1.15 Schematic representation of a vertically polarized electromagnetic wave.

For ellipsometry, the electric field of light is considered. As it is always orthogonal to the propagation direction z, the electric wave can be de decomposed as x- (also called p- from "parallel") and y- (also called s- from "senkrecht" as "perpendicular" in German) components. If the two orthogonal electrical waves are in-phase, the synthesized light is linearly polarized, the orientation is determined by the relative amplitudes of the two components. If the orthogonal waves are $\pi/2$ out-of-phase and equal in amplitude, the resultant light is circularly polarized. If the amplitudes and phases of the orthogonal waves are arbitrary, it is called elliptical polarization, which is used in ellipsometry. Figure 1.16 illustrates the three types of polarization [16].

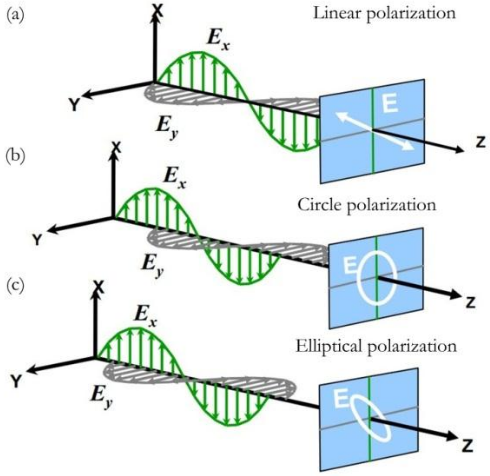


Figure 1.16 Combination of two orthogonal electric waves for three types of polarization: (a) linear, (b) circle and (c) elliptical polarization [16].

When an elliptically polarized light interacts with a material, it can be reflected, absorbed and refracted (or transmitted) by the material. Figure 1.17 illustrates a light beam propagating from the air with refractive index n_1 to a material with refractive index n_2; θ_i, θ_r, θ_t represent the incident, reflected and transmitted angles, respectively. According to law of reflection,

$$\theta_i = \theta_r \,. \tag{1-2}$$

According to Snell's law,

$$n_1 sin\theta_i = n_2 sin\theta_t \,, \tag{1-3}$$

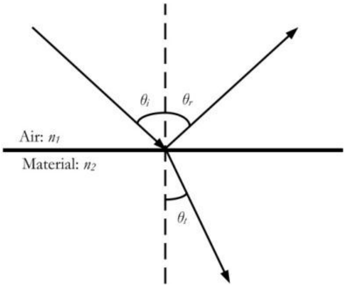


Figure 1.17 Schematic representation of a light propagating from air to a material, being reflected and refracted.

The complex refractive index $\tilde{n}$ of a medium determines the propagation of a light in it:

$$\tilde{n} = n + i\kappa \, , \tag{1-4}$$

where the index *n* describes the phase velocity of the polarized light in the material with respect to the velocity in vacuum *c*, as written by:

$$v = \frac{c}{n} \, , \tag{1-5}$$

and the extinction coefficient *κ* indicates the energy loss degree of the light propagating through the material.

The complex dielectric function of a medium, from another point of view, describes the interaction between the medium and the light, as written by:

$$\varepsilon = \varepsilon_1 + i\varepsilon_2 \, , \tag{1-6}$$

where the real part ε_1 represents the amount of a material becoming polarized when an electric field is applied due to creation of electric dipoles in the material, as illustrated in Figure 1.18; and the imaginary part ε_2 represents the light absorption by the material.

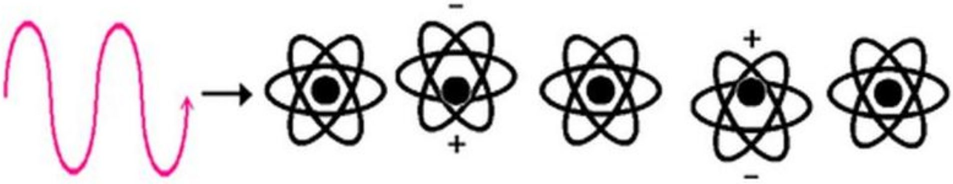


Figure 1.18 Schematic representation of polarization inside a material induced by an oscillating electric field [17].

The relationship between the complex refractive index and the complex dielectric function is expressed by:

$$\varepsilon(\lambda) = \tilde{n}^2 \, , \tag{1-7}$$

by combining equations (1-4), (1-6) and (1-7), we have

$$\begin{cases} \varepsilon_1 = n^2 - \kappa^2 \\ \varepsilon_2 = 2\mathrm{n}\kappa \end{cases} , \tag{1-8}$$

The measurement of the change of polarization of the light by ellipsometry relies on the comparison of the amplitude and phase of the reflected polarized light with the ones of incident polarized light, as illustrated in Figure 1.19.

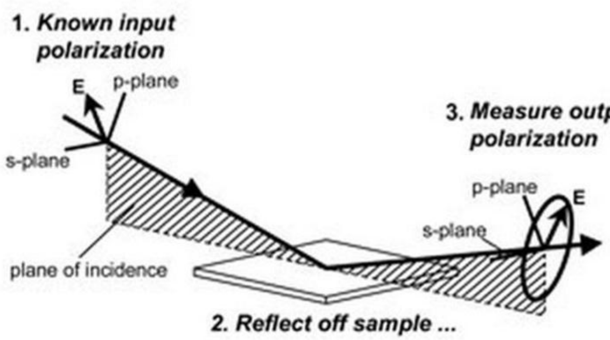


Figure 1.19 Typical ellipsometry configuration, where linearly polarized light is reflected from the sample surface and the polarization change is measured to determine the sample response [18].

Fresnel coefficients [19] describe the intensity fraction of the reflected and refracted (or transmitted) light when an incident polarized light propagates through the interface of two mediums:

$$\begin{cases} r_s = \frac{\widetilde{n_1} cos\theta_i - \widetilde{n_2} cos\theta_t}{\widetilde{n_1} cos\theta_i + \widetilde{n_2} cos\theta_t} \\ t_s = \frac{2\widetilde{n_1} cos\theta_i}{\widetilde{n_1} cos\theta_i + \widetilde{n_2} cos\theta_t} \\ r_p = \frac{\widetilde{n_2} cos\theta_i - \widetilde{n_1} cos\theta_t}{\widetilde{n_1} cos\theta_t + \widetilde{n_2} cos\theta_i}, \\ t_s = \frac{2\widetilde{n_1} cos\theta_i}{\widetilde{n_1} cos\theta_t + \widetilde{n_2} cos\theta_i} \end{cases} \tag{1-9}$$

where $r_{s,p}$ represent the reflectance coefficients of s- and p- plane electric waves, respectively, which are the ratios of the reflected electric wave amplitudes; and $t_{s,p}$ represent the transmittance coefficients of s- and p- plane electric waves, respectively, which are transmitted electric wave amplitudes.

The polarization change in ellipsometry is represented by:

$$\rho = \frac{r_p}{r_s} = \tan(\psi)\, e^{i\Delta}, \tag{1-10}$$

where Ψ is determined by the ratio of absolute values of reflectance coefficients

$$\tan(\psi) = \left| r_p / r_s \right| , \tag{1-11}$$

and $\Delta = \delta_p - \delta_s$ is the phase difference. For a semi-infinite material, the ratio ϱ is related to the complex dielectric function ε:

$$\varepsilon = sin_{\theta_i}^2 + sin_{\theta_i}^2 tan_{\theta_i}^2 [(1-\rho)/(1+\rho)]^2 , \tag{1-12}$$

After the (Ψ, Δ) data are measured, a model is constructed to use the measured data to evaluate the optical properties of the material by adjusting specific fit parameters. For semiconductors and insulators under an electric field, the binding between electrons and nucleus are assumed to be a mass-spring system, where electrons vibrate like damped harmonic oscillators, called Lorentz oscillators, as illustrated in Figure 1.20 [20].

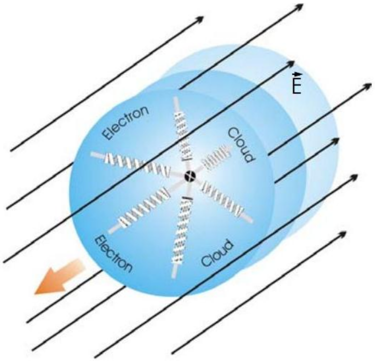


Figure 1.20 Schematic representation of Lorentz dispersion model, assuming that the electron-nuclei is similar to a mass-spring system [20].

The tauc-Lorentz dispersion formula [21] is developed by using Tauc joint density of states and the Lorentz oscillator and often used to model the ellipsometry data of *a*-Si:H thin films. The complex dielectric function is:

$$\widetilde{\varepsilon_{TL}} = \varepsilon_{r,TL} + i(\varepsilon_{i,T} \times \varepsilon_{i,L})\,, \tag{1-13}$$

where the imaginary part is given by the product of imaginary part $\varepsilon_{i,T}$ of Tauc's dielectric function with Lorentz one $\varepsilon_{i,L}$. Tauc's dielectric function describes inter-band transitions above the band edge as:

$$\begin{cases} \varepsilon_{i,T}(E > E_g) = A_T\left(\frac{E-E_g}{E}\right)^2 \\ \varepsilon_{i,T}(E \leq E_g) = 0 \end{cases}, \tag{1-14}$$

where A_T is the Tauc coefficient, E is the photon energy, E_g is the optical band gap. The imaginary part of the Lorentz oscillator is given by:

$$\varepsilon_{i,L}(E) = \frac{A_L{\cdot}E_0{\cdot}C{\cdot}E}{\left(E^2-E_0^2\right)^2+C^2{\cdot}E^2}\,, \tag{1-15}$$

where A_L is the strength of the $\varepsilon_{i,TL}(E)$ peak, C is the broadening term of the peak, E_0 is the peak central energy. By combining (1-13), (1-14) and (1-15), the imaginary part of Tauc-Lorentz dielectric function can be expressed as:

$$\varepsilon_{i,TL}(E) = \begin{cases} \frac{1}{E}\cdot\frac{A_T A_L E_0 C(E-E_0)^2}{\left(E^2-E_0^2\right)^2+C^2E^2} & (E > E_g) \\ 0 & (E \leq E_g) \end{cases}, \tag{1-16}$$

Figure 1.21 shows the measurement and the fitting results of *a*-Si:H deposited on *c*-Si wafer with native oxide by phase-modulated ellipsometry from 1.5 to 4.5 eV at an incident angle of 70°. The thickness of native oxide on *c*-Si substrate is fixed at 10 Å. As the oxidation is inevitable to occur on the surface of *a*-Si:H layer, in the model a top layer of SiO_2/*a*-Si:H/void mixture was initially added, based on Bruggeman effective-medium approximation [22]. The fitting result shows that the surface of *a*-Si:H is completely oxidized. Note that this measurement was carried out immediately after unloading the sample from the PECVD system at substrate temperature of 150°C, the thickness of grown *a*-Si:H oxide layer is calculated around 3 Å. A series of measurement were carried out for demonstrating that the continuous growth of oxide layer in ambient as a function of time, as listed in Table 1.1.

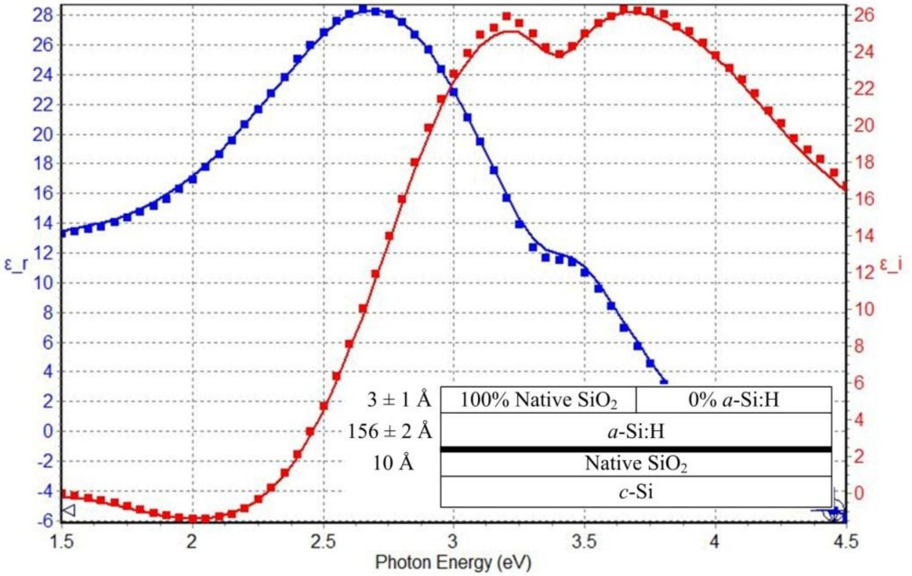


Figure 1.21 measurement and the fitting results of *a*-Si:H deposited on c-Si wafer with native oxide by a phase-modulated ellipsometry from 1.5 to 4.5 eV with incident angle of 70°.

Table 1.1 Fitting results of *a*-Si:H deposited on c-Si with native oxide after exposure to ambient air.

Time	**+ 0 hour**	**+ 19 hours**	**+ 44 hours**
Oxide of a-Si:H (Å)	**3±1**	**10±2**	**14±2**
***a*-Si:H (Å)**	156±2	155±3	154±3
E_g (eV)	1.65±0.02	1.65±0.02	1.66±0.02
A	191±4	191±6	195±6
E_0 (eV)	3.58±0.01	3.58±0.02	3.60±0.02
C	2.10±0.02	2.11±0.02	2.12±0.02
$\varepsilon(\infty)$	Fixed at 1.		

1.3 LITHOGRAPHY

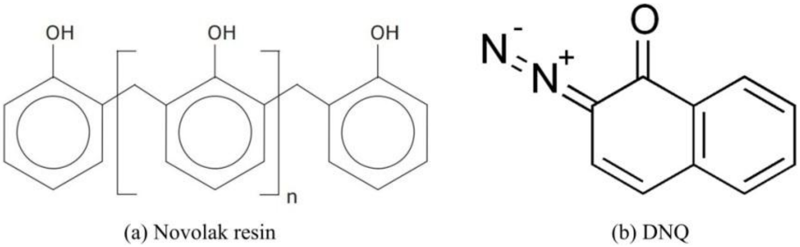
The word lithography is derived from ancient Greek “λίθος”, lithos in Latin letters, meaning “stone”, and “γϱάφειν”, graphein, meaning “to write”. In history, it was a method of printing texts from a stone or metal plate onto papers or other materials [23]. In modern semiconductor and integrated circuits (ICs) industry, micro-/nano- lithography technologies are applied to pattern the materials in small feature sizes down to submicron scale, accompanied with thin film deposition and wet/dry etching techniques.

In general, lithography techniques can be classified into two types [24]: (i) mask lithography, which use a pre-designed mask or template to transfer patterns on the substrates, including optical lithography, soft lithography, nanoimprint lithography and extreme ultraviolet (EUV) lithography; (ii) maskless lithography, which fabricates the patterns by in-situ writing without masks, including electron beam lithography, focused ion beam lithography, etc. In this thesis, optical lithography is used to pattern the substrate surface for the guided growth of in-plane SiNWs; electron beam lithography is used to define the electrode for measuring the resistivity of randomly grown in-plane SiNWs.

1.3.1 OPTICAL LITHOGRAPHY

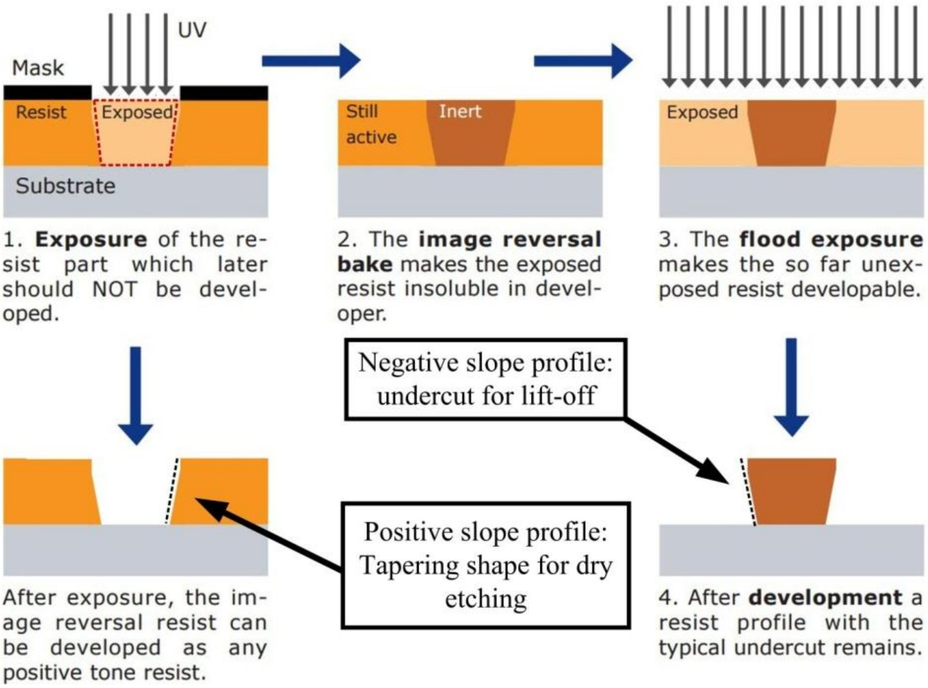
Optical lithography defines patterns by exposing a light-sensitive resin (called photo-resist) to an ultraviolet (UV) light whose wavelengths range from 193 to 436 nm. The desired patterns are pre-designed on a transparent substrate (e.g. quartz or glass) with metallic opaque features (e.g. chrome) on it, through which the UV light is illuminated to the photo-resist which is spin-coated on the sample surface.

Take AZ5214-E [25] image reversal (IR) photo-resist used in this thesis for example: it is composed of a Novolak resin and Diazonaphthoquinone (DNQ) as photoactive compound (as shown in Figure 1.22), which is same as positive photo-resist. The UV exposure will release nitrogen from DNQ and transform it into a carboxylic acid, which is soluble in the aqueous alkaline solution based on NaOH, KOH, or TMAH (called developer). On the other hand, a baking step (called image reversal baking) after the UV exposure will produce a special crosslinking agent only in the exposed AZ5214-E, making this part of the photo-resist insoluble in developer as well as insensitive to the UV light, while the unexposed areas still behave like a normal unexposed positive photo-resist. After a flood exposure without photo-mask, only the crosslinked areas remain in the developer for positive photo-resist. Figure 1.23 illustrates the process of AZ5214-E as positive and image reversal photo-resist [26]. Also, it shows that the profile of positive photo-resist after development has a positive slope (75-85°), from which the name “positive” is derived. This is because during the exposure process, the UV light is attenuated when propagating through the photo-resist layer due to the absorption by the DNQ, called bulk effect, as shown in Figure 1.23 process 1. This type of positive tone is used as dry etching mask. On the other hand, the profile of IR photo-resist after development has a negative slope, also called undercut, which favours the lift-off process, as shown in Figure 1.24. A modified method for lift-off process is to introduce a mediated photo-resist layer (LOR for lift-off resist), which has different development rate with the AZ5214E so that the undercut can be formed for ensuring a discontinuous thin film deposition, as shown in Figure 1.25[27]. This method is also called bilayer lift-off.



(a) Novolak resin (b) DNQ

Figure 1.22 Composition of AZ5214E photo-resist: (a) Novolak resin, (b) Diazonaphthoquinone (DNQ) [26].



1. **Exposure** of the resist part which later should NOT be developed.

2. The **image reversal bake** makes the exposed resist insoluble in developer.

3. The **flood exposure** makes the so far unexposed resist developable.

Negative slope profile: undercut for lift-off

Positive slope profile: Tapering shape for dry etching

After exposure, the image reversal resist can be developed as any positive tone resist.

4. After **development** a resist profile with the typical undercut remains.

Figure 1.23 Process of AZ 5214E as image reversal photo-resist: (1) exposure with photo-mask, (2) reversal bake, (3) flood exposure without mask, (4) development. After the first exposure (1), the image reversal resist would behave as a positive tone resist in the developer [26].

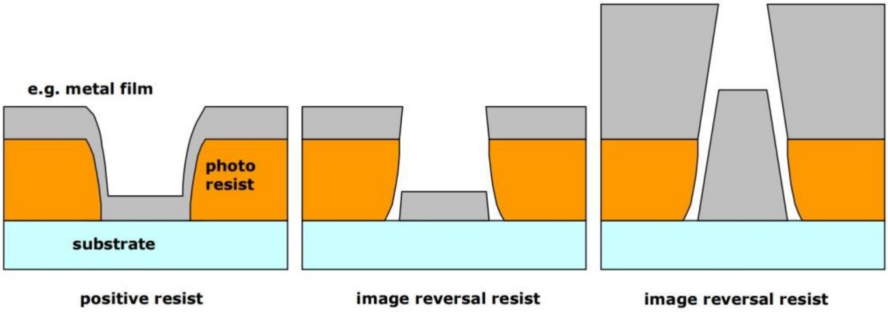


Figure 1.24 Comparison of the lift-off process with positive resist and image reversal resist, which shows that IR resist allows reproducible lift-off of film [26].

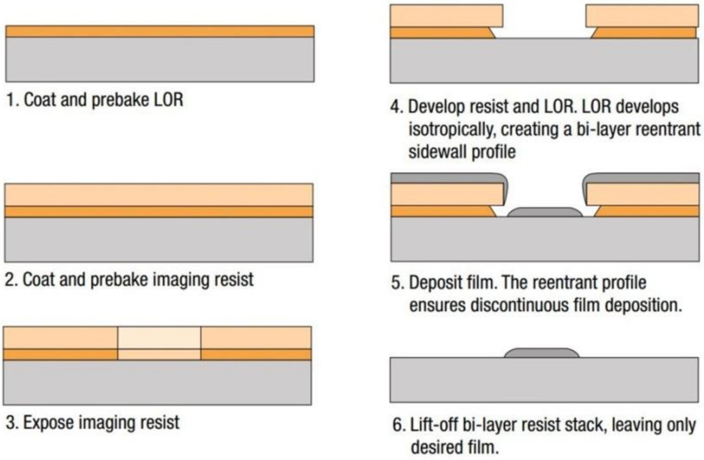


Figure 1.25 Bilayer photo-resists for lift-off process.

1.3.2 ELECTRON-BEAM LITHOGRAPHY

Electron-beam lithography, as a maskless method, can be used to write patterns directly by activating the chemical transformation of photo-resist by electron, instead of the photon of UV light. As electrons used in e-beam lithography (5-100 keV) have extremely short wavelength, features in atomic dimension are required to diffract the electron beam, so that producing features with high resolution (less than 10 nm) turns to be possible by electron-beam lithography [28]. Figure 1.26 shows a schematic representation of a multi-electron-beam system using a single-column electron lens. The emitted electron source is generated into several separated electron beams by the aperture array, after traversing through the various electron lens, the electron beams are focused on the wafer. Compared with single electron beam (not shown here), multi electron beam favours the separation of electrons in the trajectory to the wafer, which reduces the stochastic blurring due to the single electron beam broadening effect caused by electron-electron interaction.

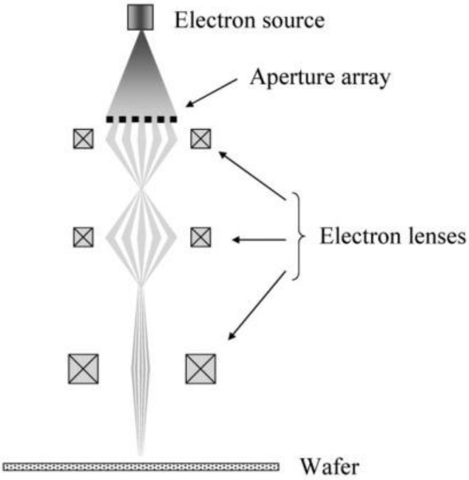


Figure 1.26 Schematic representation of a multi-electron-beam system using a single-column electron lens.

1.4 DRY ETCHING

Dry etching is a process of structuring wafers with reactive species in gaseous phase, whose counterpart is wet etching with liquid etchants. The development of dry etching techniques has made available and reliable the miniaturisation in VLSI industry, in comparison with isotropic wet etching. The interaction between gaseous etchants and target materials (i.e. semiconductors, insulators and metals) can be dominated by (i) chemical reactions on the target surface, (ii) physical process like high energetic ion beam bombardment to the target surface, (iii) or a mixture of chemical and physical processes.

Technically, the gaseous etchant can be produced in glow discharge, beam or ion beam methods. Figure 1.27 lists the categories of dry etching and typical energy and pressure ranges [29]. In this thesis, capacitively-coupled plasma reactive ion etching (CCP-RIE) and reactive ion beam etching (RIBE) are used to fabricate the structured substrates.

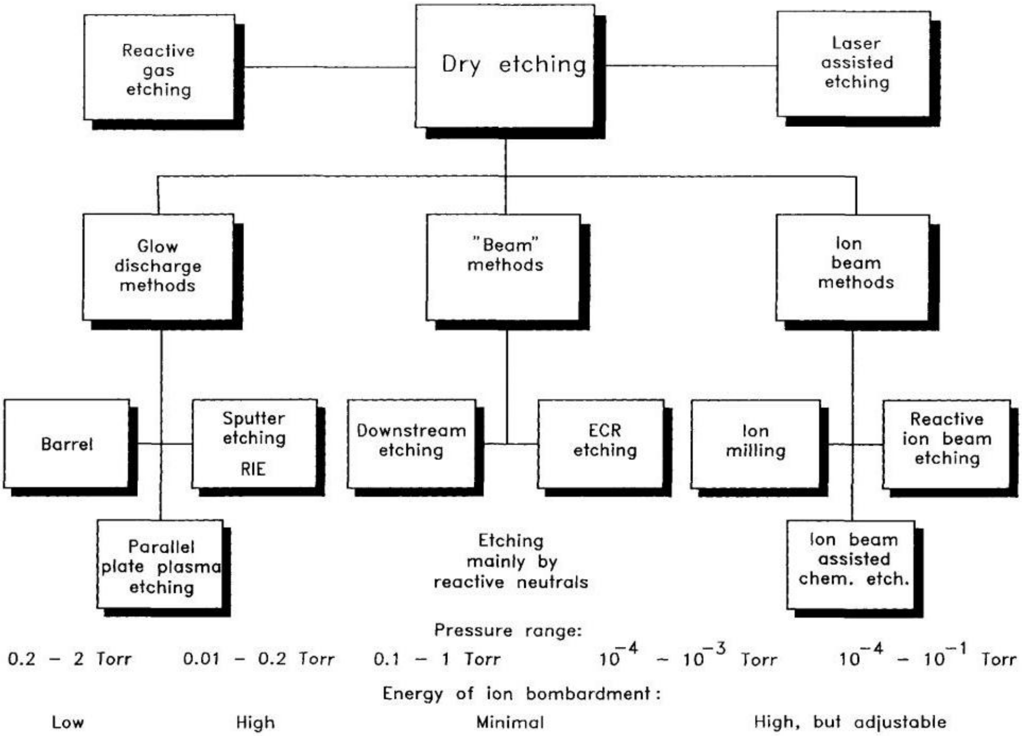


Figure 1.27 Categories of dry etching and typical energy and pressure ranges.

1.4.1 REACTIVE ION ETCHING

In general, Reactive ion etching (RIE), as a glow discharge method, is based on a similar process as plasma-assisted deposition (PECVD), where reactive species (ions and/or radicals) are generated due to the electron-impact ionization and dissociation of selected gas precursors fed in the PECVD system. However, in the case of RIE, they react with the target substrate and form volatile products which are pumped away. Figure 1.28 shows a schematic representation of the basic steps of plasma etching [30]: (1) generation of reactive species, (2) diffusion to the substrate surface, (3, 4, 6) adsorption, surface diffusion, desorption of reactive species, (5) chemical reaction between reactive species and substrate, (7) diffusion of volatile reaction products.

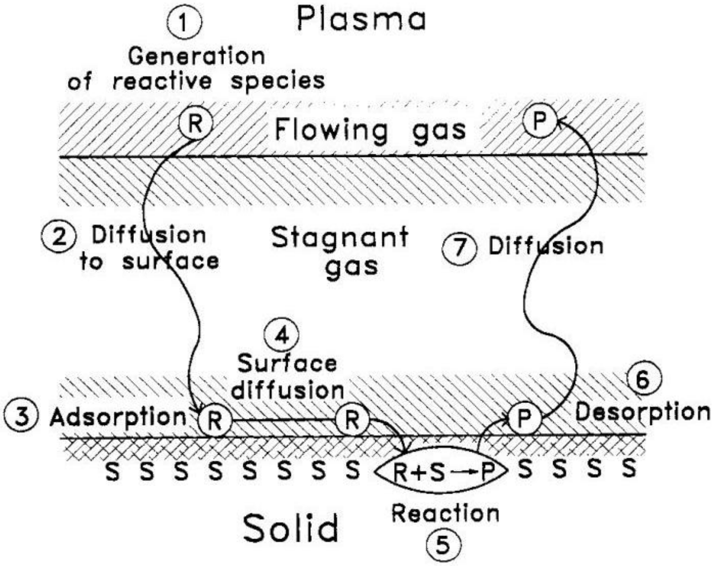


Figure 1.28 Schematic representation of basic steps of plasma etching [30].

The etching profile produced by RIE process is influenced by the plasma system configuration [31]. For Si-based materials (Si, SiO_2, Si_3N_4 or SiC), fluorine-based gases, such as SF_6 and CHF_3, can be used as etching precursors [31][32]. Figure 1.29 illustrates the etch profiles of silicon by pure SF_6 RIE and SF_6/CHF_3 RIE. Pure SF_6 RIE is an isotropic plasma etching process which can produce an undercut pattern. In order to obtain vertical sidewalls, CFH_3 is added to SF_6 gas, so that a blocking fluorocarbon layer (C_xF_y) [33][34] will be deposited on the substrate surface as well as on the sidewall with different rates; however the layer deposited at the bottom of the substrate will be re-sputtered on the sidewalls by ion beam bombardment, which enables the etching progress. In this thesis, SF_6/CHF_3 RIE is used to etch SiO_2 thin films.

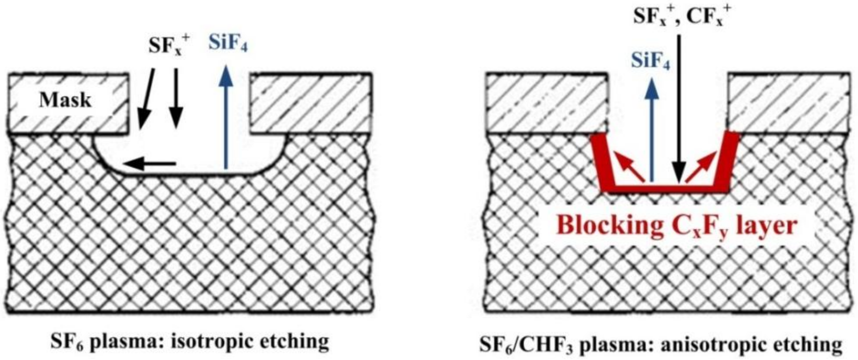


Figure 1.29 Schematic representation of etch profile due to different plasma system configuration: (a) undercut profile by isotropic SF_6 RIE; (b) relatively vertical sidewall profile by anisotropic SF_6/CHF_3 RIE.

1.4.2 REACTIVE ION BEAM ETCHING

Ion beam etching (IBE), similar to sputtering, can be described as a physical process where atoms on the target substrate are removed by energetic ion bombardment [35]. The etching directionality is ensured by the ion beam configuration. Argon ions are normally used as etchant, which can etch both the substrates and masks. Reactive ion beam etching (RIBE) is a special type of IBE, in which the ion beam reacts with the target substrate, improving the etching selectivity and etching rate [36]. Figure 1.30 shows the schematic representation of an Ion-beam etching system. The microwave electron cyclotron resonance (ECR) excitation mode [37] is used to generate a high density of ions in the discharge chamber [38]. The grids system screens the plasma and accelerates the ions to eject a collimated ion beam into the etching chamber. This set of multi-level aperture grids is also called ion optics [39]. As the positively charged ions will accumulate on insulating target substrates and repel the following ions, a neutralizer providing electrons is added in front of the grids in the etching chamber, which mainly allows the target surface to be neutral. In this thesis, $Ar/CH_4/O_2$ RIBE is used to etch ITO thin films.

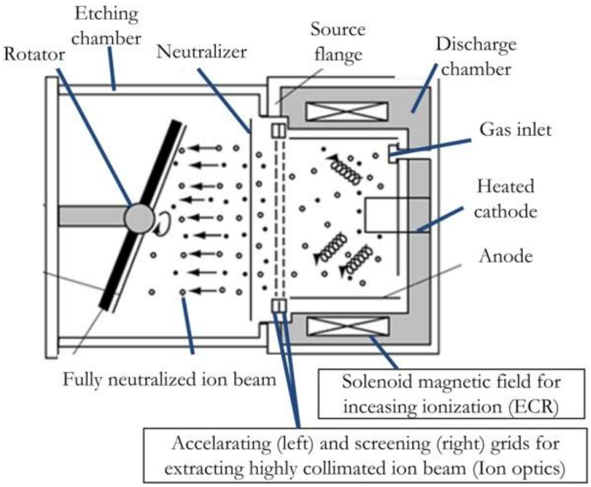


Figure 1.30 Schematic representation of an Ion-beam etching system [40].

1.4.3 ENDPOINT DETECTION TECHNIQUES

In order to control the etching stop, endpoint detection equipment should be integrated in the dry etching system. In this thesis, laser interferometry and mass spectrometry are used to detect the etching endpoint in RIE and RIBE etchers, respectively.

1.4.3.1 LASER INTERFEROMETRY

Laser interferometry monitors *in-situ* the etching process based on the alternative constructive and destructive interferences of the reflected light. Figure 1.31.a shows the principle of interferometry: a laser light is incident on the sample surface; it propagates through the two transparent layers till the opaque substrate surface; at each interface the laser light is reflected; as the thicknesses of the transparent layers keep changing during the etching process, the reflected laser light from different interfaces will periodically experience constructive and destructive interference (see b), resulting in a sinusoidal change of the reflectance signal intensity (see c). In particular, if there is only one transparent layer on an opaque substrate, after top layer is completely etched, the reflectance signal stops to oscillate because there remains only one gas-substrate interface, as shown in inset picture c(1). If there are multi layers with different refractive index, the signal oscillation period will change after each layer is completely etched; inset picture c(2) shows an example of two different transparent layers on an opaque substrate.

In addition, for a single transparent layer on an opaque substrate, the signal oscillation period Δ of sequential constructive and destructive interference is determined by:

$$\Delta = \frac{\lambda}{2\sqrt{n^2 - sin^2\theta}}, \tag{1-17}$$

where λ is the wavelength of laser beam, n is the refractive index, θ is the incident angle.

The etching depth *d* can be calculated by:

$$d = n\Delta = \frac{n\lambda}{2\sqrt{n^2 - sin^2\theta}}, \tag{1-18}$$

where *n* is counts of the oscillation period of the signal.

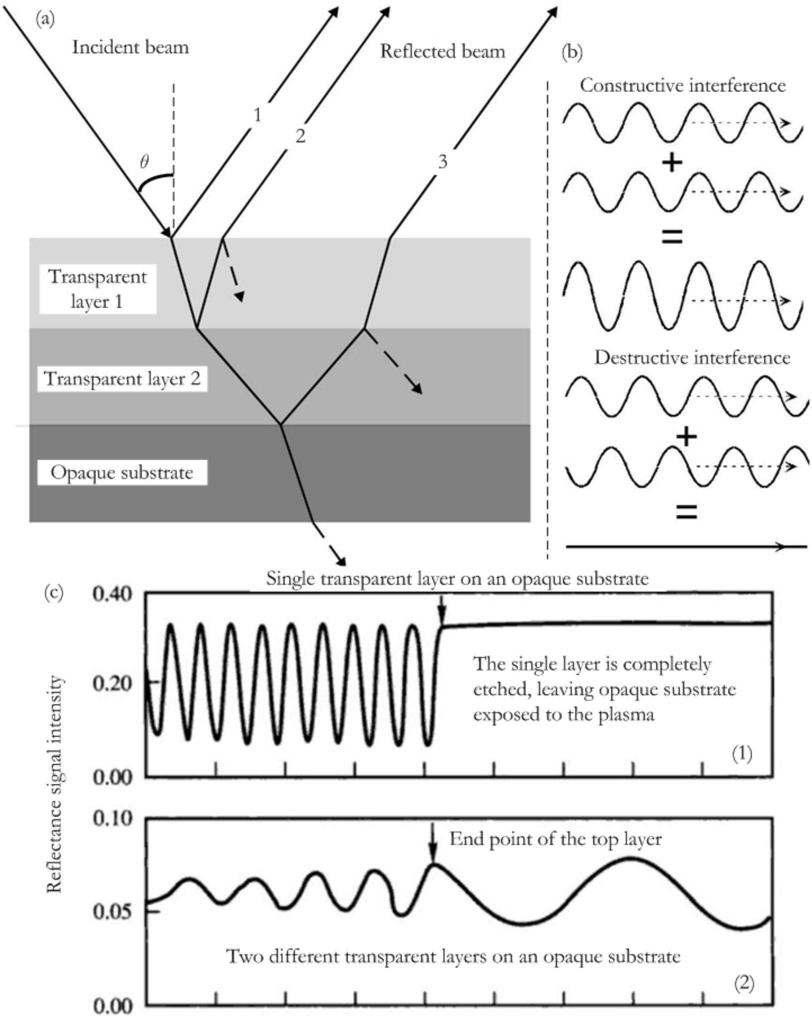


Figure 1.31 Principle of laser interferometry based on monitoring periodic constructive and destructive interference of the reflected laser light. (a) is from [41], (b) is from [42] and (c) is from [43].

1.4.3.2 MASS SPECTROMETRY

Instead of monitoring the target surface, one may also measure the species injected in the discharge as a result of the etching process. Mass spectrometry is an *in-situ* chemical analysis technique of the etching products by measuring their mass-to-charge ratios. The principle of chemical detection is by dispersing the ionized etching products with different mass-to-charge ratios in an electromagnetic field with varying potentials, as illustrated in Figure 1.32.a. Quadrupole mass filter is a common technique of ionizing the gaseous etching products by a filament and focusing the ions towards the collector through a quadrupole electrode, as shown in Figure 1.32.b.

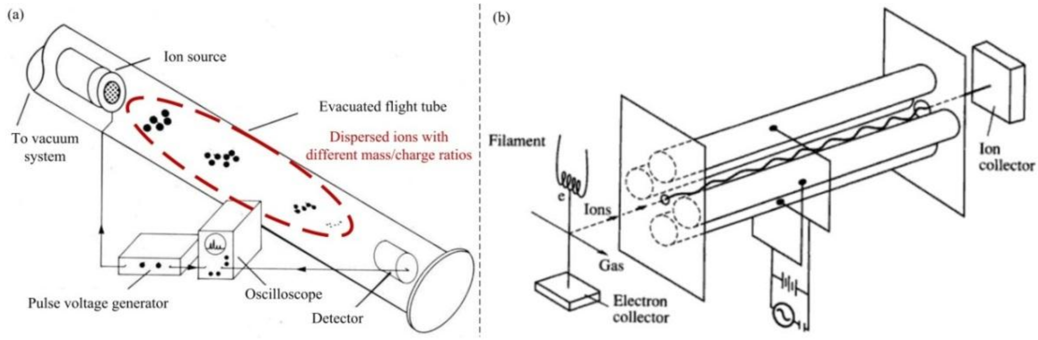


Figure 1.32 Schematic representation of time-of-flight mass spectrometer dispersing ions having different mass-to-charge ratios (a) [44], and of a quadrupole mass filter (b) [45].

1.5 ELECTRON MICROSCOPY

Electron microscopes rely on the electron-sample interaction [46] to image and chemically analyse the samples, depending on the electron energy. Figure 1.33 illustrates the possible emitted photons and charged particles due to electron-sample interaction, including (1) secondary electrons, (2) reflected or backscattered electrons, (3) transmitted electrons, (4) X-ray radiation, (5) Auger electrons, (6) cathodoluminescence radiations and (7) absorbed current. In particular, secondary electrons and/or backscattered electrons are used in imaging bulk samples in scanning electron microscopy (SEM), and transmitted electrons are used for thin film samples in transmission electron microscopy (TEM). Other emitted photons and charged particles can provide supplementary analytical information in either type of microscope.

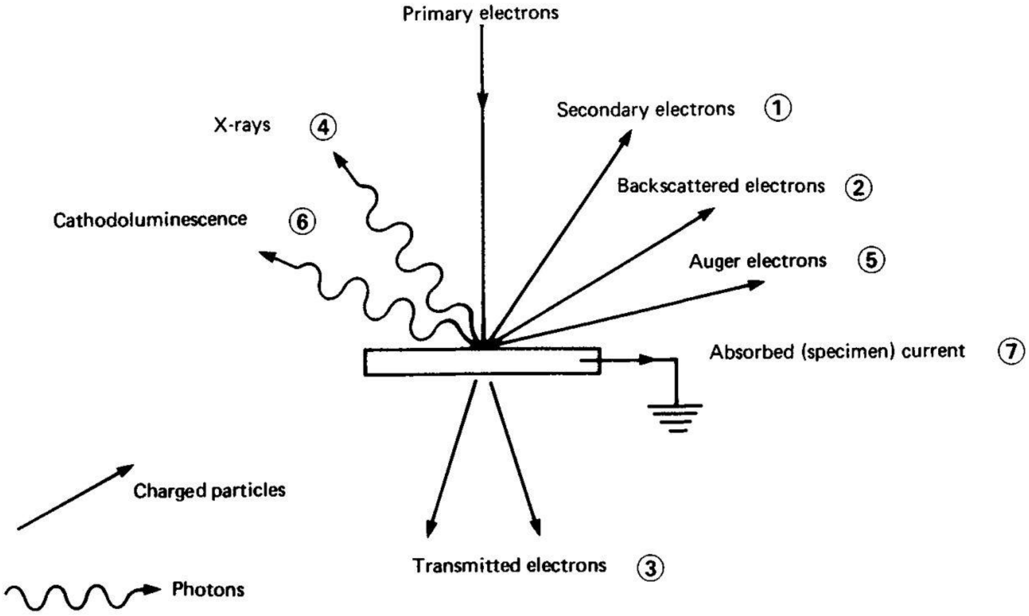


Figure 1.33 Schematic representation of photon and charged particle emissions from an electron-bombarded surface [46].

1.6 SUMMARY

In this chapter, the synthesis process of in-plane SiNWs via a solid-liquid-solid mode was firstly presented. Then the techniques used in this thesis are introduced as well as their corresponding principles. The techniques include thin film deposition and characterization techniques, optical and electron-beam lithography, dry etching (reactive ion etching and reactive ion beam etching) and endpoint detection (laser interferometer and mass spectrometer) techniques and the electron microscopes (scanning electron microscope and transmission electron microscope).

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2 INDIUM CATALYST: FROM THIN FILM TO NANOPARTICLES

CONTENTS

In the Chapter 1, the synthesis of in-plane solid-liquid-solid SiNWs based on thin film deposition techniques was introduced, which can be viewed as producing one-dimensional (1-D) nanostructures out of thin films. The interaction between liquid In nanoparticles and *a*-Si:H thin films results in the production of the in-plane silicon nanowires. In this chapter, metal catalysts for the growth of semiconductor nanowires (NWs) are first reviewed, then thin film growth modes are introduced. The two types of source for indium (In) catalyst (i.e. evaporated In and sputtered ITO thin films) have different microstructural and chemical properties, which lead to different NPs formation mechanisms under similar H_2 plasma treatment on heated substrates. Indium NP formation from evaporated In and sputtered ITO thin films are systematically investigated; the gained understanding will be the basis for developing strategies for large-scale organising in-plane SiNWs.

2.1 METAL CATALYSTS FOR GROWING SEMICONDUCTOR NANOWIRES

Semiconductor nanowires can be obtained via two main methods:

Top-down method is based on plasma and/or chemical etching process for tailoring bulk semiconductors into lateral nanowire arrays lying on them or into vertical nanowire arrays standing on them, which is enabled by the development of high resolution lithography techniques (e.g. electron-beam lithography and nanoimprint lithography, etc.) and anisotropic plasma etching techniques (e.g. ICP-RIE, R/IBE, etc.). Using this method, high performance lateral SiNWFETs on SOI have been fabricated by plasma etching method [1]. Moreover, metal-assisted (e.g. Ag, etc.) solution-based chemical etching has proved itself as a high throughput way for SiNW arrays and in application of photovoltaic [2]-[4].

Bottom-up method relies on a growth process during which a NW is synthesized by bringing a precursor in contact with a catalyst nanoparticle. The precursors can be a gas (e.g. $SiCl_4$ or SiI_2 [5][6], SiH_4 [7], GeH_4 [8] etc.), while they are also possible in liquid (e.g. diphenylsilane ($C_{12}H_{10}Si_2H_6$) [9], phenyl-$GeCl_3$ ($C_6H_5GeCl_3$) [10], etc.) or even in solid phase (e.g. *a*-Si:H) [11][12]. In particular of the source gases, they can be dissociated into various speciees or be directly evaporated on a substrate. The growth of NWs can take place during the deposition from vapour phase or after the deposition (i.e. solid phase), which is compatible with the thin film deposition techniques. In contrast to the top-down method, the grown NWs are mostly produced with the help of metal NPs as medium for collecting and rearranging the atomic semiconductor atoms.

The metal element can be the constituent of compound NWs such as III-V NWs (e.g. Ga for GaAs NWs, In for InP NWs, etc.) grown by MOVPE [13]-[16] or MBE [17]-[19], ITO NWs with In as catalyst by Direct-Current (DC) sputtering[20], electron beam evaporation [21] or MBE [22], or ZnO NWs catalysed by Zn [23], which is a self-catalytic growth.

However, in most cases of group IV NWs (i.e. Si, Ge, and SiGe [24], etc.), a foreign metal catalyst is required. Commonly, the metals are in the liquid phase (vapour-liquid-solid (VLS) method) [25], from which the vapour-solid-solid (VSS) method is derived (i.s. solid metals have also been reported to catalyse the NWs growth [25]-[29]). Many metals have been used for NWs growth, which consists of two types based on the different metal-semiconductor interactions (take Si for instance): 1) forming a metal-Si eutectic alloy as growth medium, like Au [30] as the most popular metal in VLS method, and various low melting point metals such as Al [31][32], In [11][12], Sn [33][34], Ga [35][36], Bi [37], etc.; 2) forming metal silicide as growth medium, in most cases of transition metals like Ni [38], Ti [39], Pt [40], Fe [41], etc.

Another topic on metal catalyst is the techniques used for obtaining NPs, which can be catalogued as:

I. Forming NPs by annealing metal thin films. This is the most common way of forming metal NPs. Take Au on Si (111) for instance, the size of the NPs can be controlled by the thickness of the thin films. However the redistribution of Au NPs can be achieved by the subsequent annealing as liquid Au migrates and coarsens due to its high surface mobility at high temperature [42].

II. Depositing metal NPs directly on the substrates. For example, Au colloid [43] is used for spraying Au NPs on the substrate. This method is supposed to control the size and density defined by the colloid, but only to a certain degree. Colloidal gold is a sol or colloidal suspension of sub-micrometre-size nanoparticles of gold in an aqueous solution [44].

III. Patterning the metal catalyst for selective area growth. In order to control the distribution of NPs, electron-beam or nanoimprint lithography can be used to define the position of the deposited metal. This method is especially favourable in growing vertical NWs array, which is known as selective area growth [45].

IV. Forming NPs on the corresponding metal oxide thin film by H_2 plasma. Besides the techniques above, a novel method is developed to form metal NPs on the surface of the corresponding oxide thin film, the most successful case is In NPs formation on ITO [46][47] or indium oxide [48]. H_2 plasma is employed to reduce the oxide on the substrate surface. Understanding the mechanism of this nanoparticle formation process and thus developing this technique for a better control, is still in progress.

In this thesis, indium is selected as the catalyst for the growth of in-plane SiNWs, since it is till now the most practical metal candidate according to LPICM experience (see 3.5). Indeed, transition metals like Au or other low melting point metals like Sn lead to porr NW morphologies, as discussed in Chapter 3.

As mentioned in Chapter 1, both evaporated In thin films and RF-magnetron sputtered ITO can be used for the In NPs formation. As the thin film properties depend on the deposition techniques and conditions, the thin film growth modes are introduced below.

2.2 THIN FILM GROWTH MODES

Depending on the bonding behaviour between the atomic precursors and the substrate surfaces, thin film formation can be classified into three primary modes [49][50], as illustrated in Figure 2.1.

I. **Volmer-Weber** (**VW**) or island growth mode occurs when the atoms or molecules of the deposit are more strongly bonded to each other than to the substrate. Slow atomic or molecular surface diffusion also permits the island formation. This growth mode dominates the systems of metals depositing on insulators.

II. **Frank-van der Merwe** (**FM**) or layer-by-layer growth mode, occurs when the atoms or molecules of the deposit tend to bind to the substrate rather than to each other. Fast atomic or molecular diffusion also favours the layer by layer growth. This growth mode is observed in some metal-metal systems, and in semiconductor growth on semiconductors.

III. **Stranski-Krastanov** (**SK**) or layer plus island mode, which is a mixed growth mode, describes the phenomenon that after forming the first or a few monolayers, subsequent film formation shifts to the islands mode. It occurs especially in cases when the deposited thin film-substrate interface energy is high (permitting the initial layer-by-layer growth) while the strain energy of the thin film is also high (favouring the islands formation to minimize the strain energy).

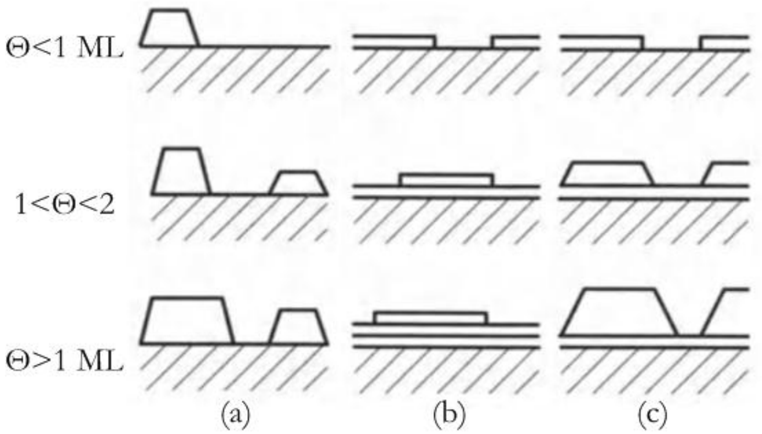

Figure 2.1 Primary thin film growth modes: (a) Volmer-Weber (VW) or island mode; (b) Frank-van der Merwe (FM) or layer-by-layer mode; (c) Stranski-Krastanov (SK) or layer-plus-island mode. Each mode is shown for several different amounts of surface coverage, Θ. [49]

2.3 EVAPORATED INDIUM THIN FILMS

Evaporated In thin films are one choice for providing In NPs for growing in-plane SiNWs. In order to obtain *a*-Si:H/In contact, a H_2 plasma treatment should be carried out to reduce the surface oxide before *a*-Si:H coating. In this section, the evolution of evaporated In thin films treated by H_2 plasma on various substrates and at different substrate temperatures is investigated, in order to understand their effects on In NPs formation.

2.3.1 MICROSTRUCTURE OF EVAPORATED INDIUM THIN FILMS

Indium thin films are deposited on *c*-Si substrates with native oxide by thermal evaporation. This results in island-like films, corresponding to the **VW growth mode**. Figure 2.2 shows SEM images revealing the thickness dependence of the microstructure of the films, with a nominal thickness of ~5 nm in (a to c) and ~50 nm in (d to f), respectively. The island growth mode is clearly demonstrated by the microstructure evolution from ~5 nm to ~50 nm thin films.

Furthermore, Figure 2.3 shows the SEM images of nominal ~5 nm and ~50 nm In thin films deposited on three substrates: sputtered SiN_x, SiC_x and ZnO_x:Al (i.e. AZO). Based on these results, we assume that substrate material dependence of In thin film deposition can be omitted for the moment, and comparable to the deposition on *c*-Si wafer with native oxide.

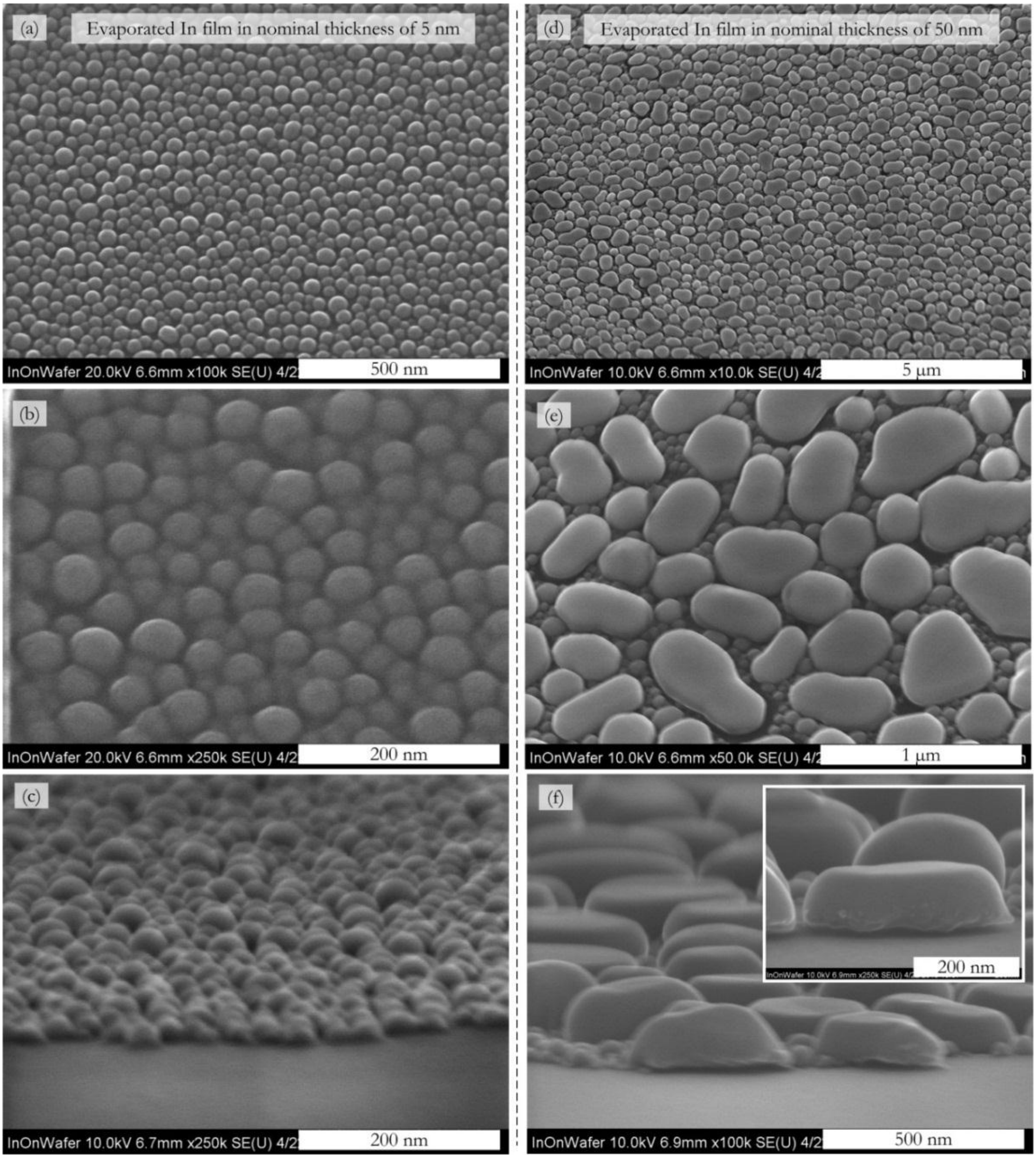

Figure 2.2 SEM images showing the microstructures of indium thin films evaporated on Si wafer with native oxide: (a-c) SEM images of In thin film with nominal thickness of ~5 nm, tilt angle of 75° in (c); (d-f) SEM images of In thin film with nominal thickness of ~50 nm, tilt angle of 75° in (f).

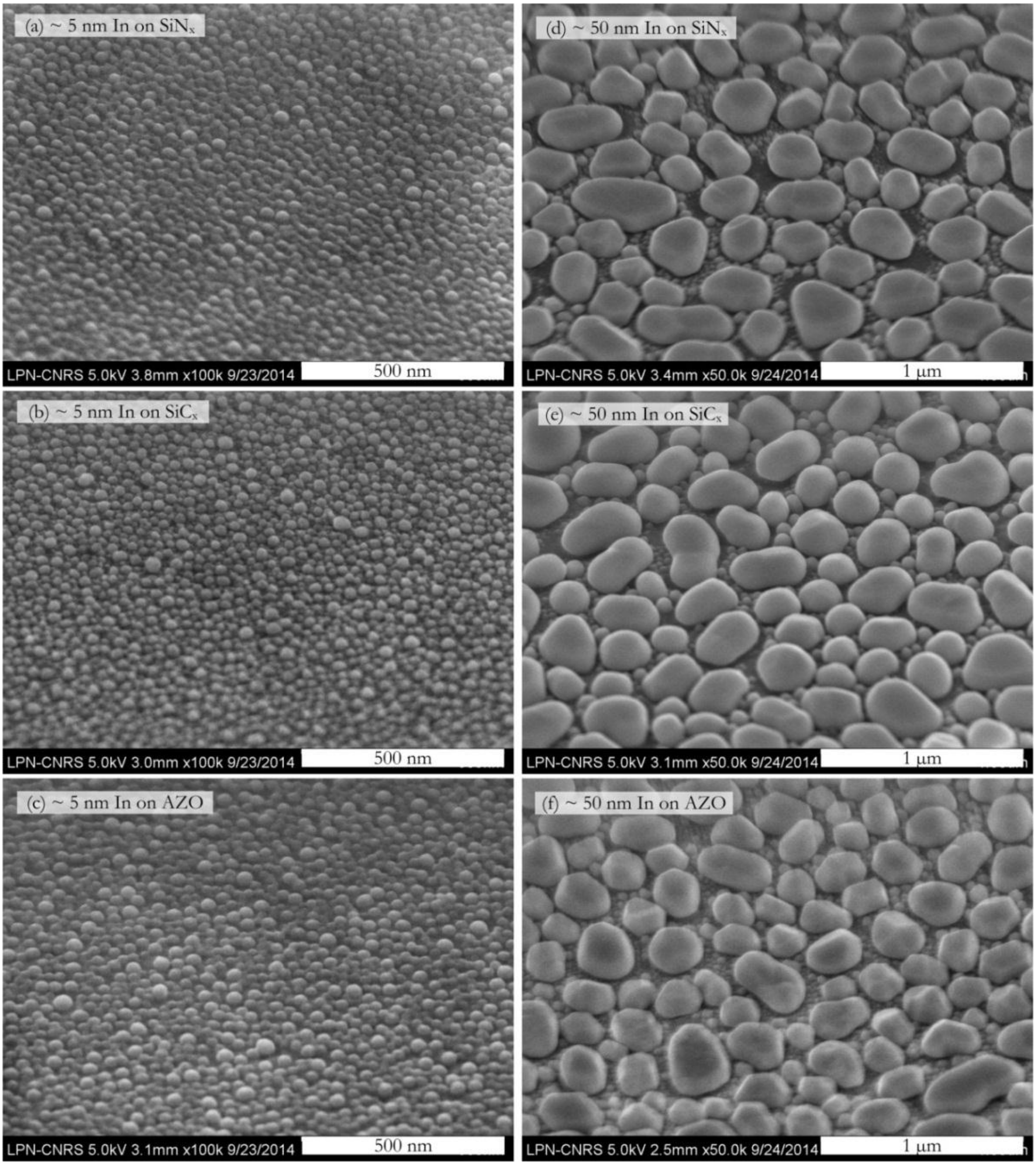

Figure 2.3 SEM images of indium thin films evaporated on different substrates: room temperature sputtered SiN_x, SiC_x, and ZnO_x:Al (AZO).

2.3.2 H_2 PLASMA REDUCTION FOR THE a-SI:H/INDIUM CONTACT

In contrast with Au, H_2 plasma treatment on In thin films is a requirement before introducing Si precursors for the SiNWs growth [33]. Figure 2.4 shows the SEM images of failure of SiNWs growth without H_2 plasma treatment (only with *a*-Si:H coating and annealing), with no chemical reaction between *a*-Si:H coating layer and the In thin film beneath it.

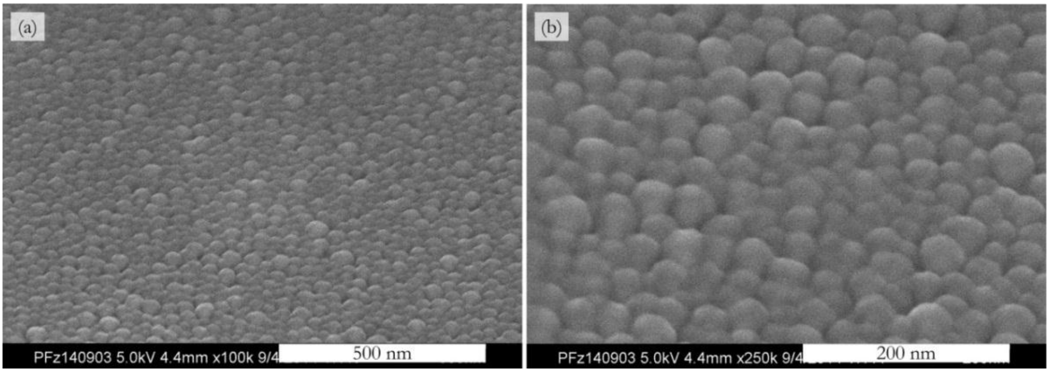

Figure 2.4 Failure of SiNW growth without H_2 plasma treatment, showing that the In thin film was coated by an *a*-Si:H layer with no reaction, note that the substrate is Si wafer with native oxide.

It is known that a self-passivating layer of native oxide can form on the surface of In thin film even at room temperature [51]. As In thin films are exposed to air after the evaporation, this self-passivation process is quite probable. In addition, the surface oxidation might occur during the pumping stage in the PECVD system as the substrate heater is set at 160°C. TEM analysis of the evaporated In films with EELS analysis confirms the oxidation of the In. Figure 2.5 provides the TEM-EELS analysis of a typical island-like In thin film evaporated on a Si_3N_4 membrane. Different electron diffraction patterns were observed in the centre and two sides of In island surface. Further nano-scale EELS analysis shows that the larger peaks around 540 eV (contributed by oxygen) in the spectrum were obtained on the left and right side of surface, compared to the centre part, indicating that the surface of the In islands is oxidized. Thus we can conclude that the native oxide on the In surface prevents the reaction between In and *a*-Si:H. Therefore, a H_2 plasma reducing process, as expressed in (2-1), is necessary for enabling the contact between In and *a*-Si:H.

$$\mathrm{InO_x} + \mathrm{H} \rightarrow \mathrm{In} + \mathrm{H_2O(g)}, \tag{2-1}$$

where g represents that H_2O is in vapour phase as substrate temperature is set at ~150°C, above its boiling point of 100°C.

Furthermore, a typical H_2 plasma treatment is carried out on the heated substrates above the In melting point 157°C (e.g. 350°C). With the purpose of investigating the substrate heating contribution to the H_2 plasma reduction, before depositing *a*-Si:H, In thin films of different thicknesses were annealed at 350°C for 5 mins in 100 sccm, 400 mTorr H_2 atmosphere. Note that this is the same parameter set of the typical H_2 plasma treatment, except for the absence of plasma (no RF power). The results of SiNWs growth (with ~20 nm *a*-Si:H) are shown in Figure 2.6. For In thin films of ~5 nm, small Si crystals were produced, as shown in (a, b), this means that substrate heating it-self can improve the In-*a*-Si:H contact. Interestingly, numerous SiNWs were grown in the case of thicker In thin films (~50 nm), as shown in (f). Furthermore, it is found that the In surface turned to be rough, as shown in (d, e). A direct impression is that H_2 could also reduce the indium oxides on heated substrates. However, the broken surface shell of the smaller In islands highlighted in (e) indicates that most of the surface oxide survived the annealing treatment in H_2 atmosphere.

For understanding this phenomenon, a longer and intensive annealing test was carried out. Figure 2.7 shows that after 350°C annealing in the Ar/H_2 atmosphere of 400 mbar for 30 mins, the shells of surface oxide were broken and left on the substrate, with the disappearance of pure In, which must have been evaporated due to the high temperature annealing.

Thus, it is clarified that only the H_2 plasma can reduce indium oxide under our experiment conditions. However, the surface oxide shell breaking process still remains unclear, so next step is to study the influence of substrate temperature during H_2 plasma treatment.

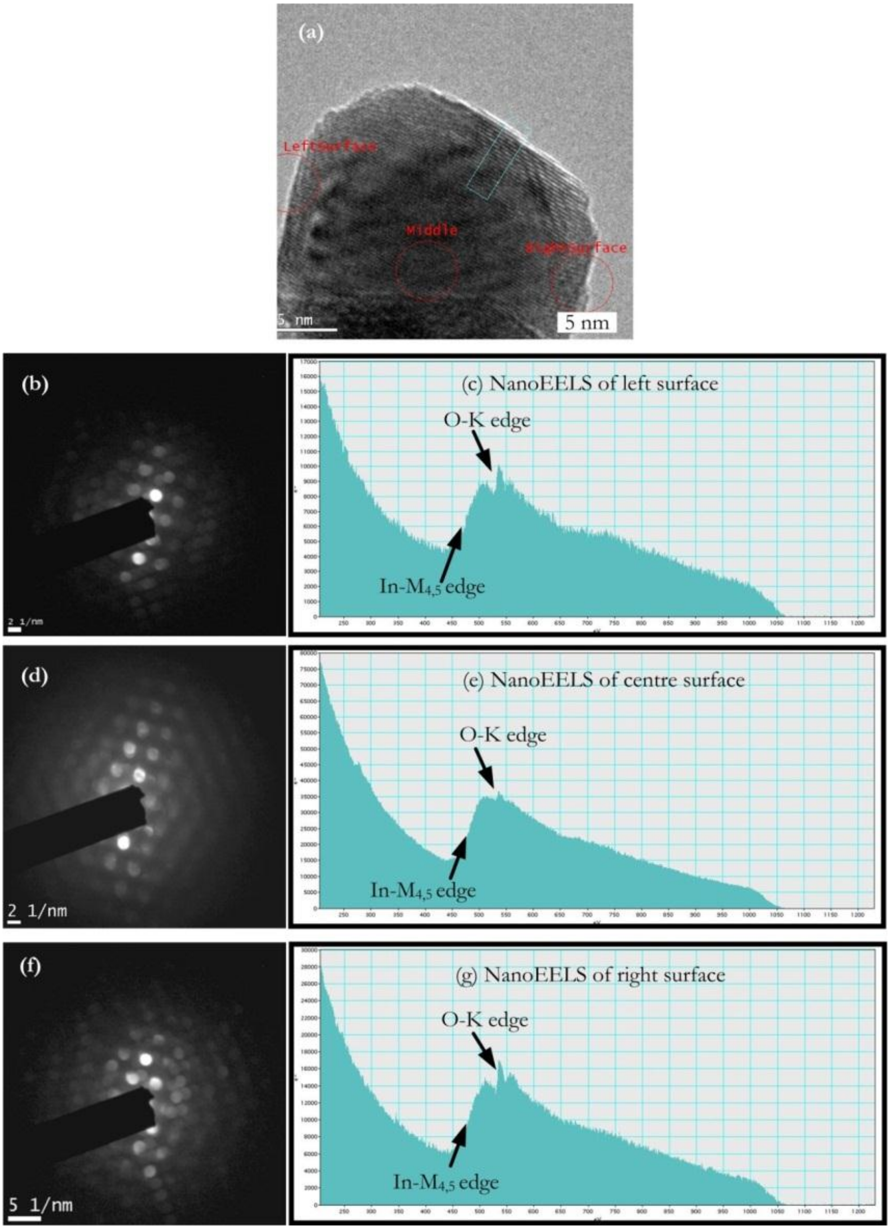

Figure 2.5 TEM-EELS analysis of In thin films: (a) TEM image of a typical In nanoparticle; (b), (d), (f) show the nano-scale electron diffraction patterns of the left, centre and right part of the indium nanoparticle, respectively. (c), (e), (g) show the chemical analysis by nano-scale EELS of the left surface, centre, and right surface, respectively. The higher contributions of oxygen element are confirmed on the left and right surface of the In nanoparticle, due to the larger O-K edge compared to the one in the central part. Also different electron diffraction patterns are observed, indicating different chemical compositions.

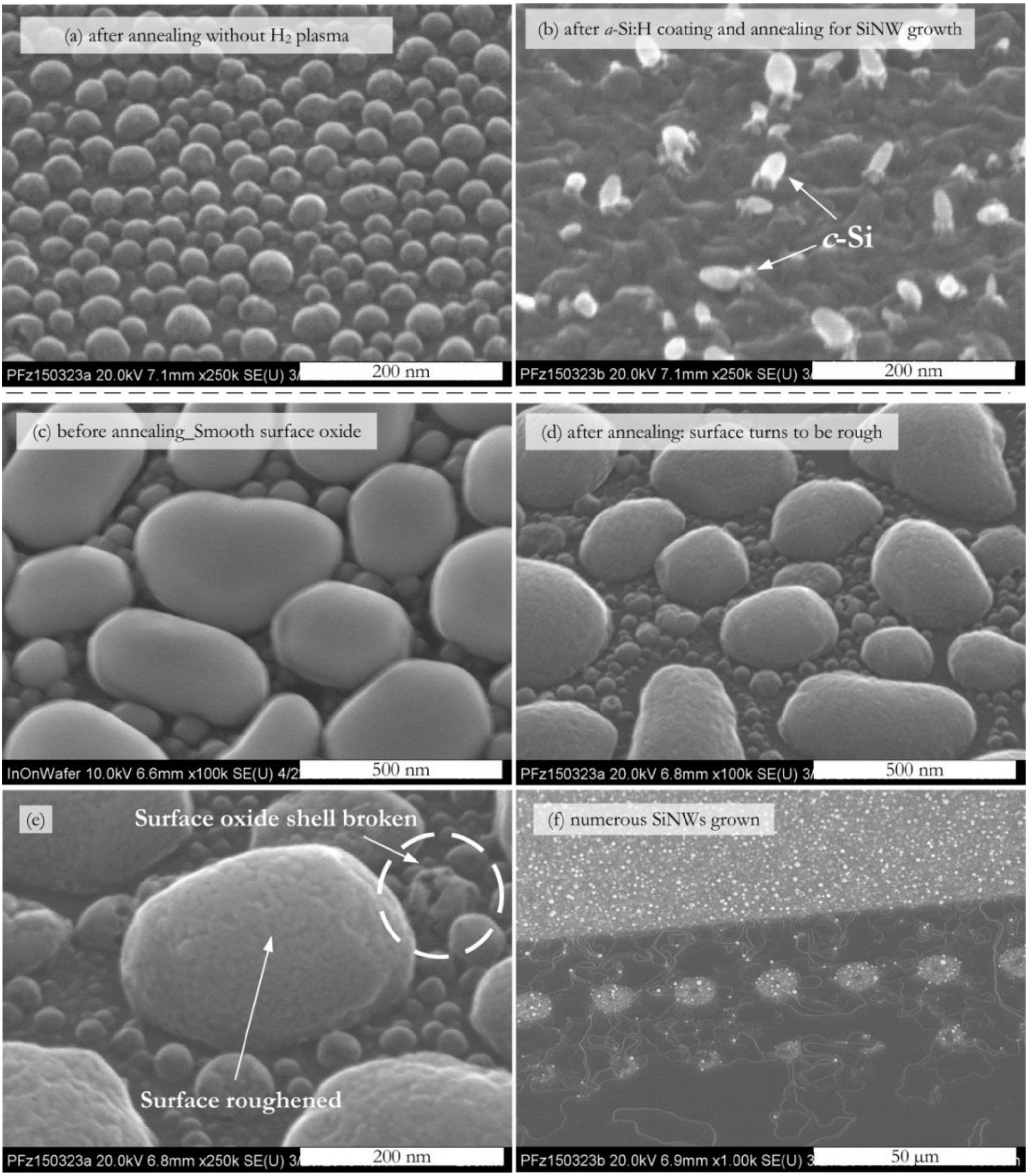

Figure 2.6 Contribution of substrate heating to the growth of SiNWs: (a)~5 nm indium thin film after annealing on heated substrate. After all the steps for SiNWs growth, small Si crystals were produced as shown in (b). (c) as-deposited ~50 nm In thin film before annealing, showing smooth surface; (d, e) ~50 nm In thin film after annealing, with roughened surface and some small NPs with broken surface; (f) for ~50 nm In thin film after annealing, numerous SiNWs were grown, instead of small Si crystals. Note that the substrate is a *c*-Si wafer with native oxide.

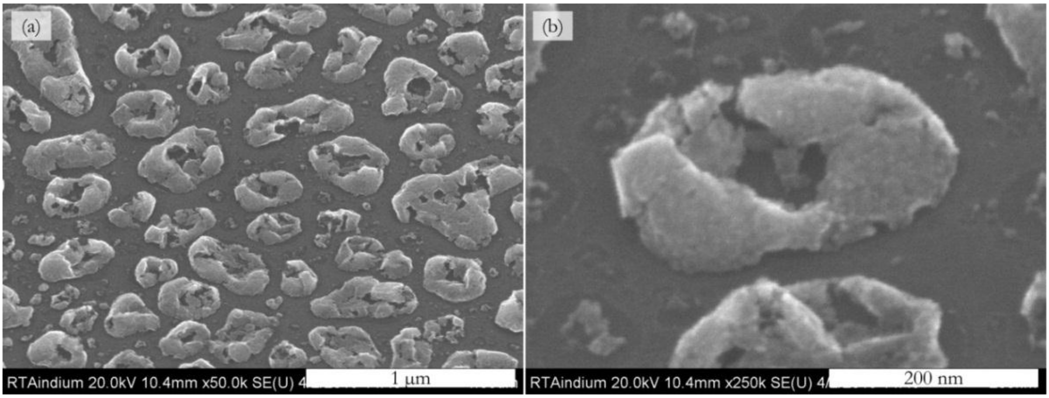

Figure 2.7 SEM images of an indium thin film in nominal thickness of ~50 nm after annealing at 350°C in H_2/Ar mixture gas at 400 mbar for 30 mins. Note that the substrate is Si wafer with native oxide.

2.3.3 EFFECT OF SUBSTRATE TEMPERATURE ON THE REDUCTION OF INDIUM OXIDE

In principle, the substrate temperature is a critical parameter in thin film processing techniques. It activates the surface chemical reactions (e.g. reactive ion etching of ITO by CH_4/H_2 gas mixture above 60°C [52]), determines the thin film optical, structural and electrical properties (e.g. ion beam sputtered ITO at different substrate temperatures [53]), affects the deposition rate (e.g. *a*-Si:H deposition in PECVD system [54]), the etching rate [52][55][56], and etching selectivity [57]-[61] etc. Besides, it is also necessary to operate certain III-V plasma etching processes on heated substrates for volatizing chemical etchants (e.g. fluoride or chloride plasma above 150°C [62]).

Thus, we studied the effect of the substrate temperature on H_2 plasma reduction process (i.e. at different temperatures of 150°C, 250°C and 350°C).

In the case of a 5 nm In thin film, as shown in Figure 2.8, we found that there is almost no redistribution of In NPs due to the H_2 plasma treatment (100 sccm, 400 mTorr, 5 watts, 5 mins) at three different substrate temperatures, as shown in (a), (c), and (e). After ~20 nm *a*-Si:H coating and annealing at 450°C, only small Si crystals were produced from the In thin film treated by H_2 plasma at 150°C, as shown in (b), indicating that the H_2 plasma reduction is not sufficient. Also, this phenomenon is quite similar to the case of growth failure of SiNWs from In thin film treated by thermal annealing in H_2 atmosphere instead of H_2 plasma as shown in Figure 2.6 (b). However, the difference between H_2 plasma treatments at 250°C and 350°C (above melting point of In) can be neglected, as shown in (d) and (f).

In the case of ~50 nm In thin film, as shown in Figure 2.9, after the same H_2 plasma exposure, no redistribution of In NPs was observed, which is in agreement with the case of ~5 nm In thin film. However, in contrast to ~5 nm thin film, after ~20 nm *a*-Si:H coating and annealing at 450°C, SiNWs were successfully grown from In thin film treated by H_2 plasma at 150°C, as shown in (b). This result is similar to the case of SiNWs growth from In thin film treated by thermal annealing at 350°C in H_2 atmosphere instead of H_2 plasma as shown in Figure 2.6 (f). Another important result is the change in the morphology of the In thin films. Indeed, In thin films after H_2 plasma on substrates heated at 250°C and 350 °C turned to be spherical after solidification (i.e. phase transition from liquid back to solid), as shown in Figure 2.9 (c) and (e), in comparison with the island-like In thin film by H_2 plasma at 150°C (below the melting point of In) as shown in (a). As spheres have the lowest **surface-area-to-volume ratio** (the value is 4.8 for for unite volume [63]). Assuming that the volume loss of In thin film can be omitted, this morphology evolution can be explained by the In surface energy minimization induced by thermal annealing, as the surface energy positively correlates with the surface area [64].

In addition, the thermal annealing-induced oxide shell roughening and breaking phenomenon in 2.3.2 (see Figure 2.6.d and e, and Figure 2.7) can be explained by the phase transition-induced indium reshaping, as illustrated in Figure 2.15 (page 69). Due to the annealing above the In melting temperature, the core of the solid island-like In NP starts to become a liquid spherical cap (see 3.3), however this process is inevitably constrained by the solid oxide shell. The oxide shell itself gets wrinkled or even broken caused by this core/shell interplay during the In phase transition. This can explain NW growth on large indium droplets without H_2 plasma.

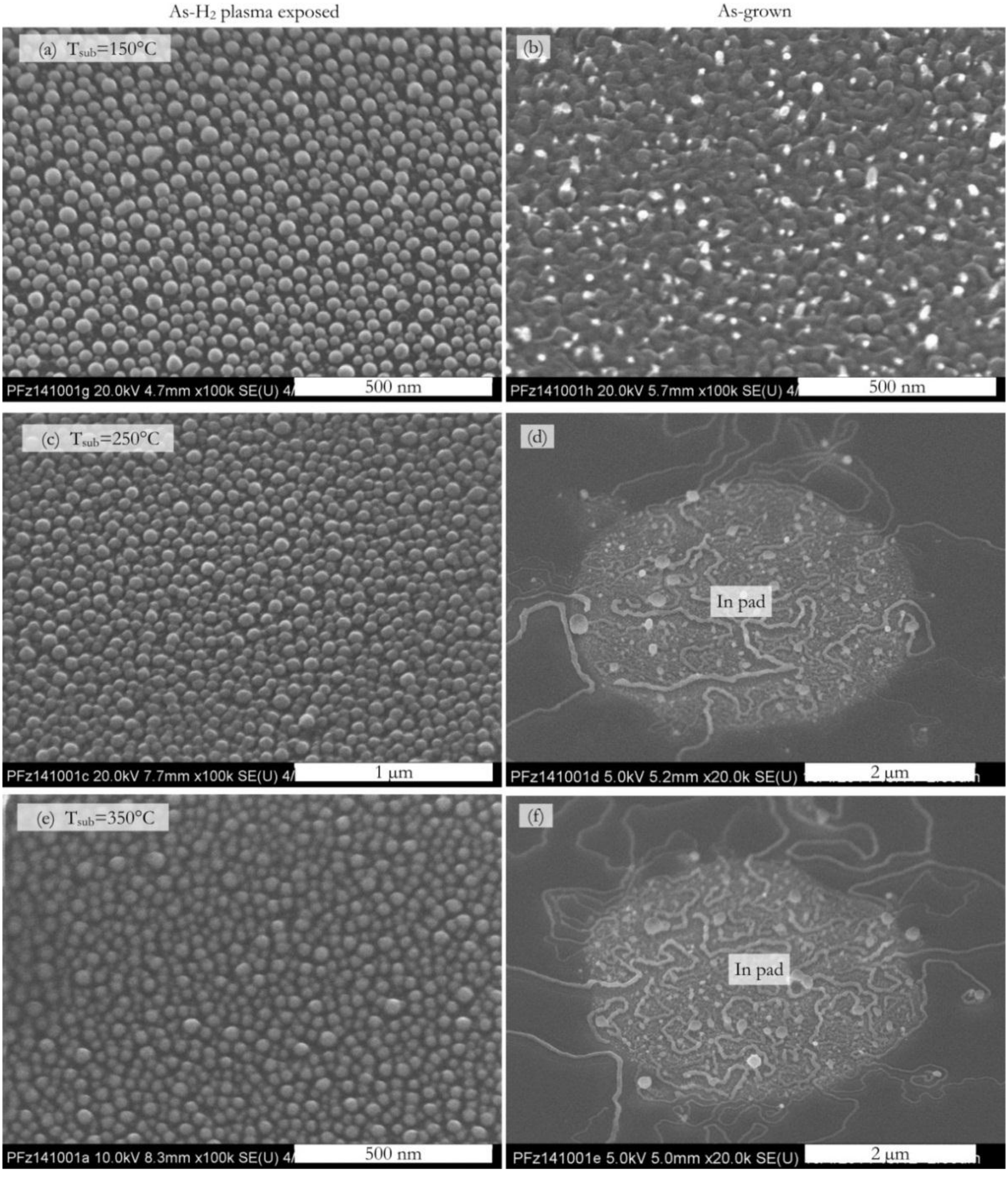

Figure 2.8 H_2 plasma treatment (100 sccm, 400 mTorr, 5 watts, 5 mins) of 5 nm In film on *c*-Si substrate with their native oxides at different substrate temperatures (a, c, e) and the corresponding results of SiNWs growth (after ~20 nm *a*-Si:H coating and annealing at 450°C) from indium pads of ~5 nm thick (b, d, f).

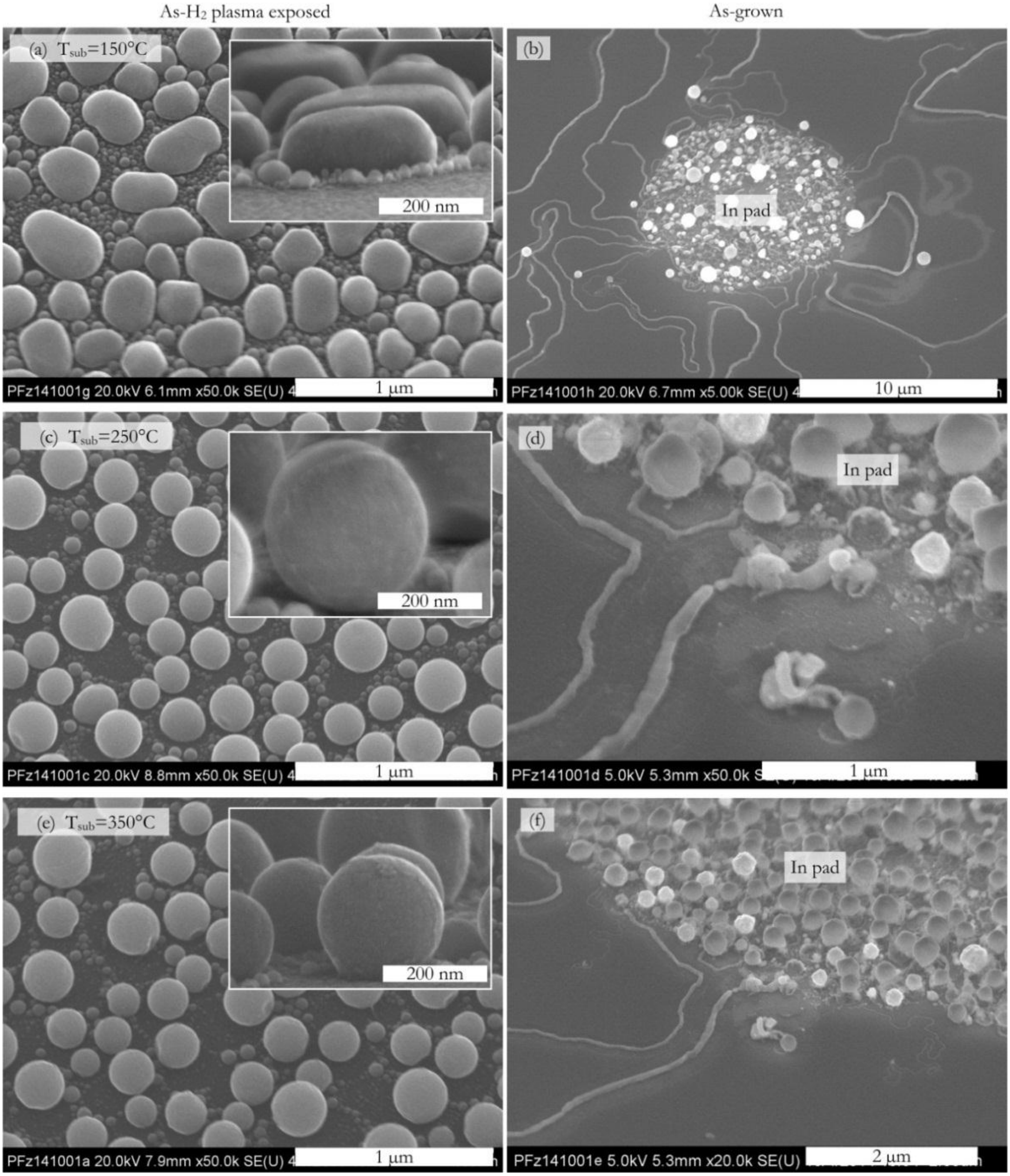

Figure 2.9 H_2 plasma treatment (100 sccm, 400 mTorr, 5 watts, 5 mins) of 50 nm indium film on *c*-Si substrate with their native oxides at different substrate temperatures (a, c, e) and the corresponding results of SiNWs growth (after ~20 nm *a*-Si:H coating and annealing at 450°C) from In pads in thickness of ~50 nm (b, d, f).

Table 2.1 summarizes the results of In-*a*-Si:H interaction after the two treatments on the In thin films: (1) annealing In thin films at 350°C in H_2 atmosphere for 5 mins without plasma, as shown in Figure 2.6; (2) H_2 plasma exposure to In thin films at 150°C for 5 mins, as shown in Figure 2.8 and Figure 2.9. For both cases of ~5 nm In thin film, only Si crystals were obtained but not nanowire growth, however SiNWs growth were successful in the cases of ~50 nm In thin film. This gives insight that there exists a size effect on the *a*-Si:H/In interaction. It is known that the native indium oxide formation is a self-passivation process, which means that the oxidation process cannot propagate deep inside the In thin films, hence the thickness of surface oxide shell does not vary much for In thin films of different thicknesses. Hence, thicker In thin films have higher **core-to-shell volume ratio**, where **core** and **shell** represent the In inside and the surface native indium oxide layer, respectively. In thin films with high core/shell ratio favour the breaking of the oxide shell and therefore are more favourable for building up the In-*a*-Si:H contact required for SiNW growth under the circumstance of insufficient reduction of surface oxide.

Table 2.1 Summary of In-*a*-Si:H interaction after two different In thin film treatments

Thin film treatment	Annealing at 350°C in H_2 atmosphere without plasma for 5 mins[1]	H_2 plasma at 150°C substrate temperature for 5 mins[2]
~5 nm In	Si crystals	Si crystals
~50 nm In	SiNWs	SiNWs

2.3.4 EFFECTS OF THE SUBSTRATE PROPERTIES ON INDIUM NPS REDISTRIBUTION

As concluded above, there is no evolution of the size and density of In NPs by heating the *c*-Si wafer with native oxide at various temperatures from 150°C to 350°C. However, two cases of In NPs coalescence were observed during a H_2 plasma treatment, which provide us insight on the effect of substrate properties on In NPs redistribution.

2.3.4.1 INDIUM NPS COALESCING ON MICROCRYSTALLINE SI SUBSTRATES

Indium with a nominal thickness of 5 nm was evaporated on a microcrystalline silicon (*μc*-Si:H) thin film (100 sccm 1.9 Torr of H_2, 50 mTorr 2 sccm of SiH_4, 20W, T_{sub}=150°C, 5 mins). After our standard H_2 plasma treatment (100 sccm, 400 mTorr, 5 W, T_{sub}=300°C, 5 mins), we observe a strong coalescence of In NPs, as shown in Figure 2.10.a, b, c, d. However no crystalline silicon nanowire was observed. Spectroscopic Ellipsometry characterization shows that *c*-Si is the dominant fraction in the thin film, as shown in Figure 2.11. A control group of *μc*-Si:H coating on the same In thin film was annealed in the same batch but also in this case no Si crystallization events occurred, as seen in Figure 2.10.e, f. Therefore, for both types of In/*μc*-Si:H bilayer structures, the chemical interaction between

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[1] See Figure 2.6

[2] See Figure 2.8 and Figure 2.9

liquid In and the amorphous silicon phase (27%) in the *μc*-Si:H film can be omitted. Therefore, the root cause of liquid In diffusing and coalescing on *μc*-Si:H should not be the *a*-Si:H element on the substrate. The possible reason should be other properties of the *μc*-Si:H substrate, which still remains unclear.

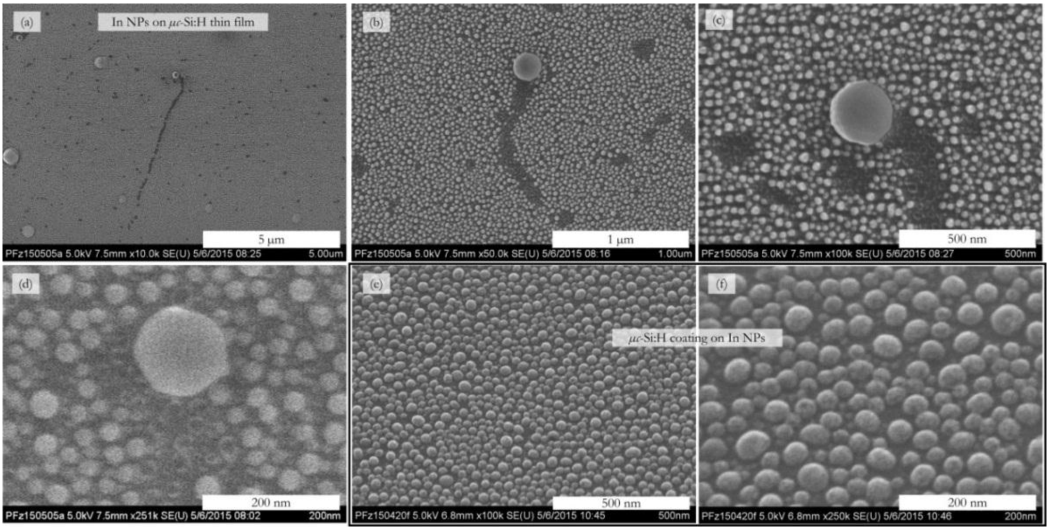

Figure 2.10 In NPs diffusing and coalescing on a hydrogenated microcrystalline silicon (*μc*-Si:H) thin film deposited on *c*-Si wafers with native oxide: (a, b, c, d) SEM images showing the coalescing behaviour of In NPs on *μc*-Si:H; (e, f) SEM images of control group of In NPs coated with the same *μc*-Si:H thin film, with no coalescence.

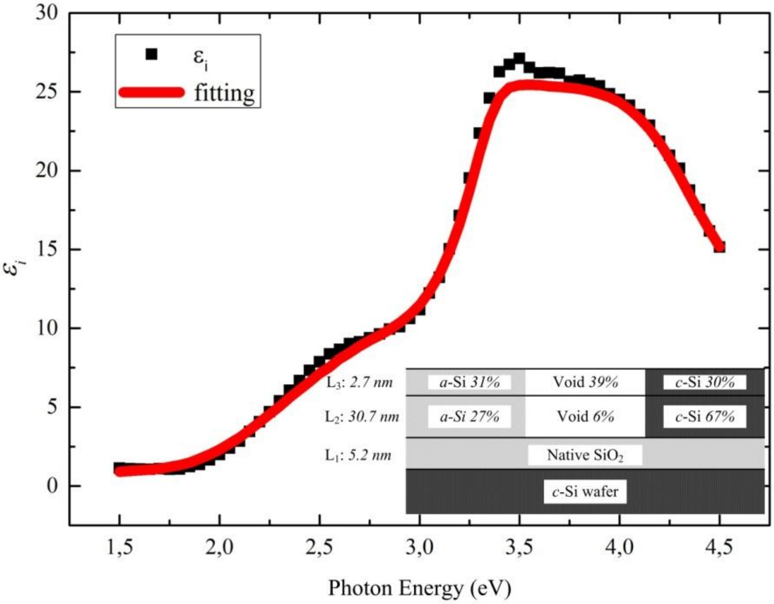

Figure 2.11 Fitting of the imaginary part of the pseudo-dielectric function ε_i measured by Spectroscopic Ellipsometry for a *μc*-Si:H thin film deposited on a *c*-Si wafer with native oxide. Fitting model is from [65].

2.3.4.2 INDIUM NPS COALESCING ON POLYCRYSTALLINE AL-DOPED ZNO SUBSTRATES

A coalescing phenomenon quite similar to the liquid In (thin film in thickness of ~50 nm) coalescing on *μc*-Si:H (see Figure 2.10) was observed occasionally when a standard H_2 plasma treatment was applied to evaporated In on RT-sputtered Al-doped ZnO (AZO), as shown in Figure 2.12. Assuming that no Si material contaminates the AZO substrate, it is the AZO substrate itself which should provide the driving force for the liquid In diffusing and coalescing on AZO.

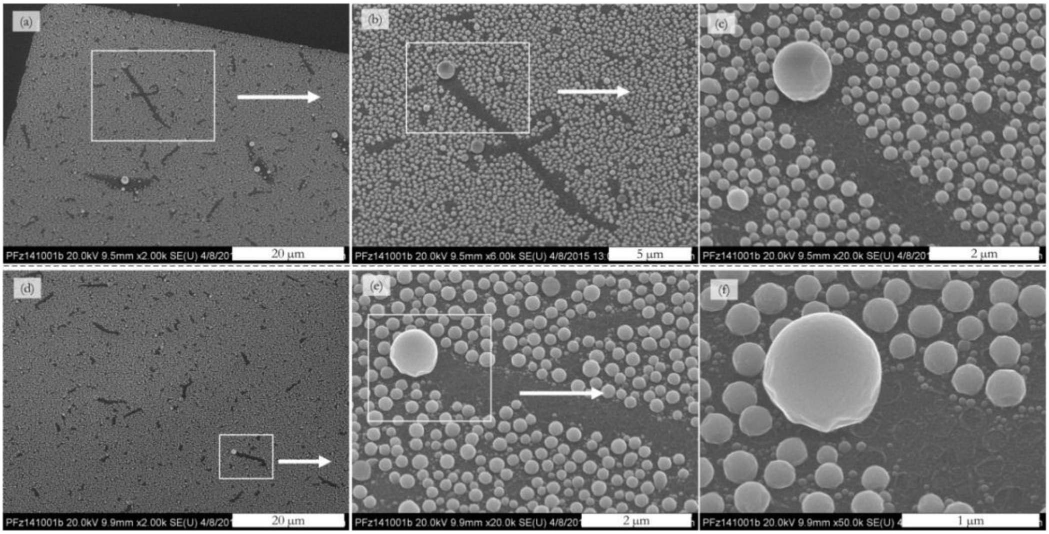

Figure 2.12 In NPs diffusing and coalescing on Al-doped ZnO (AZO) substrate.

2.3.4.3 GRAIN-BOUNDARY WETTING INDUCED COALESCING MECHANISM

The similarity of liquid In diffusing and coalescing phenomena on *μc*-Si:H and AZO substrates can be related to similar features in solid surface properties. It is known that a liquid can spontaneously move on a substrate with a thermal or chemical gradient as driving force (see 3.1.2).

In the case of a H_2 plasma treatment on heated substrates, given that: 1) substrate heating is isotropic; 2) chemical reactions between liquid In and the substrates can be ignored; it can be deduced that the surfaces of *μc*-Si:H and AZO must have a certain chemical gradient due to their intrinsic properties, and the most probable one is the presence of grain boundaries (GB) which provide excess free energy per unit area with respect to an homogeneous surface [66].Thus liquid In prefers to wet the GBs on these two substrates rather than the grains with relatively low surface free energy. Note that like ITO thin film[3], the RT-sputtered AZO can also experience phase transition from amorphous to polycrystalline on heated substrate [67].

As a matter of fact, the grain boundary wetting (GBW) or GB penetrating is a hot topic in the field of liquid metal embrittlement (LME) induced structural fracture [68]-[70]. This type of behaviour was studied experimentally (e.g. liquid Ga on Al [71]-[73]) and theoretically [74]-[77]. Figure 2.13 shows an example of liquid metal wetting on GB. A continuous penetration and accumulation of liquid Ga along the grain boundary of an Al bicrystal was observed *in-situ* by synchrotron radiation X-ray microradiography [73]. Based on the GBW mechanism [77], the liquid In coalescing process is illustrated in Figure 2.14.

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[3] The phase transition by substrate annealing is discussed later in detail in 2.4.3.

This mechanism will be used to understand In NPs formation on ITO sidewalls (see 4.2.2), which enables a reproducible positioning of In NPs for self-organizing the in-plane SiNWs.

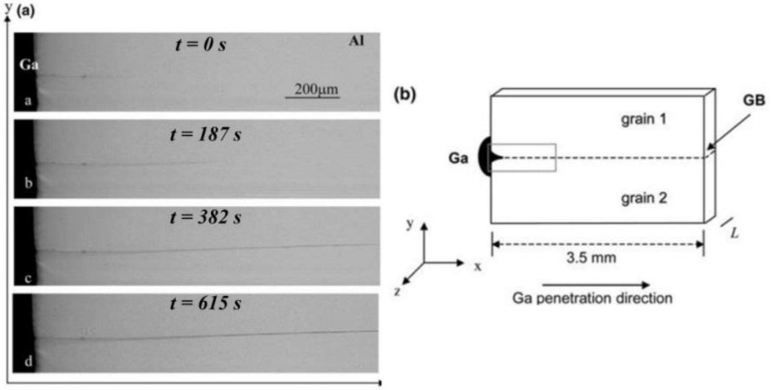

Figure 2.13 An example of liquid gallium wetting on an allumium GB: (a) continuous penetration an thickening of liquid Ga along the grain boundary of an Al bicrystal; (b) schematic of the Al bicrystal in contact with the liquid Ga [73].

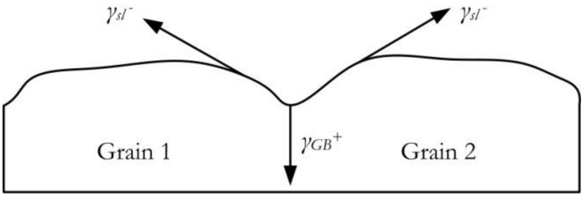

Figure 2.14 Schematic representation of the profile of a Mullins groove with two grains and a grain boundary [74]: as a surface energy gradient exists on such kind of a solid surface, liquid In tends to diffuse from low surface energy sites (γ_{sl}^{-}) to higher ones (γ_{GB}^{+}), which results in the coalescence at the grain boundary.

2.3.5 CONCLUSION

Based on the analysis above, the process of H_2 plasma on heated substrates is schematically illustrated in Figure 2.15.

Generally speaking, in the case of an evaporated In thin film, H_2 plasma reduces its native surface oxide, which enables the *a*-Si:H/In contact between In and *a*-Si:H for the SiNWs growth. An efficient H_2 plasma treatment needs to be operated on a heated substrate (e.g. at nominal 350°C). At such temperature the In NPs experience a morphology evolution during the phase transition: from solid islands based on VW growth mode to liquid spherical-caps after removing the surface oxide (above its melting point), and turn to be solid spheres by solidification due to the surface energy minimization.

At low substrate temperature (e.g. at 150°C), the reduction of indium oxide by H_2 plasma is less efficient. However the substrate temperature and heating time should be moderate, as intensive annealing can cause a loss of In. Size effect of In islands was also observed, as In in the core can wrinkle or even break the oxide shell during the phase transition during substrate annealing process, which also makes In/*a*-Si:H contact available, however this method is not recommended for ultrathin In thin film considering the Core/Shell ratio and interplay.

Finally, no obvious redistribution of In NPs on SiO_2 (a substrate with relatively homogeneous surface chemistry) was observed after H_2 plasma at different temperatures. However, it turns to be possible on micro/poly-crystalline substrates based on grain boundary wetting kinetics, even though this approach still remains uncontrolled.

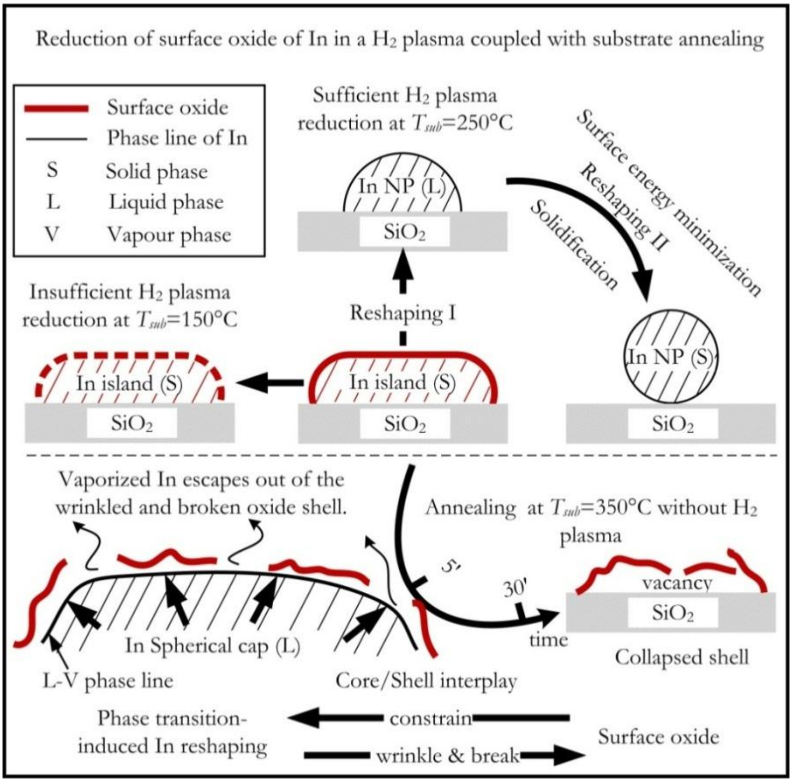

Figure 2.15 Illustration of surface oxide reduction of evaporated In thin film by H_2 plasma coupled with substrate annealing.

2.4 INDIUM NANOPARTICLES FORMATION ON SPUTTERED ITO THIN FILMS

Forming In NPs on its oxide thin film is another route for obtaining In NPs [46]-[48]. Indeed, the oxygen on ITO[4] surface is reduced by H_2 plasma on heated substrates [52] and In atoms are released and form In NPs[5], as shown in Figure 2.16. However, as shown in (c) and (d), In NPs are randomly formed with uncontrolled sizes and density (i.e. broad NPs distribution), which is detrimental for the following SiNWs growth and applications (see 4.2.2). In order to control the In NPs distribution, the mechanism of In NPs formation on ITO is firstly investigated, based on which a method of controlling the In NPs distribution is proposed. In the following, the crystallization of ITO and the effects of H_2 plasma parameters are discussed.

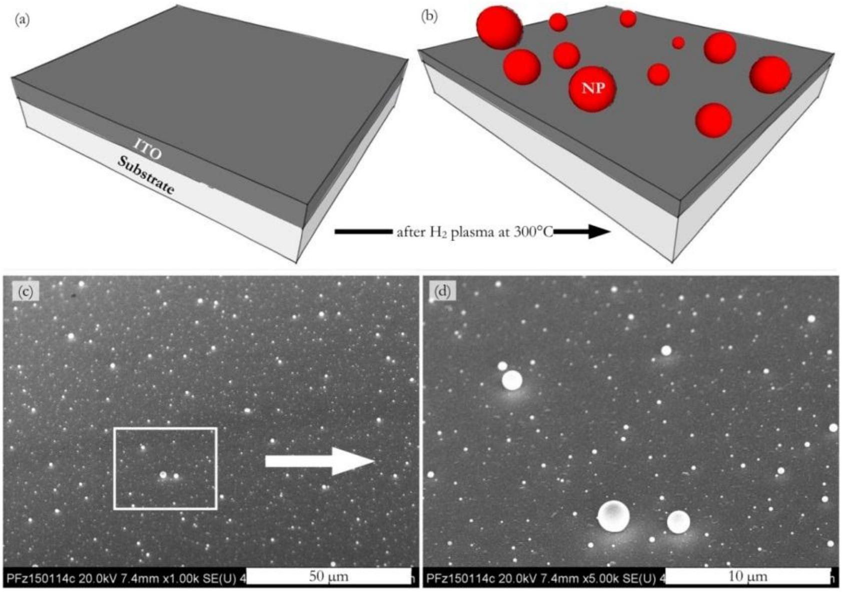

Figure 2.16 In NPs formation on ITO surface: (a, b) schematic of In NPs forming on ITO surface; (c, d) SEM images of In NPs formed on ITO surface with a broad distribution.

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[4] Without notation, the ITO thin films are deposited at room temperature by RF magnetron sputtering.

[5] To be precise, a NP formed on an ITO surface is a composition of In and Sn. Our EDX measurement reveals it as an In-rich In-Sn alloy with 11.9% atomic fraction of Sn [78], which is in liquid phase above ~140°C [79] (lower than the indium melting point). Therefore, we simply consider this In-rich In-Sn alloy NPs as In NPs, and do not consider the Sn contribution to the In NPs formation on ITO surface. Further studies on the differences between these two types of NPs and this contribution to the in-plane SiNWs growth and electrical properties are certainly interesting but out of the scope here.

2.4.1 MECHANISM OF INDIUM NPS FORMATION ON ITO

In contrast with evaporated In thin films, the formation of In NPs on ITO is a **growth process** based on the reduction of ITO by a H_2 plasma. In order to understand the In NPs formation mechanism on ITO substrate, substrate heating and plasma reducing effects are considered, as in the case of evaporated In thin films.

2.4.1.1 SUBSTRATE TEMPERATURE DEPENDENCE OF INDIUM NPS FORMATION

In NPs formation on a ITO surface was carried out thanks to a H_2 plasma treatment (400 mTorr, 100 sccm, 5W, 5 mins) at different substrate temperatures, as shown in Figure 2.17. No In NPs were formed at T_{sub}=200°C, however the ITO surface was roughened (see image b), implying the H_2 plasma reduction is activated. From T_{sub}=300°C to 500°C, the density of In NPs decreases while the size increases.

Mohri *et al.* studied the CH_4/H_2 plasma etching to ITO thin films [52]: (1) the etch rate of ITO thin film by CH_4/H_2 increases when the substrate temperature arises; (2) pure CH_4 plasma cannot etch ITO and results in the deposition of carbon film. The authors mentioned that hydrogen reduces oxygen in the thin films first and then In and Sn get volatile by reacting with CH_3 species. Therefore, the oxygen reduction process by H_2 plasma has a positive correlation with substrate temperature, which is also in agreement with the conclusion from evaporated In thin film study (see 2.3.5). This means that more In atoms are released from ITO surface under H_2 plasma at higher substrate temperatures.

However, the mechanism of In NPs formation from the released atoms is still unclear. Of course increasing the substrate temperature should enhance the surface diffusivity of In atoms and/or liquid NPs, thus small NPs migrate and coalesce into large ones on ITO surface. But no redistribution of In NPs on SiO_2 was observed at various substrate temperatures (see 2.3.3). This suggests that ITO heating substrate plays a prime role on the indium atomic surface diffusivity.

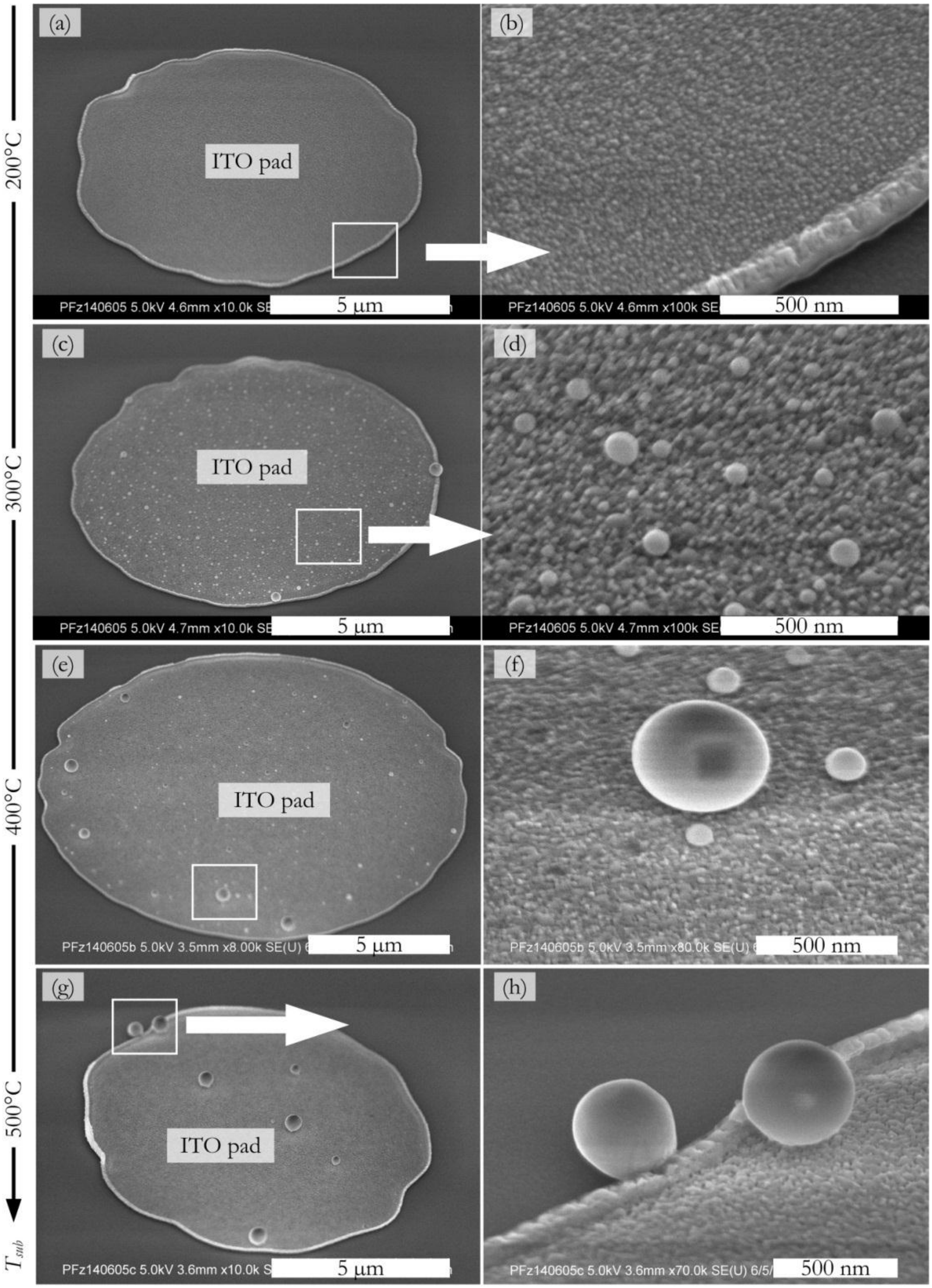

Figure 2.17 SEM images of In NPs formation on an ITO pad upon H_2 plasma treatment (H_2 400 mTorr, 100 sccm, 5W, 5 mins) at different substrate temperatures.

2.4.1.2 INVESTIGATION OF ITO SURFACE EVOLUTION

In order to verify the assumption that In atoms and/or liquid NPs are more likely to diffuse on ITO than on c-Si with native oxide on heated substrate, three tests were carried out. Furthermore, the ITO surface evolution upon H_2 plasma reduction is also revealed in some degree.

TEST I: SUBSTRATE HEATING EFFECT ON THE RELEASED IN FROM ITO SUBSTRATES

In order to discriminate the possible contribution of H_2 plasma to the In atoms and/or liquid NPs diffusion on ITO surface, we adopted the following strategy: 1) first, release In atoms on ITO surface by H_2 plasma reduction (400 mTorr, 100 sccm, 5 W) at 150°C, which modifies the ITO surface into an indium-rich solid phase, therefore the In/ITO bilayer is formed; 2) then annealing the substrate in 400 mTorr H_2 atmosphere at 300°C for 5 mins. SEM images in Figure 2.18 show that no large In NPs were formed, indicating that no significant In surface diffusion and coalescence occurred.

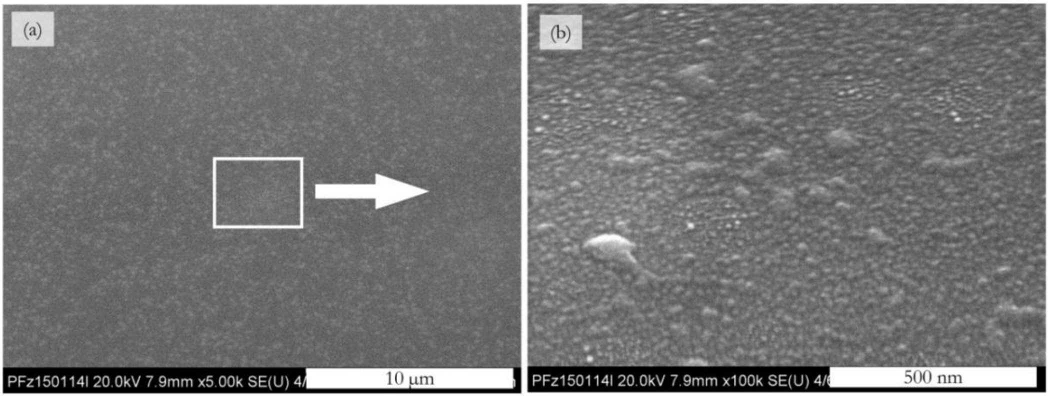

Figure 2.18 SEM images of ITO surface treated by H_2 plasma (400 mTorr, 100 sccm, 5 W) at 150°C for 5 mins, and then followed by 5 mins annealing at 300°C in 400 mTorr H_2 atmosphere.

TEST II: SUBSTRATE HEATING EFFECT ON IN EVAPORATED ON ITO SUBSTRATES

An alternative way to form In/ITO bilayer is by evaporating In on ITO substrate, after removing the surface indium oxide by 5 vol. % HCl etching for 3s, we immediatly annealed the substrate at 300 °C in 400 mbar H_2/Ar mixture gas for 5 mins. Figure 2.19 shows the SEM results of ~50 nm evaporated In on ITO substrate. Like In on SiO_2, evaporated In thin film on ITO surface also follows the Volmer-Weber mode, indicating that In atoms prefer to bind to each other rather than to the ITO surface. Comparing the morphologies of NPs with and without HCL dipping confirms the removal of the surface oxide by HCL, which is in agreement with our previous study on heating the evaporated In with and without H_2 plasma (see Figure 2.6 and Figure 2.9). This indicates that the HCl dipping is efficient for etching the oxide shell. However, in agreement with Test I, no remarkable redistribution was observed.

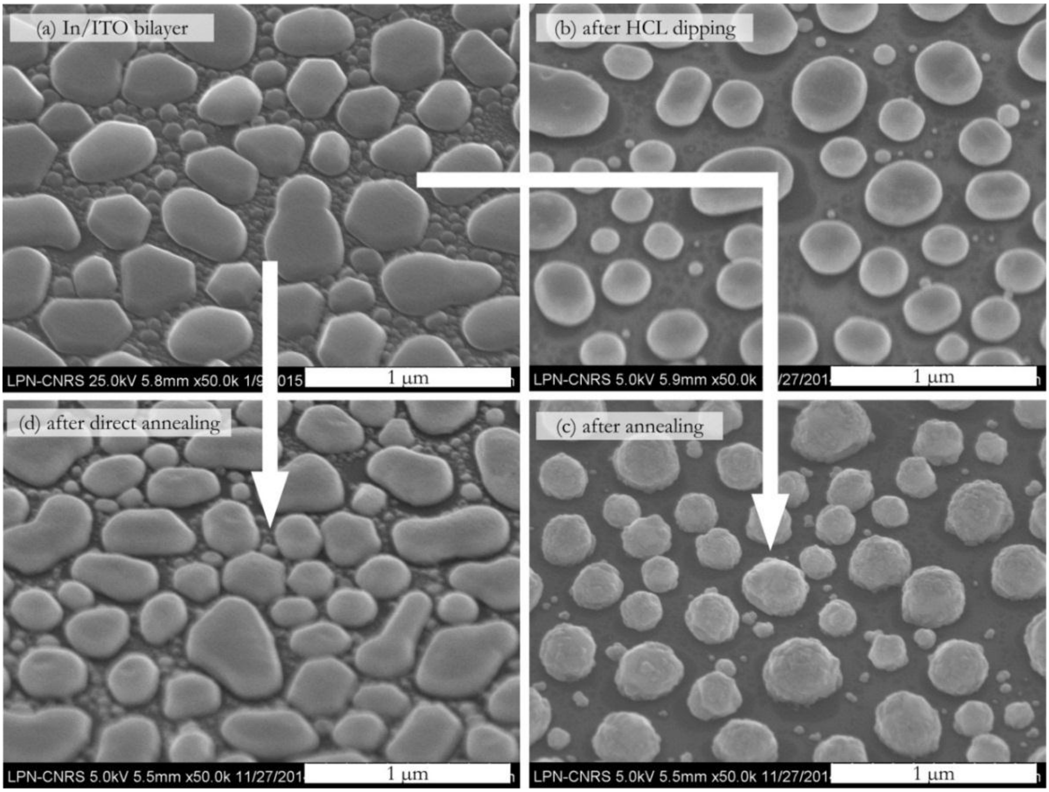

Figure 2.19 SEM images of ~50 nm evaporated indium on RT sputtered ITO treated by 5 vol. % HCL etching for 3s and followed by 300 °C annealing in 400 mbar mixture gas of H_2/Ar for 5 mins.

Test III: H_2 plasma reducing effect on In evaporated on ITO substrates

Treating the samples same as Test II by a standard H_2 plasma exposure (400 mTorr, 100 sccm, 5W) at 300°C for 5 mins. In particles larger than 10 µm were formed on In/ITO bilayer, compared with the ones of several µm formed on pure ITO thin film, as shown in Figure 2.20.(a, b) and (e, f), respectively. Another important finding is that these huge In particles were always in the In/ITO bilayer region (see image a). And both ITO surfaces (with and without evaporated indium) after H_2 plasma treatment were found in different roughness but with similar tiny In NPs, as shown in (c, d) and (g, h), respectively. Note that as only liquid In can be solidified as spheres, thus only the tiny NPs are believed to be In, and the rough surface be the ITO.

Figure 2.21 summarizes the ITO surface evolution during these three tests.

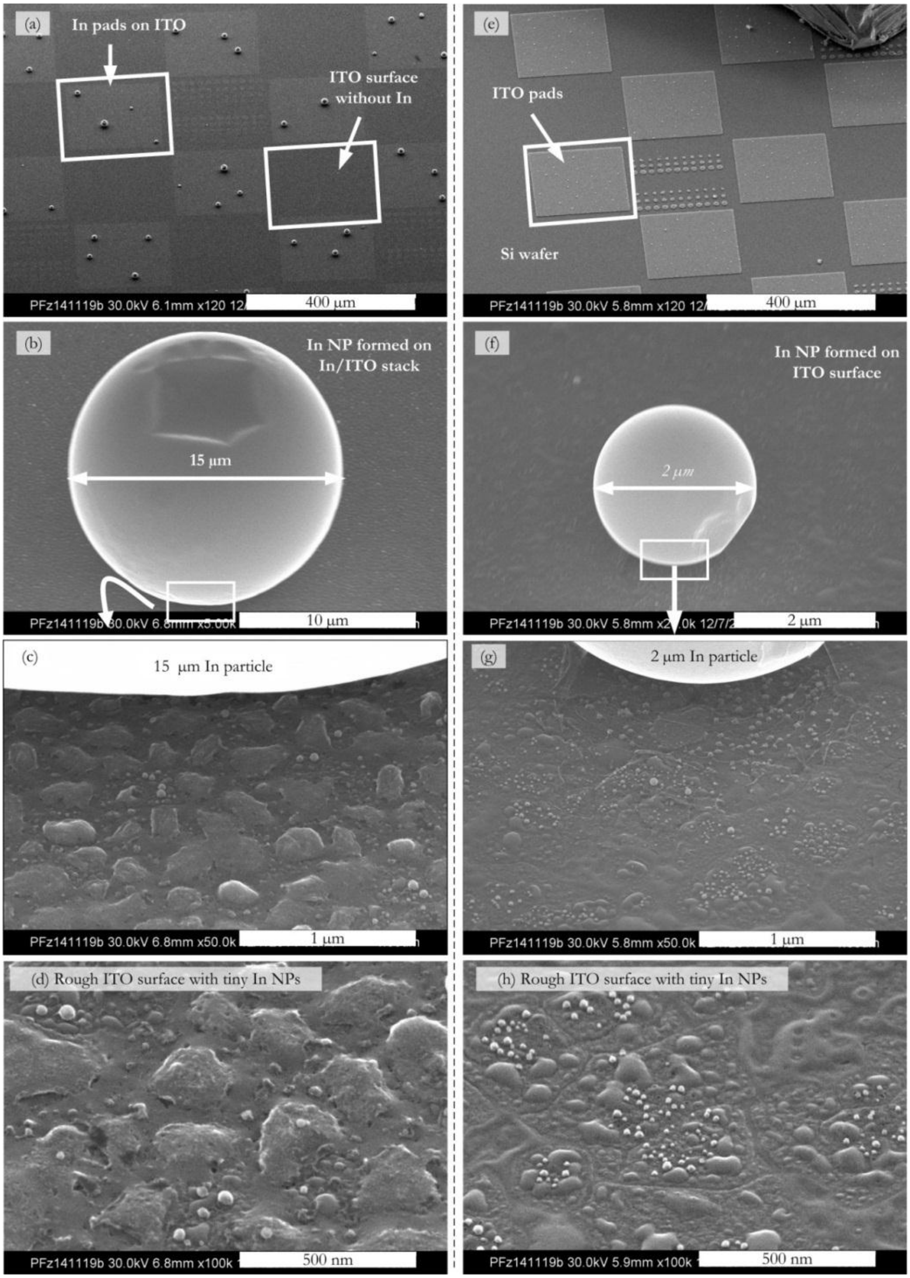

Figure 2.20 SEM images of evaporated indium pads on ITO treated by H_2 plasma at 300°C, compared with the results of ITO pads exposed to the same treatment.

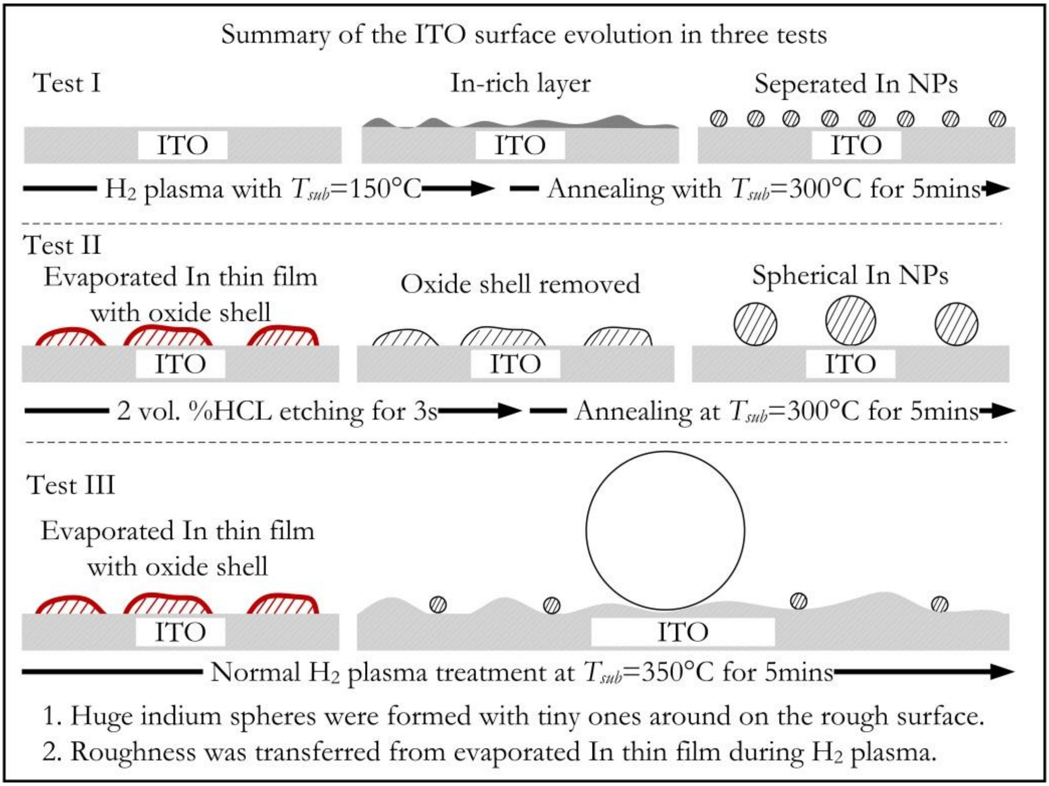

Figure 2.21 Summary of ITO surface evolution for in three testing conditions.

2.4.1.3 A GROWTH-AND-COALESCENCE MECHANISM

Comparing Test I with II, the main difference is the amount (or thickness) of In layer on ITO surface: in test 1, In atoms were released from the reduction of ITO surface by H_2 plasma, in small amount; in test 2, In was evaporated on ITO, in large amount (~50 nm in thickness). However, the evolution of liquid In on ITO is quite similar, which indicates that substrate heating alone cannot promote the In diffusion and coalescence on the ITO substrate.

In Test III, H_2 plasma helped forming huge In particles (larger than 10 μm) on In/ITO bilayer. As mentioned above, the huge In particles were observed only in the In/ITO region, and never on the pure ITO surface, no matter whether there was evaporated In nearby (see Figure 2.20.a) or not (see Figure 2.20.e). This strongly implies that the huge In particles were formed locally on In/ITO bilayer, mainly originating from the evaporated In. The difference in roughness of the two kinds of ITO surfaces is supposed to be caused by the different surface morphologies during H_2 plasma reduction. As liquid In NPs act as barrier against the H_2 plasma, it is logic that evaporated In/ITO bilayer has higher roughness due to the thicker In layer on ITO surface. Compared with Test II, the only difference is the extra H_2 plasma treatment, whose function is to reduce

ITO and release In atoms on ITO surface, other possibilities like modification of ITO surface energy or of In atomic surface diffusivity still remain unclear. Based on these results, we propose that interaction between in-situ released indium atoms and ex-situ evaporated indium results in the huge indium particle formation.

Considering the ex-situ evaporated In as separated pools, in-situ releasing In by H_2 plasma can be therefore viewed as: (1) digging channels among the separated pools (i.e. forming new NPs or indium wetting layer among its neighbouring evaporated NPs), (2) or expanding the original pools (i.e. the evaporated In NPs grow by the supplement of nearby released In atoms/NPs), these two events together make the neighbouring pools connected to be larger ones, which means In NPs coalescing is achieved in a **Growing-and-Connecting mode**. This process can be analogous to a chain effect.

Our proposal may explain why no redistribution of In exists on SiO_2 substrates, as no fresh In can be provided from the substrate surface to start the chain effect. Thus, it is the ITO layer that modifies the substrate chemistry in a way of supplying In. Therefore, In NPs formation on In/ITO bilayer can be considered as a particular case of In NPs formation on clean ITO surface, as before in-situ releasing In by H_2 plasma, there has been In (by evaporation) on the ITO surface.

Based on the analysis above, it is logic to explain the evolution of In NPs formation on pure ITO surface by the same **Growing-and-Coalescing mechanism**. In particular, ITO surface experiences: (1) releasing In via reducing ITO by a H_2 plasma treatment, (2) nucleating, (3) growing, and (4) coalescing to In NPs. Figure 2.22 illustrates the Growing-and-Coalescing mechanism of In NPs formation on ITO substrate, in comparison with In NPs formation on In/ITO bilayer and on SiO_2.

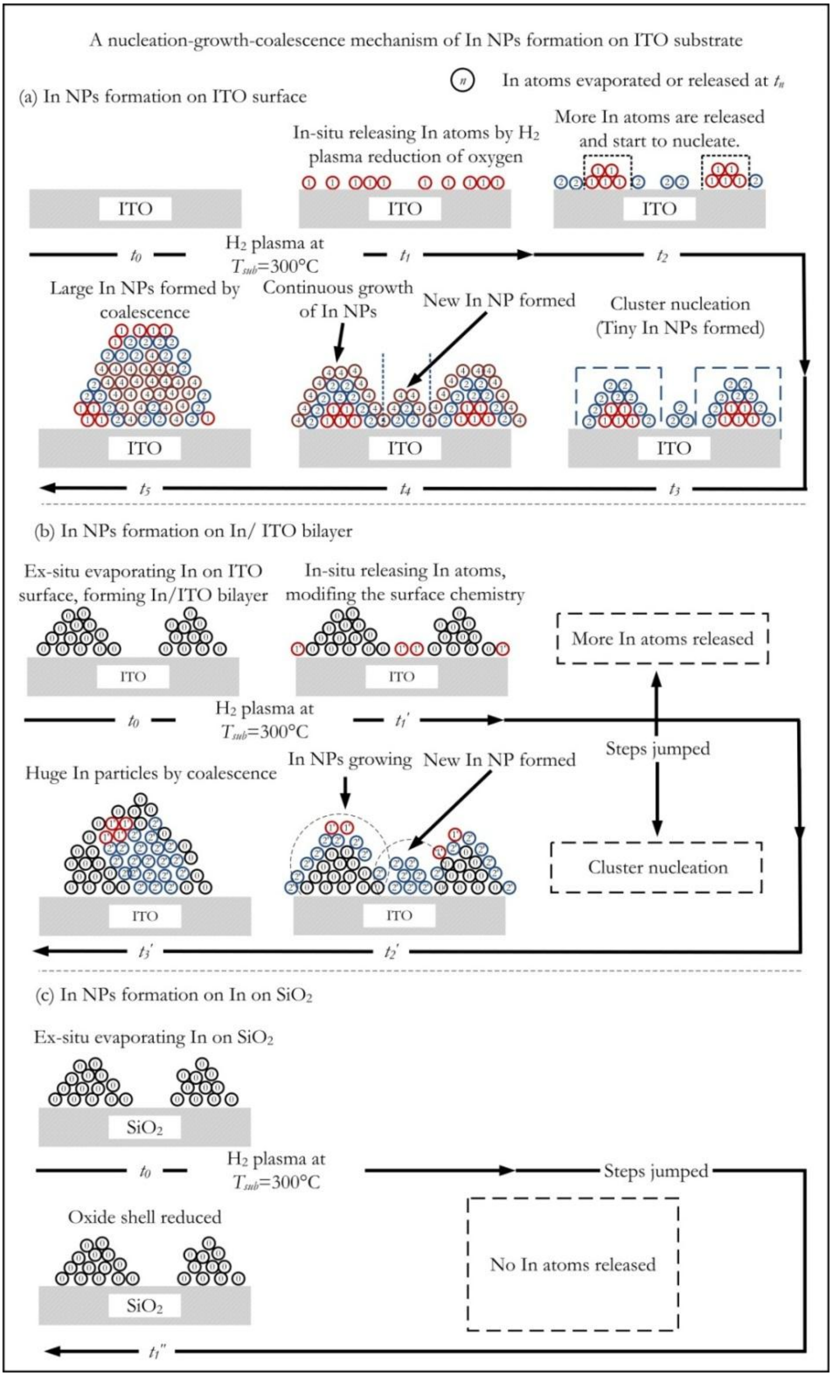

Figure 2.22 A Growing-and-Coalescing mechanism of In NPs formation on ITO substrate (a), in comparison with In NPs formation on In/ITO bilayer (b) and on SiO_2 (c).

2.4.2 REDISTRIBUTION OF INDIUM NPS ON INDIUM/ITO BILAYERS

Based on the Growing-and-Coalescing mechanism of In NPs formation on ITO, a technique for dispersing In NPs is developed on In/ITO bilayer structure. Figure 2.23 shows SEM images of a nominal 5 nm In on ITO substrate after a standard H_2 plasma treatment (100 sccm, 400 mTorr of H_2, with RF power of 5 W at T_{sub}=300°C for 5 mins). As shown in the figure, we can obtain a redistribution of In NPs. In comparison with the In NPs redistribution on micro or poly-crystalline surface based on GBW mechanism (see 2.3.4.3), this novel technique modifies the substrate chemistry by inserting a ITO layer between the substrate (SiO_2) and evaporated In thin film, and the dispersion of In NPs is achieved by in-situ releasing In on ITO which activates the growing-and-coalescing behaviour. Optimisation of NPs density and size will be carried out for further applications (e.g. radical junction SiNWs solar cell [47]).

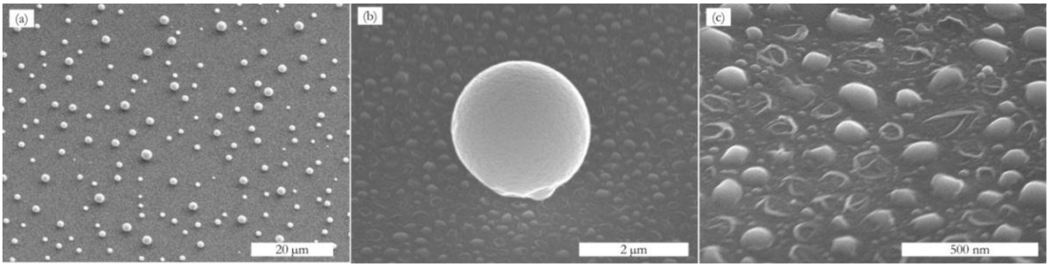

Figure 2.23 Redistribution of In NPs on In/ITO bilayer structure: (a) ~5nm In on ITO substrate after a standard H_2 plasma treatment at T_{sub}=300°C; (b) a typical In NP based on Growing-and-Coalescing mechanism; (c) typical surface of In/ITO bilayer after In NPs formation.

2.4.3 PHASE TRANSITION OF ITO THIN FILMS UPON HEATING

Besides the activation of ITO reduction by H_2 plasma exposure, annealing during or after ITO deposition also modifies the quality of ITO thin film such as surface microstructure, electrical and optical properties, and the crystallinity, etc.

ITO thin films deposited at room temperature usually grow amorphous and transform to fully crystalline thin films from 150°C to 400°C [81][82].This transition from amorphous to polycrystalline growth coincides with the observation that ITO thin films grow in 3-D island mode (VW mode) on unheated substrate and alternate to 2-D growth mode (FM mode) at about 150°C [83].

Annealing above 150°C (after deposition) also transforms amorphous ITO into polycrystalline thin films, and increasing annealing temperature improves their crystallinity [84]-[89]. Cross-sectional TEM analysis reveals the columnar microstructure of polycrystalline ITO thin films after post-annealing, and a lateral grain growth mode is proposed to describe this transformation process [84]. The structural relaxation with local ordering after post-annealing is considered to improve the conductivity of ITO thin films by increasing the carrier density [85].

The homogeneity of ITO thin films also depends on the substrate temperature during deposition or post-deposition annealing. It is reported that ITO thin films deposited on unheated substrates consist of an amorphous phase adjacent to the glass substrate with a severely stressed polycrystalline layer on top. This is in agreement with experimental studies which show that without substrate annealing ITO thin films also transform from amorphous at a lower thickness to polycrystalline at a larger thickness [91][92]. The amorphous phase was crystallized and stress free by post-annealing, while films deposited at higher temperature are homogeneously polycrystalline after deposition [90]. Besides, higher RF power (in RF magnetron sputtering) [93] and electron beam irradiation [94] can also induce the crystallization of the amorphous ITO thin films.

TEM observation is employed to investigate the substrate annealing effect on ITO thin films. ITO films with a thickness of 200 nm were deposited by RF magnetron sputtering (ITO as target with pure Ar plasma) on holey carbon TEM copper grids at room temperature. Then the samples were annealed at 300°C in H_2 atmosphere (400 mTorr, 200 sccm) for 5 mins. Figure 2.24 shows the bright field (BF) TEM images and the corresponding selective area electron diffraction (SAD) patterns of ITO thin film before and after thermal annealing. Except for several small ITO crystallites (c and d), the as-deposited ITO thin films are generally amorphous (a and b). The annealed sample was confirmed to undergo a phase transition from amorphous to polycrystalline by substrate annealing (e and f), with grain sizes up to 500 nm (g and h).

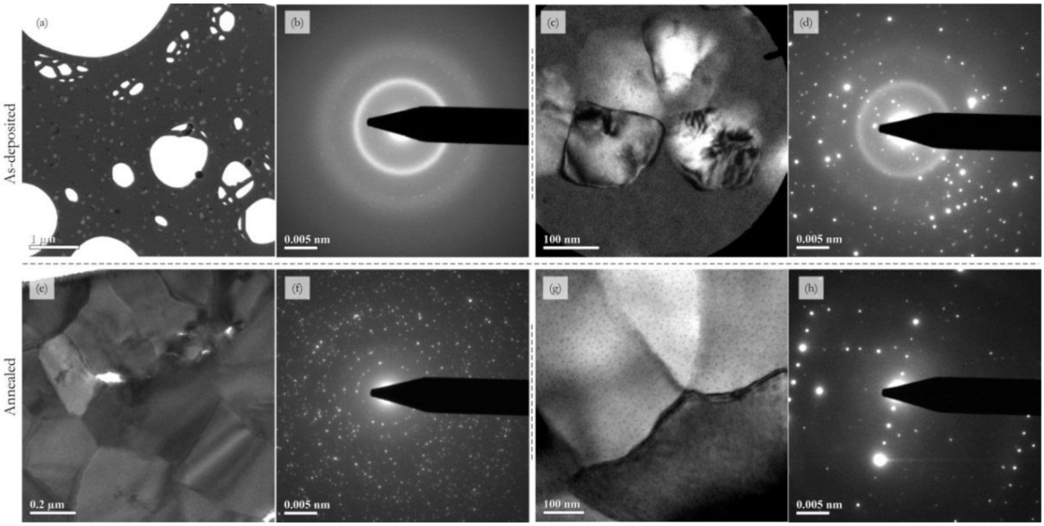

Figure 2.24 Phase transition of ITO thin film upon thermal annealing: (a, c) bright field TEM images of as-deposited ITO thin film on holey carbon TEM copper grid, and the corresponding selective area electron diffraction (SAD) patterns (b, d), respectively; (e, g) bright field TEM images of annealed ITO thin film, and the corresponding selective area electron diffraction (SAD) patterns (f, h), respectively.

For investigating the effect of the ITO phase on In NPs formation, two types of ITO thin films are prepared: 1) ITO films sputtered on *c*-Si wafer at RT with thickness of ~ 200 nm (same with the ones for TEM observation), 2) ITO films sputtered on *c*-Si wafer at 350°C with the same thickness. These samples were treated by standard H_2 plasma on a heated substrate (400 mTorr, 200 sccm H_2, 5W, T_{sub}=300°C, 5 mins) in the same batch.

Figure 2.25 (a and b) show SEM images of In NPs formed on polycrystalline ITO deposited at 350°C while (c, d) show the case of ITO deposited at RT. A low density of In NPs and narrow size distribution was obtained on polycrystalline ITO, compared with the case of amorphous ITO. Based on the Growing-and-Coalescing mechanism, possibilities for explaining the different results are proposed and discussed:

1) Polycrystalline ITO surface is more resistant against H_2 plasma reduction, thus fewer In atoms can be released. A possible explanation is that: ITO thin films deposited at high temperature are stress free so that it is less efficient for H radicals to insert and break the relaxed In-O bonds compared with the bonds in amorphous ITO with no well-defined lattice. This is supported by the study on the etching behaviour of ITO by HCl, in which amorphous ITO deposited at RT dissolved in HCL solution at an extremely high rate, however the post-annealing treatment or high temperature deposition retard the bond breaking and thus decrease the etching rate [95]. This could explain the lower density of In NPs formed on polycrystalline ITO surface.

2) Besides hindering the H_2 plasma reduction, polycrystalline ITO surface favours the homogeneity of the H_2 plasma reduction process since the stress and void free thin film surface is more homogeneous compared with amorphous ITO, therefore providing a relatively isotropic probability throughout the ITO surface for the chemisorption and reaction with H radicals, which decreases the spacing of the nucleation sites of In clusters and hence favours the coalescence of these growing In clusters into large In NPs. This assumption could explain the narrow size distribution of In NPs formed on polycrystalline ITO surface.

3) The third possibility is that polycrystalline ITO thin films with oriented surface ([222] is the most common orientation for post-annealed ITO thin films deposited at RT or the ones by high temperature deposition [85]-[89]) favours the surface diffusion of In atoms, and the following nucleation and growth of In NPs. This could explain the larger sizes of In NPs formed on polycrystalline ITO surface.

To summarize, substrate annealing transforms RT-deposited ITO from amorphous to polycrystalline, this phase transition can be achieved by 5 mins annealing at 300°C in H_2 atmosphere, which means that during the In NPs formation, the RT-deposited ITO surface undergoes a complicated process, including In-O bond breaking by H radicals from H_2 plasma, In atoms surface diffusion, In clusters nucleation, growth and coalescence; and also the phase transition. Comparing amorphous ITO thin films deposited at RT with the polycrystalline ones deposited at 350°C, low density and less broad size distribution of small In NPs can be formed on polycrystalline ITO, in which the stress free and relatively homogeneous surface microstructure could be main factors.

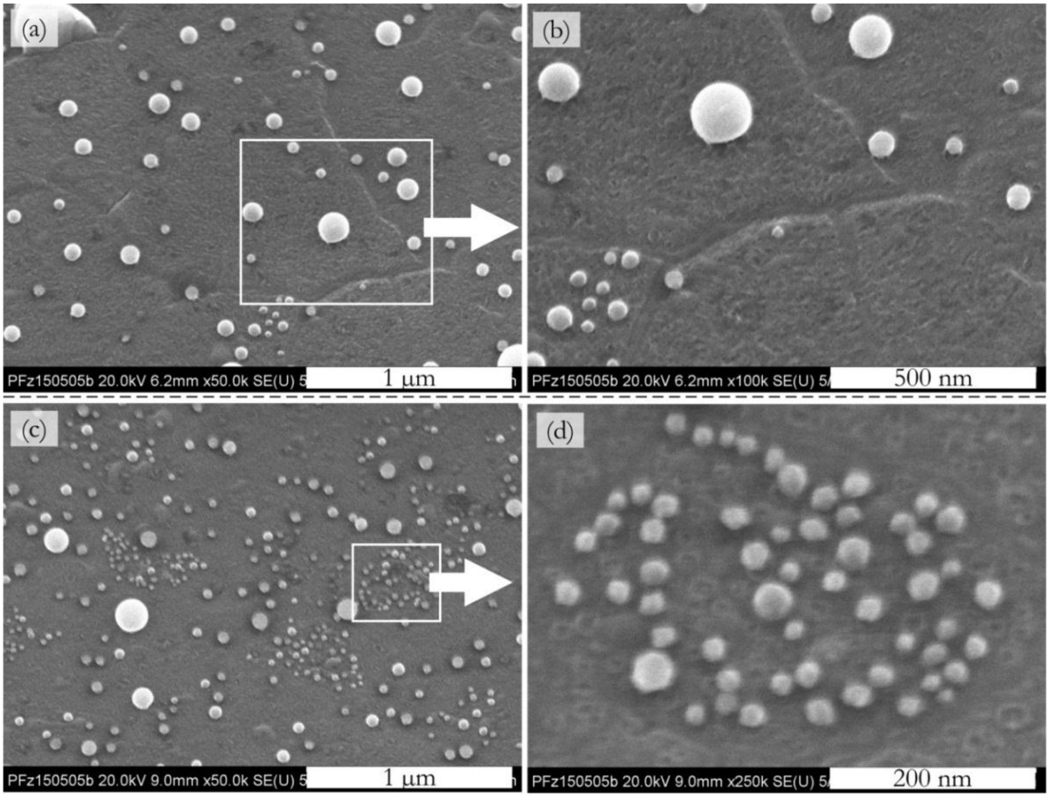

Figure 2.25 SEM images of In NPs formation on ITO deposited at 350°C (a, b) and at RT (c, d).

2.4.4 ITO REDUCTION UNDER VARIOUS H_2 PLASMA CONDITIONS

To investigate the ITO reduction efficiency by H_2 plasma, various RF powers (5 W, 20 W, 40 W), H_2 pressure (400 mTorr, 1 Torr) and exposure durations (5 mins, 10 mins) were employed. In general, RF power and H_2 pressure determine the dissociation of H_2 gas, and the degree of ion bombardment to the ITO surface, which influences the probability of In-O bond breaking. It is also expected that longer H_2 plasma exposure will release more In atoms on the ITO surface. In addition, it is necessary to note that as all the H_2 plasma exposures were carried out at 300°C, hydrogen ion bombardment and long time annealing might transform the ITO thin films from amorphous to polycrystalline, modify the surface morphology and bring about damages to the surface.

Figure 2.26 and Figure 2.27 show SEM images of In NPs formation on ITO by different sets of (RF power + exposure duration) at a substrate temperature of 300°C with 100 sccm, 400 mTorr of H_2, in magnification of x5k and x100k, respectively.

From SEM images at lower magnification in Figure 2.26, no benefit can be observed by increasing the RF power, neither the H_2 plasma duration. The density of large In NPs even decreases with increasing RF power for 5 mins exposure (a to c), and some non-spherical In islands were formed by 30 mins exposure with high RF power (e and f).

Comparing the ITO surfaces in Figure 2.27, the density of small In NPs increases with increasing RF powers (a to c), which demonstrates that increasing RF power can reinforce the ITO reduction and subsequently release more In atoms. However, after 30 mins exposure (d to f), the morphology of the ITO surface changed a lot and indicates no regularities. But it is interesting that compared with 5mins exposure, the contrast of the ITO surface in SEM images turns to be sharper, and it even starts from the case of 40 W RF power for 5 mins. This phenomenon is supposed to the phase transition of ITO from amorphous to polycrystalline during the high RF power and/or long time H_2 plasma treatment.

Another interesting observation is that higher RF power could release more small In NPs (see Figure 2.27.(a, b, c)) but resulted in a lower density of large In NPs (see Figure 2.26.(a, b, c)). This might be due to the fact that indium hydride was formed under higher RF power.

Figure 2.28 and Figure 2.29 show SEM images of In NPs formation on ITO surface by different groups of (H_2 pressure + RF power + exposure duration) at a substrate temperature of 300°C with 100 sccm of H_2, in magnification of x5k and x100k, respectively. Comparing with the case of 400 mTorr H_2 plasma, the only remarkable difference of 1 Torr H_2 plasma (see Figure 2.29 (c, d)) is that the ITO surface got rougher. Based on the nucleation-growth-coalescence mode, this phenomenon might be explained by the fact that 1 Torr H_2 plasma can release more In atoms and consequently larger In clusters are nucleated at the initial stage, these larger In clusters act as barrier between the ITO surface beneath them and H_2 plasma, finally after growth and coalescence they leave the ITO surface rougher. Moreover, Figure 2.28 shows that by 1 Torr H_2 plasma, there is no significant improvement of forming large In NPs. Perhaps the high RF powers (20 or 40 W) caused the In evaporation by local heating, making the contribution of H_2 pressure less remarkable.

To summarize, various H_2 plasma conditions were investigated for ITO reduction, the expected contribution of RF power and H_2 pressure was in agreement with the SEM observation, however no significant improvement was realized by long time, high RF power and high pressure of H_2 plasma. An explanation could be the formation of a continuous liquid In layer which protects the ITO underneath from further reduction.

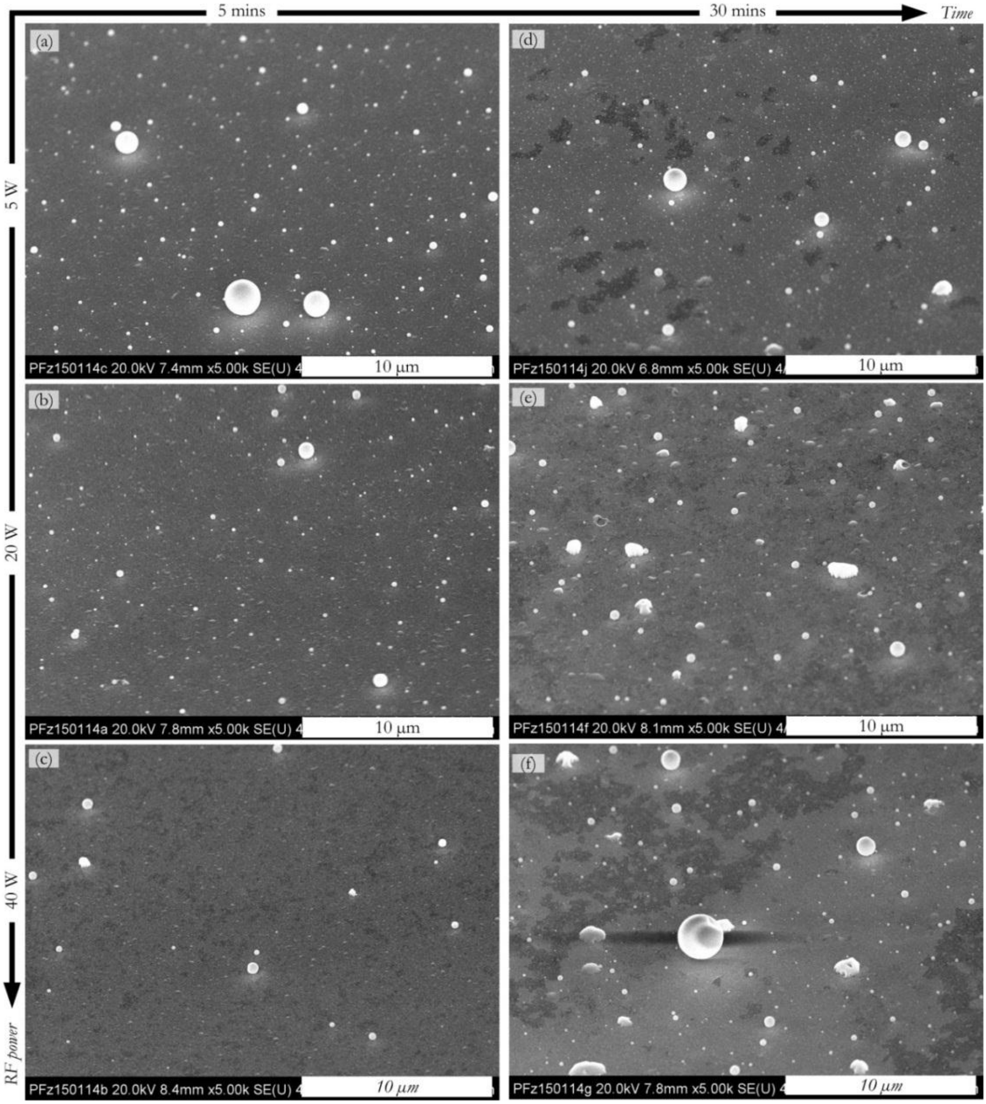

Figure 2.26 SEM images of In NPs formation on ITO substrates by different conbinations of RF power and H_2 plasma duration (with 100 sccm, 400 mTorr of H_2 at T_{sub}=300°C), at a magnification of x5k.

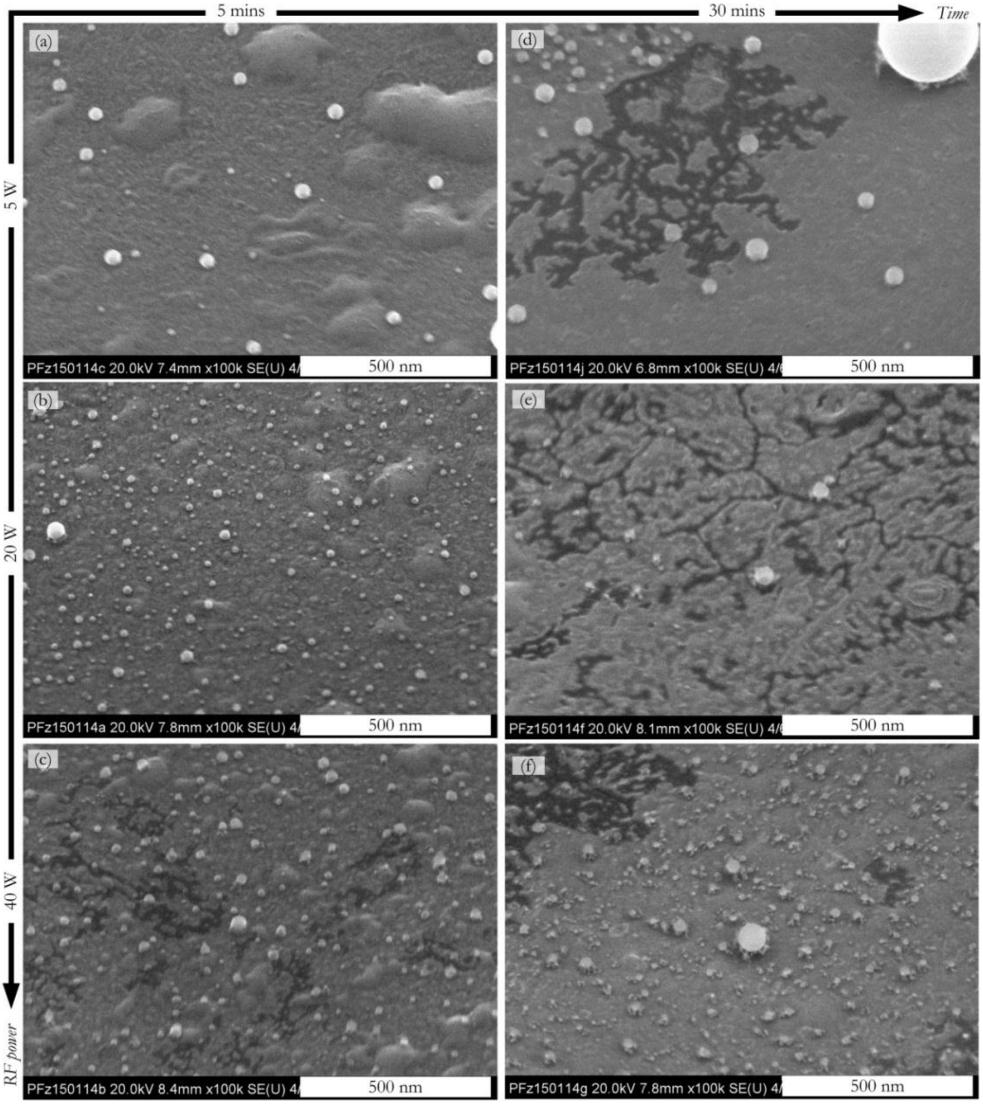

Figure 2.27 SEM images of In NPs formation on ITO substrate by by different conbinations of RF power and H_2 plasma duration (with 100 sccm, 400 mTorr of H_2 at T_{sub}=300°C), at a magnification of x100k.

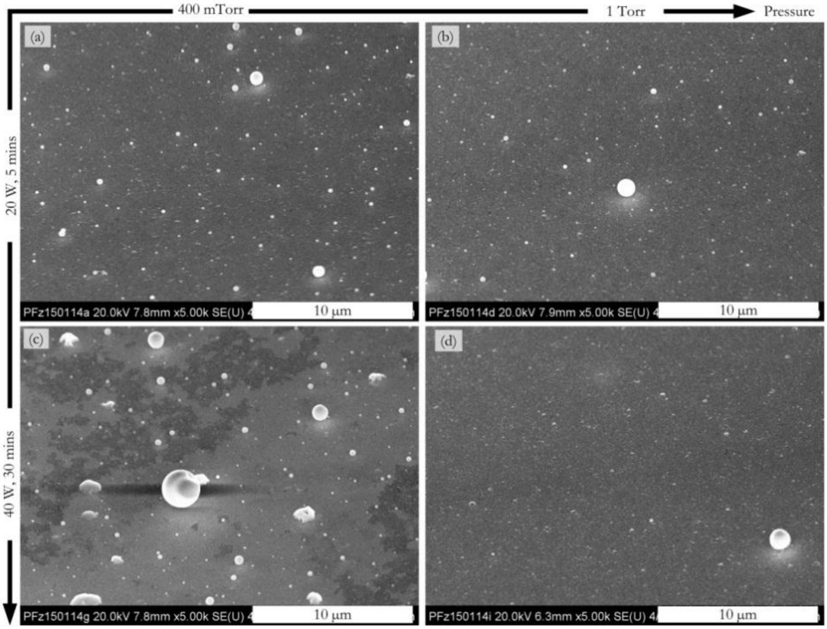

Figure 2.28 SEM images of In NPs formation on ITO surface by different conbinations of (H_2 pressure + RF power + exposure duration), in magnification of x5k.

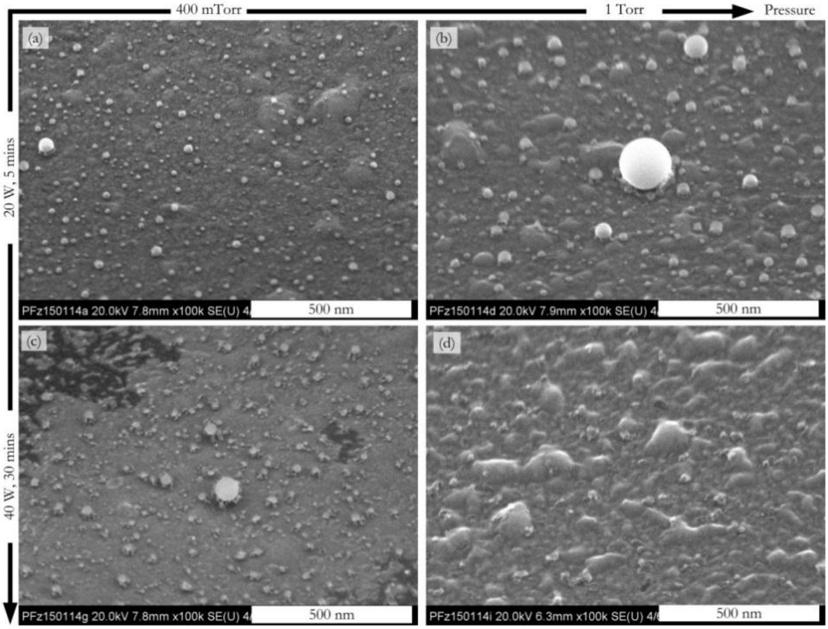

Figure 2.29 SEM images of In NPs formation on ITO surface by different conbinations of (H_2 pressure + RF power + exposure duration), in magnification of x100k.

2.4.5 CONCLUSION

When ITO surface undergoes a H_2 plasma treatment on a heated substrate, In NPs are formed. A **Growth-and-Coalescence mechanism** is proposed: H radicals break the In-O bonds and release In atoms on ITO surface, subsequently In starts to nucleate and grow on local positions, and subsequently neighbouring In clusters coalesce into In NPs in liquid phase, during which the ITO thin film transforms from amorphous to polycrystalline phase due to annealing. Substrate temperature should be above the melting point of In, however higher temperatures do not favor the In NPs formation. Based on the Growing-and-Coalescing mechanism, a technique for the In NPs redistribution is developed, the dispersion of In NPs has been achieved on In/ITO bilayer structure, with relatively less broad size distribution and moderate density.

On polycrystalline ITO surface, the density of In NPs is lower while the size distribution is narrow, as the relatively homogeneous thin film with less stress and voids provides a rather equal probability for the surface chemisorption and reaction with H radicals throughout the entire surface as compared to amorphous ITO deposited at RT.

RF power and H_2 pressure are demonstrated to affect the ITO reduction efficiency by tuning the H_2 plasma density and ions energy, however high RF power is supposed to induce In evaporation by local heating, which does not bring any benefit to In NPs formation. Long H_2 plasma treatment time on heated substrates does not favour the In NPs formation.

2.5 SUMMARY AND PERSPECTIVES

As a bottom-up catalyst for in-plane SiNWs growth, In is selected. Evaporated indium and sputtered ITO are the two types of thin films from which In NPs are obtained, thanks to their exposure to a H_2 plasma on a heated substrate (e.g. 300°C) before *a*-Si:H coating. The effects of H_2 plasma, substrate temperature and substrate properties are investigated, during which the physical and chemical process is studied.

Evaporation of In leads to discontinuous islands, H_2 plasma is used to reduce their surface oxide, assisted by substrate heating (typically above 250°C) for achieving the reducing efficiency, which enables a sufficient *a*-Si:H/In contact for NW growth. During this treatment, morphology of In experiences transformation from solid flat islands with surface oxide to liquid spherical caps with surface oxide reduced and finally solidifies to spheres, in comparison with the unchanged morphology of In treated by a simple substrate annealing process above its melting point (e.g. 300°C) or by H_2 plasma at low temperature (e.g. 150°C). This provides a method of verifying whether the indium surface oxide is sufficiently reduced or not, even though the morphology itself does not affect the following SiNWs growth. However, substrate heating at high temperatures for long duration can cause In loss. In addition, In NPs can get redistributed on micro/poly-crystalline substrates (i.e. μc-Si:H and polycrystalline AZO) based on grain boundary wetting, which is not possible on substrates with relatively isotropic surface chemistry (i.e. SiO_2). This technique provides the opportunity to disperse the In NPs for following applications; however the size and density control needs further studies.

In comparison with evaporated indium thin films, indium is generated in-situ on ITO surface. A Growth-and-Coalescence mechanism is proposed to explain the In NPs formation, where the continuous sputtered ITO surface undergoes procedures of releasing In atoms upon its reaction when exposed to a hydrogen plasma, In atoms nucleating, In crystal growing and coalescing with the neighbour ones into NPs. The size and density control is still a problem. However an approach based on the Growing-and-Coalescing mechanism is developed by using In/ITO bilayer structure. Compared with In NPs redistribution by grain boundary wetting, this approach is believed to be more feasible and advantageous in size and density control, even though further optimisation is also needed. Besides, the RT-deposited ITO thin film phase transition from amorphous to polycrystalline on heating substrates is confirmed by TEM investigation, which makes the In NPs formation on ITO surface more complicated. It plays a criminal role on the In NPs formation on ITO sidewall, which enables the In NPs positioning in large scale (see 4.2.2). Finally, due to the same reason as indium loss, long time substrate heating is not recommended, neither the high RF power which can induce local heating. Systematic understanding of the evolution of these two types of In thin films indeed brings benefits to the development of In NPs positioning technique, which is elaborated in Chapter 4.

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3 GROWTH MECHANISM OF IN-PLANE SILICON NANOWIRES

CONTENTS

Right away after the indium catalyst preparation by H_2 plasma exposure of evaporated indium or ITO thin films on heated substrates (e.g. 300°C), a thin film of *a*-Si:H is coated directly on it after cooling to low temperature (e.g. 150°C) to avoid vapour-liquid-solid growth. After *a*-Si:H deposition, the in-plane SiNW growth is activated by heating the sample, via a solid-liquid-solid mode.

The in-plane solid-liquid-solid (IPSLS) dynamic system consists of several physical and chemical processes such as In-Si interaction, Si crystallization and "spontaneous" motion of liquid In on *a*-Si:H surface. Therefore, prior to the growth mechanism discussion, several related topics are briefly reviewed, which shed light on the understanding of IPSLS growth mode. Then we discuss two cases of liquid In motion on *a*-Si:H, and a mechanism based on reactive wetting of liquid indium on *a*-Si:H is proposed to account for the experimental observations. Later, the geometric investigations of the IPSLS system support the proposed mechanism, and statistical analysis reveal a clear relationship between In NP diameter, *a*-Si:H layer thickness and SiNW diameter. In order to integrate IPSLS SiNWs into flexible electronics, a growth temperature range is studied, and is found to be dependent on the *a*-Si:H structural properties. Based on the understanding of IPSLS growth mode, we comment on other possible metal catalyst candidates and also on use of the *a*-Ge:H as an alternative precursor. Finally, we explore the consistency behind the two growth modes (IPSLS vs. VLS), by which the understanding of the growth mechanism is reinforced.

3.1 THEORETICAL BACKGROUND

As introduced in Chapter 1, the process flow for the IPSLS SiNWs growth can be described as: the liquid In NPs move on the substrates with a thin *a*-Si:H layer on top, consume Si atoms from the *a*-Si:H matrix at their advancing edge, and precipitate continuous one dimensional crystalline Si (*c*-SiNW) at their receding edge on the substrate. This complex dynamic process consists of several physical aspects, which are discussed below.

3.1.1 METAL-INDUCED CRYSTALLIZATION OF SEMICONDUCTORS

The Si phase transition from amorphous to crystalline via the contact with moving liquid In NPs can be associated to the metal-induced crystallization (MIC) of semiconductors [1]-[6], but in a particular mode of selective area crystallization. In contrast with other crystallization technologies such as solid phase crystallization (SPC) by thermal annealing (above 600°C) [8]-[12], laser annealing [13]-[19], ion beam irradiation [20]-[25], or even electrical-field enhancement [26], the crystallization of amorphous silicon or amorphous germanium can be induced below the SPC temperature when put in contact of various metals[27].

Take Si for example[6], most of the transition metals react with Si to produce compounds called metal silicides [28]-[29], such as Au, Al, Ag, Ni, Pt, Pd, Ti, Cr, etc.[5][30][31] This procedure can occur at low temperature below the lowest eutectic points in metal-Si binary phase diagrams [32]. In practice, by contacting with metal thin films, amorphous Si can get crystallized below the SPC temperatures [33]-[41]. Tu *et al.* proposed the most popular postulate that the metal-rich silicide formed at the interface facilitates the high interface mobility of metal atoms and maintains their diffusion into Si thin films, which results in the transformation of Si atoms at the interface from covalent bonding to metallic bonding induced by forming metal interstitials in Si [42]. Therefore, Si atoms get reorganised at the interface with metal-rich silicide as a transport phase. Specially, Au-Si and Al-Si compounds were detected in metastable phase by XRD [43] and electron diffraction pattern analysis [43]-[46] and were utilized to explain the formation of *pc*-Si/Al/*pc*-Si sandwich structure [47] and the layer exchange process from *a*-Si on Al to Al on pc-Si [48]-[52].

In parallel with this silicide-mediating crystallization mode, the metal-rich alloy formation at the metal/*a*-Si interface is also suggested as the mechanism for Al [53][54], Au [55] and Sn [56][57] induced crystallization, when the Si nucleation occurs due to the supersaturation (see 3.1.3) of Si atoms in the solid or liquid metallic solution. Hiraki proposed a semiconductor-metal intermixing model based on electronic screening of Coulomb interaction [58]-[69], claiming that the semiconductor covalent bond weakening or breaking occurs as the electrons in the outermost shell of the semiconductor atoms are electrostatically attracted by free electrons in the contact metals (e.g. Au or Al) due to their high electronegativities [70]-[71].

Both postulates of the metal interstitial formation in Si and the electronic screening of Coulomb interaction are based on the metal-semiconductor intermixing process. However, recently a novel mechanism of MIC was proposed in which the *a*-Si can wet and crystallize at Al grain boundaries (GBW) with no requirement of mutual diffusion between Si and solid Al [72]-[76], as Si in amorphous phase tends to diffuse along the high energy Al grain boundaries and starts to nucleate there.

Figure 3.1 summarizes the different postulates of MIC mechanism in the literature. With respect to liquid In NPs mediated SiNWs growth, the electric screening effect postulate is believed as the most suitable one as no In-Si compound exists to our knowledge and neither the existence of GBW in the *a*-Si:H/liquid In system.

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[6] Germanium has the similar interaction with metals.

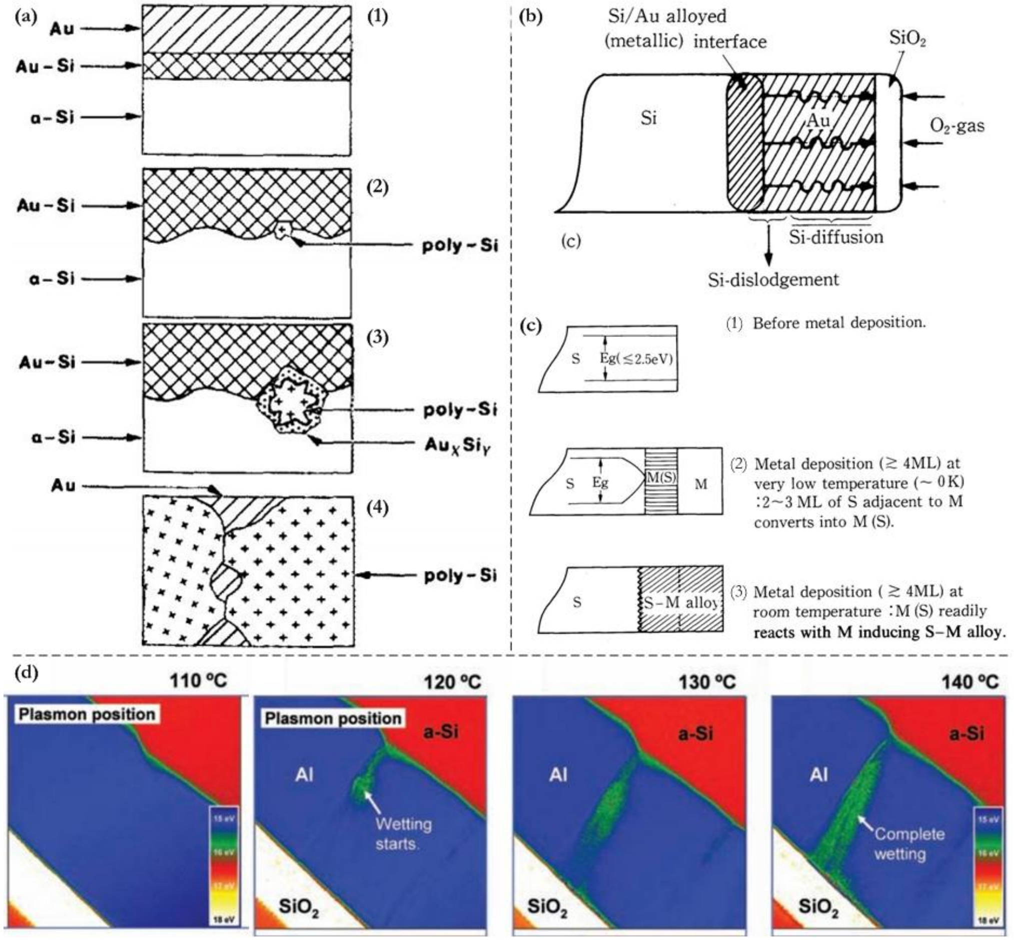


Figure 3.1 Summary of metal-induced crystallization mechanisms in the literature. (a) Metal-silicide mediated MIC mode[44], illustrating: (1) Au and Si diffuse into each other to form an intermixed region near RT; (2) nucleation of *c*-Si islands at T>130°C; (3) further annealing at T 175°C causes dendritical growth of *c*-Si by Si atoms diffusing through Au-Si compound; (4) Segregation of Au to the top and bottom surfaces of the *pc*-Si at 300°C. (b) SiO$_2$ formation at ~100°C in air on Au film in contact with Si substrate, illustrating Si atoms diffuse through a Au-Si alloy layer and deposit and oxidize on the top of the sample [58]. (c) Electric screening of Coulomb interaction mode, illustrating that after metal (M) contact, the semiconductor (S) near the M-S interface with covalent bonding is converted into metallic phase (M(S)), and M(S) readily reacts with M inducing M-S alloy at RT. This effect occurs for semiconductors with energy gap ($E_g \leq 2.5$ eV) and the thickness of metal thin film should be larger than 4 monolayers (ML) [66]. (d) Grain boundary wetting (GBW) induced MIC [75]: In-situ valence energy-filtered TEM observation of wetting of an Al GB by *a*-Si during annealing of the bilayer structure. Evolution of the mapping of the plasmon-loss peak energy at the same location of the sample upon in-situ annealing at temperatures increasing in steps of 10°C starting from 110°C with 15 minutes at each step, showing that the wetting starts at 120°C and completes at 140°C.

3.1.2 SPONTANEOUS MOTION OF LIQUID DROPLETS ON SOLID SURFACES

In a macroscopic view, the movement of liquid In NPs on an *a*-Si:H thin film is a type of spontaneous motion of droplets on solid substrates, and the SiNWs are the byproducts of the chemical reaction between liquid In and solid *a*-Si:H substrate.

In general, thermal or chemical gradients on the solid substrate surface are the driving force for the self-motion of droplets, as it generates solid surface energy gradient [77]. Figure 3.2 shows the contact angle of a liquid drop on a substrate without (a) [78] and with (b) [79] solid surface energy gradient, respectively. For a droplet standing on a homogeneous solid substrate surface, it obeys Young's equation in equilibrium:

$$\gamma_{SV} = \gamma_{LV} \cos\theta + \gamma_{SL} \tag{3-1}$$

where γ_{SV}, γ_{LV}, γ_{SL} represent the interfacial energy of solid-vapour, liquid-vapour and solid-vapour, respectively; θ represents the contact angle.

If there exists a surface energy gradient on the solid surface, this equilibrium is interrupted, and the unbalanced Young's force is given by:

$$F = (\gamma_{SV} - \gamma_{SL})_A - (\gamma_{SV} - \gamma_{SL})_B \tag{3-2}$$

where a surface energy gradient on the solid substrate is build up from A to B; θ_A *and* θ_B are the local contact angles at two sides of the liquid drop, respectively. By equations (3-1) and (3-2), the drive force can be expressed by:

$$F = \gamma_{LV}(\cos\theta_A - \cos\theta_B) \tag{3-3}$$

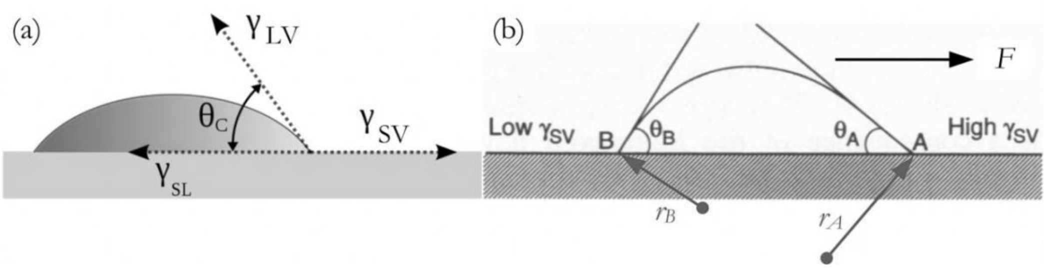


Figure 3.2 Schematic of contact angles of a liquid drop on solid substrate surface with (a) and without (b) solid surface energy gradient in Young's equation.

Note that the deformation of a liquid drop with nonuniform surface curvatures (i.e. $r_B < r_A$, as shown in Figure 3.2(b)) will cause a Laplace pressure ΔP gradient established inside it, as their relationship is determined by Young-Laplace equation [80]:

$$\Delta P = 2\gamma_{drop}/r_{curve} \tag{3-4}$$

where γ_{drop} and r_{curve} represent the local surface tension and curvature radius on liquid drop surface. So the Laplace pressure inside the liquid drop will equalize its curvature and the final dynamic contact angle between θ_A and θ_B. A diversity of techniques has been employed for establishing this driving force in the literature.

On solid substrates with thermal gradient [81]-[83], as the droplet surface tension is a function of temperature, a surface tension gradient is established within the droplet, and the droplet will advance towards the higher surface tension direction: this phenomenon is called Marangoni effect [84]. In addition, a concentration gradient within the liquid also causes surface tension gradient, for example the tear of wine effect [85]. Another interesting case is the migration of Au-rich droplets on Si (111) in a constant thermal gradient [86], however the authors described the velocity of this thermomigration by a diffusion control model, as it was mentioned that the Si concentration in Au droplets depends on temperature, therefore Si atoms diffuse along the concentration gradient direction, and the Au-rich droplet can be viewed as moving towards the reversing direction.

Another group of self-organized droplet motion is based on the chemical gradient of the solid substrate. For most cases, a gradient of wettability was built up on the substrate. According to the unbalanced Young's equation [87], the solid surface energy difference between the advancing and receding edges of the droplets is the driving force for all types of motion, the contact angles at the two edges reflect this surface energy difference.

The most popular objects for the study were pure water or organic droplets, so the wettability gradient turns to be the gradient of hydrophobicity [79], as these droplets move towards the hydrophilic region with higher solid surface energy. The techniques used to modify the solid surface chemistry are various: direct chemical treatment of the substrate surface [79][88], activating chemical reactions of substrate surfaces with solutes in droplets [89]-[96] or with external surfactants [97]-[99].

Liquid metals also experience self-moving phenomena based on chemical reactions with substrates. Liquid Au-Si alloy particles were observed migrating on Si (111) surface, leaving faceted trails behind them caused by the dissolution (or precipitation) of Si atoms into (or out of) the liquid alloy during the heating (or cooling) period [100][101]. The migration of Sn islands on Cu (111) was observed even at RT, leaving a Cu-Sn alloy (bronze) as trail, the driving force was attributed to the surface energy gradient as bronze has a lower surface energy than Cu (111) [102].

Figure 3.3 shows selected examples of spontaneous liquid motion on a solid surface in the literature.

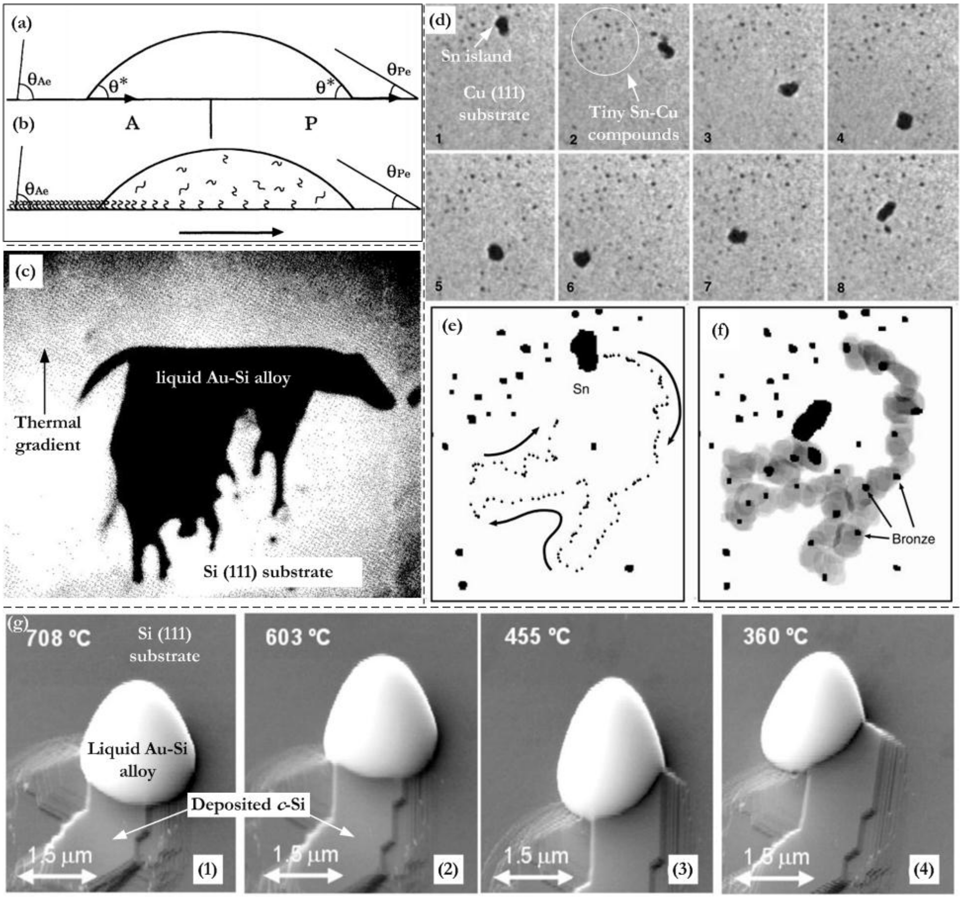


Figure 3.3 Examples of spontaneous liquid motion on a solid surface from literature. **Type I**: Free-running droplet due to in-situ surface chemistry modification [92]: (a) Schematic of a droplet deposited on the boundary between the two parts A (hydrophilic denoted as Anti-polar) and P (hydrophobic denoted as Polar) of a mixed surface. θ_{Ae} and θ_{Pe} are the equilibrium contact angles of A and P, respectively, and θ^* is the dynamical contact angle of the droplet. The arrows depict the resultant of the Young forces that occur on each contact line. (b) Schematic of a free-running droplet. The silanes in solution are grafted on the surface to give a hydrophobic surface. **Type II**: Migration of liquid Au-Si alloy on Si (111) substrate with thermal gradient [86]: (c) infrared photomicrography of an Au-Si liquid alloy migrating along a <111> plane. The direction of thermal migration is upwards in the same direction as thermal gradient. **Type III**: Alloying at surfaces by the migration of reactive islands [102]: (d) Sequence of low electron energy microscope (LEEM) images (0.6 µm width) of a Sn island running on a Cu (111) surface at 290K. The time images is 36 s. The large black object is the Sn island and the small static dark objects are the ordered bronze (Sn-Cu alloy) islands that have been ejected from the Sn island. (e) The trajectory of the centre of mass of this island. (f) Superposition of the intermediate positions of the islands, the gray level indicates how long the Sn island was over each position on the surface. **Type IV**: Migration of liquid Au-Si alloy on Si (111) substrate with no thermal gradient [100]: (g) Migration of liquid Au-Si alloy and deposition of *c*-Si during the temperature decrease from (1) to (4).

3.1.3 HETEROGENEOUS NUCLEATION FROM SOLUTION

From an atomic point of view, Si atoms diffusing into liquid In NPs and precipitating on substrates is a process of heterogeneous nucleation and crystal growth from solution on foreign substrates (i.e. Si atoms as solutes and liquid In NPs as solution). The nucleation of Si atoms occurs when the liquid In-Si alloy gets supersaturated [102]. The driving force [103]-[107] is the increase of chemical potential of Si atoms μ_s in supersaturated liquid In solution in comparison with the one at equilibrium μ_e, denoted as:

$$\Delta\mu = \mu_s - \mu_e \tag{3-5}$$

The chemical potential is expressed by

$$\mu = \mu_0 + \kappa T \ln(\varepsilon C) \tag{3-6}$$

where μ_0 is the chemical potential in standard solution, κ is the Boltzmann constant, T is the absolute temperature, ε is the activity coefficient, C is the solute concentration. Therefore, the driving force is determined by

$$\Delta\mu = \mu_s - \mu_e = \kappa T ln[(\varepsilon_s/\varepsilon_e)(C_s/C_e)] \tag{3-7}$$

where ε_s and ε_e are the activity coefficients of solute in supersaturated and equilibrium solution, with the corresponding solute concentrations C_s and C_e, respectively. Normally it is assumed that $\varepsilon_s = \varepsilon_e$, thus

$$\Delta\mu = \kappa T ln(C_s/C_e) = \kappa T ln(S) \tag{3-8}$$

where S represents the supersaturation ratio.

Due to supersaturation, a new solid phase is formed in the system, with the creation of an interfacial area between the new phase and the solution, this means the system will lose free energy during the transfer from supersaturation to equilibrium status (i.e. from high to low chemical potential); meanwhile the new phase within the solution will bring extra free energy to the system as an interface is created. Therefore, the free energy for nucleation is given by:

$$\Delta G = -N\Delta\mu + A\gamma = -\frac{V}{\Omega}\kappa T ln(S) + A\gamma \tag{3-9}$$

where the term $-N\Delta\mu$ represents the system free energy consumption due to supersaturation, and the term $A\gamma$ represents the system free energy gain contributed by the interface creation; N is the number of atoms (or molecules) forming the nucleus, Ω is the volume of an atom (or molecule) inside the crystal, A and V are the surface area and volume of the nucleus, respectively, and γ is the interfacial energy between nucleus and solution. Let

$$\Delta G_{dV} = -\kappa T ln^{S}/\Omega = -\Delta\mu/\Omega \tag{3-10}$$

be the free energy change of a unite volume, thus equation (3-9) can be written by

$$\Delta G = V\Delta G_{dV} + A\gamma = \Delta G_V + \Delta G_A \tag{3-11}$$

where $A\gamma$ is denoted as ΔG_A as the surface term, and $V\Delta G_{dV} = \Delta G_V$ be the volume term.

Consider a spherical nucleus of radius r in a solution, as shown in Figure 3.4.b, the equation (3-11) turns to be

$$\Delta G_{homo} = (4\pi r^3/3)\Delta G_{dV} + 4\pi r^2\gamma \tag{3-12}$$

And ΔG as a function of r is shown in Figure 3.4.a due to the competition between surface term and volume term. Let

$$d\Delta G_{homo}/dr = 0 \tag{3-13}$$

thus, ΔG_{homo} reaches a maximum at a critical radius r^*

$$r^* = -2\gamma/\Delta G_{dV} \tag{3-14}$$

where the critical free energy of homogeneous nucleation (i.e. free energy barrier) is

$$\Delta G^*_{homo} = (16\pi/3)(\gamma^3/\Delta G_{dV}{}^2) \tag{3-15}$$

For the case of heterogeneous nucleation, the foreign substrates (or walls, impurities, etc.) catalyse the nucleation as they offer extra interfacial free energy and thus lower the free energy barrier [108]. For example, a foreign substrate is added in the system, on which a spherical cap shaped nucleus with a radius of curvature r_c and contact angle θ is formed, as shown in Figure 3.4.c. Equation (3-11) should be modified as

$$\Delta G_{heter} = V_c\Delta G_{dV} + A_{12}\gamma_{12} + A_{23}(\gamma_{23} - \gamma_{13}) \tag{3-16}$$

where V_c is the volume of cap shaped nucleus, A_{12}, A_{23} are the interfacial area of solution-nucleus and substrate-nucleus, respectively; and γ_{12}, γ_{23}, γ_{13} are the interfacial energy of solution-nucleus, substrate-nucleus and the solution-substrate, respectively, as shown in Figure 3.4.c. This means that besides the contribution of nucleus-solution interfacial energy $A_{12}\gamma_{12}$, the foreign substrate also provides extra interfacial energy $A_{23}\gamma_{23}$ during the nucleation, which however causes the substrate-solution interfacial energy loss $-A_{23}\gamma_{13}$.

The volume V_c can be expressed by

$$V_c = \int_0^\theta (\pi r_c{}^2 \sin^2\varepsilon)(r_c\, d\varepsilon \sin\varepsilon) = \frac{\pi r_c{}^3}{3}[2 - 3\cos\theta + \cos^3\theta] \tag{3-17}$$

The solution-nucleus interfacial area A_{12} is given by

$$A_{12} = \int_0^\theta (2\pi r_c \sin\varepsilon)(r_c\, d\varepsilon) = 2\pi r_c{}^2(1 - \cos\theta) \tag{3-18}$$

The relationship of γ_{12}, γ_{23}, γ_{13} is determined by Young's equation in equilibrium:

$$\gamma_{13} = \gamma_{13}\cos\theta + \gamma_{23} \tag{3-19}$$

By combining equations (3-17), (3-18) and (3-19) into (3-16), the free energy change for heterogeneous nucleation is expressed by

$$\Delta G_{heter} = \left[\frac{4\pi {r_c}^3}{3}\Delta G_{dV} + 4\pi {r_c}^2\gamma_{12}\right] \cdot \left[\frac{2-3\cos\theta+\cos^3\theta}{4}\right] \tag{3-20}$$

Compared with equation (3-12), it means that for a constant volume V of nucleus, the free energy change provided by heterogeneous nucleation is determined by its homogeneous counterpart and the nucleus-substrate contact angle:

$$\Delta G_{heter} = \Delta G_{homo} \cdot \left[\frac{2-3\cos\theta+\cos^3\theta}{4}\right] = \varphi(\theta)\Delta G_{homo} \tag{3-21}$$

where $0 \leq \varphi(\theta) \leq 1$ represents the evolution of interfacial energy as a function of the contact angle θ. Hence, the nucleation free energy barrier also follows this relationship:

$$\Delta G^*_{heter} = \varphi(\theta)\Delta G^*_{homo} \tag{3-22}$$

which indicates the nucleation free energy barrier on a foreign substrate is lower, in comparison with the one in the solution.

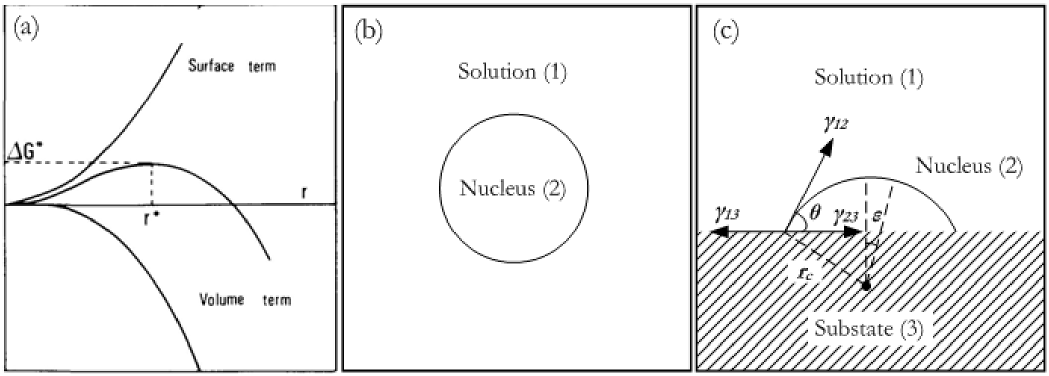


Figure 3.4 Nucleation from solution: (a) Variation of activation free energy ΔG for homogeneous nucleation from solution [107]; (b) illustration of a spherical nucleus homogeneously nucleated from solution (c) illustration of heterogeneous nucleation of a special cap shaped nucleus of radius of r_c on a solid substrate with contact angle θ.

3.1.4 BACKGROUND ON THE IN-PLANE SINWS GROWTH

Since the first report on SiNWs via in-plane solid-liquid-solid growth mode [110], endeavours are being made on understanding the growth dynamics [111][112] and controlling the morphology [113]. In general, the growth process is considered to be driven by a Gibbs energy difference between *a*-Si:H and crystalline SiNWs (see 3.4.2.). The liquid In NPs absorb Si atoms from *a*-Si:H in solid phase, and deposit them in crystalline phase in 1D morphology. Figure 3.5 illustrates the growth mechanism proposed by Yu and Roca i Cabarrocas [112]. As mentioned in their publications, the detailed mechanism and nature of driving force is still an open field for further exploration.

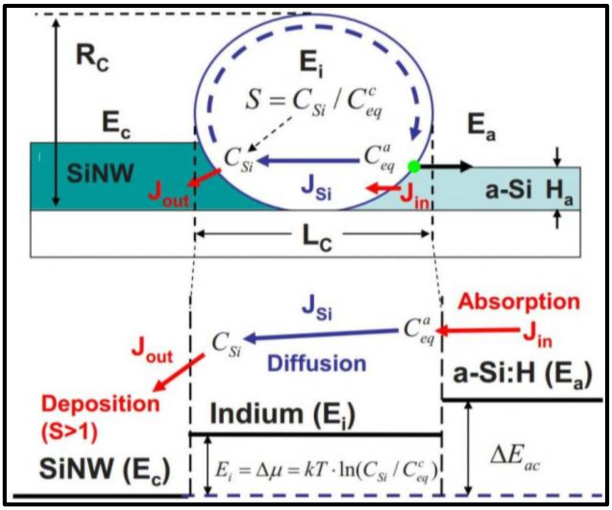


Figure 3.5 Growth mechanism proposed by Yu and Roca i Cabarrocas [112]: schematic illustration for the absorption, diffusion, and deposition steps involved in the growth of lateral SiNW via IPSLS mode. E_a, E_c, and E_i denote the Gibbs energy of Si atoms in the amorphous, crystalline and dissolved (in liquid In) states, respectively; C_{si} is the dissolved Si atom concentration in the catalyst drop; J_{in}, J_{out} and J_{Si} are the absorption, deposition, and mass transport (diffusion) flux rate of Si atoms.

According to the review above, it can be postulated that two conbined processes enable the continuous growth of IPSLS SiNWs: 1) the motion of liquid In NPs on substrates with *a*-Si:H coating layer; 2) the continuous growth of SiNWs at the receding edge of moving In NPs in contact with *a*-Si:H at the advancing edge. Process 2 transforms Si from amorphous to crystalline phase, thereby results in the substrate chemistry modification and maintains the chemical gradient (from *c*-Si to *a*-Si:H) which is the driving force for process 1; reversely, the Si-In alloying during process 1 causes the ongoing supersaturation in the moving liquid In NPs and therefore sustains process 2.

In order to verify this postulate, several unique phenomena in this solid-liquid-solid system are discussed.

3.2 SPONTANEOUS MOTION OF LIQUID INDIUM ON *a*-SI:H

In Chapter 2, we concluded that liquid In NPs do not move on *c*-Si substrates with native oxide at temperature above the melting point of In (e.g. 300°C), which is consistent with the theory of motion of droplets [77] because there is no thermal gradient or chemical gradient on the substrates. However, in the following examples we demonstrate that modifying the substrate chemistry by coating it with a thin *a*-Si:H layer provides a novel strategy that efficiently achieves the spreading, coalescence and motion of liquid In on the corresponding non-reactive substrates (i.e. SiO_2).

3.2.1 EVOLUTION OF IN NANOPARTICLES AT THE INITIAL STAGE OF SINWS GROWTH

As shown in chapter 2, the 3D islands of evaporated indium do not experience a significant evolution on their density and size after the treatment by a H_2 plasma at a substrate temperature around 300°C (above their melting point). However, during the initial stage of SiNWs growth, the redistribution of In NPs occurs due to their interaction with the *a*-Si:H film covering the substrate and thus modifying its surface energy.

3.2.1.1 REDISTRIBUTION OF IN NPS UPON THEIR INTERACTION WITH *a*-SI:H

We have found that, an evaporated In thin film (patterned by optical lithography, as illustrated in the inset image in Figure 3.6.f), after a standard H_2 plasma exposure, is composed of In NPs with diameters of ~30 nm (as shown in Figure 3.6.a and b), after ~10 nm *a*-Si:H thin layer coating and annealing at 400°C for 1 min, the resulting In NPs which lead to SiNWs growth out of the patterned In region are much larger (as shown in Figure 3.6.e and f), in comparison with the ones shown in Figure 3.6.a and b. Removing the amorphous and crystalline Si materials by H_2 plasma etching (100 sccm, 400 mTorr, 20 W, T_{sub}=150°C, 10mins), reveals the coalescence of In NPs inside the In pad region (as shown in Figure 3.6.c, compared with a) with the residues left by small In NPs before coalescence (as shown in Figure 3.6.d, compared with b), and also the remarkable displacement of In NPs out of the In pad region (as shown in Figure 3.6.f). The trail of SiNW in Figure 3.6.f is probably the residual *c*-Si due to the insufficient H_2 plasma etching. These results clearly show that the interaction of In with *a*-Si:H results in the strong change of density and size of the NPs during the initial stage of SiNWs growth.

Another test on an In thin film of nominal thickness ~50 nm (as shown in Figure 3.7.a and b) reinforces this NPs redistriubution phenomenon, applying the same procedure of H_2 plasma treatment, *a*-Si:H coating and annealing, the coalescing behaviour was revealed by SF_6 plasma etching (25sccm, 10mTorr, RF power of 30W, 2mins) of Si materials, as shown in Figure 3.7.c and d.

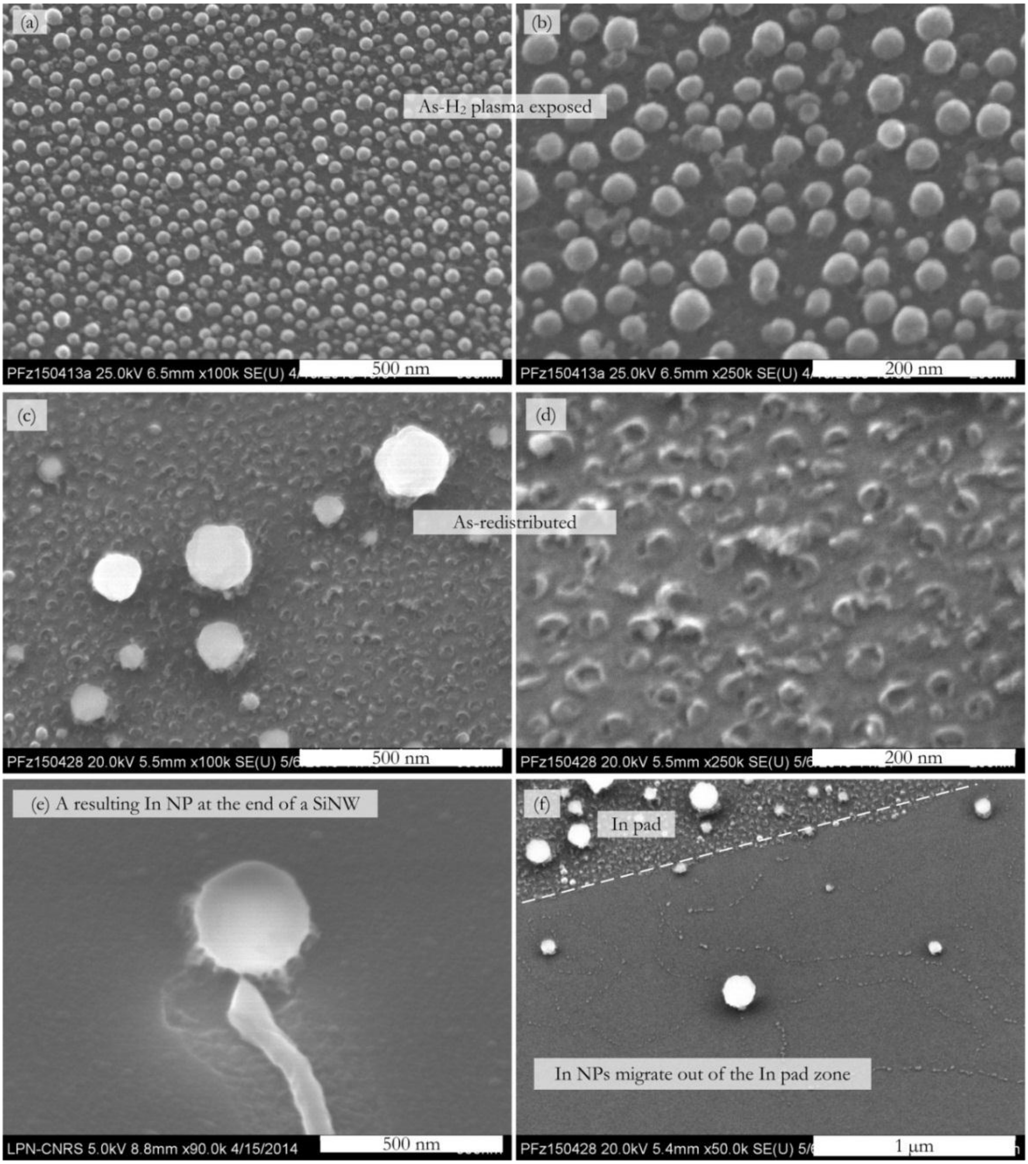


Figure 3.6 SEM images demonstrating the redistribution of In NPs as a result of the In interaction with *a*-Si:H: (a, b) evaporated In film of nominal thickness 5 nm after H_2 plasma at 300°C for 5 mins; (c, d) redistribution of In NPs after *a*-Si:H coating and annealing, revealed by H_2 plasma etching; (e) a resulting In NP leading the growth of a SiNW (~10 nm *a*-Si:H coating and annealing at 400°C for 1 min); (f) migration of In NPs out of the In pad zone, the *a*-Si:H and *c*-SiNWs were etched by H_2 plasma; (c) a final In NP leading the growth of a SiNW (~10 nm *a*-Si:H coating and annealing at 400°C for 1 min); (d) migration of In NPs outwards the In pad zone, the accompanied SiNWs were etched by H_2 plasma; (e, f) redistribution of In NPs after *a*-Si:H coating and annealing, revealed by H_2 plasma etching.

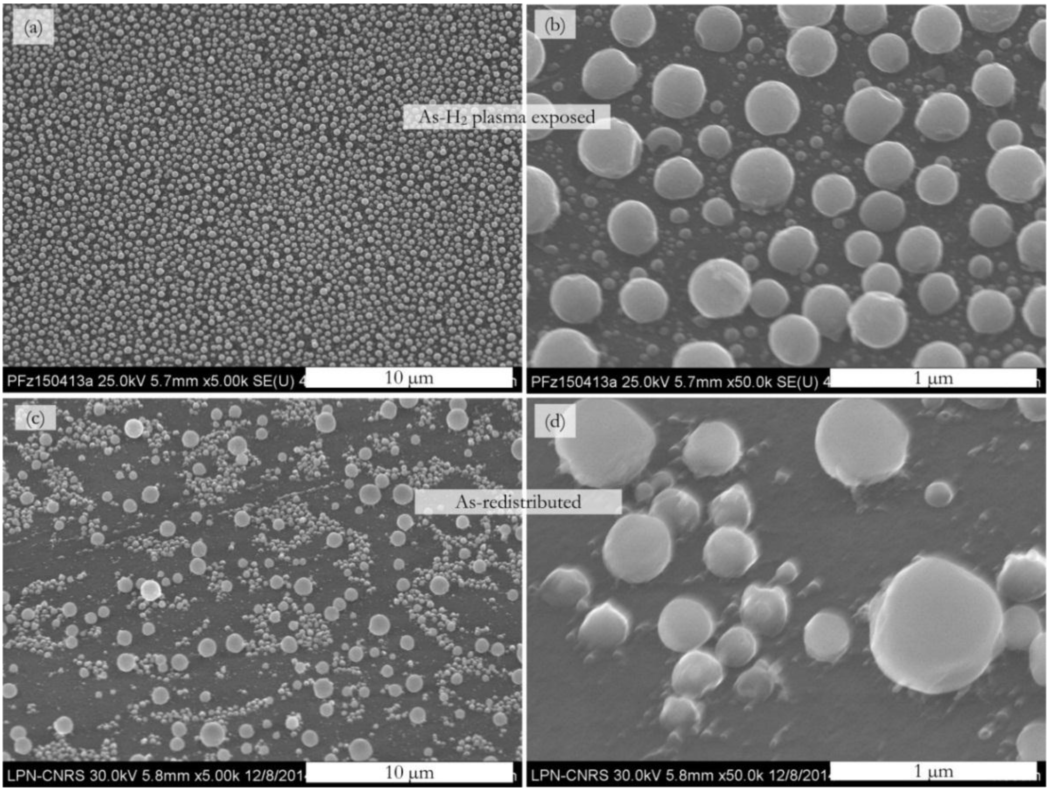


Figure 3.7 Redistribution of In NPs: (a, b) SEM images of as-evaporated In NPs of a nominal thickness of 50 nm on *c*-Si substrate with native oxide, after a standard H_2 plasma exposure; (c, d) redistribution of In NPs, after the same treatment of *a*-Si:H coating, annealing and SF_6 plasma etching of *a*-Si:H and *c*-SiNWs.

As discussed in Chapter 2, evaporation of In on ITO can form large particles (with diameters above 10 μm) based on a growth-and-coalescence mode (see 2.4.1.3), due to in-situ release of In from ITO surface by H_2 plasma reduction. Here, for In on a *c*-Si wafer with native oxide coated by an *a*-Si:H layer, a reactive spreading [77][87][114] -and-coalescing mode is proposed to illustrate the evolution of In NPs, as illustrated in Figure 3.8.

The dewetting behaviour of liquid In NPs on a SiO_2 substrate with no interface reaction has been observed under in-situ SEM [115], while the cross-sectional TEM analysis shows their profiles as semi-spheres with a contact angle of ~90° [116]. As illustrated in Figure 3.8.a, the In NPs in solid phase are perfectly spherical (see 2.3.3), the phase transition from solid to liquid by substrate annealing above the In melting point will cause a change of contact angle and contact area. Inevitably, in the initial stage, the liquid semi-spherical In NPs will overlap with the surrounding *a*-Si:H (as illustrated in Figure 3.8.b). It should be noted that as the profile of *a*-Si:H coating layer cannot be perfectly conformal, the sidewall deposition rate is lower than the one on flat surface (as shown in Figure 3.8.e). Therefore, there are regions with thinner *a*-Si:H coating under the shadow of solid spherical In NPs (as illustrated in Figure 3.8.d). As a consequence, a chemically inhomogeneous solid-liquid interface is generated (as illustrated in Figure 3.8.f) and reactive spreading can be activated [88]. Furthermore, chemical processes differ along the solid-liquid interface: In-Si intermixing occurs at the In-*a*-Si:H interface near the solid-liquid contact line, while no reaction is expected at the In-SiO_2 interface, in the centre of the solid-liquid contact region. This means that *a*-Si:H with a high surface energy is **indium-philic**, in comparison with the **indium-phobic** SiO_2 surface. Table 3.1 lists some surface energy values of well-relaxed *a*-Si, Si (111) surface, SiO_2 and Si_3N_4 in the literature. Thus, the surface energy of *a*-Si is more than one order of magnitude higher than that of dielectrics like SiO_2 and Si_3N_4. Besides, considering that: (i) structural relaxation [117][118] lowers the Gibbs energy of *a*-Si by repairing the defects [119], (ii) structural relaxation is the preliminary step prior to rapid crystallization [120], (iii) no hydrogen-induced disorder exits in pure *a*-Si [121], then one can expect a well-relaxed *a*-Si to have a similar surface energy as Si (111) surface. However, we expect that our PECVD-deposited *a*-Si:H to have a higher surface energy than the calculated one for well-relaxed pure *a*-Si as well as *c*-Si.

Moreover, supersaturation of Si atoms in liquid indium will result in precipiration of *c*-Si (as illustrated in Figure 3.8.c). This chemical reaction at the liquid-solid interface can also contribute to the reactive spreading process. On the one hand, as liquid In shows a similar non-reactive dewetting behaviour on *c*-Si [116] with the one on SiO_2, in contrast with the reactive spreading behaviour of liquid In on *a*-Si:H, it is thereby reinforced that the reduction of substrate surface energy is realized by this phase transition from amorphous to crystalline [112]. On the other hand, it is also reported that the negative Gibbs energy of chemical reaction (i.e. MIC process of In-Si intermixing and Si nucleation) can contribute to the reduction of solid-liquid interfacial energy [122][123]. So no matter which one the dominating factor is, the chemical reaction at the solid-liquid interface lowers the substrate surface energy [89]-[95], maintains the wettability gradient and the following reactive spreading-and-coalescing process can proceed.

Based on the analysis above, it is also logic to explain why a very limited number of In NPs grown by coalescence prefer to move away from the In pad zone (see Figure 3.6.f) while most In NPs in the centre of the zone stop moving. We suggest that *a*-Si:H is exhausted by indiuml-induced crystallization inside the zone, thereafter the solid-liquid interface turns to be relatively chemically homogeneous (i.e. interfaces of SiO_2/In and *c*-Si/In, in comparison with *a*-Si:H/In) and the wettability gradient is weakened.

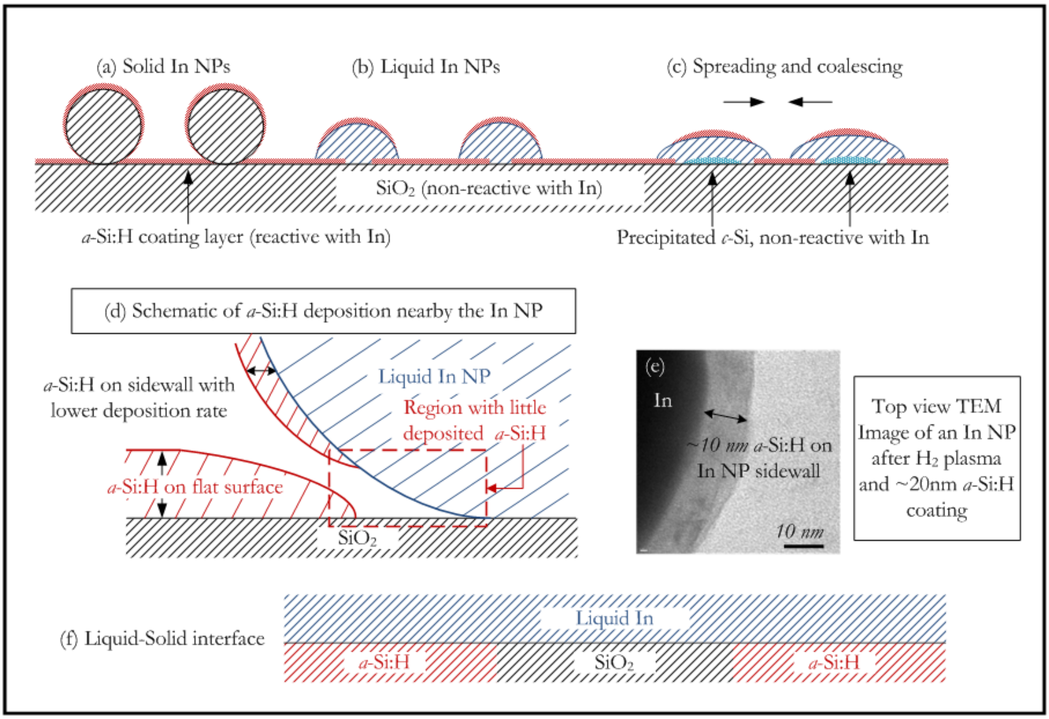


Figure 3.8 Illustration of the evolution of In NPs based on a reactive spreading-and-coalescing mode.

Table 3.1 Selected surface energy values of different materials in the literature.

Materials	Surface energy (J/m^2)	Note	Reference
Well-relaxed *a*-Si	1.05	Calculated by CMD	[124]
Well-relaxed *a*-Si	1.13	Calculated by CMD-DFT[125]	[124]
c-Si (111)	1.23	Measured	[126]
SiO_2	0.05	Measured	[127]
SiO_2	0.05	Thermally grown, measured	[128]
SiO_2	0.04	PECVD, measured	[128]
SiO_2	0.03	Measured	[129]
Si_3N_4	0.04	Measured	[129]

3.2.1.2 EFFECT OF *a*-SI:H SHELL ON THE COALESCENCE OF INDIUM NANOPARTICLES

Another test was carried out on small square indium pads (with side lengths smaller than 1 µm) defined by electron-beam lithography on a *c*-Si wafer with native oxide. These In pads were treated by a standard process for SiNWs growth. Figure 3.9 (a to f) show several In pads with SiNWs grown, compared with the failed cases presented in Figure 3.9 (g to j). For the failed cases, the In NPs seem to be restricted by the covering shells, while it is found that, without exception, most of the shells along the trajectories of the grown SiNWs were broken. The process is probably that the In NPs leading the growth of SiNWs pass by the In NPs fixed on the substrate with shells, dissolve the shells and allow the In inside the shells to flow out and coalesce with the moving one, as illustrated in Figure 3.9.l. Therefore, the material of the shells should be *a*-Si:H, as the interaction between In and *c*-Si can be neglected. This "blooming" phenomenon implies that the *a*-Si:H coating layer on In NPs can impede the coalescence and redistribution process, which is also demonstrated by comparing the distribution of In NPs before and after *a*-Si:H coating and annealing (as shown in Figure 3.9.j and k). Based on the SiNWs synthesis process, till now it is still inevitable to circumvent this covering shell, the only way of weakening this effect is to coat *a*-Si:H film as thin as possible.

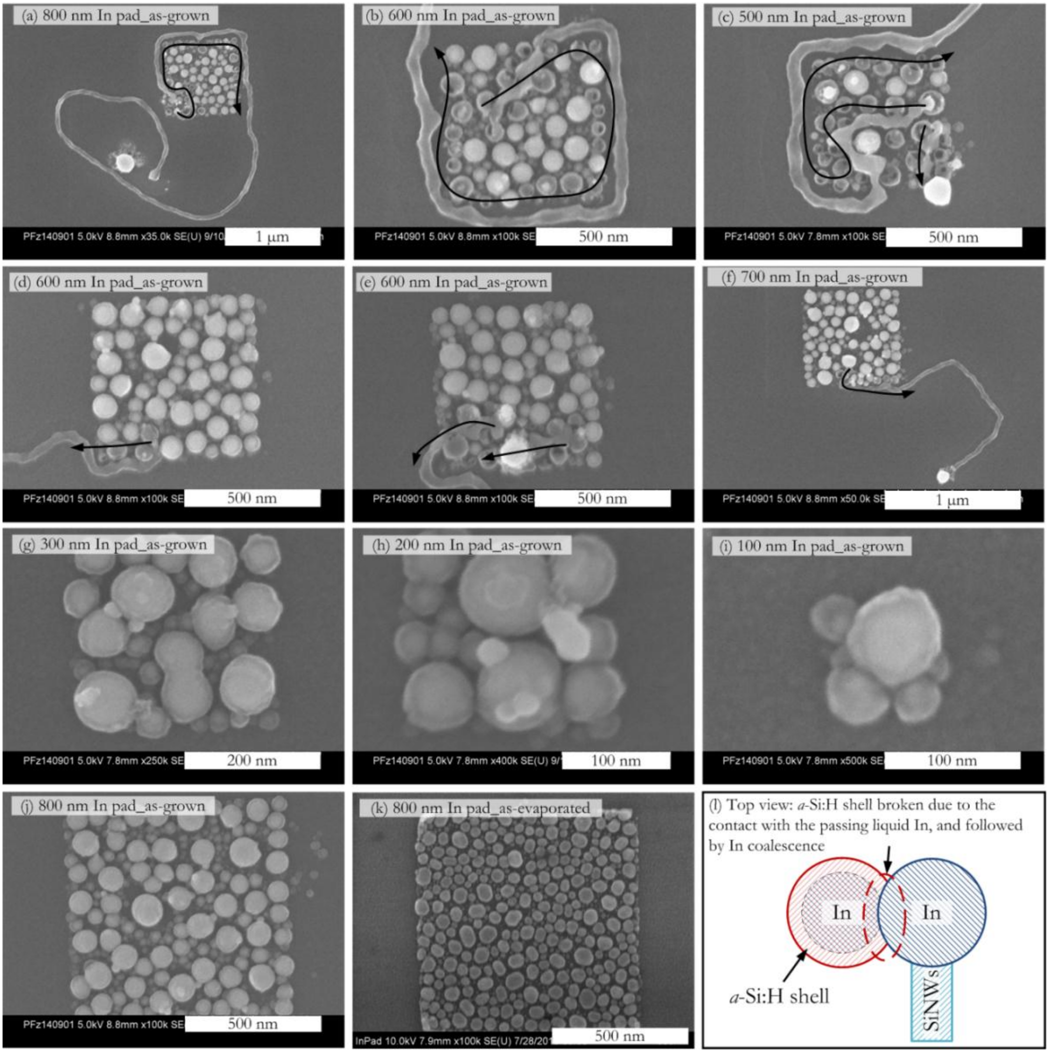


Figure 3.9 Effect of the *a*-SiH shell on the coalescence of indium NPs: (a-f) SEM images of In pads (in different sizes) with SiNWs grown; (g-j) SEM images of In square pads (in different sizes) without SiNWs grown; (k) SEM image of as-evaporated In pad in side of 800 nm; (l) schematic representation of the “Blooming” phenomenon due to the *a*-Si:H shell breaking and liquid In coalescing process.

3.2.1.3 INVESTIGATION OF *μc*-SI:H/IN INTERACTION

In order to fully verify the different interface chemistry between *a*-Si:H/In and *c*-Si/In, *μc*-Si:H was selected as it contains *c*-Si gains and *a*-Si:H along the grain boundaries. In this study, an In film of nominal thickness of ~50 nm evaporated on SiO_2, treated by a standard H_2 plasma exposure, was coated by a *μc*-Si:H thin film (see 2.3.4.1), instead of coating by *a*-Si:H. After a standard annealing at 400°C, no coalescence of In NPs or SiNWs growth was observed. Comparing the In NPs before and after *μc*-Si coating and annealing (as shown in Figure 3.10.a, c, respectively), it shows no significant redistribution of In NPs, indicating that no remarkable chemical reaction took place at the *μc*-Si:H/In interface. Figure 3.10.d shows that the *μc*-Si:H coating layer on the In NP is asymmetric: this is probably due to the slight vibration during phase transition from liquid to solid by cooling the substrate. Furthermore, as *c*-Si dominates the *μc*-Si:H thin film (see Figure 2.11), it implies that *c*-Si-In interaction can be neglected in the SLS system.

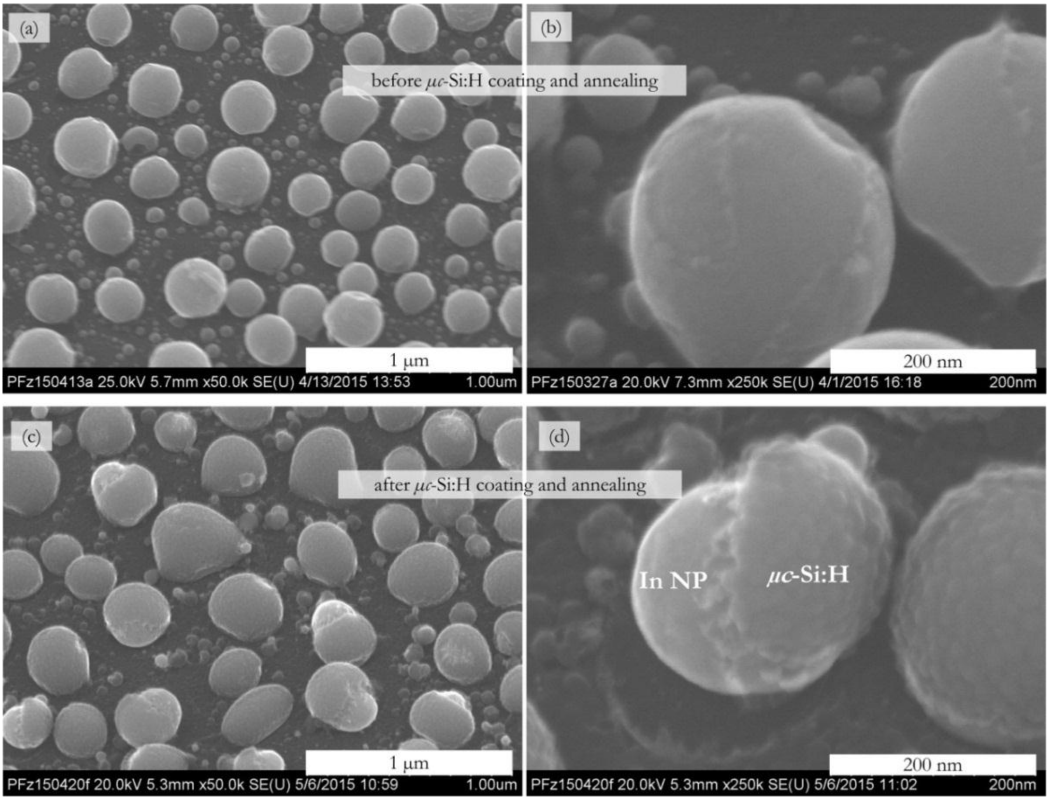


Figure 3.10 Investigation of *μc*-Si:H coating on In NPs: (a, b) SEM images of as-H_2 plasma exposed In NP; (c, d) SEM images of In NPs after ~30 nm μc-Si:H coating and then annealing at 400°C.

3.2.2 LARGE INDIUM DROPLETS MOVING ON *a*-SI:H

Reactive spreading due to substrate wettability gradient results in the redistribution of In NPs, as discussed in 3.2.1. Putting aside the growth of SiNWs, it is supposed that this reactive spreading behaviour is also the driving force for the motion of liquid In on *a*-Si:H. In this experiment, large In droplets with diameters of ~10 μm were formed on In/ITO bilayer structure (see 2.4.1.2 Test III). After a standard ~20 nm *a*-Si:H coating and substrate annealing, the liquid In moved on the substrate (as shown in Figure 3.11.a), leaving a trail with dispersed Si crystals on the substrate (as shown in Figure 3.11.b, c). Figure 3.11.d illustrates the driving force for this motion, which is also the wettability gradient on the surface. Liquid In transforms the *a*-Si:H beneath it to *c*-Si, therefore lowering the surface energy, meanwhile no chemical reaction occurs at the In-ITO interface (see 2.4.1.2 Test II), hence liquid In can only reactively spread towards the *a*-Si:H surface, and the ongoing supersaturation in In-Si alloy and the sequential precipitation of *c*-Si on the ITO substrate enable the continuity of this driving force.

If the size of a liquid droplet exceeds its capillary length κ^{-1}, the gravitational effect should be considered; the droplet cannot maintain an isotropic curvature, and its shape transforms from a spherical cap to a "pancake" [77]. The capillary length can be calculated by the set of equations below:

$$\begin{cases} \gamma_{In} = 0.568 - 9.45 \times 10^{-5} T \ (N \cdot m^{-1}) \\ \rho_{In} = 7.05 \times 10^{3} - 0.776 T \ (kg \cdot m^{-3}) \\ \kappa^{-1} = \sqrt{\gamma/\rho g} \end{cases} \tag{3-23}$$

where γ_{In} is the surface tension of liquid In, ϱ_{In} is the density of liquid In and κ^{-1} is the capillary length of the liquid In, *g* is the gravitational acceleration, *T* is the temperature in Celsius scale [77][130]. Substituting T=450°C, g=9.8 $m \cdot s^{-2}$, the capillary length $\kappa^{-1}_{(In,\ 450°C)}$ is calculated to be ~3 μm. Therefore the profile of the large In particle (diameter ~10 μm) should be like a pancake in the liquid phase, as illustrated in Figure 3.11.d.

This enlightens that the requirement for maintaining the liquid In motion on *a*-Si:H is just the Si phase transition from amorphous to crystalline (i.e. *c*-Si precipitation from supersaturated liquid In-Si alloy), which lowers the substrate surface energy. Note that in this experiment the substrate is ITO and it also has a low surface energy [131] of the same order of magnitude as SiO_2. Furthermore, as shown in Figure 3.11, the precipitated Si crystals is not necessary to be in continuous 1-D morphology (i.e. nanowire), thereby the deposition of SiNWs at the receding edge of moving liquid In is a particular case.

However, why dispersed Si crystals were precipitated? We suggest that as indium drops have large sizes with respect to the *a*-Si:H, the large-area substrate where *a*-Si:H is depleted beneath the In drop provides numerous preferential sites for Si nucleation and crystal growth (heterogeneous nucleation from liquid indium solution [105]), as illustrated in Figure 3.11.d.

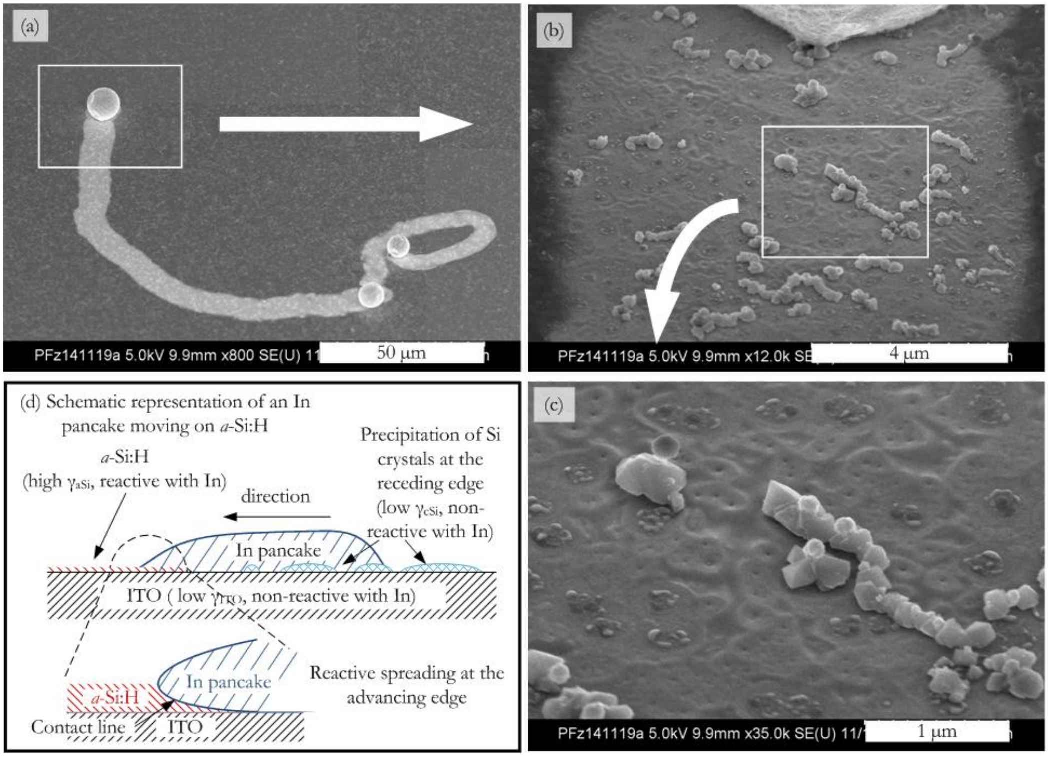


Figure 3.11 Motion of a large indium droplet on *a*-Si:H: (a) shows a spontaneous motion of liquid In on a-Si:H; (b, c) shows the trail of dispersed Si crystals on the substrate at its receding edge; (d) illustrates the motion mechanism based on wettability gradient.

3.2.3 CONCLUSION

According to the unbalanced Young's equation, see equation (3-2), the spontaneous motion of drops is governed by solid substrate surface energy gradients, which can be established by thermally or chemically modifying the substrates. From this viewpoint, a mechanism is proposed to account for the IPSLS growth mode, thanks to the two special cases of liquid In movement on *a*-Si:H.

The evolution of In NPs on *a*-Si:H is governed by the reactive spreading-and-coalescing behaviour, as a surface energy gradient is built up between SiO_2 (as well as *c*-Si on it) and *a*-Si:H due to indium-induced crystallization. The *μc*-Si:H/In interaction demonstrates the In does not react with *c*-Si. Furthermore, the large liquid In droplets moving on *a*-Si:H while leaving disperse Si crystals along their trajectory indicates that solid phase crystallization (SPC) of *a*-Si:H is the requirement for activating the movement of liquid In, and the growth of SiNWs is attributed to a particular case from this kind of phenomena, where the heterogeneous nucleation sites on the substrates are quite limited so that 1-D *c*-Si (i.e. SiNW) growth from In-Si liquid alloy is realized.

Figure 3.12 shows a schematic representation of the in-plane silicon nanowire growth mechanism: a liquid indium nanoparticle reactively wets (or spreads) on *a*-Si:H, depletes *a*-Si:H and precipitates crystalline silicon nanowire, which builds up a substrate surface energy between *a*-Si:H (high surface energy) and the non-reative substrate without *a*-Si:H. The movement of indium droplet maintains the *a*-Si:H/In contact, which enables a continuous growth of silicon nanowires.

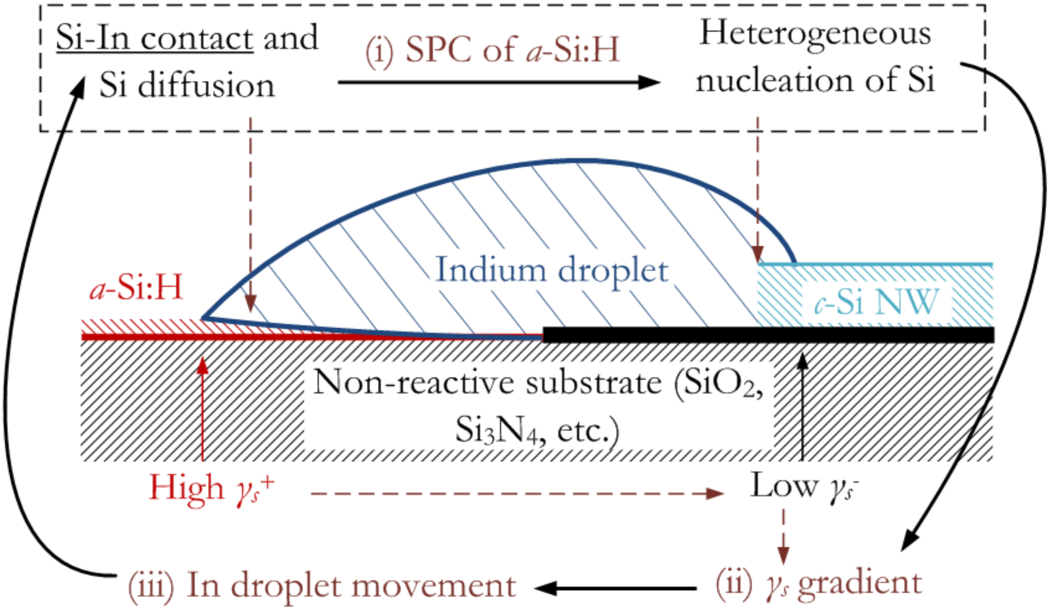


Figure 3.12 Schematic representation of in-plane silicon nanowire growth mechanism: a liquid indium nanoparticle reactively spreads on *a*-Si:H, depletes *a*-Si:H and precipitates crystalline silicon nanowire, which builds up a substrate surface energy between *a*-Si:H (high surface energy) and the substrate without *a*-Si:H.

3.3 DETAILED ANALYSIS OF THE GROWTH OF SOLID-LIQUID-SOLID SINWS

As discussed in 3.2, the phase transition from amorphous to crystalline Si due to In-induced crystallization establishes the substrate wettability (or solid surface energy) gradient, breaking the equilibrium of liquid on a-Si:H, thereafter spontaneous motion of liquid In on a-Si:H is activated due to the unbalanced Young's equation (see 3.1.2). The ongoing phase transition of Si on the substrate enables the continuity of this spontaneous motion.

However, the growth of SiNWs is not the requirement for the movement of liquid In, as shown in Figure 3.11. In order to investigate the mechanism of this 1-D *c*-Si growth based on spontaneous motion of liquid In, and furthermore to achieve a better control of the growth (e.g. morphology, direction, etc.), a systematic analysis on the geometry of IPSLS SiNWs was carried out via SEM observation.

3.3.1 SETTING UP THE IPSLS SYSTEM

In an in-plane Solid-Liquid-Solid system as shown in Figure 3.14.a. (Note that the In NP under SEM observation is in solid phase, while during the growth it is in liquid phase). There are two independent parameters: (1) $d_{s\text{-}NP}$ (or $d_{l\text{-}NP}$) is the diameter of In NP in solid (or liquid phase), as marked in Figure 3.14.b (for solid phase); (2) h_{aSi} is the thickness of *a*-Si:H layer on SiO_2 substrate, as illustrated in Figure 3.14.j. Due to the *a*-Si:H/In reactive contact, a **Trench** can be observed under SEM (as shown in Figure 3.14.c and illustrated in image j, its width is denoted as $d_{contact(aSiH)}$. A SiNW is located in the trench, which is resulted from the movement of liquid In on *a*-Si:H. Referring to Figure 3.14.d, e, f, the cross-sectional profile of the SiNWs can be simplified as spherical caps on the substrate, as illustrated in Figure 3.14.j, and the diameter is denoted as d_{NW}. We assume that there still exists residual *a*-Si:H on the substrate; on the contrary, based on the heteronucleation mechanism, the substrate under the SiNWs is probably exhausted of *a*-Si:H. Thereby, we suggest that the *a*-Si/In contact zone can be divided into two parts: **Zone 1** has remnant *a*-Si:H after liquid In passing over it, and **Zone 2** is depleted of *a*-Si:H which facilates the heterogeneous nucleation of silicon, as illustrated in Figure 3.14.j. As a matter of fact, Yu *et al.* have published a cross section image of in-plane epitaxial growth of SiNWs in which an *a*-Si:H edge as the one proposed here was measured [132], as shown in Figure 3.13. In this article the authors report that the shape of epitaxially grown SiNWs is flat in comparison with the non-epitaxial ones, which is in agreement with our SEM observation of SiNWs grown on *c*-Si substrate with native oxide (see Figure 3.14.d, e, f). We suggest that this may be due to higher surface energy of Si (100) plane with respect to that of SiO_2. Therefore the contact angle of crystalline Si on Si (100) is lower than the one on SiO_2, resulting in the flat cross-sectional profile of SiNWs (see 3.1.3 Heterogeneous nucleation from solution and Figure 3.4).

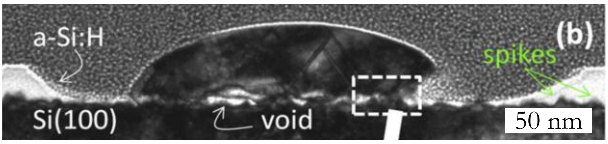


Figure 3.13 Cross-sectional TEM image of epitaxially grown IPSLS SiNWs.

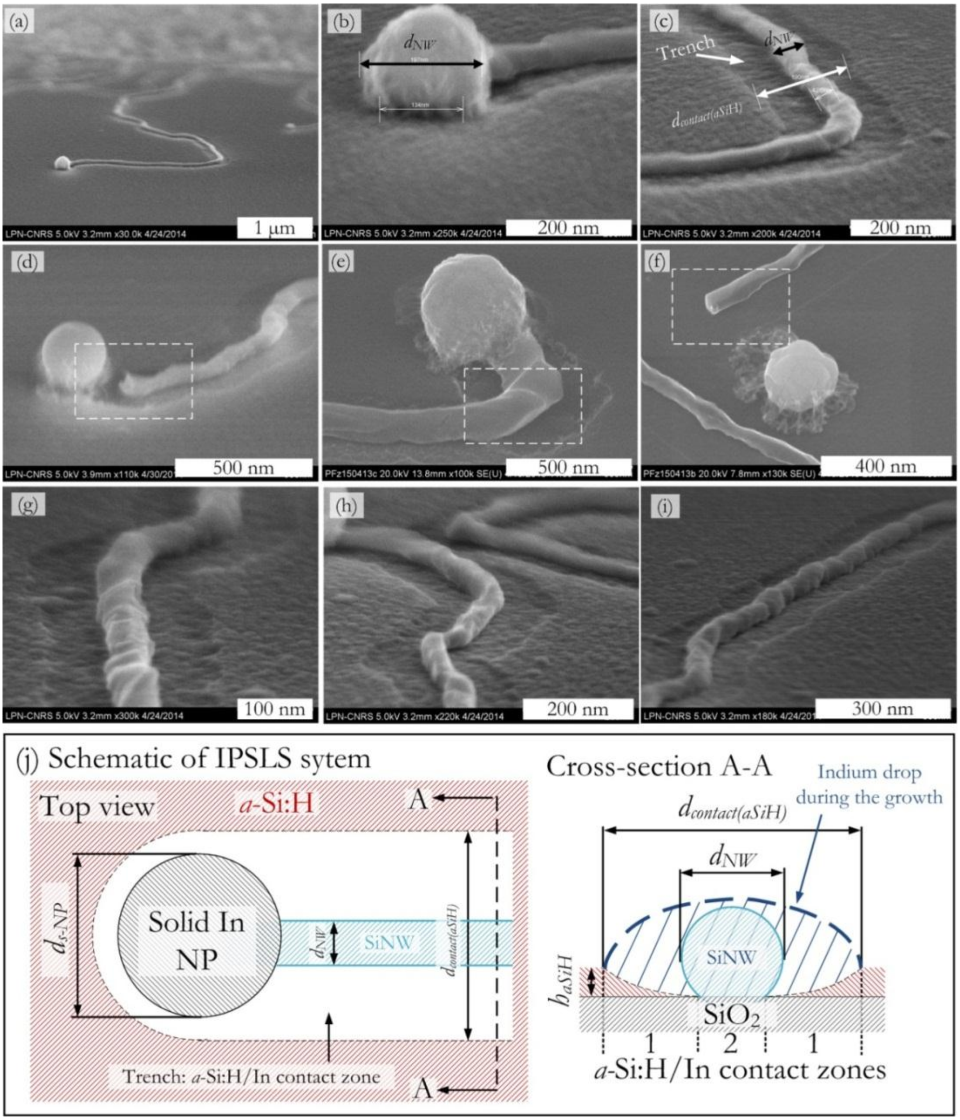


Figure 3.14 Set-up of the Solid-Liquid-Solid system: (a) SEM image of a typical SiNW grown via SLS mode; (b) SEM images showing the diameter of the In NP in solid phase ($d_{s\text{-}NP}$); (c) SEM image showing the diameters of a SiNW (d_{NW}) and the *a*-Si:H/In contact width $d_{contact(aSiH)}$; (d, e, f) SEM images indicating that the cross-sectional profile of SiNWs can be simplified as spherical caps; (g, h, i)

SEM images (with a tilt angle of 75°) showing the roughness of SiNWs and the probable residual *a*-Si:H in the *a*-Si:H/In contact zone, indicating that the *a*-Si:H/In contact zone consists of two parts: (1) Zone 1 with residual *a*-Si:H, at the two sides of the SiNW; (2) Zone 2 depleted with *a*-Si:H, which facilitates the heterogeneous nucleation of silicon, corresponding to d_{NW}. (j) schematic representation of IPSLS system, illustrating the geometrics in the SLS system, the cross-sectional view (A-A) emphasizing the part of *a*-Si:H/In contact zone with residual *a*-Si:H on the substrate, and the part with precipitated *c*-Si; The dashed line in the cross-section (j) represents the In drop during the growth.

3.3.2 INVESTIGATION OF IN-PLANE SOLID-LIQUID-SOLID SYSTEM

In order to investigate the relationship between the parameters determined by the process conditions (i.e. solid In NP diameter $d_{s\text{-}NP}$ and *a*-Si:H thickness h_{aSiH}) and the ones resulting from the NW growth process (i.e. SiNW diameter d_{NW} and *a*-Si:H/In contact width $d_{contact(aSiH)}$), *a*-Si:H layers of different thicknesses (9, 19 and 33 nm) were coated on substrates with ~5 nm thick In patterns defined electron-beam lithography for the growth of SiNWs at 450°C. Due to the redistribution of In NPs in the initial stage of SiNWs growth as mentioned in 3.2.1.1, different diameters of In NPs were obtained.

Figure 3.15 shows the diameter of the NWs and the contact width as functions of the diameter of the solid In nanoparticle for 3 thicknesses of the *a*-Si:H layer. We can see that there is a strong correlation between the *a*-Si:H/In contact zone $d_{contact(aSiH)}$ and the diameter of the solid In NP $d_{s\text{-}NP}$. On the contrary, there is a subtle variation of the SiNWs diameter d_{NW} as a function of d_{NP}. Interestingly, Figure 3.16 reveals that a linearity does exist between d_{NW} and $d_{s\text{-}NP}$, in particular for the thinnest *a*-Si:H layer (i.e. 9 nm) On the other hand, Figure 3.17 shows the variation of the diameter of SiNW d_{NW} as a function of *a*-Si:H thickness, also in a monotonic increasing mode like the effect of In NP diameter.

Figure 3.18 shows the diameter of the SiNWs as a function of the width of the contact . We obtain a strong correlation with a ratio of d_{NW} over $d_{contact}$ around 0.3, indicating that for the successful growth of SiNWs, the ratio of *a*-Si:H/In contact zone 2 depleted with *a*-Si:H for Si precipitation (as illustrated in Figure 3.14.j) over the entire contact zone is a constant.

Thus, the diameter of SiNW d_{NW} is a function of the contact width $d_{contact(aSiH)}$, and $d_{contact(aSiH)}$ is a function of diameter of the In NPs $d_{s\text{-}NP}$ and *a*-Si:H thickness h_{aSiH}, as shown in equations (3-24) and (3-25):

$$d_{NW} = 0.3d_{contact(aSiH)}, \tag{3-24}$$

$$d_{contact(aSiH)} = f(d_{s-NP}, h_{aSiH}). \tag{3-25}$$

To study the dependence of $d_{contact(aSiH)}$ on $d_{s\text{-}NP}$ and h_{aSiH}, $d_{contact(aSiH)}$ and h_{aSiH} are normalized by the corresponding $d_{s\text{-}NP}$, as shown in equation (3-26):

$$\beta = f(\alpha, 1), \tag{3-26}$$

where a and β denote $h_{aSiH}/d_{s\text{-}NP}$ and $d_{contact(aSiH)}/d_{s\text{-}NP}$, respectively.

Figure 3.19 shows the linear relationship between α and β, and the fitting result is given by equation (3-27):

$$\beta = 1.26 + 3.2\alpha \tag{3-27}$$

By substituting α with $h_{aSiH}/d_{s\text{-}NP}$, β with $d_{contact}/d_{s\text{-}NP}$ in equation (3-27), the In-*a*-Si:H contact zone as a function of the size of solid In NP and thickness of *a*-Si:H is given by equation:

$$d_{contact(aSiH)} = f(d_{s-NP}, h_{aSiH}) = 1.26d_{s-NP} + 3.2h_{aSiH}. \tag{3-28}$$

By combining equations (3-24) and (3-28), the diameter of SiNWs d_{NW} can be expressed as:

$$d_{NW} = 0.3f(d_{s-NP}, h_{aSiH}) = 0.4d_{s-NP} + h_{aSiH}. \tag{3-29}$$

Furthermore, the intercept 1.26 and the slope 3.2 of the linear fitting in Figure 3.19 provide several informations:

(i) If there is no *a*-Si:H on the SiO_2 substrate; then $\alpha=0$ and β turns to be $d_{contact(SiO2)}/d_{s\text{-}NP}=1.26$, which is in agreement with previous contact angle studies of liquid In on SiO_2 [115]. This means that the profile of liquid In NP on SiO_2 is semi-spherical, with contact angle of 90°, given that no volume change of In NP occurs during the phase transition from solid to liquid, the relationship between $d_{s\text{-}NP}$ and $d_{l\text{-}NP}$ ($d_{l\text{-}NP}$ on SiO_2 can be also denoted as $d_{contact(SiO2)}$, as illustrated in Figure 3.20.a and b) is determined by equation (3-30):

$$\frac{4}{3}\pi(d_{s-NP}/2)^3 = \frac{1}{2} \times \frac{4}{3}\pi(d_{contact(SiO2)}/2)^3, \tag{3-30}$$

thus

$$d_{contact(SiO2)}/d_{s-NP} = \sqrt[3]{2} = 1.26. \tag{3-31}$$

(ii) If the size of In NP is far greater than the thickness of *a*-Si:H, as $d_{NP} \gg h_{aSiH}$, then α approaches to 0 and β also approaches to 1.26, reflecting that under this condition the width of contact zone mainly relates with the size of In NP, the example can be referred to the liquid In pancake moving on *a*-Si:H as discussed in 3.2.2.

(iii) Equation (3-27) indicates the remarkable reactive spreading phenomenon of liquid In on *a*-Si:H, compared with its wetting behavior on SiO_2.

Let

$$\eta = \frac{d_{contact(aSiH)} - d_{contact(SiO2)}}{d_{contact(SiO2)}} \tag{3-32}$$

be the **reactive spreading coefficient**, by combining equations (3-27), (3-31) and (3-32), we obtain:

$$\eta = 2.5\alpha = 2.5h_{aSiH}/d_{s-NP}, \tag{3-33}$$

which monotonically increases with the thickness of *a*-Si:H and monotonically decreases with the diameter of In NP.

(iv) Considering the redistrution of In NP in the initial stage of SiNWs growth, as illustrated in Figure 3.8, let $d_{spacing}$ be the distance between a pair of neighbouring idendical In NPs. In order to realize the redistribution via coalesence behavior induced by reactive spreading, it has to satisify the relationship:

$$d_{spacing} < d_{contact(aSiH)} - d_{contact(SiO2)}, \tag{3-34}$$

as illustrated in Figure 3.21. By combining equations (3-28), (3-31) and (3-34), the condition for coalescence can be written as:

$$d_{spacing} < 3.2 h_{aSiH}. \tag{3-35}$$

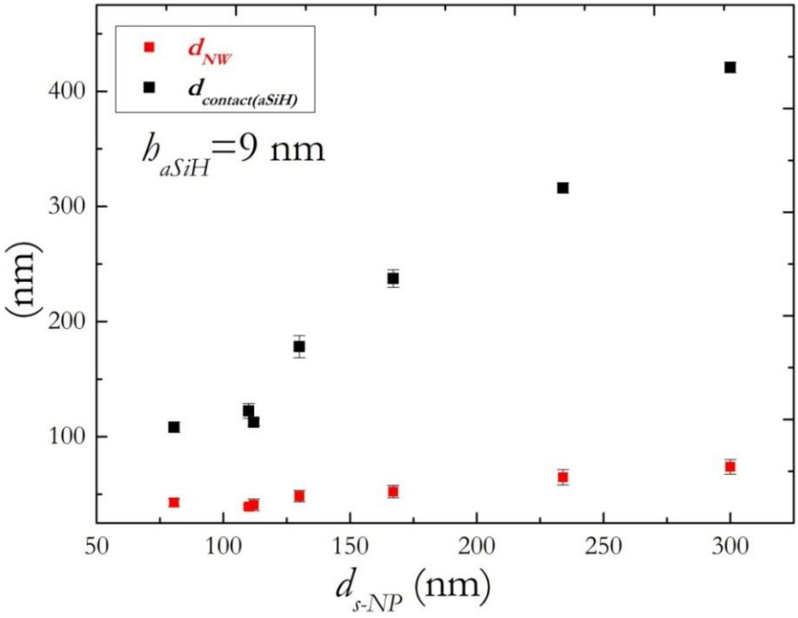


Figure 3.15 SiNW diameter d_{NW} and width of *a*-Si:H/In contact zone $d_{contact(aSiH)}$ as a function of the solid In NP diameter $d_{s\text{-}NP}$, with three *a*-Si:H thicknesses h_{aSiH}. To be continued in the next page.

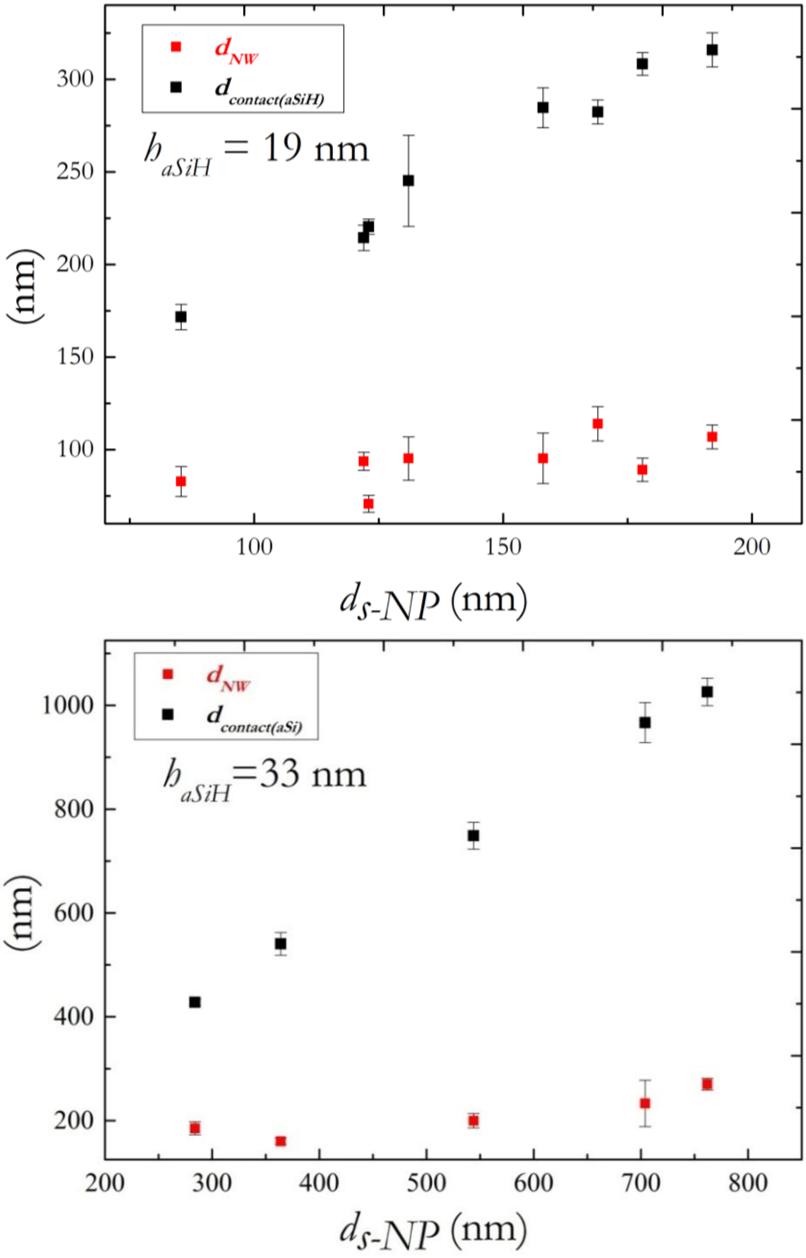
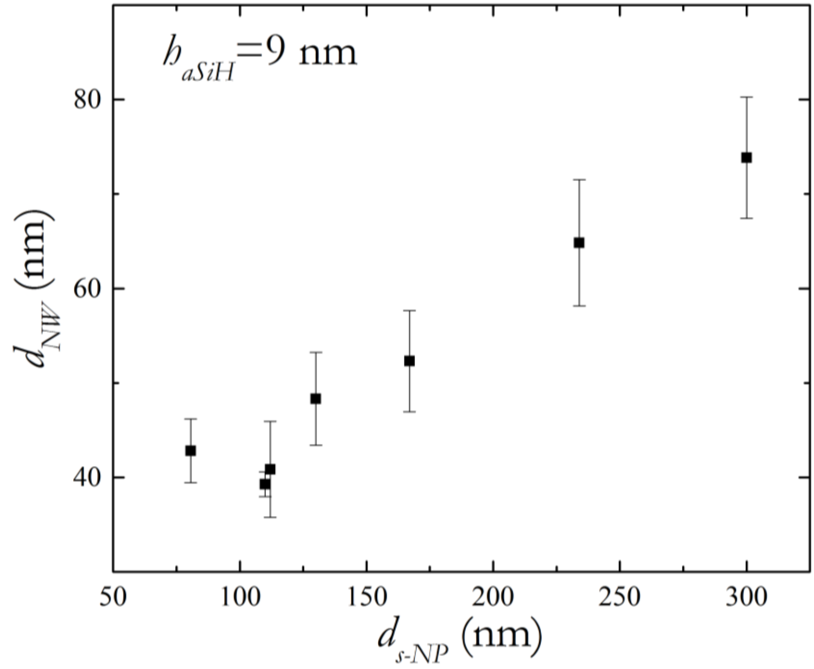


Figure 3.15 (Continued) SiNW diameter d_{NW} and the *a*-Si:H/In contact width $d_{contact(aSiH)}$ as a function of the solid In NP diameter $d_{s\text{-}NP}$, with three *a*-Si:H thicknesses h_{aSiH}.



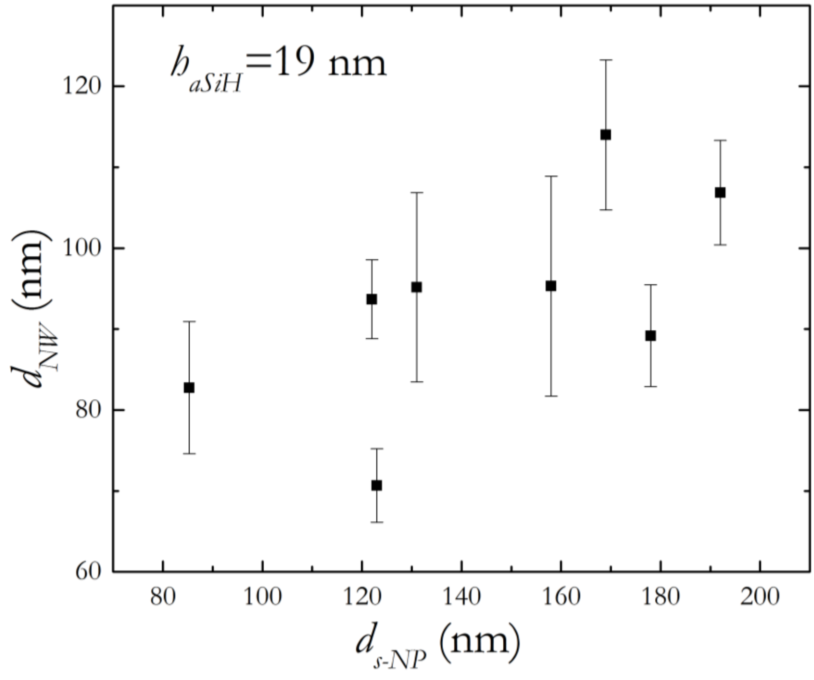


Figure 3.16 SiNW diameter d_{NW} as a function of the solid In NP diameter $d_{s\text{-}NP}$, for the three different *a*-Si:H thicknesses h_{aSiH}. To be continued in the next page.

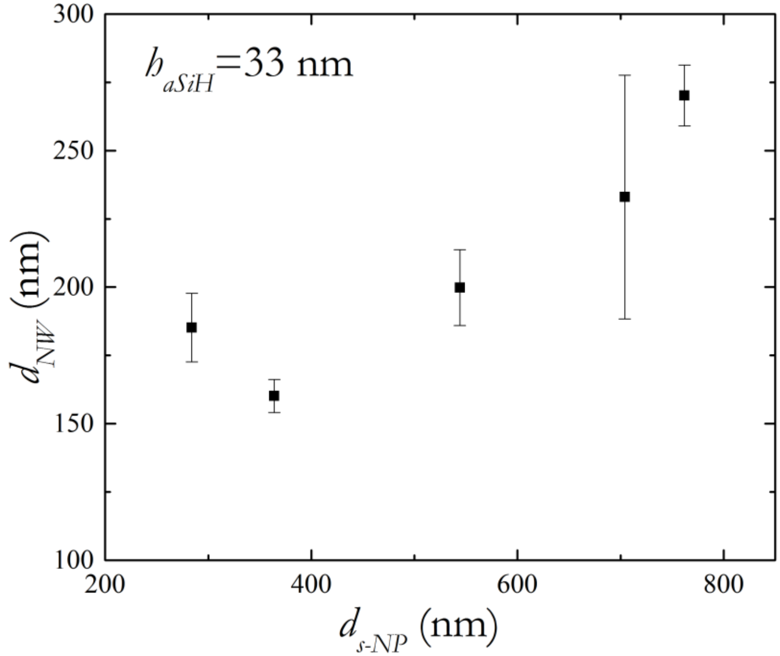


Figure 3.16 (Continued) SiNW diameter d_{NW} as a function of the solid In NP diameter $d_{s\text{-}NP}$, for the three different *a*-Si:H thicknesses h_{aSiH}.

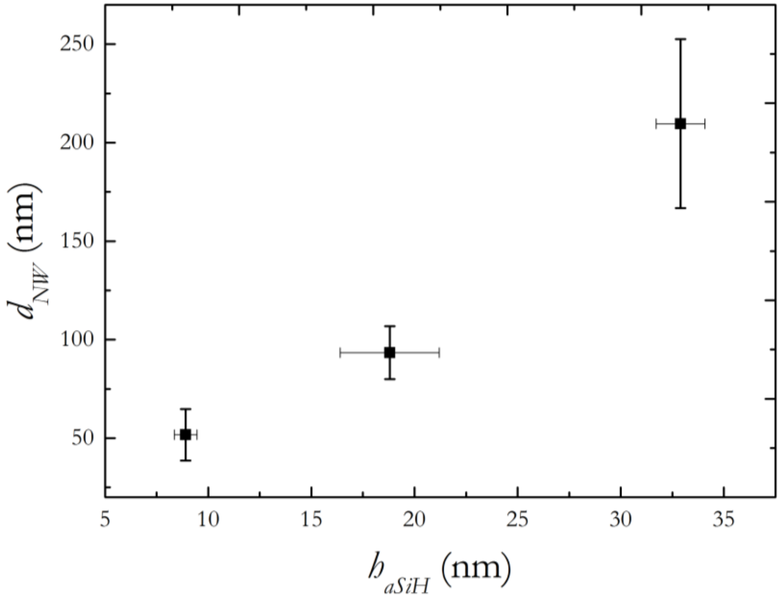


Figure 3.17 SiNW diameter d_{NW} as a function of *a*-Si:H thickness h_{aSiH}.

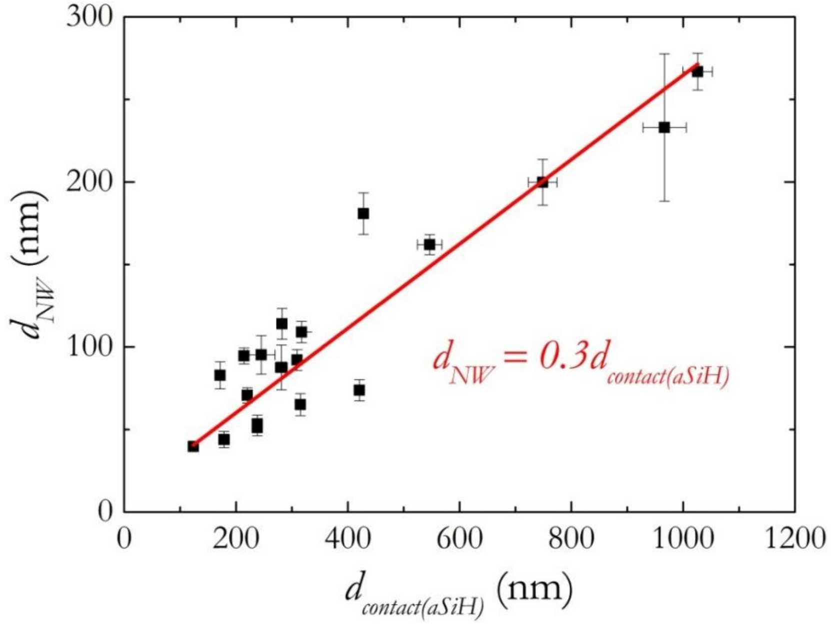


Figure 3.18 SiNW diameter d_{NW} as a function of the *a*-Si:H/In contact width $d_{contact(aSiH)}$.

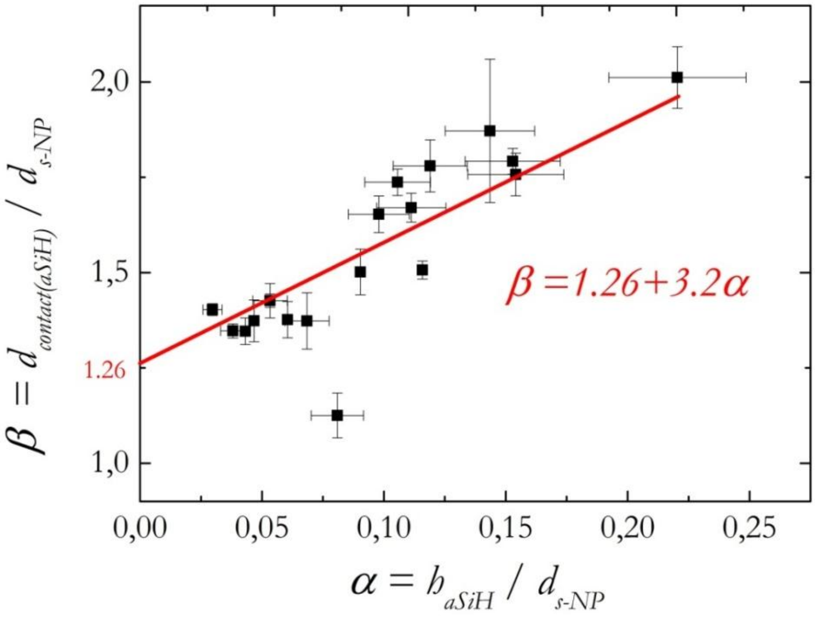


Figure 3.19 The contact width $d_{contact(aSiH)}$ and *a*-Si:H thickness h_{aSiH}, normalized by the corresponding solid In NP diameter $d_{s\text{-}NP}$, with the linear fitting. A strong correlation is obtained.

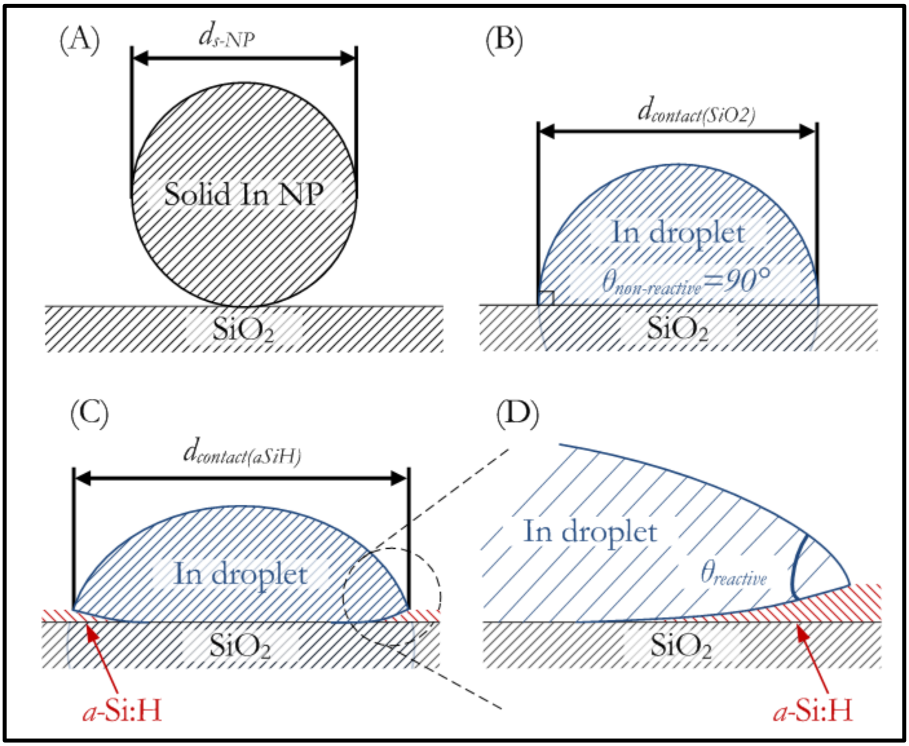


Figure 3.20 Schematic representation of the reactive spreading of liquid In NP on *a*-Si:H: (a) spherical In NP of diameter $d_{s\text{-}NP}$ in solid phase on SiO$_2$; (b) semi-spherical In NP in liquid phase on SiO$_2$ with a contact diameter $d_{contact(SiO2)}$; (c) Liquid In NP reactively spreads on a-Si:H with a contact diameter $d_{contact(aSiH)}$; (d) Triple phase line in SLS system with contact angle $\theta_{reactive}$.

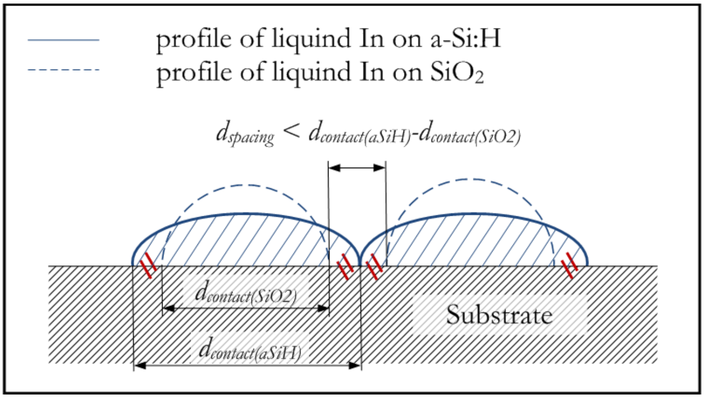


Figure 3.21 Illustration of the limitation on the distance ($d_{spacing}$) between two neighbouring identical In NPs: the profiles of liquid In on *a*-Si:H and SiO$_2$ are in solid and dash line, respectively. $d_{spacing}$ should be less than $d_{contact(aSiH)}$-$d_{contact(SiO2)}$.

3.3.3 CONCLUSION

The growth of IPSLS SiNWs can be considered as a special type of spontaneous motion of liquid In on *a*-Si:H, which leaves continuous 1-D *c*-Si at the receding side of the liquid In. In order to study the uniqueness of this type of liquid In movement, a geometric investigation and statistical analysis are carried out to analyse the SiNWs grown by In NPs of various diameters and *a*-Si:H films of different thicknesses (in the range of 8~30 nm).

In the in-plane solid-liquid-solid dynamic system, a liquid In NP moves on the *a*-Si:H surface with a thickness of h_{aSiH}, leaving a trench with a width $d_{contact(aSiH)}$, where a SiNW (in diameter of d_{NW}) is located inside the zone. SEM observations show that there might be residual *a*-Si:H left at the two sides of the SiNW in the trench; however, it is expected that the substrate surface beneath the SiNW is exhausted of *a*-Si:H, providing heterogeneous nucleation site for *c*-Si crystal growth. Our study shows that the ratio of d_{NW} over $d_{contact(aSiH)}$ is constant around 0.3. Moreover, normalized $d_{contact(aSiH)}$ and h_{aSi} by solid In NPs $d_{s\text{-}NP}$ show a linear relationship. Thus, the relationship between d_{NW}, $d_{contact(aSiH)}$ and h_{aSi} is quantitatively described. Also, our results demonstrate that the contact angle of liquid In on SiO_2 (where h_{aSiH}=0 nm) is around 90°C, which is in agreement with previous studies. As the normalized $d_{contact(aSiH)}$ (i.e. $d_{contact(aSiH)}/d_{s\text{-}NP}$) reflects the deformation of the liquid In on *a*-Si:H with respect to its spherical shape in solid phase, this linear relationship (see Figure 3.19) indicates that liquid In NPs experience stronger reactive spreading on thicker *a*-Si:H layers.

3.4 SUBSRATE TEMPERATURE DEPENDENCE OF *a*-SI:H PROPERTIES

With the purpose of integrating in-plane SiNWs in flexible electronics [133]-[135], growth temperature should be limited as much as possible [136][137] (e.g. below 250°C [138]). In this section, the minimum temperature for activating the SiNWs growth is firstly investigated. Furthermore, efforts are made to lower this growth temperature by modifying the structural properties of *a*-Si:H thin films, in particular by reducing their deposition temperature.

3.4.1 ACTIVATION TEMPERATURE OF *a*-SI:H/IN REACTION

Indium thin films with a nominal thickness of ~50 nm were thermally evaporated on *c*-Si wafers with native oxide. Then the samples were treated by a standard H_2 plasma exposure and a ~20 nm *a*-Si:H coating (deposited at a norminal temperature of 180°C[7]) and annealing at 350°C and 300°C, respectively. Figure 3.22 shows the SEM results: (1) annealing at 300°C cannot activate SiNW growth; (2) growth of SiNWs can be activated by 350°C annealing, however the growth of SiNWs seems to be less continuous[8], the light points circled in images (b) and (c) are expected as tiny Si crystals, therefore we suggest that the liquid In NP experiences a stick-and-slip behaviour. One possible explanation is that temperature affects the nucleation rate J [107]:

$$J = K_0 \exp(-\Delta G_{heter}^{*}/\kappa T) \tag{3-36}$$

where K_0 is the kinetic coefficient, $\Delta G_{heter}{}^{*}$ is the heterogeneous nucleation energy barrier, κ is the Boltzmann constant, and T is the absolute temperature. Therefore, J decreases monotonically as T decreases. Furthermore, the kinetic coefficient K_0 can be determined by:

$$K_0 = N_0 \nu_0 \tag{3-37}$$

where N_0 is the solubility of the solute expressed as the number of atoms (or molecules) per unit volume, and ν_0 is the frequency at which the critical nuclei becomes supercritical and transform into crystals. According to In-Si binary phase diagram [139] (see Figure 3.23), the solubility of Si atoms in liquid In decreases with temperature, resulting in a decrease of the kinetic coefficient K_0. This also contributes to the delay of nucleation process.

Therefore, the *c*-Si nucleation rate is lowered at 350°C with respect to higher temperature, which means the Si phase transition from amorphous to crystalline is retarded, and subsequently the establishment of surface energy gradient is delayed. Therefore the liquid In is stuck on the substrate for a moment, after completing the Si phase transition underneath it, liquid In can move on towards the *a*-Si:H region with higher surface energy.

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[7] Note that the calibrated substrate temperature is below the melting point of In (157°C), see Appendix A.

[8] The standard annealing temperature is 450°C, and the grown SiNWs can be referred to the cover picture of this thesis.

That could be a reason why in the SEM images (a), (b) and (c) there are almost identical circular prints in regular interval along the trajectory of SiNWs.

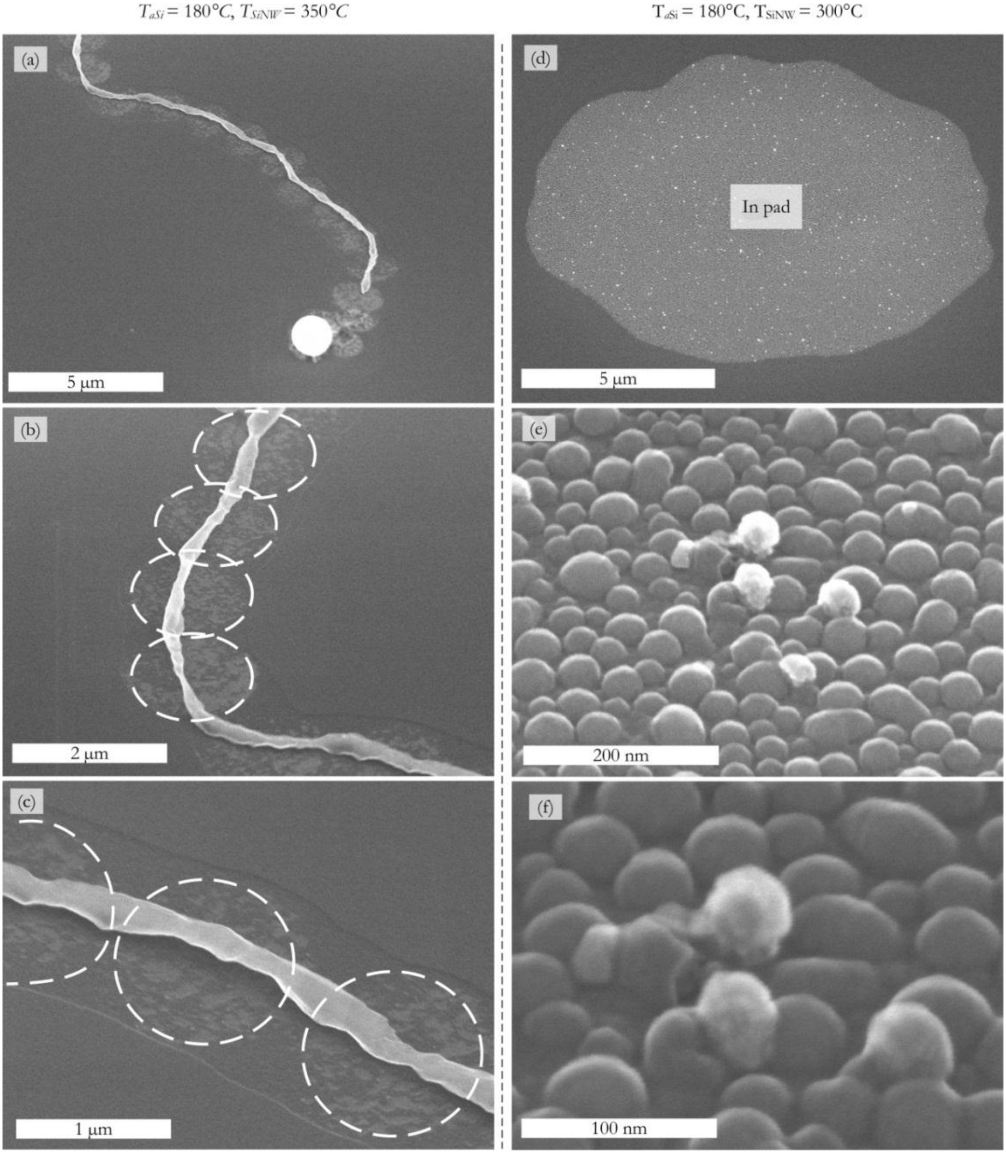

Figure 3.22 Temperature dependent *a*-Si:H/In interaction: (a-c) SEM images of reaction of In with *a*-Si:H (deposited at 180°C) at 350°C, with SiNWs grown; (d-f) SEM images of reaction of In with *a*-Si:H (deposited at 180°C) at 300°C, without SiNWs grown.

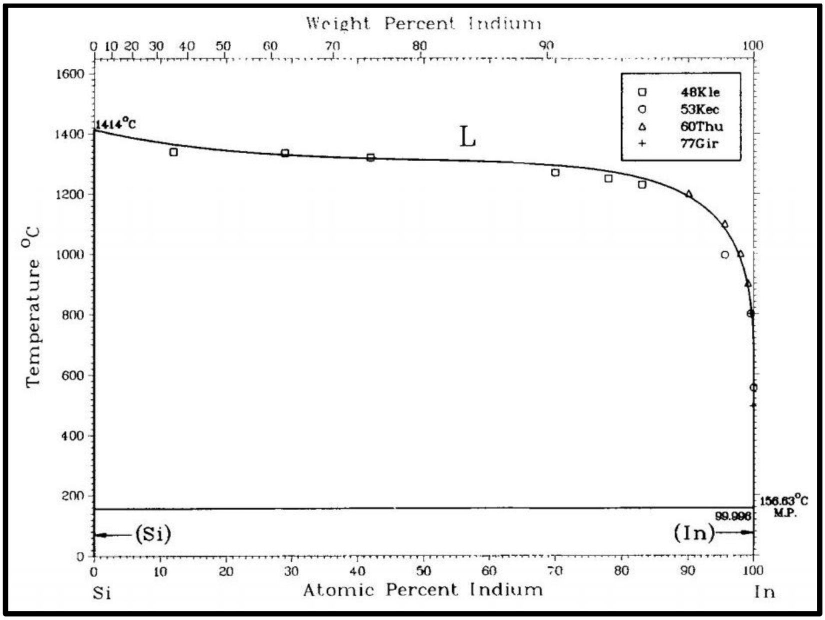

Figure 3.23 In-Si binary phase diagram [139].

3.4.2 EFFECT OF *a*-SI:H STRUCTURE ON SINW GROWTH

As discussed above, low temperature (e.g. 300°C~350°C) does not favour the SiNW growth, behind which it is the weakening of *a*-Si:H/In interaction. Solid phase crystallization (SPC) [140]-[142] theory relies on the fact that *a*-Si:H has higher Gibbs energy than *c*-Si, however the phase transition from amorphous to crystalline cannot take place spontaneously without a Gibbs energy barrier jump [143], assisted by thermal annealing [144] for instance. Figure 3.24 illustrates the Gibbs energy configuration of crystalline and amorphous states, showing the Gibbs energy change ΔG_{ac} in phase transition and the Gibbs energy barriers $\Delta G_{1,2}$ of the forward and reverse jump of atoms due to the crystallization dynamics.

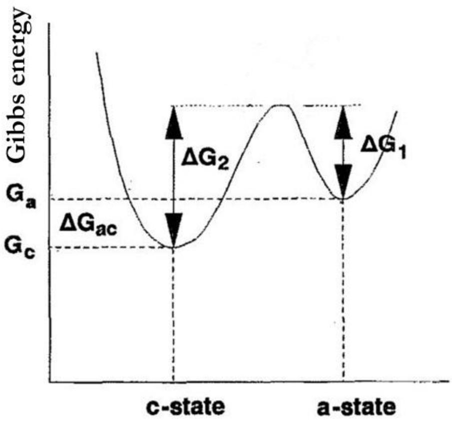

Figure 3.24 Gibbs energy configuration of crystalline and amorphous states [143].

Hence, in order to decrease the critical growth temperature of in-plane SiNWs, lowering the forward jumping barrier ΔG_1 by increasing the Gibbs energy of *a*-Si:H ΔG_a seems a logic way to proceed. G_a is associated with the structural relaxation of the *a*-Si:H network [145]. The *a*-Si:H structure can be modified by tuning the deposition parameters [146]. In practice, the deposition temperature is one of the main parameters determining the structural properties of *a*-Si:H thin films. As the substrate temperature is increased in the range of 100°C~250°C, the density of states (DOS) [147], hydrogen concentration C_H [148] and optical band gap E_g [149] are reduced. Besides, the gas flow rate, pressure and ion bombardment (i.e. RF power) also influence the structure of a-Si:H [150][153].

Raman scattering [154] sensitively reflects the vibrational DOS of amorphous semiconductors [155][156], by which the structural disorder [157] like bond distortion and stretching strain can be probed [158][159]. The energy barrier for structural relaxation can be determined [160]. The average bond-angle distortion ΔΘ can be extracted from Raman spectrum [161]:

$$\Gamma/2 = 3.2 \cdot \Delta\Theta + 7.4 \tag{3-38}$$

where $\Gamma/2$ is the full width at half maximum (FWHM) of the transverse optical (TO) peak, which means that the broadening degree of the peak reflects the disorder in the amorphous Si network [162]. Furthermore, modelling of the bond distortion energy distribution [163] provides an approximation of the strain energy U in *a*-Si as a function of bond-angle distortion:

$$U = \sum 6 \cdot [\tfrac{1}{2} k_\Theta (d_{Si-Si} \cdot \Delta\Theta)^2] \tag{3-39}$$

where k_Θ is the bond bending force constant and $d_{Si\text{-}Si}$ the Si-Si atomic distance. Therefore, the decrease of ΔΘ reflects the structural relaxation, which results in the Gibbs energy reduction. Besides, the TO peak shift towards the higher wavenumbers also indicates the structural relaxation [164].

Based on the above review, a simple strategy for lowering the in-plane SiNWs growth temperature is proposed: to intentionally enhance the disorder degree in the amorphous network by lowering the deposition temperature. Figure 3.25 shows the plotting of TO peak position and FWHM of *a*-Si:H thin films prepared at different conditions. From nominal 180°C to 120°C, TO peak shifts to lower wavenumbers and FWHM increases, which indicates that extra disorder is introduced in the *a*-Si:H and raises its Gibbs energy. Moreover, post-annealing at 350°C does not remarkably get *a*-Si:H (120°C) structure relaxed, compared with the Raman spectrum before annealing. This means that the Gibbs energy decrease of *a*-Si:H can be ignored during the annealing step for in-plane SiNWs. Furthermore, as shown in Table 3.2, the fitting results of the imaginary part ε_2 of pseudo dielectric function in Tauc-Lorentz dispersion model [165][166] reinforces this strategy as both the optical band gap E_g, and the broadening of the ε_2 peak (*C*) (related to the increase of the disorder) increase when going from high to low temperature deposition, reflecting the increase the Gibbs energy in the *a*-Si:H film.

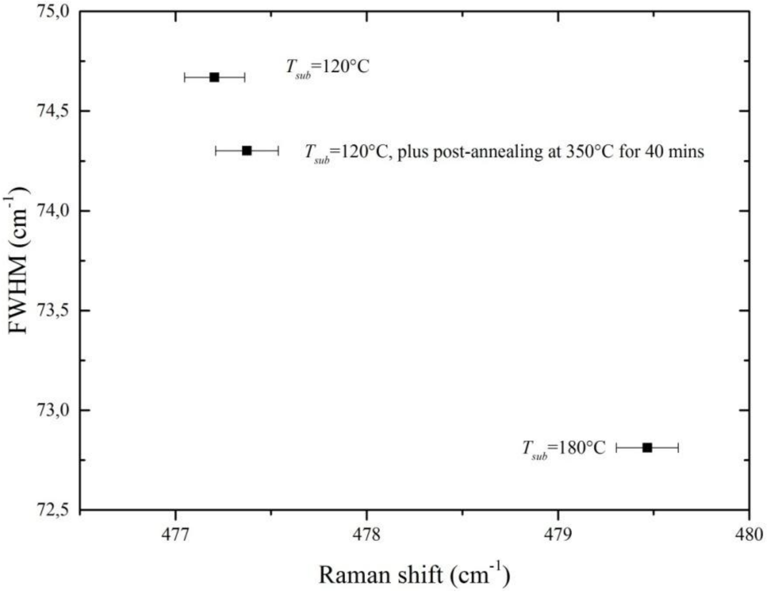

Figure 3.25 FWHM as a function of the TO peak position for Raman Spectra of *a*-Si:H deposited at different substrate temperatures.

Table 3.2 Fitting results of the imaginary part ε_2 of the pseudo-dielectric function in Tauc-Lorentz dispersion model for *a*-Si:H deposited at 120°C and 180°C, where E_g is the optical band gap, E_0 is the peak central energy of ε_2, and C is the broadening term of the peak.

$T_{deposition}$ (°C)	E_g (eV)	E_0 (eV)	C
180	1.72 ± 0.01	3.54 ± 0.12	2.06 ± 0.04
120	1.79 ± 0.12	3.62 ± 0.02	2.18 ± 0.04

Figure 3.26 shows the SiNWs growth at nominal 350°C with *a*-Si:H deposited at 120°C and 180°C. Consistent with the results in 3.4.1, the trail of stick-and-slip is very common for SiNWs grown on *a*-Si:H deposited at 180°C (see a, b), however SiNWs look pretty continuous on *a*-Si:H deposited at 120°C (see c, d). Hence, this successful preliminary test demonstrates that our strategy for lowering the growth temperature is logic and easy to apply. Further experiments should be continued, not only limited on the *a*-Si:H deposition temperature, but also involving other considerations such as gas pressure and ion bombardment to enhance the Gibbs energy of *a*-Si:H films.

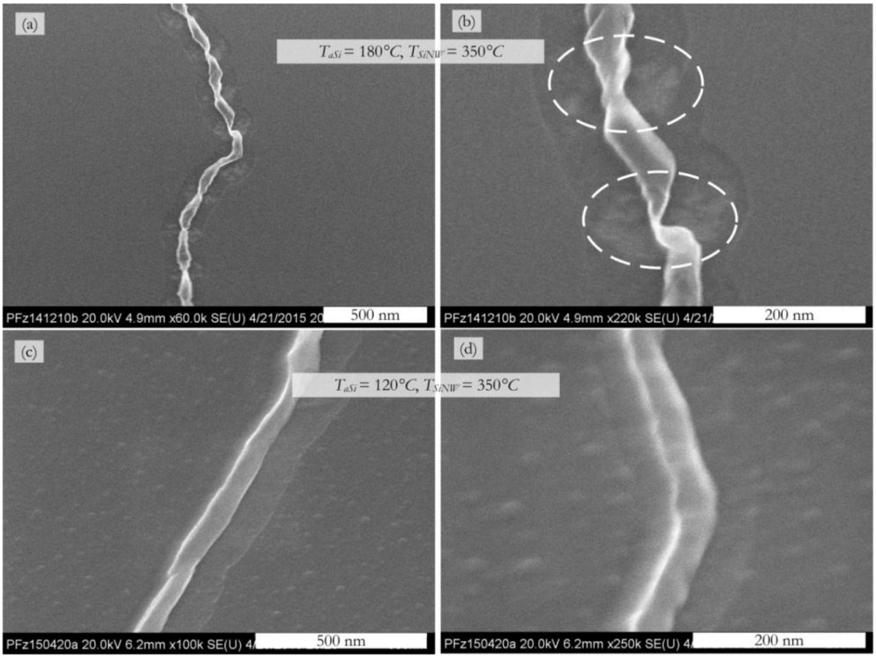

Figure 3.26 Effect of the *a*-Si:H deposition temperature on the SiNWs growth at 350°C: (a, b) SEM images of SiNWs grown on *a*-Si:H deposited at 180°C; (c, d) SEM images of SiNWs grown on *a*-Si:H deposited at 120°C.

3.4.3 CONCLUSION

The above results show that as the substrate temperature decreases, the growth of SiNWs (or, in another view, liquid In reactive spreading on *a*-Si:H) tends to be in a stick-and-slip manner, and finally gets completely suppressed below a critical value (<350°C). This is because low temperature does not favour the In-Si intermixing, nor the Si nucleation and crystal growth. Solid phase crystallization theory tells that in order to succeed the phase transition from amorphous to crystalline state, a Gibbs energy barrier should be overcome. With the purpose of lowering this barrier, we have to raise the Gibbs energy of *a*-Si:H, which can be tuned by the preparation conditions and probed by characterization tools like Raman scattering and spectroscopic ellipsometry.

Therefore, a simple strategy of decreasing the *a*-Si:H deposition temperature has been proposed to intentionally introduce extra disorder in the amorphous network. In this way, we succeed the growth at nominal 350°C. This method can be explained in another way: it spends less energy ($T_{depostion}$) to build up amorphous network, it spends less energy (T_{growth}) to break and reorganise it.

3.5 METAL CATALYST CANDIDATES FOR IN-PLANE SINWS GROWTH

In order to verify the uniqueness of In as the metal catalyst for mediating the growth of IPSLS SiNWs, tin (Sn) and gold (Au) are selected for testing their interaction with *a*-Si:H, which also brings insight to deepen our understanding of the growth mechanism. Besides, *a*-Ge:H/In interaction is also investigated, with the purpose of producing GeNWs by the growth techniques we have developed.

3.5.1 SN/*a*-SI:H INTERACTION

Sn thin films with a nominal thickness of ~5 nm were thermally evaporated on *c*-Si substrates with native oxide. After that, the Sn thin films were treated by our standard H_2 plasma reduction (100 sccm, 400 mTorr of H_2, 5W, 300°C, 5 mins) and ~10 nm *a*-Si:H was deposited at nominal 180°C. Then this bilayer structure was annealed at a nominal 600°C[9] for activating the reaction. Note that the eutectic temperature of Sn-Si alloy is 232°C (see Table 3.3).

As shown in Figure 3.27, the redistribution of Sn NPs is quite similar to that we have obtained for indium (see 3.2.1.1), which is revealed by etching the residual *a*-Si:H and *c*-Si materials by H_2 plasma after all the steps.

However, the morphology of SiNWs differs from the ones catalysed by In. Indeed, as shown in Figure 3.28, the diameters of SiNWs decrease along the axial direction, and no Sn NPs are observed at the tips of SiNWs. Thus, it seems that liquid Sn NPs did not move on *a*-Si:H as smoothly as the ones of In NPs. On one hand, the structure of *a*-Si:H was relaxed due to high temperature annealing at 420°C, thereby the reactive spreading behaviour of liquid Sn on it was suppressed. On the other hand, the reactive spreading effect in the initial stages of SiNWs growth seems stronger than that of In, as shown in Figure 3.28.e. This is probably because liquid Sn can dissolve more Si atoms than In, whose atomic fraction is five orders of magnitude higher at the eutectic point, as listed in Table 3.3. It is known that interfacial chemical bonding can be built up between the solute and the solid substrates and thus affects the wetting behaviour [167]-[172]. This could explain the difference in the reactive spreading between liquid Sn and In at the initial stage of SiNWs growth, that liquid Si-Sn alloy with higher Si atomic fraction wets the substrate more significantly than liquid Si-In alloy.

Another especial phenomenon is the disappearance of Sn NPs at the end points of SiNWs, which indicates that the growth was stopped unintentionally due to the consumption of Sn catalyst during the growing process. The reason still remains unclear: (1) the evaporation of Sn at high temperature (calibrated value is 420°C) could be one (see Figure 2.7); (2) the behaviour of metallic atoms incorporating into NWs during growth [173]-[179] could also contribute to the consumption of Sn, however the amount of Sn

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[9] The calibrated temperature is ~420°C, see Appendix A.

atoms diffused into SiNWs is quite limited in the range of $10^{19}\sim10^{20}$ atoms per cm^3 as measured by APT (atomic probe tomography) [180]; (3) surface migration of metal on NWs surfaces was also proposed to explain the evolution of metal catalyst (Au and Sn) during VLS growth [181][182], however, from our point of view, this surface wetting behaviour is expected due to the reactive spreading of liquid metal on the *a*-Si:H deposited on the sidewall during the VLS growth, but as no *a*-Si:H deposition takes place during the IPSLS growth (see 3.6), this argument does not hold.

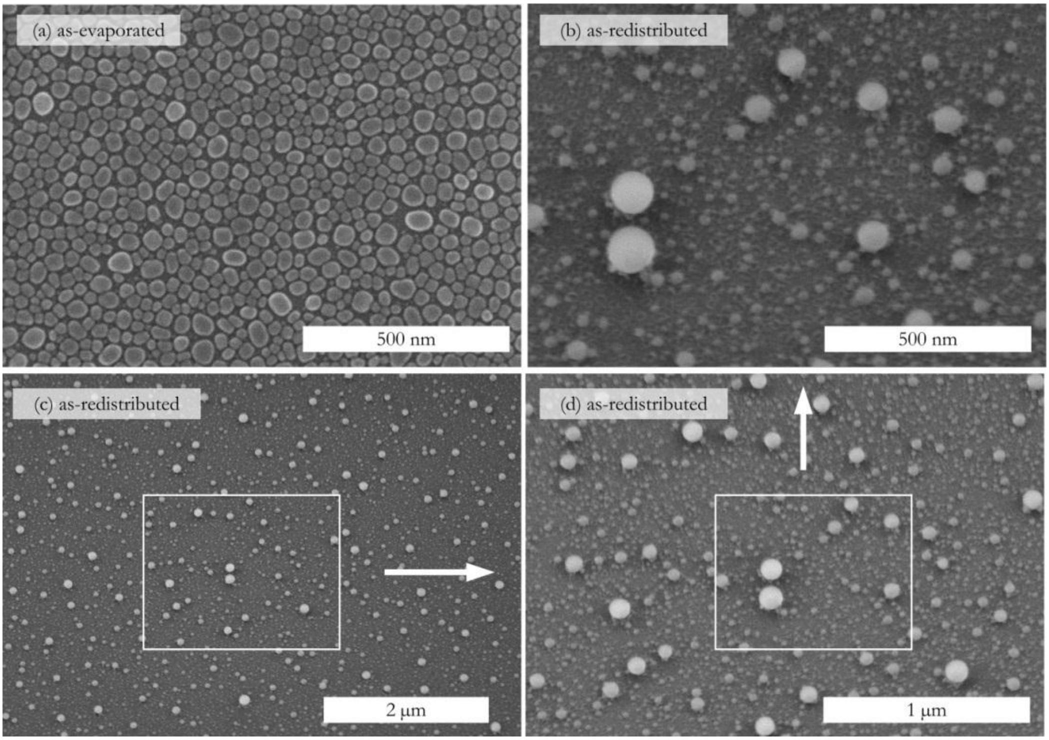

Figure 3.27 Redistribution of Sn NPs: nominal 5nm Sn thin film (a) treated by normal H_2 plasma reduction, 10 nm *a*-Si:H coating and annealing at 600°C, then treated by H_2 plasma for removing the remnant *a*-Si:H and *c*-Si (b, c, d).

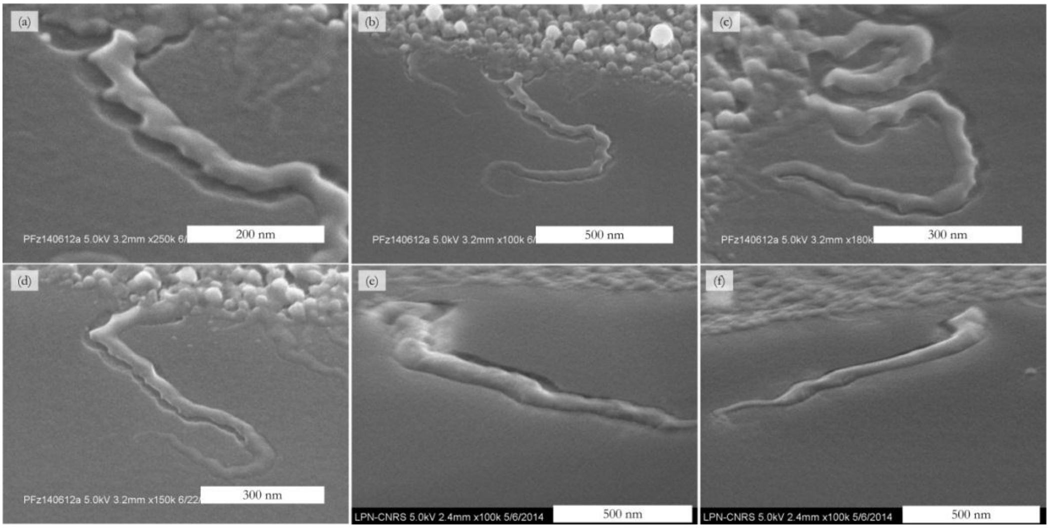

Figure 3.28 Morphology of SiNWs catalysed by Sn NPs.

3.5.2 AU/*a*-SI:H INTERACTION

Au thin films with a nominal thickness of ~5 nm were thermally evaporated on *c*-Si wafer coated with a barrier layer of ~100 nm sputtered SiO_2 layer, and treated with the same *a*-Si:H coating and bilayer annealing process as in the case of Sn. Figure 3.29 shows SEM images of: (1) the as-evaporated Au (a, b) displaying an island-like morphology; (2) the annealed bilayer (c, d) in which tiny Si crystals can be observed, but no SiNWs growth; (3) after removing residual *a*- and *c*- Si materials by H_2 plasma etching, the redistribution of Au islands was also revealed.

Here, a direct impression is that this Au-Si interaction is more like a MIC process (i.e. polycrystalline Si segregates the Au above and beneath it, see Figure 3.1.a) rather than the IPSLS growth. It has been also reported that Au-catalysed SiNWs via the VLS mode can be grown horizontally on the SiO_2 [183] or Si (111) surface [184], thus it is expected that the difference in the growth methods (VLS vs IPSLS) does determine the different morphologies of Au-Si interaction products, as will be also discussed later in 3.6.

Another assumption is that the Si atomic fraction in liquid Au-rich Au-Si alloy is much higher (see Table 3.3) than that of Si in In and Sn. Therefore, more Si atoms are needed for the Au-Si intermixing at the initial stage in order to accomplish supersaturation and the following *c*-Si nucleation for establishing chemical gradient. In the experiment, perhaps the sizes of Au NPs are so large that *a*-Si:H surrounding them has been depleted and left them isolated on the substrates, with no critical chemical gradient built up, nor the continuous supply of Si atoms.

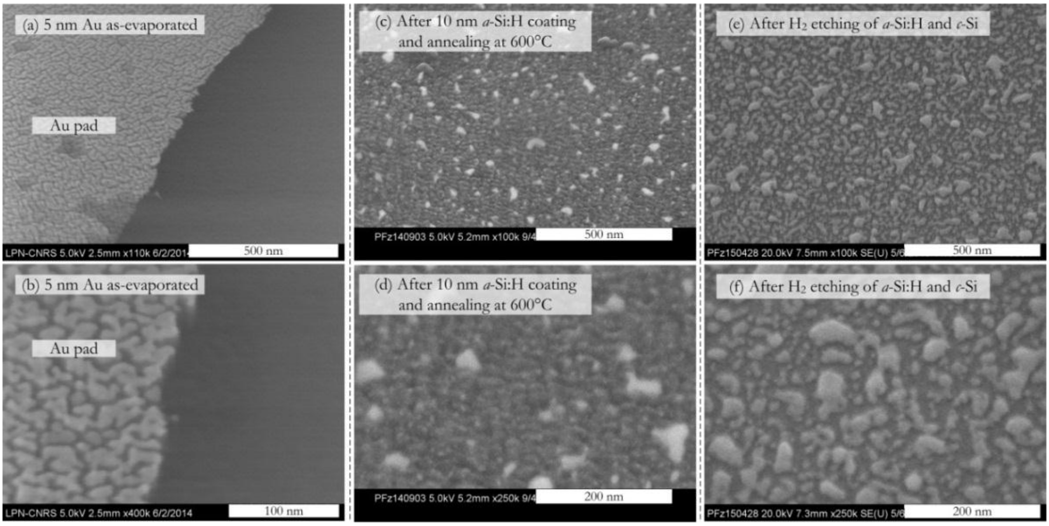

Figure 3.29 Interaction of *a*-Si:H/Au bilayer annealed at 600°C.

3.5.3 IN/*a*-GE:H INTERACTION

Indium thin films with nominal thicknesses of ~5 and ~50 on SiO_2 nm were treated by the same H_2 plasma treatment, 10 nm *a*-Ge:H coating and annealing at 350°C for the GeNWs growth. Note that this experiment was carried out in another PECVD system ARCAM, the setting temperature is considered as the real value, which is high enough for activating the growth of In-catalysed GeNWs. GeNWs can be rarely found from the sample of ~ 5 nm *a*-Ge:H/In bilayer structure, with morphology similar with the one observed for SiNWs grown from *a*-Si:H/Sn interaction (see Figure 3.28); and no GeNWs are found on ~ 50 nm *a*-Ge:H/In bilayer.

It is known that hydrogen effusion out of *a*-Ge:H starts at 200°C, compared with 300°C for *a*-Si:H [185]; also *a*-Ge crystallizes at lower temperatures (e.g. 250°C [185], 300-400°C [3]) than *a*-Si (600°C) [8]. Ellipsometry characterization tells that *a*-Ge:H did not crystallize after 1 hour, 350°C annealing, as shown in Figure 3.31. Anyhow, its structure might be relaxed, so less-reactive with liquid In for the GeNWs growth. The few-grown GeNWs probably took place during temperature raising period, since it takes time for substrate temperature arising from 150°C to 350°C. Therefore, lowering the annealing temperature is expected as a possible solution for the IPSLS GeNWs growth.

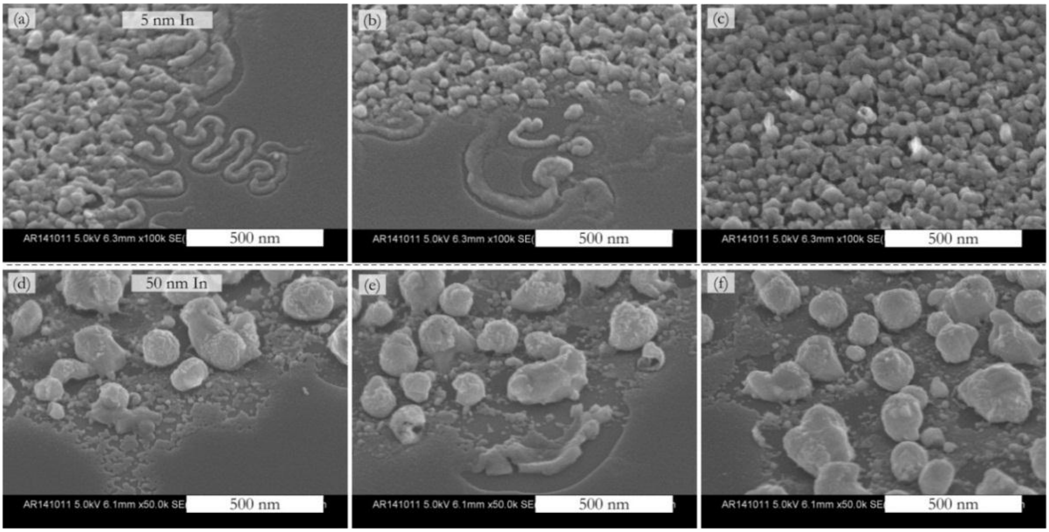

Figure 3.30 Interaction of *a*-Ge:H/In thin films treated with the same process carried out on *a*-Si:H/In bilayer structure.

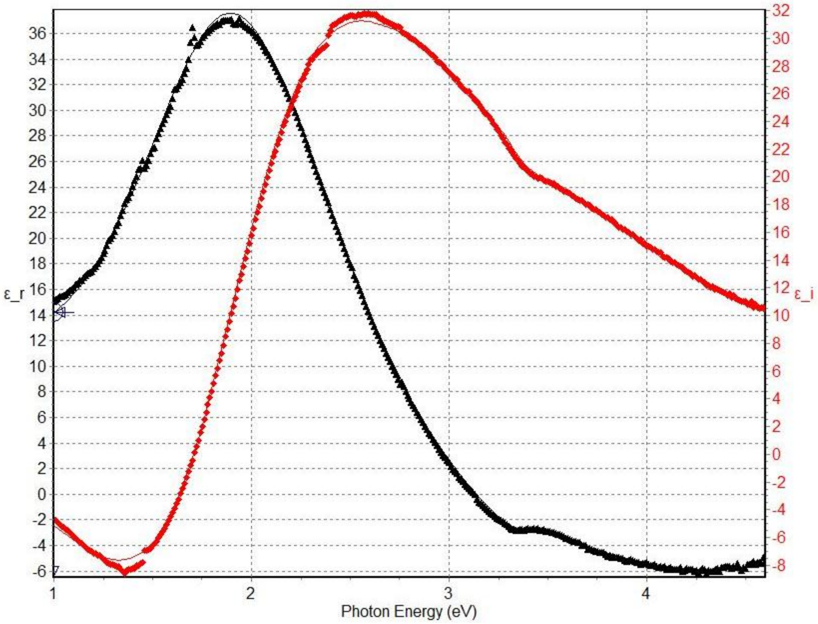

Figure 3.31 Fitting result of the pseudo-dielectric function in Tauc-Lorentz dispersion model for *a*-Ge:H deposited at 150°C on *c*-Si wafer and annealed at 350°C for 1h.

Table 3.3 Summary of metal catalyst-Si (or Ge) binary alloy phase diagrams

Binary alloy	**$T_{eutectic}$ (°C)**	**Composition $X_{Si, Ge}$, atomic fraction % at $T_{eutectic}$**	**Reference**
Si-Ga	30°C	6×10^{-10}	[186]
Si-In	157°C	4×10^{-10}	[137]
Si-Sn	232°C	5×10^{-5}	[187]
Si-Au	363°C	1.8×10	[188]
Ge-Ga	30°C	6×10^{-5}	[189]
Ge-In	157°C	7×10^{-4}	[190]
Ge-Sn	232°C	2.6×10^{-1}	[191]
Ge-Au	361°C	2.8×10	[192]

3.5.4 CONCLUSION

The above results show that indium is still the only metal that efficiently catalyses the growth of IPSLS SiNWs. Au/*a*-Si:H interaction leads to a MIC process of bilayer structure, which cannot produce a 1-D material. Sn/*a*-Si:H interaction can produce SiNWs, but with low yield and uncontrollable morphology. Moreover, the SiNWs growth mediated by Sn seems quite unstable. Reviewing the experiments with Au and Sn as metal catalyst, it seems to us the main mistake is the growth temperature was set at nominal 600°C (calibrated value=420°C), which probably activated the structure relaxation of *a*-Si:H. On the one hand, relaxed *a*-Si:H has lower Gibbs energy and therefore its Gibbs energy barrier for crystallization arises. This indicates that the metal catalysing effect at a certain temperature can be weakened. On the other hand, from the point of view of Si-In intermixing, it tends to be difficult to weaken and break the bonds in relaxed *a*-Si:H network, which can result in the failure of reactive spreading behaviour of liquid metals. These postulates are also applicable for explaining the failure of In/*a*-Ge:H interaction.

Figure 3.32 summarizes the composition $X_{Si\ (Ge)}$ of selected metal-Si (Ge) binary alloys at their eutectic points.The hydrogen effusion and crystallization temperatures are also indicated, respectively. Assuming that hydrogen effusion can induce the structural relaxation, it appears from this graph that there are not so many choices of metal catalyst for *a*-Ge:H (Ga and In), compared with *a*-Si:H (Ga, In, Sn, Au). However, the eutectic points of Au-Si and In-Ge are quite close to their respective H effusion temperature, further tests should be carried out.

Based on the above results, the uniqueness of indium for IPSLS growth mode appears to be its low melting point (same as Si-In eutectic point), which does not bring out significant modification of *a*-Si:H structural properties when forming liquid In-Si alloy. According to these results, Ga is expected to be another favourable catalyst for Si and Ge NWs growth. However this requires to deposit *a*-Si:H below Ga melting point (30°C). Furthermore, we suggest that this uniqueness is tightly correlated with the process of IPSLS growth mode, say, growing SiNWs (GeNWs) after Si (Ge) precursor deposition, which is discussed in the next section.

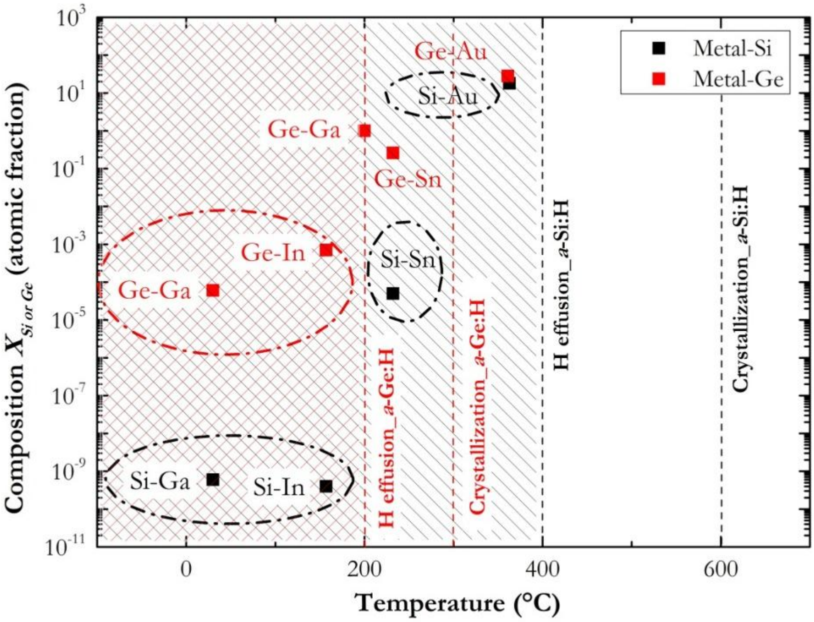

Figure 3.32 Summary of the composition $X_{Si\,(Ge)}$ of metal-Si (Ge) binary alloy at the eutectic and H effusion and solid-phase crystallization temperatures, respectively.

3.6 IPSLS VS. VLS GROWTH MODES

The IPSLS growth mode has been investigated and explained from the point of view of reactive spreading of liquid In on *a*-Si:H, which is supported by:

1) the metal-Si intermixing theory in the field of metal-amorphous Si interaction (i.e. MIC);

2) the theory of spontaneous motion of liquid drop on a solid surface with chemical potential gradient (i.e. surface energy gradient);

3) the heterogeneous nucleation theory when focusing the *c*-Si precipitation from liquid Si-In alloy.

In order to deepen our understanding of the IPSLS growth mode, we compare it with vapour-liquid-solid (VLS) growth mode [193]-[196]. Table 3.4 summaries the IPSLS and VLS growth modes.

Table 3.4 Summary of IPSLS vs VLS growth modes [197]-[201]. Note that M and S represent metal and semiconductor, respectively.

Growth mode	**IPSLS**	**VLS**
Driving force	**Supersaturation of M-S alloy**	
Phase of catalyst (M)	**Liquid**	
Catalyst candidates (M)	Only In (till now)	Many
Supply of precursor (S)	**Solid phase**	**Vapour phase**
	Before growth	**During growth**
Precursor candidates (S)	Only Si (till now)	IV, III-V, metal oxides, etc.
Growth direction	Lateral	Vertical
Growth temperature	Low (above 300°C)	High (aove 400°C)
Growth rate[10]	High (40 nm/s) [110]	Low (< 10 nm/s) [202]

Similarities exist in these two growth modes (in blue colour): (1) metal catalysts for mediating the growth are in liquid phase; (2) supersaturation in the M-S liquid alloys activates the semiconductor nucleation and crystal growth. Thereby, the physical and chemical events occurring at the M-S interfaces are similar. So the difference between the two growth modes derives from the supply manner of semiconductor precursors (in red colour).

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[10] For giving a general idea, we only use data of SiNWs grown in PECVD system, published from LPICM.

Figure 3.33 presents a comparison between VLS and IPSLS mode. Take SiNWs growth in a PECVD system for instance, as the nanowire growth results from the interaction between catalyst droplets and *a*-Si:H deposition (see Figure 3.33.a), we consider that different *a*-Si:H deposition conditions result in VLS or IPSLS growth mode. Misra *et al.* suggested that there exists a wetting layer of metal catalyst (Sn in their study) during the VLS growth of SiNWs [182]. As illustrated in Figure 3.33.b, the *a*-Si:H deposition has three basic routes: (1) directly on the metal droplet, (2) on the sidewall of SiNWs, (3) on the substrate. We suggest that the wetting behaviour is activated and maintained by the *a*-Si:H deposited on the sidewall of SiNWs. Furthermore, we assume that the tapering shape of SiNWs is caused by metal wetting layer induced crystallization of *a*-Si:H. Simply speaking, the morphology of a VLS grown NW results from a competition between axial and radial growth. Moreover, Schwartz *et al.* proposed that the stability of metal droplet/NW interface determines the NW growth behaviour via VLS method [203]. As shown in Figure 3.33.c, (1) stable droplet/NW interface leads a steady straight NW growth, while (2) kinking or (3) pinning effects are due to the fact that the catalyst droplets wet on higher surface energy edge. Yu *et al.* reported that long and straight VLS-grown vertical SiNWs are favoured by high substrate temperature and diluted silane in H_2 atmosphere [202]. In contrast, Rathi *et al.* achieved VLS-grown lateral epitaxial SiNWs by undiluted silane at low substrate temperature [184]. This is in agreement with our assumption that *a*-Si:H deposition conditions determine the NWs growth behaviour. Lateral SiNWs growth via VLS mode needs high surface energy at its initial pedestal edge (i.e. condition (3) in Figure 3.33.c), so the *a*-Si:H deposition on the substrate (i.e. route (3) in Figure 3.33.b) should be emphasized rather than other two deposition routes. So we suggest that IPSLS growth mode is a particular variant of VLS mode, where *a*-Si:H is deposited on the substrate before NW growth so that its high surface energy pins the catalyst droplets and realizes the lateral NW growth, as illustrated in Figure 3.33.d.

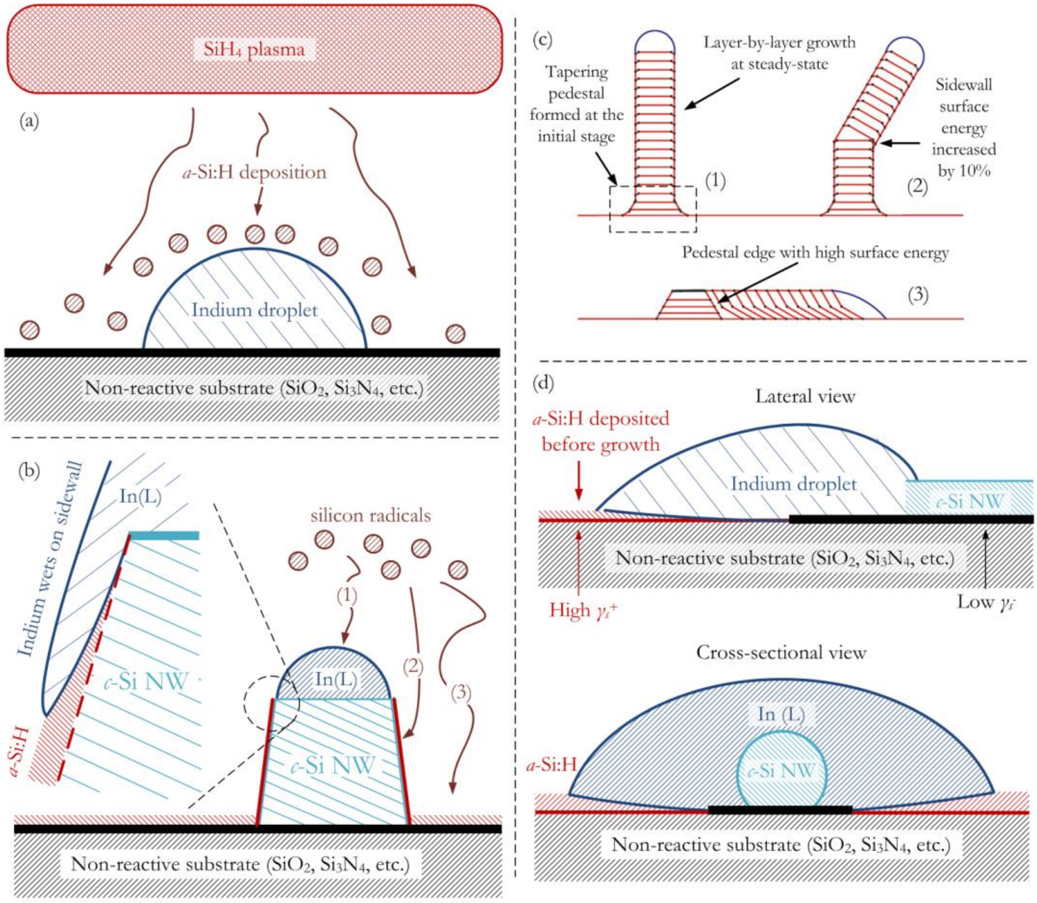

Figure 3.33 IPSLS mode vs VLS mode. (a) SiNWs growth in a PECVD system: interaction between indium catalyst and *a*-Si:H deposition, different *a*-Si:H deposition conditions result in VLS or IPSLS growth modes. (b) VLS grown vertical SiNW, during which silicon radicals are deposited directly on the indium droplet (1), on the NW sidewall (2), or on the substrate. (3) A wetting layer on the NW sidewall is reported [182], the *a*-Si:H deposited on NW sidewall is suggested to activate and maintain this wetting behaviour. (c) Simulation results of different NW growth behaviours via VLS method, indicating that (1) stable droplet/NW interface leads a steady straight NW growth, while (2) kinking or (3) pinning effects are due to the fact that the catalyst droplets wet on higher surface energy edge [203]. (d) IPSLS SiNW growth, where the *a*-Si:H is deposited before NW growth (i.e. during *a*-Si:H deposition indium catalyst is solid so that Si-In reaction is suppressed), which enables to pin the indium droplet on the substrate.

3.7 SUMMARY AND PERSPECTIVES

In this Chapter, the growth mechanism of in-plane solid-liquid-solid SiNWs has been explained from the viewpoint of spontaneous motion of liquid In NPs on *a*-Si:H. Liquid In reactively spreads on *a*-Si:H, transforms Si from amorphous to crystalline phase, thereby builds up a surface energy gradient from *a*-Si:H surface to low energy substrate surface. Driven by the unbalanced Young's force, the liquid In move forwards to the *a*-Si:H region. The SiNW growth contributes to maintain the surface energy gradient; reversely, it is also the products from the liquid In movement on *a*-Si:H.

SEM observations indicate that the movement of a liquid In NP on *a*-Si:H leaves a trail which can be divided into two parts with a constant ratio: the SiNW located in the center and at its two sides there is a wider trench with some residual *a*-Si:H. A possible reason is that the central region depleted of *a*-Si:H favours the precipitation of *c*-Si. Further geometric investigation and statistical analysis reveals that the liquid In reactive spreading behaviour can be enhanced by relatively thicker *a*-Si:H. The relationship between SiNWs diameter, *a*-Si:H thickness and In NP size has been quantitatively described.

As it is the *a*-Si:H layer that modifies the substrate surface and enables the liquid In movement, the structural properties of *a*-Si:H have been studied, in order to lower the growth temperature. From the atomic viewpoint, the growth of SiNWs is a series of processes: Si bond breaking in *a*-Si:H, In-Si intermixing and alloying and Si nucleation and crystal growth. Based on it, a simple strategy of lowering the *a*-Si:H deposition temperature is proposed to intentionally introduce extra disorder in the amorphous network so that the Si bonds are weakened and the Gibbs energy barrier of crystallization is lowered. The *a*-Si:H structural modification is demonstrated by Raman and spectroscopic ellipsometry measurement. By depositing *a*-Si:H at 120°C we could achieve SiNW growth at a nominal temperature of 350°C, compared with growth temperature of 450°C for *a*-Si:H deposited at 180°C.

To further understand the IPSLS growth mode, other metal catalysts (i.e. Sn and Au) and alternative solid precursor (*a*-Ge:H) are applied to grow NWs. However, none of them produced SiNWs. A possible reason for their failure is that the eutectic points of binary alloys (i.e. Si-Sn, Si-Au, and Ge-In) are quite near the respective hydrogen effusion temperature of *a*-Si:H or *a*-Ge:H, which is assumed as the boundary for NWs growth. Above this temperature, the amorphous network can get relaxed or even start to crystallize so that the interaction between liquid In and *a*-Si:H is impeded and so is the SiNWs growth. Indium is till now the most successful catalyst candidate as the eutectic temperature of In-Si alloy is far lower than the temperature for hydrogen effusion from *a*-Si:H. Based on this criteria (Figure 3.32), Ga and In are predicted as favorable candidates for GeNWs growth.

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4 SELF-ORGANISATION OF IN-PLANE SILICON NANOWIRES

CONTENTS

For practical use of semiconductor NWs in electronic applications such as sensors, piezotronics, photonics, photovoltaics, etc. [1], it is of prime importance to organize the large-scale 1-D semiconductors in a controllable way [2]. In this Chapter, a step-guided growth method is proposed for the large-scale organization of IPSLS SiNWs, based on the mechanisms of In NPs formation and IPSLS growth mode of SiNWs discussed in Chapters 2 and 3. First of all, previous endeavours on ordering the semiconductor NWs are summarized. Then a step-guided growth method is proposed to guide the liquid In movement on *a*-Si:H, based on solid surface energy engineering by nano-patterning the substrates. The large-scale self-organization of in-plane SiNWs is enabled by buried ITO/guiding-step matrix, thanks to the reproducible technique of In NPs formation on ITO sidewall. The fabrication process is introduced and several key points are discussed.

4.1 LARGE-SCALE ORDERED ONE-DIMENSIONAL SEMICONDUCTORS

A diversity of strategies for organizing large-scale one-dimensional semiconductor nanostructures (i.e. nanowires and carbon nanotubes) has been reported. As IPSLS SiNWs are grown via a bottom-up method, a brief review is firstly introduced on the methods of precisely localizing and aligning the NWs on the substrates. This can be achieved by positioning the 1-D semiconductors after this growth (named growth-and-place method) or during this growth (named growth-in-place method).

4.1.1 GROWTH-AND-PLACE METHOD

The growth-and-place method derives from the increasing motivation of assembling and integrating vertical VLS-grown NWs or CNTs in nano-scale electronics [3]-[7], especially in flexible electronics [8]-[11] due to its low-cost, low-temperature processing advantage [12].

The contact-printing technique is based on the transfer of semiconductor NWs or CNTs from their mother-substrates to foreign ones (e.g. flexible substrates) with pre-designed positions by nano-patterning [13]-[15] or even employing substrate surface functionalization for improving the alignment yield[16]. A similar technique is to press the vertical-grown 1-D semiconductors directly on their mother-substrates [17].

Electrical forces can also be used to realise the precise localization and alignment [18], assisted by surface chemical [19] and biological [20] functionalization, or thanks to the contribution of hydrodynamic forces, named dielectrophoresis assembly [21][22]. Fluid flow has also been reported to reorganise 1-D nanostructures [23][24].

In contrast to the above techniques, the suspension-based transfer technique is another way, which does not rely on external forces. Solutions with dispersed 1-D semiconductors (i.e. suspension) are spread on foreign substrates with pre-patterned and functionalized surfaces, and their self-assembly is facilitated by the surface chemical [25]-[27] or biological [28] interactions. Another interesting example is to incorporate 1-D semiconductors into blown bubble films and transfer them onto foreign substrates with alignment [29].

Figure 4.1 provides some examples of the growth-and-place method for organizing 1-D semiconductor nanostructures: (a) [14] and (b) [13] illustrate contact-printing techniques that transfer NWs or CNTs from their mother-substrates onto foreign (or transfer) substrates with pre-designed positions by nano-patterning; (c) [26] and (e) [7] illustrate the 1-D nanomaterials' suspension-based transfer techniques on foreign substrates with functionalized pattern for precise localization and alignment, and (d) [29] illustrates the method of nanomaterial-incorporated blown bubble films; (f) [18] illustrates the electrical field-assisted assembling method.

4.1.2 GROWTH-IN-PLACE METHOD

Besides the methodology of growth-and-place, the organization of 1-D semiconductor nanostructures can also be achieved during the growth step, named growth-in-place method. Here, we focus on works of the horizontally (or in-plane) guided growth of semiconductor NWs or CNTs, most of which relies on the epitaxial effect, no matter the growth mode is (e.g. VLS mode [30][31], IPSLS mode [32] and solution-based growth mode [33]). Nano-facets (i.e. atomic nano-steps) on the substrate surface reinforce the epitaxial guiding effect and thereby enhance the yield of the laterally guided growth [34], which is named graphoepitaxy [35]. This is till now the most successful method for various semiconductor NWs and CNTs grown on different flat or faceted planes of sapphire [36]-[40], quartz [41]-[43], SiC [44] and spinel (i.e. $MgAl_2O_4$) [45] substrates, and even integrated into circuits [46]. Besides the epitaxial guided growth, it is also reported that nanochannels can direct the VLS-grown SiNWs, by means of imposing the growth direction of SiNWs growing out of the template nanochannels [47]-[49]. Figure 4.2 provides examples of growth-in-place method: (a) [30] and (b) [32] show the epitaxial guided growth, (c) [35], (d) [38] and (e) [46] show the graphoepitaxial guided growth; (f) [49] shows the nanochannel-template-guided growth.

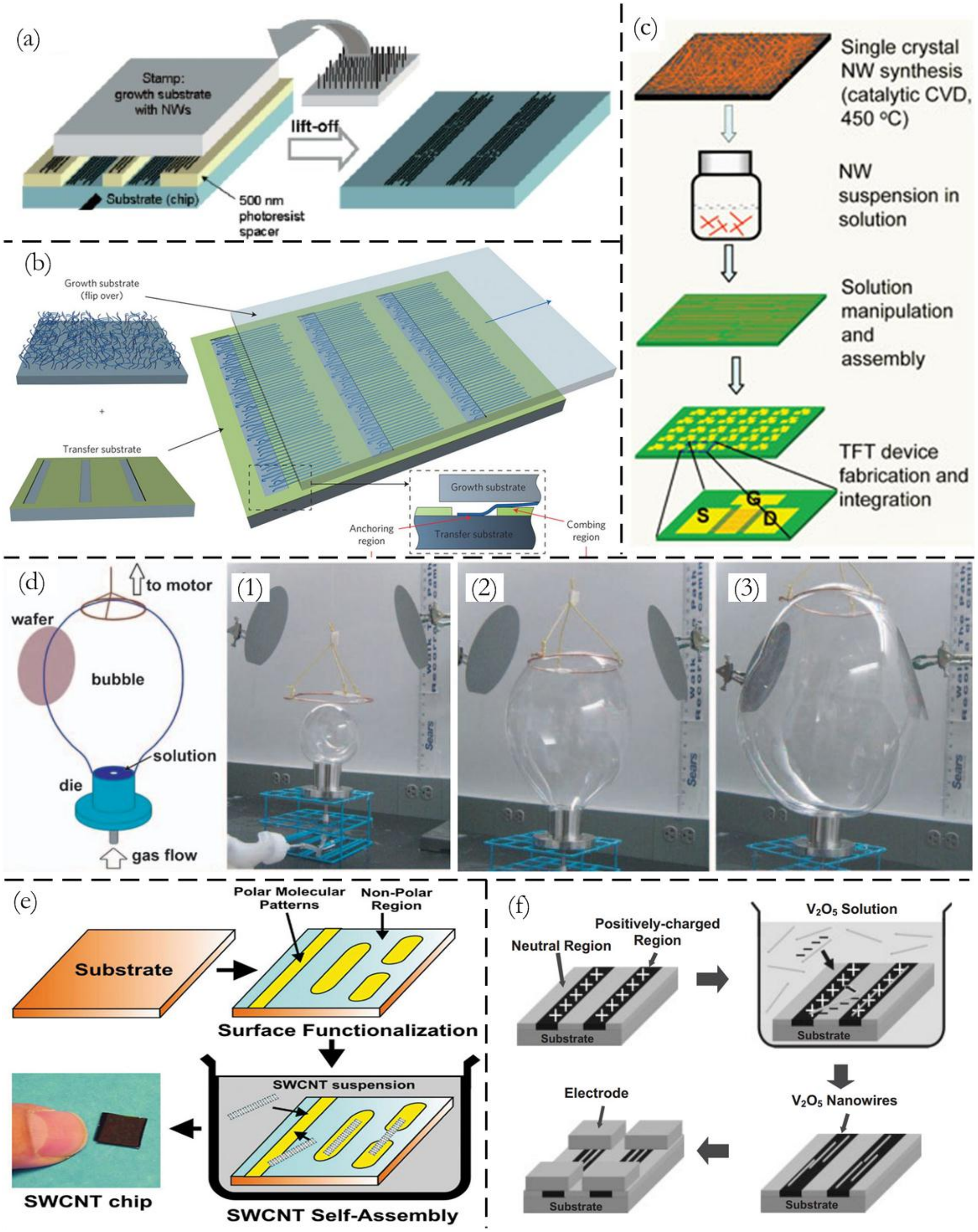

Figure 4.1 Examples of Growth-and-place techniques for organizing 1-D semiconductor nanostructures: (a) [14] and (b) [13]: contact-printing transfer method; (c) [26], (d) [29] and (e) [7]: solution-based transfer method; (f) [18] electrical field-assisted assembly.

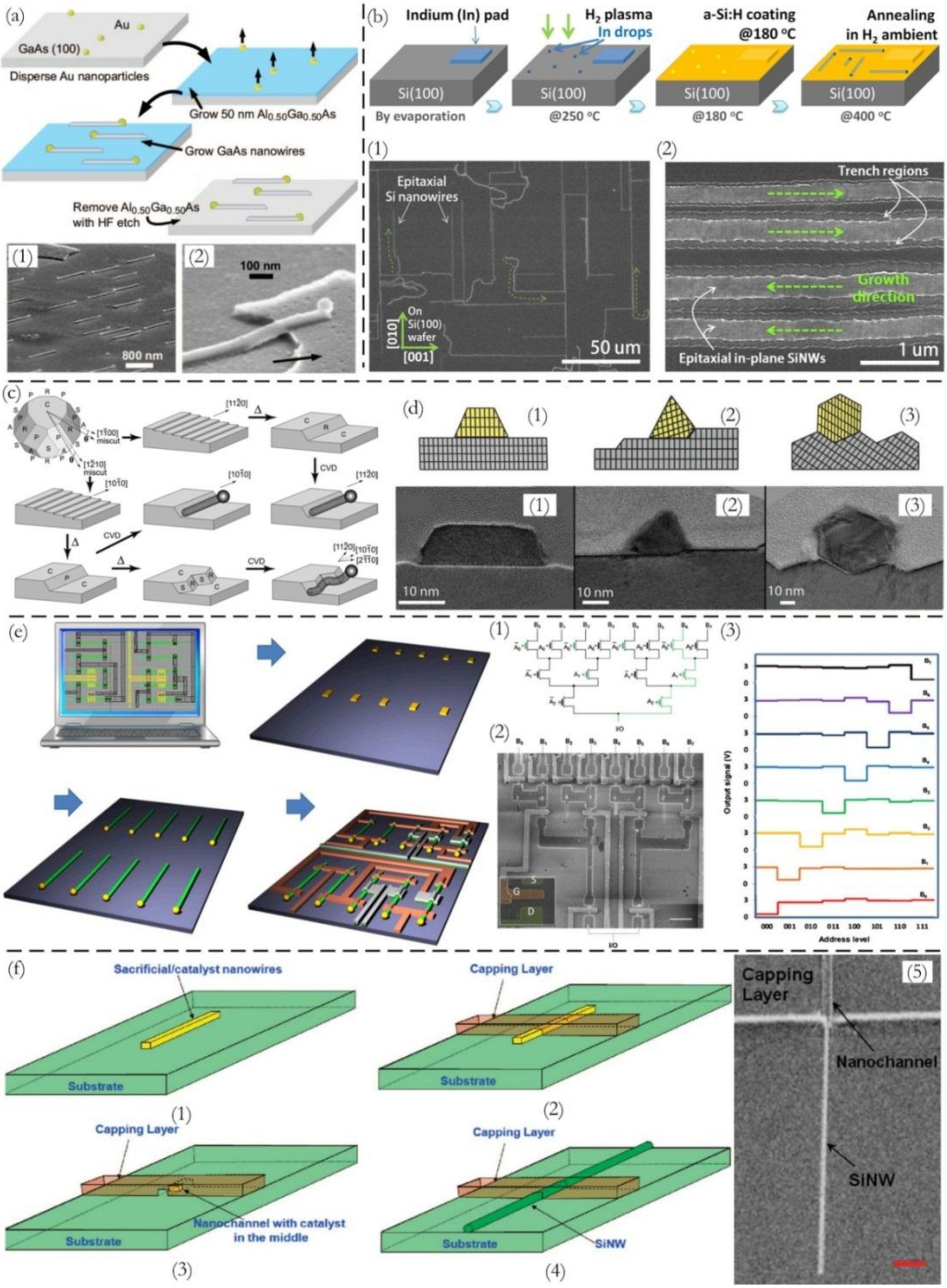

Figure 4.2 Examples of Growth-in-Place techniques: (a) [30] and (b) [32]: epitaxial guided growth; (c) [35], (d) [38] and (e) [46]: graphoepitaxial guided growth; (f) [49]: nanochannel-template-guided growth.

4.1.3 SUMMARY

As presented above, two types of strategies for organizing the bottom-up grown 1-D semiconductor nanostructures have been reviewed.

For the growth-and-place method, the grown nanostructures are transferred on foreign substrates with pre-patterned and/or functionalized areas for the localization and alignment. This can be achieved by external forces like contact-printing or electrical field, and also by solution-based transfer approaches with no need of external forces.

For the growth-in-place method, most of the strategies are based on lateral growth of graphoepitaxial NWs or CNTs. Besides the growth direction, the crystallographic orientations of NWs can also be controlled thanks to the epitaxial effect. It has been reported that a nano-faceted substrate favours the lateral VLS growth of SiNWs with increased miscut angles [34] (i.e. the angles of intersecting nano-facets, see Figure 4.2.c), thanks to the spreading behaviour of liquid Au-Si alloy on VLS-grown NWs [50]-[52] and trijunction stability in VLS system [53][54]. This lateral growth phenomenon has been theoretically studied by modelling and simulation [55][56], which indicates that the high edge energy (i.e. facet surface energy of the VLS-grown pedestal) prevents dewetting of the liquid catalyst drops and pins them on the substrate surface at the onset of the growth. Figure 4.3 shows the simulation results of different VLS growth behaviours by introducing excess surface energy perturbations [55].

However, as introduced in 4.1.2, the lateral epitaxial NWs can also be aligned with the crystallographic orientations on Si (100) surface free of nano-facets. Compared with randomly grown lateral NWs on substrate like SiO_2, the main contribution of epitaxial growth is that it is possible to deposit Si atoms from the supersaturated liquid Au-Ge [31] (or In-Si [32]) alloy onto the substrate surface in an ordered manner, so that the direction of the established surface energy gradient (see 3.2.3) is transferred from the crystallographic orientation, and the growth direction of NWs is determined, as illustrated in Figure 4.4. Thus, it is predicted that the failure of the guided growth is due to the failure of epitaxial growth.

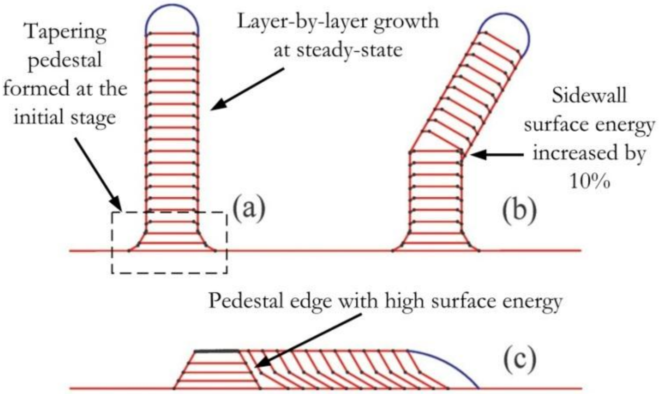

Figure 4.3 Simulation results of different NW growth behaviours by a model for a 12-fold crystal, the straight red lines represent the computed wire profiles at equal time intervals with the black dots indicating the facet edge positions. (a) Calculated straight wire, with a transition of an initial tapering pedestal shape to a steady-state shape; (b) kinked NW at the halfway of the steady-state by introducing a sidewall energy perturbation (increased by 10%) on the right side; (c) lateral growth by introducing an sufficiently high edge energy at the onset of growth, resulting in pining the catalyst droplets on the surface [55].

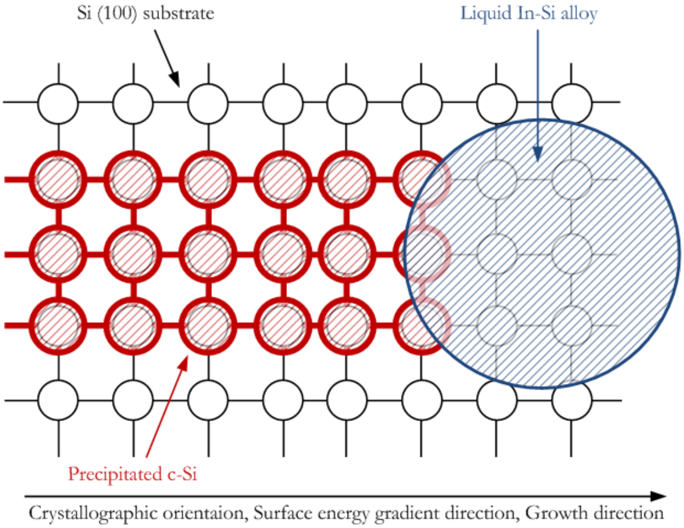

Figure 4.4 Illustration of self-assembled in-plane epitaxial SiNWs via IPSLS growth mode on Si (100) substrate.

4.2 SELF-ORGANIZATION OF IN-PLANE SINWS

In general, self-organization of IPSLS SiNWs involves two steps: (1) guiding the growth of SiNWs, and (2) positioning the In NPs at the place where we want the SiNWs start to grow. In this section, we discuss these two aspects in sequence.

4.2.1 STEP-GUIDED GROWTH OF IN-PLANE SINWS

A step-guided growth method for IPSLS SiNWs has been proposed in previous reports [57][58], which paves the way for organizing the IPSLS SiNWs in large scale. Figure 4.5 shows a typical step-guided IPSLS SiNW.

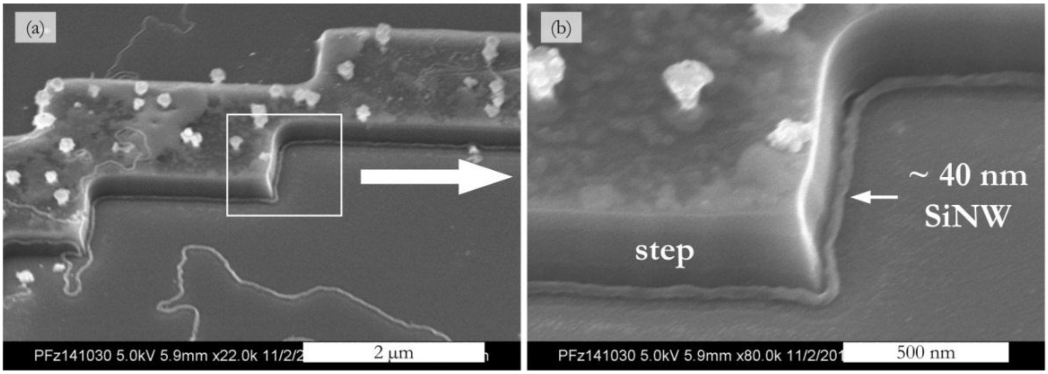

Figure 4.5 SEM images of a typical IPSLS SiNW via the step guided growth.

In order to understand and further improve the reproducibility of the step-guided growth, a theoretical assessment was carried on. In chapter 3, we concluded that the growth of IPSLS SiNWs can be viewed as the by-product of liquid In moving on *a*-Si:H based on reactive spreading on a substrate with surface energy gradient (or surface wettability gradient, see 3.2.3). Therefore, controlling the direction of SiNWs growth calls for the confinement of liquid In motion. According to the theories of liquid wetting on solid surfaces, both the heterogeneity of solid surfaces and the solid surface roughness can affect the liquid wetting or spreading behaviour [59]. Based on this, two possible strategies of surface wettability engineering are suggested, looking forward to control the liquid In movement on *a*-Si:H, which is discussed below.

4.2.1.1 MODIFICATION OF SUBSTRATE SURFACE CHEMISTRY

In order to control the motion of water droplets on solid surface, Dos Santos proposed a method that confines the aqueous droplets on a heterogeneous substrate surface with different surface energy [60]. The directed movement of the same droplet at three different times with an interval of 0.1 s is shown in Figure 4.6.a. One can see that the droplet runs on the hydrophilic surface track (light part), delimited by hydrophobic regions (shaded parts). The driving force of the droplet motion is the substrate surface energy gradient, as introduced in 3.1.2.

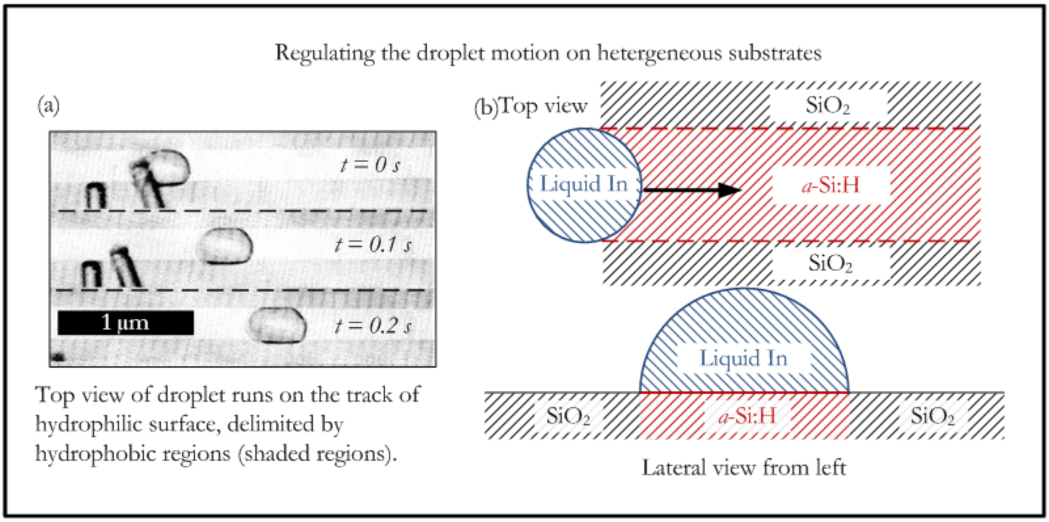

Figure 4.6 Controlling the droplet motion on heterogeneous substrates: (a) top view photographs of droplet running on the hydrophilic surface track, delimited by hydrophobic regions (shaded regions) [60]; (b) a similar guiding strategy of liquid In on heterogeneous surface (*a*-Si:H as indium-philic surface and SiO_2 as indium-phobic surface).

The idea of modifying the substrate surface chemistry is supposed to be universal for all kinds of spontaneous liquid motion on a solid surface. Figure 4.6.b illustrates a similar strategy for guiding the movement of liquid In on *a*-Si:H. However, defining the *a*-Si:H patterns is not easy: on the one hand, as the synthesis of IPSLS SiNWs is a one-pump down process (see 1.1), nano-patterning *a*-Si:H stripes, as shown in Figure 4.6.b, probably causes oxidation of *a*-Si:H as well as In NPs in some degree[11, 12]; on the other hand, the critical feature size by optical-lithography is ~1µm, which is one order of magnitude larger than the size of In NPs used for in-plane SiNWs growth (from tens to hundreds nm), so even though the *a*-Si:H stripes could be patterned with no oxidation, the small liquid In would randomly move on the broad *a*-Si:H stripes, resulting in the failure of the guiding movement.

In sum, controlling the droplet motion on chemically heterogeneous substrates is a straightforward way, and theoretically universal for most of liquid-solid pair. However, in the case of liquid In moving on *a*-Si:H, it has technical limitations.

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[11] The oxidation of *a*-Si:H is discussed in 1.2.5, as shown inTable 1.1 Fitting results of *a*-Si:H deposited on c-Si with native oxide after exposure to ambient air.

[12] The oxidation of indium is discussed in 2.3.2, and shown in shown in Figure 2.5 and Figure 2.15.

4.2.1.2 PATTERNING OF THE SUBSTRATE

Since SiNWs can grow along a guiding step, as shown in Figure 4.5, it is worth of investigating and assessing the reproducibility of this step-guiding effect.

As introduced in 4.1.3 and illustrated in Figure 4.3, simulations indicate that, in the VLS epitaxial growth of NWs, the wetting or dewetting behaviour of catalyst droplets on the NWs can be modulated by changing the surface energy of the sidewalls of NWs in the steady-state or at the onset of the growth, resulting in the kinking or surficial crawling phenomena, respectively.

Also, it has been studied extensively that, besides solid surface chemistry, the substrate morphology also affects the wettability [59]. In particular, the surface roughness provides additional liquid-solid interfacial area, and thus augments the surface energy [61]-[63], as illustrated in Figure 4.7.a [64][65]. Therefore the relationship between liquid-solid interfacial surface energy γ_{sl} and interfacial area A_{sl} can be expressed as:

$$\gamma_{sl} \propto A_{sl}. \tag{4-1}$$

Considering that the volume of liquid In does not vary on SiO_2 substrates with different morphologies, the liquid-solid contact radius on a flat surface $R_{sl(\pi)}$ and on a concave corner in angle of θ, $R_{sl(\theta)}$ (as shown in Figure 4.7.b) has the relationship:

$$1/2 \times 4/3\,\pi R_{sl(\pi)}^{3} = \theta/2\pi \times 4/3\,\pi R_{sl(\theta)}^{3}, \tag{4-2}$$

note that the flat surface can be considered as a concave with angle of π, and due to the chemical homogeneity of the solid surface [66], the curvature of the liquid In NP on the concave SiO_2 is a constant, and the contact angle is also around $\pi/2$ (see 3.2.1.1 in page 107). So the volume of the liquid In for a spherical cap spreading on a concave is in proportion of $\theta/2\pi$ to the spherical In NP with the same radius. By transforming (4-2), the liquid-solid contact radius as a function of θ is determined by:

$$R_{sl(\theta)} = \sqrt[3]{\pi/\theta}\; R_{sl(\pi)}, \tag{4-3}$$

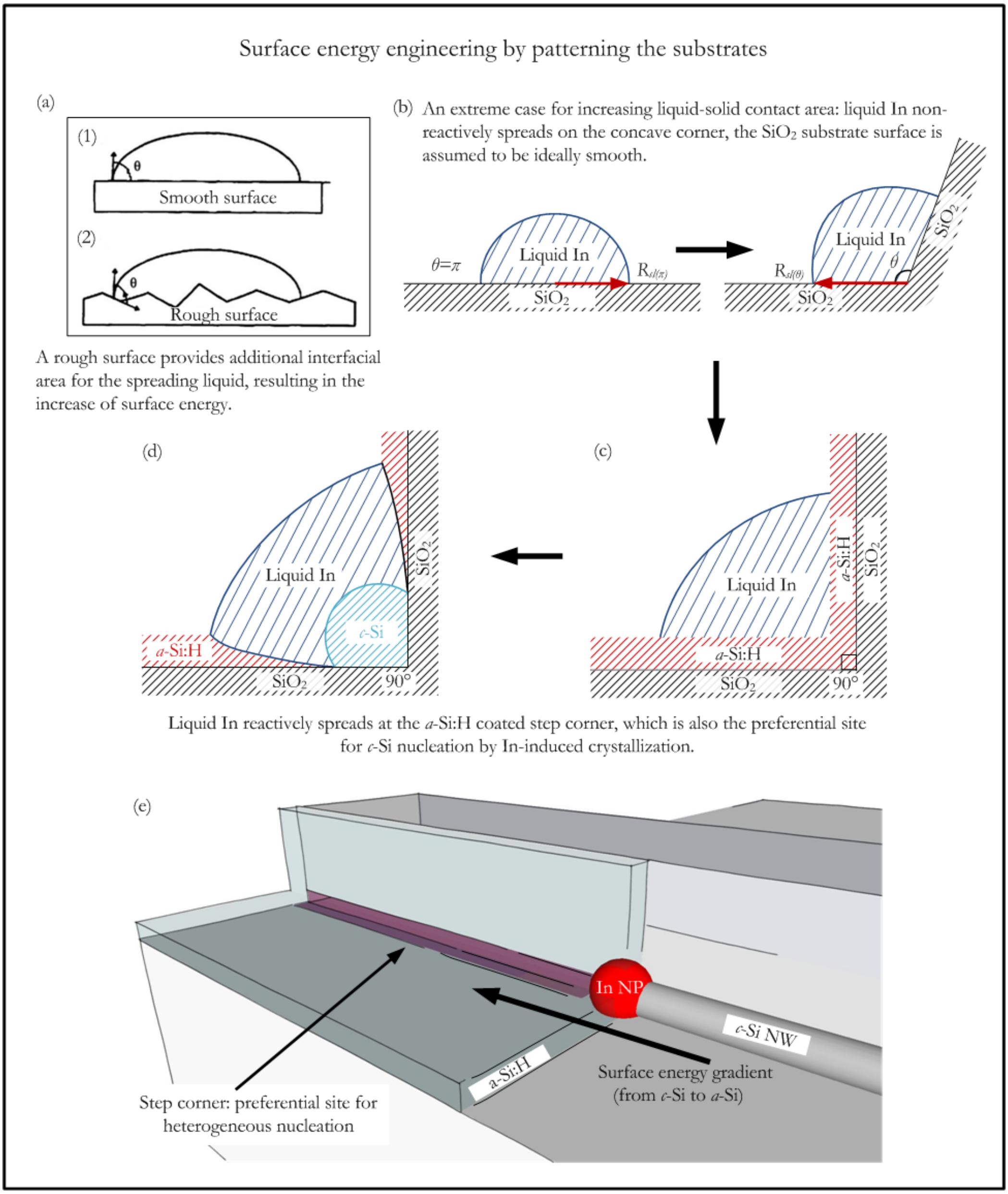
note that $R_{sl(\pi)}$ is determined by the liquid-solid wetting system, for liquid In spreading on SiO_2, it equals $1.26R_{s\text{-}NP}$, where $R_{s\text{-}NP}$ represents the liquid In in solid phase (see Figure 3.19). Thus the liquid-solid contact area in function of θ can be expressed by:

$$A_{sl(\theta)} = \pi R_{sl(\theta)}^{2} = (\pi/\theta)^{2/3}\pi R_{sl(\pi)}^{2}, \tag{4-4}$$

showing that $A_{sl(\theta)}$ increases monotonically with the decrease of concave angle θ, and so does the substrate surface energy. This indicates that the spreading effect of a liquid is more significant at a concave corner with a small angle. From a practical point of view, the angle will be limited by the fabrication techniques, 90° step being the most convenient one. Concave angles of less than 90° are not considered in this thesis.

Moreover, if the chemistry of step corner is modified by coating a layer of *a*-Si:H, the spreading effect of In will be further augmented, thanks to the In-*a*-Si:H chemical reaction. Figure 4.7.c and d illustrate this reactive spreading of liquid In at the *a*-Si:H coated step corner. Besides its benefit to the spreading effect, the step corner also provides a preferential site for *c*-Si nucleation and precipitation. This Si phase transition at the step corner is another critical factor that confines the moving liquid In along the step corner, driven by the same surface energy gradient mechanism mentioned in Chapter 3. The schematic representation is shown in Figure 4.7.e.

In sum, patterning the substrate surface is another efficient way for surface energy engineering, and easier to implement in comparison with the method of substrate chemistry modification. The discussion above also clarifies the mechanism of the step-guided growth of IPSLS SiNWs.



Surface energy engineering by patterning the substrates

A rough surface provides additional interfacial area for the spreading liquid, resulting in the increase of surface energy.

An extreme case for increasing liquid-solid contact area: liquid In non-reactively spreads on the concave corner, the SiO_2 substrate surface is assumed to be ideally smooth.

Liquid In reactively spreads at the *a*-Si:H coated step corner, which is also the preferential site for *c*-Si nucleation by In-induced crystallization.

Step corner: preferential site for heterogeneous nucleation

Surface energy gradient (from *c*-Si to *a*-Si)

Figure 4.7 Surface energy engineering via patterning the substrate surface: (a) a rough surface provides additional interfacial area for the spreading liquid, resulting in the increase of surface energy; (b) liquid In non-reactively spreads on the concave corner with an angle θ is an extreme case of increasing the liquid-solid contact area, supposed that the SiO_2 surface is ideally smooth. The calculations indicate that the liquid-solid contact area increases monotonically with the decrease of angle θ, liquid In on a perpendicular step corner (90°) has the largest contact area, resulting in the most significant surface energy enhancement. Note that limited by the fabrication techniques, angles smaller than 90° are not considered. (c, d) for a 90° step with the largest available surface energy, after coating with an *a*-Si:H layer, the reactive spreading effect of liquid In on the step corner is furthermore augmented, and the step corner is also probably the preferential site for *c*-Si nucleation and precipitation. (e) schematic representation of guided growth of a SiNW along the step corner: high surface energy at the guiding step corner pins the liquid In NP, facilitates the Si heterogeneous nucleation and crystal growth, and enables the surface energy gradient to build up right along the step corner (from *c*-Si to *a*-Si).

4.2.1.3 THE STABILITY OF STEP-GUIDED GROWTH IN THE IPSLS SYSTEM

Xu *et al.* [67] recently proposed an operating principle of step-guided growth of IPSLS SiNWs. An analytical model was established based on the calculation of the total surface Gibbs energy in the solid-liquid-solid system, which was also supported by experimental statistical analysis. They consider that for a successful step-guided growth of in-plane SiNWs, the sizes of liquid In NPs (which determines the diameter of SiNWs, see 3.3.2) should be compatible with the height of the guiding step edges. The NPs out of the size range failed to be pinned along the step corner.

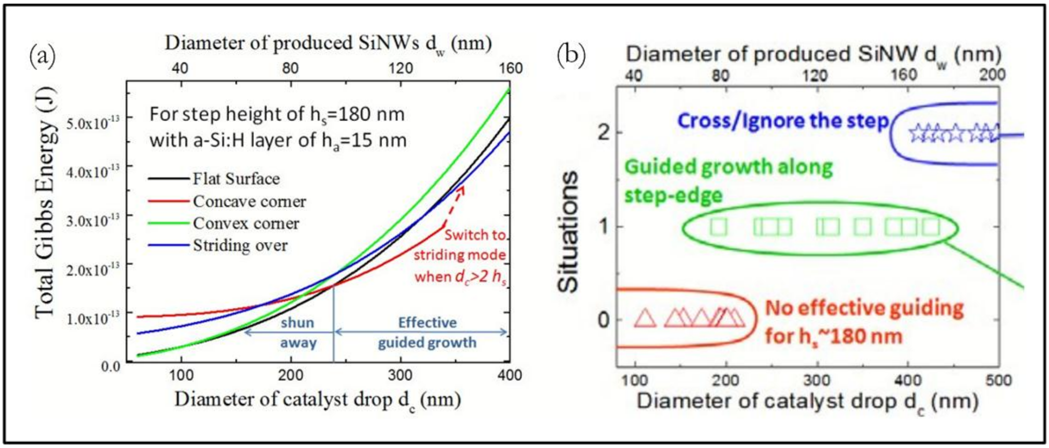


Figure 4.8 Operating principle of step-guided growth: (a) plotting of total Gibbs energy calculation under different liquid-solid system configurations based on an analytical model (i.e. liquid In on flat surface, concave corner, convex corner and striding over); (b) experimental statistics of the guiding effect under different configurations in liquid-solid system [67].

However, as shown in Figure 4.5, the growth of SiNWs with diameter of ~40 nm can be guided along the ~250 nm high step with less than 10 nm *a*-Si:H coating layer, which is out of the range in Figure 4.8.b. This implies that the guided growth is still effective for *high step-small In NP* system. Thus, it is worth reconsidering the stability of this step-guided growth strategy.

As elaborated in 4.2.1.2 and illustrated in Figure 4.7, the pinning effect of liquid In at the guiding-step corner is caused by the introduction of a new solid surface (i.e. the guiding-step edge) in the SLS system, and thereby increasing the liquid-solid contact area

A_{sl} and the interfacial energy γ_{sl}. Hence, for all the liquid In wetting behaviours on high step edges, the liquid-solid contact area A_{sl} is uniquely determined by the size of liquid In NP, the height of the guiding-step can only affect the situations when liquid In NPs are large enough to spread on the top surface of the step. Figure 4.9 illustrates the evolution of the liquid In spreading and wetting behaviour on different SLS configurations: the guiding step in infinite height (a) keeps being lowered (b and c) and finally degenerates to a flat solid surface (d), during which the liquid In starts to spread and wet on the top surface of guiding step. The red lines represent the liquid-solid contact lines. Even though the contact area is difficult to be determined mathematically till now, it is expected that the configuration (a) has the largest contact area and thereby provides the greatest liquid-solid energy. Thus, a step higher than the size of liquid In NP is the most stable configuration for the guided growth. Thereby, the dominant factor that affects the stability of step guided growth turns to be the thickness of *a*-Si:H. Figure 4.7.d illustrates that, besides its pinning effect to liquid In, the step corner also facilitates the heterogeneous nucleation and crystal growth of Si, therefore a surface energy gradient can be established along it (from *c*-Si to *a*-Si:H). If the *a*-Si:H coating at the corner is not conformal, liquid indium tends to spread on relatively thicker *a*-Si:H on planar substrate rather than on sidewall of guiding step (as shown in Figure 3.19), as shown in Figure 4.9.f. Figure 4.10 shows a failure example of step-guided growth: an In NPs of ~50 nm moves along a ~150 nm guiding step with a non-conformal *a*-Si:H coating layer[13] of ~20 nm, resulting in the failure of step-guided growth. Thus, it is postulated that conformal *a*-Si:H of a moderate thickness plays a key role for stabilizing this step-guided growth strategy, as shown in Figure 4.9.e.

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[13] The unconformality of *a*-Si:H deposited in the PECVD system (Plasfil) is confirmed by SEM, see Figure 3.8.e.

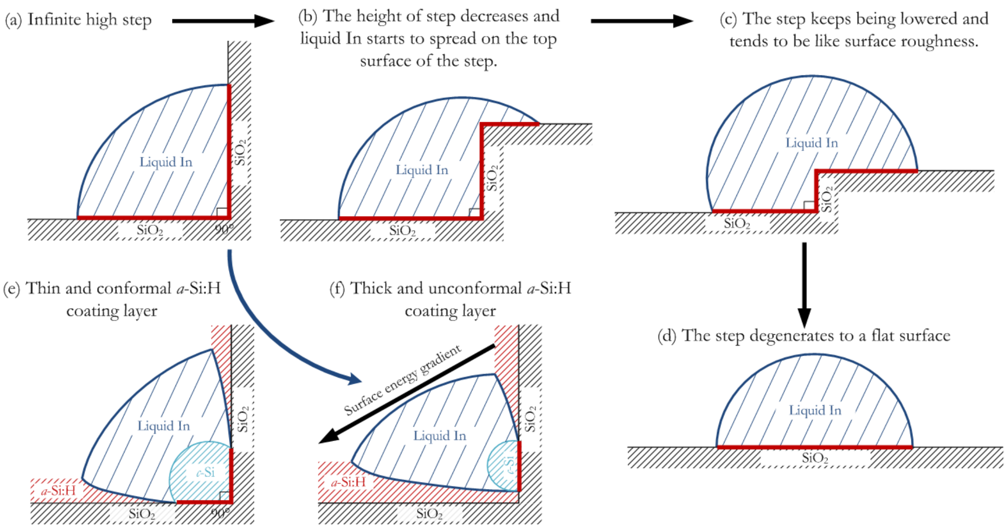


Figure 4.9 Evolution of the liquid indium spreading and wetting behaviour on different SLS configurations: (a) liquid wets the corner of step in infinite height; (b) liquid In starts to wet the top surface of the step with decreased height; (c) the step tends to be like surface roughness as it keeps being lowered; (d) the step degenerates to a flat surface; (e) thin and non-conformal *a*-Si:H coating layer at the step corner is fully depleted by liquid In, succeeding the guided growth along the corner; (f) thick and uncomformal *a*-Si:H coating layer at the step corner is partially depleted by liquid In, moreover a surface energy gradient is built up between the *a*-Si:H on planar substrate and the relatively thinner one on the sidewall of guiding step, resulting in the failure of guided growth.

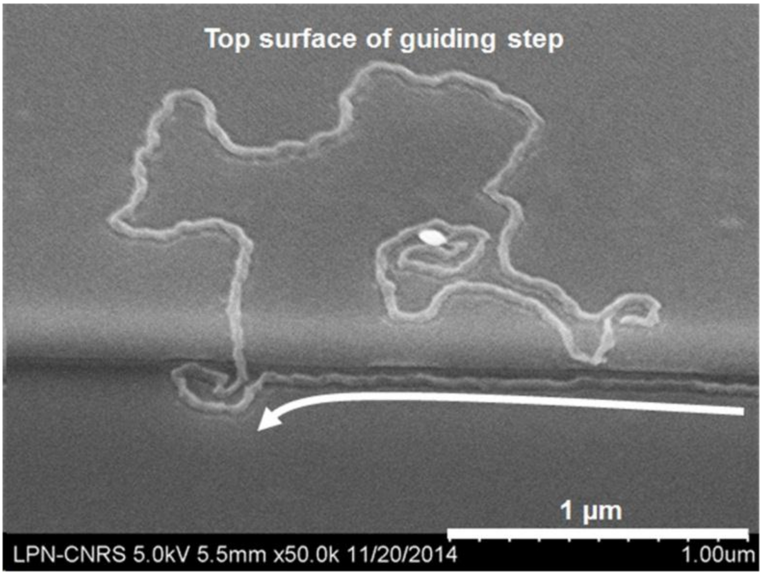


Figure 4.10 SEM image of a ~ 50 nm In NP moving along a ~150 nm guiding step with an non-conformal *a*-Si:H coating layer of ~20 nm, resulting in the failure of guided growth of in-plane silicon nanowires.

4.2.2 POSITIONING INDIUM NANOPARTICLES ON SIDEWALLS OF BURIED ITO MATRIX

After elaborating the strategy for directing the growth of SiNWs, another challenge is proposed and discussed: the way of precisely localizing the step-guided SiNWs. As reviewed in 4.1.2, previous works rely on electron-beam lithography to pattern and position the metal catalysts at places, where the NWs start to grow. Here, we propose an *ITO/guiding step* matrix for positioning the In NPs, as shown in Figure 4.11. A novel method is developed for reproducibly forming In NPs on buried ITO sidewall, see inset image (a); afterwards the growth of SiNWs can be guided along the step corner, see inset image (b).

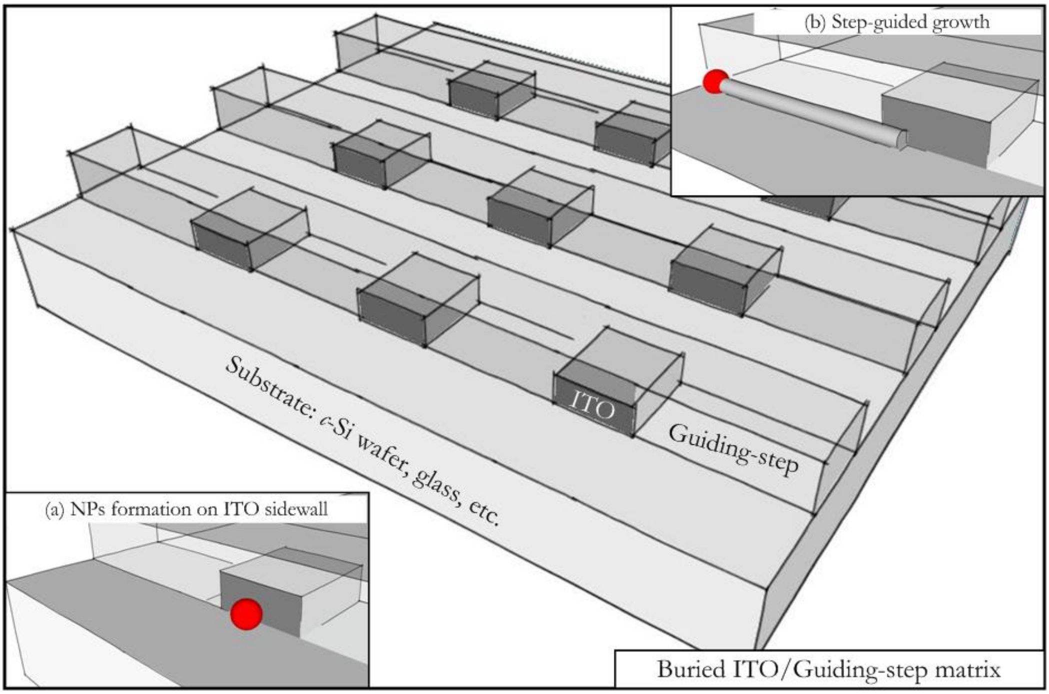


Figure 4.11 Strategy of positioning the In NP by fabricating *ITO/guiding steps* matrix. (a) In NPs are formed on the ITO sidewall via a H_2 plasma treatment and afterwards (b) the growth of SiNWs can be guided along the step corner.

Figure 4.12 shows examples of an In NP formed on buried ITO sidewall (see SEM images a and b), and of a step-guided IPSLS SiNW (see SEM image e), with its starting point at ITO sidewall (see image d) and its ending point at the guiding step corner (see image c).

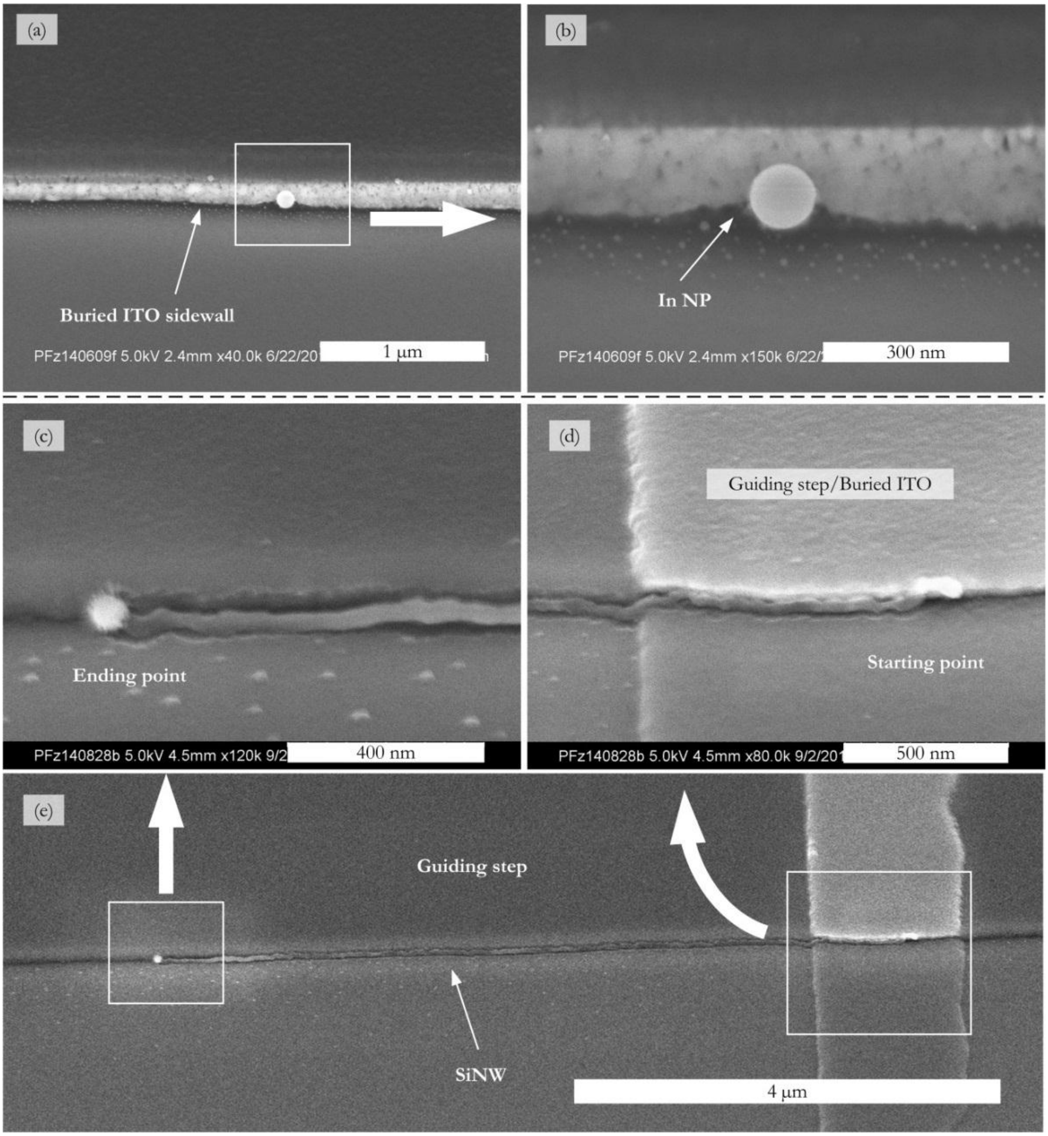


Figure 4.12 Example of an In NP formed on ITO sidewall (a, b) and the step-guided growth of an IPSLS SiNW (c, d, e).

The choice of ITO rather than an evaporated In thin film for the sidewall In NPs formation will be detailed in 4.3.2.1. Simply speaking, it is more practical to fabricate sharp and continuous buried ITO sidewall by conventional dry etching technologies. However, In NPs formation on the sidewall of buried ITO layer encounters similar difficulties with the condition on planar ITO surface (i.e. size and density control, see 2.4.5).

In contrast with a planar ITO surface which is completely exposed to H_2 plasma, it needs sufficient reactive H species (i.e. radicals and ions) to approach the sidewall of buried ITO layer with the guiding step (as a barrier against H_2 plasma) coating on it. Figure 4.13 illustrates the various H_2 plasma processes on planar ITO surface and sidewall of buried ITO layer with a plasma barrier coating on it. To achieve the sufficient H_2 plasma reduction of the ITO sidewall, two main pathways are proposed, as detailed in the figure: (1) hydrogen radicals directly diffuse onto the ITO sidewall; (2) hydrogen ions impinging on the surface are reflected as fast neutrals onto the ITO sidewall due to strong ion bombardment.

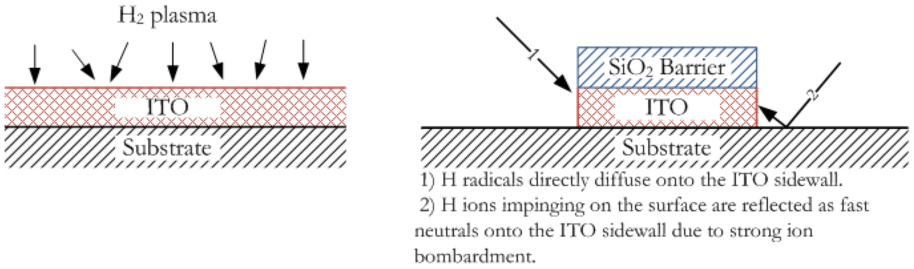


Figure 4.13 Illustration of different H_2 plasma processes on planar ITO surface (left) and sidewall of buried ITO layer with a H_2 plasma barrier (SiO_2) coating on it. Three pathways make possible the ITO reduction, as detailed in the figure.

It is known that (1) low RF power with high gas pressure promotes the isotropy of plasma; in contrast, (2) high RF power with high gas pressure enhances the plasma density; (3) high RF power facilitates hydrogen ion bombardment while it weakens the isotropy of plasma; and (4) high substrate temperature favours high surface mobility of H radicals. Table 4.1 lists the effects of parameters on the H_2 plasma and the reduction of ITO. Take RF power for example, high RF power enhances the density plasma (denoted as "↑"), while weakens the plasma isotropy (denoted as "↓"). "–" means for the moment there is no significant relationship in the range of our knowledge.

Table 4.1 Effects of parameters on the H_2 plasma and its reduction to ITO

PLASMA	DENSITY	ISOTROPY	H-O REACTION
RF POWER	↑	↓	↑
GAS PRESSURE	↑	↑	↑
TEMPERATURE	–	–	↑
DURATION	–	–	↑

In order to optimize the H_2 plasma treatment for the reproducible sidewall In NPs formation, different parameter configurations (i.e. H_2 pressure, RF power, exposure duration, and substrate temperature) were tested, as shown in Figure 4.14, Figure 4.15 and Figure 4.16, and detailed in the legends. However, only tiny NPs can be formed; these efforts seem to bring about few improvement of forming In NPs with typical size for the SiNWs growth.

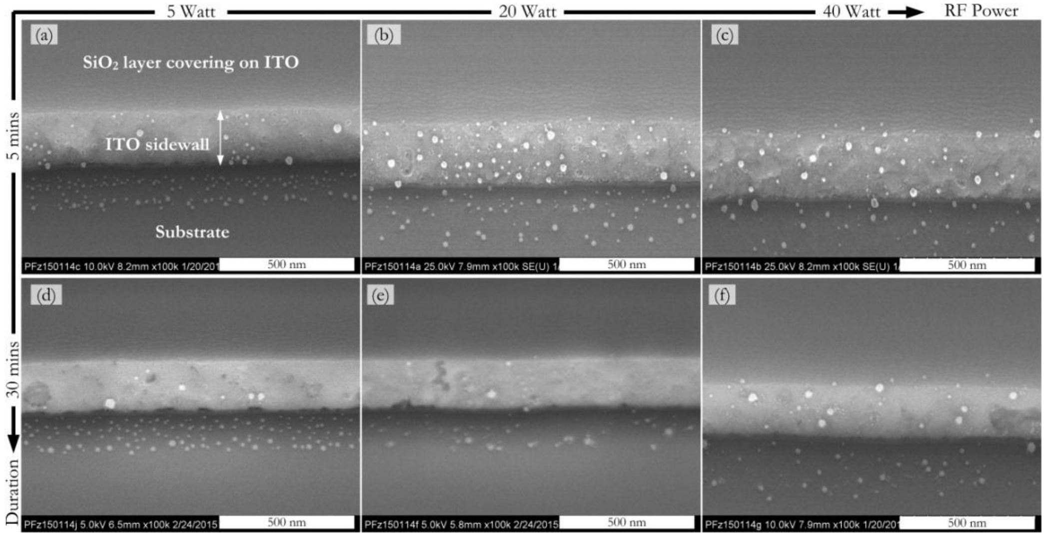


Figure 4.14 In NPs formation on the sidewall of buried ITO layer beneath guiding step, with different (RF power, exposure duration) groups. H_2 flow rate is in 100 sccm, 400 mTorr, and substrate temperature is 350°C.

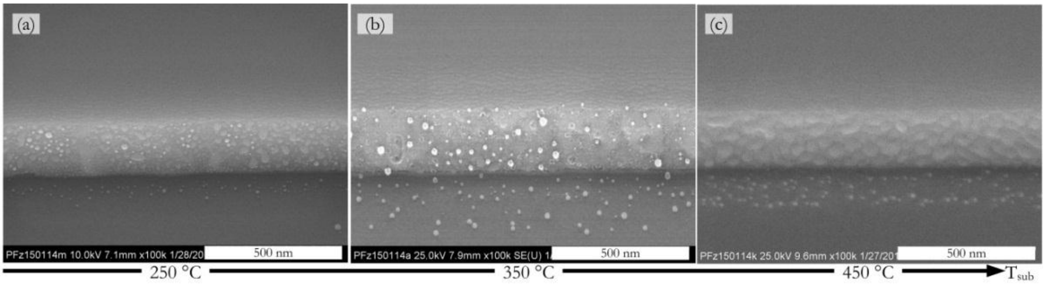


Figure 4.15 In NPs formation on the sidewall of buried ITO layer beneath guiding step at different substrate temperatures, with 100 sccm, 400 mTorr, 20 Watt H_2 plasma.

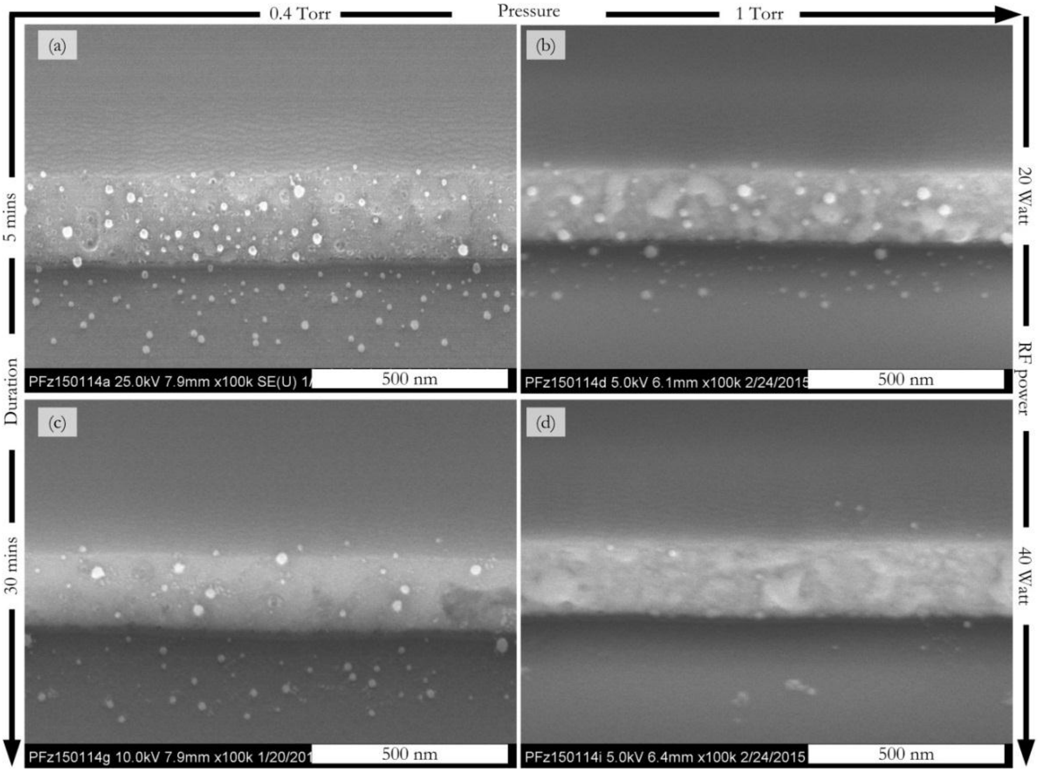


Figure 4.16 In NPs formation on the sidewall of buried ITO layer beneath guiding step, with different (RF power, exposure duration, H_2 pressure) groups. H_2 gas is in 100 sccm, and substrate temperature is 350°C.

As modulating H_2 plasma parameters does not help forming In NPs on the ITO sidewall, the efforts should be focused on the ITO sidewall surface chemistry.

In 3.2.1.1, *a*-Si:H is demonstrated to modify the substrate chemistry and In NPs reactively spread and coalesce into larger ones. Figure 4.17 shows the SEM images of small In NPs formed on the sidewall of buried ITO layer exposed to 100 sccm, 400 mTorr H_2 plasma with a RF power of 20 Watts and at substrate temperature at 300°C for 5 mins (see image a), and their evolution after 20 nm *a*-Si:H coating at 150°C and annealing at 450°C for 10 mins (see image b). No significant coalescence of small In NPs is observed by coating *a*-Si:H thin film on the sidewall. The enlargement of the In NPs is probably due to the *a*-Si:H coating. A possible explanation is that the *a*-Si:H shell coating on the small In NPs is so thick that it impedes the spreading and following coalescing behaviours. Moreover, the density of small In NPs (see image a) is relatively small in comparison with discontinuous evaporated In thin film (i.e. In islands), so it is expected that even if the spreading of small In NPs is achieved by adjusting the thickness of *a*-Si:H, the coalescence is still difficult to take place.

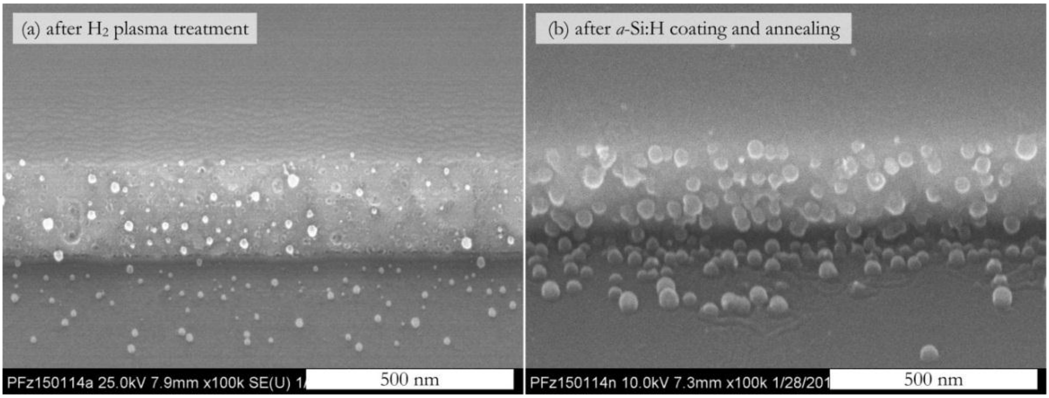


Figure 4.17 Tests to redistribute In NPs formed on the sidewall of buried ITO layer by H_2 plasma treatment (100 sccm, 400 mTorr of H_2, 20 Watts, at 300 °C for 5 mins) (a) by coating 20 nm *a*-Si:H and annealing at 450°C for 10 mins (b).

In 2.4.1.3, a nucleating-growing-coalescing mechanism was proposed to describe the In NPs formation on planar ITO surface. Apparently, for the case of ITO sidewall, In atoms are released and nucleate into small drops, however it seems that these small In drops do not coalesce. A possible reason is that they cannot grow larger in order to connect each other, which might be limited by the small area of the sidewall surface. However, a successful case has been shown in Figure 4.12.a and b. It reflects that the geometry of the sidewall surface is not the limiting factor.

TEM observations reveal a phase transition of RT-sputtered ITO from amorphous to polycrystalline states by post-deposition annealing (see Figure 2.24 in page 80). Moreover, it is found that the density of In NPs formed on ITO deposited at 350°C (supposed to be polycrystalline) is low and the sizes are larger, in comparison with the ones formed on RT-sputtered ITO (see Figure 2.25 in page 82). It is expected that this phase transition can help to form larger In NPs on ITO sidewall. Therefore, we anneal the buried ITO layer at 400°C for 30 mins before H_2 plasma treatment. Figure 4.19 and Figure 4.20 compare the In NPs formation on the sidewall of buried ITO layer with and without post-annealing. The thickness of buried ITO layer is 100 and 200 nm, respectively. The post-annealing is demonstrated to make the In NPs formation efficient and reproducible.

The grain boundary wetting theory (see 2.3.4.3) is considered to explain this phenomenon. The polycrystalline ITO thin films have columnar structure after thermal annealing, the joints of the *c*-ITO columns (i.e. grain boundaries) act as sinks to collect the liquid In, due to their high surface energy.

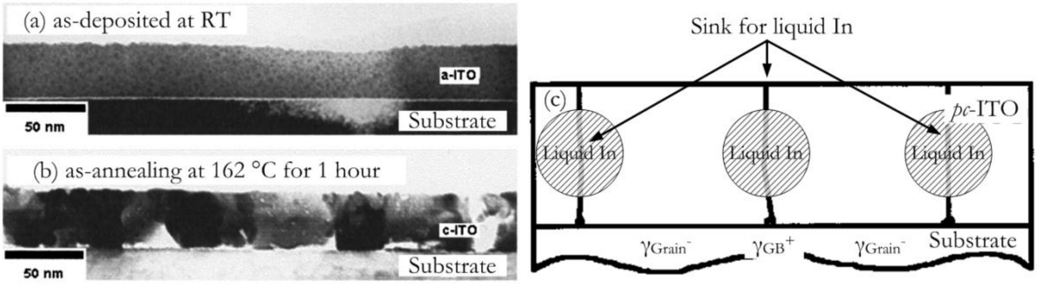


Figure 4.18 Schematic representation of In NPs formation on the sidewall of polycrystalline ITO: (a) and (b) show the cross-sectional TEM images of as-deposited ITO at RT and after annealing at 162 °C for 1 hour, respectively [68]; (c) illustration of high surface energy *pc*-ITO grain boundaries acting as sinks for collecting liquid In, the schematic of *pc*-ITO is from Cleva W. Ow-yang *et al*. [69].

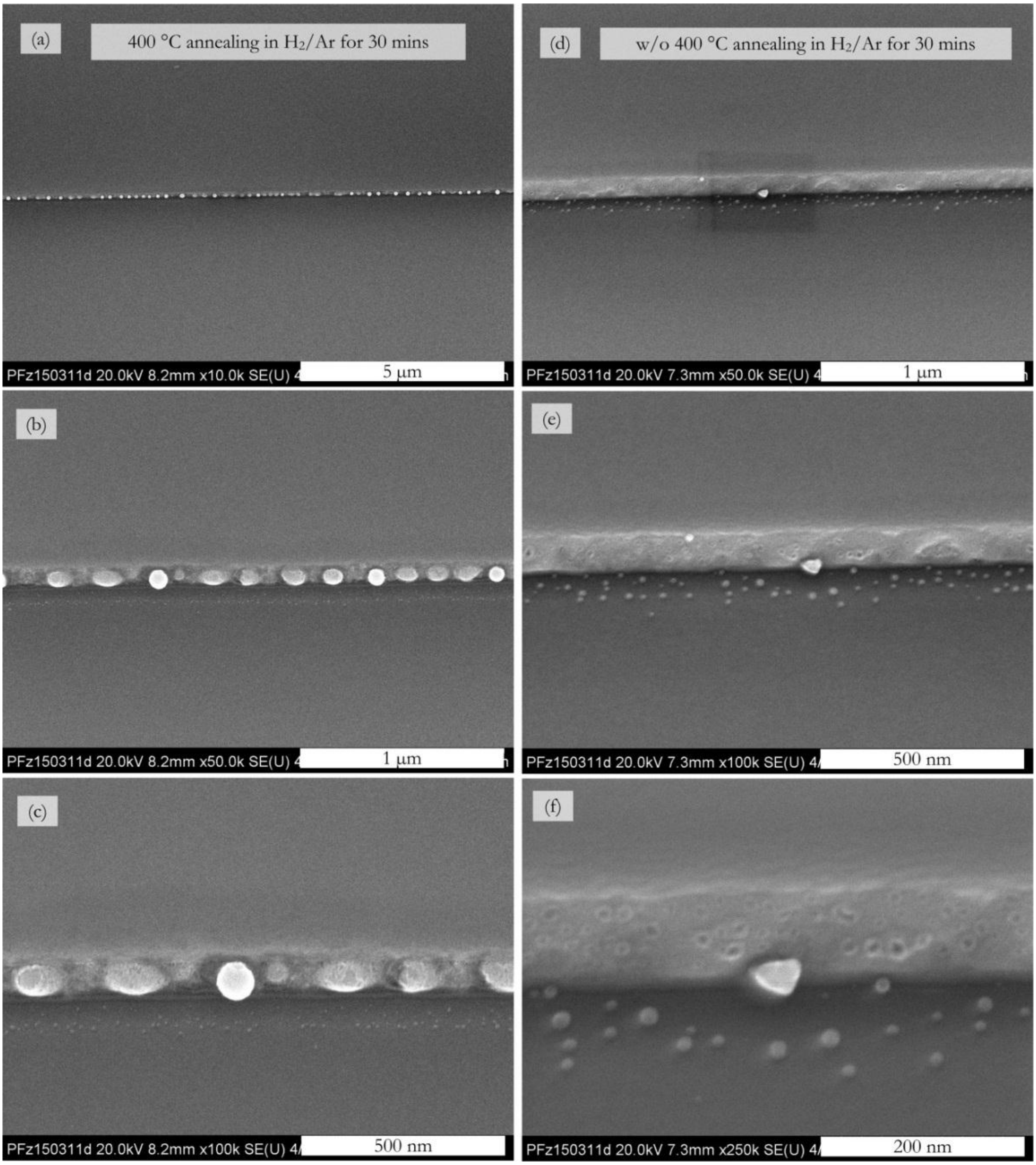


Figure 4.19 Comparison of In NPs formation on the sidewall of buried RT-deposited ITO layer with (a, b, c) and without post-annealing (d, e, f). The thickness of buried ITO layer is 100 nm.

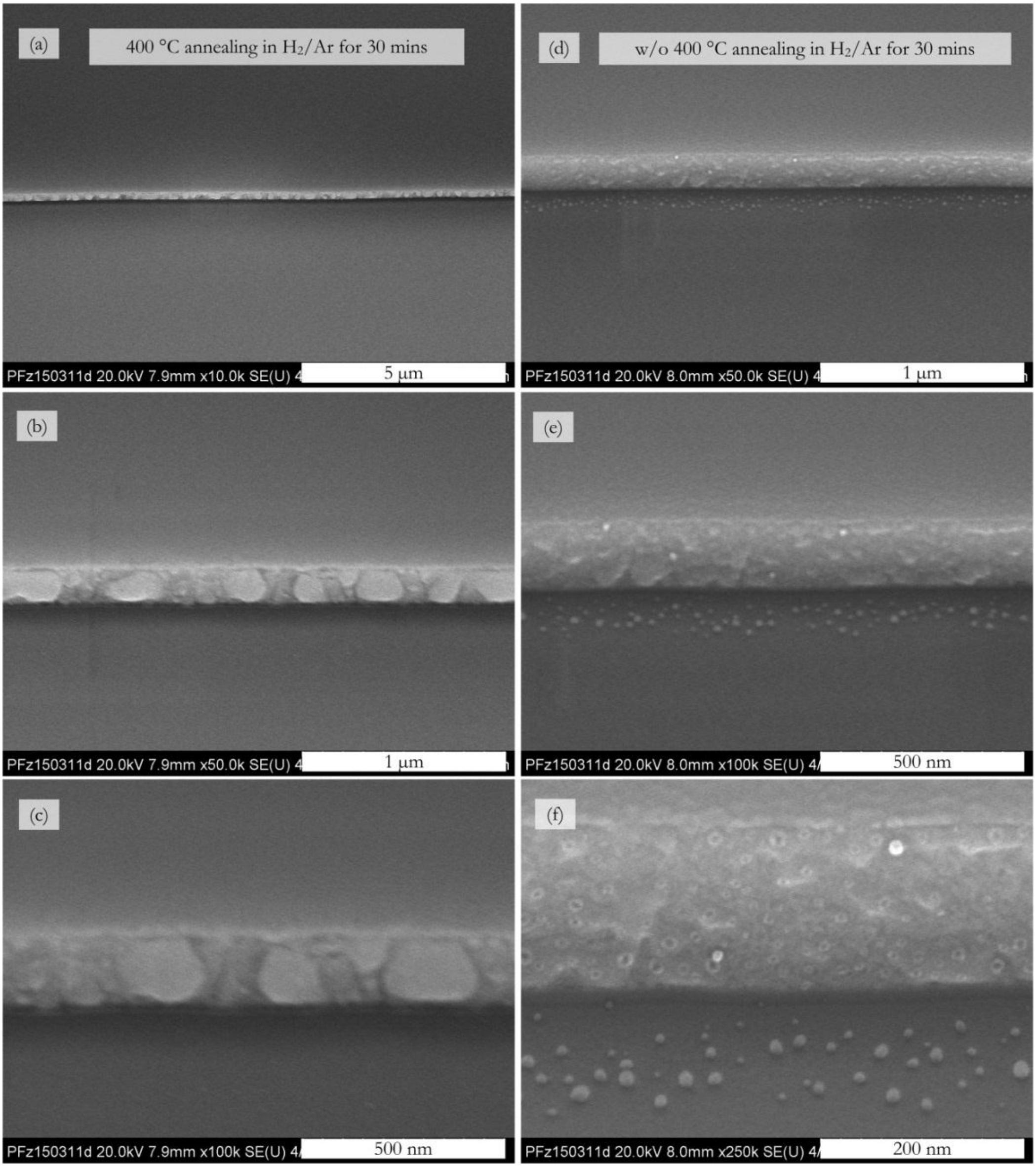


Figure 4.20 Comparison of In NPs formation on the sidewall of buried RT-deposited ITO layer with (a, b, c) and without post-annealing (d, e, f). The thickness of buried ITO layer is 200 nm.

4.2.3 CONCLUSION

In this section, a growth-in-place strategy for precise alignment and localization for in-plane SiNWs has been elaborated.

Guiding-steps are introduced on the substrate in the solid-liquid-solid system, so that liquid In NPs can be pinned at the step corner with high surface energy. Moreover, the step corners facilitate Si heterogeneous nucleation and crystal growth from liquid In-Si alloy, as they lower the Gibbs energy barrier of nucleation. Therefore, a surface energy gradient is built-up, directing from *c*-Si to *a*-Si:H, which enables the guided growth of in-plane SiNWs along the step corners. Furthermore, the dominating factors for stabilizing the guiding effect are discussed. The guiding steps should be high enough to avoid the liquid In NPs spreading on the top surface of guiding steps, so that liquid In NPs can be pinned to the step corners in a stable manner. The *a*-Si:H coating layer should be as thin as possible, so that the region at the step corner can be fully depleted by In-Si intermixing and alloying, where *c*-Si precipitation is able to take place.

A technique of forming In NPs on the sidewall of buried ITO layers beneath the guiding steps is developed, which makes possible the positioning of In NPs and of the following grown in-plane SiNWs. Post-annealing of the substrate before H_2 plasma treatment is the key factor for the reproducible and reliable sidewall In NPs formation; as on the cross-sectional polycrystalline ITO in columnar structure (obtained by post-deposition annealing), the grain boundaries with high surface energy are considered to be the basin for collecting liquid In, based on the grain boundary wetting behaviour.

4.3 FABRICATION OF GUIDING-STEP/BURIED ITO LAYER STRUCTURE

In this section, the fabrication process of guiding-step/buried ITO layer structure is introduced. Moreover, several key points for optimizing the reliability of fabrication are elaborated.

4.3.1 FABRICATION PROCESS

The fabrication process utilizes optical-lithography and plasma etching techniques, which are detailed in Table 4.2 and Table 4.3, respectively.

Table 4.2 Optical-lithography procedures

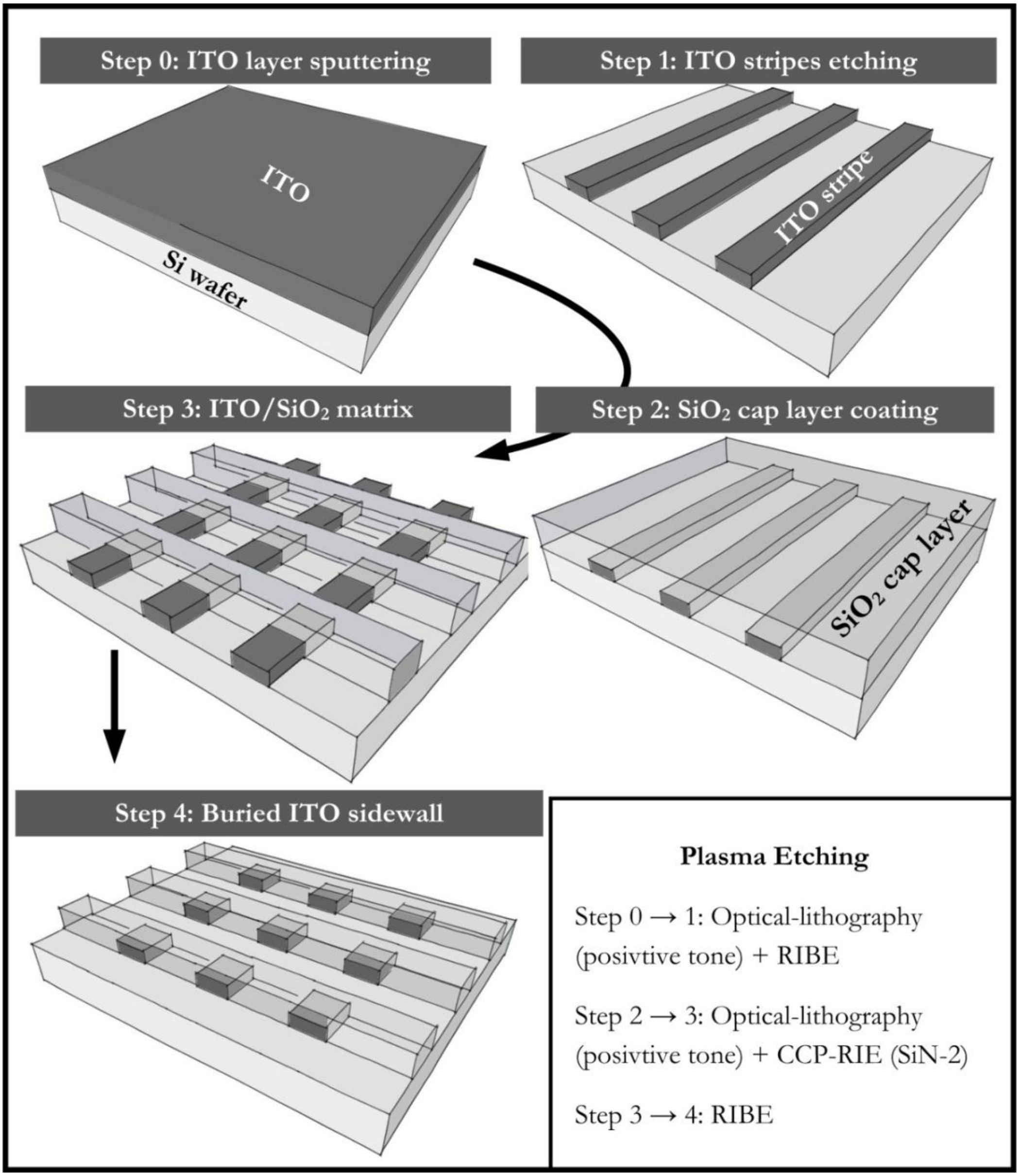
TECHNIQUE	**N°**	**STEP**
SAMPLE CLEANING	1	Wet samples (i.e. *c*-Si wafers) in acetone with ultra-sonication for 3 mins.
	2	Wet samples in isopropanol with ultra-sonication for 3 mins.
	3	Dry the sample by nitrogen gun.
DEHYDRATION	1	Bake the sample on hot plate at 190°C for 2 mins.
PHOTO-MASK CLEANING	1	Wet photo-masks in acetone with ultra-sonication for 3 mins.
	2	Wet photo-masks in isopropanol with ultra-sonication for 3 mins.
	3	Dry the sample by spin cleaner.
	4	Wet photo-masks in chromic sulphuric acid for 5 mins.
	5	Rinse photo-masks in deionized water.
	6	Repeat Step 2°.
	7	Repeat Step 3°.
OPTICAL-LITHOGRAPHY (NEGATIVE TONE FOR LIFT-OFF)	1	Sample cleaning and dehydration.
	2	Deposit *Primer* by spin-coater, 2000 rpm, 2000 rpm/s, 15 s.
	3	Deposit photo-resist *AZ5214E* by spin-coater, 4000 rpm, 2000 rpm/s, 30 s.
	4	Bake at 125°C for 1 min.
	5	Do the exposure in litho-machine (SÜSS MJB-4) under ultra-violet UV300 (wavelength 320 nm, ~10 mW/cm^2) for 5 s. The aligned photo-mask is in vacuum contact (-0.8 Pa) with the sample.

TECHNIQUE	**N°**	**STEP**
	6	Bake at 125°C for 1 min.
	7	Do the flood exposure for 30 s, without photo-mask.
	8	Do the development in developer *AZ-826MIF* for 20 s.
	9	Rinse samples in deionized water for 1~2 mins.
	10	Dry samples by nitrogen gun.
	11	Deposit thin films for lift-off
	12	Do the SAMPLE CLEANING procedure.
OPTICAL-LITHOGRAPHY (POSITIVE TONE FOR PLASMA ETCHING)	1	Sample cleaning and dehydration.
	2	Deposit *Primer* by spin-coater, 2000 r/min, 200 r/min^2, 15 s.
	3	Deposit photo-resist *AZ5214E* by spin-coater, 4000 r/min, 200 r/min^2, 30 s.
	4	Bake at 125°C for 1 min.
	5	Do the exposure in litho-machine (SÜSS MJB-4) under ultra-violet UV300 (wavelength 320 nm, ~10 mW/cm^2) for 15 s. The aligned photo-mask is in vacuum contact (-0.8 Pa) with the sample.
	6	Do the development in developer *AZ-826MIF* for 50~60 s.
	7	Rinse samples in deionized water for 1~2 mins.
	8	Dry samples by nitrogen gun.
	9	Plasma etching.
	10	Do the SAMPLE CLEANING procedure.

Table 4.3 Plasma etching conditions in CCP-RIE and RIBE

PLASMA ETCHING	**PROGRAM**	**RECIPE**
CCP-RIE	SiN-2	SI-BASED MATERIALS ETCHING: 5 mTorr, 15 Watt, 8 sccm SF_6/20 sccm CHF_3 plasma
	Delaq30	CARBON-BASED MATERIALS ETCHING: 100 mTorr, 30 Watt, 10 sccm O_2 plasma
	OXYALU	SURFACE ORGANIC ETCHING 10 sccm, 30 mTorr, 10 Watts O_2 plasma etching for 1 min.
		IN OR ITO ETCHING: CH_4/H_2 plasma
RIBE	ITO	Ion Beam Source (IBS): 20 sccm Ar, 9 sccm CH_4, 2.5 sccm O_2, for the etching.
		Back Side Cooling (BSC): 6 sccm He, for cooling the sample holder.
		Plasma Beam Neutralizer (PBN): 9 sccm Ar, for neutralize the positively charged sample surface due to the ion beam sputtering.
		Incidence angle of ion beam: 20°; rotation speed: 6 r/min.
		Micro-wave power: 350 Watt; ion beam voltage: 350V; ion beam current: 280 mA; acceleration voltage: 500 V.

The fabrication process of the guiding-step/buried ITO layer structure involves thin film sputtering deposition, optical lithography (positive tone) and plasma etching (CCP-RIE and RIBE); the flow chart is schematically represented in Figure 4.21.



Plasma Etching

Step 0 → 1: Optical-lithography (posivtive tone) + RIBE

Step 2 → 3: Optical-lithography (posivtive tone) + CCP-RIE (SiN-2)

Step 3 → 4: RIBE

Figure 4.21 Flow chart of guiding-step/buried ITO fabrication process

4.3.2 KEY POINTS IN THE FABRICATION PROCESS

The flow chart illustrated in Figure 4.21 is till now the optimized one for the reproducible and reliable fabrication. In order to detail the strategy on the guiding-step/buried- ITO fabrication, several key points are discussed.

4.3.2.1 BURIED IN LAYER: EVAPORATED IN OR SPUTTERED ITO

In order to develop a reproducible technique for the sidewall In NPs formation, the first task is to select the right material for buried In layer. Evaporated In and ITO thin films are the two candidates. The In NPs formation on these two types of In thin films has been studied in previous chapters.

The morphology of evaporated In thin films consists of 3D islands. The function of H_2 plasma treatment at 300°C is to reduce their surface indium oxide (see 2.3.2) and to obtain fresh In NPs which can lead the growth of SiNWs after *a*-Si:H coating and annealing, via a reactive-spreading-and-coalescing behaviour of liquid In on *a*-Si:H (see 3.2.1). Figure 4.22 shows the SEM images of buried evaporated In layer beneath guiding steps by different dry etching techniques, i.e. CH_4 RIE for evaporated In sidewall as seen in (a, b); $CH_4/H_2/O_2/Ar$ RIBE for evaporated In sidewall as seen in (c, d); and the result of RIBE etched In sidewall after 20 nm *a*-Si:H coating and annealing at annealing at 450°C, as seen in (e, f). This indicates that evaporated In is less practical. The detrimental drawback is its discontinuous morphology. On the one hand, it is difficult to control the etching stop for discontinuous thin film, since CH_4 plasma etching (CCP-RIE) is an isotropic etching process, over-etching leaves some holes on the sidewall of buried In layer, as shown in (a) and (b). On the other hand, even though $CH_4/H_2/O_2/Ar$ RIBE process is much more directional, the fabricated sidewall consists of discrete In islands, as shown in (c) and (d). Therefore, the guiding step coating on the discrete 3D In islands impedes their following spreading-and-coalescing on *a*-Si:H. Besides, H_2 plasma can only reduce the exposed surface oxide of buried evaporated In, which does not facilitate the sufficient In-*a*-Si:H contact for the reactive spreading-and-coalescing mode, hence the final In NPs leading the growth are rarely formed, as shown in (e) and (f). Figure 4.24 schematically represents the drawback of buried evaporated In layer.

In contrast, on a continuous ITO surface, In atoms are released in-situ by H_2 plasma reduction of oxygen and In NPs are formed via a nucleating-growing-and-coalescing behaviour (see 2.4.1.3). Figure 4.23 shows the sidewall of buried ITO layer fabricated by $CH_4/H_2/O_2/Ar$ RIBE, whose sharp and smooth surface demonstrates itself as the favourable choice for the sidewall In NPs formation.

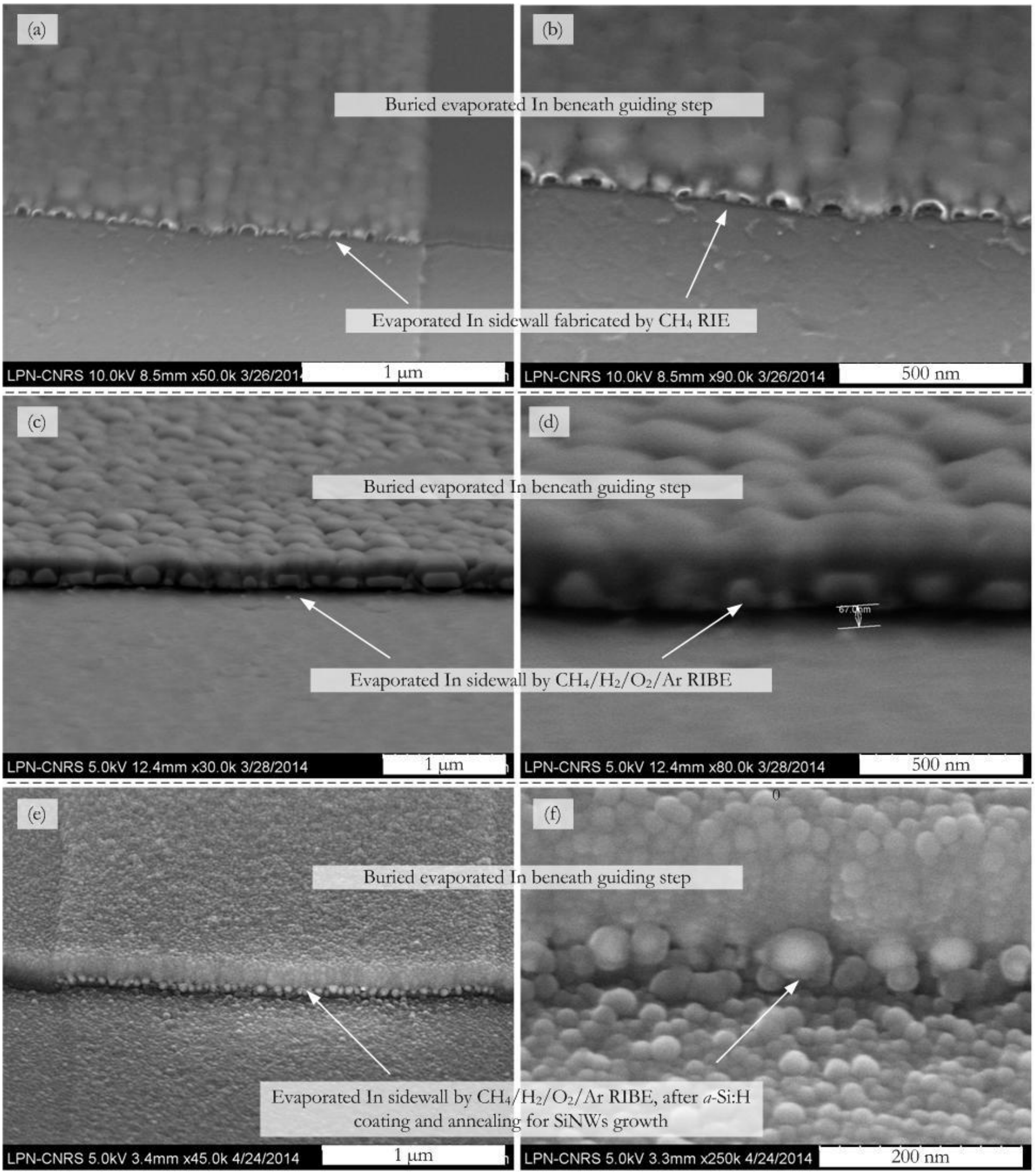


Figure 4.22 Buried evaporated indium layer beneath guiding step

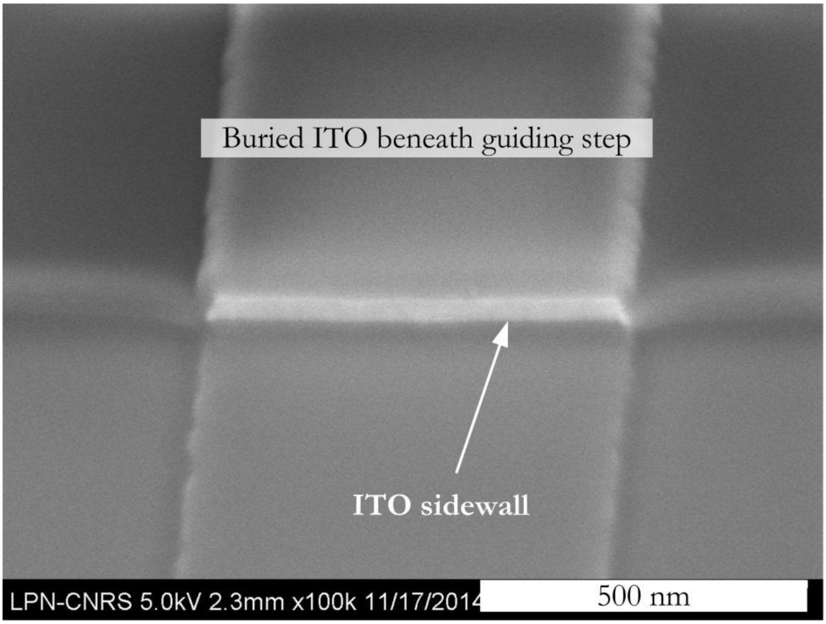
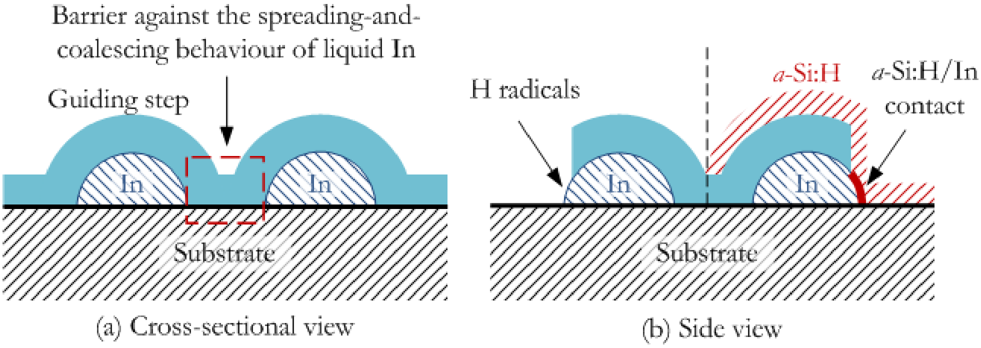


Figure 4.23 Buried ITO layer beneath the guiding step



(a) Cross-sectional view (b) Side view

Figure 4.24 Schematic representation of an evaporated In layer beneath guiding step: (a) cross-sectional view, guiding step as barrier against the spreading-and-coalescing behaviour of liquid In on *a*-Si:H (not shown); (b) side view, H radicals and the following *a*-Si:H can only arrive at the a partial region of surface indium oxide exposed outside, as illustrated at the left and right side, respectively.

4.3.2.2 STRIPES FABRICATION: LIFT-OFF VS. PLASMA ETCHING

As illustrated in the flow chart (see Figure 4.21), stripes of ITO and guiding steps are fabricated by optical-lithography (positive tone) and plasma etching, corresponding to step 0→1 and 2→3, respectively. As introduced in Chapter 1, surface damage cannot be completely avoided during plasma etching process; moreover it can bring about re-sputtering to guiding step edges. Lift-off (normally for patterning metal thin films) can circumvent these problems, however SiO_2 sputtering is less anisotropic than thermal evaporation, SiO_2 can be sputtered on the sidewall of photo-resist and left on the substrate after lift-off. Bilayer photo-resist structures were tested to solve this problem. With bilayer structures[14] (LOR5A/AZ5214E), the sidewall sputtering cannot be efficiently avoided, as shown in Figure 4.25. With thick bilayer structure (LOR5A/SU8-2002), the sidewall sputtering is avoided, however the guiding step edge after lift-off is not sharp anymore, as shown in Figure 4.26. The same problem was encountered when patterning an ITO thin film, as shown in Figure 4.27.

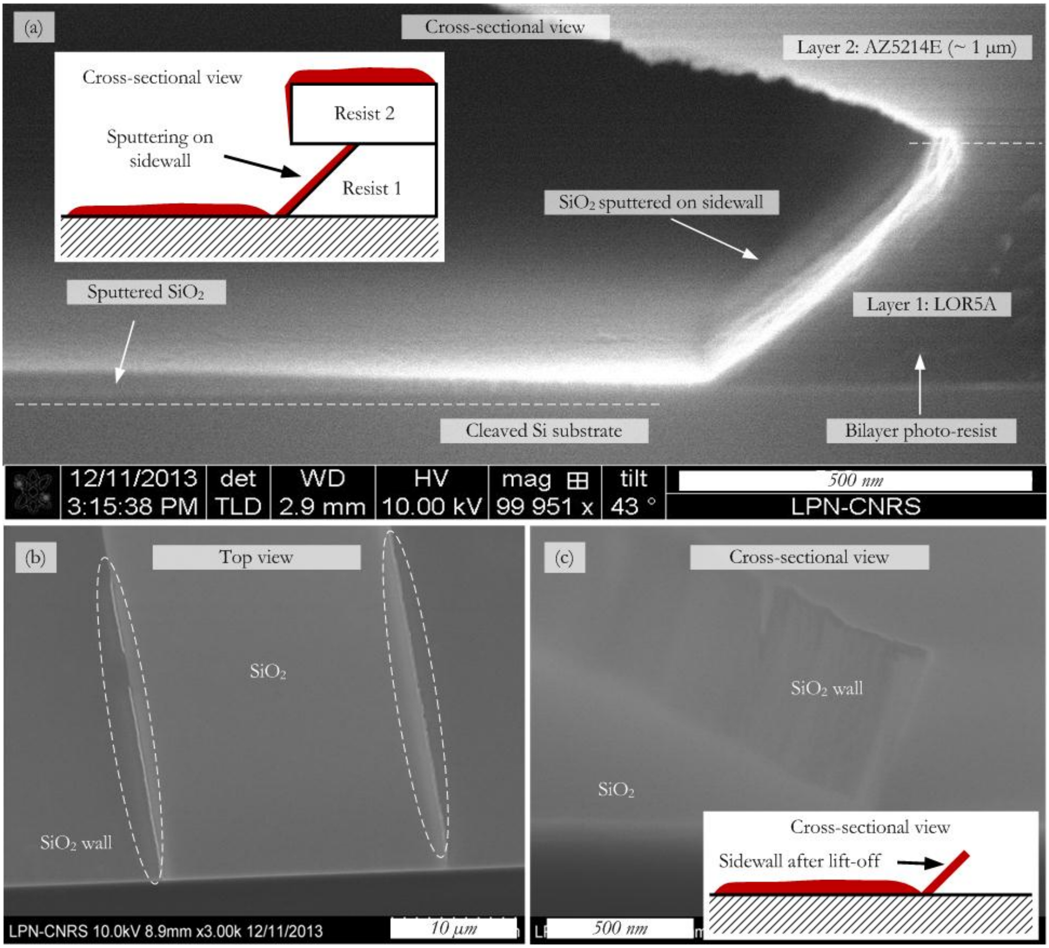


Figure 4.25 Bilayer lift-off (LOR5A/AZ5214E) for fabricating a guiding-step: (a): SiO_2 film is sputtered on sidewall of bilayer photo-resist (AZ5214E is ~1µm thick), the inset image is the schematic representation after sputter deposition; (b) and (c): after lift-off SiO_2 walls are left, the inset image in (c) is the schematic representation after lift-off.

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[14] Schematic representation can be referred to Figure 1.25 Bilayer photo-resists for lift-off process.

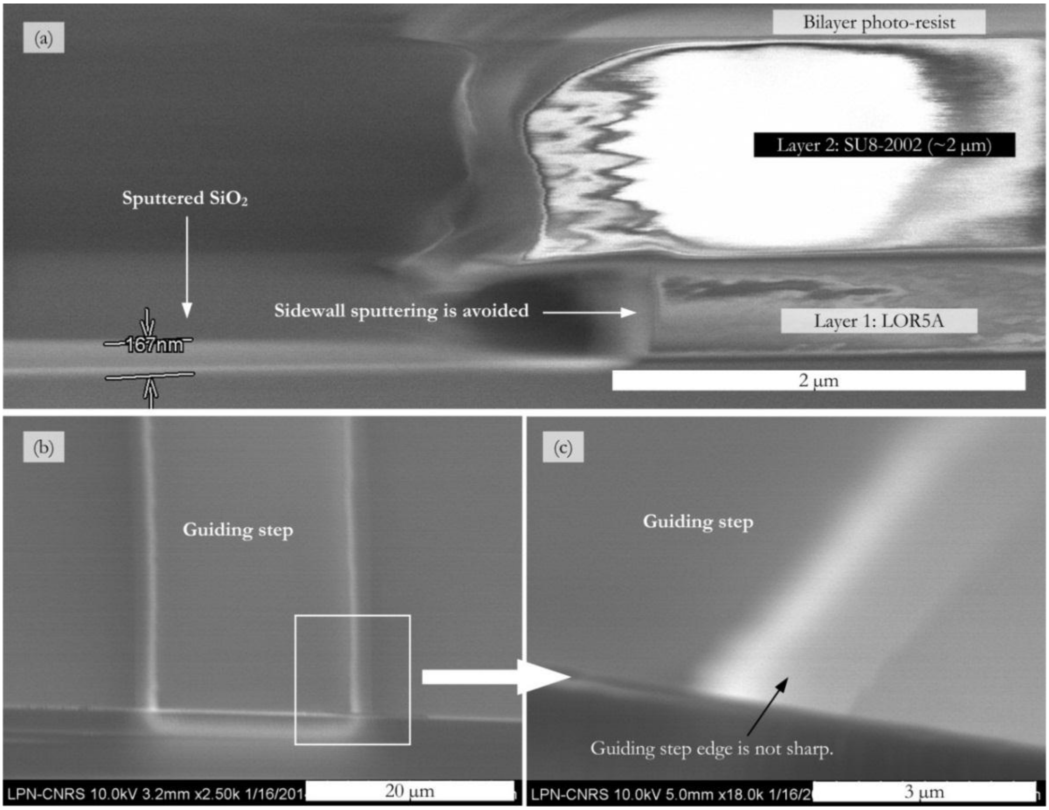

Figure 4.26 Bilayer lift-off (LOR5A/SU8-2002) for fabricating a guiding-step: (a) sidewall SiO_2 sputtering is avoided as SU8-2002 is thicker (~2 μm); (b) and (c) however the guiding step edge is not sharp any more.

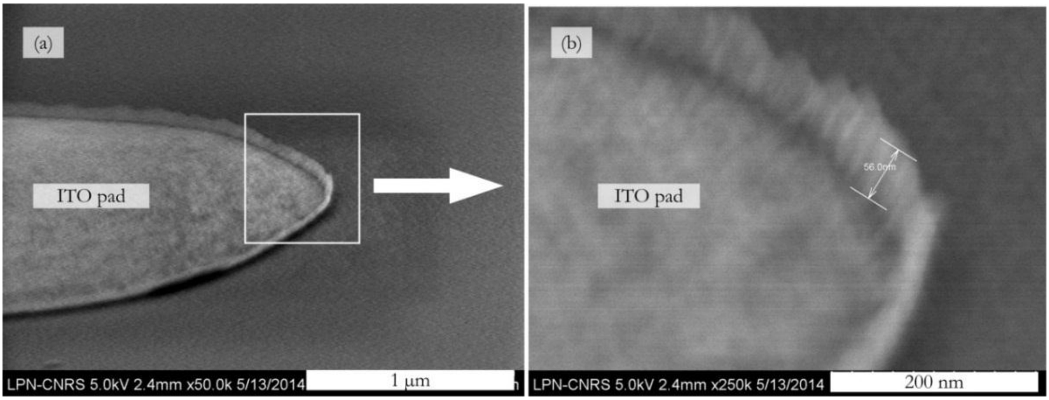

Figure 4.27 Lift-off (monolayer photo-resist AZ5214E) for patterning ITO.

Therefore, we use CCP-RIE technique to fabricate the guiding steps, whose vertical sidewall is achieved by SF_6/CHF_3 plasma etching. Figure 4.28 shows SEM images of guiding steps fabricated by SF_6 (see image a) and SF_6/CHF_3 (see image b) RIE etching. Pure SF_6 RIE etching brings roughness to the surfaces and results in less sharp vertical sidewall, in comparison with the SF_6/CHF_3 etching thanks to the fluorocarbon films formation during the etching process (see Figure 1.29).

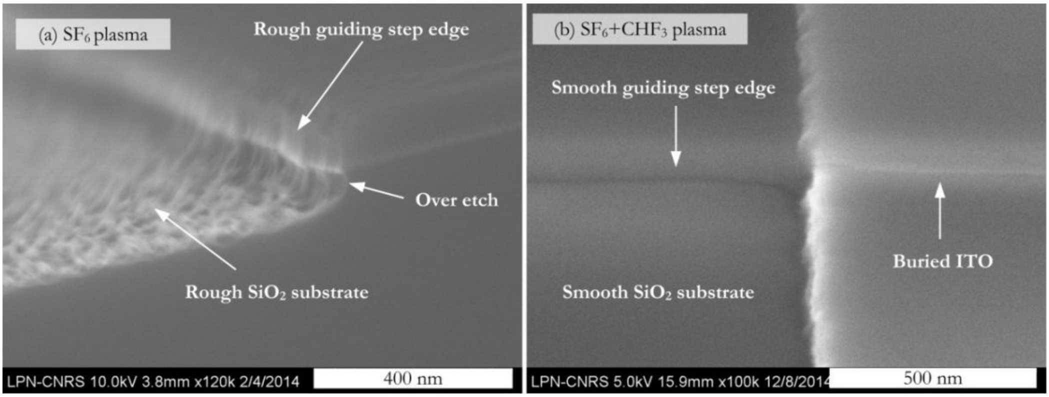

Figure 4.28 Different CCP-RIE processes for fabricating guiding steps. This is a practical illustration of the schematics shown in Figure 1.29.

4.3.2.3 ETCHING MASK FOR BURIED ITO FABRICATION

As illustrated in Figure 4.21, the flow chart for buried ITO sidewall fabrication (step 3→4), photo-resist is removed before step 4, thus the guiding-step functions as an etching mask. Figure 4.29 shows the results of RIBE process with photo-resist as etching mask. The ITO etching is not sufficient, and fails to yield a sharp sidewall of buried ITO layer. A shadow effect is not supposed to be the main cause to this problem: on the one hand, it mostly takes place for high aspect ratio nano-structure etching; on the other hand, the incidence angle is 20° in RIBE etching, for which shadowing is less likely to occur. The reason remains unclear. A possible explanation is that the photo-resist is damaged during the guiding step fabrication by SF_6/CHF_3 CCP-RIE etching (step 2→3). Anyhow, sharp ITO sidewall (see Figure 4.23) can be reproducibly fabricated with a guiding step as etching mask (or as sacrificing layer), as illustrated in Figure 4.30.

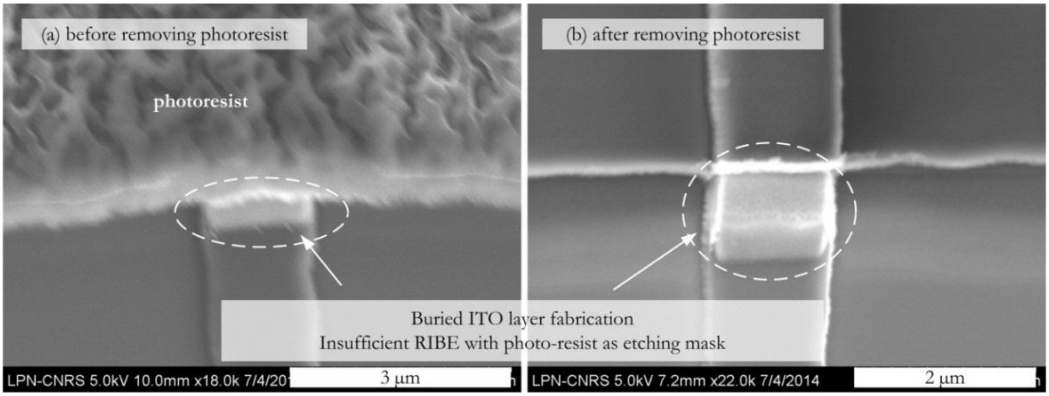

Figure 4.29 Buried ITO layer fabrication by RIBE with photo-resist as etching mask, corresponding to step 3 →4 in Figure 4.21 of fabrication flow chart.

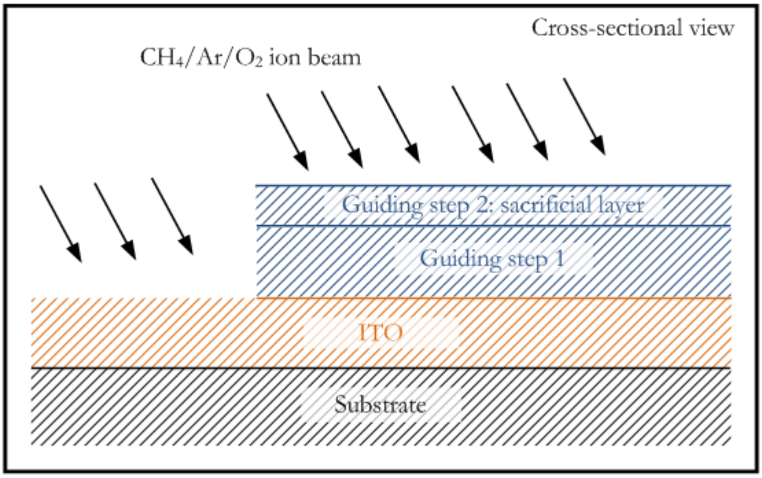

Figure 4.30 Schematic representation of a sacrificial layer of guiding step as RIBE etching mask for buried ITO fabrication.

4.3.3 CONCLUSION

The process of fabricating a guiding step/buried ITO layer has been presented in this section. This involves sputter deposition of thin films, optical-lithography (positive tone) and plasma etching (CCP-RIE and RIBE). Furthermore, key points in the fabrication process have been clarified, including strategies on selecting buried In layer candidates, guiding step fabrication methods, and RIBE etching masks for buried ITO fabrication.

4.4 SUMMARY AND PERSPECTIVES

In this chapter, the growth-and-place and growth-in-place approaches for organising 1-D semiconductor nanostructures have been briefly reviewed. In particular, graphoepitaxy is applied to most of the growth-in-place cases, where nano-facets (or atomic steps) with high surface energy pin the liquid metal catalysts and guide the growth of NWs or CNTs.

We propose a step-guided growth method for the alignment of in-plane SiNWs, where a guiding step is introduced in the in-plane solid-liquid-solid system by substrate surface patterning, so that the step corners have higher interfacial area in contact with liquid In NPs in comparison with flat substrate surface, thereby providing a higher solid-liquid interfacial energy for pinning liquid In. Moreover, guiding step corners are also the preferential sites for Si heterogeneous nucleation and crystal growth from supersaturated liquid Si-In alloy, hence the surface energy gradient is built up along them, which maintains the guided growth. The key factor for stabilizing the step-guided growth is considered to be the thickness of *a*-Si:H coating layer, since *c*-Si precipitation at guiding step corners requires the depletion of *a*-Si:H there by In-*a*-Si:H intermixing. In order to localize the aligned in-plane SiNWs, a technique of In NPs formation on the sidewall of buried ITO layer beneath the guiding step has been proposed and developed. Thermal annealing by H_2 plasma treatment is the key factor for the reproducible and reliable In NPs formation. The grain boundary wetting theory is utilized to explain this phenomenon, where RT-deposited ITO layer is transformed from amorphous to polycrystalline by thermal annealing. The grain boundaries on the sidewall of columnar *pc*-ITO collect liquid In as sinks due to the high grain boundary energy compared with uniform grains.

The fabrication process has been detailed; it involves thin film sputtering deposition, optical-lithography and plasma etching (CCP-RIE and RIBE). The key points of the fabrication process have been discussed, which elaborate the strategies on selecting buried In layer candidates (evaporated indium or sputterd ITO), guiding step fabrication methods, and RIBE etching masks for buried ITO fabrication.

Figure 4.31 shows a long guided in-plane SiNW (see image a), however with a surface rough probably transferred from substrate and guiding step corner (see images b and c). Further efforts will be focused on suppressing the surface roughness by chemical process and testifying the possibility of growing long guided in-plane SiNW array on insulator in high density and small diameter (< 20 nm), which is expected to be an alternative technique for Fully-Depleted Silicon-On-Insulator (FD-SOI) (see Introduction: Planar vs. Non-planar architectures), as illustrated in Figure 4.32.

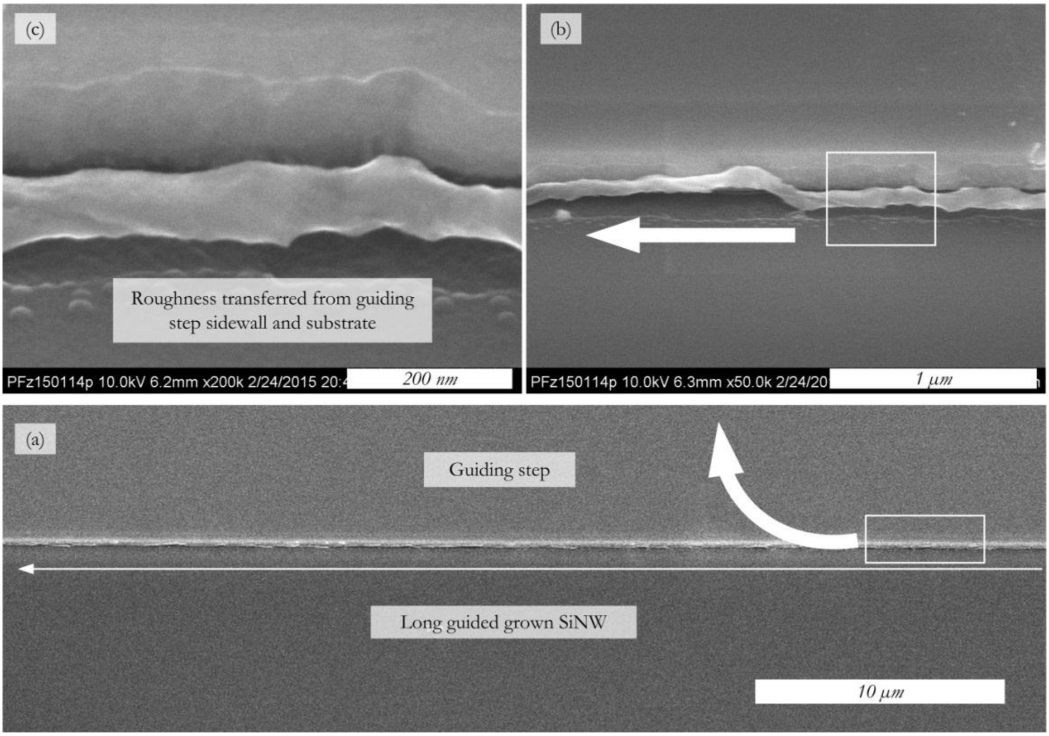

Figure 4.31 A long guided in-plane SiNW (a) with surface rough transferred from substrate and guiding step corner (b, c).

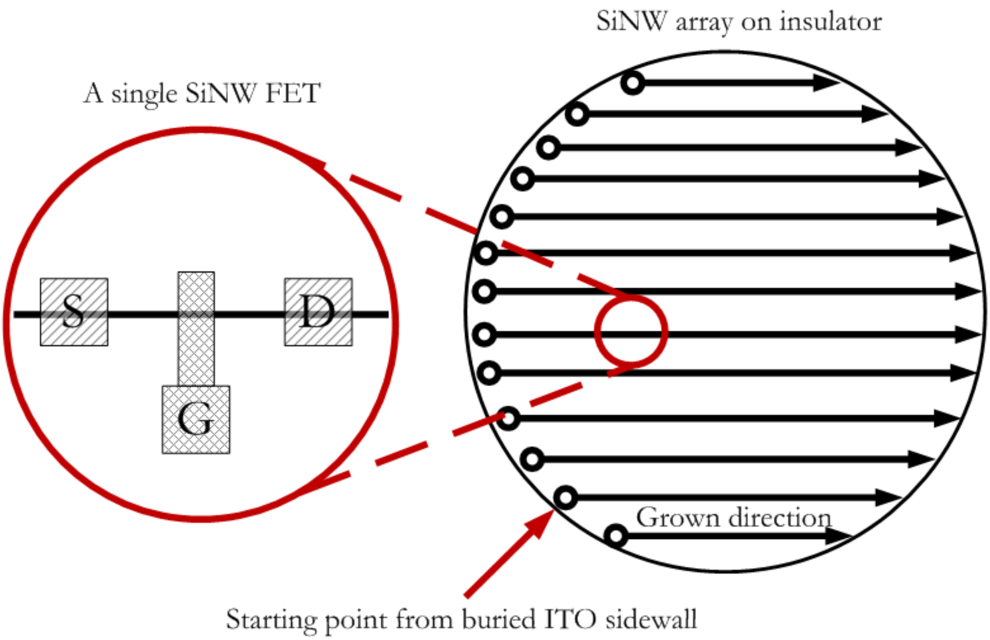

Figure 4.32 Schematic representation of guided SiNW array on insulator.

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SUMMARY AND PERSPECTIVES

This is the first PhD thesis on the study of the growth of in-plane silicon nanowires (SiNWs) as well as on the development of a method for their self-organisation in view of nano-electronic applications. The growth of in-plane SiNWs is based on plasma-enhanced chemical vapour deposition (PECVD) thin film techniques and results from the interaction between a liquid metal drop and a hydrogenated amorphous silicon (*a*-Si:H) thin film (i.e. a solid-liquid-solid growth mode).

We use indium as a catalyst for the bottom-up growth of in-plane SiNWs. Evaporated indium and sputtered ITO are the two types of thin films from which indium NPs are obtained, thanks to their exposure to a H_2 plasma on a heated substrate (e.g. 300°C) before *a*-Si:H coating at temperatures lower than the indium melting point. The effects of H_2 plasma conditions as well as the substrate temperature are investigated. The evaporation of indium leads to discontinuous islands which get oxidized during their transfer to the PECVD reactor. A H_2 plasma is used to reduce the oxide layer formed at the indium surface, assisted by substrate heating (typically above 250°C). This enables a sufficient *a*-Si:H/In contact, required for NW growth. During the hydrogen plasma treatment, the morphology of indium experiences a transformation from solid flat islands with surface oxide to liquid spherical caps and finally solidifies into spheres. This is in contrast with the effect of a simple annealing of the particles at substrate temperatures above the indium melting point or with the effect of a H_2 plasma treatment at substrate temperatures below its melting temperature (e.g. 150°C). Scanning electron microscopy is a conviennent method to verify whether the indium surface oxide is sufficiently reduced or not, even though the morphology of the particles itself does not affect the following SiNWs growth. Interestingly, substrate heating at high temperatures for long durations can cause indium loss. In addition, indium NPs can get redistributed on micro/poly-crystalline substrates (i.e. *μc*-Si:H and polycrystalline AZO) based on grain boundary wetting (GBW), which is not possible on substrates with relatively isotropic surface chemistry (i.e. amorphous SiO_2). This GBW-based mechanism provides an opportunity to disperse the indium NPs for various applications; however the accurate control of the size and density of nanoparticles needs further efforts. In comparison with evaporated indium thin films, indium can be generated in-situ in the PECVD reactor by exposing an ITO thin film to a hydrogen plasma. A Growth-and-Coalescence mechanism is proposed to explain the In NPs formation, where the sputtered ITO surface is reduced by the hydrogen plasma and thus releases indium atoms which can nucleate to produce indium nanoparticles. The increase of the density of nanoparticles with hydrogen exposure time leads to the growth and coalescence of the indium nanoparticles with neighbouring ones. The size and density control is still a problem, however a technique based on the Growth-and-Coalescence mechanism is developed via inserting an ITO layer between evaporated indium thin films and the substrates (i.e. In/ITO bilayer). Compared with indium NPs redistribution by grain boundary wetting, this technique is believed to be more feasible and advantageous in size and density control, even though further optimisation is needed.

ITO thin films deposited at room temperature (RT) undergo a phase transition from amorphous to polycrystalline when heated at temperatures above 150 °C as confirmed by TEM investigation. The change from amorphous to polycrystalline structure makes the indium NPs formation on ITO surface to seem more complicated. We found that it plays a crucial role on the indium NPs formation on ITO sidewall, which enables the indium NPs positioning at large scale. However, long time substrate heating is not recommended, neither a high RF power plasma which can induce local heating. This systematic understanding of the evolution of the two types of indium thin films brings benefits to the development of indium NPs positioning for the self-organisation of in-plane SiNWs.

The growth mechanism of in-plane solid-liquid-solid SiNWs is explained from the viewpoint of spontaneous motion of liquid indium NPs on *a*-Si:H. Liquid indium reactively spreads on *a*-Si:H, induces the solid phase crystallization of *a*-Si:H, and thereby builds up a surface energy gradient from *c*-Si to *a*-Si:H. Driven by the unbalanced Young's force, the liquid In move forward to the *a*-Si:H region. The growth of SiNWs is a particular type of contribution to the surface energy gradient maintenance. Moreover, it is also a particular type of product resulting from the liquid indium movement on *a*-Si:H. SEM observations indicate that the movement of a liquid indium NP on *a*-Si:H leaves a trail which can be divided into two parts with a constant ratio: a SiNW located in the centre and a residual *a*-Si:H at its two sides. A possible reason is that the central region depleted from *a*-Si:H favours the precipitation of *c*-Si. Further geometric investigation and statistical analysis reveal that the liquid indium reactive spreading behaviour can be enhanced by a relatively thicker *a*-Si:H. The relationship between SiNWs diameter, *a*-Si:H thickness and indium NP size has been quantitatively described. As it is the *a*-Si:H layer that modifies the substrate surface and enables the liquid indium movement, the structural properties of *a*-Si:H have been studied, in order to lower the growth temperature. From the atomic viewpoint, the growth of SiNWs consists of a series of processes: Si bond breaking in *a*-Si:H, In-Si intermixing-and-alloying and Si nucleation and crystal growth. Based on this, a simple strategy of lowering the *a*-Si:H deposition temperature is proposed to intentionally introduce extra disorder in the amorphous network so that the Si bonds are weakened and the Gibbs energy barrier for crystallization is lowered. The *a*-Si:H structural modification is demonstrated by Raman spectroscopy and spectroscopic ellipsometry measurements. As a result, SiNW growth is succeeded at a nominal substrate temperature of 350°C for a-Si:H films deposited at 100 °C, which compares favourably with the growth temperature of 450°C required for *a*-Si:H deposited at 180°C. To further understand the IPSLS growth mode, other metal catalysts (i.e. Sn and Au) and an alternative solid precursor (*a*-Ge:H) are applied to grow NWs. However, none of these metals leads to SiNWs growth. A possible reason for their failure is that the eutectic points of binary alloys (i.e. Si-Sn, Si-Au, and Ge-In) are quite close to the respective hydrogen effusion temperature of *a*-Si:H or *a*-Ge:H, which is assumed as the boundary for NWs growth. Above this temperature, the amorphous network can get relaxed or even start to crystallize so that the interaction between liquid indium and *a*-Si:H is impeded and so is the SiNWs growth. Indium is till now the most successful catalyst metal as the eutectic temperature of In-Si alloy is far lower than the temperature for hydrogen effusion from *a*-Si:H. Based on this criteria, Ga and In are predicted to be favourable candidates for GeNWs growth.

For a practical use of in-plane SiNWs in electronic applications, it is of prime importance to organize them in a controllable way. We propose a step-guided growth method for the alignment of in-plane SiNWs, where a guiding step is introduced in the in-plane solid-liquid-solid system by substrate surface patterning, so that the step corners have higher interfacial area in contact with liquid indium NPs in comparison with a flat substrate surface, thereby providing a higher solid-liquid interfacial energy for pinning liquid In. Moreover, guiding step corners are also the preferential sites for Si heterogeneous nucleation and crystal growth from supersaturated liquid Si-In alloy. Hence, a surface energy gradient is built up along them, which maintains the guided growth. The key factor for stabilizing the step-guided growth is considered to be the thickness of the *a*-Si:H coating layer, since *c*-Si precipitation at guiding step corners requires the depletion of *a*-Si:H and therefore *a*-Si:H/In intermixing. In order to localize the aligned in-plane SiNWs, a technique of In NPs formation on the sidewall of buried ITO layer beneath the guiding step has been proposed and developed. Thermal annealing by H_2 plasma treatment is the key factor for the reproducible and reliable In NPs formation. The grain boundary wetting theory is utilized to explain this phenomenon, where RT-deposited ITO layers are transformed from amorphous to polycrystalline by thermal annealing. The grain boundaries on the sidewall of columnar *pc*-ITO collect liquid In as sinks due to the high grain boundary energy compared with grains. The fabrication process has been detailed; it involves thin film sputtering deposition, optical-lithography and plasma etching (CCP-RIE and RIBE). The key points of the fabrication process have been discussed, which allowed to elaborate the strategy based on selecting the material for buried In layer, guiding step fabrication methods, and RIBE etching masks for buried ITO fabrication.

As a summary, the research carried out during this PhD has promoted our understanding on: (1) indium nanoparticles formation from evaporated indium and sputtered ITO thin films; (2) the growth mechanism of in-plane silicon nanowires obtained from a solid-liquid-solid growth process. Based on the above understanding, we proposed a self-organisation technique (alignment and localization) for in-plane silicon nanowires, consisting of a step-guided growth method for the alignment and a method of forming indium nanoparticles on buried ITO sidewall for the localization.

In perspective, *in-situ* TEM observation and analysis would be a powerful tool to verify the in-plane silicon nanowires growth mechanism we proposed, as well as the indium nanoparticles formation on ITO surface. Lowering the growth temperature of silicon nanowires is always an expectation and challenge. Futher efforts should be focused on the effects of *a*-Si:H structural properties and preparation conditions on the silicon nanowires growth temperature. Moreover, germanium and silicon/germanium alloy nanowires are also of great interest for electronic applications. We expect that these two types of semiconductor nanowires can be obtained via our growth process, by adjusting the process parameters. Finally, this work sets the basis for the fabrication of SiNW field effect transistors on insulator, which also allows for gate engineering.

APPENDIX A: PECVD SUBSTRATE TEMPERATURE CALIBRATION

We used resistance thermometers (Pt100) to calibrate the substrate temperature of PLASFIL. Figure A.1 shows the calibration result carried our on 2012/11/05. We used *c*-Si wafer and corning glass as substrates. During the heating process, the chamber pressure was 1 Torr with mixture gas of 100 sccm H_2 and 10 sccm SiH_4. The upper electrode (RF) was set at nominal 400 °C. It shows that the temperature difference in these twe types of substrates can be omitted. Figure A.2 shows the calibration result carried our on 2015/09/07. We used corning glass as substrates. During the heating process, the chamber pressure was 1 Torr with 100 sccm H_2. The upper electrode (RF) was set at nominal 200 °C. Figure A.3 and A.4 shows the substrate temperature stabilization time in PLASFIL, when heating the corning glass substrate in H_2 (1 Torr, 100 sccm) from nominal 200°C to 250°C and from nominal 250°C to 600°C, respectively. It takes around 15 mins for stabilize the substrate temperature.

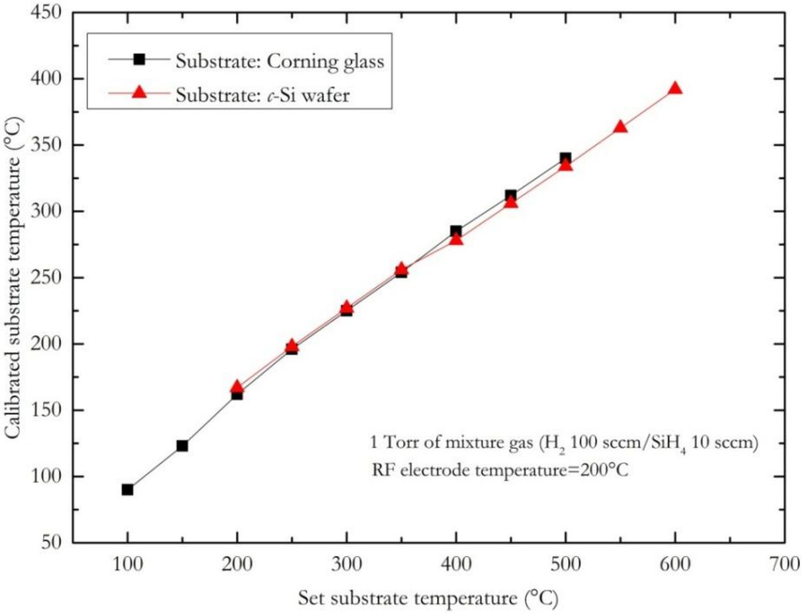

Figure A.1 Substrate temperature calibration of PLASFIL (Corning glass and p-type (100) *c*-Si wafer as substrates). Date: 2012/11/05. By Zheng FAN, Linwei YU, Pavel BULKIN.

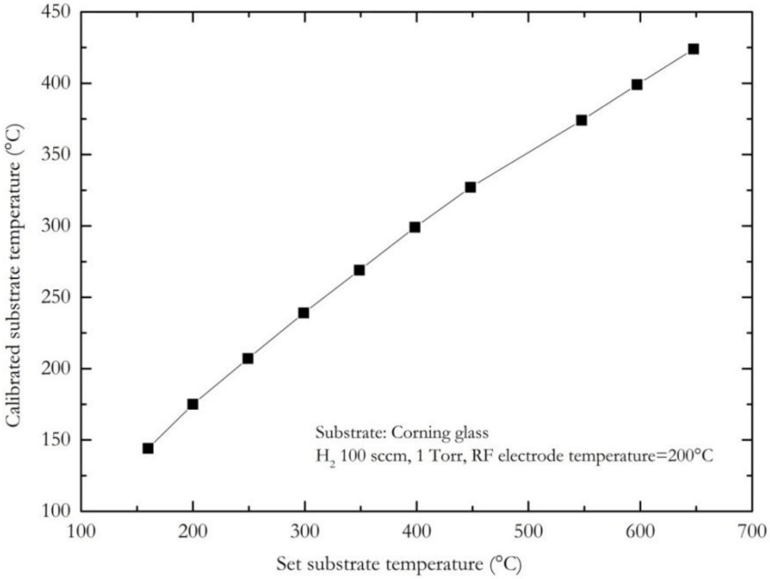

Figure A.2 Substrate temperature calibration of PLASFIL (Corning glass as substrate). Date: 2015/09/07. By Jian TANG, Dmitri DAINEKA, Cyril JADAUD, Pavel BULKIN.

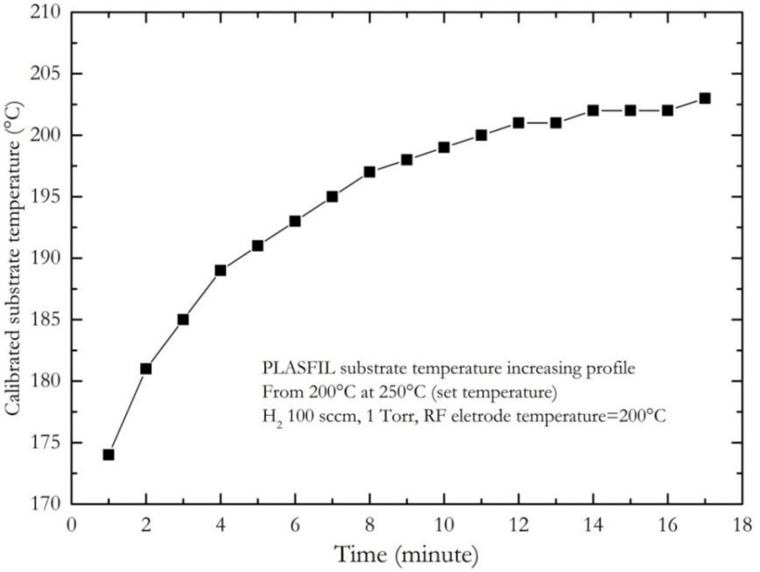

Figure A.3 Substrate temperature stabilization time of PLASFIL (Corning glass as substrate, at nominal 250°C). Date: 2015/09/07. By Jian TANG, Dmitri DAINEKA, Pavel BULKIN, Cyril JADAUD, Pavel BULKIN.

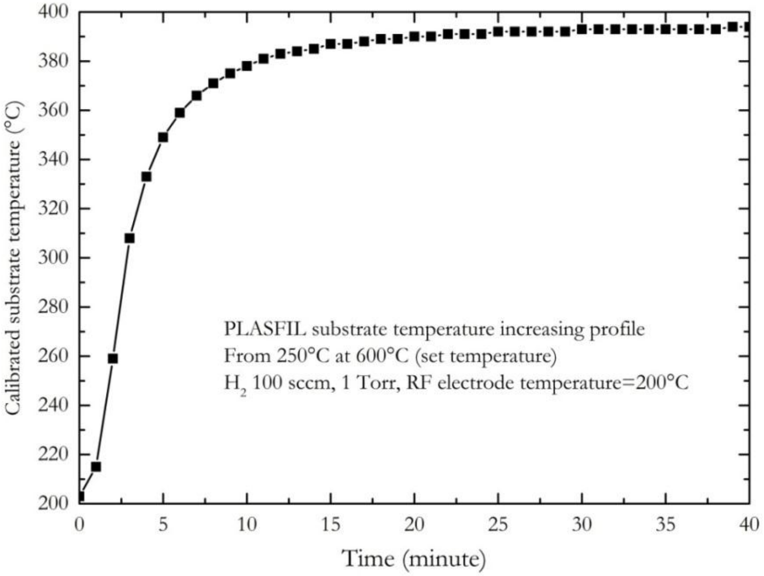

Figure A.3 Substrate temperature stabilization time of PLASFIL (Corning glass as substrate, at nominal 600°C). Date: 2015/09/07. By Jian TANG, Dmitri DAINEKA, Cyril JADAUD, Pavel BULKIN.

ABSTRACT This is the first Ph.D. thesis on studying the growth of in-plane silicon nanowires (SiNWs) and developing a method for self-organising them for nano-electronics applications. The growth of in-plane SiNWs is based on plasma-enhanced chemical vapour deposition (PECVD) thin film techniques and results from the interaction between a metal droplet and a hydrogenated amorphous silicon (*a*-Si:H) thin film. This in-plane solid-liquid-solid (IPSLS) growth mode can be considered as a reactive-spreading and moving behaviour of indium droplet on *a*-Si:H activated by the establishment of a surface energy gradient due to the phase transition from *a*-Si:H at the advancing NP edge to *c*-Si at the NP receding edge. In order to integrate IPSLS SiNWs in nano-electronic devices it is of prime importance to organise them in a controllable way. We propose a growth-in-place strategy which enables the SiNWs to grow along pre-patterned guiding steps. Moreover, this technique is applied to form In NPs on the sidewall of buried ITO layers, which facilitates the localization of the step-guided SiNWs. This work sets the basis for the fabrication of SiNW field effect transistors on insulator, which also allows for gate engineering and the obtaining of Fully Depleted Silicon-On-Insulator (FD-SOI).

KEY WORDS: in-plane silicon nanowires, solid-liquid-solid growth mode, reactive spreading, step-guided growth, Indium nanoparticles formation, SiNW field effect transistors.

RESUME Celle-ci est la première thèse sur la fabrication et caractérisation de nanofils de silicium (SiNWs) horizontaux basé sur des techniques de dépôt chimique en phase vapeur assisté par plasma (PECVD). La croissance de nanofils de silicium dans le plan de l'échantillon découle de l'interaction entre une goutte métallique et une couche de silicium amorphe hydrogéné (*a*-Si:H). Dans ce procédé la nanoparticule d'indium liquide (NP) se déplace sur un substrat couvert d'une couche d'*a*-Si:H. Lors de son déplacement la NP dissout et absorbe la couche d'a-Si:H sur sa face avant et précipite un nanofil de silicium cristallin (c-Si) par sa face arrière. Ce mode de croissance de nanofils, que nous avons appelé in-plane solid-liquid-solid (IPSLS), peut être considéré comme un processus de mouillage réactif dans lequel le déplacement de l'indium liquide sur le *a*-Si:H est activé par l'établissement d'un gradient d'énergie superficielle entre le a-Si:H en face avant de la NP et le c-Si à l'arrière. Afin d'intégrer les nanofils dans dispositifs électroniques (transistors), il est primordial de les organiser d'une manière contrôlée. Nous proposons une méthode pour guider la croissance des nanofils basée sur la formation de marches sur le substrat par des techniques de nanofabrication. Qui plus est, nous avons développé une technique de formation de NPs d'In à la surface d'une paroi d'oxyde d'indium et étain (ITO) enterrée. Ceci permet la localisation du point de départ des nanofils. Cette stratégie de croissance de nanofils établit les bases pour la fabrication de transistors à base de nanofils de silicium sur l'isolant, ce qui ouvre la voie à la réalisation de transistors complétement déplétés sur isolant (FD-SOI).

MOTS CLES: nanofils de silicium horizontaux, le mode de croissance solide-liquide-solide, le guidage de croissance long marches, le mouillage réactif, la formation de nanoparticules de l'indium, les transistors à base de nanofils de silicium