Design of wideband high-resolution low-pass continuous-time delta-sigma modulators in CMOS process

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Conception de modulateurs Delta-Sigma passe-bas à temps continu en technologie CMOS pour des applications large bande et haute résolution

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T H È S E

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Conception de modulateurs Delta-Sigma Passe-bas à temps continu en technologie CMOS pour des applications à large bande passante et haute résolution

RESUME :

Le marché des convertisseurs analogique-numérique peut être segmenté en deux catégories de circuits. Nous distinguons d'une part, les blocs de propriété intellectuelle (IP) qui sont généralement optimisés pour une application spécifique. Et d'autre part, les circuits intégrés discrets qui sont conçus pour répondre aux besoins d'une plus large gamme d'applications.
Ce travail de thèse concerne la deuxième catégorie de composants. Il s'inscrit dans le cadre d'un programme de recherche et développement initié en 2010 dans le projet européen FP7 SACRA et dont le but était d'étudier la faisabilité d'un convertisseur analogique-numérique Delta-Sigma ($\Delta\Sigma$) qui pourrait rivaliser avec l'architecture pipeline pour des applications nécessitant une large bande passante (≥10MHz) et une haute résolution (>10-bit) comme l'imagerie médicale, les communications numériques sans fils ou câblées, la vidéo ou encore l'instrumentation.
A l'heure actuelle, le pipeline est toujours largement prédominant pour de telles applications et les rares solutions commerciales à base de modulateurs $\Delta\Sigma$ rapides se limitent à des bandes passantes de 10MHz ou 25 MHz pour une résolution effective autour de 12-bit et des consommations respectives de 100mW et 20mW.

Ce manuscrit synthétise les travaux de conception, fabrication et mesure d'un modulateur $\Delta\Sigma$ Passe-bas à temps continu avec une bande passante de 40MHz, et visant une résolution effective de 12-bit tout en consommant moins de 100mW. Pour atteindre nos objectifs nous avons tout d'abord analysé en détail les architectures de modulateurs $\Delta\Sigma$ publiés dans la littérature durant les dix dernières années. Cette première étape a permis de dégager les tendances qui se dessinent pour les applications nécessitant une large bande passante et une haute résolution. Sur base de cette étude et de notre expérience, nous avons proposé une architecture de modulateur $\Delta\Sigma$ qui s'articule autour d'un filtre à temps continu du $5^{ième}$ ordre et d'un quantificateur 5-bit. Ce choix atypique de résolution facilite, d'une part, l'intégration de notre ADC dans un système complet car les contraintes sur la gigue d'horloge sont relaxées. D'autre part, les contraintes de conception sur le filtre de boucle du modulateur lui-même sont également allégées. L'impact de ce choix architectural sur la consommation du modulateur a été analysé et une solution a été proposée pour optimiser le compromis entre la performance et l'efficacité énergétique du modulateur.
Un taux de sur-échantillonnage (OSR) de 8 a été choisi pour réduire autant que possible la vitesse d'horloge ce qui se traduit par une réduction de la consommation du modulateur et du filtre de décimation associé. Les problèmes de stabilité inhérents à l'utilisation d'un faible OSR sont résolus en injectant une fraction du signal d'entrée à différents nœuds du filtre de boucle.
Afin de faciliter le dimensionnement de chacun des sous-blocs du modulateur, un modèle comportementale incluant les principales imperfections du filtre de boucle, du quantificateur et des CAN de retour, a été réalisé et simulé sous Matlab. Cette approche nous a permis de spécifier le cahier des charges des sous-blocs du modulateur.
L'implémentation en technologie CMOS 65nm de chaque sous-bloc du modulateur est détaillée en insistant sur les critères de dimensionnement qui ont conduit à l'implémentation d'un circuit robuste.
Afin de valider nos choix architecturaux ainsi que notre méthodologie de conception, un prototype a été fabriqué et caractérisé dans notre laboratoire de test.
Les performances mesurées montrent que le prototype atteint une résolution effective de 11-bit dans une bande passante de 40MHz tout en consommant 87.3mW. L'efficacité énergétique de notre circuit est donc de 533fJ/conversion-step. Cette valeur est supérieure à notre objectif de départ mais reste comparable face aux solutions pipeline commerciales disponibles sur le marché. D'autre part, la mesure de la fonction de transfert anti-repliement du modulateur montre que l'atténuation du filtre de boucle est équivalente à celle que nous obtiendrions avec un filtre Butterworth du $3^{ième}$ ordre placé devant le CAN. Cet avantage combiné à l'impédance d'entrée résistive du modulateur simplifie grandement la conception du circuit de conditionnement situé devant le CAN $\Delta\Sigma$.

Enfin, l'écart de performance observé par rapport au cahier des charges initial a été analysé en détail et son origine a été clairement identifiée. Des solutions sont proposées pour améliorer les performances d'un futur prototype.

Mots clés : Delta-Sigma, pipeline, passe-bas, CMOS, large bande, haute résolution, temps continu

Design of Wideband High-Resolution Low-Pass Continuous-Time Delta-Sigma Modulators in CMOS process

ABSTRACT:

The market of A/D converters can be segmented in two categories. From one side we distinguish the Intellectual Property (IP) blocks that are generally optimized for a specific application. On the other side, the general-purpose discrete Integrated Circuits (ICs) that are designed such as they could be used in different applications.
This thesis work deals with the second category. It is part of a research and development program initiated in 2010 in the European project FP7 SACRA, whose purpose was to study the feasibility of a delta-sigma ($\Delta\Sigma$) analog-to-digital converter that could compete with the pipeline architecture for applications that require high bandwidth (≥10MHz) and high resolution (>10-bit) such as medical imaging, wireless and wireline communications, video or instrumentation.

Currently, the pipeline is still largely predominant for such applications and the few commercial wideband solutions based on a $\Delta\Sigma$ architecture have a signal bandwidth limited to 10 MHz or 25 MHz while consuming respectively 100mW and 20mW for an ENOB around 12-bit.

This manuscript summarizes the design, fabrication and measurement of a low-pass CT $\Delta\Sigma$ modulator with a signal bandwidth of 40MHz, while targeting an effective resolution of 12-bit and a power consumption of less than 100mW.
To achieve our goal we have analyzed in detail the $\Delta\Sigma$ modulators architectures reported in the literature over the past ten years. This first step helped us to identify trends in broadband and high-resolution applications. Based on this study and our experience, we proposed architecture built around a 5^{th}-order continuous-time loop filter and a 5-bit quantizer. This unusual choice of resolution facilitates the PCB-level integration because the requirements on the clock jitter are relaxed.
Moreover, the design constraints on the loop filter of the modulator itself are also reduced. The impact of this architectural choice on the power consumption of the modulator was analyzed and a solution was proposed to optimize the tradeoff between the performance and the energy efficiency of the modulator.
An oversampling rate (OSR) of 8 was chosen to minimize the clock speed which results in a reduction of the power consumption of the modulator and the associated decimation filter. The stability problems associated with the use of a low OSR are resolved by injecting a fraction of the input signal to various nodes of the loop filter.
To facilitate the design of each sub-block of the modulator, a behavioral model of the imperfections that affects the loop filter, the quantizer and the feedback DACs, was built and simulated in Matlab. This approach allowed us to derive all the specifications of the modulator sub-blocks.
The implementation of each sub-block of the modulator in 65nm CMOS is detailed with emphasis on design criteria that led to the implementation of a robust system.
To validate our architectural choice and the proposed design methodology, a prototype was fabricated and characterized in our lab.
Measurements prove that the prototype achieves 11-bit ENOB in a signal bandwidth of 40MHz while consuming 87.3mW. It leads to a figure of merit of 533fJ/conversion-step. This value is higher than our goal but is still comparable to the FoM obtained with pipeline of the market. However, we showed that the anti-aliasing transfer function provided by the CT loop filter is equivalent to what would be obtained by adding a 3^{rd} order Butterworth filter in front of the ADC. This advantage combined with the resistive input impedance of the modulator greatly simplifies the circuit design of the front $\Delta\Sigma$ ADC front-end and makes it an attractive alternative to the pipeline architecture.

Finally, the performance gap compared to original specifications was analyzed in detail and its origin was clearly identified. Solutions are proposed to improve the performance of a future prototype.

Keywords : Delta-Sigma, pipeline, low-pass, CMOS, wideband, high resolution, continuous-time

Résumé étendu

Introduction

Le marché des Convertisseurs Analogique-Numérique (CAN) peut être segmenté en deux catégories. D'une part nous distinguons les blocs de propriété intellectuelle (IP) qui sont généralement optimisés pour une application spécifique. Et d'autre part, les circuits intégrés à usage général, conçus pour répondre aux besoins d'une large gamme d'application.
Ce travail de thèse se focalise sur la deuxième catégorie de composant dont le marché est dominé par les quatre fabricants cités dans le tableau 1.
L'évolution agressive de la technologie CMOS dictée par la loi de Moore a atteint un point qui permet de mettre en œuvre des CAN $\Delta\Sigma$ à temps continu rapides et à usage général [1] [2]. Ces rares produits disponibles sur le marché, intègrent dans un boîtier très compact et à faible coût : un modulateur $\Delta\Sigma$ à temps continu, un synthétiseur de fréquence, un filtre de décimation numérique et une référence de tension. Ils ont des performances exceptionnelles tout en consommant peu d'énergie. Cependant, leur bande passante est limitée à 10 MHz [2] et 25 MHz [1].

Les travaux présentés dans ce document s'inscrivent dans le cadre d'un programme de recherche et de développement qui a été initié dans le projet FP7 SACRA et dont le but était d'étudier la faisabilité d'un CAN $\Delta\Sigma$ pouvant rivaliser avec l'architecture pipeline pour les applications qui nécessitent un faible niveau de bruit (SNR=12-bit), une faible distorsion (THD>14-bit) et une bande passante de signal supérieure à 25MHz.
Afin de comparer de façon réaliste notre circuit aux produits disponibles sur le marché [1] [2], nous avons conçu un prototype qui embarque sur le même substrat de silicium, une référence de tension, un filtre de décimation et tous les circuits qui compensent les imperfections des composants analogiques. Un schéma simplifié du CAN est représenté sur la Figure 1. Les travaux présentés dans ce manuscrit se concentrent sur la conception et la caractérisation du modulateur $\Delta\Sigma$ à temps continu uniquement et plus précisément:

- Un filtre de boucle du $5^{ième}$ ordre à temps continu ainsi q'un quantificateur et un DAC 5-bit sur-échantillonnés d'un facteur 8.

- Un circuit qui compense les variations des constantes de temps des intégrateurs, un circuit qui corrige le décalage en tension dans les comparateurs du quantificateur flash 5-bit.

- Des « buffers » rapides pour faire l'acquisition de la sortie du modulateur à 640MHz.

Un flot de conception incluant la modélisation des principaux défauts du modulateur a été introduit afin de faciliter son implémentation au niveau transistor.
Les résultats de mesures ont été détaillés et l'écart par rapport au cahier des charges a été analysé en profondeur.

Tableau 1. Répartition des revenus entre les leaders mondiaux de la conversion de données entre 2010 and 2011

Société	2011 RANG	2011 $M	2011 part	2010 RANG	2010 $M	2010 part
Analog Devices	1	1,312	48.5%	1	1,422	47.5%
Texas Instruments	2	625	23.1%	2	659	22%
Maxim Integrated	3	185	6.8%	3	197	6.6%
Linear Technology	4	125	4.6%	4	142	4.7%

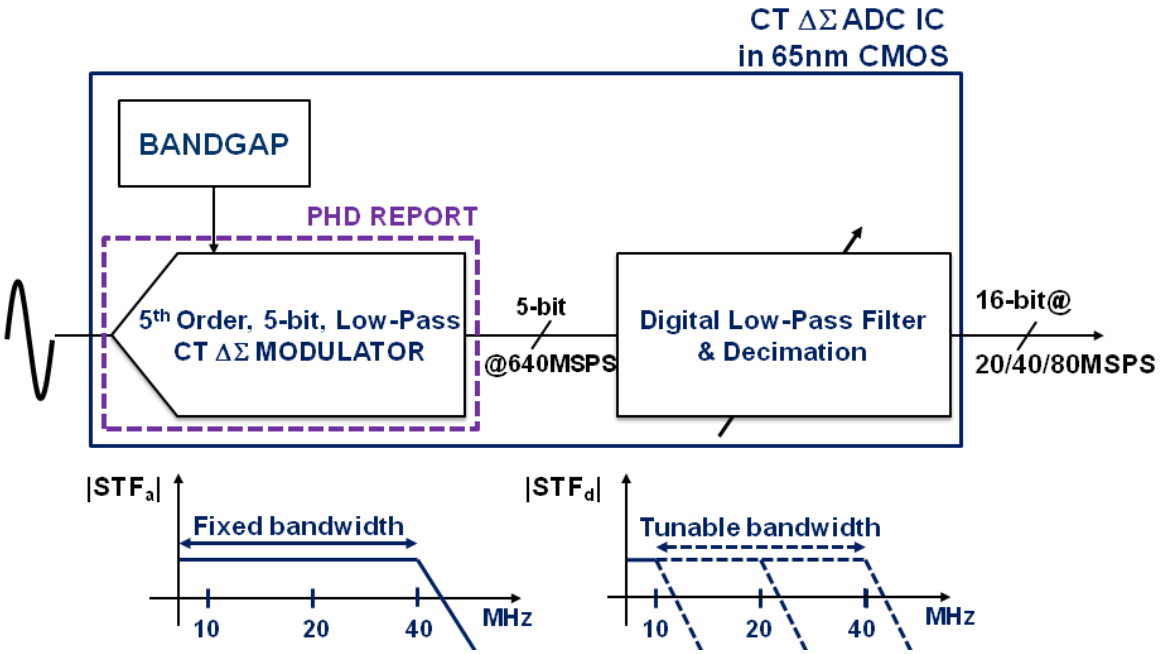

Figure 1. Architecture du convertisseur ΔΣ à temps continu implémenté en technologie CMOS 65nm.

Architecture du modulateur ΔΣ et spécifications visées

Tableau 2. Spécifications du CAN ΔΣ

PARAMETERS	VALUE	UNIT
Taux de sur-échantillonnage	8	_
Bande passante	40	MHz
Fréquence d'échantillonnage	640	MHz
SNR	74	dBc
THD	86	dBc
SNDR	74	dBc
ENOB	12	Bit
Power	<100	mW
FoM	<305	fJ/conversion-step
Technologie CMOS	65nm	_

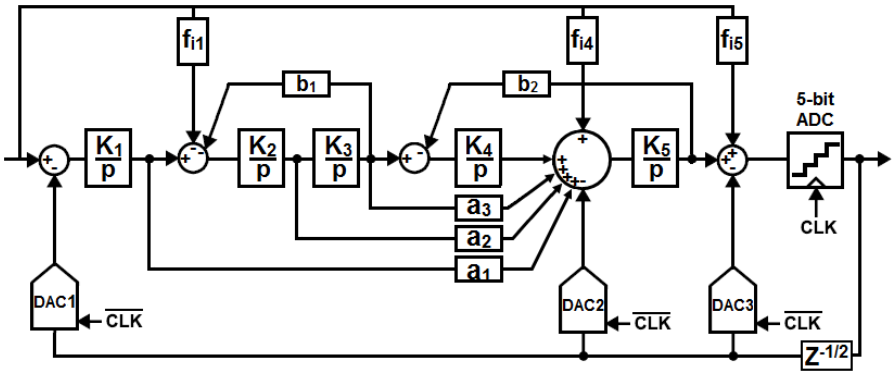

Figure 2. Architecture du modulateur ΔΣ à temps continu.

Les spécifications du CAN ΔΣ sont résumées dans le tableau 2. Le circuit vise des applications qui exigent simultanément une bande passante élevée, une haute résolution ainsi qu'une faible consommation de puissance, comme les communications filaires et sans fil, l'imagerie médicale, la vidéo ou encore l'instrumentation. L'architecture utilisée pour répondre à ces spécifications est représentée sur la Figure 2. Un OSR de seulement 8 est choisie pour réduire au maximum les contraintes de vitesse sur le filtre de boucle et le quantificateur multi-niveaux, ce qui se traduit par une faible consommation d'énergie de la partie analogique. La bande passante maximale du signal d'entrée étant de 40MHz, le modulateur ΔΣ est cadencé à une fréquence d'horloge de 640MHz. La valeur de l'OSR a été choisie en gardant à l'esprit la consommation d'énergie du filtre de décimation qui peut être aussi importante que le modulateur lui-même [2]. Par exemple, le modulateur large bande décrit dans [3] a une très bonne efficacité énergétique, mais la fréquence d'horloge de 3.6GHz reporte un sérieux défi sur la conception du filtre de décimation. D'autre part, la réduction de la vitesse de commutation de la partie numérique réduit la diaphonie à travers le substrat.
Pour compenser la faible valeur d'OSR, une fonction de transfert en bruit (NTF) du $5^{ième}$ ordre avec un gain maximal (Q_{max}) de 12dB et un quantificateur 5-bit sont combinés pour maintenir le niveau du bruit de quantification en dessous du plancher de bruit du CAN, dominé par le bruit thermique du modulateur. Une valeur élevée de Q_{max} est également nécessaire pour améliorer la stabilité du modulateur à faible OSR [4]. Les coefficients directs f_{i1}, f_{i4} et f_{i5} permettent de réduire fortement l'excursion de tension en sortie des intégrateurs, comme le montre le tableau 3 d'une part et améliore la dynamique du modulateur, comme illustré sur la Figure 3 (a) d'autre part. L'indice de modulation est de 0,85. Cadencé à 640MHz, le modulateur ΔΣ réalise un rapport signal à bruit de quantification supérieure à 90dBc dans une bande passante de 40 MHz.

Tableau 3. Amplitude de l'excursion de tension en sortie des intégrateurs

PARAMETERS	sans Feed-in	avec Feed-in
Fréquence du signal d'entrée	1MHz	1MHz
Amplitude du signal d'entrée	-4.4dBFS	-4.4dBFS
Référence du quantificateur	800mV	800mV
Excursion maximale de sortie		
Intégrateur 1	±261mV	±235mV
Intégrateur 2	±247mV	±67mV
Intégrateur 3	±313mV	±52mV
Intégrateur 4	±450mV	±48mV
Intégrateur 5	±766mV	±421mV

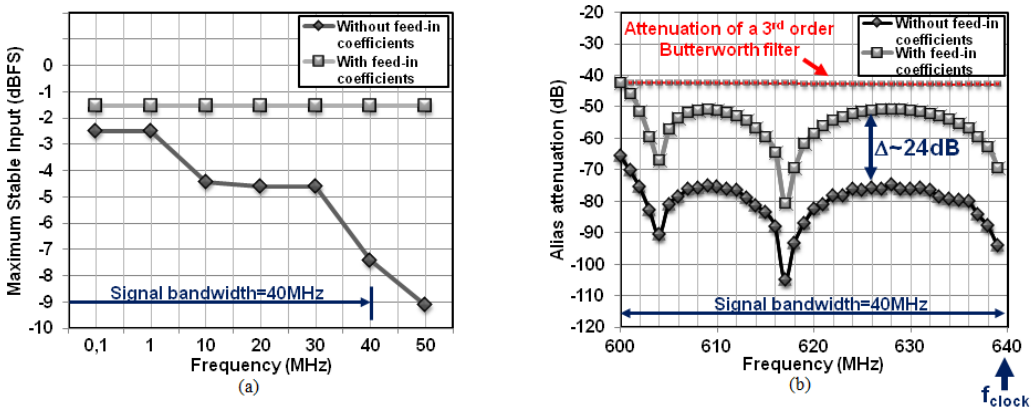

Figure 3. Effet des coefficients directs (a) sur la tension d'entrée maximum, (b) la fonction de transfert anti-repliement du modulateur.

Bien que les coefficients directs réduisent la dynamique des signaux à l'intérieur du filtre de boucle, il est rarement rappelé que c'est au prix d'une fonction de transfert anti-repliement moins efficace. Ce compromis est illustré sur la Figure 3 (b).
Le scénario de repliement le plus défavorable (le moins d'atténuation) arrive lorsqu'une interférence se situe à 600MHz. Dans ce cas, ce signal serait atténué de 42.3dB. A titre indicatif, la fonction de transfert anti-repliement intrinsèque du modulateur fournit la même atténuation à 600MHz qu'un filtre Butterworth du troisième ordre ayant une atténuation maximale de 1 dB en bord de bande.

Bien qu'un quantificateur 4-bit soit la solution la plus utilisée dans les modulateurs à large bande passante [2,5], augmenter la résolution à 5-bit réduit d'avantage la dynamique des signaux à l'intérieur du filtre de boucle, améliorant ainsi le compromis entre la puissance et la distorsion. Les autres avantages sont un meilleur compromis entre la stabilité et la dynamique du CAN. La sensibilité du CNA principale à la gigue d'horloge est également relaxée, ce qui permet de réduire les contraintes sur le bruit de phase de l'horloge externe.
Afin de réduire la consommation de courant et la capacité d'entrée du quantificateur 5-bit, les composants à l'intérieur des comparateurs sont intentionnellement dimensionnés avec une petite taille et le décalage en tension résultant est calibré. Un algorithme DWA est choisi pour réduire le bruit et la distorsion induits par le désappariement des cellules de courant unitaires du CNA principale.
Un retard de boucle correspondant à une demi période d'horloge est inséré dans la boucle de retour du modulateur afin d'absorber à la fois, la latence de la DWA et le temps de réponse du quantificateur, réduisant ainsi la probabilité de métastabilité.
Pour réduire la charge capacitive à la masse virtuelle du 5^{ième} intégrateur, les tailles des cellules unitaires des deuxième et troisième CNA (DAC2 et DAC3) sont réduites par rapport au premier CNA (DAC1). En conséquence, la technique DWA est également appliquée aux CNA secondaires pour réduire leur distorsion harmonique, faiblement atténuées par le filtre de boucle à faible OSR.

Les performances visées sont comparées à l'état de l'art sur la Figure 4.

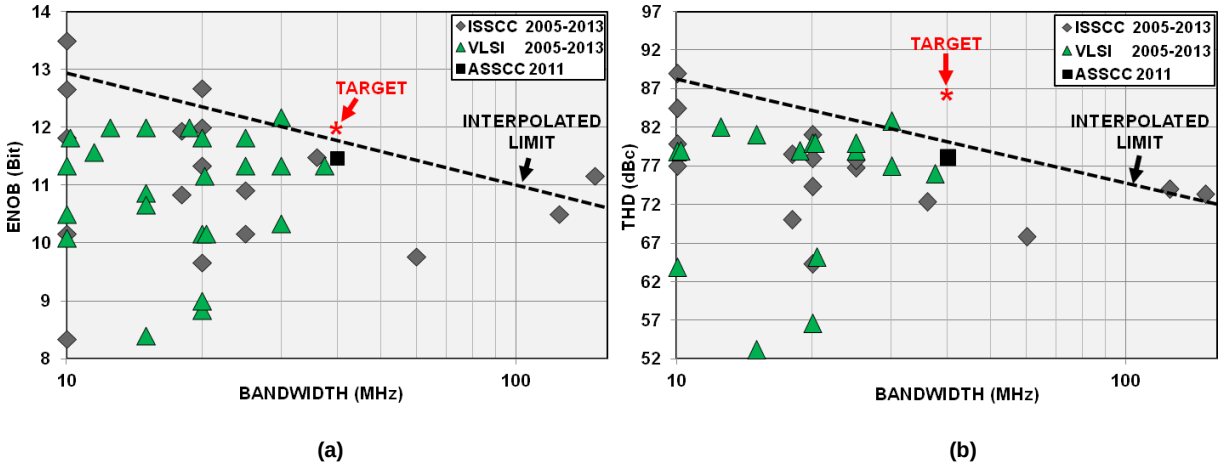

Figure 4. Comparaison des performances visées par rapport à l'état de l'art (a) THD, (b) ENOB.

Simulation système

Les principaux blocs du modulateur se composent du filtre de boucle, du quantificateur et des CNA de retour qui se distinguent entre le CNA de la boucle de retour principale dont les imperfections ne sont pas mises en forme par le filtre de boucle et les CNA secondaires dont les imperfections sont mises en forme par le filtre de boucle.
Le but de l'étude système est de quantifier avec une précision acceptable et dans un délai raisonnable, l'impact des non-idéalités qui affectent la performance du modulateur ΔΣ. Cette information sera exploitée pour définir les spécifications des sous-blocs lors de leur implémentation en technologie CMOS 65nm. La modélisation comportementale et la simulation de l'impact des non-idéalités sont effectuées avec Matlab [6]. Les coefficients du modulateur ont été calculés avec la boîte à outils de Schreier [7] et la procédure de conversion utilisée pour obtenir les coefficients du modulateur à temps continu est détaillée dans [2].
La fonction de transfert en signal (STF) et la fonction de transfert en bruit (NTF) du modulateur idéal sont présentées sur la Figure 5 et la Figure 6 respectivement. Alors que la STF a une ondulation à l'intérieur de la bande qui est inférieure à 0.1dB, son dépassement s'étend sur plus d'une décade en dehors de la bande passante du signal, avec une valeur maximale de 14 dB à 478MHz.
Une attention particulière doit être accordée pour les applications où le signal est reçu en présence de brouilleurs. Même si le filtre anti-repliement intrinsèque du modulateur fournit suffisamment d'atténuation contre les interférences susceptibles de se replier dans la bande passante du signal, certain types de modulateurs nécessitent un filtre pour réduire le dépassement de la STF [8]. Le dépassement de la STF n'est pas étudié dans ce travail puisque ce problème est bien connu dans la littérature [9] et de nombreuses solutions ont été proposées pour réduire cet effet [10] [11] [12] [13].
Les principales caractéristiques des sous-blocs du modulateur sont résumées dans le tableau 4. Le budget de bruit du modulateur a été fait tel que le bruit thermique soit la source de bruit dominante. Ce choix impose une gigue d'horloge de 450fs rms et peut être obtenue avec un synthétiseur de fréquence consommant environ 12mW [2].
Une simulation comportementale qui tient compte de toutes les non-idéalités est illustrée sur la Figure 7.

Tableau 4. Spécifications des sous-blocs du modulateur ΔΣ

PARAMETERS	VALUE	UNIT
Filtre de boucle		
Erreur sur les coefficients (σ)	1	%
Erreur sur la fréquence gain unité	±2	%
PGB du 1er amplificateur	6	f_s
Gain DC du 1er amplificateur	≥40	dB
CNA Principale		
Désappariement de courant	0.2	%
Gigue d'horloge	450	fs
Impédance de sortie	>1	MΩ
Quantificateur		
Offset (σ)	2	mV
Hysteresis	>2	mV
Constante de temps du "latch"	1%	T_s
Budget de bruit		
Quantification	89	dBc
Thermique	77.4	dBc
Gigue d'horloge	86.5	dBc
Filtre de décimation	91.8	dBc
SNDR total (marge de 2dB)	**76.5**	**dBc**

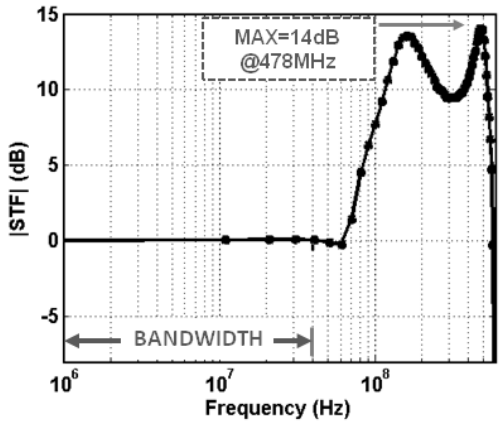

Figure 5. Fonction de transfert en signal simulée avec une sinusoïde d'amplitude–12dBFS et une fréquence qui varie de 1MHz up to 600MHz.

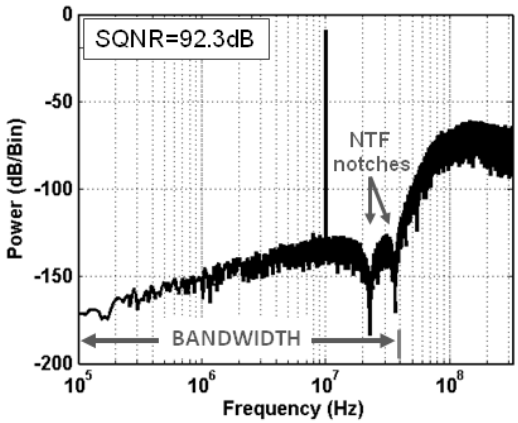

Figure 6. Densité spectrale de puissance en sortie du modulateur ΔΣ (2^{16} FFT points) pour un signal sinusoïdale d'entrée dont la puissance et la fréquence valent respectivement -1.1dBFS et 10MHz.

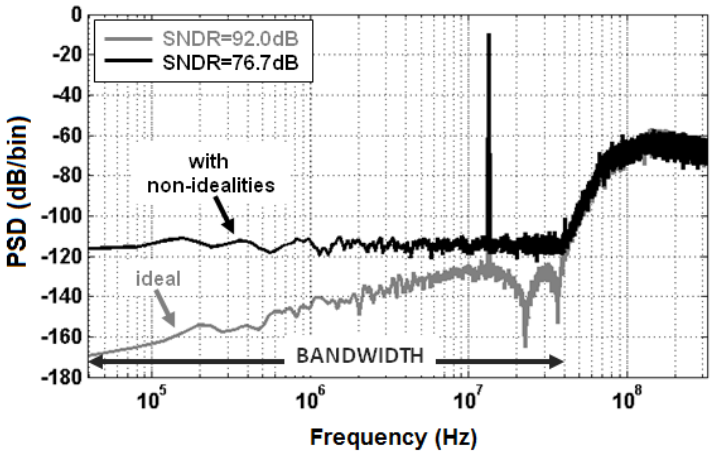

Figure 7. Densité spectrale de puissance en sortie du modulateur avec et sans les imperfections du modulateur ΔΣ (V_{in}=-1.8dBFS et f_{in}=13.32MHz).

Implémentation en technologie CMOS 65nm

Le modulateur ΔΣ a été implémenté dans un procédé CMOS 65nm de ST Microelectronics. Ce procédé de fabrication utilise un substrat de type P et offre plusieurs options telles que des transistors à faible tension de seuil, des condensateurs MIM ou la possibilité d'isoler les caissons des transistors NMOS du substrat. Cette dernière technique est largement utilisée dans ce travail pour isoler les blocs numériques de la partie analogique.
Tous les sous-blocs du modulateur sont implémentés avec des circuits différentiels afin de minimiser le bruit de mode commun, améliorer le taux de réjection d'alimentation (PSRR) et réduire la distorsion harmonique d'ordre pair. Les circuits analogiques sont conçus pour avoir une performance optimale à une tension d'alimentation nominale de 1,2 V et de telle sorte que le modulateur reste fonctionnel avec une fluctuation d'alimentation de ± 10%.

Filtre de boucle

La Figure 8 détaille l'implémentation du filtre de boucle à temps continu. Les intégrateurs sont de type OPAMP-RC plutôt que Gm-C car la performance de linéarité requise est sévère. Le coefficient direct f_{i5} est réalisé par le rapport de la capacité C_{f5} et de la capacité de rétroaction du dernier intégrateur C_5, ce qui évite l'utilisation d'un additionneur. Les autres coefficients sont implémentés par des rapports de résistance. Tous les composants passifs utilisés pour implémenter les coefficients sont dimensionnés pour répondre à la contrainte d'appariement de 1% indiqué dans le tableau 4.
Le plancher de bruit du modulateur est dominé par le bruit thermique du frontal qui se compose des résistances d'entrée, de l'amplificateur opérationnel de l'intégrateur principal et des sources de courant unitaires du CNA principale.

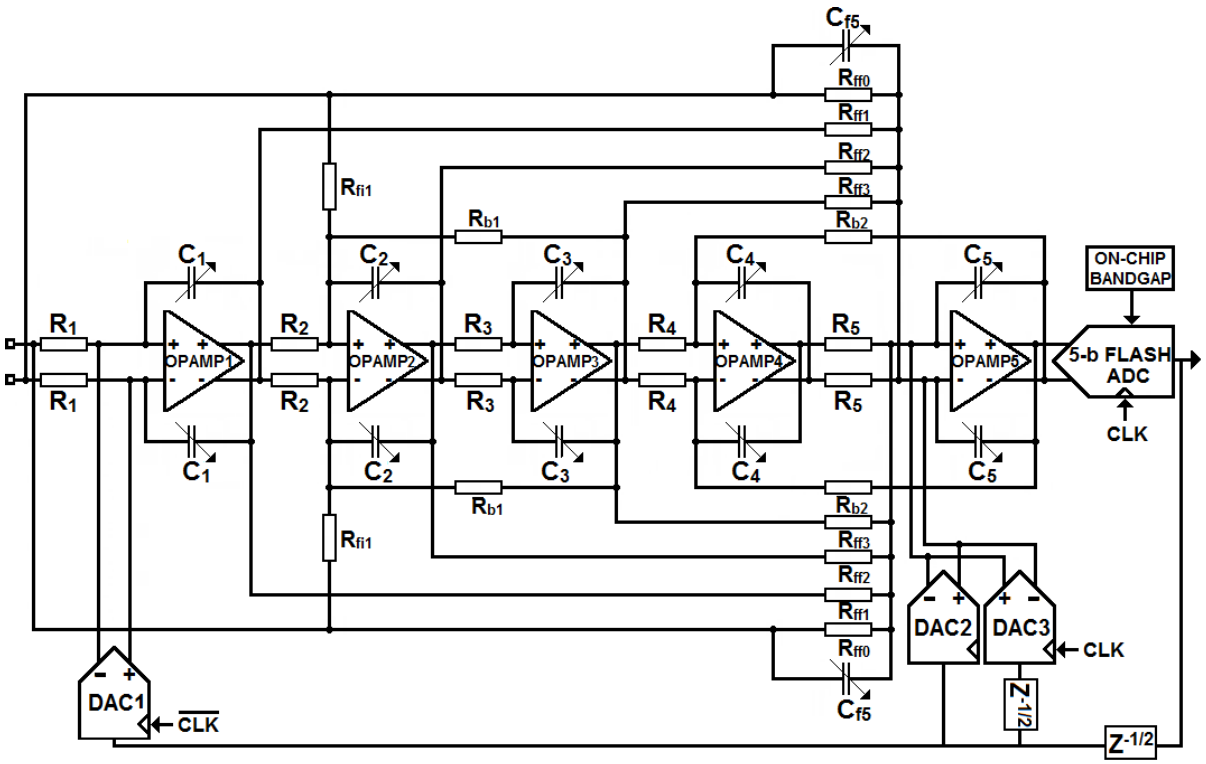

Figure 8. Architecture simplifiée du modulateur ΔΣ à temps continu.

La distorsion visée (THD> 14-bit) impose une forte contrainte de linéarité sur le frontal du modulateur. L'excursion de tension sur la masse virtuelle du premier amplificateur opérationnel (opamp1) due à son produit gain-bande (PGB) fini est la principale source de distorsion. Habituellement, la valeur du PGB du premier amplificateur opérationnel est choisi égale à la fréquence d'échantillonnage [5]. Cette stratégie de conception garantit une très bonne efficacité énergétique au détriment de la performance de linéarité car la réduction du PGB augmente l'excursion de tension à la masse virtuelle du premier

amplificateur. Même si le délai dans le filtre de boucle induit par le PGB fini est rigoureusement compensé par un ajustement de la valeur des composants [5], la stabilité du modulateur ne peut pas être garantie avec un rendement élevé lorsque nous prenons en compte les variations du procédé de fabrication. Comme le montre la Figure 9, le principal intégrateur utilise un amplificateur à 4 étages dont le PGB et la marge de phase valent respectivement 3.9 GHz et 88 °, ce qui permet de réduire simultanément la distorsion et le délai dans le filtre de boucle.
La dernière transconductance (gm4) utilise des transistors de longueur minimale pour augmenter la marge de phase tout en réduisant la consommation de puissance. L'amplificateur principal consomme 20 mA et sa composante harmonique du troisième ordre à la sortie du modulateur est 100 dB en dessous de la tension pleine échelle du modulateur. Ce choix garantit que le taux de distorsion harmonique soit dominé par le désappariement de courant dans le CNA principale. Les performances de l'amplificateur sont résumées dans le tableau 5.
Le circuit représenté sur la Figure 10 [14] est utilisé pour compenser la variation absolue de la constante de temps RC des intégrateurs qui peut atteindre ± 35% dans ce procédé. Les condensateurs de rétroaction de chaque intégrateur sont ajustés à la valeur idéale avec une précision de ± 2%.

Tableau 5. Principaux paramètres de l'amplificateur principal

PARAMETER	VALUE	UNIT
Gain DC	45	dB
Produit gain-bande en boucle ouverte	3.9	GHz
Marge de phase	88	°
Densité de bruit ramenée à l'entrée @10KHz @1MHz @40MHz	 30 3.2 1.3	 $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
Bruit ramené à l'entrée et Intégré dans [10KHz:40MHz]	11.6	µVrms
Décalage de tension (±3σ)	±2	mV
HD3*	100	dBFS
Tension d'alimentation	1.2	V
Consommation de puissance	24	mW

***simulé à l'intérieur de la boucle ΔΣ avec une sinusoïde d'entrée à 10MHz**

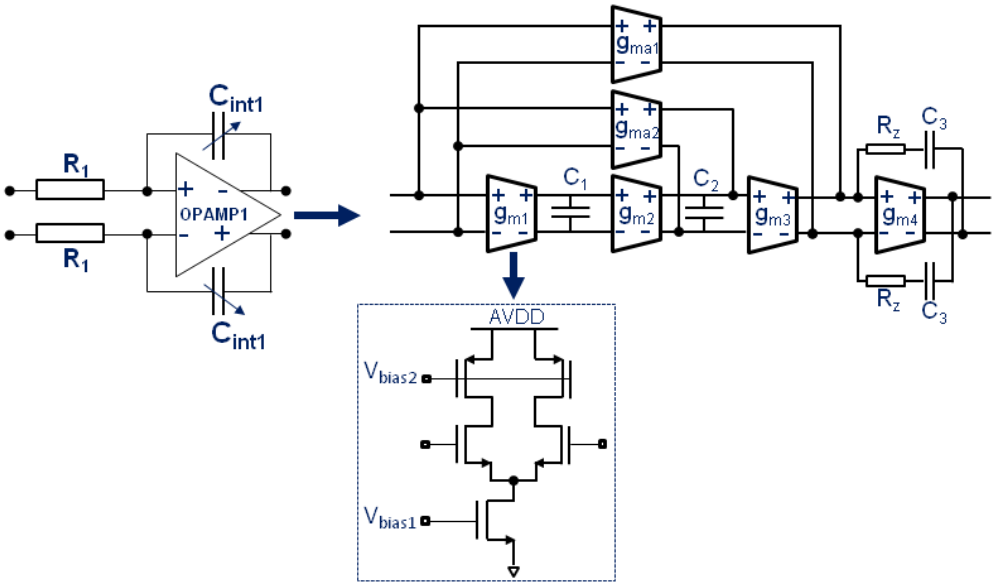

Figure 9. Schéma simplifié de l'amplificateur utilisé dans le frontal du modulateur.

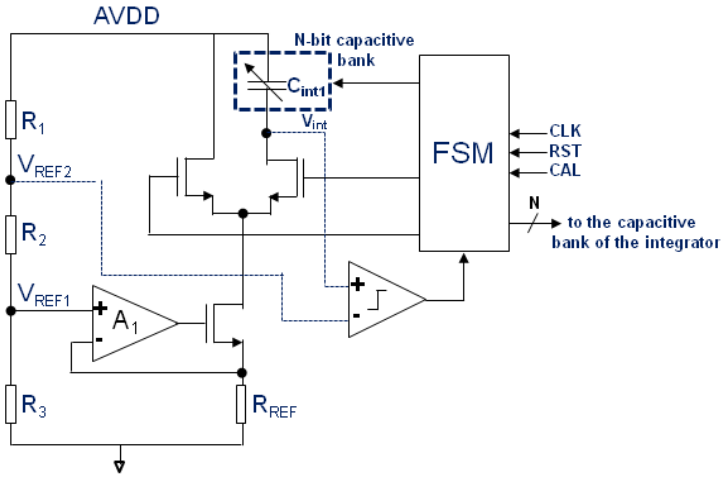

Figure 10. Circuit utilisé pour corriger les variations des constantes de temps des intégrateurs [14].

CNA dans la boucle de retour

CNA principale

L'architecture de la cellule de courant unitaire utilisée dans le CNA principale est détaillée sur la Figure 11. Elle se compose d'une source de courant cascode régulée avec une paire de commutateurs NMOS et deux sources de courant PMOS qui fixent le mode commun à la masse virtuelle de l'amplificateur (opamp1).
Les commutateurs sont dimensionnés de manière à minimiser le délai de commutation ainsi que la capacité de sortie de la cellule de courant. Une conception soignée du circuit de distribution d'horloge et des bascules TSPC [15] qui pilotent les commutateurs a conduit à une valeur de gigue additive de seulement 137fs$_{rms}$. Cette valeur laisse une marge suffisante pour tenir compte de la gigue de l'horloge externe.
Le PGB de l'amplificateur auxiliaire est optimisé pour augmenter l'impédance de sortie du CNA sur une large gamme de fréquences. Une valeur d'impédance plus élevée que 3MΩ est obtenue jusqu'en fin de bande (40MHz) ce qui rend négligeable le mécanisme de distorsion due au PGB fini du premier amplificateur (opamp1).
Le bruit du circuit de polarisation est filtré par un filtre RC intégré sur la puce. Le pôle de ce filtre est fixé à 200KHz mais sa valeur peut être réduite en connectant un condensateur de découplage à l'extérieur du circuit comme illustré sur la Figure 12.
La référence de tension utilisée est une version CMOS du circuit BiCMOS proposé dans [16]. Le transistor bipolaire a été implémenté avec un transistor MOS vertical.
La capacité de sortie du CAN a une valeur de 464fF dont 16% correspondent à la capacité intrinsèque des cellules de courant et 84% à la capacité de la ligne d'interconnexion des cellules de courant à la masse virtuelle de l'amplificateur. Les principales caractéristiques du CNA principale sont résumées dans le tableau 6.

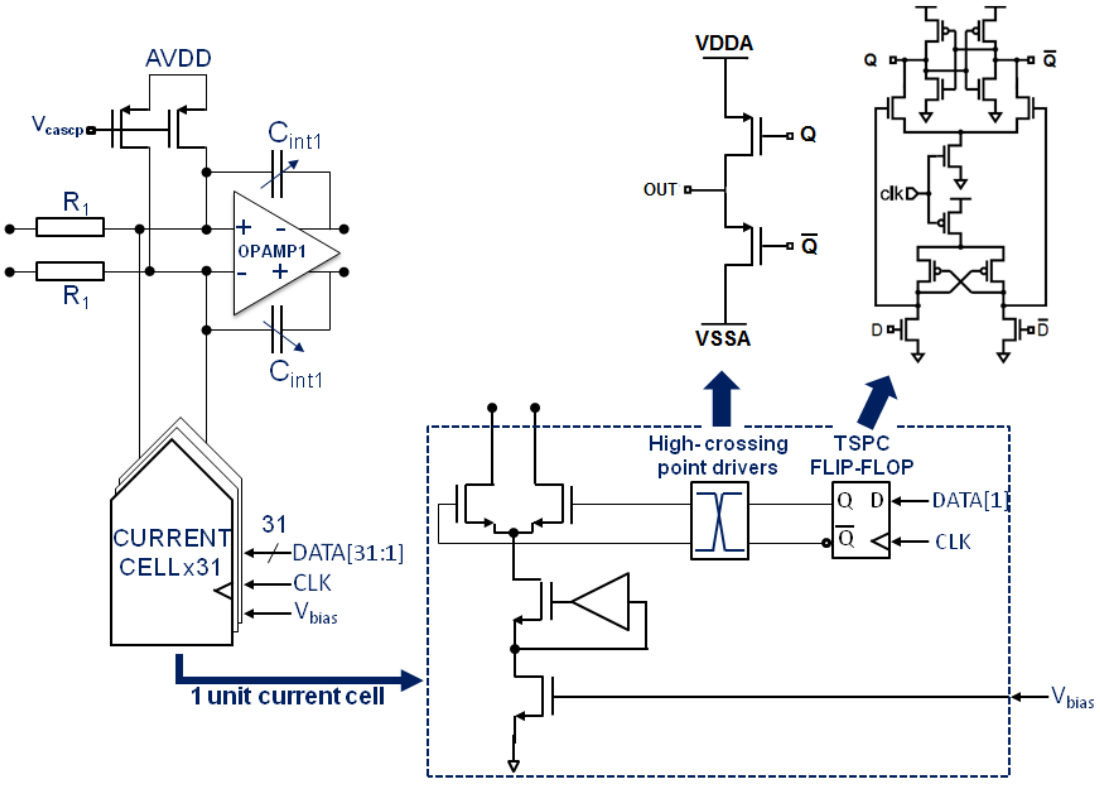

Figure 11. Schéma de la cellule de courant unitaire utilisée dans le CAN principale.

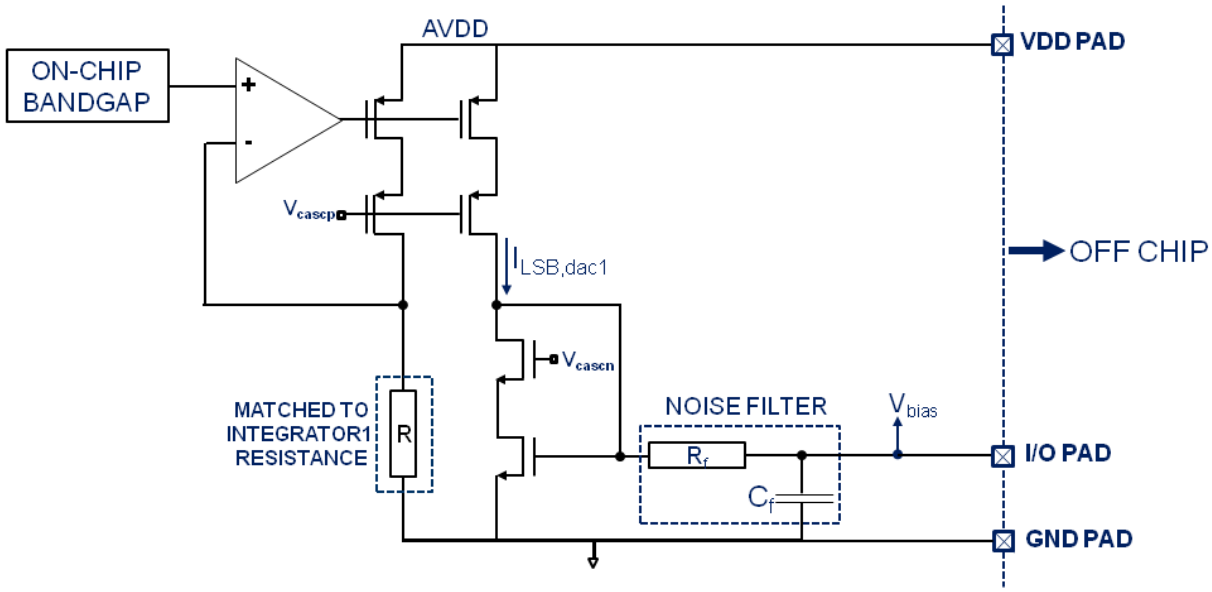

Figure 12. Schéma du circuit de polarisation du CAN principale.

Tableau 6. Performance typique du CAN principale

PARAMETRES	VALEUR	UNITE
Nombre de cellule unitaire	31	_
Résolution	50	µA
Impédance@40MHz	3.1	MΩ
Bruit ramené à l'entrée*	6	µV rms
Ecart type de l'appariement (σ)	0.2	%
Gigue d'horloge	137	fs
Tension d'alimentation analogique numérique	 1.2 1.0	 V V
Consommation de puissance (31cellules) analogique numérique	 3.84 1.1	 mW mW

CNAs secondaires

L'application de la DWA aux CNA secondaires permet de réduire la taille de leurs cellules de courant unitaires ce qui permet de réduire la surface du circuit. Cette stratégie a également l'avantage de réduire la capacité de sortie des CNA secondaires qui sont connectés à la masse virtuelle du 5^{ième} intégrateur. Pour un PGB donné, la consommation du 5^{ième} intégrateur est donc réduite.
Etant donné que les contraintes sur l'impédance de sortie des CNA secondaires sont réduites par rapport au CNA principale, les cellules de courant unitaires sont implémentées avec des sources de courant cascode régulé comme représenté sur la Figure 13.
La valeur totale de la capacité de sortie des CNA secondaires est de 239fF dont 37% proviennent de la capacité intrinsèque des cellules de courant et 63% sont dus à la ligne de métal qui relie les cellules de courant à la masse virtuelle du dernier intégrateur.

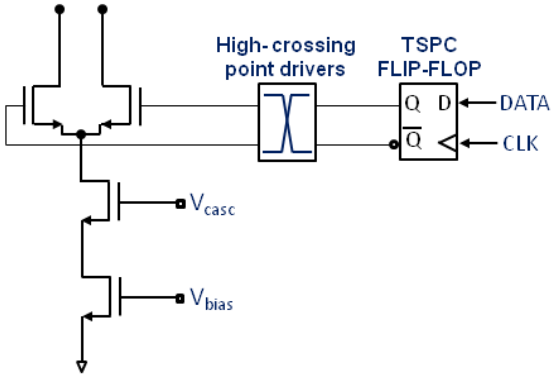

Figure 13. Cellule de courant unitaire utilisée dans les CAN secondaires.

Quantificateur

Le schéma simplifié du quantificateur flash est représenté sur la Figure 14. Il se compose de trente et un comparateurs qui convertissent la sortie du filtre de boucle en un code thermométrique. Deux comparateurs (non représentés) sont rajoutés afin de détecter les excursions de signaux qui pourraient saturer le quantificateur. Le code à 2-bit délivré par ces comparateurs peut être exploité par un amplificateur à gain variable (AGC) pour ramener l'excursion de la tension d'entrée du modulateur à l'intérieur de la dynamique du quantificateur.
Les tensions de seuil VREF[k] des comparateurs sont générées par un diviseur résistif qui est alimenté par une référence de tension externe à la puce. Le schéma d'un comparateur est détaillé sur la Figure 15. Un commutateur CMOS déconnecte chaque comparateur du filtre de boucle pendant la procédure de calibration de la tension de décalage qui a lieu après la mise sous tension du modulateur $\Delta\Sigma$. Lorsque la calibration n'est pas activée, la résistance non-nulle de l'interrupteur et la capacité d'entrée du quantificateur créent un pôle dont la valeur est choisie très grande par rapport à la fréquence d'échantillonnage du modulateur afin de préserver sa stabilité. Les contraintes sur le bruit et la distorsion du commutateur sont fortement relaxées car ils sont mis en forme par le filtre de boucle du 5^{ième} ordre.
Pour chaque comparateur, la valeur de la tension de décalage est estimée par une boucle de rétroaction qui est constituée d'un compteur/intégrateur et un CNA. Pour chaque code du CNA, la sortie du comparateur est intégrée durant plusieurs fractions de la période d'horloge afin de réduire l'influence du bruit. Quand la valeur moyenne en sortie du comparateur est égale ou supérieure à zéro, le compteur s'arrête et fixe le courant de sortie du CNA à une valeur qui compense la tension de décalage avec une précision qui dépend de la résolution du CNA. Par rapport à [2], chaque comparateur est calibré autour de son seuil de basculement plutôt qu'autour de sa tension de mode commun d'entrée ce qui a l'avantage de corriger les décalages de tension statique et dynamique. Comme tous les comparateurs sont calibrés en parallèle, le temps de calibration maximale n'est que de 1.6 µs pour les 33 comparateurs. Si l'application le permet, la phase de calibration peut être répétée pendant la durée de vie du circuit afin de compenser la variation de la tension de décalage due au vieillissement des composants.
Le schéma du préamplificateur et du « latch » de sortie sont présentées sur la Figure 16. Le préamplificateur utilise une double paire différentielle [17] avec une charge PMOS et un commutateur

de réinitialisation [18]. Par rapport à l'architecture proposée dans [2], notre préamplificateur utilise une charge qui ne commute pas, ce qui réduit fortement l'effet du « kickback » à la sortie du filtre de boucle et du pont diviseur.
Les portes logiques utilisées pour générer les différentes phases de comparaison sont présentés sur la Figure 16. Lorsque le commutateur de remise à zéro est ouvert, la différence de tension entre la sortie du filtre de boucle et la tension de référence est effectuée. Immédiatement après, les commutateurs de sortie sont ouverts et le « latch » est activé. Le courant de polarisation de la source de courant dynamique PMOS est choisi de sorte à réduire la métastabilité et laisser suffisamment de temps à la DWA pour faire ses calculs.

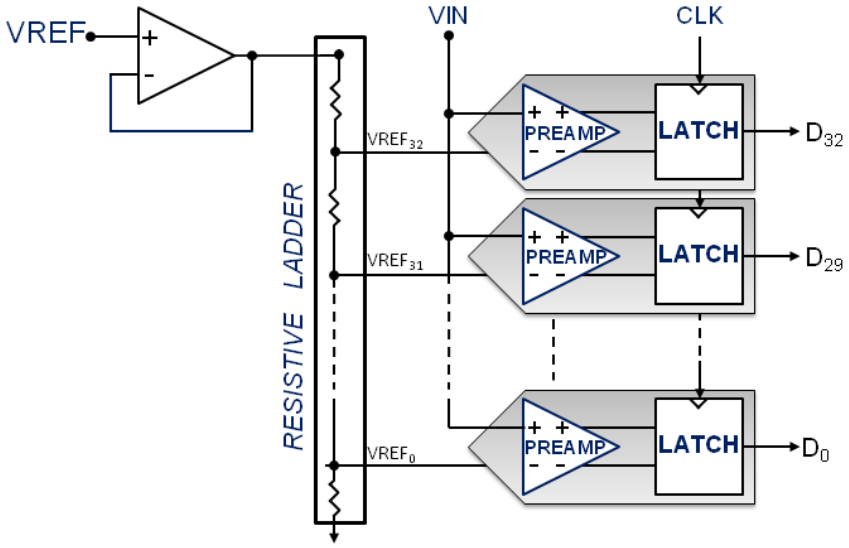

Figure 14. Schéma simplifié du quantificateur FLASH.

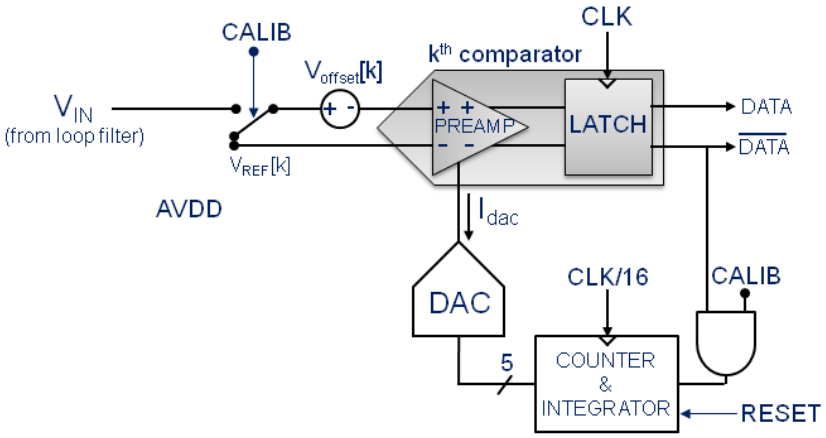

Figure 15. Schéma d'un comparateur.

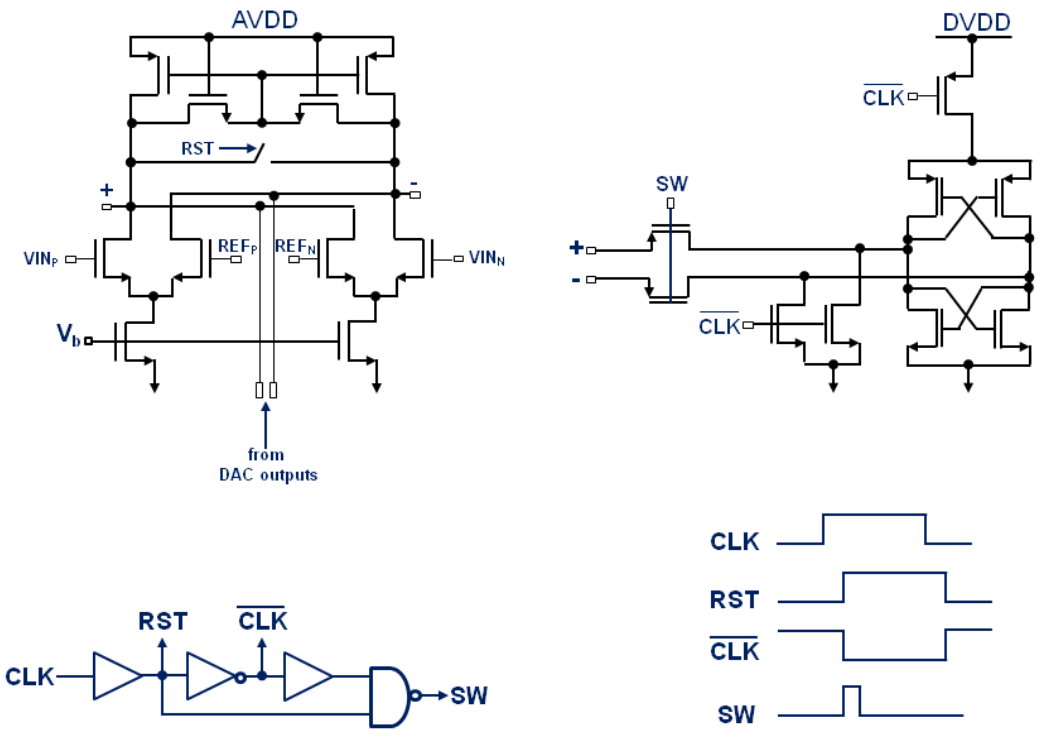

Figure 16. Schéma des circuits utilisés dans le comparateur.

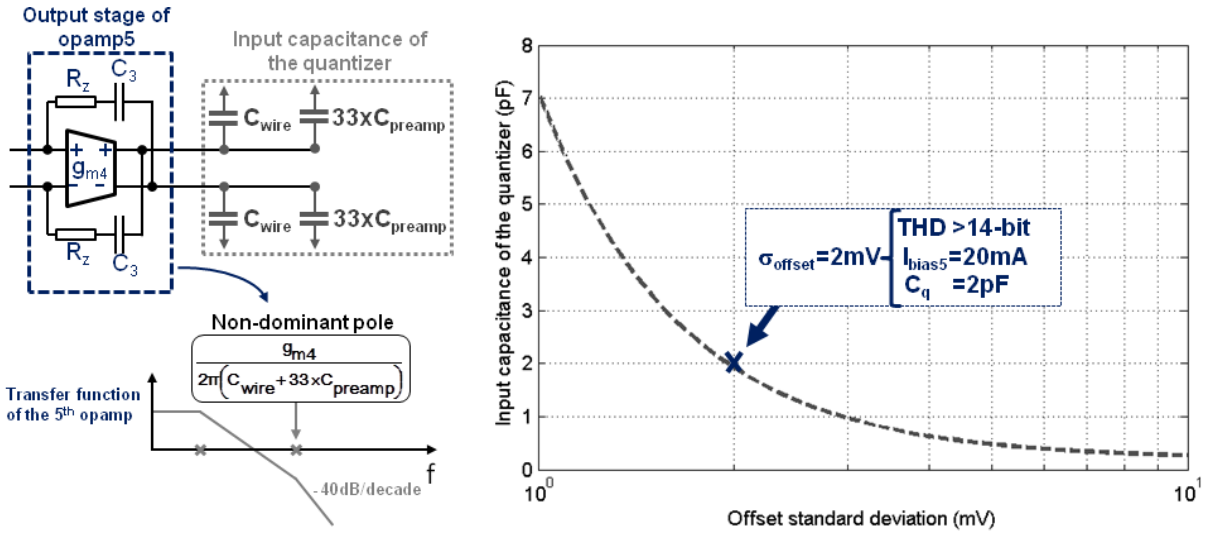

Figure 17. (a) Charge capacitive du dernier intégrateur, (b) Compromis entre l'offset et la capacité d'entrée du préamplificateur qui doit être pilotée par le filtre de boucle.

Comme représenté sur la Figure 17 (a), la conception du préamplificateur doit être considérée en tenant compte de l'étage de sortie du dernier intégrateur. La transconductance de l'étage de sortie de l'intégrateur et la capacité d'entrée du quantificateur créent un pôle non dominant qui rajoute du délai dans le chemin direct du modulateur $\Delta\Sigma$.
Il y a un compromis naturel entre le décalage de tension ramené à l'entrée des comparateurs qui exige des transistors de grande dimension et la capacité d'entrée du préamplificateur qui exige des transistors de faible dimension. Ce compromis est illustré sur la Figure 17 (b). Les simulations système ont montré que l'écart type de la tension de décalage doit être inférieur ou égale à 0.06LSB (2 mV) pour garantir une valeur de THD de 14-bit avec un rendement élevé. Dans ce cas, la capacité d'entrée résultante aurait une valeur de 2pF ce qui nécessiterait 20mA dans l'étage de sortie du dernier intégrateur pour obtenir une marge de phase de 65°.
La stratégie utilisée dans ce travail consiste à dimensionner les composants du comparateur avec une petite taille, puis corriger le décalage en tension à l'entrée des comparateurs.
Ainsi, les transistors d'entrée du préamplificateur ont une superficie de 0.14µm² qui se traduit par une capacité d'entrée de seulement 33.8fF pour les préamplificateurs. La capacité parasite de la connexion métallique qui relie le filtre de boucle au quantificateur augmente cette valeur à 280fF.
Avant calibration, la distribution aléatoire (Gaussienne) de la tension de décalage s'étend de -84mV à +84mV ($\pm 3\sigma$) comme illustré sur la Figure 18 (a). Les résistances du pont diviseur sont dimensionnées de telle sorte que leur contribution à la tension de décalage à l'entrée des comparateurs soit négligeable. D'après les simulations système, si le décalage en tension à l'entrée de chaque comparateur est uniformément distribué dans la plage 0-5mV après calibration, la spécification de linéarité est atteinte. Le LSB du CNA de calibration est donc choisi égale à 5 mV. Afin d'avoir un compromis raisonnable entre la linéarité et la complexité du circuit de calibration, la résolution du CNA est fixée à 5-bit ce qui permet d'avoir une gamme de correction allant de -80mV à +80mV. Dans ce prototype, la valeur du LSB reste contrôlable depuis l'extérieure du circuit et peut donc être ajustée pour couvrir une gamme de correction plus large au prix d'un décalage en tension résiduel plus important.
Comme le montre la Figure 18 (b), la tension de décalage à l'entrée du comparateur est uniformément distribuée dans la plage de 0-5 mV après la procédure de calibration. Cette stratégie permet de réduire le courant de sortie du dernier étage de l'intégrateur de 60% par rapport au cas sans calibration.

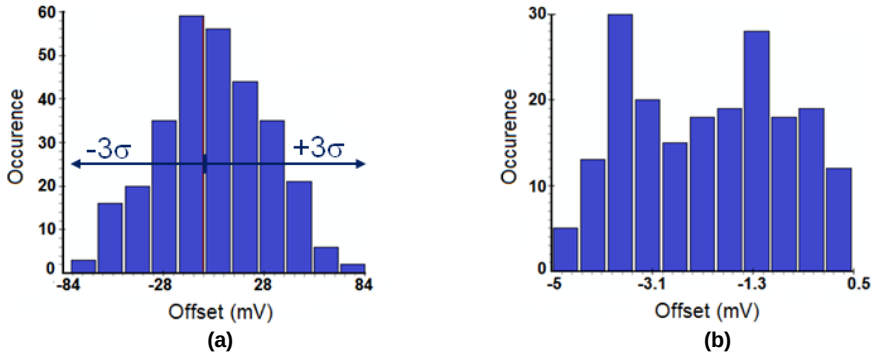

Figure 18. Histogramme de l'offset ramené à l'entrée du comparateur (a) avant calibration, (b) après calibration des échantillons situés dans l'intervalle [-80mV :+80mV].

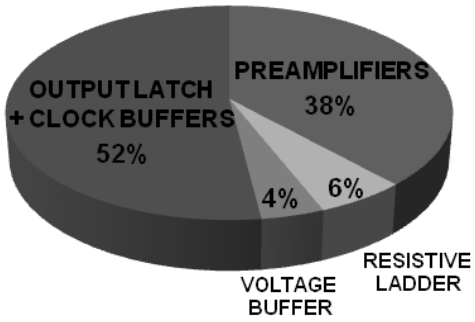

Figure 19. Répartition de la consommation de puissance dans le quantificateur simulé avec une sinusoïde ayant une amplitude d'entrée égale à la tension pleine échelle du convertisseur et une fréquence de 40 MHz.

Tableau 7. Principaux paramètres du quantificateur

PARAMETERS	VALUE	UNIT
Fréquence d'échantillonnage	640	MHz
Référence du quantificateur	0.8	V
Résolution	5	bit
Capacité d'entrée *préamplificateur* *piste de métal*	 80 200	 fF fF
Gain du préamplificateur	2.1*	_
Produit gain x bande du préamplificateur	10*	GHz
Bande passante à -3dB	4.7*	GHz
Tension de décalage	0-5	mV
Temps de conversion		ns
Résolution du CNA	5	mV
Tension d'alimentation *analogique* *numérique*	 1.2 1.0	 V V
Consommation de puissance *analogique* *numérique*	 5 4	 mW mW

***** simulations « post-layout »

Mesures

Description du banc de test

Le banc de test utilisé pour évaluer les performances dynamiques de notre prototype est illustré sur la Figure 20. Le générateur R&S AFQ100A permet de générer un signal sinusoïdal qui attaque un filtre passe-bande passif (K&L D5BT-6/12) dont la fréquence centrale est ajustable sur toute la largeur de bande du CAN. Il supprime les harmoniques et le bruit du générateur de signal assurant ainsi que la résolution mesurée est limitée par la performance du CAN uniquement. Un transformateur RF (Mini-Circuits ADT1-6T+) convertit le signal purifié en un signal différentiel qui sert d'entrée au CAN $\Delta\Sigma$.
Le signal d'horloge est fourni par un générateur large bande (R&S SMA 100A), pouvant générer une forme d'onde sinusoïdale avec une très faible gigue (50 fs_{rms}). La sortie différentielle du modulateur est acquise par un analyseur logique rapide (Agilent 16901) ayant une profondeur mémoire de 4 Mo. Les données stockées sont ensuite post-traitées avec MATLAB sur un PC.

Toutes les tensions d'alimentations du circuit sont fournies par des régulateurs sur le PCB de test. Les tensions d'alimentation analogique (1.2V), numérique (1.0V) et les tensions d'alimentation des blocs d'entrée/sortie (2.5V) sont séparées ainsi que leur masse. Chaque broche d'alimentation est découplée à l'aide de condensateurs qui sont soudés aussi près que possible du boitier afin de minimiser l'inductance de la piste. En pratique, les condensateurs de forte valeur ont un ESR élevé qui limite leur efficacité à une gamme de fréquence limitée. Pour réduire cet effet, plusieurs condensateurs ayant des valeurs de capacité différentes sont mis en parallèle. Le mode commun d'entrée du CAN $\Delta\Sigma$ (V_{CM}) est généré par un diviseur résistif à partir de l'alimentation analogique 1.2 V (non représenté sur la Figure 20). Cette tension de mode commun est découplée et connectée au point milieu du transformateur.

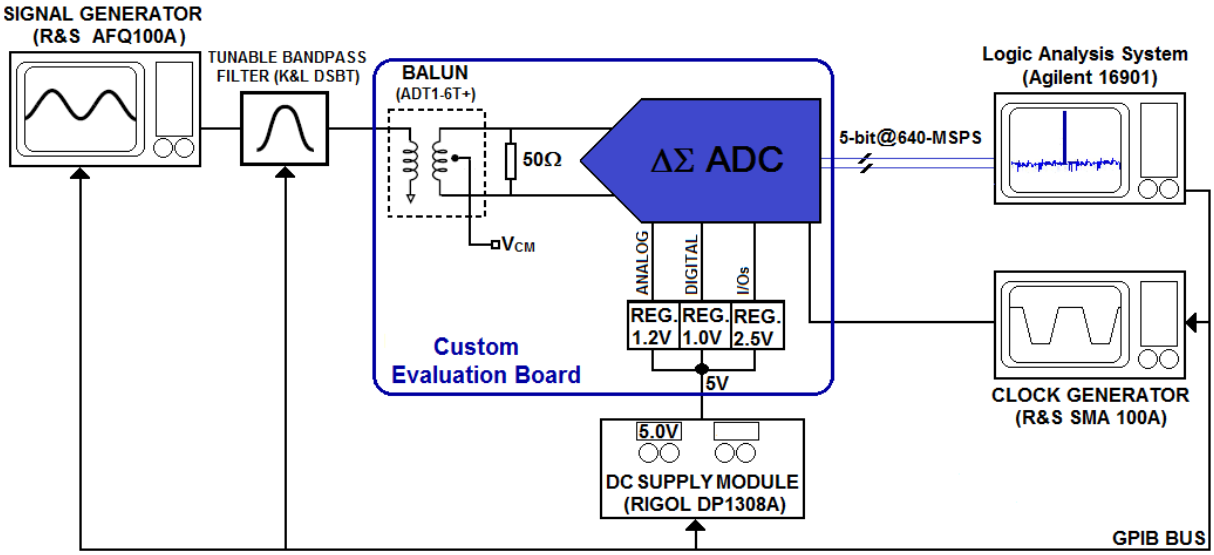

Figure 20. Banc de test utilisé pour évaluer le convertisseur ΔΣ.

La photo de la puce prise au microscope électronique est illustrée sur la Figure 21. Le prototype a été fabriqué en technologie CMOS 65nm. La surface du circuit avec les plots d'entrée/sortie est de 2.35mm² et comprends le modulateur ΔΣ, une référence de tension, un filtre de décimation programmable, des « buffers » CML ainsi que les circuits de calibration. Le circuit est conditionné dans un boitier CQFP à 100 broches. Les parties analogique et numérique utilisent des tensions d'alimentation de 1.2V et 1V respectivement. Les blocs analogiques sensibles tels que la référence de tension et le générateur de courant de polarisation ont été placés dans la partie supérieure gauche de la puce afin de réduire le couplage avec les signaux numériques à travers le substrat.

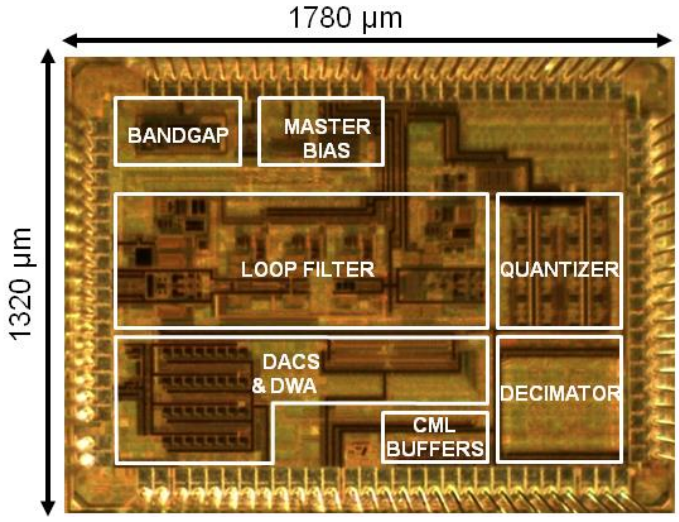

Figure 21. Schéma de la puce fabriquée dans une technologie CMOS 65nm de ST Microelectronics.

Premiers tests et analyse des résultats

Les mesures effectuées sur l'un des vingt-cinq échantillons révèlent que le prototype est fonctionnel avec et sans signal d'entrée. Les Figures 22 (a) et la Figure 22 (b) montrent que le plancher de bruit dans la bande passante est blanc, laissant présager que le bruit thermique est dominant, conformément au choix réalisé pendant l'étape de conception. La mise en forme du 5^{ième} ordre du bruit

de quantification a été mesurée sur la Densité Spectrale de Puissance (DSP) du signal en sortie du modulateur, avec et sans signal d'entrée.
Cependant, le bruit et la distorsion sont plus élevés que prévu lorsque la DWA est activée. Tout d'abord le plancher de bruit augmente de 3 dB. Concernant la linéarité, la DWA réduit l'amplitude des harmoniques impaires mais augmente celle des harmoniques paires, en particulier l'harmonique d'ordre deux comme représenté sur la Figure 22 (b). Cette constatation est mieux illustrée à la Figure 22 (c) où l'on voit que la valeur de l'harmonique d'ordre deux se dégrade fortement lorsque la DWA est activée. En ce qui concerne l'harmonique d'ordre trois, sa valeur s'améliore lorsque la DWA est activée comme le montre la Figure 22 (d).

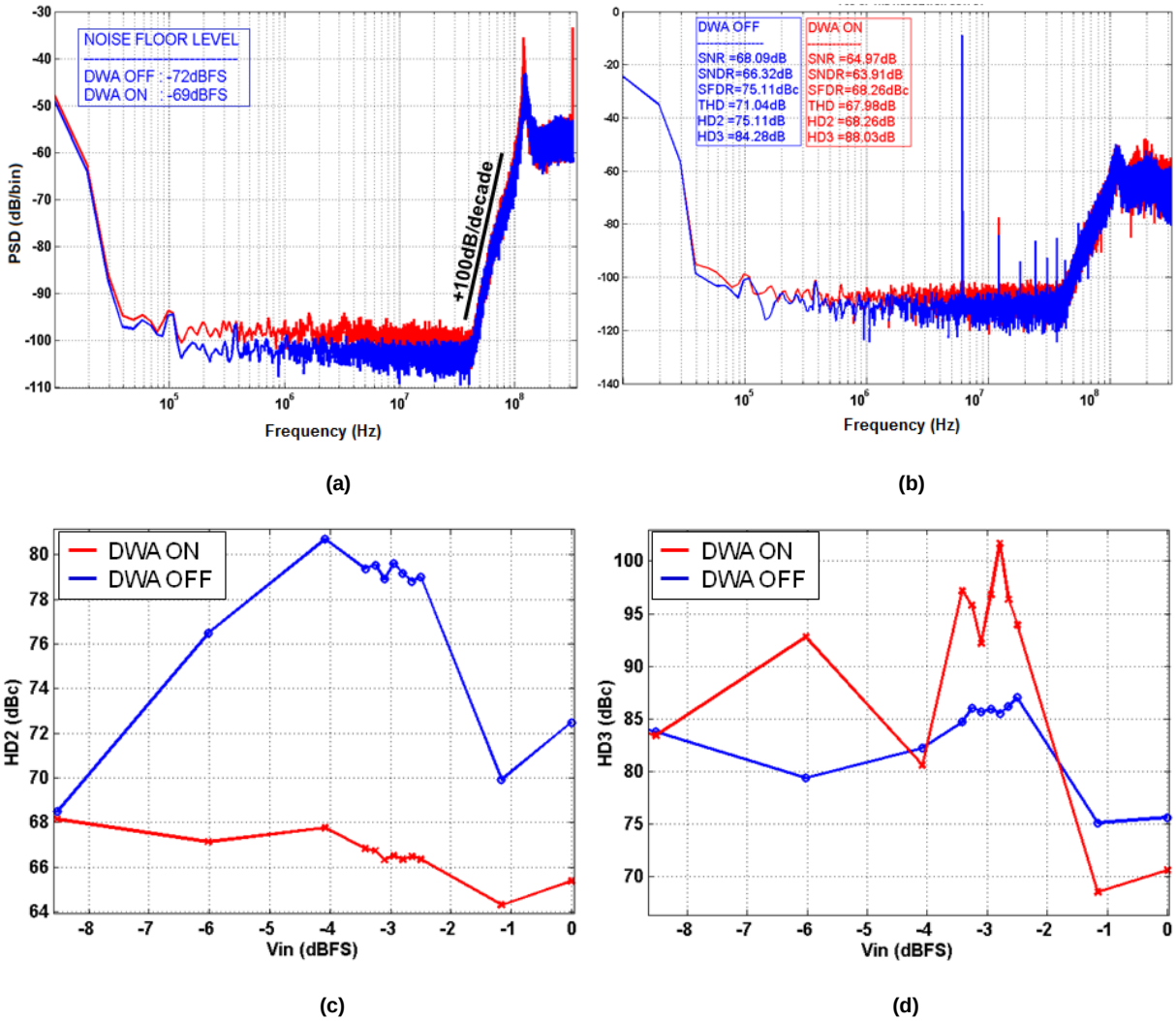

Figure 22. (a) Densité Spectrale de Puissance (DSP) en sortie du modulateur sans signal d'entrée, (b) DSP en sortie du modulateur avec une sinusoïde d'entrée ayant une amplitude et une fréquence de -4dBFS et 6MHz, (c) Mesure de l'harmonique d'ordre deux en fonction du signal d'entrée avec et sans DWA (d) Mesure de l'harmonique d'ordre trois en fonction du signal d'entrée avec et sans DWA.

Pour identifier l'origine de la dégradation des performances, des recherches bibliographiques approfondies ont été effectuées. Nous avons découvert dans la référence [19] que l'utilisation de la DWA dans un CNA avec de l'interférence entre symboles (ISI) conduit à une dégradation de performance similaire au phénomène observé en mesure.
Afin de réduire l'ISI, la taille de l'interrupteur et des circuits qui les pilotent peut être augmentée. Cependant les capacités parasites à la masse virtuelle du premier intégrateur deviennent plus importantes. Une autre possibilité est de choisir un CNA avec Retour à Zéro (RZ) [20] au prix d'une sensibilité accrue à la gigue d'horloge.
Il est également possible d'implémenter une DWA ayant une activité de commutation réduite par rapport à la DWA traditionnelle [19] mais au prix d'une correction moins efficace.

Un algorithme de mise en forme permettant l'atténuation des erreurs dues à l'ISI a été proposé dans [21] et validé pour une application audio.
Tous les résultats de mesure présentés dans la suite du document ont été réalisés sans la DWA.

Performance dynamique

Test avec une sinusoïde

La Figure 23 (a) montre la DSP de la sortie du modulateur ΔΣ pour une sinusoïde d'entrée dont l'amplitude et la fréquence sont respectivement de -2.5dBFS et 6 MHz. Le SNR_{peak} et THD_{peak} mesurés sont respectivement de 69.4dBc et 76.5dBc, ce qui se traduit par une résolution effective de 11-bit dans une bande passante de 40 MHz. La consommation de puissance du modulateur est de 87.3mW ce qui donne une Figure de mérite de Walden égale à 533fJ/pas-de-conversion. La dynamique mesurée (71.4dB) est représenté sur la Figure 23 (b).

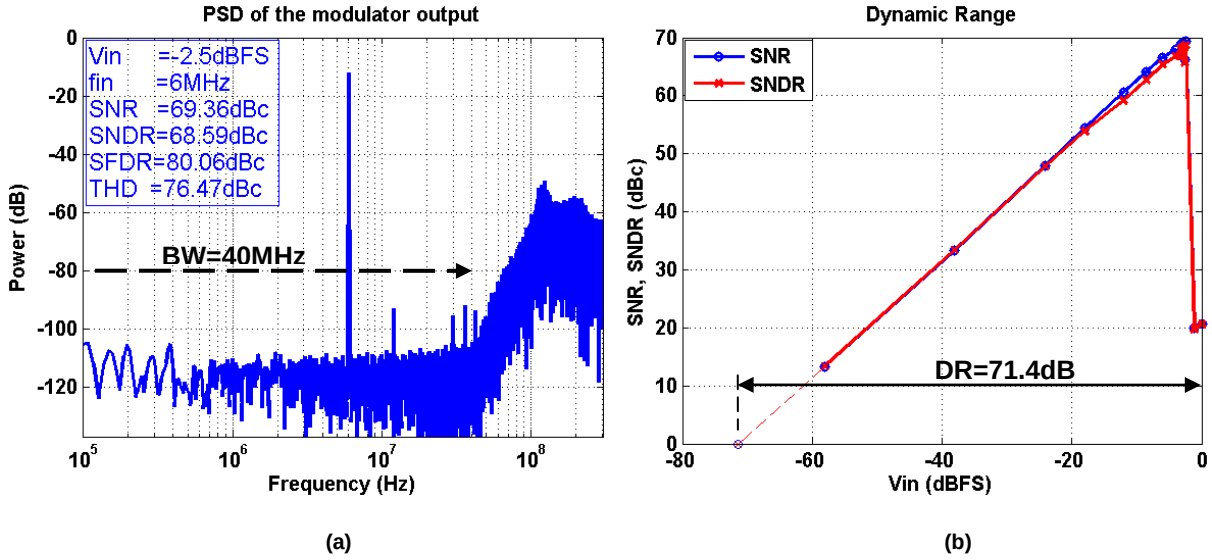

Figure 23. (a) Densité Spectrale de Puissance (DSP) en sortie du modulateur, (b) Mesure du SNR et du SNDR en fonction du signal d'entrée (f_{input}=6MHz).

Test avec deux sinusoides

Les produits d'intermodulation sont mesurés en injectant à l'entrée du modulateur deux sinusoïdes de même amplitude (-8.5dBFS) avec des fréquences respectives de 10MHz (f_{TONE1}) et 11MHz (f_{TONE2}).

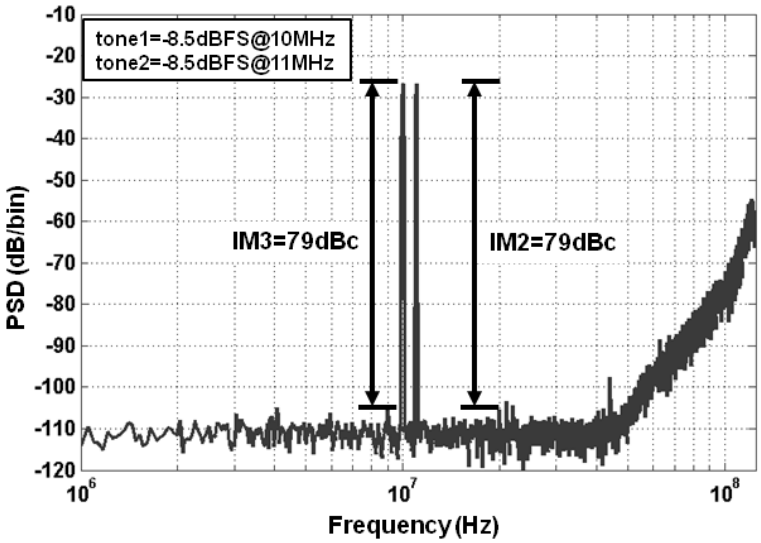

Figure 24. Mesure des produits d'inter-modulation.

Filtrage anti-repliement

La bande passante du signal et la fréquence d'échantillonnage du modulateur valent respectivement 40MHz et 640MHz. Tout signal parasite (bruit ou brouilleur) présent dans la gamme de fréquence allant de 600MHz à 640MHz peut se replier dans la bande utile.
La réjection de ces signaux parasites a été mesurée en faisant varier la fréquence du signal d'entrée sinusoïdal entre 600 MHz et 639MHz. Pour chaque fréquence, le rapport entre la puissance de sortie et la puissance d'entrée est calculé. Les résultats sont présentés sur la Figure 25. Comme prédit en simulation, le filtre de boucle du modulateur fournit une réjection aussi performante qu'un filtre de Butterworth du troisième ordre.

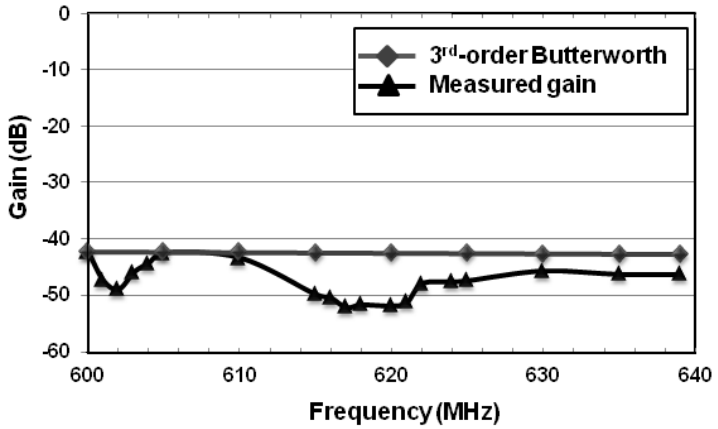

Figure 25. Mesure de la fonction de transfert anti-repliement et comparaison avec l'atténuation obtenue par un filtre Butterworth du troisième ordre ayant une bande passante de 40MHz.

Résumé des performances et comparaison à l'état de l'art

Les performances de notre modulateur ΔΣ à temps continu sont résumées dans le tableau 8.
L'efficacité énergétique (FoM de Walden), le taux de distorsion harmonique et la résolution effective sont comparés à l'état de l'art sur les Figure 26, Figure 27 et Figure 28, respectivement.

Tableau 8. Résumé des performances du modulateur ΔΣ

PARAMETRES	VALEUR	UNITE
Bande passante	40	MHz
Fréquence d'horloge	640	MHz
Tension d'entrée maximale	1.6	$V_{pp,diff}$
SNR_{peak}*	69.4	dBc
THD_{peak}*	76.5	dBc
$SNDR_{peak}$*	68.6	dBc
$SFDR_{peak}$*	80	dBc
ENOB*	11	bit
Dynamique*	71.4	dBc
$IM2@_{fin1=10MHz,fin2=11MHz}$	79	dBc
$IM3@_{fin1=10MHz,fin2=11MHz}$	79	dBc
PSRR@40MHz	51	dB
Anti-repliement@600MHz	42.4	dB
Consommation	87.3	mW
FoM_{Walden}	533	fJ/conv-step

***Mesuré avec une sinusoïde ayant une fréquence de 6MHz**

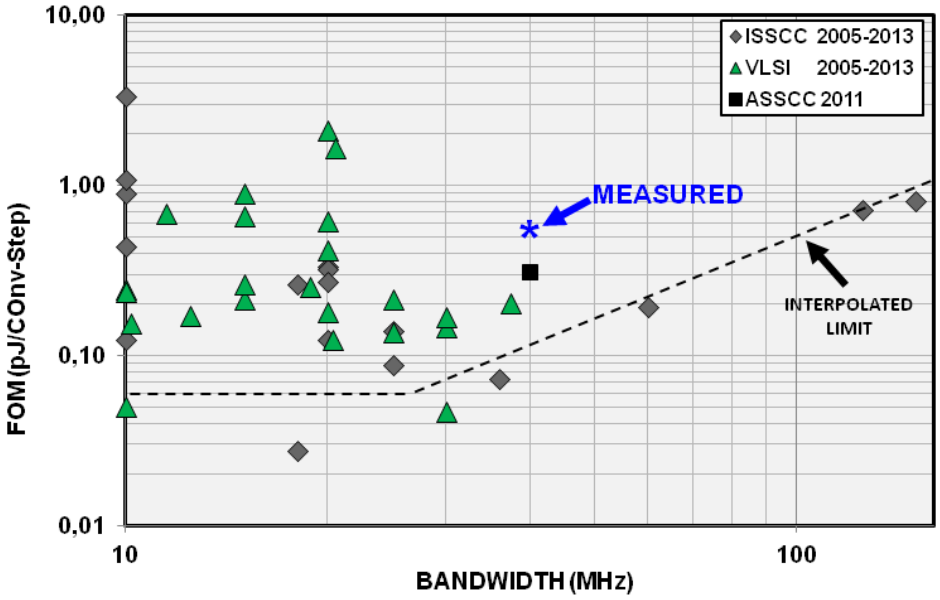

Figure 26. Comparaison de la figure de mérite obtenue à l'état de l'art.

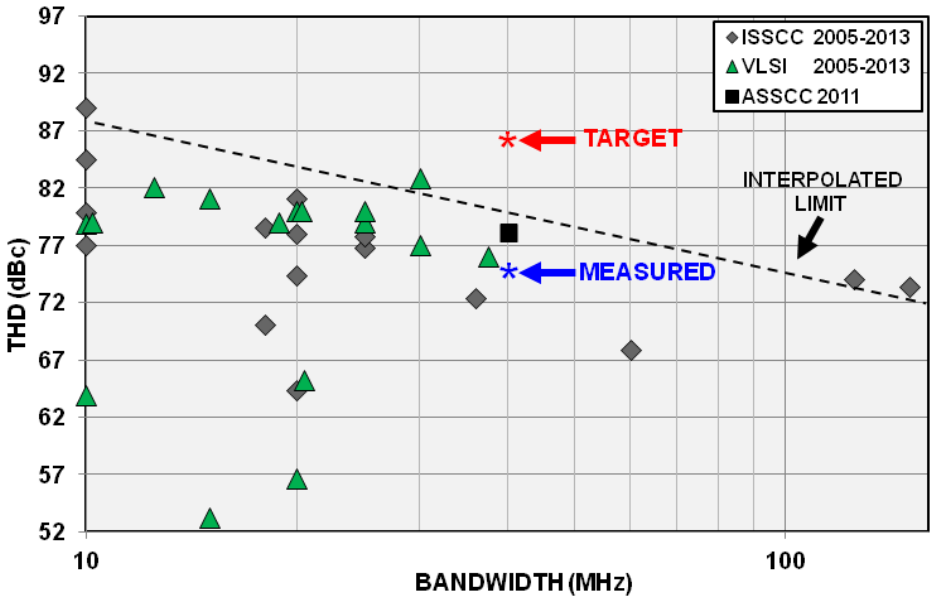

Figure 27. Comparaison du taux de distorsion harmonique mesuré à l'état de l'art.

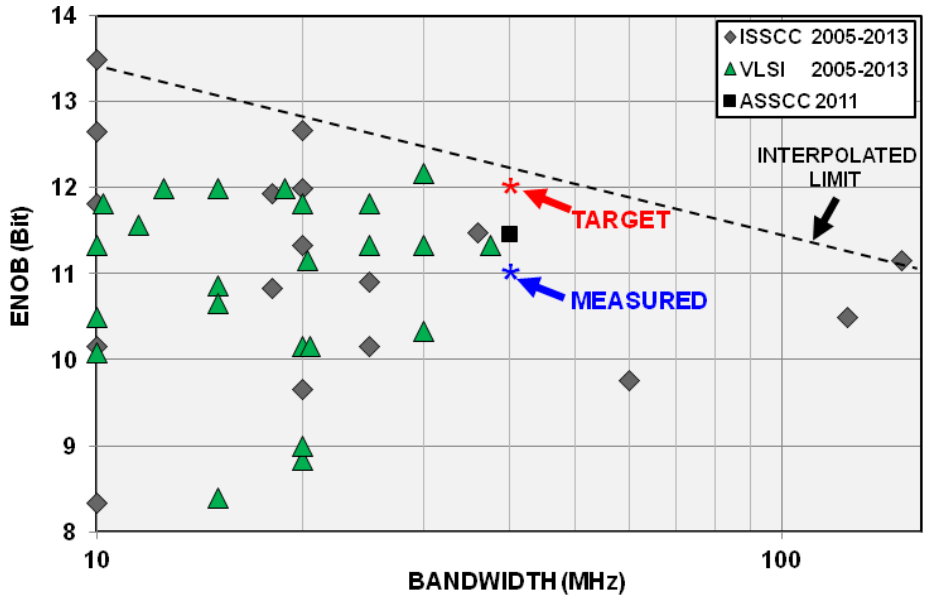

Figure 28. Comparaison de la résolution effective mesurée à l'état de l'art.

References

[1] W. Yang et al., “A 100mW 10MHz-BW CT ΔΣ Modulator with 87dB DR and 91dBc IMD,” ISSCC Dig. Tech. Papers, pp. 498–500, February 2008.

[2] G. Mitteregger, et al., “*A* 14 b 20 mW 640 MHz CMOS CT ΔΣ ADC with 20MHz signal bandwidth and 12b ENOB,” ISSCC Dig. Tech. Papers, pp. 62–63, February. 2006.

[3] Pradeep Shettigar, et al., “A 15mW 3.6GS/s CT- ΔΣ ADC with 36MHz Bandwidth and 83dB DR in 90nm CMOS,” ISSCC Dig. Tech. Papers, pp. 155–157, February 2012.

[4] Ruoxin Jiang,Terri Fiez, “A 14-bit ΔΣ ADC With 8x OSR and 4-MHz Conversion Bandwidth in a 0.18µm CMOS Process”, J. Solid State Circuits, vol. 39, pp.63-74, January 2004.

[5] J. G. Kauffman et al., “An 8mW 50MS/s CT ΔΣ Modulator with 81dB SFDR and Digital Background DAC Linearization,” ISSCC Dig. Tech. Papers, pp. 472–474, February 2011.

[6] www.mathworks.fr/

[7] http://www.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox

[8] http://www.analog.com/

[9] Kathleen Philips and Arthur H.M van Roermund, “ΣΔ A/D conversion for signal conditioning”, Springer, 2006 edition.

[10] K. Philips, P.A.C. M. Nuijten, R. Roovers, F. Munoz, M. Tejero, A. Torralba, “A 2mW 89dB DR Continuous-Time ΔΣ ADC with Increased Immunity to Wide-Band Interferers,” IEEE ISSCC Dig. Tech. Papers, February 2004.

[11] Yann Le Guillou, Hussein Fakhoury, “Elliptic filtering in continuous-time sigma-delta modulator”, Electronics Letters, Volume 41, Issue 4, February 2005.

[12] Mohammad Ranjbar, Omid Oliaei and Robert W. Jackson, “A Robust STF 6mW CT ΔΣ Modulator with 76dB Dynamic Range and 5MHz Bandwidth,” IEEE CICC Dig. Tech. Papers, Sept. 2010.

[13] Chi-Lun Lo, Chen-Yen Ho, Hung-Chieh Tsai, Yu-Hsin Lin, “A 75.1dB SNDR 840MS/s CT ΔΣ Modulator with 30MHz Bandwidth and 46.4fJ/conv FOM in 55nm CMOS,” IEEE VLSI Dig. Tech. Papers, June 2013.

[14] Bo Xia, Shouli Yan, and Edgar Sánchez-Sinencio, “An RC Time Constant Auto-Tuning Structure for High Linearity Continuous-Time ΣΔ Modulators and Active Filters », IEEE Trans. on Circuits and Systems-I: Regular Papers, VOL. 51, NO. 11, November 2004.

[15] Matthew Park and Michael H. Perrott, “A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-Time ΔΣ ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 µm CMOS,” IEEE J. of Solid-State Circuits, VOL. 44, NO. 12, December 2009.

[16] Piero Malcovati, Franco Maloberti, Carlo Fiocchi, and Marcello Pruzzi, “Curvature-Compensated BiCMOS Bandgap with 1-V Supply Voltage,” IEEE J. of Solid-State Circuits, VOL. 36, NO. 7, July 2001.

[17] Eduard Sackinger and Walter Guggenbuhl, “A Versatile Building Block: The CMOS Differential Difference Amplifier,” IEEE J. of Solid-State Circuits, VOL.SC-22, NO.2, April1987.

[18] Michael Choi and Asad A. Abidi, “A 6-b 1.3-Gsample/s A/D Converter in 0.35µm CMOS,” IEEE J. of Solid-State Circuits, VOL. 36, NO. 12, December 2001.

[19] Tao Shui, Richard Schreier, “Mismatch Shaping for a Current-Mode Multibit Delta-Sigma DAC”, J. Solid State Circuits, vol. 34, NO. 3, pp.331-338, March 1999.

[20] James A. Cherry, W. Martin Snelgrove, “Continuous-time delta-sigma modulators for high-speed A/D conversion, Theory, Practice and Fundamental Performance Limits”, Kluwer Academic Publisher, 1999.

[21] Lars Risbo, Rahmi Hezar, Burak Kelleci, Halil Kiper, Mounir Fares, “A 108dB-DR 120dB-THD and 0.5Vrms Output Audio DAC with Inter-Symbol-Interference-Shaping Algorithm in 45nm CMOS”, J. Solid State Circuits, vol. 40, pp.2408-2415, February 2011.

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List of abbreviations

ADC	Analog to Digital Converter
BER	Bit Error rate
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BoM	Bill of Material
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CQFP	Ceramic Quad Flat Package
CT	Continuous Time
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DR	Dynamic range
DT	Discrete Time
DWA	Data Weighted Averaging
ENOB	Effective Number of bits
ESD	Electro Static Discharge
FF	Flip Flop
FIR	Finite Impulse Response
FoM	Figure of Merit
FS	Full Scale
GBW	Gain Bandwidth Product
HD2	Second-Order Harmonic Distortion
HD3	Third-Order Harmonic Distortion
IC	Integrated Circuit
IF	Intermediate Frequency
INL	Integral Non Linearity
ISI	Inter Symbol Interference
LDO	Low Drop Output
LP	Low Pass
LSB	Least Significant Bit
MSA	Maximum Stable Amplitude
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal
MSPS	Mega Samples Per Second
NTF	Noise Transfer Function
NRZ	Non Return to Zero
OSR	Over-Sampling Ratio
PCB	Printed Circuit Board

PDK	Process Design Kit
PGA	Programmable Gain Amplifier
PVT	Process Voltage Temperature
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
opamp	operational amplifier
RMS	Root Mean Square
RF	Radio Frequency
RZ	Return to Zero
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SNR	Signal to Noise Ratio
SNRj	Signal to Jitter Noise Ratio
SNDR	Signal to Noise plus Distortion Ratio
SQNR	Signal to Quantization Noise Ratio
STF	Signal Transfer Function
THD	Total Harmonic Distortion
TSPC	True Single Phase Clock

List of symbols

A	opamp dc gain
A_β	Matching constant
A_{VT}	Voltage threshold matching constant
C_q	Input capacitance of the quantizer
C_{ox}	Gate oxide capacitance per unit area
C_{wire}	Capacitance of the metal wire
f	Frequency in Hz
f_s	Sampling frequency
g_m	MOSFET transconductance
H_i	Transfer function of a real integrator
H_{R_ideal}	Transfer function of the real resonator
H_{i_ideal}	Transfer function of the ideal integrator
I_{LSB}	LSB current
k	Boltzmann constant
KF_n	Flicker noise constant of NMOS transistor
KF_p	Flicker noise constant of PMOS transistor
L	Modulator order
L_p	PMOS transistor length
L_n	NMOS transistor length
L_R	Resistor length
N	Quantizer resolution
p	Laplace variable ($p=j\omega$)
Q	Quality factor of an OPAMP-RC resonator
Q_{max}	Maximum out-of-band gain of the NTF
T	Absolute temperature
T_s	Clock period
T_{ox}	Gate oxide thickness
t_p	time propagation of a latch
V_c	Voltage across the integrating capacitor
VOH	Voltage value of a ‘1’ logic level
VOL	Voltage value of a ‘0’ logic level
V_{os}	Input referred offset voltage
V_{gt}	Overdrive voltage
V_R	Voltage across the input resistor of an integrator
V_{REF}	Voltage reference of the quantizer
W_p	PMOS transistor width
W_n	NMOS transistor width

Z_{dac}	Output impedance of the DAC
α_{1c}	Linear coefficient of the polynomial approximation
α_{2c}	Quadratic coefficient of the polynomial approximation
α_{1R}	Linear coefficient of the polynomial approximation
α_{2R}	Quadratic coefficient of the polynomial approximation
$\Delta\Sigma$	Delta Sigma
ε	Quantization error
σ	Standard deviation
τ_p	Time constant of a latch
μ_n	Electron mobility
μ_p	Hole mobility
ω_o	Central pulsation of the resonator
ω_{ug}	Unit gain pulsation of the ideal integrator
ω_{ug_error}	Error on the unit gain pulsation of the integrator

Chapter 1

Introduction

1.1 Motivation

The market of A/D converters can be segmented in two categories. From one side we distinguish the Intellectual Property (IP) blocks that are generally optimized for a specific application. On the other side, the general purpose discrete Integrated Circuits (ICs) that are designed such as they could be used in different applications.
This thesis work deals with the second category whose market is dominated by the four suppliers shown in Table 1-1. Each of these companies purposes a portfolio of discrete ADC ICs that cover a wide range of applications. As this work targets applications that require wideband and high-resolution ADC ICs, we focused on the components with a data-rate≥20MSPS and ENOB>10-bit. By classifying them according to their topology, it clearly appears that the pipeline architecture is mostly implemented compared to the $\Delta\Sigma$ architecture as shown in Figure 1-1. This is quite paradoxical because the Continuous-Time (CT) $\Delta\Sigma$ architecture has attractive advantages over its pipeline counterpart, such as:

- Better power efficiency inherent to the CT nature of the loop filter.
- Relaxed requirements on the anti-aliasing filter due to the oversampling and the intrinsic CT loop filter.
- A linear time-invariant input impedance which relaxes the design constraints of the ADC driver.

A probable reason of the unequal distribution between pipeline ADCs and $\Delta\Sigma$ ADCs goes back to the early age of the $\Delta\Sigma$ architecture. At this time, the fabrication technology of ICs was not advanced enough to implement wideband $\Delta\Sigma$ ADCs because they require a clock speed of several hundred of megahertz [1][2]. This is why this architecture has been extensively implemented in audio applications for a long time. The pipeline which is intrinsically fast, has taken the lead for broadband applications and now this architecture is very mature.
Another popular feature of the pipeline (as others Nyquist converters) is the possibility to use it above the first Nyquist zone while it is not possible with a CT $\Delta\Sigma$ ADC. But in this case, the pipeline must use a power hungry input buffer to maintain its dynamic performances. When the buffer is not integrated on-chip, a matching network must be inserted between the buffer and the ADC input which increases the bill of material (BOM) on the printed circuit board (PCB).
Furthermore, even in the first Nyquist zone, a buffer with low output impedance is recommended to isolate the input-sampling stage of the pipeline ADC from the bonding wires of the package.
For a fair comparison, the pipeline used above the first Nyquist zone should be opposed to the bandpass $\Delta\Sigma$ modulator [3] which digitizes a signal around an intermediate frequency (IF) rather than at a zero IF.
In this work, the $\Delta\Sigma$ ADC IC is designed for applications in which the signal to be converted is centered on DC. It should be noted that a $\Delta\Sigma$ ADC which converts a signal centered on DC is also called a low-pass $\Delta\Sigma$ ADC. When the LP term is not written, it is implicitly assumed.

Today, the aggressive scaling of the CMOS technology dictated by Moore's Law has reached a point which makes possible to implement wideband CT $\Delta\Sigma$ ADC IC for general purpose applications [1][2]. The few products available in the market are introduced in the next chapter. They integrate a CT $\Delta\Sigma$ modulator core, a frequency synthesizer, a digital decimation filter and a voltage reference in the same die which is mounted in a small footprint package available at low cost. They have outstanding performance while consuming low power. However, their signal bandwidth is limited to 10MHz [2] and 25 MHz [1].

Table 1-1. Worldwide data converter revenue share by supplier between 2010 and 2011

COMPANY	2011 RANK	2011 $M	2011 Share	2010 RANK	2010 $M	2010 Share
Analog Devices	1	1,312	48.5%	1	1,422	47.5%
Texas Instruments	2	625	23.1%	2	659	22%
Maxim Integrated	3	185	6.8%	3	197	6.6%
Linear Technology	4	125	4.6%	4	142	4.7%

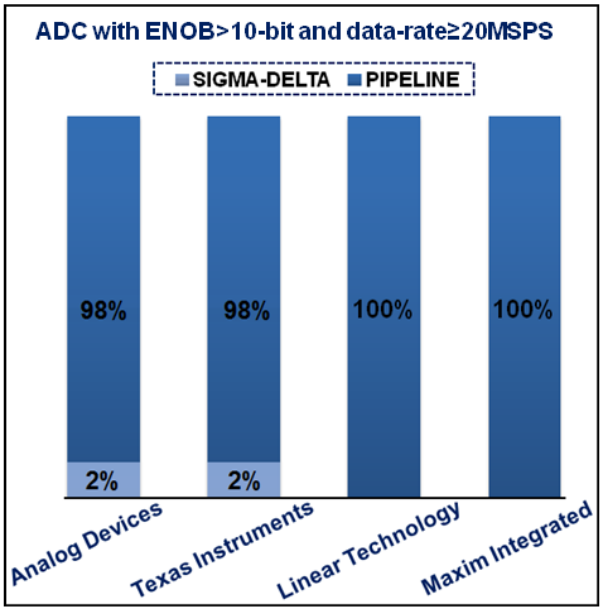


Figure 1-1. Architecture repartition of discrete ADC ICs with ENOB>10-bit and data-rate≥20MS/s available in the portfolio of worldwide leaders in data conversion market.

1.1 Thesis objectives

This PHD work is part of a research and development program that was initiated in the FP7 SACRA project and whose goal was to study the feasibility of a ΔΣ ADC IC that would be able to compete with the pipeline architecture for applications that require low noise (SNR=12-bit), low distortion (THD>14-bit) and a signal bandwidth greater than 25MHz.
For a fair comparison with state-of-the-art products available in the market [1][2], the architecture of our ADC IC includes beyond the CT ΔΣ modulator core, most of the features needed in a commercial product such as a voltage reference, a decimation filter and all the calibration circuits that compensate for the imperfections of the analog components. A simplified schematic of the ADC IC is shown in Figure 1-2.

As highlighted in Figure 1-2, the work presented in this manuscript is focused on the design and the characterization of the CT ΔΣ modulator only.

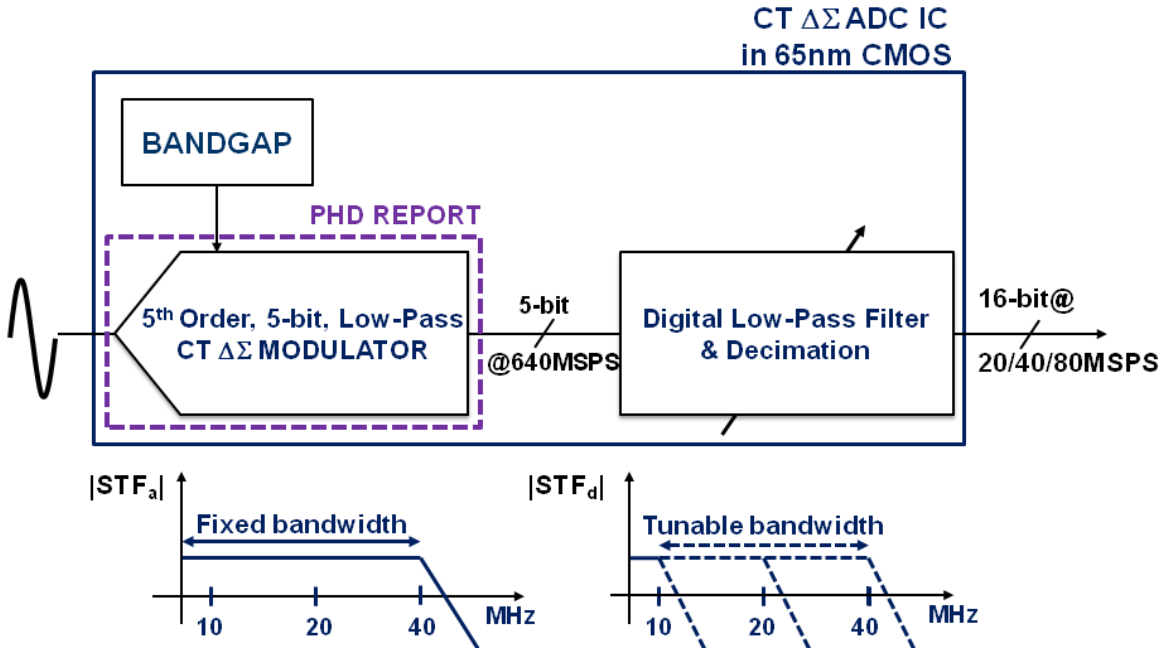


Figure 1-2. Architecture of the 65nm CMOS ΔΣ ADC IC.

1.2 Contribution

In this work we purposed the modeling, design and measurement of a complete CT ΔΣ modulator. The circuit-level part includes:

- The design of a 5th-order CT single-loop filter with a 5-bit quantizer clocked with an OSR of only 8X.

- The design of all the calibration and correction techniques that are often done off chip. It includes a mixed-signal circuit that compensates for the shift of the integrators time constant, another mixed-signal circuit that corrects the random offset within the comparator of the 5-bit flash, and a digital block that corrects the mismatch-induced noise and distortion in the feedback DACs

- For the test, custom high-speed buffers were designed to bring safely the modulator output out of the chip.

Furthermore, a design flow which consists in modeling the main imperfection of the ΔΣ modulator was introduced to facilitate the transistor-level implementation.
Measurement results were detailed and the gap compared to the circuit-level performance was analyzed in depth.

1.3 Thesis outline

Chapter 1 provides an introduction to explain the motivation, the goal and the context of this work.

Chapter 2 is a state of the art that focuses on wideband $\Delta\Sigma$ modulator architecture. The architecture proposed in the catalog of leading suppliers such as Analog Devices (ADI) and Texas Instruments (TI) are analyzed. Furthermore, the wideband architectures presented the last 10 years in the best solid-state circuit conferences such as ISSCC and VLSI Symposium, are analyzed in depth to see if it exists a natural choice for applications that require wideband conversion signal with high resolution. The chosen architecture and the targeted performance are also introduced.

Chapter 3 presents the system-level modeling of the imperfections of each sub-block of the $\Delta\Sigma$ modulator. We analyze in depth the impact of these non-idealities on the performance of the overall modulator which allows deriving the specifications of each building blocks of the modulator.

Chapter 4 presents the implementation details of each sub-block of the modulator in the 65nm CMOS process of ST Microelectronics and we give design strategy for implementing a robust modulator.

Chapter 5 presents the fabricated prototype and the measurement results that validate most of choices done at architectural level and circuit level. The difference between the simulation and the measurement is analyzed in depth and the problem is clearly identified. Solutions are proposed to improve the performance of a future prototype.

Chapter 6 concludes with an overview of accomplishments and contribution. In addition, we purpose directions to improve the power efficiency and the signal transfer function of our IC prototype. Finally we highlight the future challenges that $\Delta\Sigma$ modulators designers will face.

1.4 References

[1] G. Mitteregger, et al., "*A* 14 b 20 mW 640 MHz CMOS CT $\Delta\Sigma$ ADC with 20MHz signal bandwidth and 12b ENOB," ISSCC Dig. Tech. Papers, pp. 62–63, February. 2006.

[2] W. Yang et al., "A 100mW 10MHz-BW CT $\Delta\Sigma$ Modulator with 87dB DR and 91dBc IMD," ISSCC Dig. Tech. Papers, pp. 498–500, February 2008.

[3] S. R. Norsworthy, R. Schreier, G. Temes, "Delta-Sigma Data Converters, Theory, Design and Simulation," IEEE Press, 1996.

Chapter 2

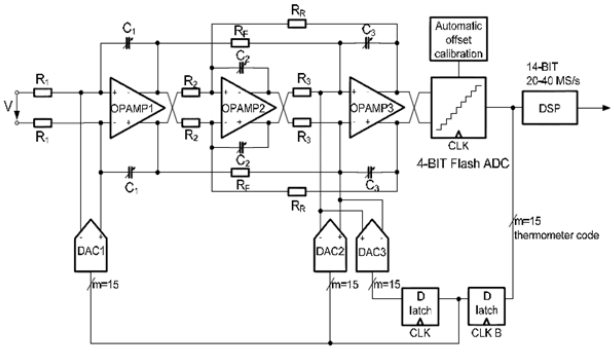
State of the art

2.1 From the market side

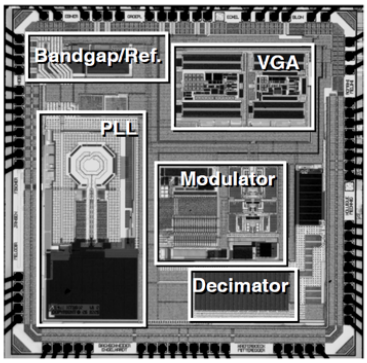
The AD926X family from Analog Devices and the ADC12EU050 from Texas Instruments prove that the CT ΔΣ architecture is an attractive alternative to the pipeline architecture in broadband applications. Their architecture is discussed in the next two sub-sections.

2.1.1 The ADC12EU050 from Texas Instruments

The ADC12EU050 [1] is the fastest and more power efficient ΔΣ ADC IC. The core of the IC is based on a CT ΔΣ architecture that was initially designed by Xignal Technologies and introduced in 2006 at the International Solid State Circuit Conference (ISSCC) [2]. Compared to previous published broadband ΔΣ A/D converters, this IC was a breakthrough. The architecture of the ΔΣ modulator is shown in Figure 2-1(a). Clocked at 640MHz, it achieves 12-bit ENOB within 20MHz of signal bandwidth while consuming only 20mW. The unit current cells of the main DAC are sized to meet the linearity requirement. The decimation filter is integrated on-chip together with an LC- PLL that provides a low-jitter clock signal to the modulator. The 450kHz bandwidth of the PLL provides a cleaning function that reduces the jitter requirement of the reference clock source. The chip is implemented in a 130nm 1P8M 1.2V CMOS process and the ΔΣ modulator achieves a FoM of only 121fJ/conversion-step. This design is a reference and it is still widely cited in publications that referred to state of the art CT ΔΣ ADCs.
The chip micrograph and the performance summary are shown in Figure 2-1(b) and Figure 2-1(c) respectively. It should be noted that the ADC12EU050 is a modified version of the prototype introduced in [2]. More details about the performance of this product can be found in [1].



(a)



(b)

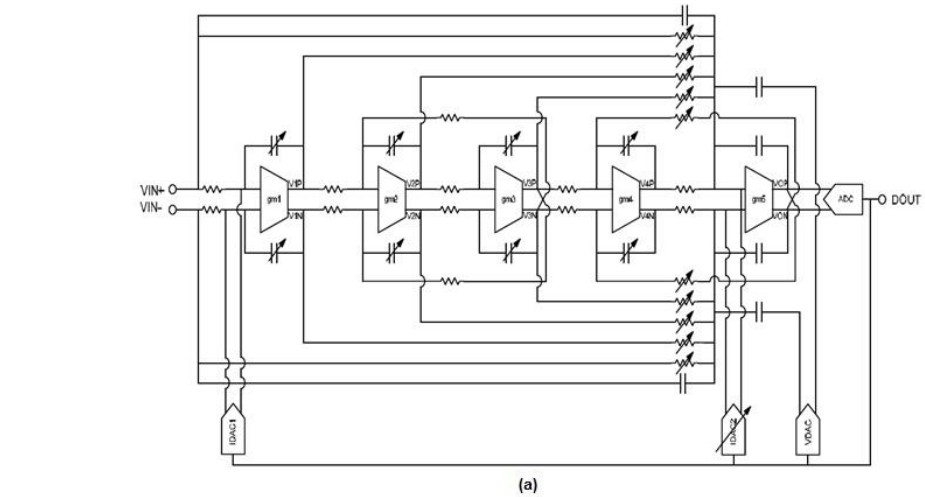
Sampling Frequency		640MHz
Conversion Rate		40MS/s
Input Range		0-20MHz
Peak SNR		76dB
THD		-78dBc
Peak SNDR		74dB
ENOB		12
Process		1.2V 130nm CMOS
Chip Area		8.6mm²
Power	Modulator	20mW
	Decimator 40MS/s	18mW
	PLL 2.56GHz	12mW
	I/O 1.8V	4mW

(c)

Figure 2-1. Characteristics of the ΔΣ ADC IC introduced by Xignal Technologies in 2006 [3]. (a) CT ΔΣ Modulator architecture, (b) Chip micrograph, (c) Performance summary.

2.1.2 The AD926X family from Analog devices

In 2008, Analog Devices has introduced a wideband ΔΣ modulator with more than 13-bit ENOB and ultra-low distortion of -89dBc within 10MHz of signal bandwidth [3]. The architecture of the ΔΣ modulator is shown in Figure 2-2(a). It is built around a 5th-order loop filter and a nine-level flash quantizer clocked with an OSR of 32. The mismatch-induced noise and distortion in the main DAC are corrected by shuffling the thresholds of the comparators.
The chip was implemented in a 180nm 1.8V 1P6M CMOS process. The micrograph showing the ΔΣ modulator only and the performance summary are shown in Figure 2-2(b) and Figure 2-2(c) respectively.
This ΔΣ modulator is the core of the AD926X products series whose characteristics are shown in Table 2-1. More information about these products can be found is [4].



Sampling Frequency	640MHz
Conversion Rate	640MS/s
Input Range	0-10MHz
Peak SNR	84.3dB
THD	-89dBc
Peak SNDR	82dB
ENOB	13.3-bit
Process	1.8V 180nm CMOS
Chip Area	0.7mm²
Power	100mW
FOM	486fJ/conv-step

(c)

Figure 2-2. ΔΣ ADC IC presented by Analog Devices at ISSCC in 2008 [3] (a) CT ΔΣ Modulator architecture, (b) Chip micrograph of the ΔΣ modulator, (c) Performance summary.

Table 2-1. AD926x Continuous-Time Converter Family [4]

Part Number	Resolution (Bits)	Bandwidth (MHz)	Channel Count	SNR (dBFS)	SFDR (dBFS)	Power (mW)	Output Interface	Package	Integration
AD9262	16	2.5	2	90.5	87	580	16-bit CMOS	9 mm × 9 mm 64-lead LFCSP	PLL, decimation filters, sample rate converter
AD9262-5	16	5	2	87.5	87	630	16-bit CMOS	9 mm × 9 mm 64-lead LFCSP	PLL, decimation filters, sample rate converter
AD9262-10	16	10	2	84.5	87	675	16-bit CMOS	9 mm × 9 mm 64-lead LFCSP	PLL, decimation filters, sample rate converter
AD9267	4-bit modulator*	10*	2	85*	87	400	4-bit LVDS	9 mm × 9 mm 64-lead LFCSP	PLL
AD9261-10	16	10	1	84.5	87	350	16-bit CMOS	7 mm × 7 mm 48-lead LFCSP	PLL, decimation filters, sample rate converter

2.2 Architectural trend in wideband and high resolution ΔΣ ADC

In this section, we present possible architectural alternatives to implement a wideband ΔΣ modulator. The fundamental parameters of the modulator such as the Over-Sampling Ratio (OSR), the order of the modulator (L) and the number of bit in the quantizer (N) are also discussed. The goal of this section is to give a qualitative analysis by showing the architectural trends in wideband ΔΣ modulators. Except otherwise specified, all data presented in this section are extracted from papers published in the best solid-state-circuits conferences (ISSCC, VLSI, CICC, ESSCIRC) between 2005 and 2014.

2.2.1 ΔΣ modulator topology: single-loop or multi-loop

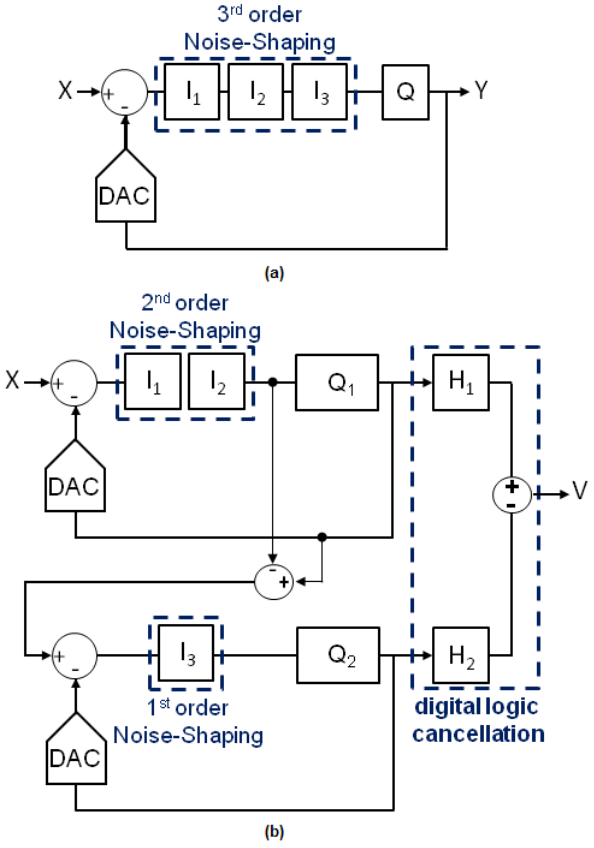


Figure 2-3. Third-order ΔΣ modulator with (a) third-order single-loop topology, (b) cascaded second-order and first-order stages, also known as 2-1 cascaded or 2-1 MASH ΔΣ modulator.

As shown in Figure 2-3(a), an L^{th} order single-loop modulator consists of L integrators cascaded in the forward path. Due to the high loop-gain, this topology is relatively robust against analog imperfections. When L is greater than two, the dynamic range (DR) of the modulator must be reduced to preserve its stability, especially if a mono-bit quantizer is used [5].
The cascaded topology avoids this issue by decomposing the order of the noise shaping transfer function in several stages of lower-order single-loop modulator. In Figure 2-3(b), a 2-1 cascaded modulator that has the same noise shaping behavior as the third-order single loop modulator shown in Figure 2-3(a), is shown as an example. Assuming a linear model of both quantizer (Q_1 and Q_2) the output of the cascaded modulator can be written as:

$$\mathbf{V = H_1STF_1 \times X + (H_1NTF_1 - H_2STF_2) \times \varepsilon_1 - H_2NTF_2 \times \varepsilon_2} \quad (2\text{-}1)$$

where STF_1, NTF_1, and ε_1 are the Signal transfer Function (STF), Noise transfer Function (NTF) and quantization error of the first stage respectively, and STF_2, NTF_2, and ε_2, the STF, NTF and quantization error of the second stage respectively.
If the analog transfer functions of the modulator stages and the digital transfer functions of the logic cancellation match each other according to relations 2-2 and 2-3, the quantization error of the first stage is cancelled and the quantization error of the second stage is shaped to an order that is the

summed of each order stage as expressed by equation (2-4). That is why this topology is also called Multi-stAge noise SHaping (MASH).

$$\mathbf{H_1 = STF_2} \tag{2-2}$$

$$\mathbf{H_2 = NTF_1} \tag{2-3}$$

$$\mathbf{V = H_1 STF_1 \times X - NTF_1 NTF_2 \times \mathcal{E}_2} \tag{2-4}$$

This topology is particularly attractive for broadband applications that require high resolution at low OSR. In [6] an 8th order cascaded modulator with an OSR of only 3 is reported while the maximum order of a single-loop topology rarely exceeds five [1]. It should be noted that the noise-shaping efficiency of a single-loop modulator that uses a low-OSR is very poor when the order of the loop filter goes beyond five.

A flexible feature of the MASH structure is that each stage can be implemented with a different architecture. On the example of Figure 2-3(b), the first stage can be a $\Delta\Sigma$ modulator while the second stage could be a pipeline architecture [7][8]. A particular case of the cascaded architecture is the 0-$\Delta\Sigma$ MASH which increases the dynamic range beyond the ADC full-scale [9].

In practice, the noise performance of the cascaded architecture is limited by the mismatch between the transfer functions of the analog modulator and those of the digital logic cancellation. The consequence is that the quantization noise of the first stage leaks to the output of the modulator and degrades the theoretical SQNR. Calibration algorithms are often used to reduce the effect of mismatch [10-13]. Another drawback of the MASH compared to the single loop topology is the more stringent requirement on the DC gain of the integrators in the first stages, especially when a low-order noise shaping is used. For negligible degradation of the SQNR, the opamp gain should be in the range of OSR^M for a M-cascaded stage [14] while it should be in the range of OSR for a single-loop structure [5]. This can be a penalty when the modulator must be implemented in a deep submicron process in which transistors have poor intrinsic gain.

In [15] an architecture that combines the stability advantages of the multi-loop with the relaxed circuit requirement of the single-loop such as opamp gain is introduced. It is called Sturdy-MASH (SMASH) and it does not require digital logic cancellation. As shown in Figure 2-4, most of the published wideband high resolution $\Delta\Sigma$ modulators have used a single-loop topology. But its MASH counterpart is a very promising architecture for wideband applications that require very low noise. Recently, Y. Dong et al. have introduced a CT 0-3 MASH with an SNR of 84.6dB within 53MHz of signal bandwidth [16].

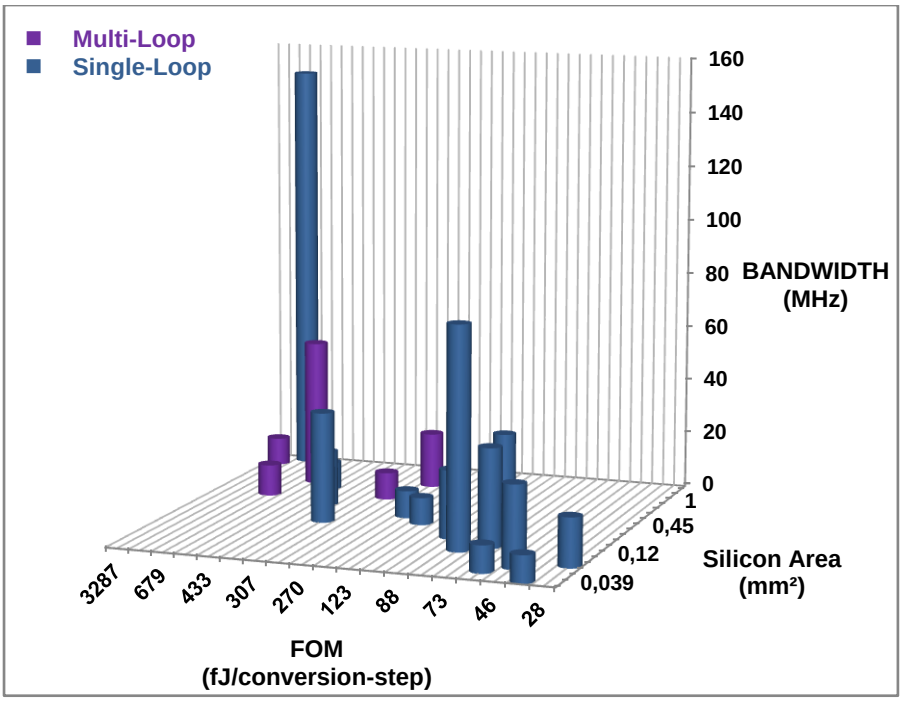


Figure 2-4. 3D plot of the signal bandwidth as a function of the FoM and silicon area of wideband $\Delta\Sigma$ modulators with ENOB≥11-bit.

2.2.1 Loop filter compensation-style

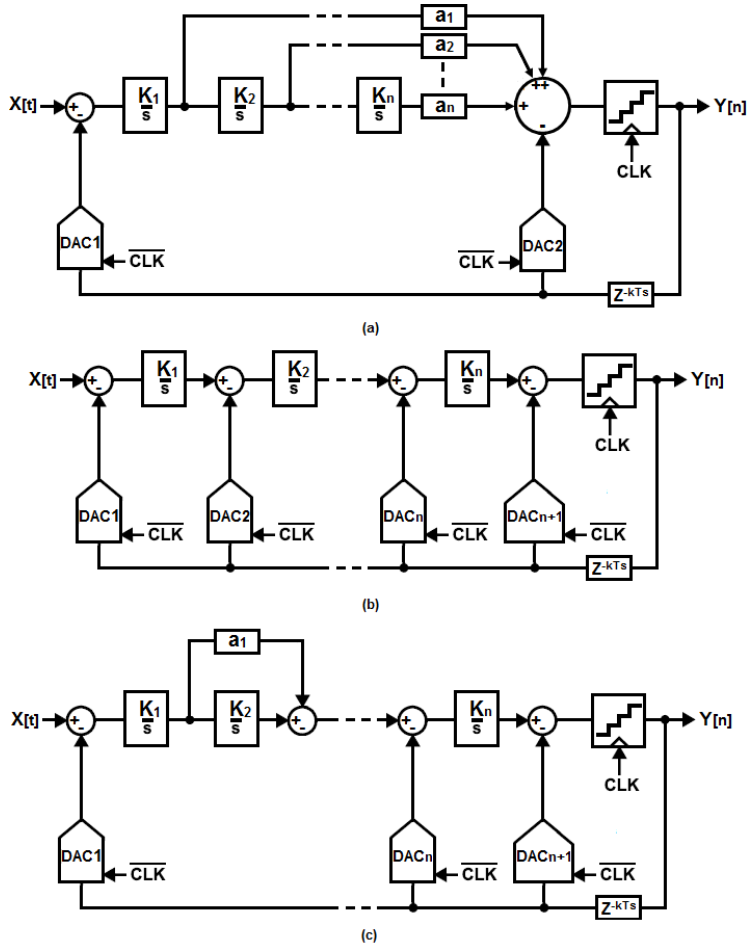


Figure 2-5. ΔΣ modulator with (a) a feedforward loop filter and, (b) feedback loop filter, (c) mixed feedforward-feedback loop filter.

When the order of the loop filter is equal to or higher than two, the open-loop transfer function of the modulator must be compensated to obtain a robust phase margin as in any system used in a feedback loop. In a ΔΣ modulator, the poles of the open-loop transfer-function are compensated by introducing zeros. This can be done by using feedforward compensation, feedback compensation or a combination of the two techniques as shown in Figure 2-5(a), Figure 2-5(b), Figure 2-5(c) respectively.
The feedforward compensation is mostly used because the voltage swings inside the loop filter are a small fraction of the reference voltage which results in low distortion and low power consumption. If a direct feedforward path is added from the input of the modulator to the input of the quantizer, the loop filter processes the quantization noise only, which improves the linearity performance [17].
However, the feedforward architecture suffers from peaking in the STF and adding a direct feedforward path degrades the anti-alias transfer function as explained in Figure 2-6. This degradation may result in a more stringent requirement on the anti-aliasing filter in front of the ADC which in turn will increase the power consumption and the area of the acquisition system as a whole.
The feedback architecture has a robust peaking-free STF and better alias rejection compared to the feedforward compensation. But as a portion of the signal is injected at each internal node of the loop filter, it results in a more stringent requirement on the integrators. Furthermore, each feedback coefficient needs an additional DAC for its implementation.
The pure feedback architecture is implemented in applications that require robust filtering requirements and when the power consumption is not critical [18]. As confirmed in Figure 2-7, the feedforward architecture is the more power efficient. However, to do a fair comparison between feedback and feedforward compensation techniques, the power and the silicon area of the anti-aliasing filter in front of the ADC should be taken into account. The use of a mixed feedforward-feedback compensation technique is a good compromise because it is power efficient while reducing the STF peaking [19].

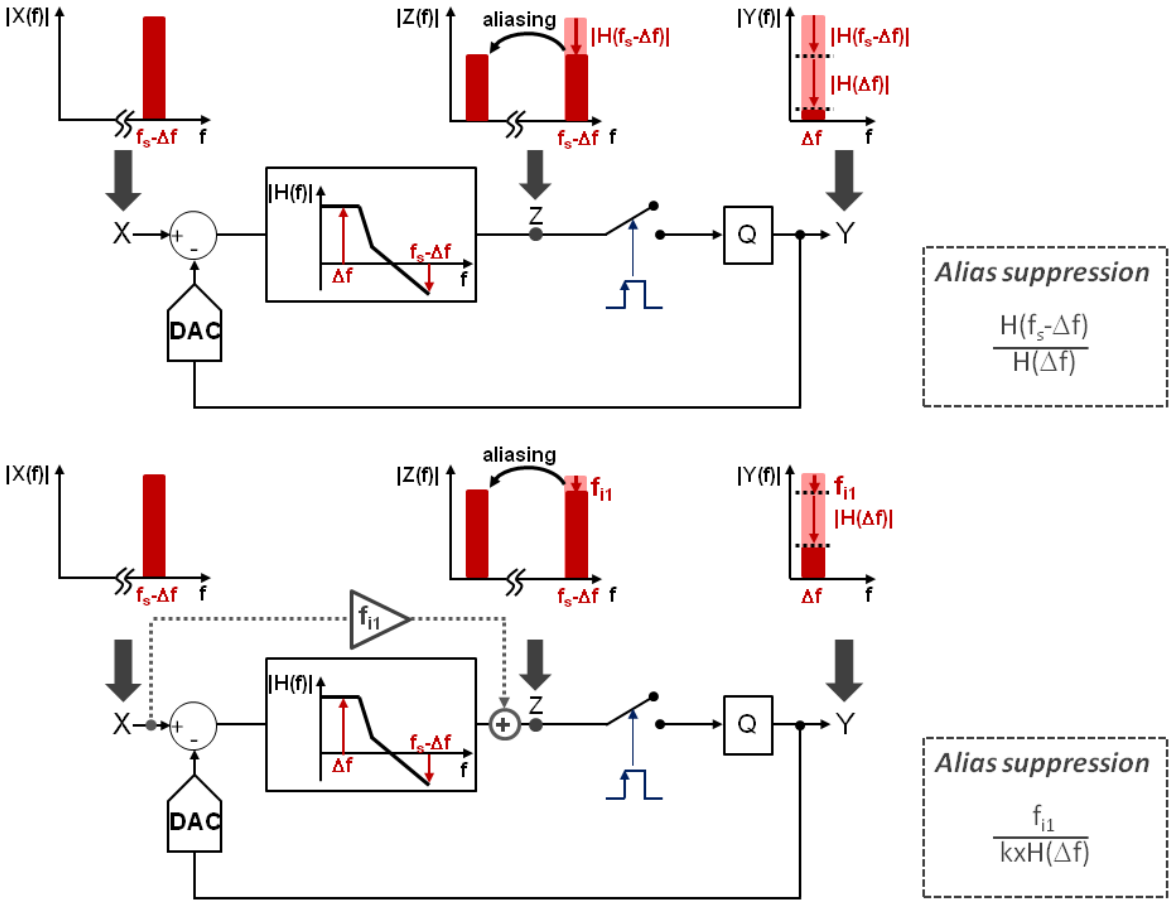


Figure 2-6. Anti-aliasing mechanism in CT ΔΣ modulator (a) without input feed-in coefficient, (b) with an input feed-in coefficient.

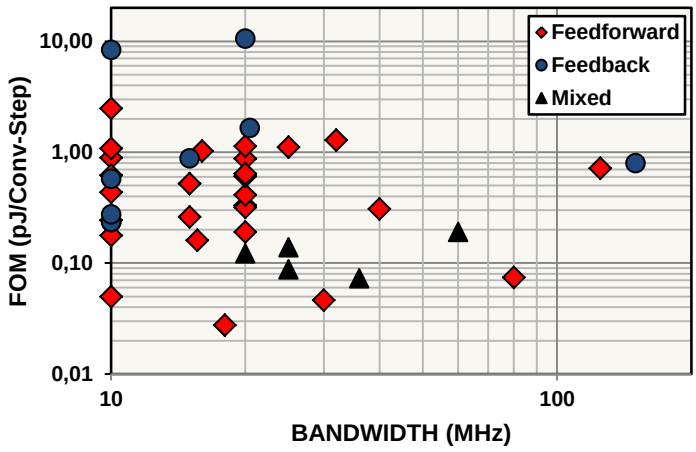


Figure 2-7. Loop filter architectures used in wideband ΔΣ modulators prototype.

2.2.2 Loop-filter implementation: Discrete-Time, Continuous-Time or Hybrid

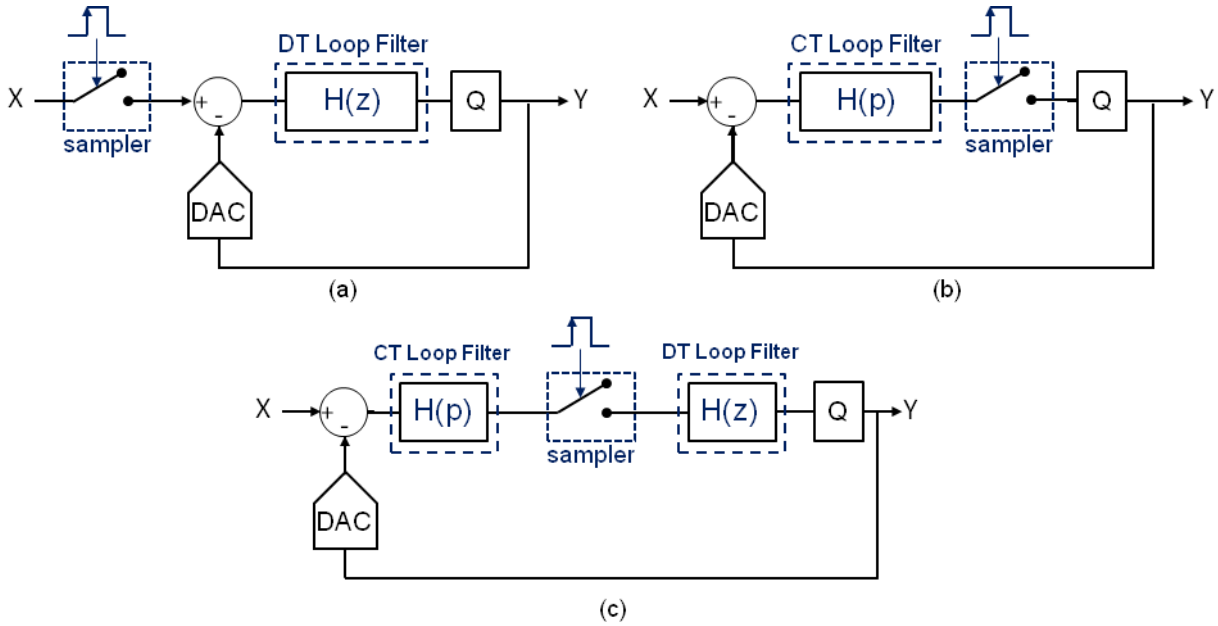


Figure 2-8. Implementation of a ΔΣ modulator with (a) DT loop-filter, (b) CT loop-filter, (c) Hybrid DT/CT loop filter.

The fundamental difference between the DT and the CT implementation is the place at which the sampling process occurs. In the case of a DT implementation, it occurs at the input of the modulator, i.e. outside the ΔΣ loop while it occurs inside the ΔΣ loop in the case of a CT implementation, as shown in Figure 2-8(a) and Figure 2-8(b) respectively.

Thus, the CT implementation provides several attractive advantages over the DT implementation such as reduced requirements on the sampler and an inherent anti-alias filtering function because both the sampler imperfections and the alias that may fall back at baseband are attenuated by the loop filter.

Moreover, the input impedance of the front-end is not "switching", which does not emit signal-dependent charges back to the package pins. This feature simplifies the design of the ADC driver. In addition, a CT implementation is less prone to signal-dependent glitches that are coupled to the first stage of the modulators through the power supply, bias lines or the substrate. Finally, in DT implementation, the virtual ground of the main integrator must absorb a peak voltage during a short amount of time which requires a high dc gain to avoid harmonic distortion.

Discrete-Time (DT) implementation was used at the earlier story of the ΔΣ modulator. Advantages are the robustness of the loop filter coefficient against PVT variations and the natural scaling of the NTF with the clock frequency of the modulator. Furthermore, a DT DAC has lower sensitivity to transient errors such as clock jitter compared to its CT counterpart in which the full DAC-pulse is continuously processed by the loop filter over time. It should be noted that a switched-capacitor DAC can be used in a CT modulator to reduce the effect of clock jitter [20]. However, in that case, a careful attention must be paid to preserve the anti-aliasing property of the CT modulator [21].

Another fundamental advantage of the CT implementation, especially for low-power application, is the speed requirement on the loop filter. In a CT modulator, the integrators have a full clock period for settling which results in a GBW requirement in the range of f_s [22] while in a DT modulator a GBW of $5xf_s$ is a rule of thumb [23]. This has allowed implementing wideband CT ΔΣ modulators with outstanding power efficiency as shown in Figure 2-9.

An attractive compromise that was introduced in [24] is the hybrid architecture which combines most of the advantages of DT and CT implementations. This architecture is shown in Figure 2-8(c). It consists in implementing the front-end stage with CT circuits while others stages are made of DT circuits.

It is interesting to note that even if the hybrid architecture combines robustness, good power efficiency and anti-aliasing properties, its implementation has been limited to narrow band or medium band applications such as audio [24-27], analog FM-radio [28], or 2G/3G cellular phone [29] and does not appear in the wideband modulators presented in Figure 2-9.

The linearity of wideband implementations was also reported in Figure 2-10. It is interesting to see that wideband CT realizations achieve the best Total Harmonic Distortion (THD).

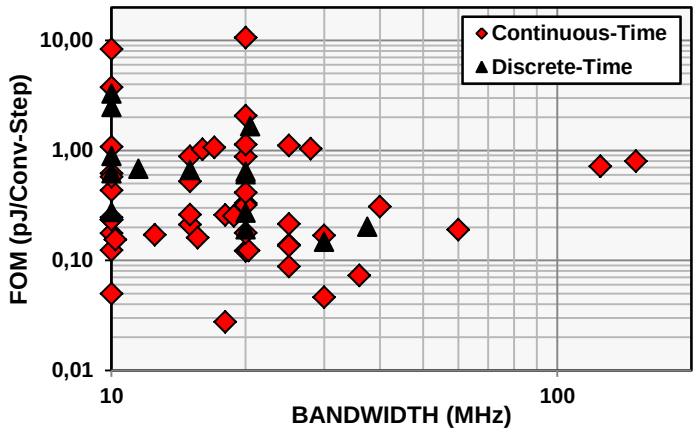


Figure 2-9. FoM repartition as a function of signal bandwidth for CT and DT wideband ΔΣ modulators.

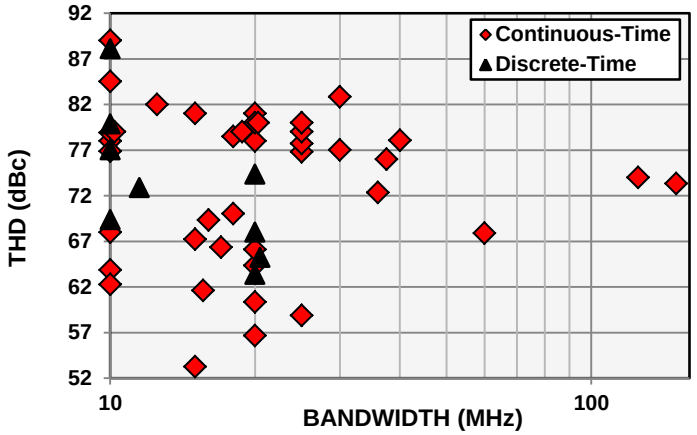


Figure 2-10. Linearity repartition as a function of the signal bandwidth for CT and DT wideband ΔΣ modulators.

2.2.3 Fundamental parameters: L, N, OSR

The theoretical dynamic range of a ΔΣ modulator employing pure differentiation noise transfer function depends on the oversampling ratio (OSR), the order of the noise shaping L, and the internal quantizer resolution N, as expressed by equation (2-5) [15]:

$$\mathbf{DR} = \mathbf{1} + \frac{\mathbf{3}}{\mathbf{2}}\left(\frac{\mathbf{2L+1}}{\boldsymbol{\pi}^{\mathbf{2L}}}\right)(\mathbf{2^N - 1})^{\mathbf{2}}\mathbf{OSR}^{\mathbf{2L+1}} \quad (2\text{-}5)$$

In broadband applications that require high resolution (ENOB≥11-bit), it is common to use a low OSR value (≤32) and a multi-bit quantizer rather than a mono-bit quantizer with a high OSR, as shown in Figure 2-11. It should be noted also that whatever the quantizer type, a high order loop filter is mostly employed to get a SQNR well beyond 11-bit.
A low OSR reduces the speed requirement on the loop filter because the finite gain-bandwidth product (GBW) of the opamp used in the first integrator, which is the most sensitive, could be as low as the sampling frequency value [22]. The power consumption of the multi-bit quantizer, which requires several comparators, is relaxed as well. On the top of that, a non-negligible amount of power is saved in the digital gates that are used in the clock distribution circuits and data buffers.
Besides choosing a low OSR value, the multi-bit approach reduces the voltage swing inside the loop filter and improves the stability of the modulator, allowing aggressive noise shaping.
For each quantization bit added, the sensitivity to the clock jitter is reduced by 6dB if a Non-Return to Zero (NRZ) DAC is used [20].
But multi-bit quantizers are usually considered to consume a large silicon area and high power consumption. Furthermore, as the loop filter is loaded by the quantizer, the input capacitance of the comparators may be an issue if the resolution goes beyond 3-bit. However, techniques such as calibration [2], averaging, interpolation and the used of fully dynamic architectures [30] may help to reduce both power and area, resulting in multi-bit implementation with very low complexity and excellent power efficiency.
In nanoscale process, time-domain quantizer may be an interesting approach to the traditional flash architecture [31] [32]. Finally, SAR quantizers are also an attractive solution that has already been implemented with low area and good power efficiency [33].

The other architectural alternative to build a wideband ΔΣ modulator is to use a mono-bit quantizer clocked with a high OSR value. Regarding the power consumption and the complexity of the quantizer and the DAC only, this solution is by far the most efficient. But according to the Figure 2-12, this is not obvious when we consider the ΔΣ modulator as a whole.
Despite the few number of ΔΣ modulators that use a mono-bit quantizer, this observation can be justified as follows. Mono-bit quantizers are more sensitive to the clock jitter which means that either the thermal noise contribution of the loop filter should be lowered or the phase noise performance of the clock source must be improved to keep the same resolution. Both choices decrease the power efficiency and increase the area of the ADC.
Another severe drawback of the mono-bit architecture is the higher quantization noise that must be processed by the loop filter which results in stringent requirements on the opamp performance such as, speed, slew rate and voltage swing. A multi-tap FIR DAC could reduce both the sensitivity to the clock jitter and the voltage swing of the integrators [34] but it requires additional circuitry to preserve the loop stability which increases the complexity and the power consumption of the modulator.
Regarding stability, the out of band gain of the NTF must be lower than 1.5 for a mono-bit quantizer [5] while its value can be as high as 4 with a multi-bit quantizer [2], resulting in a higher dynamic range for a multi-bit quantizer. Typically, a ΔΣ modulator with a mono-bit quantizer has a modulation depth of 70% [5] while a multi-bit quantizer can achieve 95% [35].
The inherent linearity of a two-level DAC is probably the most claimed advantage of a ΔΣ modulator that uses a mono-bit quantizer. However, many other distortion mechanisms affect strongly the linearity performance of mono-bit modulators, especially in wideband applications.
Because a real opamp has a finite GBW, a residual voltage swing is present at the virtual ground of the integrator. As explained later in Chapter 3, this creates harmonic distortion and the higher the voltage swing, the higher the performance degradation. As the loop filter must process higher quantization noise in the mono-bit architecture, the voltage swing at the virtual ground of the integrators is higher than in the multi-bit case. To reduce this effect, the GBW must be increased which require additional current in the opamp.

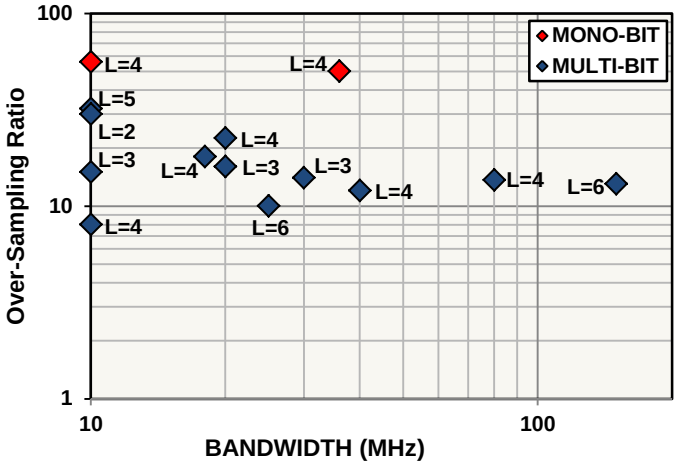


Figure 2-11. Over-Sampling Ratio as a function of the signal bandwidth of wideband L^{th}-order $\Delta\Sigma$ modulator with ENOB≥11-bit.

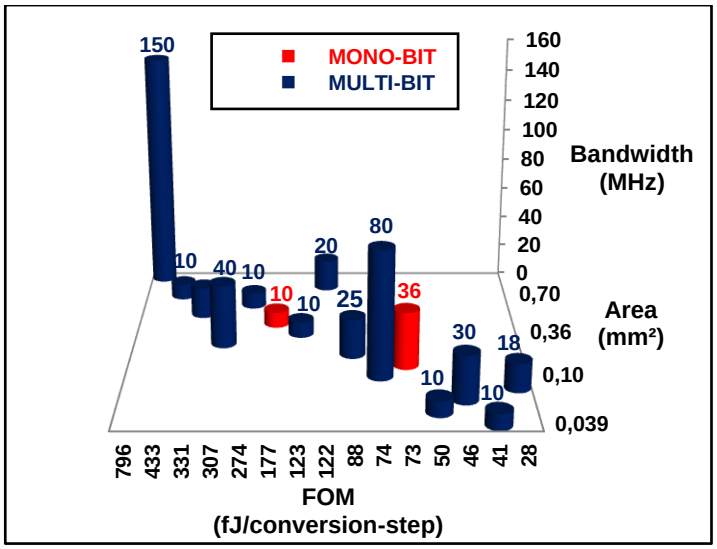


Figure 2-12. 3D plot of the signal bandwidth as a function of the FoM and silicon area of wideband $\Delta\Sigma$ modulators.

It means that for the same biasing current, the harmonic distortion in the loop filter is higher when a mono-bit quantizer is used.
Mono-bit implementation (and multi-bit quantizer as well) suffers from Inter Symbol Interference (ISI) in the DAC [20] which degrades severely the noise and linearity performance of the modulator. This phenomenon is explained in detail in Chapter 5. Generally speaking, transient errors such as ISI and jitter worsen in wideband applications because the portion of the DAC pulse that is affected with these transient errors is higher. But this is particularly exacerbated in mono-bit architecture because the clock frequency is higher than in the multi-bit case. The use of a Return-to-zero (RZ) DAC reduces the sensitivity to ISI but at the cost of increased sensitivity to clock jitter.
The main drawback of multi-bit quantizers is their sensitivity to the mismatch between the unit current cells of the DAC. However, it is interesting to note in Figure 2-14 that the linearity of mono-bit quantizer is not better than those of the multi-bit, which proves that the mismatch is not the limiting factor to achieve high linearity.
Three approaches are used to reduce the DAC mismatch-induced noise and distortion as shown in Figure 2-15. A design-oriented approach that is delay-free consists in sizing the unit current cells of the DAC such as their inherent matching satisfies the noise and linearity specifications.
However, this approach increases the die area of the unit current cell because the standard deviation of the mismatch is inversely proportional to the squared root of the transistor area [36]. This results also in a higher capacitance at the output node of the DAC that is connected to the virtual ground of the integrator, which reduces both the output impedance of the DAC and the GBW of the opamp and translates in increased harmonic distortion. This technique is mostly used in very high speed modulators [18] [37] in which the very short amount of loop delay does not allow to implement a correction algorithm such as Dynamic Element Matching (DEM). Furthermore, the design approach is adapted to applications that require THD performance below 78dBc. It should be noted that the threshold voltage mismatch (A_{VT}) decreases with CMOS scaling [38] as shown in Figure 2-13 which makes this technique attractive in high-speed applications.
DEM techniques such as the DWA algorithm [39] have proven to be very efficient up to 20MHz. But as the signal bandwidth increases, the latency of the DWA circuit becomes an issue. Furthermore, special attention must be taken in the presence of ISI in the DAC. This point will be explained in details in Chapter 5. Beyond 10MHz the calibration [30] [40] is the most popular technique because it does not add delay in the feedback path while allowing to reach nearly 14-bit of linearity [40].

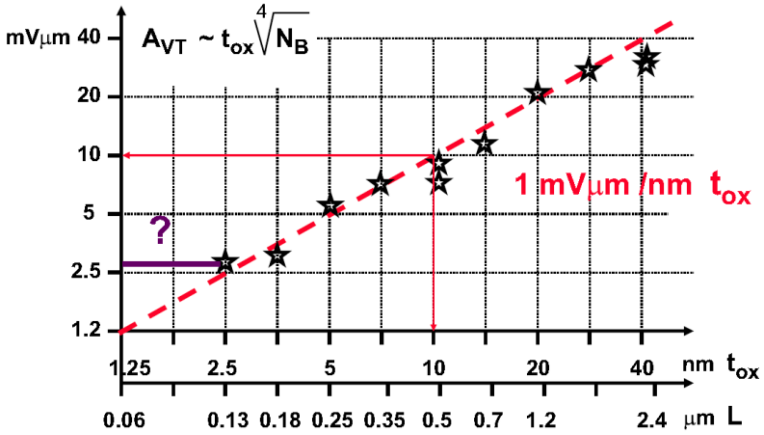


Figure 2-13. Threshold-voltage constant mismatch (A_{VT}) evolution as a function of CMOS technological node [38].

Table 2-2. Comparison of mono-bit and multi-bit architecture in broadband ΔΣ modulators

PARAMETERS	MONO-BIT	MULTI-BIT
Stability	--	++
Loop filter requirements	--	++
Clock jitter	--	++
Dynamic range	--	++
Linearity	+	-
Power	+	-
Area	+	-

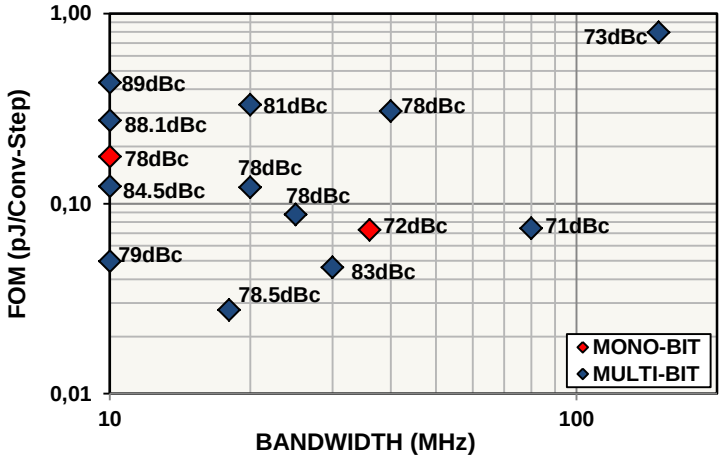


Figure 2-14. FoM repartition as a function of signal bandwidth for wideband mono-bit and multi-bit ΔΣ modulator with ENOB≥11-bit.

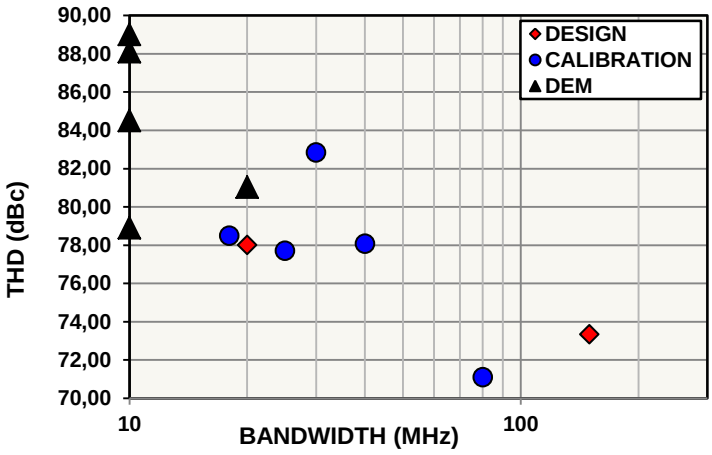


Figure 2-15. THD repartition as a function of signal bandwidth in multi-bit ΔΣ modulators (ENOB≥11-bit) that use three techniques to reduce mismatch-induced noise and distortion.

2.3 Proposed architecture and specifications

Table 2-3. ΔΣ ADC specifications

PARAMETERS	VALUE	UNIT
Over-Sampling Ratio	8	_
Signal bandwidth	40	MHz
Sampling frequency	640	MHz
SNR	74	dBc
THD	86	dBc
SNDR	74	dBc
ENOB	12	Bit
Power	<100	mW
FoM	<305	fJ/conversion-step
CMOS process	65nm	_

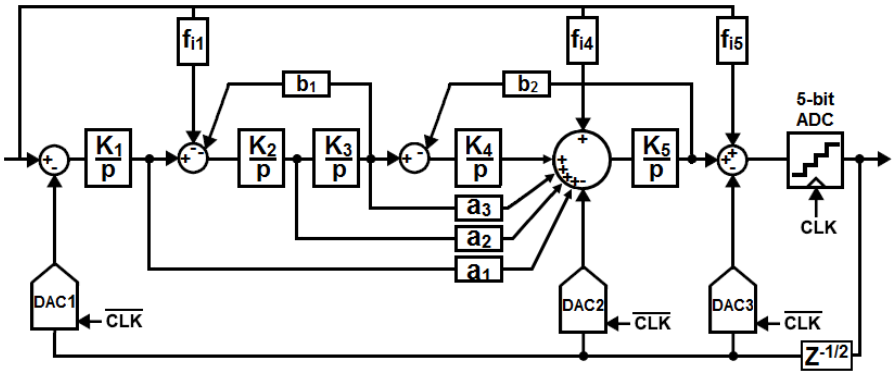


Figure 2-16. Architecture of the proposed CT ΔΣ modulator.

The specifications of the ΔΣ ADC are summarized in Table 2-3. The circuit is targeted for applications that demand high bandwidth, high resolution, and low power, such as wireless and wireline communications, medical imaging, video, and instrumentation. To meet these specification, and based on the previous analysis and our experience, we have purposed the ΔΣ modulator architecture shown in Figure 2-16. Now we detailed the advantages of our architecture.

Due to the feedback path around the 5th integrator, the first order path is composed of the 5th integrators rather than the 1st integrator which relax the speed requirement on the first opamp1 [3].

An OSR of only 8 is chosen to reduce the speed requirement of the loop filter and the multi-bit quantizer which results in a low power consumption of the analog part. As the maximum input signal bandwidth is 40MHz, the ΔΣ modulator is clocked at a fixed frequency of 640MHz. The choice of the OSR value was done keeping in mind also the design of the digital decimation filter that may consume as much power as the ΔΣ modulator [2]. For example, the wideband ΔΣ modulator described in [34] achieves outstanding power efficiency but the modulator sampling rate of 3.6GS/s defers a serious challenge on the design of the digital decimation filter. Furthermore, lowering the switching-rate of the digital part reduces the crosstalk through the substrate.

To compensate for the lower noise-shaping performance at low-OSR, a 5th-order NTF with a maximum gain (Q_{max}) of 12dB and a 5-bit quantizer are combined to keep the quantization noise level well below the ADC noise floor which is dominated by the thermal noise of the modulator front end. A high Q_{max} value is also required to reduce the inherent tonal behavior of high-order ΔΣ loops working at low-OSR, which results in a modulator with poor stability [41]. To address this issue, the signal feed-in paths f_{i1}, f_{i4} and f_{i5} are added.

The feed-in coefficient f_{i5} from the input of the modulator to the input of the quantizer has two purposes. Firstly, it bypasses the loop filter that adds phase shift to the input signal. The resulting "delay-free" path allows the quantizer to faster track the variation of the input signal. Secondly, together with the feed-in paths f_{i1} and f_{i4}, they prevent most signal energy from leaking into the loop filter, which strongly reduces the voltage excursion at integrators outputs, as shown in Table 1-4.

Table 2-4. Simulation of the Integrators output swing

PARAMETERS	Without Feed-in	With Feed-in
Modulator input frequency	1MHz	1MHz
Modulator input amplitude	-4.4dBFS	-4.4dBFS
Quantizer reference (Full Scale)	800mV	800mV
Maximum output Swing		
Integrator 1	±261mV	±235mV
Integrator 2	±247mV	±67mV
Integrator 3	±313mV	±52mV
Integrator 4	±450mV	±48mV
Integrator 5	±766mV	±421mV

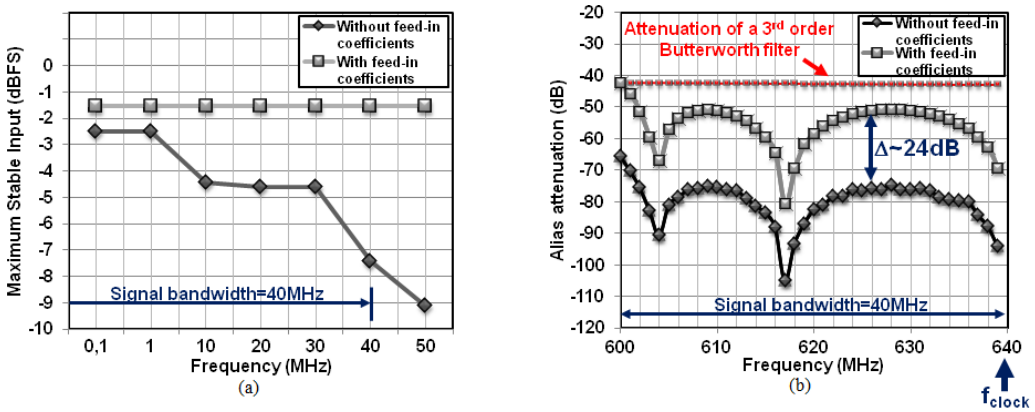


Figure 2-17. Feed-fin coefficients effect on (a) the maximum stable input amplitude, (b) the inherent anti-alias filter transfer function.

It results in a stable architecture that prevents from overload for full-scale input signals within the full bandwidth of the modulator, as illustrated in Figure 2-17(a). The modulation index is 0.85. Clocked at 640MHz, the $\Delta\Sigma$ modulator achieves a signal-to-quantization noise ratio greater than 90dBc over a 40MHz bandwidth.
While feed-in coefficients has the proven benefit of reducing the voltage swing inside the loop filter, it is rarely recalled that it is at the price of less alias rejection, as shown in Figure 2-17(b). This is because feed-in coefficients flatten the Signal Transfer Function (STF) out of the signal bandwidth.
In this design, the worst case out-of-band component that may fall back within the signal bandwidth is attenuated by 42.3dB. For comparison with what would be obtained by using an anti-alias filter in front of the ADC IC, the inherent anti-alias filter provides the same attenuation at 600MHz than a third-order Butterworth filter that has a maximum attenuation of 1dB at the edge of the signal band.

While a 4-bit flash-based quantizer has been extensively used in previous wideband architectures [2,22], going to 5-bit reduces the maximum voltage swing inside the loop filter by a factor of two at least which improves the compromise between power and distortion. Other benefits are a better trade-off between stability and dynamic range. Furthermore, the DAC sensitivity to jitter is reduced which allows relaxing the phase noise requirement on the system clock-source. To make the jitter noise contribution negligible, the rms value of the clock-source jitter must not exceed 1ps. This target value can be achieved with reasonable power consumption by an LC-PLL [2]. To reduce the current consumption and the input capacitance of the 5-bit flash quantizer, the devices inside the comparators are intentionally sized small and the resulting random offset is calibrated to meet the linearity requirement. DWA is chosen to correct mismatch-induced noise and distortion of the main DAC. As a high Q_{max} NTF is implemented, this technique is efficient even at low OSR [41].
An explicit loop delay of one-half the clock period is inserted in the feedback path to absorb the delay of the DWA and the intrinsic time response of the quantizer, which reduces the risk of having metastability-induced errors. This delay is compensated with a feedback loop around the quantizer.
To reduce capacitive loading at the virtual ground of the 5th integrator and relax speed requirement on opamp5, the unit current cells of both DAC2 and DAC3 are scaled aggressively compared to those in DAC1. As a result, the DWA technique is also applied to these DACs to reduce their mismatch-induced spurs that are weakly attenuated by the loop filter at low OSR.

2.4 Summary

In this chapter we studied different ΔΣ modulator architectures, both from the market side and the research side. We specifically focused on wideband architectural trends used the last ten years. This study has shown that the single-loop architecture is mostly used over its multi-stage counterpart. Regarding the single-loop architecture, two approaches are mostly employed to implement it.
The mono-bit approach associated to a high OSR value and a high-order loop filter may be a first solution. However, practical considerations such as, the design of the decimation filter or the clock circuitry, the propagation of the digital noise through the substrate, among others, makes the design of the ADC as a whole, very challenging.
It seems that high-order multi-bit ΔΣ modulators with a low OSR value are a more natural choice for wideband, high resolution applications that require low power consumption.

Based on this study and our experience, the proposed architecture was built around the last approach. To deal with the high-resolution requirement and the low-power constraint, we have increased the quantizer resolution to 5-bit while lowering the OSR value to 8.
This unusual choice of resolution facilitates on the one hand, the integration of our ADC into a complete system because the constraint on the clock jitter is relaxed. Moreover, the design constraints on the loop filter of the modulator itself are also reduced. The impact of this architectural choice on the power consumption of the modulator is addressed at circuit level, as explained in Chapter 5.
An OSR of 8 was chosen to minimize the clock speed, which results in a reduction of the power consumption of the modulator and the associated decimation filter. The stability problems associated with the use of a low OSR are resolved by injecting a fraction of the input to various nodes of the loop filter signal.
The targeted performance of 12-bit ENOB and 14-bit THD allows covering a wide range of applications such as wireless and wireline communications, medical imaging, video, and instrumentation. This performance goal is compared to the state of the art in Figure 2-18.

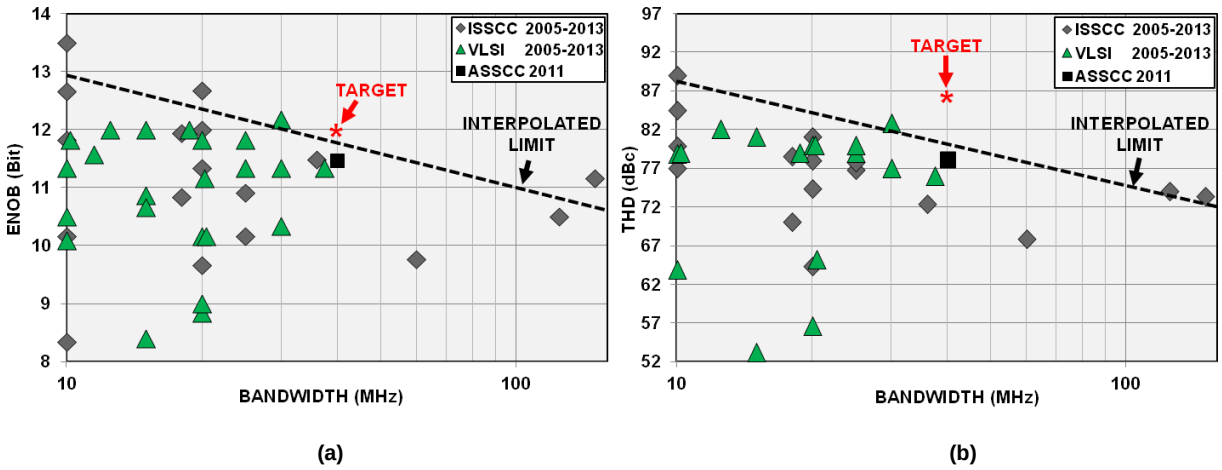


Figure 2-18. Target specifications of the ΔΣ ADC and comparison to the state of the art (a) THD, (b) ENOB.

In the next chapter, we identify the imperfection sources that may degrade the performance of the proposed architecture. Based on these considerations we purpose a behavioral model that allows simulating and quantizing these non-idealities. This design step allows translating the performance requirements such as ENOB and THD into circuit-level requirement.

2.5 References

[1] http://www.ti.com/lit/ds/symlink/adc12eu050.pdf

[2] G. Mitteregger, et al., "*A* 14 b 20 mW 640 MHz CMOS CT $\Delta\Sigma$ ADC with 20MHz signal bandwidth and 12b ENOB," ISSCC Dig. Tech. Papers, pp. 62–63, February. 2006.

[3] W. Yang et al., "A 100mW 10MHz-BW CT $\Delta\Sigma$ Modulator with 87dB DR and 91dBc IMD," ISSCC Dig. Tech. Papers, pp. 498–500, February 2008.

[4] http://www.analog.com/

[5] S. R. Norsworthy, R. Schreier, G. Temes, "Delta-Sigma Data Converters, Theory, Design and Simulation," IEEE Press, 1996.

[6] Trevor C. Caldwell and David A. Johns, "An 8th-Order MASH Delta-Sigma with an OSR of 3," ESSCIRC Dig. Tech. Papers, Sept. 2009.

[7] Todd L. Brooks et al., "A Cascaded Sigma–Delta Pipeline A/D Converter with 1.25 MHz Signal Bandwidth and 89 dB SNR," IEEE J. Solid-State Circuits, vol.32, no. 12, pp. 1896–1906, December 1997.

[8] Alessandro Bosi et al., "An 80MHz 4x Oversampled Cascaded $\Delta\Sigma$-Pipelined ADC with 75dB DR and 87dB SFDR," ISSCC Dig. Tech. Papers, pp. 174–176, February 2005.

[9] Ahmed Gharbiya and David A. Johns, "A 12-bit 3.125 MHz Bandwidth 0–3 MASH Delta-Sigma Modulator," IEEE J. Solid-State Circuits, vol.44, no. 7, pp. 2010–2018, December 2009.

[10] L. J. Breems, "A cascaded continuous-time $\Sigma\Delta$ modulator with 67-dB dynamic range in 10-MHz bandwidth," ISSCC Dig. Tech. Papers, February 2004.

[11] Junpei Kamiishi et al., "A Self-Calibrated 2-1-1 Cascaded Continuous-Time $\Delta\Sigma$ Modulator," IEEE CICC Dig. Tech. Papers, pp. 9–12, September 2009.

[12] L. J. Breems, R. Rutten, R. H. M. van Veldhoven, and G. van der Weide, "A 56 mW continuous-time quadrature cascaded $\Sigma\Delta$ modulator with 77dB DR in a near zero-IF 20 MHz band," IEEE J. Solid-State Circuits, vol.42, no. 12, pp. 2696–2705, December 2007.

[13] Yun-Shiang Shu et al., "LMS-Based Noise Leakage Calibration of Cascaded Continuous-Time Modulators," IEEE J. Solid-State Circuits, vol.45, no. 2, pp. 368–379, February 2010.

[14] M. Ortmanns, F. Gerfers, "Continuous-time sigma-delta A/D conversion : fundamentals, performance limits and robust implementations," Springer edition, 2006.

[15] Nima Maghari, Sunwoo Kwon and Un-Ku Moon, "74dB SNDR Multi-Loop Sturdy-MASH Delta-Sigma Modulator Using 35dB Opamp Gain," CICC Dig. Tech. Papers, pp. 101-104, September 2008.

[16] Yunzhi Dong et al., "A 235mW CT 0-3 MASH ADC Achieving -167dBFS/Hz NSD with 53MHz BW," ISSCC Dig. Tech. Papers, pp. 480-482, February 2014.

[17] J. Silva et al., "Wideband low-distortion delta-sigma ADC topology," Electronics Letters, Vol.37, No12, June 2001.

[18] Hajime Shibata et. al., "A DC-to-1GHz Tunable RF $\Delta\Sigma$ ADC Achieving DR = 74dB and BW = 150MHz at f_0 = 450MHz Using 550mW," ISSCC Dig. Tech. Papers, pp. 151–153, February 2012.

[19] F. Munoz et al., "A 4.7mW 89.5dB DR CT Complex $\Delta\Sigma$ ADC with Built-In LPF," ISSCC Dig. Tech. Papers, pp. 500-501, February 2005.

[20] J. A. Cherry, W. M. Snelgrove, "Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion," Kluwer Academic Publishers, 2000.

[21] Shanti Pavan, "Alias Rejection of Continuous-Time $\Sigma\Delta$ Modulator With Switched-Capacitor feedback DACs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 58, NO. 2, pp. 233–243, February 2011.

[22] J. G. Kauffman et al., "An 8mW 50MS/s CT $\Delta\Sigma$ Modulator with 81dB SFDR and Digital Background DAC Linearization," ISSCC Dig. Tech. Papers, pp. 472–474, February 2011.

[23] Su-Hao Wu et al., "A 81-dB Dynamic Range 16-MHz Bandwidth Modulator Using Background Calibration," J. Solid-State Circuits, vol.48, no. 9, pp. 2170–2179, September 2013.

[24] B. DelSignore et al., “A Monolithic 20b Delta-Sigma A/D Converter,” ISSCC Dig. Tech. Papers, pp. 170-172, February 1990.

[25] K. Nguyen et al., “A 106 dB SNR Hybrid Oversampling ADC for Digital Audio,” ISSCC Dig. Tech. Papers, pp. 244-245, February 2005.

[26] Paul Morrow et al., “A 0.18µm 102dB-SNR Mixed CT SC Audio-Band ΔΣ ADC,” ISSCC Dig. Tech. Papers, pp. 178-180, February 2005.

[27] Tien-Yu Lo, “A 102dB Dynamic Range Audio Sigma-Delta Modulator in 40nm CMOS,” ASSCC Dig. Tech. Papers, pp. 257-260, November 2011.

[28] R. Schreier et al., “A 10-300-MHz IF-digitizing IC with 90-105dB dynamic range and 15-33-kHz bandwidth,” IEEE J. Solid-State Circuits, vol.37, no. 12, pp. 1636–1644, December 2002.

[29] B. Putter, “A 5^{th}-order CT/DT Multi-Mode ΔΣ Modulator,” ISSCC Dig. Tech. Papers, pp. 244-245, February 2007.

[30] Y. Shu et al., “A 28fJ/conv-step CT ΔΣ Modulator with 78dB DR and18MHz BW in 28nm CMOS Using a Highly Digital Multibit Quantizer,” ISSCC Dig. Tech. Papers, pp. 268–270, February 2013.

[31] Matt Park, Michael Perrott, “A 0.13µm CMOS 78dB SNDR 87mW 20MHz BW CT ΔΣ ADC with VCO-Based Integrator and Quantizer,” ISSCC Dig. Tech. Papers, pp. 170-172, February 2009.

[32] Enrique Prefasi et al., “A 0.08 mm2, 7mW Time-Encoding Oversampling Converter with 10 bits and 20MHz BW in 65nm CMOS,” ESSCIRC Dig. Tech. Papers, pp. 430-433, September 2009.

[33] Chun C. Lee et al., “A 66dB 15MHz BW SAR Assisted ADC in 22nm Tri Gate CMOS,” VLSI Dig. Tech. Papers, June 2013.

[34] Pradeep Shettigar, et al., “A 15mW 3.6GS/s CT- ΔΣ ADC with 36MHz Bandwidth and 83dB DR in 90nm CMOS,” ISSCC Dig. Tech. Papers, pp. 155–157, February 2012.

[35] YuQing Yang, Terry Sculley, and Jacob Abraham, “A Single-Die 124 dB Stereo Audio Delta-Sigma ADC With 111 dB THD,” IEEE J. Solid-State Circuits, vol.43, no. 7, pp. 1657–1665, July 2008.

[36] Marcel J. M. Pelgrom, “Matching Properties of MOS Transistors,” IEEE J. Solid-State Circuits, vol.24, no. 5, pp. 1433–1440, October 1989.

[37] Muhammed Bolatkale et al., “A 4GHz CT ΔΣ ADC with 70dB DR and –74dBFS THD in 125MHz BW,” ISSCC Dig. Tech. Papers, pp. 470-472, February 2011.

[38] Willy M.C. Sansen, “Analog Design Essentials,” Springer edition, 2006.

[39] R. T. Baird, T. S. Fiez, “Improved ΔΣ DAC linearity using data weighted averaging,” International Symposium on Circuits and Systems, 1995.

[40] Chi-Lun Lo et al., “A 75.1dB SNDR 840MS/s CT ΔΣ Modulator with 30MHz Bandwidth and 46.4fJ/conv FoM in 55nm CMOS,” VLSI Dig. Tech. Papers, June 2013.

[41] Ruoxin Jiang,Terri Fiez, “A 14-bit ΔΣ ADC With 8x OSR and 4-MHz Conversion Bandwidth in a 0.18µm CMOS Process”, J. Solid State Circuits, vol. 39, pp.63-74, January 2004.

Chapter 3

System-Level Design

3.1 General considerations

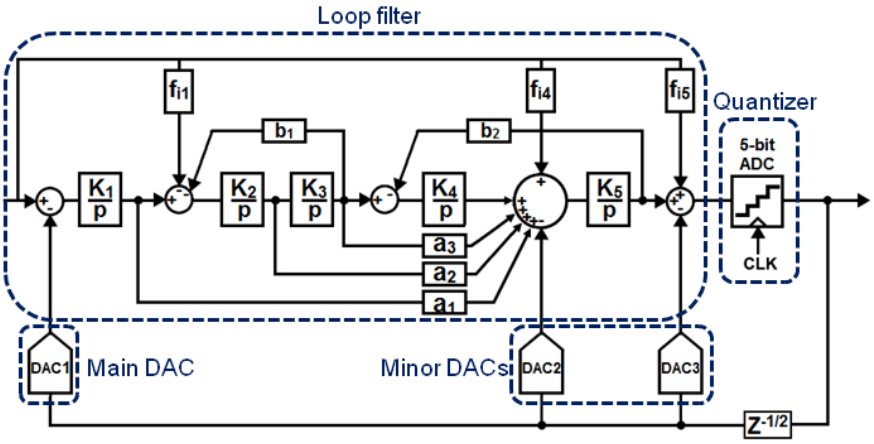


Figure 3-1. Schematic of the ΔΣ modulator with the main sub-blocks identified.

The block diagram representation of the ΔΣ modulator is repeated in Figure 3-1 for clarity. The main building blocks are highlighted and consist of the loop filter, the quantizer and the feedback DACs which are distinguished between the main DAC whose imperfections are not shaped by the loop filter and the minor DACs whose imperfections are shaped by the loop filter just like the quantization noise is.

The goal of the system-level design is to quantify with an acceptable accuracy and in a reasonable time, the impact of the non-idealities that affect the performance of the ΔΣ modulator. This information will be exploited to set the circuit-level requirement on each building-block of the ΔΣ modulator. Behavioral modeling and simulation of the non-idealities impact are done with Matlab [1]. The computation of the ΔΣ modulator coefficients was done with Schreier's toolbox [2] and the conversion procedure used to obtain an equivalent CT system is detailed in [3].

The simulated STF and NTF of the ideal ΔΣ modulator are shown in Figure 3-2 and Figure 3-3 respectively. While the STF is almost flat within the signal band (ripple<0.1dB), it exhibits a wide peaking that span over about one decade out-of the signal bandwidth, with a maximum value of 14dB at 478MHz. As a consequence, the signal amplitude must be reduced out of the signal bandwidth to preserve the stability of the modulator. Careful attention must be paid for applications in which the signal is received in the presence of interferers. Even if the intrinsic anti-alias filter of the modulator provides enough attenuation of the interferers that may fall back within the signal bandwidth, certain type of modulator require a front-end filter to reduce the STF peaking [3]. The STF peaking is not investigated in this work since this problem is well known in the literature [4] and many solutions have been proposed to overcome it [5] [6] [7] [8]. A more recent solution is also detailed in Chapter 6 of this manuscript.

Figure 3-3 shows the power spectral density (PSD) of the modulator output in which the shape of the 5^{th} order NTF is clearly visible. An inverse Chebyshev NTF was implemented since it provides a more uniform attenuation of the quantization noise within the band of interest. This is done by adding feedback coefficients b_1 and b_2 around the pair of last integrators. The notches created by the pair of resonators are visible in Figure 3-3. Compared to a 5^{th} order Butterworth NTF that has all the zeros at DC and a sharp rise of the quantization noise at the edge of the bandwidth, the improvement in the SQNR value is 18dB [9].

The PSD of Figure 3-3 is obtained from the ideal model, i.e., without non-idealities. The ideal performance within the band of interest is limited by the quantization noise only and the simulated SQNR is ~92dB for an input signal of -1.1dBFS which is the maximum stable amplitude (MSA) of the

ideal modulator. The goal of the next sub-sections is to identify each source of imperfections that reduces the SQNR from its ideal value.
Except otherwise specified, all the simulations are done with the quantizer having a voltage reference (V_{REF}) of 0.8V which represents the ADC Full Scale (FS).

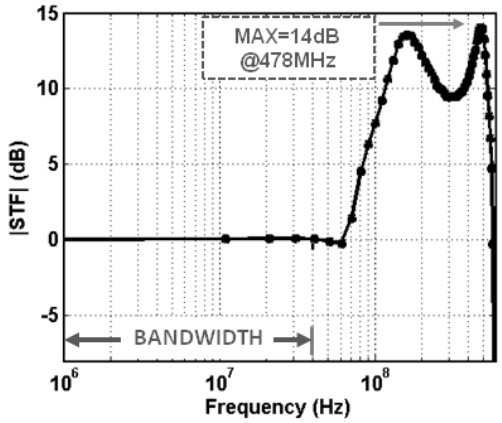


Figure 3-2. Signal Transfer Function of the ΔΣ modulator simulated with a –12dBFS input signal whose frequency is swept from 1MHz up to 600MHz.

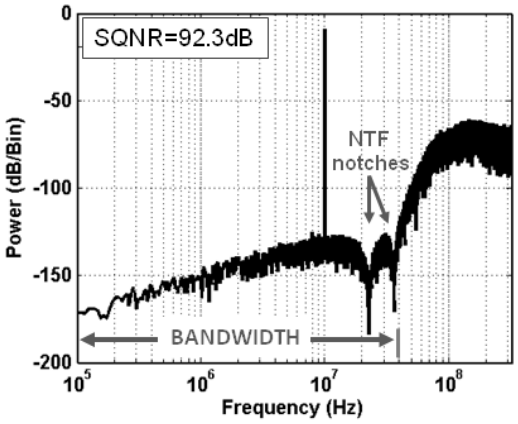


Figure 3-3. Output spectrum of the ΔΣ modulator (2^{16} FFT points and 2 times averaged) for a -1.1dBFS input @10MHz, showing the 5th order noise shaping.

3.2 Loop filter

3.2.1 Time constant of integrators

When high linearity is a targeted specification, an opamp-RC integrator is preferred to a gm-C structure. Moreover, due to its feedback configuration, the performance of an opamp-RC integrator is more robust to the imperfections of the opamp. The schematic of an opamp-RC based integrator is shown in Figure 3-4(a). A single-ended configuration is shown for simplicity. Assuming an ideal opamp, the transfer function of the ideal integrator is given by equation (3-1) whose derivation is detailed in annex A:

$$H_{i\_ideal}(p) = \frac{X}{Y} = -\frac{\omega_{ug}}{p} \quad (3\text{-}1)$$

where

$$\omega_{ug} = \frac{1}{RC} \quad (3\text{-}2)$$

ω_{ug} and the RC product are respectively the unit gain pulsation and the time constant of the ideal integrator. As the time constant is fixed by the product of the input resistance and the integrating capacitance, its value is poorly controlled during fabrication and may vary by more than ±35% in this process. As seen in Figure 3-4.b, such variations cannot be tolerated as the impact on the degradation of the SQNR is catastrophic. When the RC product is reduced, the higher gain of the integrators saturates the loop filter and the modulator becomes unstable which explains why the SQNR drops sharply beyond +10% variations. When the RC product increases, the noise shaping is less efficient as the integrator gain is reduced and the SQNR drops.
It should be noted that in this simulation all the time constants are varied at the same time which assumes that all the integrators are implemented with the same type of capacitor and resistor. In practice this is true however mismatch will create a systematic error between the time constant values.

The consequence of increasing and decreasing the time constant of all integrators together on the output voltage swing of the first integrator is shown in Figure 3-5(a) and Figure 3-5(b) respectively.
Fortunately, the time constant value may be corrected by using a calibration circuit that compensates for the RC shift due to process variation, either in the analog domain [10] or in the digital domain [11]. An accuracy better than ±2% can be obtained after correction [12]. When the sampling frequency of the clock must be reconfigurable, the appropriate calibration circuit must be chosen [13].
For applications in which the calibration is done only once at startup, the shift of the time constant due to the temperature-dependence of the resistors must be taken into account. In [14] 1% variation is obtained over the 40 °C to 105 °C range by combining two resistors that have temperature coefficient with opposite sign.
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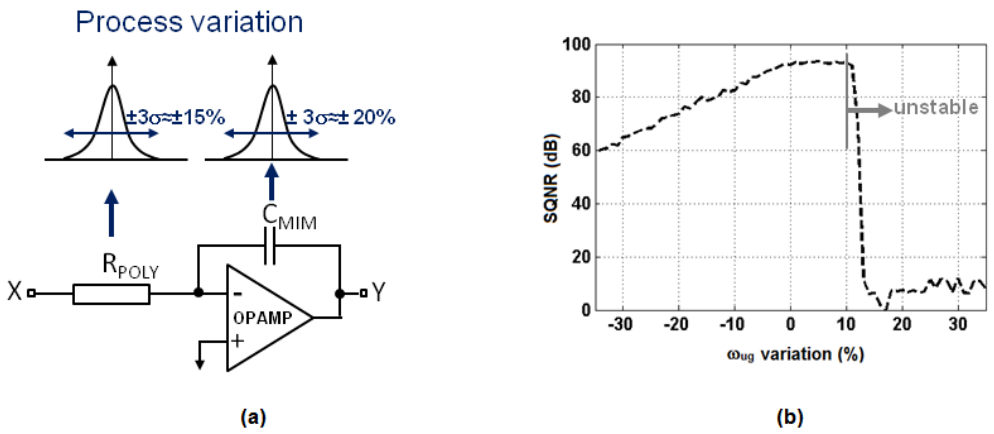


Figure 3-4. (a) Time constant shift due to the variation of R and C values after fabrication, (b) Simulated SQNR as a function of the time constant variation (inversely proportional to the unity-gain pulsation) of all the integrators together (f_{in}=39MHz & Vin=-1.1dBFS).

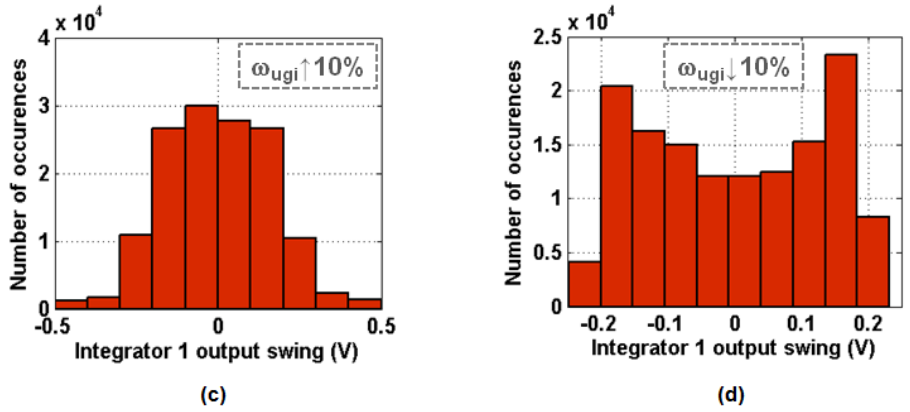


Figure 3-5. (a) Histogram of the voltage swing at the output of the first integrator, assuming +10% shift on the time constant of all-integrators, (b) Histogram of the voltage swing at the output of the first integrator, assuming -10% shift on the time constant of all-integrators.

3.2.2 Finite gain and GBW of the opamps

The structure of the loop filter is shown in Figure 3-6. It is composed of five integrators cascaded in the forward path of the modulator. The front-end integrator sets one of the NTF zeros at dc while the two others pairs of integrators are used as resonators that fix two zeros at the edge of the signal bandwidth.
Assuming a one-pole model for the opamp, the finite dc gain and the finite GBW both affect the gain and the phase of the ideal integrator whose real transfer function is given by equation 3-3.
As shown in Figure 3-7(a), the finite dc gain creates a dominant pole that increases the phase of the integrator compared to the ideal case while the finite GBW introduces a non-dominant pole that add phase lag and reduce the value of the integrator time constant. The shift of the time constant value from the ideal case can be approximated by the equation (3-5).
Regarding the resonators built around a pair of integrators, the finite dc gain of the opamp results in a quality factor that has a finite value and whose expression is given by equation (3-6). While the denominator of the quality factor is accurately set by components ratio (limited by matching however), its numerator is directly proportional to the dc gain value of the opamps.

The impact of the time constant error was studied in the paragraph 3.2.1. Regarding, the phase error, it affects the stability of the modulator and may result in a reduced dynamic range of the input signal. Both gain and phase errors can be corrected by coefficient tuning [14]. However the influence of finite gain impacts the SQNR and cannot be compensated.
A qualitative analysis of the influence of the finite opamp gain is shown in Figure 3-6. The finite gain of the main opamp impacts the quantization noise floor below 10MHz while the finite gain of the opamp-RC based resonators impact the noise performance at the edge of the bandwidth.
In the quantitative analysis shown in Figure 3-9, it seems that a gain of 40dB impacts negligibly the noise shaping performance. However, it should be noted that the imperfections of the successive integrators and DACs referred to the input of the modulator are less attenuated. This issue must be considered carefully especially when a low OSR value is used.

$$H_{i\_real}(p) = -\frac{A_o}{\left(\frac{A_o}{\omega_{ug}}p+1\right)\times\left(\frac{1}{GBW}p+1\right)} \quad (3\text{-}3)$$

$$H_{r\_real}(p) = \frac{1}{b}\times\frac{1}{\frac{p^2}{\omega_o^2}+\frac{p}{Q\times\omega_o}+1} \quad (3\text{-}4)$$

$$\omega_{ug_{error}} = \left[\frac{\omega_{ug}}{(\omega_{ug}+GBW)}\times 100\right]\% \quad (3\text{-}5)$$

$$Q = \frac{A_o}{b^{-1/2}(b-1)\times\left(\frac{R_2C_2}{R_1C_1}\right)^{1/2}+b^{1/2}\times\left(\frac{R_1C_1}{R_2C_2}\right)^{1/2}} \quad (3\text{-}6)$$

Where ω_o, Q, ω_{ug}, GBW, A_o are respectively the resonance pulsation and the quality factor of the resonator, unit gain pulsation of the ideal integrator, the finite GBW and the finite dc gain of the opamp. The derivation of equation (3-3), (3-4), (3-5) and (3-6) is detailed in appendix B.

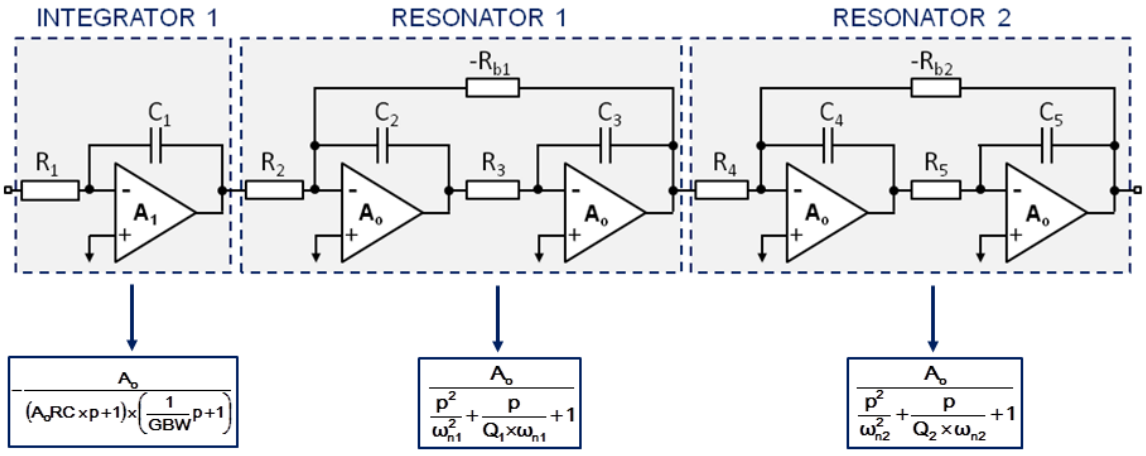


Figure 3-6. Structure of the loop filter with the transfer function associated to each noise shaping stage.

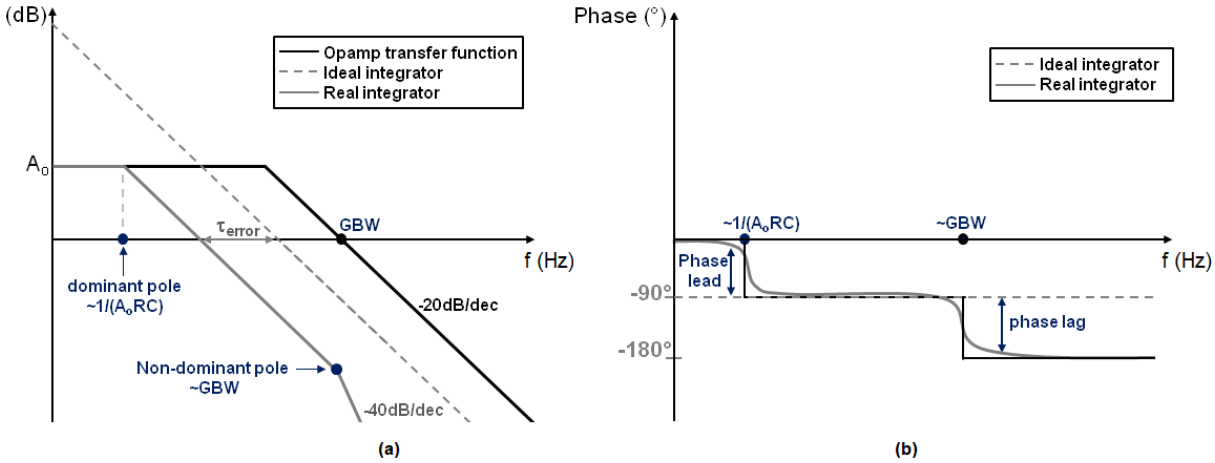


Figure 3-7. (a) Real transfer function of the integrator assuming a one-pole model for the opamp, (b) Asymptotical illustration of the transfer function modulus of the real integrator, (c) Asymptotical illustration of the transfer function phase of the real integrator.

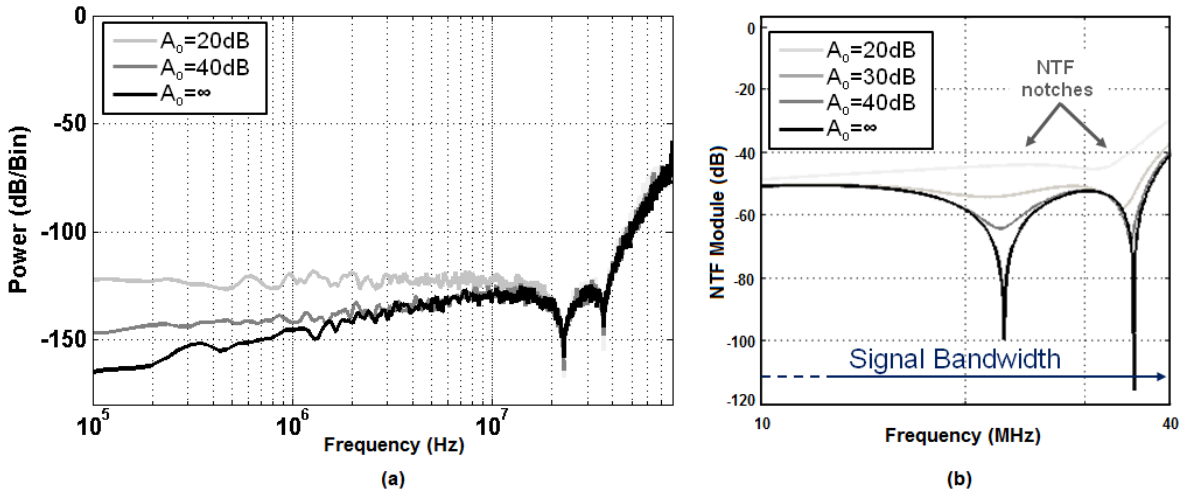


Figure 3-8. (a) influence of the finite gain of opamp 1 on the NTF (all others opamp have an infinite gain), (b) Impact of the finite gain of the opamp inside the pair of resonator on the quality factor of the resonators on the loop filter attenuation within the signal bandwidth (the gain of the first opamp is infinite).

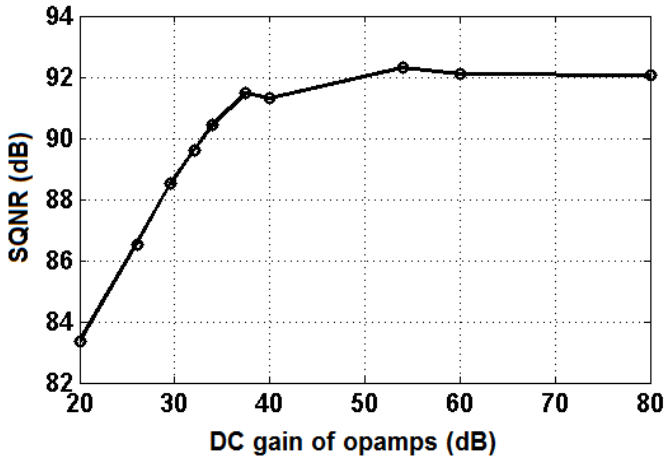


Figure 3-9. Influence of the finite gain of all opamps

3.2.3 Feedforward, feedback and feed-in coefficients

Feedforward coefficients control the position of the zeros of the loop filter. The feedback coefficients implement the loop delay compensation while feed-in coefficients control the output swing of the integrators inside the loop filter. As a consequence, the inaccuracy of these coefficients affects the stability of the modulator, reducing the overall performance.
The value of these coefficients is set either by resistances ratio or capacitances ratio as shown in Figure 3-10(a). While the value obtained by a resistive or capacitive ratio is robust against PVT variations, it is sensitive to component mismatch. As a result, the value of these coefficients will defer from their initial value after chip fabrication. The Matlab model used to study the impact of these errors is shown in Figure 3-10 (b).
The error term of the coefficient is modeled by a Gaussian random variable with zero mean value and a standard deviation whose value is swept from 0.1% to 10%.
The simulation results are shown in Figure 3-11. The worst case SNDR obtained after a Monte-Carlo simulation of 100 runs is plotted for each value of the standard deviation error. The simulations are performed for several values of the input signal.
As expected, the modulator is sensitive to the coefficients accuracy. Furthermore, there is a trade-off between the maximum input signal and the accuracy requirement on the coefficient. For example, if the value of -1dBFS is chosen as the maximum input, the maximum value of the mismatch should not exceed 1%. While this value is feasible in practice, it is at the cost of large components. Furthermore, the non-zero value of the parasitic resistors and capacitors of the wires will add a systematic mismatch that can be compensated but at the cost of more tedious layout.
The histogram of the SNDR corresponding to a standard deviation of 2% and -3dBFS input amplitude is shown in Figure 3-12. The 'histfit' function of Matlab [1] is superimposed. In this case the mean value of the SNDR is 90.1dB and the -3σ shift is 2.46dB.

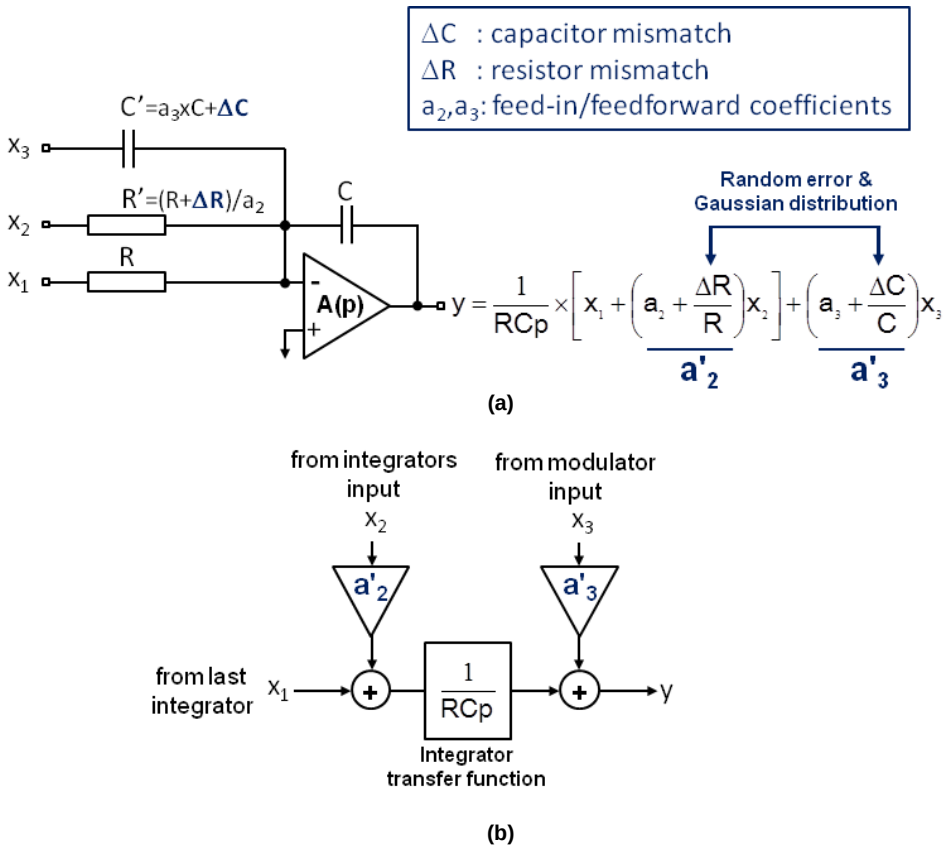


Figure 3-10. (a) Implementation of feedforward and feed-in coefficients and mismatch-induced errors, (b) Model implemented in MATLAB.

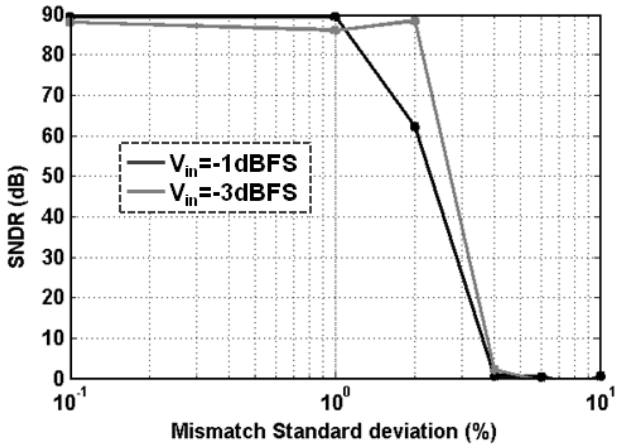


Figure 3-11. Worst-case SNDR obtained after a Monte-Carlo simulation (100 runs) in which the standard deviation of the error in the coefficient of the loop filter after is swept from 0.1% to 10% (f_{in}=10MHz).

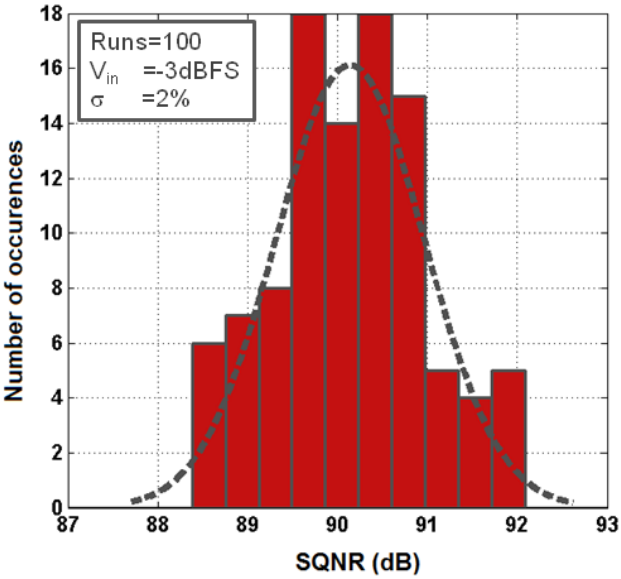


Figure 3-12. Histogram of the SNDR after a Monte-Carlo simulation (100 runs) with a -3dBFS input and 2% mismatch between the coefficients of the modulator.

3.2.4 Harmonic distortion

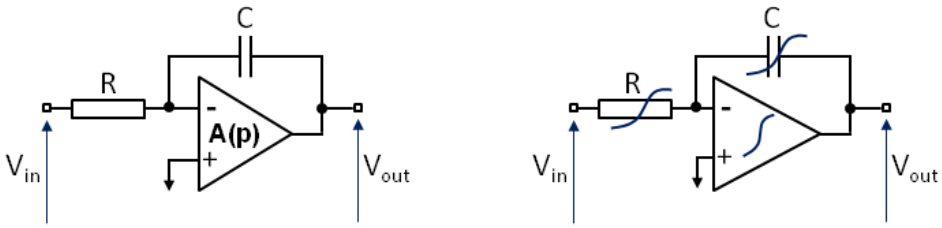


Figure 3-13. (a) Distortion-less front-end, (b) front-end with non-linear components.

While active elements are a well-known source of harmonic distortion in the loop filter, passive components are often omitted when the linearity budget of the modulator is discussed. However, the non-linear behavior of such components could be problematic when a high resolution is required and they must be taken into account especially those of the front-end.

3.2.4.1 Resistor

The non-idealities of the front-end resistor are added directly to the input signal without be shaped by the loop filter. While the thermal noise of the front-end resistor has a major contribution to the ADC noise floor, the dependence of the resistor value in regard of the modulator input voltage is rarely addressed.
A wide variety of standard resistors are available in the process design kit (PDK). Their common point is that they have a low sheet resistance. When high value resistances are needed, highly resistive poly-silicon resistors (HIPO) are available as an option in mixed-signal process but they require one additional mask to be processed which increases the cost of the fabricated chip. In this design, moderate value resistors are needed which does not justify the use of HIPO resistors. Simple poly-silicon (PO) resistors are rather preferred because they are compatible with standard CMOS process [15]. Moreover they have good matching and low dependence to temperature variations. However, it has been shown that the head of such resistor has a strong non-linear I/V characteristic [15] which introduce harmonic distortion. This non-linear behavior is exacerbated for short resistor length because the portion of the non-linear part becomes more dominant over the linear part of the resistor. The voltage dependency is approximated by the second-order polynomial equation (3-7):

$$R = R_o \times (1 + \alpha_{1R} V_R + \alpha_{2R} V_R^2) \tag{3-7}$$

where R_o is the resistance at zero bias, α_{1R} and α_{2R} are respectively the linear and quadratic coefficient of the polynomial approximation and V_R is the voltage applied to the terminals of the resistor. The detailed derivation of the second-order and third order harmonic distortion (HD_2 and HD_3) are detailed in appendix C and are given by equation (3-8) and (3-9) respectively

$$HD_2 \approx \frac{\Delta R}{R_o} \times \frac{\alpha_{1R} A}{8} \tag{3-8}$$

$$HD_3 \approx \frac{\alpha_{2R} A^2}{16} \tag{3-9}$$

where A and ΔR are respectively the amplitude of the signal at the input of the modulator and the mismatch between the two resistors.
The computed HD2 and HD3 from equations (3-8) and (3-9) are plotted in Figure 3-14 and Figure 3-15 respectively, together with the electrical simulation results of the modulator whose front-end resistance value is modeled by equation (3-7).
Regarding the second-order harmonic distortion (HD2), its value is very low for an input voltage range up to 2V even with 3% mismatch and it is not very sensitive to the resistor length (L_R).
The value of the third-order harmonic distortion (HD3) is much more problematic as the quadratic coefficient α_{2R} depends strongly on the value of the resistor length. There exists a trade-off between the maximum input voltage and the resistor length.
It should be noted that equation (3-9) fits with the electrical simulations within less than 1% so it can be used together with equation (3-8) to predict quickly the harmonic distortion due to the voltage-dependency of the resistance.

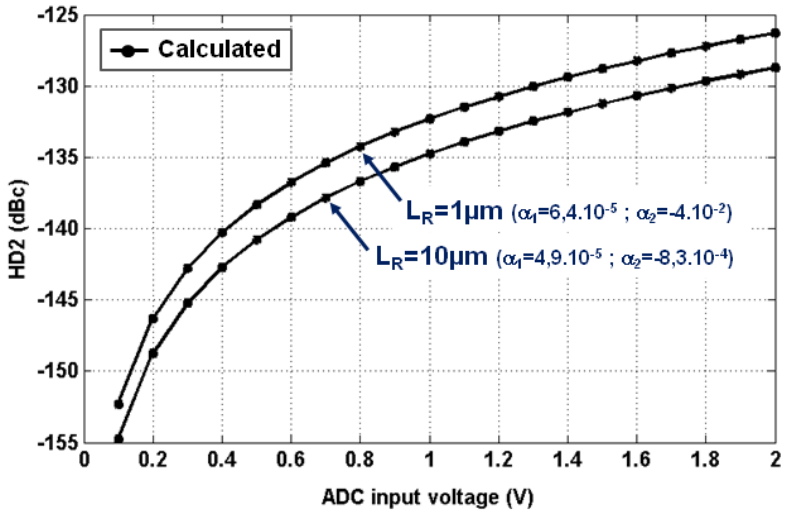


Figure 3-14. Computed second-order harmonic distortion as a function of the ADC input voltage (f_{in}=11.4MHz, V_{REF}=2V) with 3% mismatch between input resistors ($\Delta R/R_o$=3%) and using two length value of 1µm and 10µm (W_R/L_R ratio is constant).

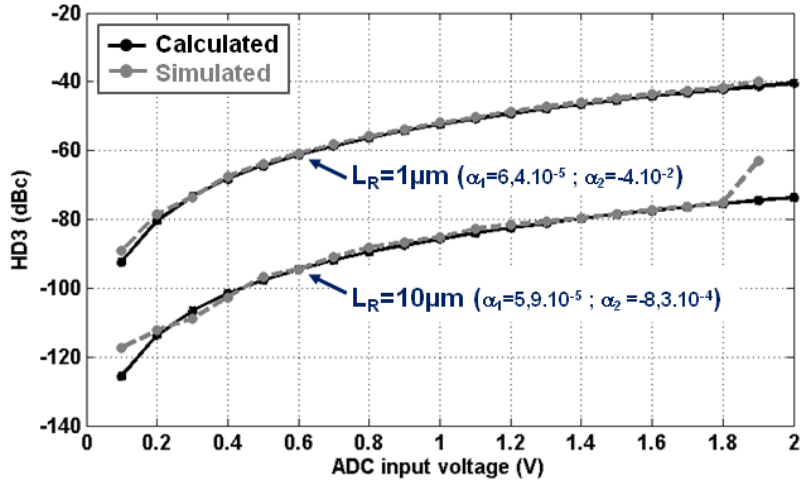


Figure 3-15. Simulation and computation from analytical equation (3-9) of the third-order harmonic distortion (HD3) at the modulator output as a function of the ADC input voltage (f_{in}=12.1MHz, V_{REF}=2V) for two resistors length values while keeping the W_R/L_R ratio constant.

3.2.4.2 Capacitor

The integrating capacitors occupy a large portion of the integrator area, especially those of the front-end (~30% in this design). To save silicon area, Metal-Insulator-Metal (MIM) capacitors are used because they have an excellent density compared to Metal-Oxide-Metal (MOM) capacitors and a lower voltage dependency compared to MOS capacitors. Furthermore, MIM capacitors have excellent matching, highly conductive electrodes and low parasitic capacitance.
However, the higher capacitance density of MIM capacitors cannot be simply achieved by further thinning the conventional silicon dioxide (SiO2) or silicon nitride (Si3N4) films because of leakage and reliability issues. Therefore, the only viable solution is adopting high-k materials as dielectrics of MIM capacitors [16]. However, unlike SiO_2, which is an almost ideal insulator, high-k dielectrics usually contain plenty of bulk traps and interface states, especially after electrical stress. These non-ideal defects cause instability of devices during operation, which leads to the distortion of analog functions performed by the MIM capacitor and further limits the performance of RF/analog circuits [16].
The expression of the capacitor value as a function of the voltage is given by the second-order polynomial equation (3-10):

$$C = C_o \times (1 + \alpha_{1C} V_C + \alpha_{2C} V_c^2) \quad (3\text{-}10)$$

C_o is the capacitance at zero bias, α_{1c} and α_{2c} are respectively the linear and quadratic coefficient of the polynomial approximation and V_c is the voltage applied between the electrodes of the capacitor.

In Figure 3-16, the linearity behavior of the capacitor is simulated as a function of the voltage at the input of the modulator. We must note that in this simulation the voltage reference of the quantizer is changed from 0.8V to 2V in order to accommodate to a wider input voltage range. Here we are interested in HD3 only since, even with strong mismatch between the integrating capacitors, the value of the linear coefficient α_{1C} is so low that the HD2 is negligible even for high input voltage swing across the capacitor. Regarding the HD3, the degradation is more severe for amplitude near the FS. The linearity is limited to -86dBc (14-bit) by the distortion of the front-end capacitor if a 2V voltage reference is chosen for the quantizer.

Figure 3-17 shows the third-order harmonic as a function of the input signal frequency with amplitude equal to the MSA computed in Figure 3-16 (1.7V). As the harmonics occurs on the capacitor they are filtered and hence the HD3 improves with frequency.
In Figure 3-18, a two-tone simulation shows that the third-order inter-modulation product is better than 16-bit even when the sum of the input tones is equal to the ADC FS.
With, a reference voltage of 0.8V, which is the choice in this design, the harmonic distortion is better than 16-bit within the full signal bandwidth of the modulator.
Even if they have very good linearity performance, it should be noted that MIM capacitors require additional masks to be processed which increases the fabrication cost. This additional cost must be balanced with the gain in silicon area provided by the high density of these capacitors.

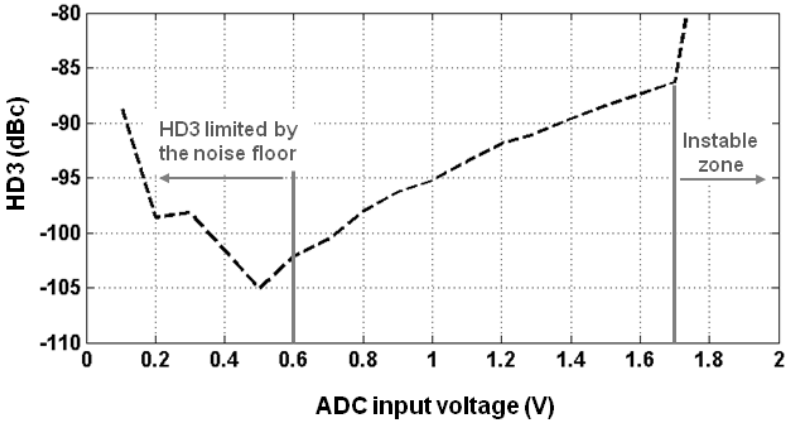


Figure 3-16. Simulated third-order harmonic distortion (HD3) at the modulator output as a function of the input voltage (V_{REF}=2V, f_{in}=1.25MHz) and taking into account the non-linearity of the integrating capacitor of the first integrator.

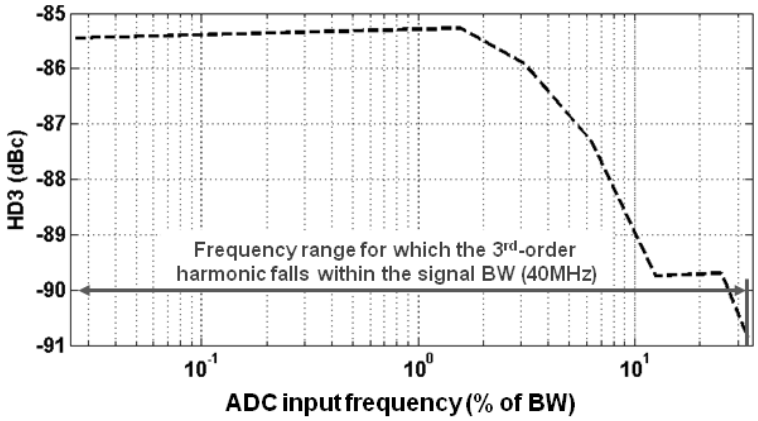


Figure 3-17. Simulated third-order harmonic distortion (HD3) at the modulator output as a function of the input frequency (V_{REF}=2V, V_{in}=1.7V) taking into account the non-linearity of the integrating capacitor of the first integrator.

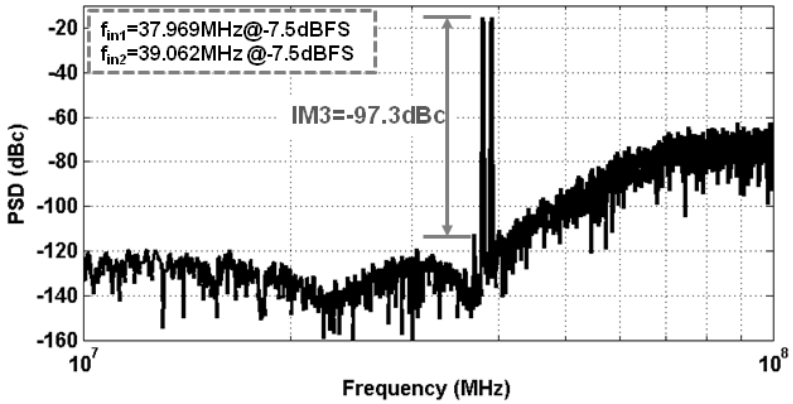


Figure 3-18. Two-tone simulation to evaluate the third-order inter-modulation (IM3) at the modulator output (V_{REF}=2V) taking into account the non-linearity of the integrating capacitor of the first integrator.

3.2.4.3 opamp

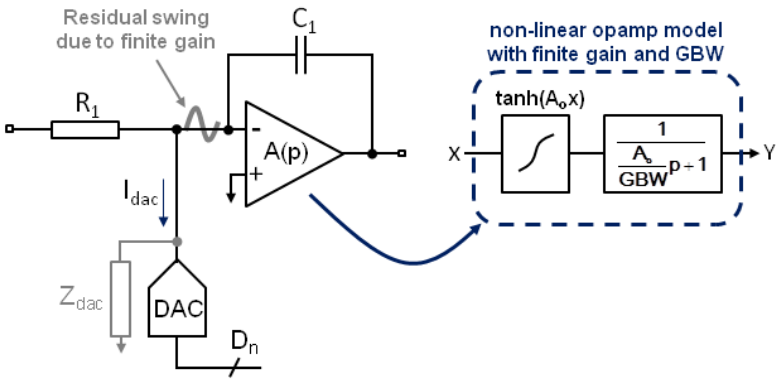


Figure 3-19. Illustration of the main distortion mechanisms in the modulator front-end.

The finite gain and GBW of the opamp induce a voltage swing at the virtual ground of the RC-integrator which is a double source of distortion in the modulator front end. As shown in Figure 3-19, this residual voltage that is signal-dependent, modulates the non-linear input stage of the main opamp and the finite output impedance of the main DAC (noted Z_{dac} in Figure 3-19), which creates harmonic distortion. The distortion due to the finite impedance of the DAC is studied in the paragraph 3.3.1.

The non-linear behavior of the opamp is modeled with a hyperbolic tangent function [17]. The impact of the finite dc gain and GBW of the opamp is shown in Figure 3-20, with a linear opamp model and a non-linear opamp model. These simulations are performed while the gain errors of the integrators, predicted by equation (3-5), are compensated to ensure that the performance degradation is due to the distortion only.
When a linear model is assumed, the finite gain and GBW affect the quantization noise only. If the non-linear behavior of the opamp is taken into account, harmonics of the signal are added to the quantization noise floor which decreases the SNDR. It should be noted that the degradation is more severe when the finite GBW is taken into account. This is quite predictable, because in this case, the amplitude of the voltage swing becomes frequency-dependent.

Another remark concerns the value of the HD3 plotted in Figure 3-21. The linearity of the modulator must be analyzed carefully, especially when the value of the GBW is set equal to the sampling frequency (f_s). This choice is mostly adopted because it allows an aggressive scaling of the loop filter power consumption. Furthermore, the noise degradation which results of this strategy may be completely negligible if the gain value of the integrators is tuned, according to equation (3-5).
However, Figure 3-21 shows that taking into account the HD3 only, leads to a linearity performance of nearly 14-bit when the GBW is chosen equal to the sampling frequency. In practice, the mismatch-induced even order distortion and the harmonics introduced by the current mismatch in the main DAC would result in a linearity performance well below 14-bit.

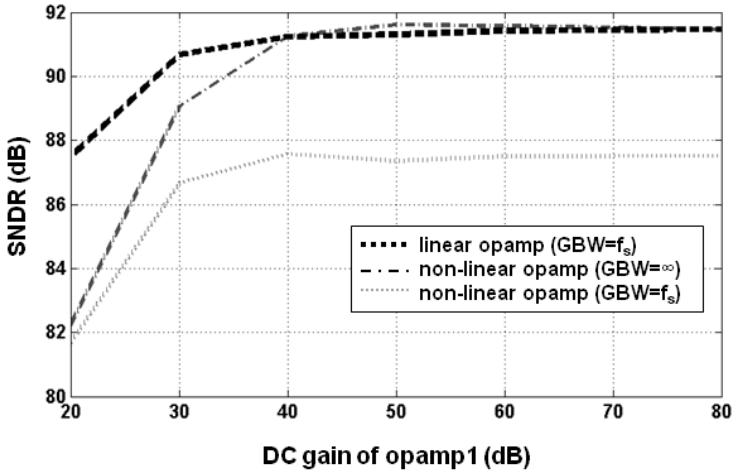


Figure 3-20. Simulated SNDR at the modulator output as a function of the finite gain of the main opamp (opamp1) with a linear and non-linear model (f_{in}=10MHz & V_{in}=-1.8dBFS).

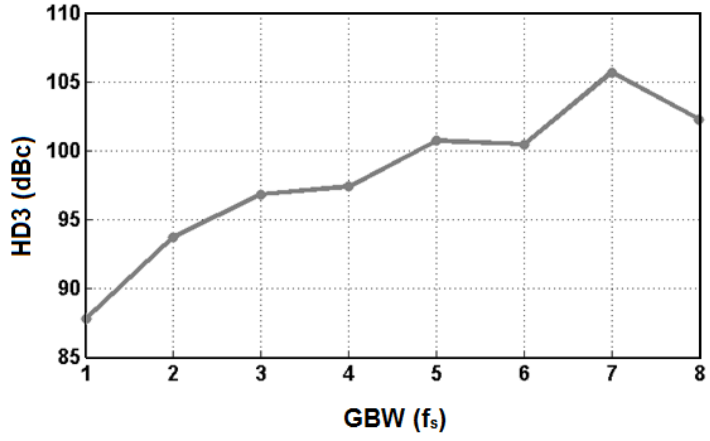


Figure 3-21. Simulated HD3 at the modulator output as a function of the finite GBW of the main opamp (opamp1) with a linear and non-linear model and 40dB of dc gain (f_{in}=10MHz & V_{in}=-1.8dBFS).

3.3 Current-steering DACs

The output of the main feedback DAC is directly subtracted from the modulator input so its imperfections are not shaped by the loop filter. As a consequence, the non-idealities of this block must be carefully analyzed. Regarding the minor DACs, their imperfections are noise shaped by the loop filter which reduces the design requirements on these blocks. However, at low OSR, the noise and distortion of the minor DACs are weakly attenuated by the loop filter which means that they must be taken into consideration when high performance is required.

3.3.1 Finite output impedance

Using an RC-opamp as the first integrator makes the interfacing of the DAC more efficient because its output terminals are connected to the virtual ground of the opamp which is ideally a zero-impedance node. But as shown in Figure 3-19, a residual swing is present at the virtual ground due to the finite dc gain of the opamp, creating a modulating current that is proportional to the amplitude of the swing and inversely proportional to the impedance value. Hence to reduce the non-linear effect of the finite impedance, whether the gain of the opamp must be increased (to reduce the voltage swing), or the value of the output impedance must be increased. The effect of the finite resistance on the performance of the whole modulator is shown in Figure 3-21 assuming a finite DC gain of 40dB in the first opamp. As expected, beyond a certain impedance value, the SNDR degradation is mainly due to the presence of harmonic distortion.

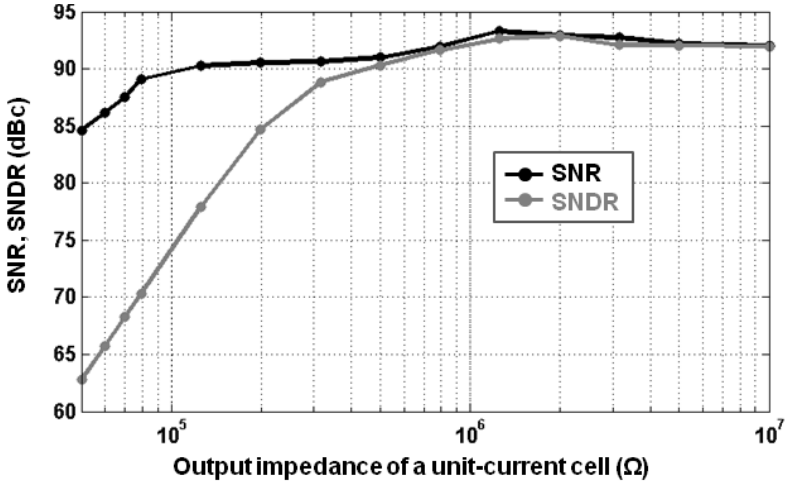


Figure 3-22. Influence of finite output impedance of the unit-current cell in the main DAC assuming a finite gain of 40dB in the main opamp.

3.3.2 Unit-current mismatch

The current mismatch between the unit-current cells of the main DAC is a severe source of degradation of noise and linearity in the modulator as shown in Figure 3-23 where only 1% of current-mismatch is assumed. Furthermore, as a low OSR value is chosen, the mismatch-induced noise and distortion of the minor feedback DAC may also be a problem if high resolution is targeted.

The impact of the current mismatch in both DACs is analyzed through Monte-Carlo simulations where the standard deviation of the mismatch is swept from 0.01% to 1%. The worst case SNDR value (-3σ shift) is plotted in Figure 3-23(a) and Figure 3-23(b) for the main DAC and for the minor DAC respectively. Simulations were performed with and without DWA which has been chosen as the correction technique to reduce the impact of mismatch.

Compared with the case where no correction is employed (DWA OFF), the DWA relaxes the mismatch standard deviation value by a factor of 8 and 3 for the main DAC and the minor DAC respectively if negligible degradation of the SNDR is desired. As this value is inversely proportional to the squared root of components area, it results in a reduction area of 64 and 9 for the main DAC and the minor DAC respectively.

The mismatch between the switches of the current cells of the DACs results in a current pulse with unequal rise time and fall time. As a result, the energy of the pulse is code-dependent which creates harmonic distortion. This is known as inter-symbol interference and it will be detailed in Chapter 5.

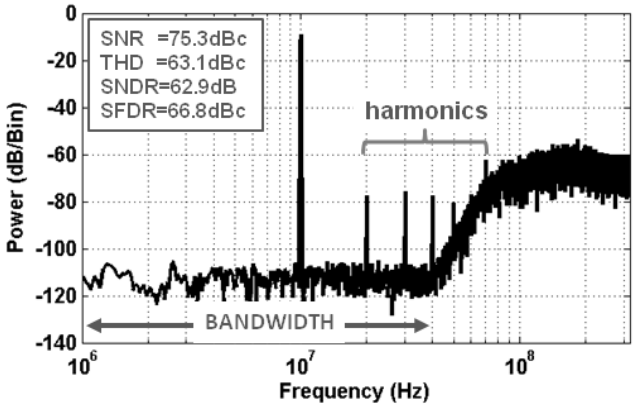


Figure 3-23. PSD of the modulator output with 1% current mismatch in the main DAC (f_{in}=10MHz and V_{in}=-1.1dBFS).

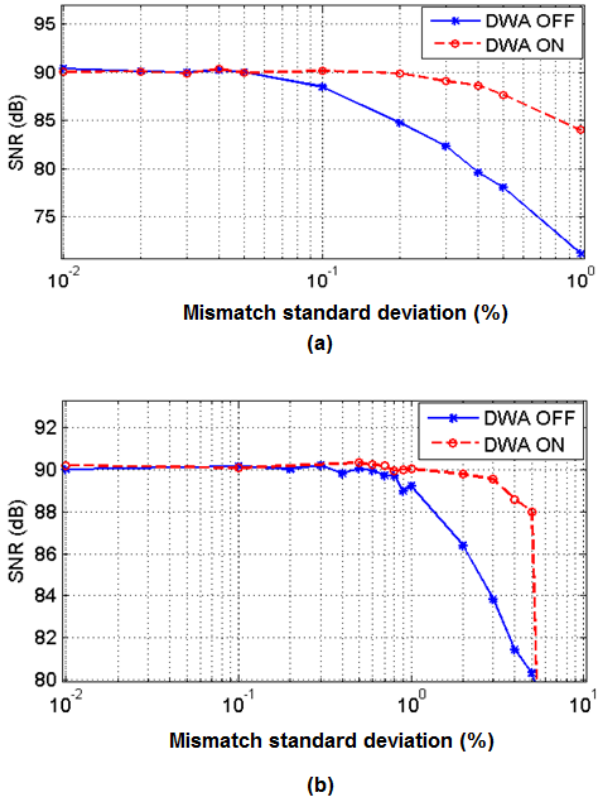


Figure 3-24. Monte-Carlo simulation (200 runs) of the SNDR as a function of the current-mismatch with and without DWA (V_{in}=-1.1dBFS@f_{in}=10MHz) in, (a) the main DAC, (b) the minor DACs.

3.3.3 Clock jitter

Due to components noise, the period of an oscillator fluctuates randomly over time. As shown in Figure 3-25, this phenomenon is referred as jitter in the time domain while it is called phase noise in the frequency domain.
The impact of clock jitter on the performance of a continuous-time ΔΣ modulator was extensively studied in the literature [20][23-26] for a wide variety of DAC pulse shape. Assuming wideband uncorrelated jitter, the signal to noise ratio due to the clock jitter only (SNR_j) of a ΔΣ modulator with an NRZ DAC used in the front-end, is given by equation (3-11) [14].

$$SNR_j = \frac{OSR \times V_{in}^2}{2\sigma_{\delta y}^2 \times \left(\frac{\sigma_j}{T_s}\right)^2} \tag{3-11}$$

where $\sigma_{\delta y}^2$ is the variance of the first-order difference of the DAC code [25]. As $\sigma_{\delta y}^2$ depends on the topology of the loop filter, its value is determined by simulation and then the SNR_j is computed using the equation (3-11).
The impact of clock jitter is shown in Figure 3-26. Beyond a clock jitter of 400fs rms, the SNR of the whole ADC is mostly dominated by the jitter-induced noise.

Even if the clock jitter is a well-known source of noise degradation in any data converters, the noise budget attributed to the jitter is rarely discussed in the literature dedicated to the design of ΔΣ modulators. A few wideband realizations have detailed the quality of the clock needed for optimal noise performance [12][17-20]. Moreover, the power penalty which results of this choice is rarely underlined. The link between the power consumption and the phase noise of an oscillator is given by the Lesson's formula [21] and written in equation (3-12), while equation (3-13) [22] shows how to convert phase noise into time jitter (assuming broadband jitter).

$$L(\Delta f) = 10 \times \log_{10}\left[\frac{2kTNF}{P_c}\left(\frac{f_s}{2Q\Delta f}\right)\right] \tag{3-12}$$

$$\sigma_j \approx \frac{\sqrt{2 \times 10^{A/10}}}{2\pi f_s} \tag{3-13}$$

L(Δf) : phase noise in dBc/Hz at and offset Δf from the carrier frequency
k : Boltzmann constant
T : absolute temperature
NF : noise factor of the oscillator
Pc : power consumption of the oscillator
Q : quality factor of the resonating circuit
f_s : carrier frequency
σ_j : rms jitter
A : phase noise in dBc

Equation (3-12) shows the trade-off between the power consumption and the clock jitter. As for data converters, many FoMs exist to express the power efficiency of an oscillator. A common one is expressed in equation (3-14).

$$FoM_{[dBc/Hz]} = -L_{[dBc/Hz]} + 20\log_{10}\left(\frac{f_s}{\Delta f}\right) - 10\log_{10}\left(P_{ower[mW]}\right) \tag{3-14}$$

In Figure 3-27 we have reported the FoM of different oscillators. This plot may be useful to identify which architecture is best suited to reach a phase noise performance given a certain amount of power.

In [12], the 300fs-jitter LC-PLL was used to clock the CT ΔΣ modulator showed at a frequency of 640MHz while consuming 12mW. This gives a qualitative idea of the power requirement needed for our target value of 450fs rms.

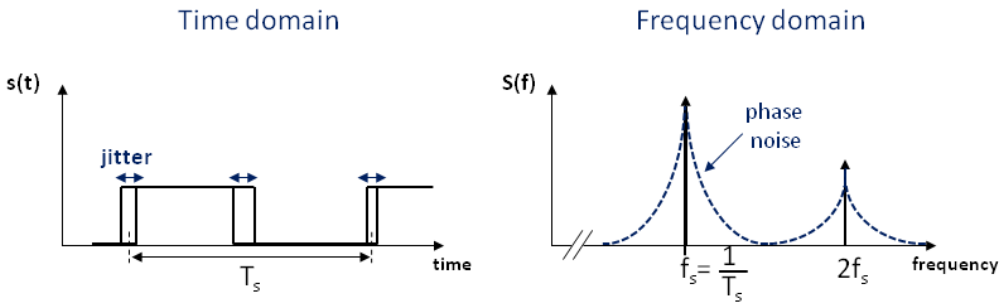


Figure 3-25. Representation of the clock period fluctuation in (a) the time domain (jitter), (b) the frequency domain (phase noise).

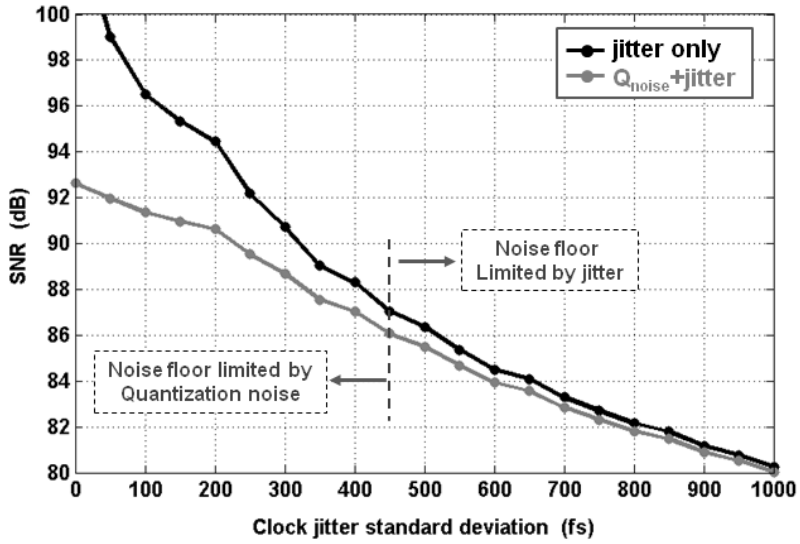


Figure 3-26. Figure of merit of different oscillator topologies (2000-2010).

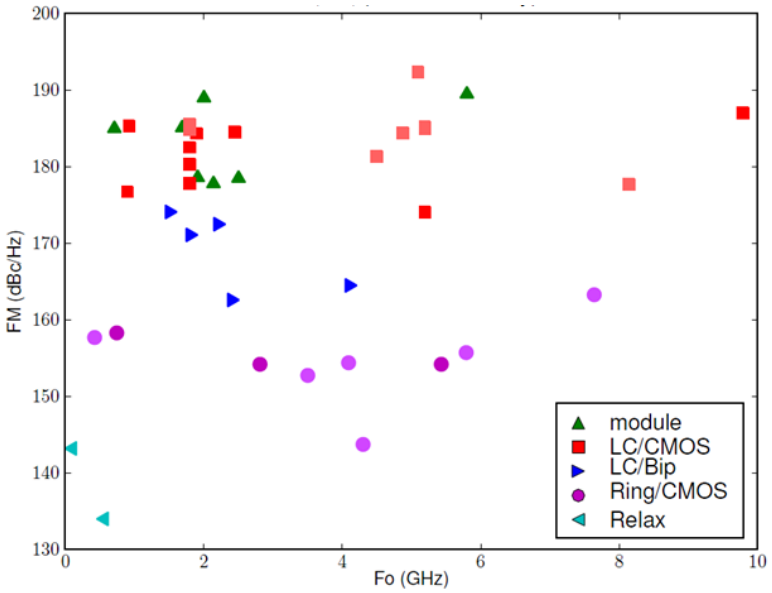


Figure 3-27. Simulated SNR at the modulator output as a function of the clock jitter standard deviation.

3.4 Quantizer

As the quantizer is located at the back-end of the modulator, its non-idealities are suppressed by the high gain of the preceding integrators, which generally results in very relaxed requirement on this block. However, in high-accuracy multi-bit converters, this is no longer true [27].

3.4.1 Metastability

The simplified schematic of the modulator back-end is shown in Figure 3-28(a). As the loop delay is set to half the clock period, the quantizer has a shorter amount of time to deliver the right digital code to the DWA circuit and the decimation filter. The used of the DWA put a challenging requirement on the timing of the comparators. The schematic of one comparator slice is shown in Figure 3-28(b).
The propagation delay of a comparator depends on the amplitude of the voltage delivered by the loop filter and the time constant of the decisional element (latch) as expressed by equation (3-15) [28].

$$t_p = \tau_L \times \ln\left(\frac{V_{OH}-V_{OL}}{A_{preamp}\times 2\Delta V_{in}}\right) \qquad (3\text{-}15)$$

Where A_{preamp}, τ_L, Δv_{in}, V_{OH}, V_{OL} are respectively the gain of the preamplifier, the regenerative time constant of the latch, the input amplitude of the comparator, the voltage corresponding to a logic value '1' and the voltage corresponding to a logic value '0'. As shown in equation 3-15 and illustrated in Figure 3-28(c), the propagation time of the latch depends on its input amplitude ΔV_{in}.
Sometimes the input voltage ΔV_{in} is so weak that the comparator cannot take the good decision during the available time slot. In this case, the comparator is in a metastable state.
In this work we have modeled the metastable comparator as a block that computes the propagation time (t_p) given by equation (3-15). We distinguish two cases, depending on the value of t_p.

- If t_p is below a threshold value δt ($\delta t < t_s/2$) then the output is either V_{OH} or V_{OL} depending on the sign of the input voltage ΔV_{in}.
- If t_p is higher than δt, the latch is in a metastable state and a decision must be made choosing a criteria.

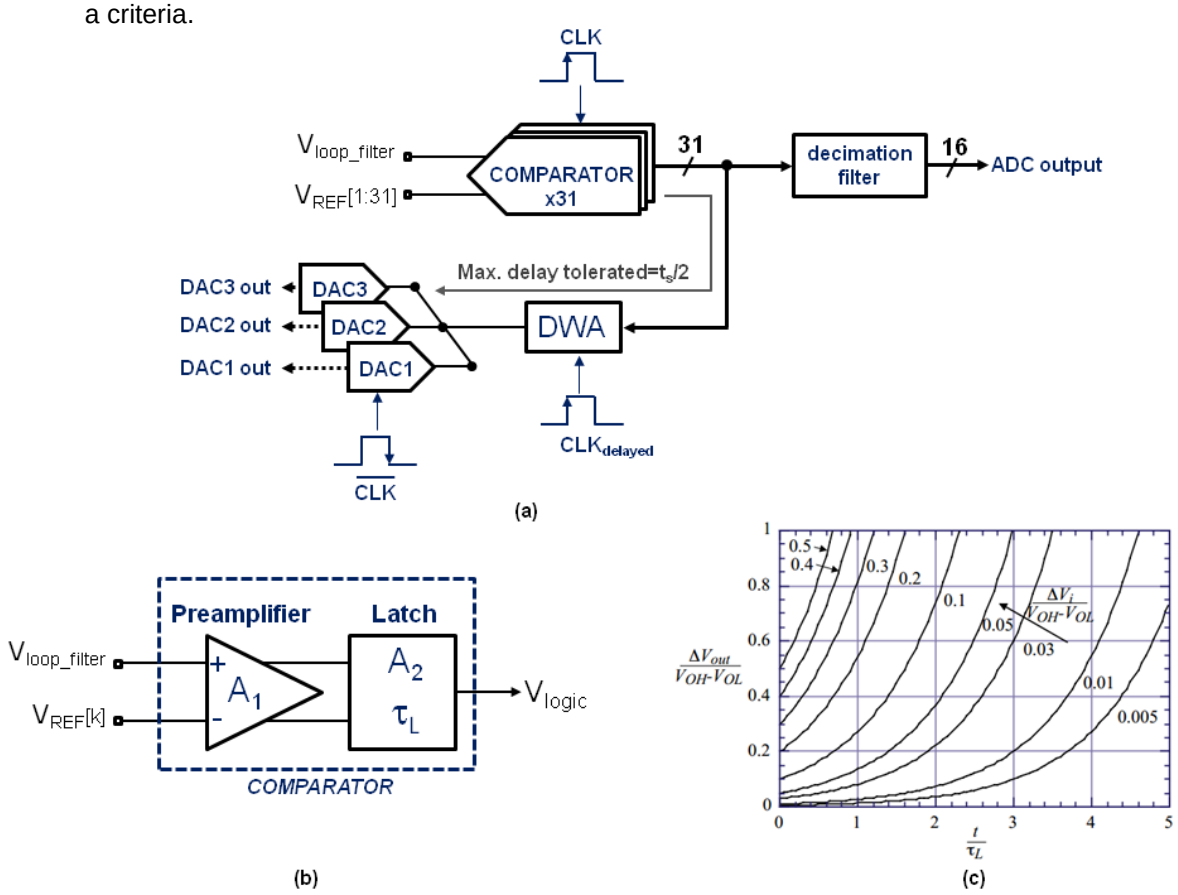


Figure 3-28. (a) Architecture of the modulator back-end an timing (b) Architecture of the comparator, (c) impact of input amplitude on the time response of the latch [28].

In the second case, many scenarios are possible. In this work the comparator was designed such as a decision is always taken either by the signal or by the component noise.
It should be noted that a specific coding of the quantizer output can be used to correct the bubble errors due to metastability [29] but this technique adds latency which reduces the available time for the DWA. The simulated SNDR as a function of the time constant of the latch is shown in Figure 3-29. Designing the comparator with a time constant lower than 30% of the clock period preserves the dynamic performance of the modulator. In certain applications, the Bit Error Rate (BER) may be an important metric. For an ADC, the BER is defined as the ratio of the errors observed at the ADC output during a defined time interval over the total number of samples. An error occurs when the difference between two successive samples is higher than 1LSB [30].
Figure 3-30 shows the BER variation as a function of the time constant of the latch. As predicted by equation 3-15, lowering the time constant of the latch reduces the propagation time of the comparator which reduces the probability of metastability. It is interesting to note that, depending on the targeted application, the BER requirement may result in a different requirement on the time constant of the latch than the value predicted by the SNDR.

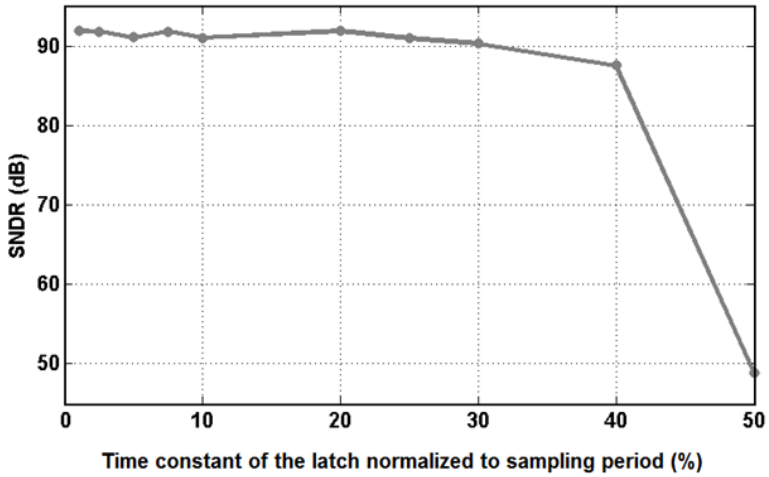


Figure 3-29. SNDR at the modulator output for different value of the time constant of the latch (V_{in}=-1.1dBFS and f_{in}=10MHz, A_{preamp}=1).

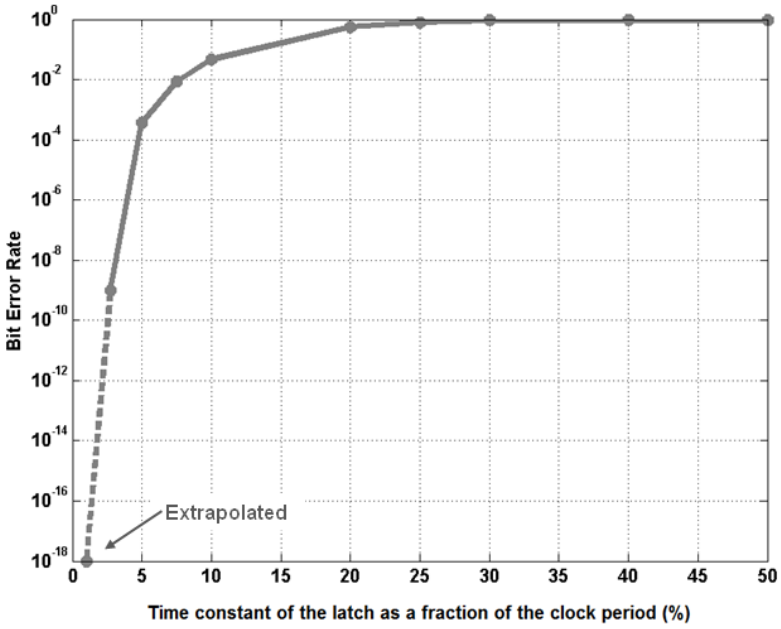


Figure 3-30. Simulated Bit Error rate at the modulator output for different value of the time constant of the latch (V_{in}=-1.1dBFS and f_{in}=10MHz, A_{preamp}=1).

3.4.2 Hysteresis

As shown in Figure 3-31(a), hysteresis is a memory effect, i.e., a logic decision at a given time is affected by the decision made on the past samples. It may come, for example, of an imperfect resetting of the decision element [31]. The degradation of the performance due to hysteresis can be modeled by an additive white noise source at the input of the comparator [27][32]. The hysteresis affects only the noise performance of the modulator. As shown in Figure 3-31(b), the hysteresis value must be kept below 0.25% of the voltage reference (2mV) to leave the SNDR unchanged, which is of the same order of magnitude found in [27].

Another source of imperfection that can be modeled as an additive white noise source is the jitter of the clock that drives the comparators. However, this noise source is attenuated by the loop filter in the same manner as the hysteresis and the quantization noise which makes the quantizer robust to clock jitter.

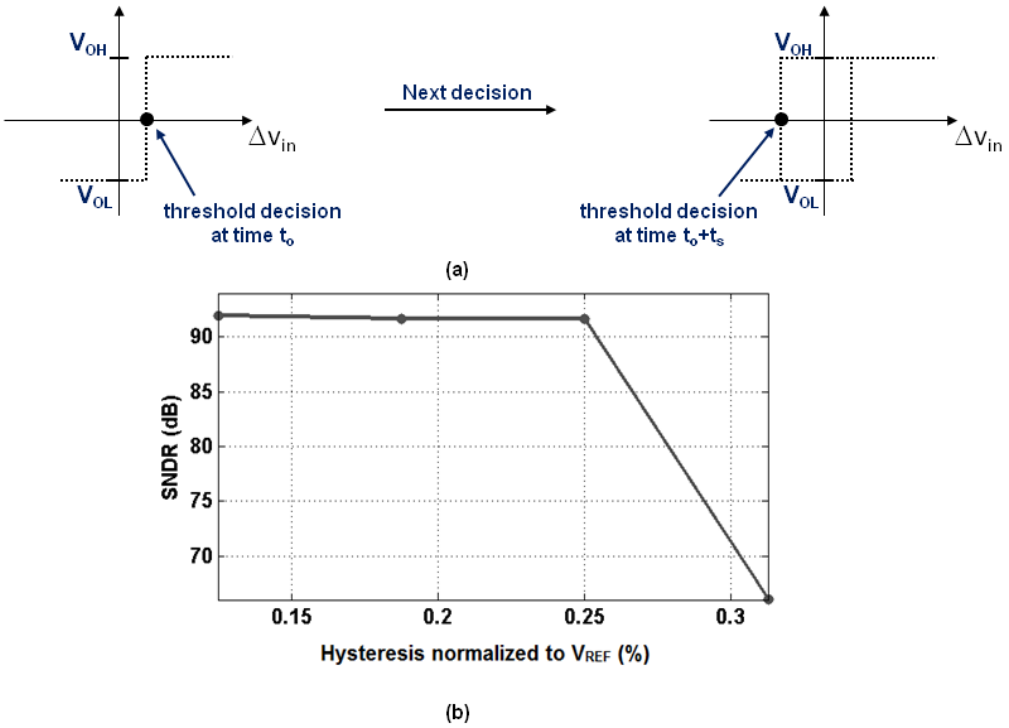


Figure 3-31. (a) Illustration of the hysteresis effect, (b) simulation of the impact of comparator hysteresis (V_{in}=-1.1dBFS@f_{in}=10MHz).

3.4.3 Offset

The random offset of the comparators must be considered carefully, especially when high linearity is required. This is confirmed in Figure 3-32 where the PSD of the modulator output is simulated with a random offset added to the input of each comparator. A standard deviation of only 0.16LSB degrades severely the THD of the $\Delta\Sigma$ modulator. Harmonics are clearly visible while the noise floor is unchanged.
The impact of the random offset is analyzed through Monte-Carlo simulations where the standard deviation of the error is swept from 0.1% to 10% of the LSB. The worst case SNR, SNDR and THD values (-3σ shift) are plotted in Figure 3-33.
While the -3σ value of the SNR remains constant below a σ value of 0.1 LSB the THD starts to degrade more than one decade before.

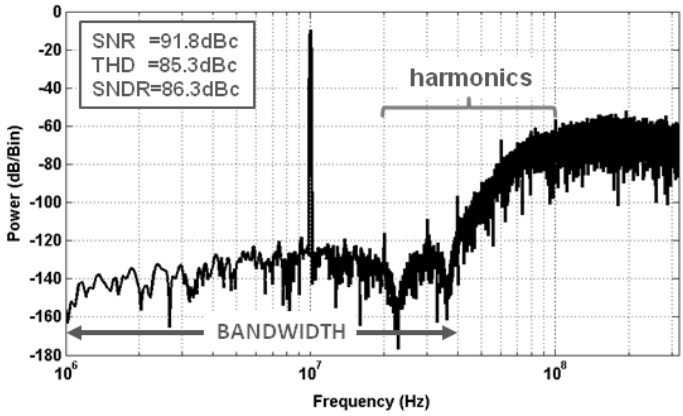


Figure 3-32. PSD of the modulator output with σ_{offset}=0.16LSB (f_{in}=10MHz and V_{in}=-1.8dBFS).

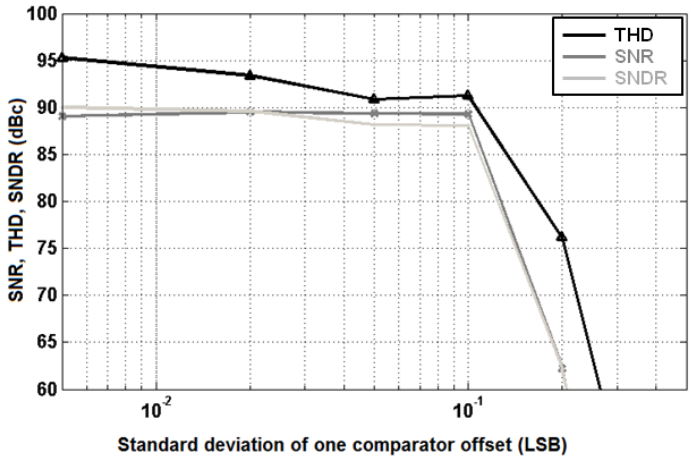


Figure 3-33. Monte-Carlo simulation (50 runs) of the effect of the random offset of the 31 comparators inside the flash quantizer (V_{in}=-1.1dBFS@f_{in}=10MHz).

3.5 Building blocks specifications

The main specifications of the modulator sub-blocks are summarized in Table 3-1. The noise budget of the modulator was done such as the thermal noise is the dominant noise source. This choice put a requirement of 450fs rms on the clock jitter which can be achieved with a low-power frequency synthesizer, that would be integrated on-chip or not.
It should be kept in mind that even if each non-ideality source was explored individually, a combination of several non-idealities may impact the overall performance more severely and would result in a more stringent requirement on each sub-block of the ΔΣ modulator.
Thus, a behavioral simulation that takes into account all the non-idealities together is shown in Figure 3-34.
At this point, we should have a good idea of the circuit-level architecture used to achieve the targeted specifications of Table 3-1. If the specifications are tight, then the errors budget should be modified accordingly.

Table 3-1. Building blocks specifications

PARAMETERS	VALUE	UNIT
Loop filter		
Coefficients mismatch (σ)	1	%
Unit gain frequency accuracy	±2	%
Opamp1 GBW	6	f_s
Opamp1 dc gain	≥40	dB
Main DAC		
Current mismatch	0.2	%
Clock jitter	450	fs
Output impedance	>1	MΩ
Quantizer		
Offset (σ)	2	mV
Hysteresis	>2	mV
Time constant of the latch	1%	T_s
Modulator Noise budget		
Quantization	89	dBc
Thermal	77.4	dBc
Jitter	86.5	dBc
Decimation filter	91.8	dBc
SNDR total (2dB margin)	**76.5**	**dBc**

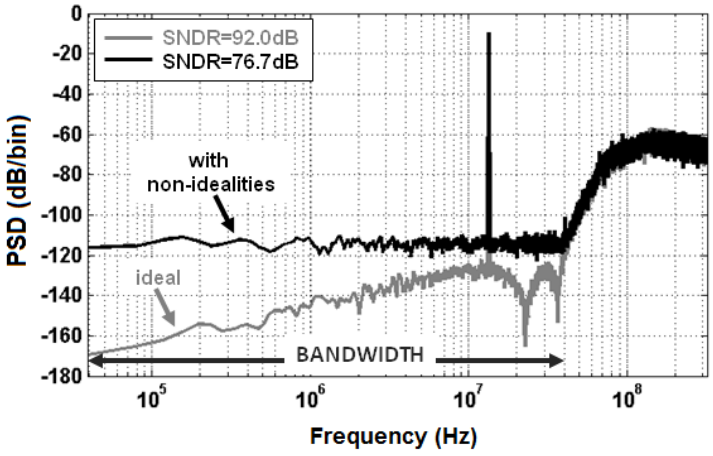


Figure 3-34. PSD of the ΔΣ modulator output with and without non-idealities (V_{in}=-1.8dBFS and f_{in}=13.32MHz).

3.6 Summary

In this chapter we have identified the main non-idealities that may affect the performance of our CT ΔΣ modulator. For each sub-block of the modulator, a behavioral model was built to quantify quickly the limit value of its non-idealities which allowed deriving a set of circuit-level specifications to meet the targeted performance of Table 2-3.
The circuit-level specifications are used to design each sub-block of the modulator in a 65nm CMOS process which is the subject of the next chapter.
Even if this manuscript is written in a linear way, a strong correlation exists between the system-level design and the circuit-level design, which requires in practice, a lot of back and forth between these two design steps.

3.7 References

[1] www.mathworks.fr/

[2] http://www.mathworks.com/matlabcentral/fileexchange/19-delta-sigma-toolbox

[3] http://www.analog.com/

[4] Kathleen Philips and Arthur H.M van Roermund, "ΣΔ A/D conversion for signal conditioning", Springer, 2006 edition.

[5] K. Philips, P.A.C. M. Nuijten, R. Roovers, F. Munoz, M. Tejero, A. Torralba, "A 2mW 89dB DR Continuous-Time ΔΣ ADC with Increased Immunity to Wide-Band Interferers," IEEE ISSCC Dig. Tech. Papers, February 2004.

[6] Yann Le Guillou, Hussein Fakhoury, "Elliptic filtering in continuous-time sigma-delta modulator", Electronics Letters, Volume 41, Issue 4, February 2005.

[7] Mohammad Ranjbar, Omid Oliaei and Robert W. Jackson, "A Robust STF 6mW CT ΔΣ Modulator with 76dB Dynamic Range and 5MHz Bandwidth," IEEE CICC Dig. Tech. Papers, Sept. 2010.

[8] Chi-Lun Lo, Chen-Yen Ho, Hung-Chieh Tsai, Yu-Hsin Lin, "A 75.1dB SNDR 840MS/s CT ΔΣ Modulator with 30MHz Bandwidth and 46.4fJ/conv FOM in 55nm CMOS," IEEE VLSI Dig. Tech. Papers, June 2013.

[9] S. R. Norsworthy, R. Schreier, G. Temes, "Delta-Sigma Data Converters, Theory, Design and Simulation," IEEE Press, 1996.

[10] Bo Xia, Shouli Yan, and Edgar Sánchez-Sinencio, "An RC Time Constant Auto-Tuning Structure for High Linearity Continuous-Time SD Modulators and Active Filters », IEEE Trans. on Circuits and Systems-I: Regular Papers, VOL. 51, NO. 11, November 2004.

[11] Shanthi Pavan and Nagendra Krishnapura, "Automatic Tuning of Time Constants in Continuous-Time Delta–Sigma Modulators," IEEE Trans. on Circuits and Systems-II: Express Briefs, Vol. 54, NO. 4, April 2007.

[12] G. Mitteregger, et al., "A 14 b 20 mW 640 MHz CMOS CT ΔΣ ADC with 20MHz signal bandwidth and 12b ENOB," ISSCC Dig. Tech. Papers, pp. 62–63, February 2006.

[13] Khiem Nguyen, Robert Adams, Karl Sweetland, and Huaijin Chen, "A 106-dB SNR Hybrid Oversampling Analog-to-Digital Converter for Digital Audio," IEEE J. of Solid-State Circuits VOL. 40, NO. 12, December 2005.

[14] Hajime Shibata et. al., "A DC-to-1GHz Tunable RF ΔΣ ADC Achieving DR = 74dB and BW = 150MHz at f_0 = 450MHz Using 550mW," IEEE J. of Solid-State Circuits, vol.32, no. 12, pp. 1896–1906, December 2012.

[15] Nicky Chau-Chun Lu, Levy Gerzberg, Chih-Yuan Lu, James D. Meindl, "Modeling and Optimization of Monolithic Polycrystalline Silicon Resistors," IEEE Trans. on Electron Devices, Vol. ED-28, NO. I, July 1981.

[16] Shu-Hua Wu, Chih-Kang Deng, Tuo-Hung Hou, and Bi-Shiou Chiou, "Stability of La2O3 Metal-Insulator-Metal Capacitors under Constant Voltage Stress", Japanese Journal of Applied Physics 49, April 2010.

[17] Matthew Park, "A Fourth-Order Continuous-Time ΔΣ ADC with VCO based Integrator and Quantizer," Ph.D. dissertation, Massachusetts Institute of Technoly, Cambridge, MA, February 2009.

[18] Muhammed Bolatkale et al., “A 4GHz CT ΔΣ ADC with 70dB DR and –74dBFS THD in 125MHz BW,” ISSCC Dig. Tech. Papers, pp. 470-472, February 2011.

[19] Pradeep Shettigar, and Shanthi Pavan, “Design Techniques for Wideband Single-Bit Continuous-Time Modulators With FIR Feedback DACs,” IEEE J. of Solid-State Circuits, VOL. 47, NO. 12, DECEMBER 2012.

[20] R.H.M. van Veldhoven, “A Triple-Mode Continuous-Time ΣΔ Modulator with Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver”, IEEE J. Solid-State Circ., vol. 38, 2069–2076, December 2003.

[21] Leeson, D. B., "A Simple Model of Feedback Oscillator Noise Spectrum", Proceedings of the IEEE, VOL.52, N°2, 329–330, February 1966.

[22] Walt Kester, “Converting Oscillator Phase Noise to Time Jitter”, Analog Devices tutorial MT-008.

[23] S. Harris, “The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters and on Oversampling Delta-Sigma ADCs”, J. Audio Eng. Soc., vol. 38, July/August 1990.

[24] D.J. van der Zwan and D.C. Dijkmans, “A 0.2-mW CMOS ΔΣ Modulator for Speech Coding with 80dB Dynamic Range”, IEEE J. Solid-State Circuits, vol. 31, 1873–1880, December 1996.

[25] J. A. Cherry, W. M. Snelgrove, “Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion,” Kluwer Academic Publishers, 2000.

[26] Ramón Tortosa, José M. de la Rosa, Angel Rodríguez-Vázquez and Francisco V. Fernández, “Analysis of Clock Jitter Error in Multibit Continous-Time ΣΔ Modulators With NRZ Feedback Waveform”, IEEE International Symposium on Circuits and Systems, May 2005.

[27] Y. Geerts and M. Steyaert, “Flash A/D specifications of multibit A/D converters,” in IEE ADDA, Glasgow, U.K., pp. 50–53, July 1999.

[28] Philip D. Allen, Douglas R. Holberg, “CMOS Analog Circuit Design,” Third Edition, Oxford University Press, 2012.

[29] Koen Uyttenhove and Michiel S. J. Steyaert, “A 1.8-V 6-bit 1.3-GHz flash ADC in 0.25-μm CMOS,” IEEE J. Solid-State Circuits, vol. 38, 1115–1122, July 2003.

[30] http://www.ti.com/lit/ug/slaa582/slaa582.pdf

[31] G. Yin, F. Op’t Eynde. W. Sansen. “A High-Speed CMOS Comparator with 8-b resolution”, IEEE J. of Solid-State Circuits, vol. SC-27, no. 2, pp. 208-211, February 1992.

[32] Bernhard D. Boser and Bruce A. Wooley, “The Design of Sigma-Delta Modulation Analog-to-Digital Converters”, IEEE J. of Solid-State Circuits, vol. SC-23, no. 6, pp. 1298-1308, December 1988.

Chapter 4

Circuit-Level Design

4.1 General consideration

The ΔΣ modulator is implemented in the 65nm CMOS bulk process of ST microelectronics. This single poly process uses a type P substrate and offers several front-end options such as low threshold voltage transistors, MIM capacitors, high-sheet resistors or deep N-well that are all free of charge through MPW runs. Deep N-well is extensively used in this design as it allows isolating the P-WELL of NMOS transistors from the substrate, which enables connecting the source terminal to the substrate of NMOS transistors to reduce modulation of the threshold voltage by the substrate noise. As PMOS transistors are realized within an N-well, they are inherently isolated from the substrate.
All the analog sub-blocks of the modulator are implemented with fully differential circuits to minimize the common mode noise, improve the power supply rejection ratio (PSRR) and reduce even-order harmonic distortion. The analog circuits are designed for an optimal performance at a nominal voltage supply of 1.2V and such as the ΔΣ modulator is functional with a supply fluctuation of ±10%. All the performance requirements that result from the system-level study are guaranteed for ±3σ variation of the process and a temperature range from -20°C to +105°C.

4.2 Loop Filter

Figure 4-1 shows the schematic of the CT ΔΣ modulator which details the implementation of the loop filter. Integrators are built around opamp-RC rather than Gm-C cells because they have higher linearity performance and better robustness over PVT variations. Furthermore, the virtual ground of the opamp-RC provides a low impedance node that facilitates the connection of a current-steering DAC. The feed-in coefficient f_{i5} is realized as the ratio of the capacitance C_{f5} to the feedback capacitance of the last integrator C_5, which avoids using an additional summing amplifier. Others feed-in and feedforward coefficients are implemented as resistance ratio. Passives that implement feed-in and feedforward coefficients are sized to meet the matching requirement of 1% as specified in Table 3-1.
The noise floor of the modulator is dominated by the thermal noise and the flicker noise of the front-end that is composed of the input resistors, the opamp of the main integrator and the unitary current cells of the main DAC.
The noise PSD referred to the input of the front-end can be approximated by equation 4-1 which is detailed in appendix D.

$$\mathrm{PSD\_total} \approx \underbrace{8kTR_1 \times \left[1 + 2\gamma \times \frac{V_{REF}}{V_{gt\_dac}}\right]}_{\textbf{THERMAL}} + \underbrace{\left[\frac{KFI_1}{fC_{ox}L_1^2 g_{m\_opamp}^2} \times (1+\alpha)\right]}_{\textbf{FLICKER}} \qquad (4\text{-}1)$$

K : **Boltzmann constant**
T : **absolute temperature**
R_1 : **input resistance of the main integrator**
γ : **noise factor (=2/3 for long channel devices)**
g_{m_opamp1} : **transconductance of the input stage of opamp1**
I_1 : **biasing current of input transistors of opamp1**
f : **frequency**
C_{ox} : **Gate-oxide capacitance per unit area**
KF : **flicker noise constant**
L_1 : **channel length of the input transistors of opamp1**
V_{REF} : **voltage reference of the quantizer**
V_{gt_dac} : **overdrive voltage of the unit current cells in DAC1**

Equation 4-1 shows that the flicker noise is dominated by the input stage of the opamp while the input resistors and the main DAC contribute the most to the thermal noise floor. For a given transconductance to current ratio, the flicker noise can be reduced by increasing the area of the devices up to a certain point (limited by parasitic capacitances).

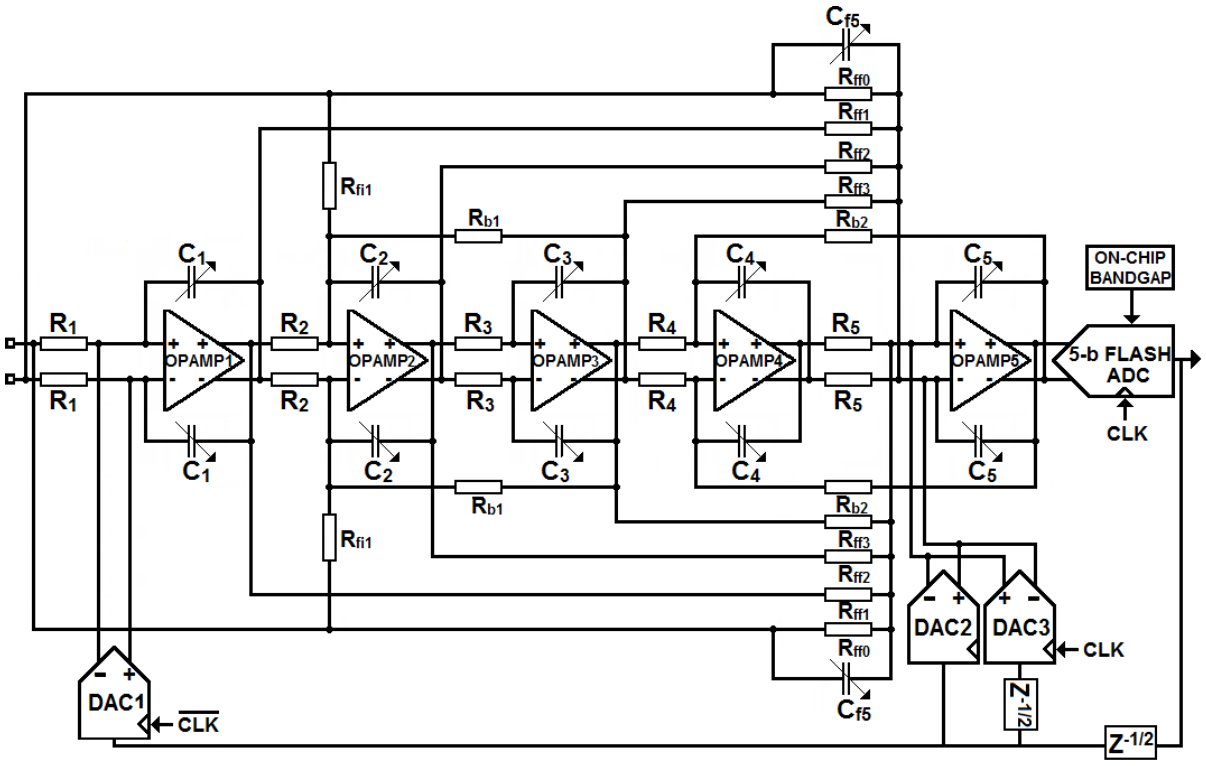


Figure 4-1. Circuit-level architecture of the CT ΔΣ modulator.

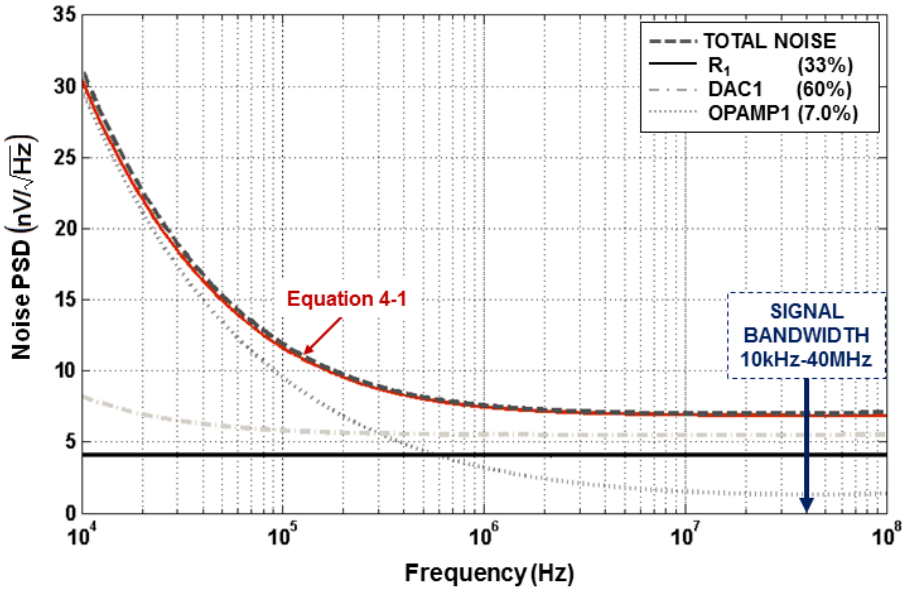


Figure 4-2. Breakdown of the noise contribution in the ΔΣ modulator front-end.

Regarding thermal noise, equation 4-1 shows that a fundamental limit exists which is set by the resistor value and a scaling factor whose value depends on the ratio of the reference voltage of the quantizer to the overdrive voltage of the current cells in the main DAC. In this design, the PSD of the flicker noise is set to $30\text{nV}/\sqrt{\text{Hz}}$ at 10KHz while the overdrive voltage of the current cells is set to ¼ of the supply voltage to optimize noise and matching performance.
The Figure 4-2 shows the contribution of each component to the noise PSD and the rms noise (integrated from 10kHz to 40MHz) contribution of each component in the front-end. The noise PSD predicted by equation 4-1 fits very well with the simulation which make it useful to budget the noise in a given process.

The targeted distortion of THD>14-bit imposes a stringent linearity requirement on the modulator front end because any harmonic components introduced by the first integrator or the main DAC (DAC1), translate into THD degradation for the ADC as a whole. The finite-GBW-induced voltage swing at the virtual ground of the first opamp (opamp1) is the main source of distortion in the front end as explained in Chapter 3. Usually, the value of the finite GBW of the first opamp is chosen equal to the sampling frequency and the original shape of the NTF is restored by coefficient tuning [1]. This design strategy guarantees high power efficiency at the cost of linearity performance because lowering the GBW increases the voltage swing at the virtual ground of opamp1. Moreover, even if the finite-GBW-induced phase shift through the loop filter is rigorously compensated by tuning components values [1], the robustness of the modulator stability against PVT variations cannot be guaranteed with a high yield. As shown in Figure 4-3, the main integrator embeds a 4-stage amplifier that achieves a GBW and a phase margin of 3.9GHz and 88° respectively which ensures low-distortion and low phase-shift against PVT variations. Each transconductance stage has its own common-mode feedback circuit (not shown in Figure 4-3) that ensures an optimal operating point for the differential path. The power consumption of the common-mode feedback circuits represent one-third of whole amplifier power budget.
The last stage (g_{m4}) uses minimum length devices to increase the phase margin while consuming low power. The main opamp consumes 20mA and its third-order harmonic amplitude at the modulator output is 100dB below the ADC FS. This guarantees a THD dominated only by the current-mismatch of DAC1. The performance of the main opamp is summarized in table 4-1.
A scaled version of opamp1 is used in the 5th integrator while 3-stage opamp are implemented in the other integrators to save area and power.
The circuit shown in Figure 4-4 [2] is used to compensate for the shifting of the RC time-constant that can vary by more than ±35% in this process. The feedback capacitors of each integrator are tuned to the ideal value with an accuracy of ±2%. To ensure a good matching between RC passives of the tuning circuit and those of the integrators each integrator has a dedicated on-chip auto-tuning circuit.

Table 4-1.Typical performance of the main opamp

PARAMETER	VALUE	UNIT
DC gain	45	dB
Open-loop GBW	3.9	GHz
Phase margin	88	°
Input referred noise density @10KHz @1MHz @40MHz	 30 3.2 1.3	 $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
Input referred noise integrated in [10KHz:40MHz]	11.6	µVrms
Input referred offset (±3σ)	±2	mV
HD3*	100	dBFS
Supply	1.2	V
Power consumption	24	mW

***simulated within the ΔΣ loop with a 10MHz single-tone**

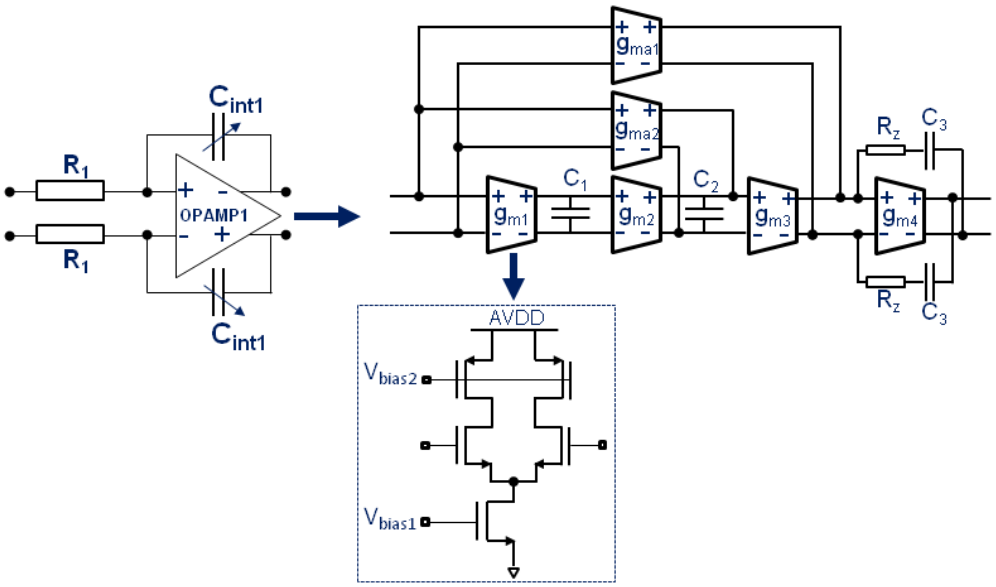


Figure 4-3. Block diagram of the opamp used in the modulator front-end.

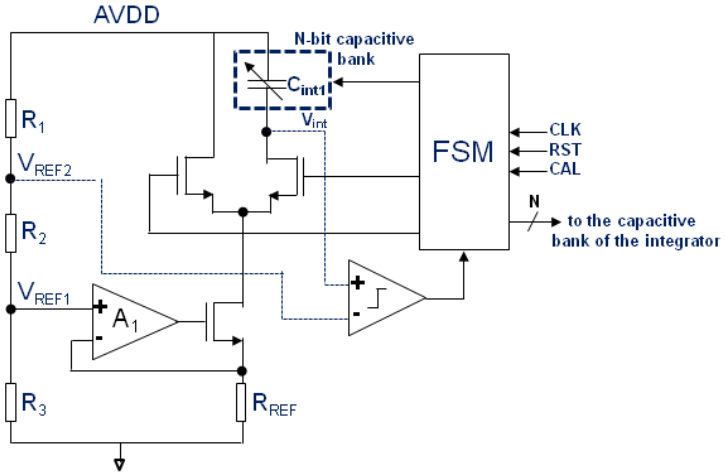


Figure 4-4. Circuit used to estimate and correct the RC time constant shift of the integrators [2].

4.3 Parasitic of the front-end

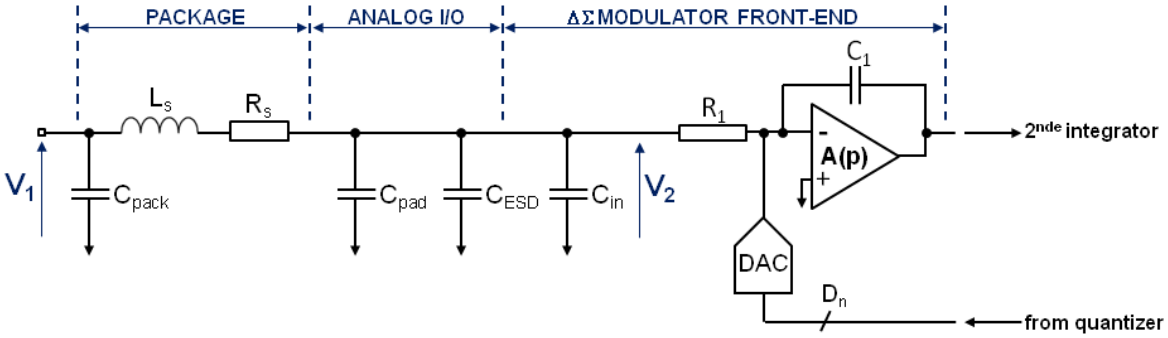


Figure 4-5. Input passive network composed by the parasitic of the package and those of the modulator front-end.

The input passive network in front of the ΔΣ modulator is shown in Figure 4-5. It implements a resonator whose transfer function, resonance frequency and quality factor are given respectively by equation 4-3 and equation 4-4.

$$H(p) = \frac{R_{int}}{R_{int}+R_{wire}} \times \frac{1}{\frac{R_{int}L_{wire}(C_{pad}+C_{ESD}+C_{in})}{R_{int}+R_{wire}}p^2+\left[\frac{R_{wire}R_{int}(C_{pad}+C_{ESD}+C_{in})+L_{wire}}{R_{int}+R_{wire}}\right]P+1} \quad (4\text{-}2)$$

$$\omega_o \approx \frac{1}{\sqrt{L_{wire}(C_{pad}+C_{ESD}+C_{in})}} \quad (4\text{-}3)$$

$$Q \approx \frac{1}{R_{wire}}\sqrt{\frac{L_{wire}}{(C_{pad}+C_{ESD}+C_{in})}} \times \left[\frac{1}{1+\frac{L_{wire}}{R_{int}R_{wire}(C_{pad}+C_{ESD}+C_{in})}}\right] \quad (4\text{-}4)$$

L_s : inductance of the bonding wire connecting the die pad to the package pin
R_{wire} : serial resistance of the inductance
C_{pack} : capacitance of the package pin
C_{pad} : capacitance of the I/O pad
C_{ESD} : equivalent capacitance of the input ESD network
C_{in} : input capacitance of the ΔΣ modulator
ω_o : resonance frequency of the input network
Q : quality factor of the resonator

When an IC prototype is targeted as proof of concept, many I/O pins may be required for test purpose only. It may results in a big package with non-negligible parasitic value.
In this work we have used a 120-pin CQFP package whose parasitic values are shown in table 4-2. The resulting frequency response of the input network is shown in Figure 4-6. Even if the resonance frequency is far from the signal edge (41 times), the peaking is high enough to amplify an interferer around the resonance frequency. This scenario is shown in Figure 4-7 and consists of a -2.5dBFS signal received without interferers (Figure 4-7(a)) and in presence of a -33dBFS interferer (Figure 4-7.(b)) at the input of the modulator. When no interferer is present, the modulator is stable because the input signal amplitude stays within the dynamic of the quantizer. In the case of Figure 4-7.b, the interferer is first amplified by 21.5dB before falling back at 280MHz where it is amplified a second time by the peaking of the STF that is approximately 9dB. As the input of the quantizer exceeds the MSA, the modulator becomes unstable and the SNR drops considerably.
The peaking due to the passive network must also be considered in application such as telecommunications where the signal may be received in the presence of strong interferers.
Another circumstance for which the peaking should be considered carefully is during the characterization of the ADC. The signal coming from the signal synthesizer must be filtered sharply to feed into the ADC.

Table 4-2. Parameters of the passive network composing the IC front-end

Package type	CQFP120
Package parasitic	
L_s (nH)	4
R_s (Ω)	0.05
I/O cell parasitic	
C_{pad} (pF)	1
C_{ESD} (fF)	340
ΔΣ Modulator parameters	
C_{in} (pF)	1
R_1 (Ω)	500

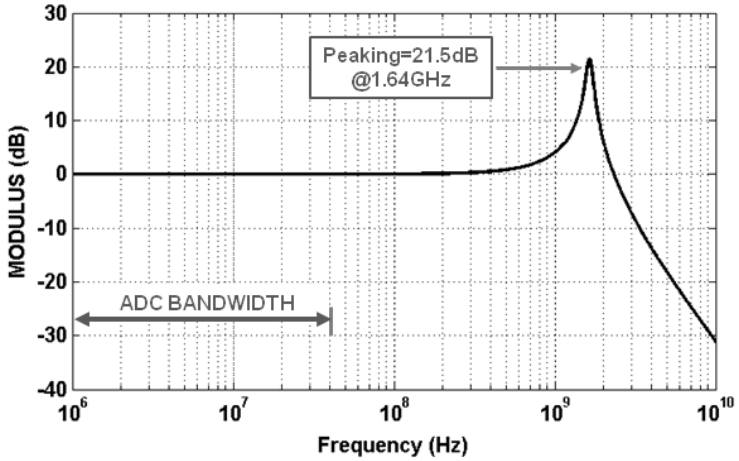
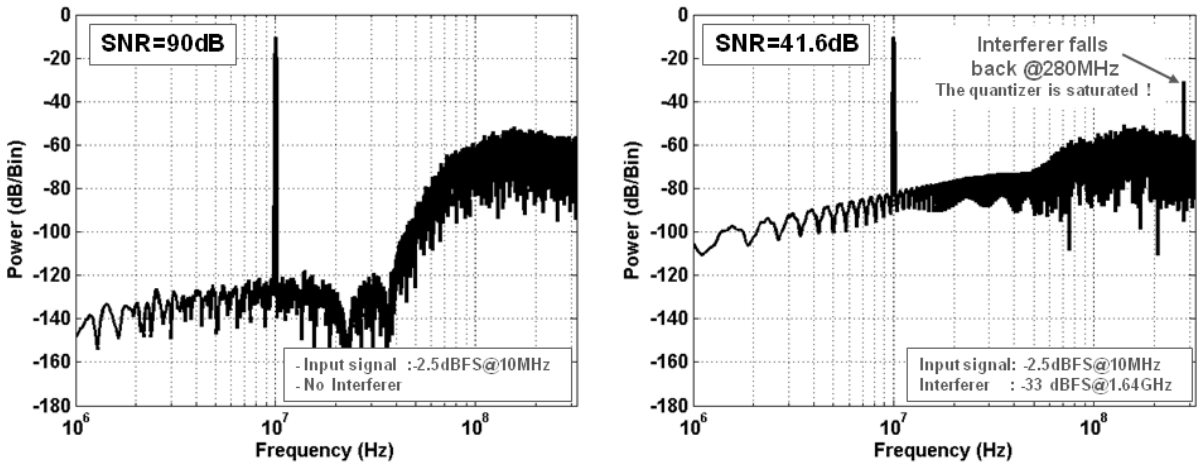


Figure 4-6. Frequency response of the input passive network composed by the parasitic of the package and those of the modulator front-end.



(a) **(b)**

Figure 4-7. Simulation of the ΔΣ modulator output PSD taking into account the transfer function of the input passive network and (a) with a -2.5dBFS input signal alone, (b) with a -2.5dBFS input signal plus a -33dBFS interferer at 1.64GHz.

4.4 Feedback DACs

4.4.1 Main DAC

The architecture of the unit-current cell used in the main DAC (DAC1) is shown in Figure 4-8. It consists of a regulated cascode current source with a pair of NMOS switches and two PMOS current sources that fixe the common-mode at the virtual ground of the opamp.
The switches are sized small to minimize the delay and the output capacitance of the current cell. Their gates are driven by high-crossing point buffers [3] that ensure that one transistor is always in the on-state and biased in saturation, allowing a double cascode configuration which further improves the output resistance of the DAC. A careful design of the clock distribution circuit and TSPC flip-flops (FF) [4] that drive DAC switches has led to an additive jitter value of only 137fs rms. This value leaves enough margin for the jitter of the clock-source. Contrarily to [3], the current cell drivers are implemented with only two PMOS transistors rather than four which reduce the propagation delay between the FF and the DAC output.
The boosting amplifier is a single-stage common-source amplifier whose GBW is optimized to boost the output impedance of the DAC over a wide frequency range. An impedance value higher than 3MΩ is obtained up to the band edge (40MHz) which makes the distortion mechanism due to the finite GBW of opamp1 negligible within the signal bandwidth.

The noise PSD of the main DAC referred to the modulator input is given by equation 4-5. It is dominated by the bottom transistors and the top current sources that fixe the output common mode of the DAC as detailed in appendix D. The first part of the equation 4-5 is related to the noise of the bottom current cells while the second part is due to the top current sources that control the common-mode at the DAC outputs.

$$\overline{V_{dac}^2}(f) \approx 16kT\gamma R_1 \times \frac{V_{REF}}{V_{gt\_dac}} + \frac{R_1 KF_{bot} V_{REF}}{fC_{ox} L_{bot}^2}\left[1 + \frac{KF_{bot}}{KF_{top}} \times \left(\frac{L_{bot}}{L_{top}}\right)^2\right] \quad (4\text{-}5)$$

Equation (4-5) shows that the thermal noise can be reduced by reducing R_1 or increasing the over-drive voltage ($V_{gt\ dac}$) of the current cells. The value of R_1 is chosen as a compromise between the noise and the size of the integrating capacitance while the value of $V_{gt\ dac}$ is limited by the available voltage supply. For example, in [5] a thick-oxide transistor is used to implement the current source which allows using a dedicated voltage supply of 2.5V for the DAC.
It should be noted that the noise of the biasing circuit is not taken into account in equation 4-5 because it is filtered by an on-chip RC filter whose pole is set to 200 KHz, as shown in Figure 4-9. The pole can be set to a lower frequency by connecting an off-chip decoupling capacitor to the IO pad that is connected to the V_{bias} node as shown in Figure 4-9.
The bandgap is a CMOS version of the BiCMOS circuit proposed in [6]. The bipolar transistor was implemented with a vertical MOS transistor.
Area requirement resulting from matching constraint study of section 3.3.2 is given by equation 4-8 [7] while the W/L ratio is obtained from the overdrive voltage and the LSB current of the DAC as shown in equation (4-9).

$$\left[\frac{\sigma(I_{LSB})}{I_{LSB}}\right]^2 = \frac{4\times\sigma^2(V_t)}{V_{gt\_dac}^2} + \frac{\sigma^2(\beta)}{\beta} \quad (4\text{-}6)$$

$$\left[\frac{\sigma(I_{LSB})}{I_{LSB}}\right]^2 = \frac{4\times A_{vt}^2}{V_{gt\_dac}^2\times(WL)} + \frac{A_\beta^2}{(WL)} \quad (4\text{-}7)$$

$$(WL) = \frac{\frac{4\times A_{vt}^2}{V_{gt\_dac}^2} + A_\beta^2}{\left[\frac{\sigma(I_{LSB})}{I_{LSB}}\right]^2} \quad (4\text{-}8)$$

$$\left(\frac{W}{L}\right) = \frac{I_{LSB}}{\frac{\mu C_{ox}}{2}\left(V_{gt\_dac}\right)^2} \quad (4\text{-}9)$$

By combining equation (4-8) and (4-9), the dimensions of the main transistor that satisfy noise and matching requirement are found.

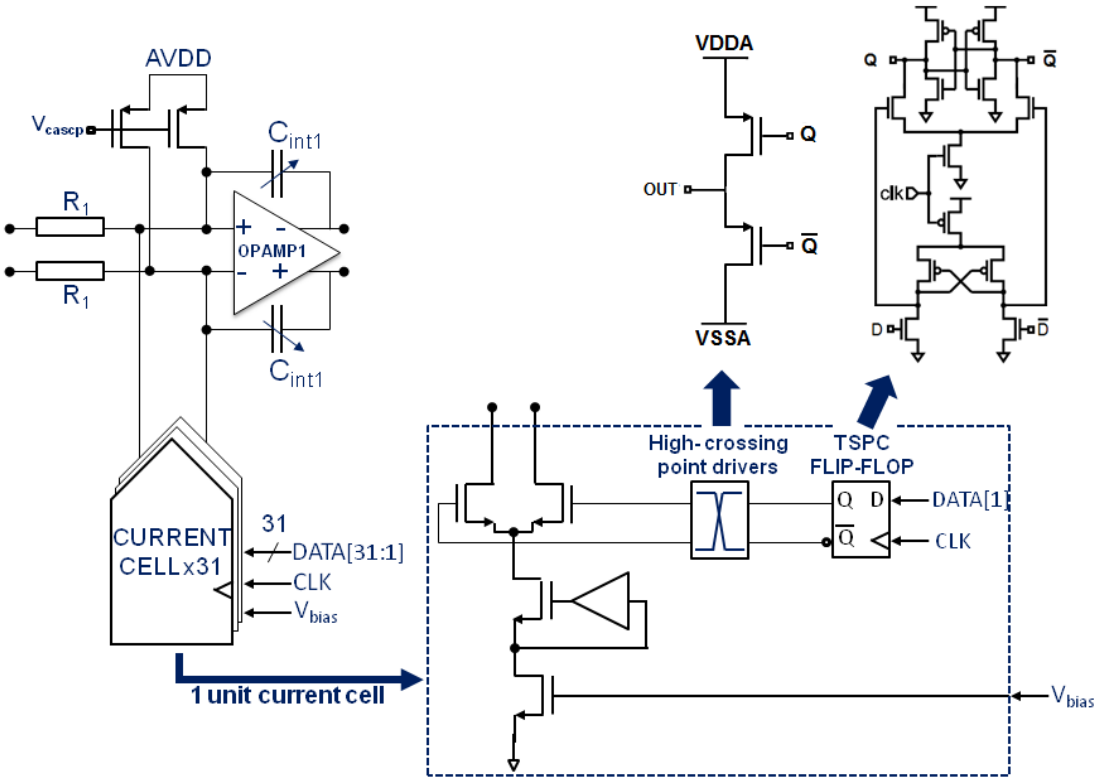


Figure 4-8. Schematic of one slice of the main DAC showing the regulated current source, the TSPC flip-flop [4] and the PMOS-only high-crossing point buffer.

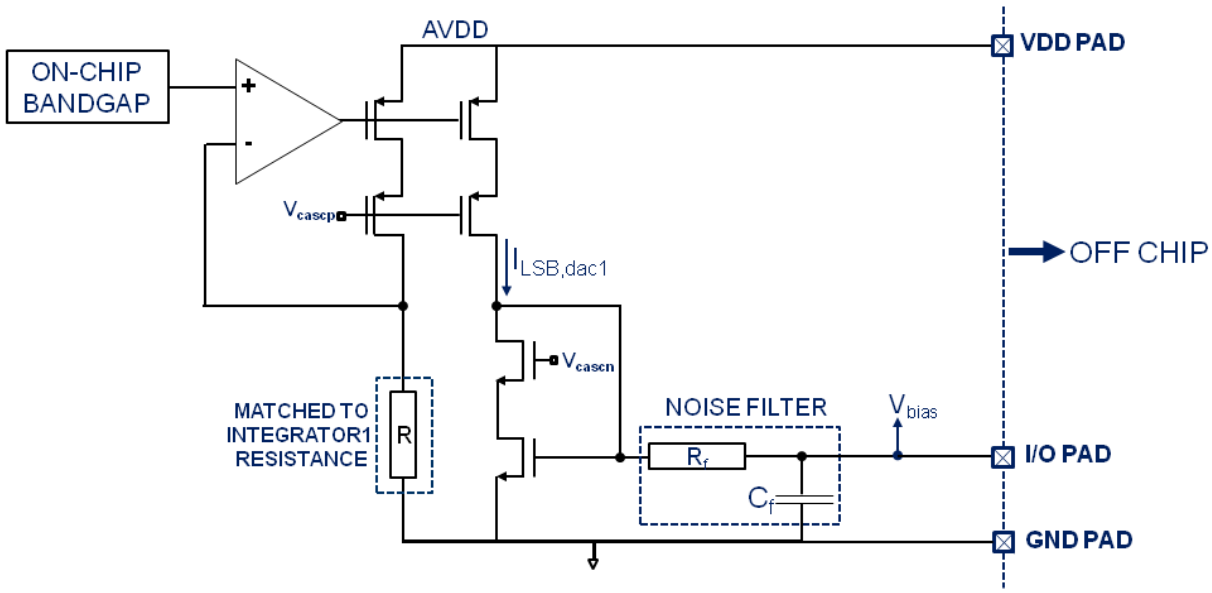


Figure 4-9. Schematic of the biasing circuit of the DAC.

It should be noted that degenerating the current source with a resistor [8] improves matching and noise performance but this technique is difficult to implement at low voltage supply due to the voltage drop along the resistor. The output capacitance value of DAC1 is 464fF whose 16% comes from the intrinsic capacitance of the current cell and 84% are due to the metal line that connects the current cells to the virtual ground of opamp1.

Table 4-3.Typical parameters of DAC1

PARAMETERS	VALUE	UNIT
Number of unit current cells	31	_
LSB current	50	µA
Unit cell impedance@40MHz	3.1	MΩ
Total input referred noise*	6	µV rms
Unit current matching (σ)	0.2	%
Aperture jitter	137	fs
Voltage supply analog digital	 1.2 1.0	 V V
Power consumption (31cells) analog digital	 3.84 1.1	 mW mW

4.4.2 Minor DACs

The loop-delay compensation technique adopted in this work was introduced in [9] and implemented in [10]. A shown in Figure 4-10, it consists in moving the compensation DAC (DAC_6) before the last integrator (R_5C_5-$opamp_5$). To keep the NTF unchanged, the input of DAC_6 must be multiplied by the transfer function of equation 4-10 before being processed by the last integrator. This operation is done in the digital domain by using the equivalent discrete transfer function of the derivator (Backward-Euler approximation) as expressed by equation 4-11.

$$H_5'(p) = \frac{1}{H_5(p)} = \frac{p}{\omega_{ug5}} \quad (4\text{-}10)$$

$$H_5'(z) = \frac{2f_s}{\omega_{ug5}} \times (1 - z^{-\frac{1}{2}}) \quad (4\text{-}11)$$

This operation is realized by DAC_{6a} and DAC_{6b} as shown in Figure 4-10.b. As the delay from the DWA output to the input of both DAC_2 and DAC_{6a} is the same, these two DACs are merged together as shown in Figure 4-10(c).
Compared to others compensation methods [11], this technique has the advantage of being robust and power efficient because the summing amplifier is replaced by a register.
The drawback is that the number of current cells connected to the virtual ground of the last opamp is doubled. As a 5-bit quantizer is used, it results in 62 unit current cells connected to the input terminals of the last opamp which may strongly reduce the GBW of the 5th opamp.

Applying the DWA to minors DAC has two advantages. First it relaxes the matching requirement on the minors DACs which translate in reduced area for current cell. The reduction of the DACs size results in a reduction of the output capacitance of the unit current cells. This technique allows aggressive scaling of DAC2 and DAC3 with negligible impact on the latency of the DWA.
The scaling of unit cells reduces the output impedance of the minor DACs which increase the harmonic distortion at the output of the 5th integrator. But these harmonics are shaped by the loop filter. Moreover, as the requirement on the output impedance of the minors DACs is relaxed compared to DAC1, their unitary current cells are implemented with regular cascode current sources to save area and power, as shown in Figure 4-11.
The total output capacitance value of DAC2 and DAC3 is 239fF whose 37% come from the intrinsic capacitance of the current cell and 63% are due to the metal line that connects the current cells to the virtual ground of the last integrator (R_5C_5-$opamp_5$).

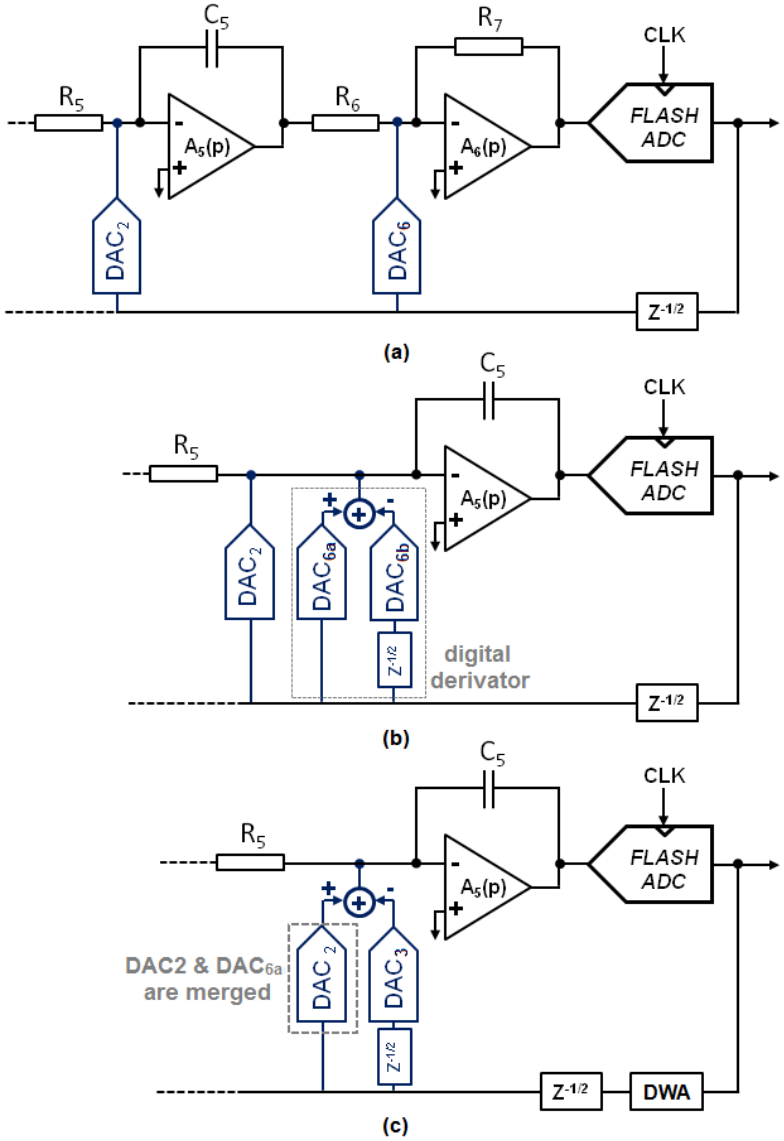


Figure 4-10. System level approach to compensate for excess loop delay (a) Classical approach, (b) The feedback coefficient K_{fb} is moved before the last integrator, (d) feedback coefficients that have the same delay are merged.

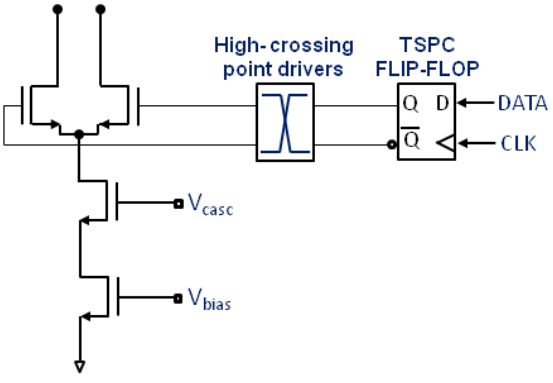


Figure 4-11. Unit current cell used in minors DACs (DAC2 & DAC3).

4.5 Quantizer

For the sake of simplicity, the single-ended schematic of the flash quantizer is shown in Figure 4-12. It consists of thirty-one comparators which convert the output of the loop filter into a thermometric code plus two comparators (not shown) that detect positive or negative signal excursions which might saturate the quantizer. The 2-bit code delivered by the overload-detection comparators might be exploited by a PGA to adjust the voltage swing at the input of the modulator within the voltage range of the quantizer.

An on-chip voltage buffer provides a copy of a voltage reference to a resistive ladder which generates the threshold voltages $V_{REF}[k]$ for the comparators. The schematic of one comparator slice is detailed in Figure 4-13. A front-end CMOS switch disconnects each comparator from the loop filter during the offset calibration procedure that is done after the power-up of the ADC IC. In normal mode (calibration off) the on-state resistance of the switch, together with the input capacitance of the quantizer create a pole whose value is set well beyond the sampling frequency of the modulator in order to preserve its stability. The noise and distortion requirement of the switch are greatly relaxed as they are shaped by the 5^{th}-order loop filter preceding the quantizer.

For each comparator, the offset value is estimated by a feedback loop which consists of a counter/integrator and a current-steering DAC. For each DAC code, the output of the comparator is integrated over several fractions of the clock period to reduce the influence of noise. When the mean value of the comparator output is equal to or greater than zero, then the counter stops and leaves the output current of the DAC at a value that compensates the offset voltage. After calibration, the residual offset is bounded within one DAC's LSB. Compared to [10], each comparator is calibrated around its trip point rather than around its input common-mode which has the benefit of correcting both static and dynamic offsets. As all the comparators are calibrated in parallel, the maximum calibration time is only 12.8 µs for the 33 comparators. If the application permits, the calibration may be redone during the lifetime of the circuit to compensate for the offset variation due to component aging.

The schematic of the preamplifier and the regenerative output latch used in one comparator are shown in Figure 4-14. The preamplifier is a double-differential amplifier [12] with a PMOS load and a resetting switch for faster overload recovery [13]. Compared to the architecture proposed in [10], our preamplifier uses a non-switching load, which strongly minimizes the "kickback" effect on the loop filter output and the reference ladder.

The digital gates used to generate the timing of the comparison step are shown in Figure 4-14. When the reset switch is opened, the voltage difference between the output of the loop filter and the reference voltage is performed. Immediately afterwards, the switches to the output latch are closed and the latch is started. The biasing current of the dynamic PMOS source as well as the size of the output latch are chosen such as the regenerative time constant of the latch is low enough to give enough time for the DWA and also to reduce metastability. In order to minimize kickback, the switches to the input stage are opened before the logic output reaches a large voltage difference.

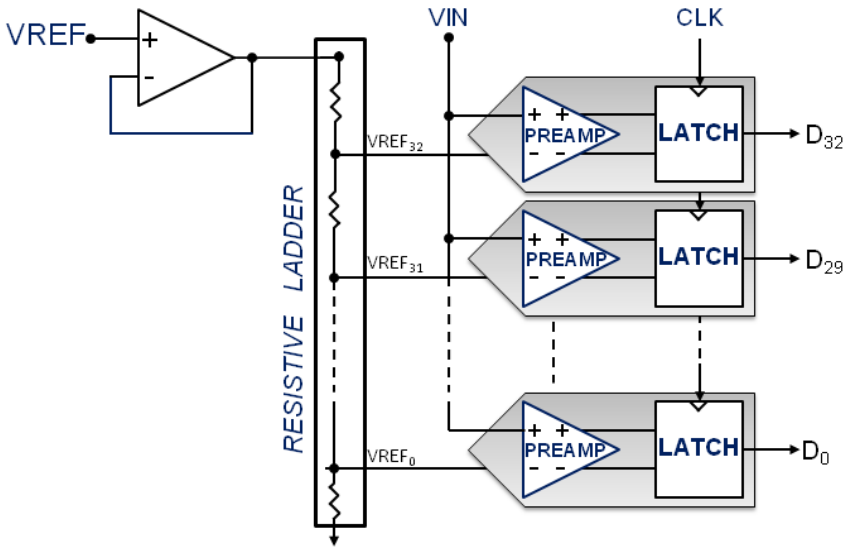


Figure 4-12. Schematic of the flash quantizer (single-ended version).

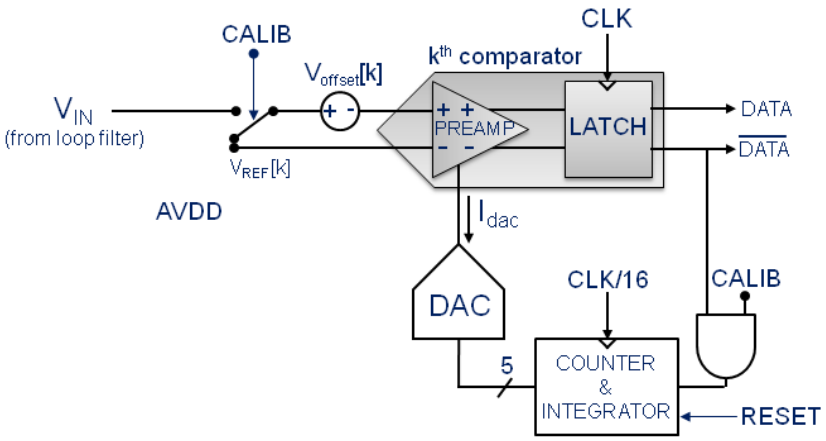


Figure 4-13. Schematic of one comparator cell.

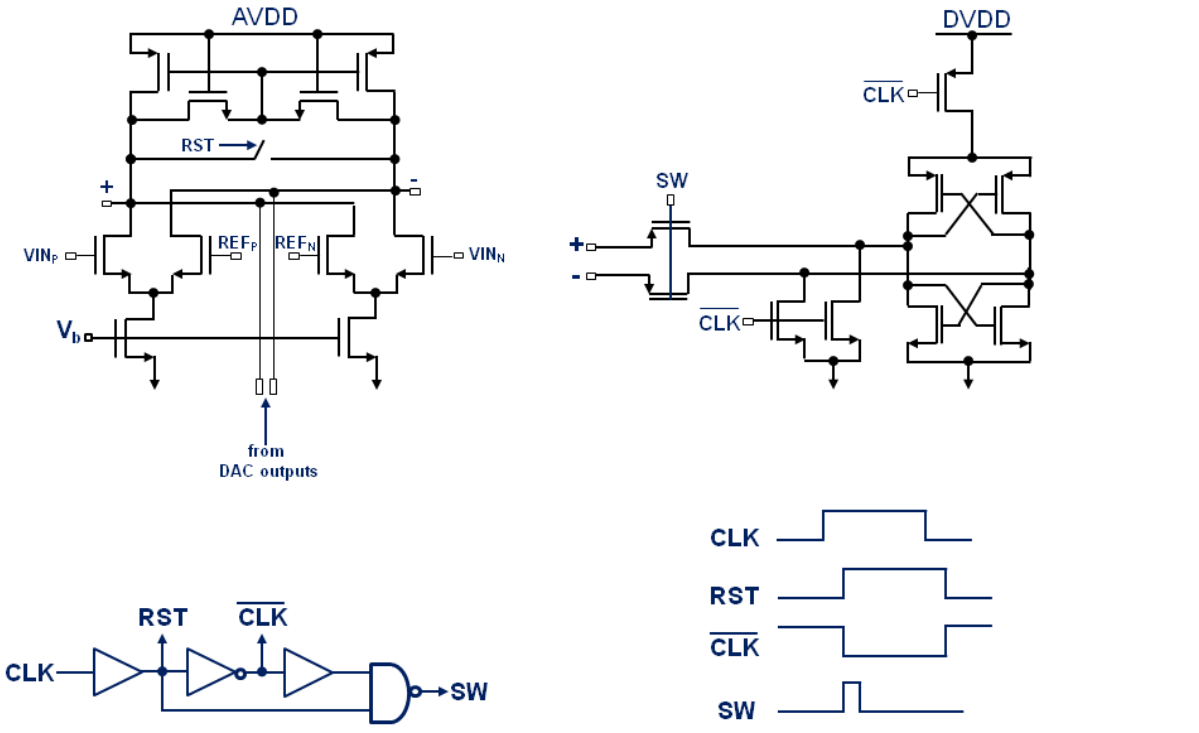


Figure 4-14. Schematic of the comparator circuitry consisting of a preamplifier and a regenerative output latch, timing diagram and digital gates used to implement it.

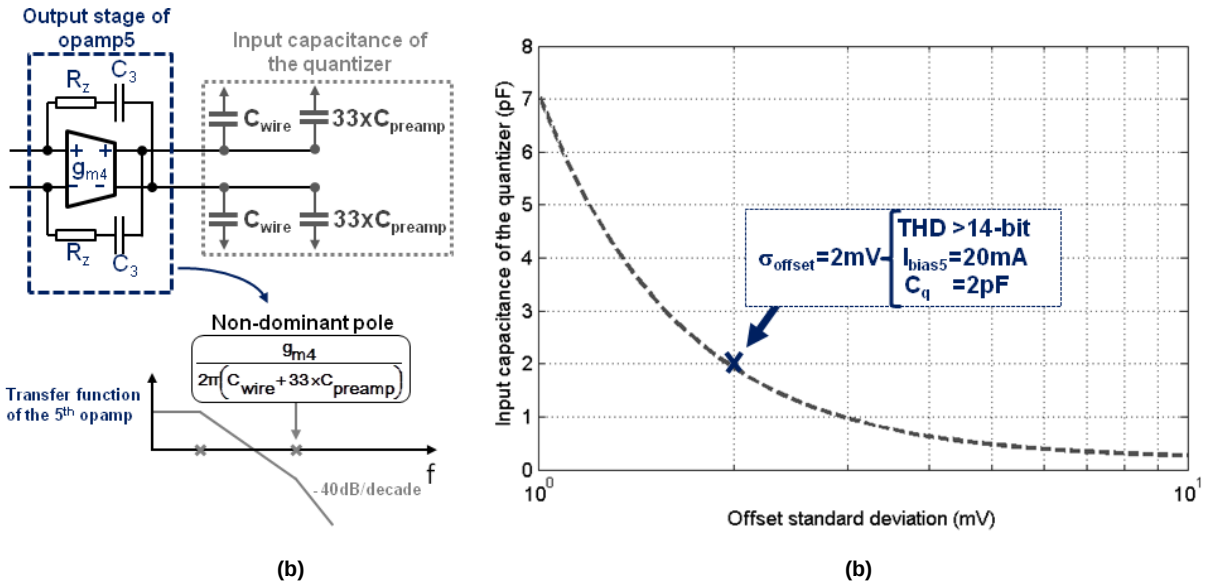


Figure 4-15. (a) Capacitive load of the last integrator, (b) Input capacitance of the preamplifier that must be driven by the loop filter as a function of the offset requirement.

As shown in Figure 4-15(a), the design of the preamplifier must be considered together with the output stage of the last integrator. The finite transconductance of the integrator output stage and the input capacitance of the quantizer create a non-dominant pole in the transfer function which degrade the phase margin of the last opamp. The expression of the input capacitance (C_q) of the preamplifier is approximated by equation (4-12) while the variance of the input referred offset of the preamplifier (σ^2_{os}) is given by equation (4-13).

$$C_q = N_c \times \left[\frac{2}{3} \times C_{ox} \times (WL)_{in}\right] + C_{wire} \tag{4-12}$$

$$\sigma^2_{os} = 2 \times \frac{(A_{vt\_n})^2}{(WL)_{in}} \tag{4-13}$$

C_{wire} : capacitance of the metal wire (~200fF)
C_{ox} : gate oxide capacitance per area unit
A_{vt_n} : Matching constant on the threshold voltage of the input NMOS transistors
V_{gt_n} : overdrive voltage of the input NMOS transistors
$(WL)_{in}$: area of input transistors of the DDA

There is a natural trade-off between the input referred offset of the comparator which require large transistors area and the input capacitance of the preamplifier which require small devices to keep its value low. This compromise is illustrated in Figure 4-15(b). System-level simulations presented in Chapter 3 revealed that the standard deviation of the offset should be kept below or equal to 0.06LSB (2mV) to guaranty a THD value of 14-bit with a high yield (99.7%). The resulting input capacitance of the quantizer is around 2pF which would require 20mA in the output stage of the last integrator to get a phase margin of 65°.
The other strategy that is used in this design consists in sizing the components of the comparator small and to compensate the offset of the comparator.
Thus, the input transistors of the preamplifier have an area of 0.14µm² which results in an input capacitance of only 80fF for the 33 preamplifiers. Including the parasitic capacitance of the metal wire that connects the loop filter to the quantizer increase this value to 280fF. The transistors of the output latch are sized near the minimum value allowed by the process. As a consequence, the resulting random offset (Gaussian distribution) of the comparator spans from -84mV to +84mV (±3σ) before calibration as shown in Figure 4-16(a). The resistors of the ladder are sized such as their contribution to the random offset is negligible. According to system-level simulation, if the input referred offset of each comparator is uniformly distributed in the 0-5mV range after calibration, this guaranties a linearity better than 14-bit for the ADC as a whole. Hence, the LSB of the calibration DAC is chosen equal to 5mV. To have a reasonable compromise between the yield and the complexity of the calibration system, the resolution of the DAC is chosen equal to 5-bit, which allows covering the offset range that spans from -80mV to + 80mV. In this prototype, the value of the LSB remains tunable off chip and can be adjusted to cover a wider offset range at the price of a larger residual voltage offset.

Thanks to calibration, the input referred offset of the comparator is uniformly distributed in the 0 to 5mV range as shown in Figure 4-16(b). Moreover, the output current of the last stage of the integrator is reduced by 60% compared to the case without calibration.

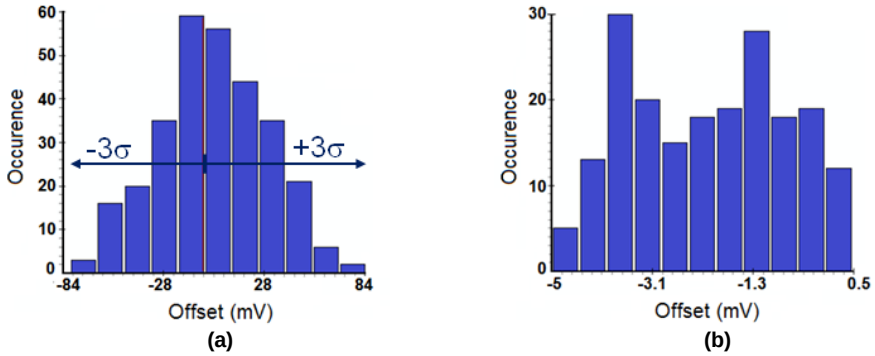


Figure 4-16. Histogram of the input referred offset simulated on one comparator after a transient simulation (a) before calibration, (b) after calibration of the samples that fall in the [-80mV:+80mV] range.

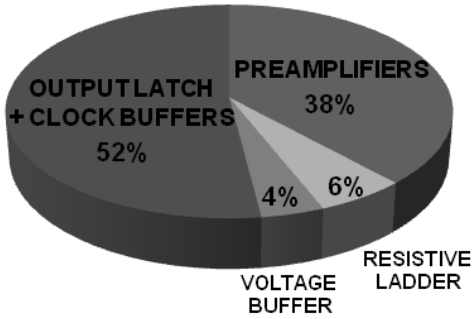


Figure 4-17. Breakdown of the power consumption among the main blocks of the flash quantizer.

Table 4-4.Typical parameters of the quantizer

PARAMETERS	VALUE	UNIT
Sampling rate	640	MHz
Reference voltage	0.8	V
Resolution	5	bit
Input capacitance *preamp* *wires*	 80 200	 fF fF
Preamp gain	2.1*	_
Preamp GBW	10*	GHz
Preamp -3dB BW	4.7*	GHz
Input offset range	0-5	mV
Worst conversion time		ns
DAC LSB	5	mV
Voltage supply *analog* *digital*	 1.2 1.0	 V V
Power consumption *analog* *digital*	 5 4	 mW mW

***** post-layout results

4.6 I/O interface

A simplified schematic of the ring showing how the supply and ground signals are distributed along the Input/Output (I/O) cells is shown in Figure 4-18. To avoid coupling between the analog and digital power lines and ground lines through the IO cells, the ring is divided in two sub-rings.
The number of power/ground cells must be chosen according to the maximum voltage drop tolerable and the maximum ringing due to the inductance of the bonding wires. This is especially important for digital cells because the Ldi/dt noise [14] may induce important delay in the digital gates.
Another important question that may be anticipated before the fabrication of the circuit is how capturing the high-speed bit-stream at the output of the modulator.
The CMOS I/O buffers available in the PDK are limited to a use frequency of 300MHz while the data rate at the modulator output is 640MSPS. CMOS buffers were used at the output of the decimator, for the 16-bit data interface whose speed is limited to 80MSPS.
To acquire data at the modulator output, dedicated buffers were designed. They were sized to drive the parasitic of the package as well as those of the logic analyzer probe as shown in Figure 4-19.
Current mode logic (CML) buffers were chosen because they use differential signaling. The architecture of the CML buffer consists of two cascaded differential pairs with resistive load. A design methodology for the implementation of multi-stage CML buffers is detailed in [15]. The performance of the CML buffers is summarized in Table 4-6.
Another great advantage of CML buffers over its CMOS counterparts is the lower ringing on the power supply line as shown in Figure 4-20. Six buffers are used to capture the 5-bit output from the modulator plus the clock signal that allows synchronized acquisition with the logic analyzer.
It should be noted that coding techniques can be used to reduce the noise influence when capturing high-speed data [16] but at the cost of extra on-chip hardware. A breakdown of the power consumption among the different I/O cells is detailed in Table 4-5.

Table 4-5. Power consumption of the digital I/O cells and analog I/O cells

PARAMETERS	VALUE	UNIT
Power consumption of I/O buffers		
CMOS	25	mW
CML	40	mW

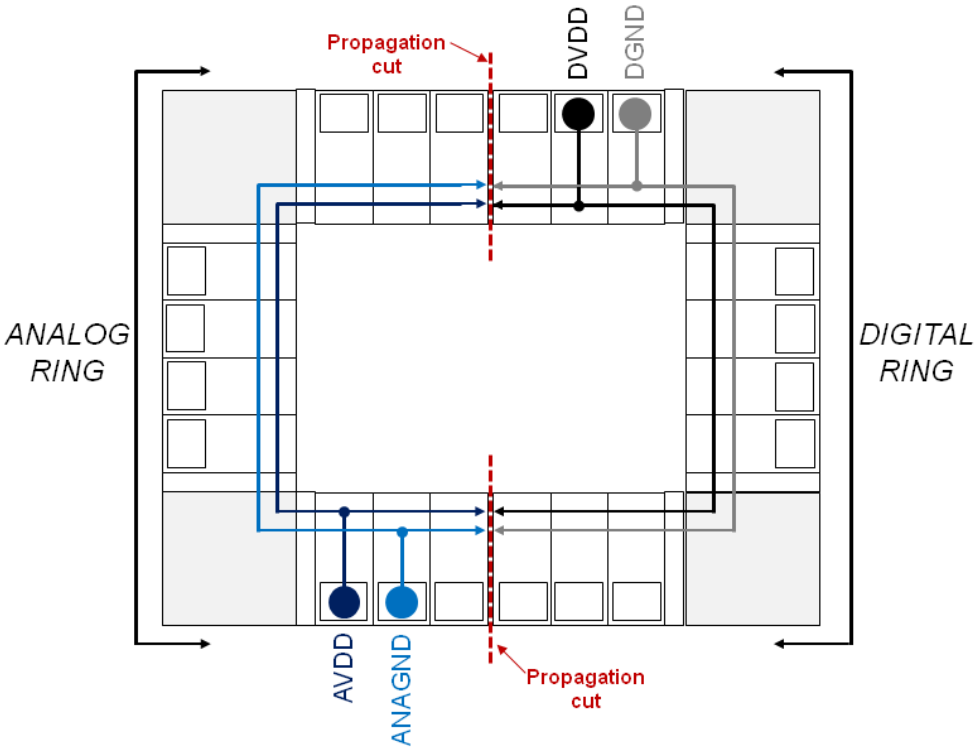


Figure 4-18. Power supply and ground partitioning in the I/Os ring.

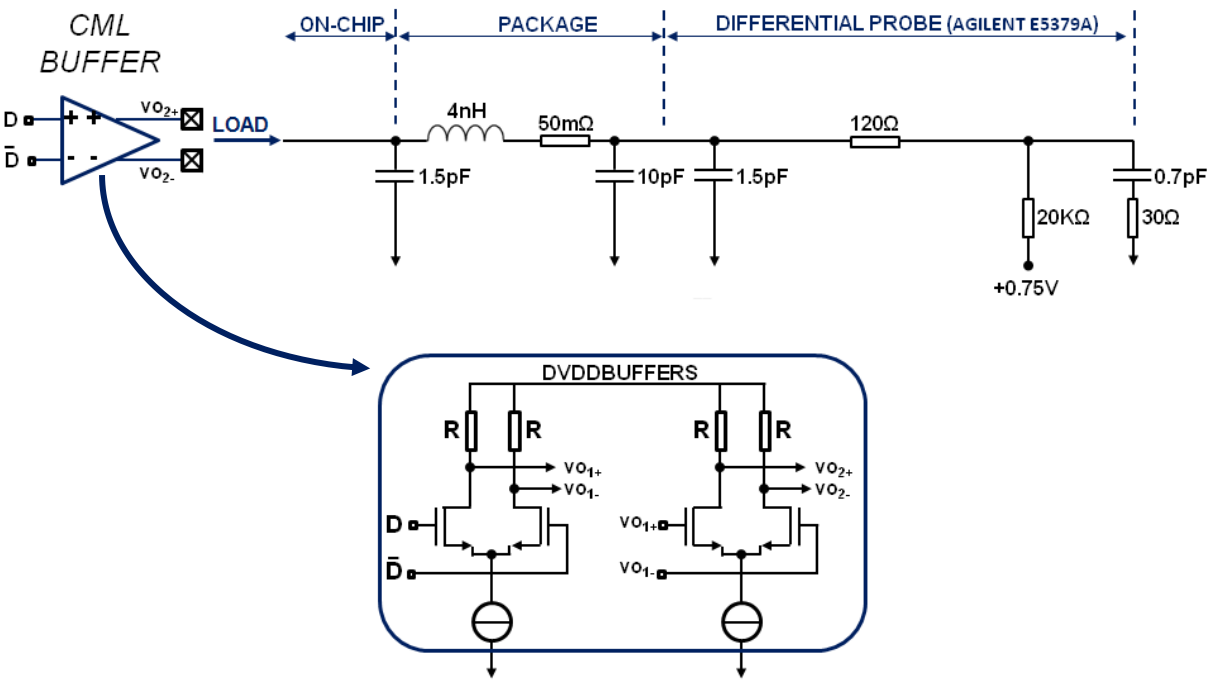


Figure 4-19. (a) CMOS buffer and the equivalent schematic of the load, (b) CML buffer and the equivalent schematic of the load.

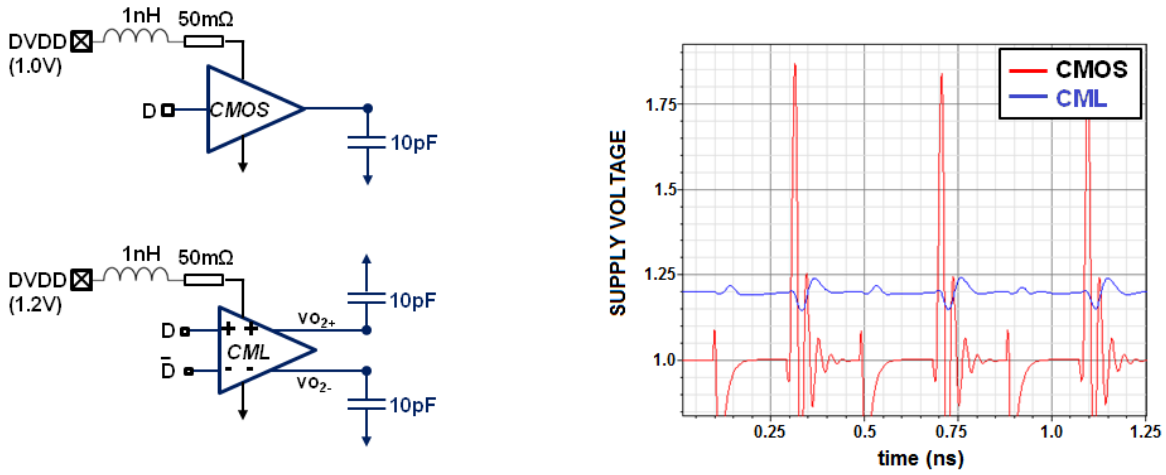


Figure 4-20. Comparison of voltage ringing on power supply between a CMOS buffer and CML buffer.

Table 4-6.Typical parameters of the CML buffer

PARAMETERS	VALUE	UNIT
Max data rate*	750	MSPS
Input offset (σ)	1.5	mV
Input capacitance	25	fF
Output swing	250	mV_{pp}
Power consumption	7.2	mW
Voltage supply	1.2	V

*C_{LOAD}=10pF (single-ended)

4.7 Summary

In this chapter we have presented the circuit-level implementation of each sub-block of the modulator. The architecture of the main components was chosen to fulfill the design requirements specified in Chapter 3 and their schematics was detailed. Design guidelines were given to implement a robust modulator while reducing as much as possible the power consumption.
We have also noted that the testing environment of the IC prototype must be anticipated and taken into account during this design step.
In the next chapter, the circuit-level design and simulation results are confronted with the measurements results.

4.8 References

[1] P. Witte, et al., "A 72dB-DR ΔΣ CT Modulator Using Digitally Estimated Auxiliary DAC Linearization Achieving 88fJ/conv in a 25 MHz BW," ISSCC Dig. Tech. Papers, pp. 154–155, February 2012.

[2] Bo Xia, Shouli Yan, and Edgar Sánchez-Sinencio, "An RC Time Constant Auto-Tuning Structure for High Linearity Continuous-Time ΣΔ Modulators and Active Filters », IEEE Trans. on Circuits and Systems-I: Regular Papers, VOL. 51, NO. 11, November 2004.

[3] Katayoun Falakshahi, Chih-Kong Ken Yang, and Bruce A. Wooley, "A 14-bit, 10-Msamples/s D/A Converter Using Multibit Modulation," IEEE J. of Solid-State Circuits, VOL. 34, NO. 5, May 1999.

[4] Yuan Ji-Ren, Ingemar Karlsson, and Christer Svensson, "A True Single-Phase-Clock Dynamic CMOS Circuit Tectilque," IEEE J. of Solid-State Circuits, VOL. SC-22,NO. 5, October 1987.

[5] Hajime Shibata et al., "A DC-to-1 GHz Tunable RF ADC Achieving DR 74 dB and BW 150 MHz at 450 MHz Using 550 mW," IEEE J. of Solid-State Circuits, VOL. 47, NO. 12, December 2012.

[6] Piero Malcovati, Franco Maloberti, Carlo Fiocchi, and Marcello Pruzzi, "Curvature-Compensated BiCMOS Bandgap with 1-V Supply Voltage," IEEE J. of Solid-State Circuits, VOL. 36, NO. 7, July 2001.

[7] Marcel J. M. Pelgrom, "Matching Properties of MOS Transistors," IEEE J. of Solid-State Circuits, vol.24, no. 5, pp. 1433–1440, October 1989.

[8] Matthew Park and Michael H. Perrott, "A 78 dB SNDR 87 mW 20 MHz Bandwidth Continuous-Time DS ADC With VCO-Based Integrator and Quantizer Implemented in 0.13 μm CMOS," IEEE J. of Solid-State Circuits, VOL. 44, NO. 12, December 2009.

[9] J. A. Cherry and W. M. Snelgrove, "Excess loop delay in continuous time delta–sigma modulators," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 46, no. 4, pp. 376–389, April 1999.

[10] G. Mitteregger, et al., "A 14 b 20 mW 640 MHz CMOS CT ΔΣ ADC with 20MHz signal bandwidth and 12b ENOB," IEEE J. of Solid-State Circuits, VOL. 44, NO. 12, December 2006.

[11] Matthias Keller, Alexander Buhmann, Jens Sauerbrey, Maurits Ortmanns, and Yiannos Manoli, "A Comparative Study on Excess-Loop-Delay Compensation Techniques for Continuous-Time Sigma–Delta Modulators," IEEE Trans. on Circuits and Systems-I: Regular Papers, VOL. 55, NO. 11, December 2008.

[12] Eduard Sackinger and Walter Guggenbuhl, "A Versatile Building Block: The CMOS Differential Difference Amplifier," IEEE J. of Solid-State Circuits, VOL.SC-22, NO.2, April1987.

[13] Michael Choi and Asad A. Abidi, "A 6-b 1.3-Gsample/s A/D Converter in 0.35μm CMOS," IEEE J. of Solid-State Circuits, VOL. 36, NO. 12, December 2001.

[14] Patrik Larsson, "di/dt Noise in CMOS Integrated Circuits," Analog Integrated Circuits and Signal Processing, Volume 14, Issue 1-2, pp 113-129, September 1997.

[15] Payam Heydari, and Ravindran Mohanavelu, "Design of Ultrahigh-Speed Low-Voltage CMOS CML Buffers and Latches," IEEE Trans. on Very Large Scale Integration Systems, VOL. 12, NO. 10, October 2004.

[16] Ankesh Jain and Shanthi Pavan, "Characterization Techniques for High Speed Oversampled Data Converters," IEEE Trans. on Circuits and Sytems—I: Regular Papers, VOL. 61, NO. 5, May 2014.

Chapter 5

Measurement results

5.1 Test Setup description

The test setup used to evaluate the dynamic performance of the prototype ADC is shown in Figure 5-1. Here, an analog signal source (R&S AFQ100A) drives a sine wave tone into a passive bandpass filter (K&L D5BT-6/12) of which the central frequency can be swept over the whole signal bandwidth of the ADC. It suppresses the harmonics and the noise of the signal source, which ensures that the measured resolution is limited by the performance of the ADC only. An RF transformer (Mini-Circuits ADT1-6T+) converts this spectrally purified tone into a differential signal that serves as the input to the prototype ADC.
The clock signal is provided by a wideband generator (R&S SMA 100A), which can generate low-jitter sine waveform (50 fs_{rms} in the bandwidth of interest). The 5-bit differential output generated by the prototype ADC is acquired by of a high-speed logic analysis system (Agilent 16901) that has a memory depth of 4MB. Stored data are then post-processed with MATLAB on a PC.

All DC supplies are provided by LDO regulators. Analog core supply (1.2V), digital core supply (1.0V) and I/Os supply (2.5V) are separated as well as their ground. Each supply pin is decoupled with large off-chip capacitors that are soldered as close as possible to the package in order to minimize the inductance of the track. In practice, high value capacitors have a high intrinsic serial inductance value which limits their decoupling action to a limited frequency range. To reduce this effect several capacitors with different values are put in parallel. The input common mode of the ADC (V_{CM}) is generated by an off-chip resistive divider supplied by the clean analog 1.2V supply (not shown in Figure 5-1). The tap of the resistive divider is decoupled and connected to the middle point of the transformer.

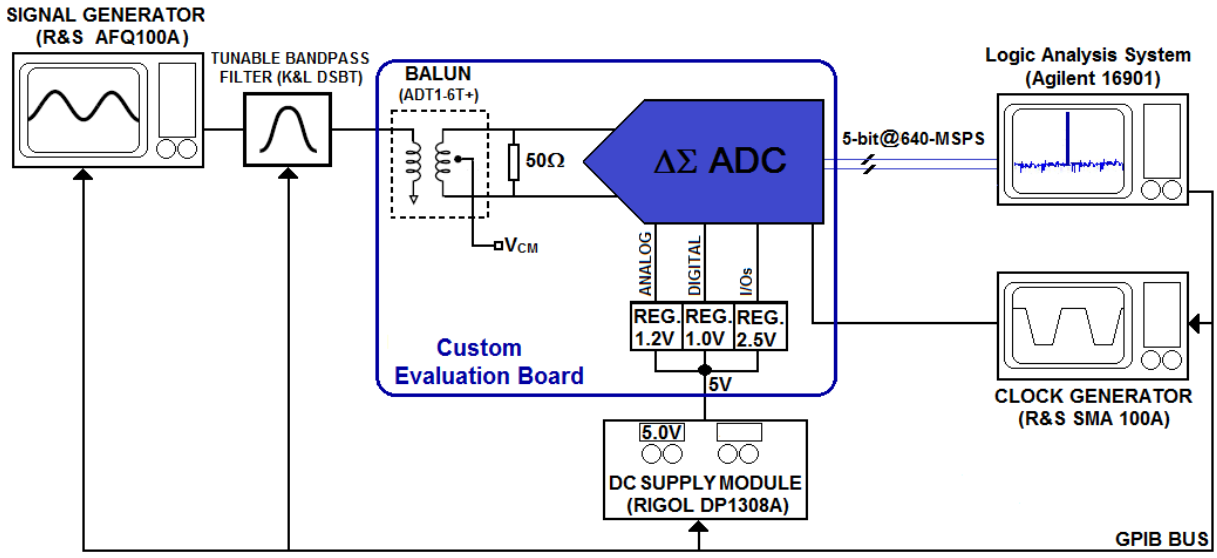


Figure 5-1. test setup for the evaluation of the prototype ADC.

The chip micrograph of the IC prototype is shown in Figure 5-2. It was fabricated in 65nm 1P7M CMOS process through the MPW program of the CMP [1]. The active die area is 2.35mm² including the ΔΣ modulator, a bandgap reference, a programmable decimation filter, high-speed CML buffers, all tuning and calibration circuits. The die is packaged in a 100 pins CQFP package. Analog and digital blocks use 1.2V and 1V of voltage supply respectively. Digital blocks were isolated in a deep N-well to reduce the coupling with the analog blocks through the substrate. The sensitive analog blocks such as the bandgap and the master bias circuit were placed at the top left part of the chip, far from the components that have a switching activity. Tiling is avoided above analog blocks that require good matching [2].

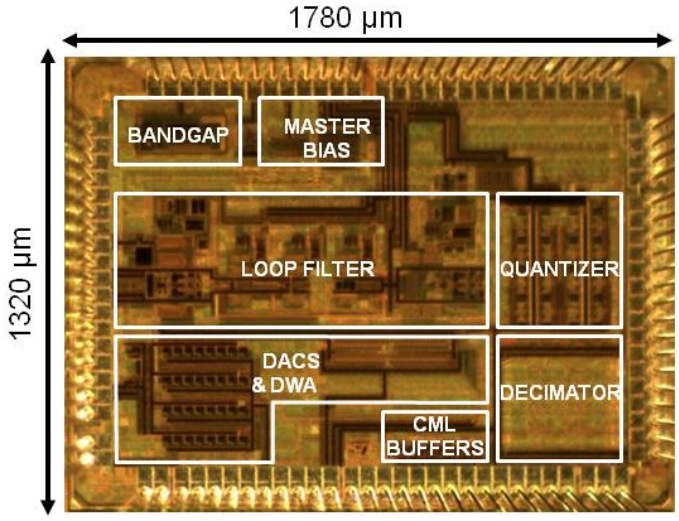


Figure 5-2. Die photo of the prototype ADC fabricated in ST's 65nm ST CMOS process.

5.2 First measurement results

The ADC was designed such as the thermal noise is the dominant noise source from 10KHz to 40MHz. To measure the noise floor down to 10KHz, the resolution of the FFT should be at least 10kHz. As the sampling frequency is 640MHz, the logic analyzer must capture 2^{16} points in one time. As the output of the ΔΣ modulator is a 5-bit word, it results in $5x2^{16}$=32768 samples.
The frequency of the input signal is always chosen as a multiple of the FFT resolution and the captured samples are windowed with a Blackman window to reduce spectral leakage.
The RC time constant of the integrators and the offset of the comparators are auto-calibrated once after the test setup power up. No calibration is redone during the measurements procedure.

The measurements on one of the twenty-five samples reveal that the prototype is functional with and without input signal. Figure 5-3(a) and Figure 5-3(b) show the flatness of the noise floor within the signal bandwidth which proves that the thermal noise is the dominant noise source as specified during the design step. The 5^{th} order noise shaping is also clearly visible on the PSD of the modulator output, with and without input signal.
However, the noise and linearity are worst than expected when the DWA is turned-on. First the noise floor increases by 3dB, which decrease the SNR by the same amount. Secondly, the DWA reduces the odd harmonics but increases the even order harmonics, especially the second-order one as shown in Figure 5-3(b). It is better illustrated in Figure 5-3(c) where the HD2 value degrades strongly when the DWA is turned-on.
Regarding the third-order harmonic, its value improves when the DWA is turned-on as shown in Figure 5-3(d).

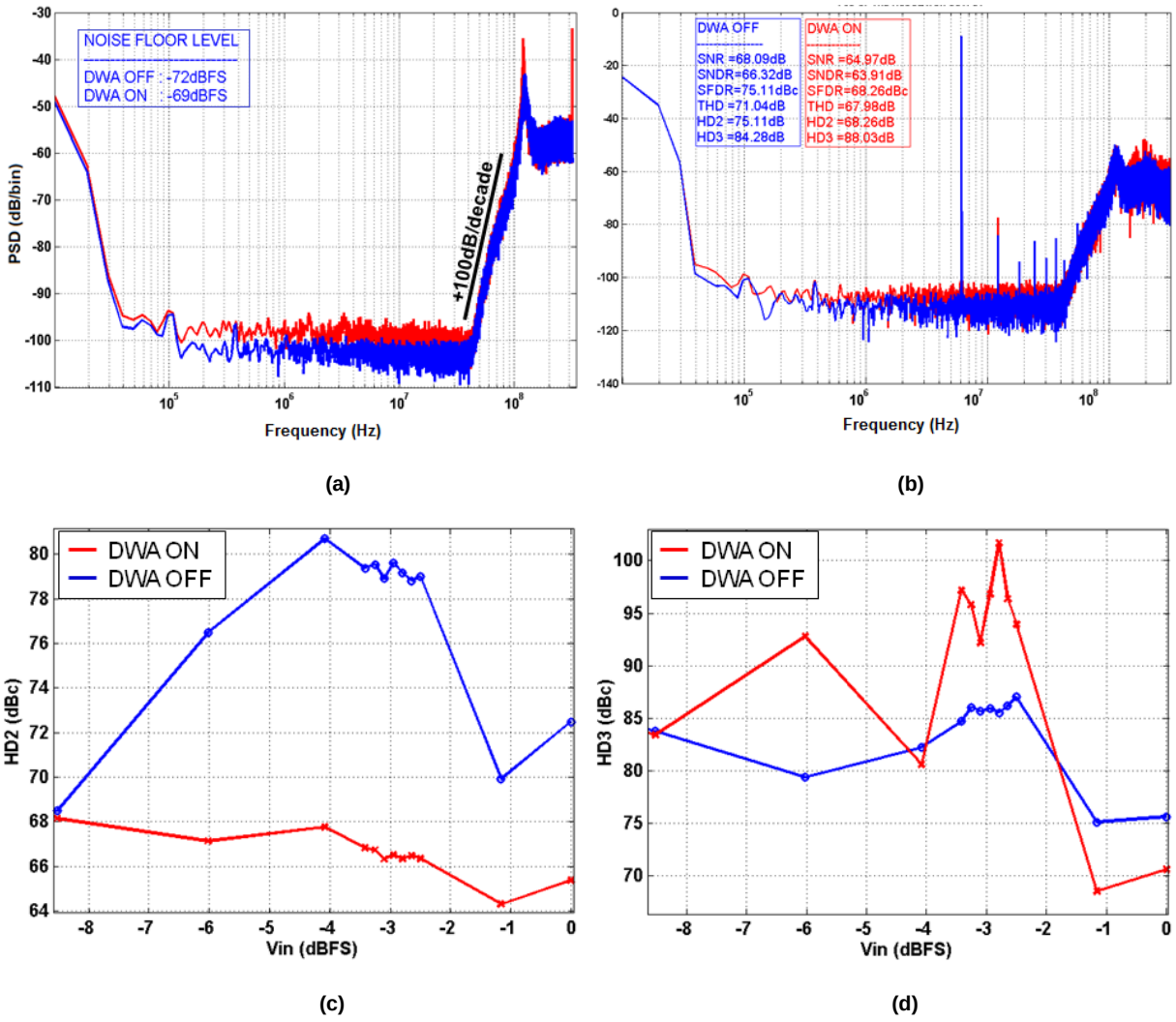


Figure 5-3. (a) PSD of the modulator output without input signal, (b) PSD of the modulator output with a 6MHz input sine tone of –4dBFS, (c) Measured second-order harmonic distortion as a function of the input signal amplitude with and without DWA (d) measured third-order harmonic distortion as a function of the input signal amplitude with and without DWA.

5.3 Measurement results analysis

To understand the problem, extensive research in the literature was done to check if this issue has already been addressed in the past. It has been found in [3] that Inter-Symbol Interference (ISI) in a DAC that uses DWA algorithm produces similar performance degradation behavior. The input common-mode at the modulator front-end may be a source of distortion also [4]. Finally, the modulation of the digital voltage supply of the DAC data buffers by the signal is another source of distortion. All these potential sources of distortion are analyzed in the following sub-sections.

5.3.1 Inter-Symbol Interference

As shown in Figure 5-4(a), due to mismatch between the switching components of I_P and I_N terminals, the current pulse delivered by each unitary cell of a current-steering DAC has unequal rise and fall time. This non-ideality is referred in the literature as ISI [5]. This imbalance creates an error that is signal dependent as shown in Figure 5-4(b). Here, the energy of two patterns is different while they have the same number of '1' and '0' but ordered differently. The energy error in the pattern "101" is higher because the number of transition is higher.
From this observation, it is obvious that the error depends on the level of asymmetry between the DAC pulses but also on the number of transitions. This last point is the explanation of the performance degradation when the DWA is turned on.

The purpose of the DWA is to use the maximum number of unit current cell in order to average the static mismatch error over time. As the switching activity of the DAC increases when the DWA is turned on, the number of transition increases, increasing the occurrence of transient errors. As the ISI-induced errors are signal-dependent, the linearity of the modulator is strongly degraded when the DWA is turned-on.

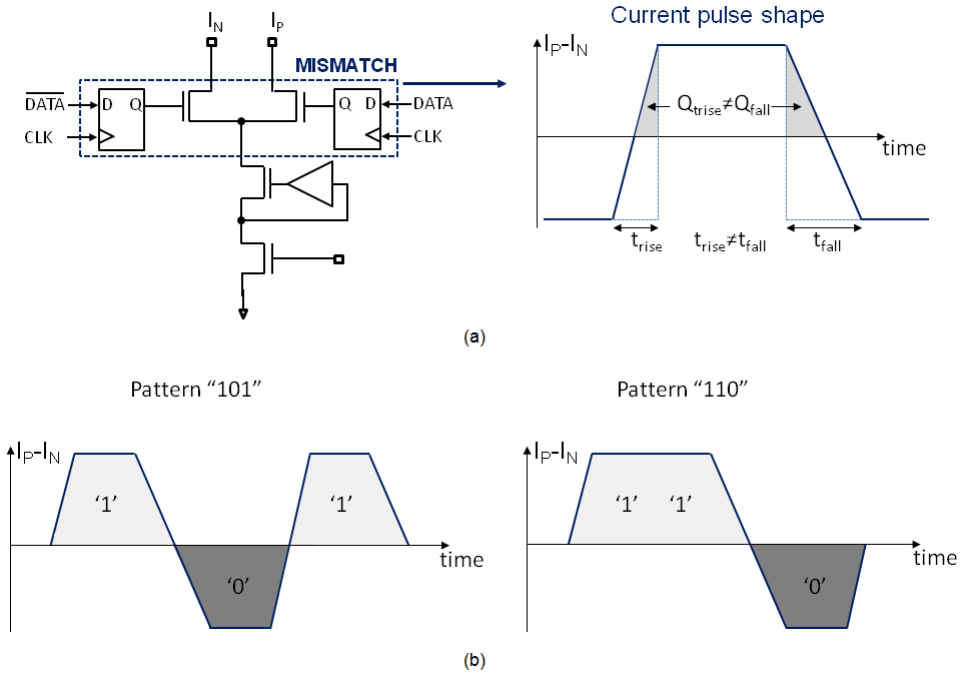


Figure 5-4. (a) Asymmetry between fall and rise time of the DAC pulse due to mismatch between the switching components, (b) DAC output-current shape for two patterns that have the same number of '1' and '0' but ordered differently.

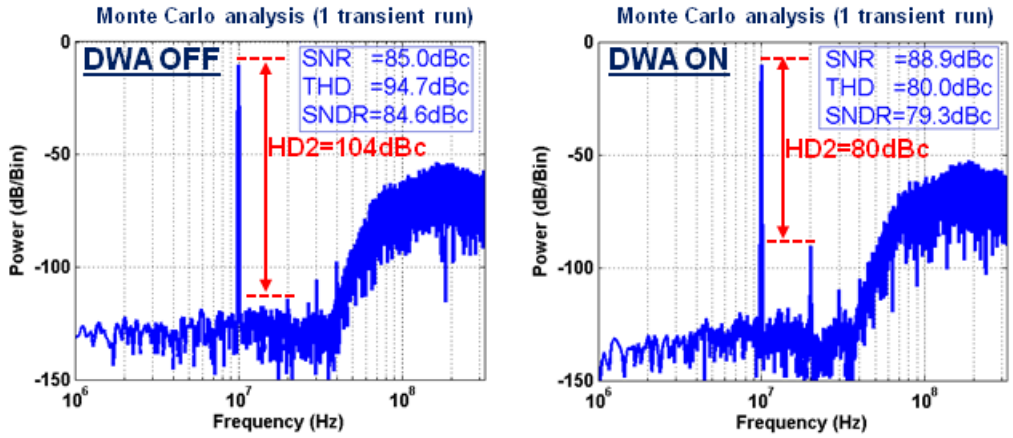


Figure 5-5. Output PSD of the modulator (FFT=16384 points) with mismatch in the switches and their drivers only and when the DWA is (a) turned off, (b) turned on.

To confirm this hypothesis, a transient simulation of the modulator is performed with random mismatch in the DAC switches and their drivers only (as shown in Figure 5-4(a)-left). The result when the DWA is turned-off and turned-on is shown in Figure 5-5(a) and Figure 5-5(b) respectively. The degradation of the second-order harmonic when the DWA is turned on is clearly visible.

To extend this result to a significant number of runs, the difference between the fall and rise time of the current pulse was extracted by a Monte-Carlo analysis. The difference has a Gaussian distribution with a zero mean value and a standard deviation of 1ps.

We built a simple verilog-A model of the DAC that takes into account the asymmetry between the rising and the falling time of the current pulse. For each of the 31 unit current cells, a random mismatch between the rise and fall time has been added (zero mean value and σ=1ps). A transient simulation was performed on the modulator for the two cases shown in Figure 5-6. The results of Figure 5-6(a) were obtained with the DAC described at transistor level and taking into account the mismatch in the switches and their drivers only. The results of Figure 5-6(b) were obtained with the verilog-A model of the DAC, which takes into account ISI.

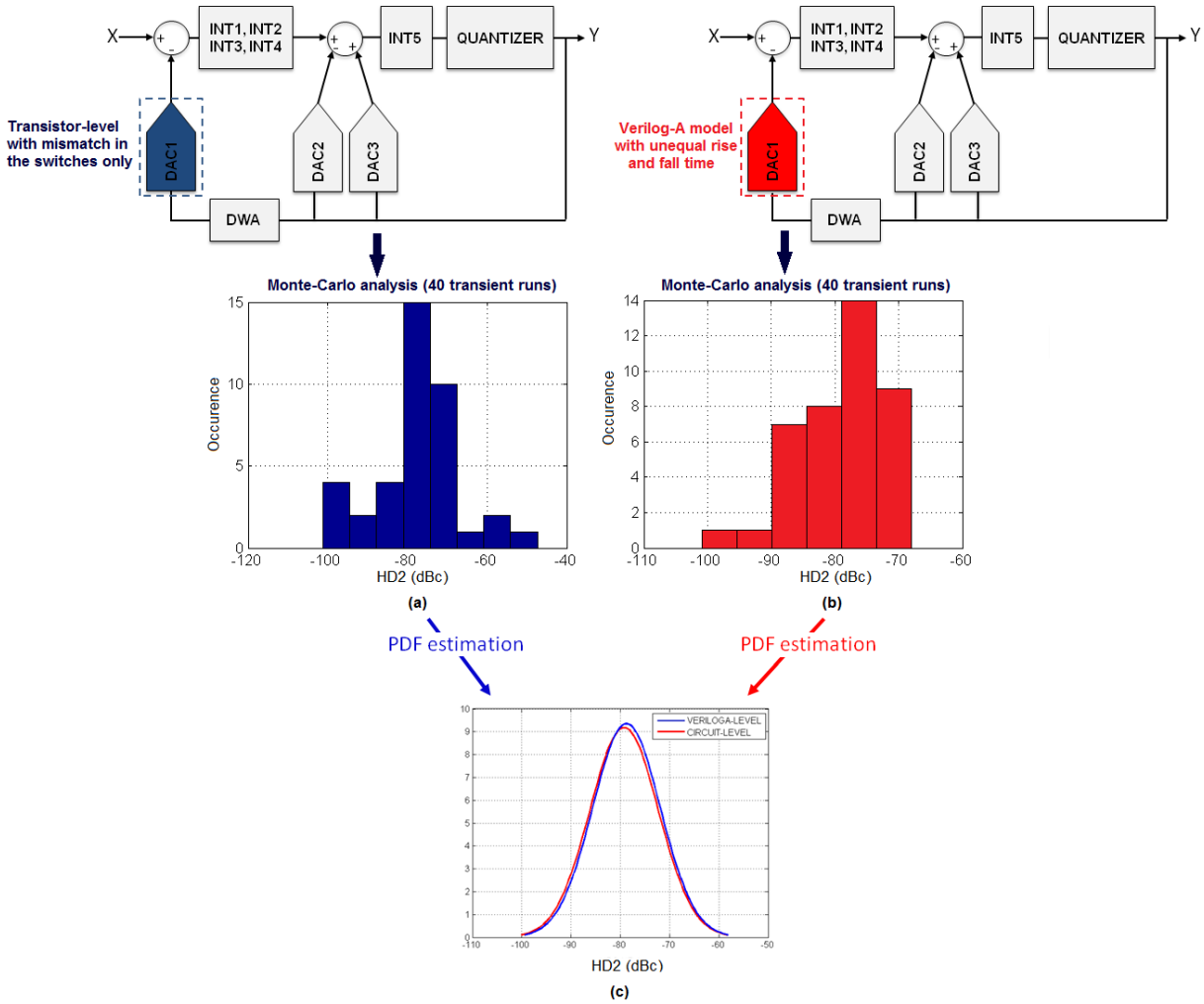


Figure 5-6. Histogram of the HD2 after a Monte-Carlo analysis (50 runs), (a) DAC in verilog A model, (b) DAC at transistor level, (c) estimation of the PDF of both histogram using the histfit function [6] of MATLAB.

The probability density functions of the HD2 obtained with the histfit function of Matlab [6] match very well. It should be noted that the simulation time in the case of Figure 5-6(a) is around 2 weeks (for 40 runs) while it is a few hours when using the verilog-A model.

5.3.2 Proposed corrections

To reduce the ISI, the size of the switch and their drivers may be increased but this will increase the parasitic capacitances at the virtual ground of the first integrator. Others alternatives are to choose a RZ DAC [5] at the cost of increased sensitivity to clock jitter, or to implement a DWA with reduced switching activity [3] at the cost of less efficient correction of mismatch induced noise and distortion.
A shaping algorithm that mitigates ISI issue was been proposed in [7] but it is limited to audio applications.

5.3.3 Input common-mode in the modulator front-end

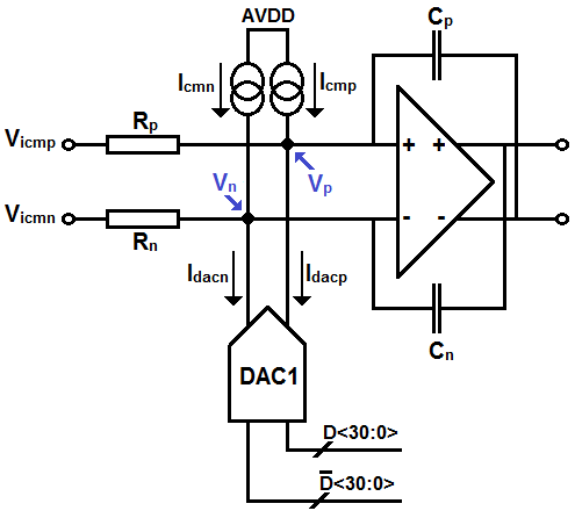


Figure 5-7. Common mode voltage in the ΔΣ modulator front-end.

We have demonstrated in appendix F that due to components mismatch in the front-end, the common mode at the virtual ground of the main opamp can be approximated within the signal bandwidth by the relation (5-1):

$$\frac{V_p + V_n}{2} = \left[\frac{V_{icmp} + V_{icmn}}{2} + RI_{cm} - \frac{(2^N - 1)}{2} \times RI_{unit}\right] + \frac{1}{2} \times \left[R \times \delta I_{cmp} + \delta R_p \times I_{cm} + \delta R_p \times \delta I_{cmp} + R \times \delta I_{cmn} + \delta R_n \times I_{cm} + \delta R_n \times \delta I_{cmn}\right] - \frac{1}{2} \times \left[\delta R_p \times \sum_{k=1}^{2^N-1}[(I_{unit} + \delta I_k) \times D_k] + \delta R_n \times \sum_{k=1}^{2^N-1}[(I_{unit} + \delta I_k) \times (1 - D_k)]\right] \quad (5\text{-}1)$$

V_{icmp}, V_{icmn} : dc voltage on the p (n) input node
R_p, R_n : input resistor of the p (n) path
C_p, C_n : integrating capacitance of the p (n) path
I_{cmp}, I_{cmn} : dc current of the p (n) top source
I_{dacp}, I_{dacn} : output current at the p (n) terminals of the DAC
δR_p, δR_n : resistor error of the p (n) path
δI_{cmp}, δI_{cmn} : dc current error of the p (n) top source
δI_k : mismatch error of the k^{th} current source
I_{unit} : unit current (LSB) of DAC
R : nominal value of the input resistor

Equation 5-1 is the sum of three expressions. The first term is the ideal common mode that would be obtained without mismatch. The second term is a static error and does not introduce distortion. However, it should be noted that this bias-offset affects the biasing of the input-transistors pair.
The last term is a dynamic error which is signal-dependent. This error term can be minimized by reducing the mismatch between the two input resistors of the integrator. This solution increases area and capacitance at the virtual ground of the integrator. Alternative techniques using common-mode feedback circuits to regulate the common-mode in the modulator front-end have been proposed in the literature [4]. Another approach may be to use a fully-differential DAC.

In this design the input resistors have large area to reduce their flicker noise contribution. As a result, the maximum mismatch between the two input resistors is insignificant and the common mode voltage swing at the virtual ground of the opamp is negligible.

5.3.4 Power supply modulation

As shown in Figure 5-8(a), due to the inductance of the bonding wire that connects the package of the pin to the pad of the core, the effective supply voltage of the DAC DATA buffers is modulated by the sequence coming from the quantizer output. It results in a pulse width modulation of the sequence at the DAC input as shown in Figure 5-8(b), which creates harmonic distortion. This phenomenon can be seen signal-dependent jitter.

To reduce this effect, several I/O pad can be put in parallel to reduce the value of the inductance at the cost of increasing the size of the package as additional pin are required. Another alternative is to use on-chip decoupling capacitor to reduce the voltage swing on the supply, at the cost of increased silicon area. However, using capacitors with high density such as MOS cap is a good compromise between cost and performance. The simulation result of Figure 5-8(c) shows the difference when no decoupling capacitance is used and when a 100pF MOS capacitor is connected between the supply pin and the ground pin of the circuit. In the first case, the linearity is decreased by 13dB and the THD value is limited by the second-order harmonic distortion the most.
It should be noted that in our prototype, none on-chip decoupling capacitance was used.

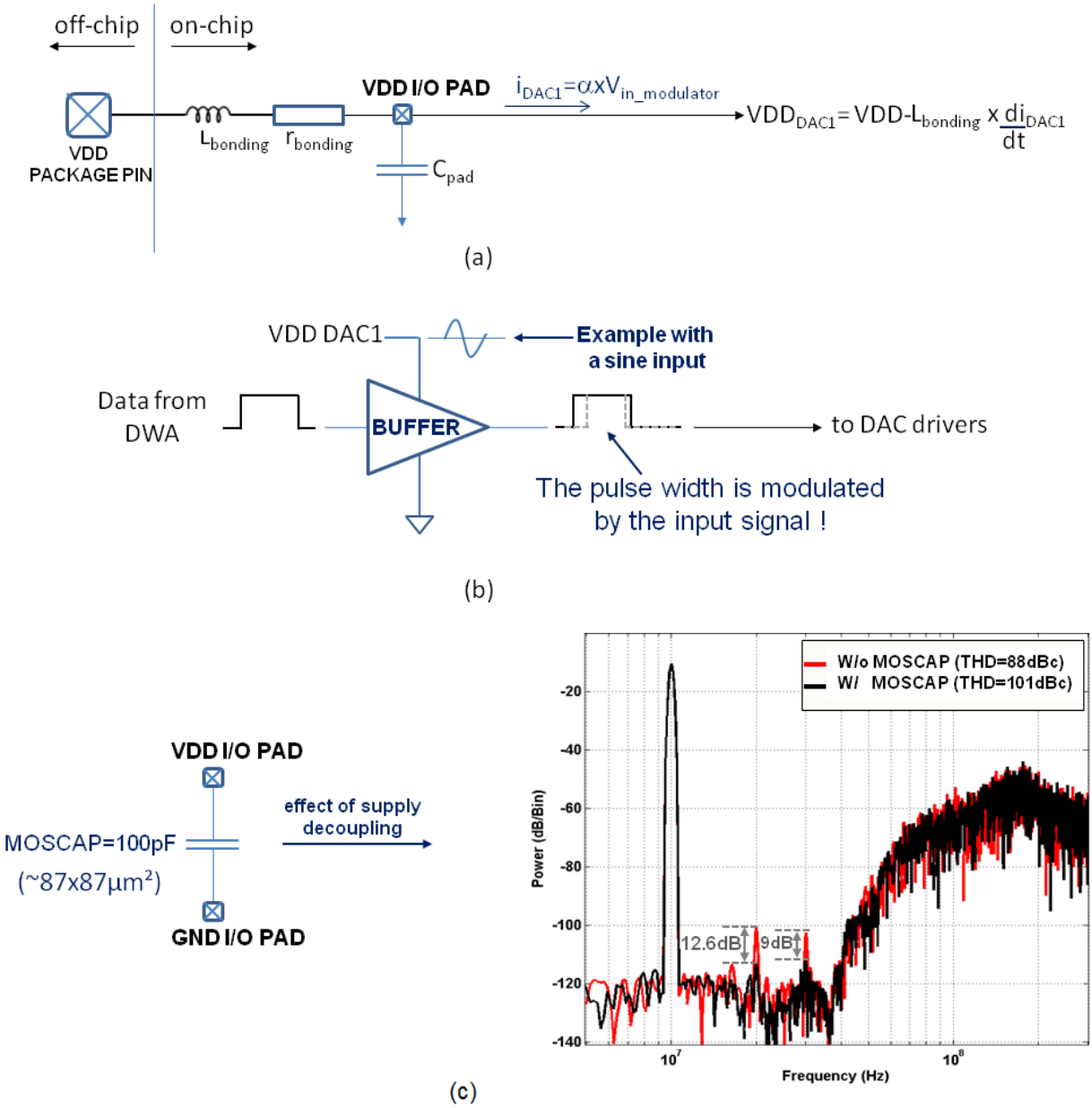


Figure 5-8. (a) Schematic of the voltage supply I/O with the parasitic of the package, (b) modulation mechanism of the DAC pulse by the voltage supply, (c) Spectre simulation ($L_{bonding}$=1.5nH, $r_{bonding}$=0.5Ω).

5.4 Measured dynamic performance

5.4.1 Single-tone test

The results shown in this section are obtained from the best measured sample.
Figure 5-9(a) shows the PSD of the ΔΣ modulator output for a -2.5dBFS input whose frequency is 6MHz. The measured peak SNR and peak THD are 69.4dBc and 76.5dBc respectively which results in 11-bit ENOB in 40MHz bandwidth. The power consumption of the ΔΣ modulator is 87.3mW, resulting in a Walden FoM of 533fJ/conversion-step. The measured dynamic range (71.4dB) is shown in Figure 5-9(b).The measured PSRR with a 40MHz, 60mV$_{pp}$ sinusoidal signal added upon the 1.2V analog voltage supply, is 54dB.

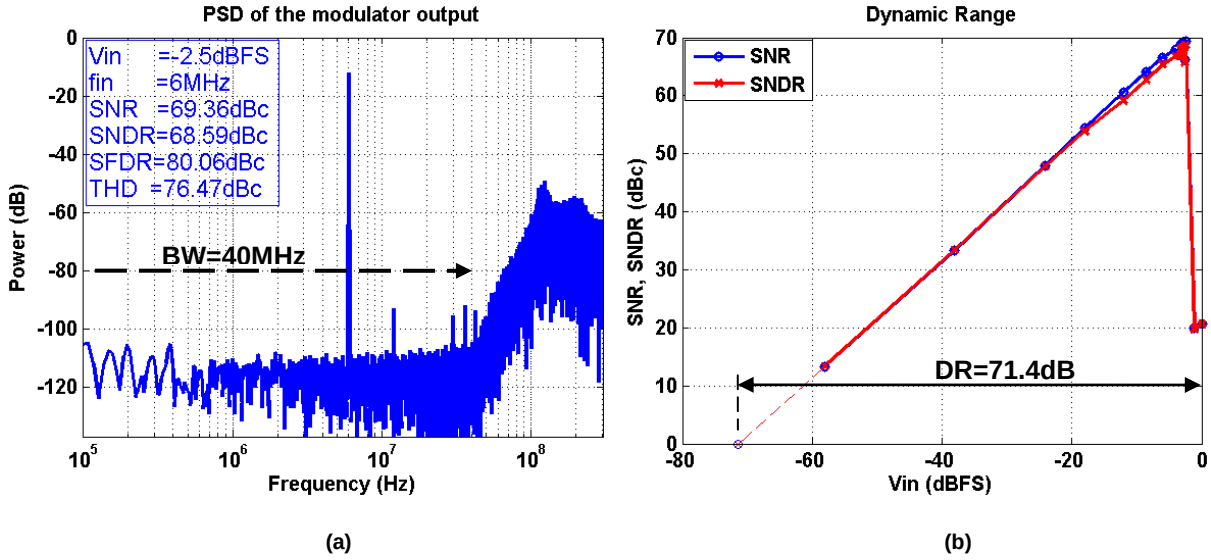


Figure 5-9. (a) Power Spectral Density of the ΔΣ modulator 5-bit output, (b) Measured SNR and SNDR as a function of the input signal level (f_{input}=6MHz).

5.4.2 Two-tone test

The inter-modulation products are measured by injecting at the input of the modulator two sinusoidal signals of equal amplitude (-8.5dBFS) and whose frequency are respectively 10MHz (f_{TONE1}) and 11MHz (f_{TONE2}). The worst-case IM2 and IM3 are located at $f_{IM2}=f_{TONE1}+f_{TONE2}$ and $f_{IM3}=2xf_{TONE1}-f_{TONE2}$ and their value is shown in Figure 5-10.

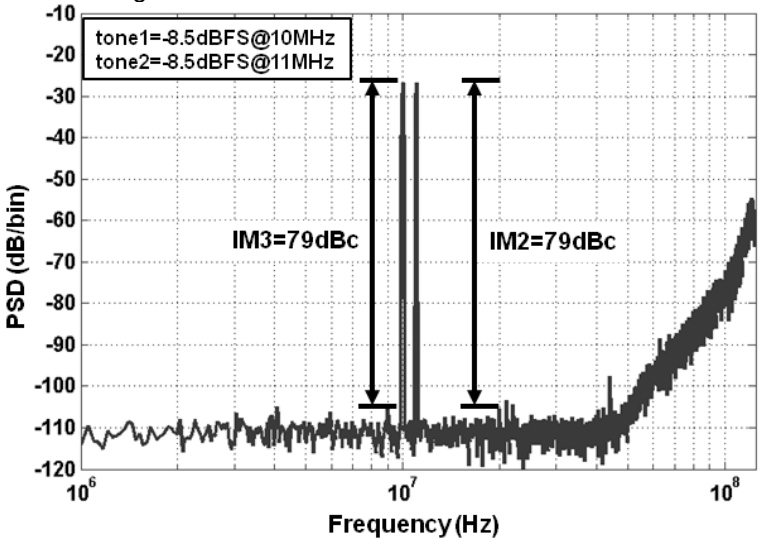


Figure 5-10. Two-tone test for Inter-modulation product measurement.

5.4.3 Alias rejection

As the signal bandwidth and the sampling frequency of the ΔΣ modulator are 40MHz and 640MHz respectively, any component (noise or interferer) present in the frequency range from 600MHz to 640MHz may fall back within the band of interest during the sampling process. The intrinsic alias rejection was measured with a sinusoidal input signal and whose frequency was swept from 600MHz up to 639MHz. For each frequency, the ratio of the output power to the input power is computed. The results are shown in Figure 5-11. As predicted by behavioral simulations shown in Chapter 2 (Figure 2-17(b)), the loop filter of the modulator provides alias rejection that is equivalent to a 3rd-order Butterworth filter.

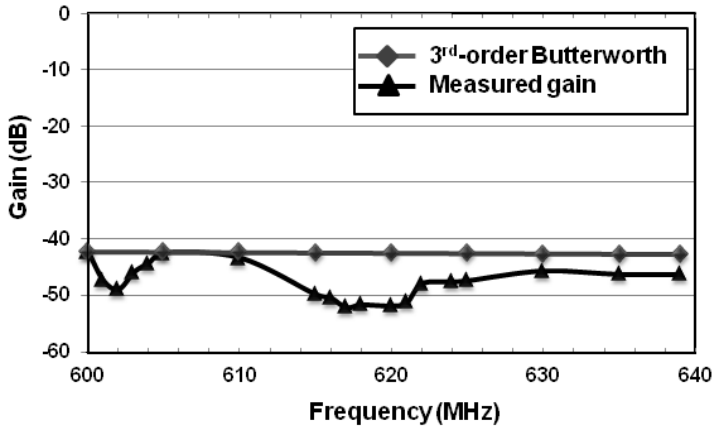


Figure 5-11. Anti-aliasing transfer function measurement and comparison to the attenuation provided by a 3rd-order Butterworth filter.

5.5 Performance summary and comparison with the state of the art

The performance of our CT ΔΣ modulator prototype is summarized in Table 5.1. The Figure of merit (FoM) is defined as:

$$FoM_{Walden} = P_{ower}/(2\times BW\times 2^{ENOB}) \quad (4\text{-}2)$$

The power efficiency (Walden FoM), the THD and the ENOB are compared against the state of the art in Figure 5-12, Figure 5-13 and Figure 5-14 respectively.

Table 5-1. performance summary of the ΔΣ modulator

PARAMETERS	VALUE	UNIT
Bandwidth	40	MHz
Modulator output rate	640	MSPS
Input range	1.6	$V_{pp,diff}$
Peak SNR*	69.4	dBc
Peak THD*	76.5	dBc
Peak SNDR*	68.6	dBc
Peak SFDR*	80	dBc
ENOB*	11	bit
Dynamic Range*	71.4	dBc
IM2@$_{fin1=10MHz,fin2=11MHz}$	79	dBc
IM3@ $_{fin1=10MHz,fin2=11MHz}$	79	dBc
PSRR@40MHz	51	dB
Alias rejection@600MHz	42.4	dB
Power consumption	87.3	mW
FoM_{Walden}	533	fJ/conv-step

***Measured with a 6MHz input sine tone**

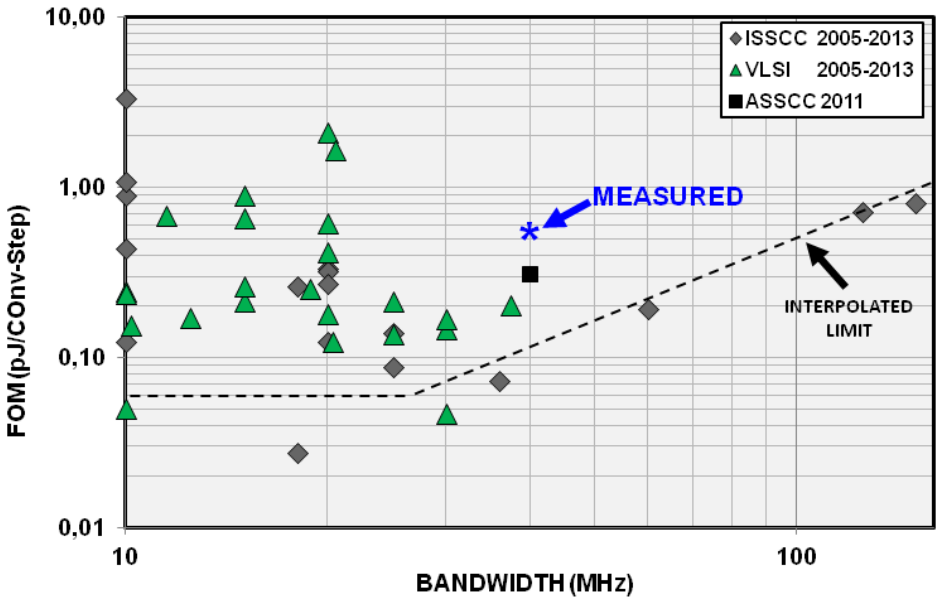


Figure 5-12. Comparison of the FoM to the state of the art.

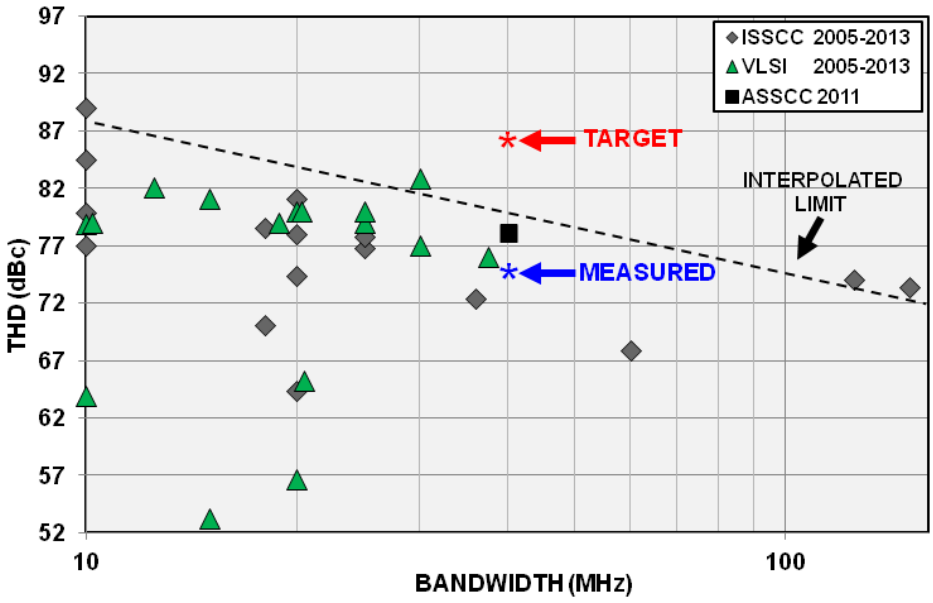


Figure 5-13. Comparison of the measured THD to the state of the art.

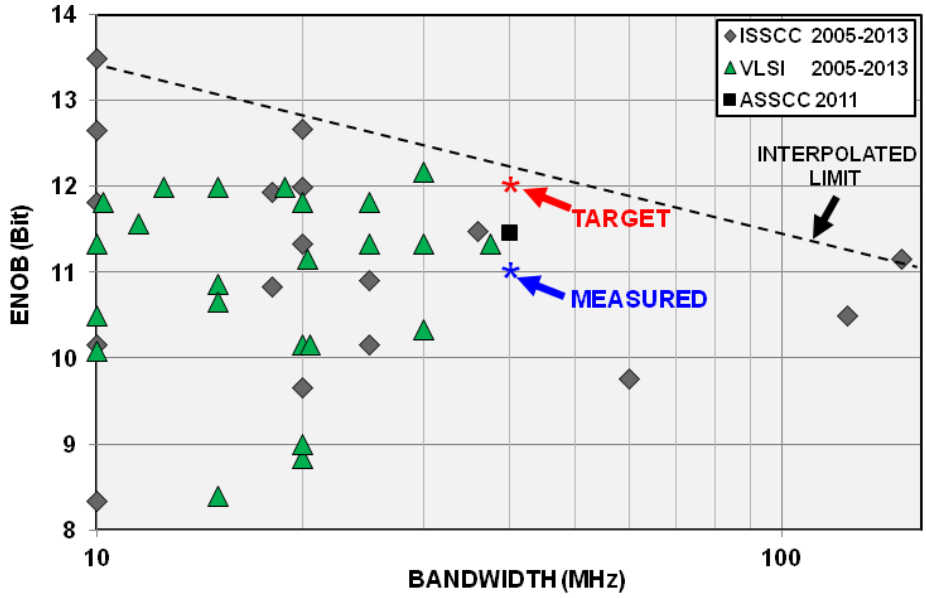


Figure 5-24. Comparison of the measured ENOB to the state of the art.

5.6 Summary

In this chapter we have presented the test setup used to evaluate the performance of the ΔΣ modulator. Directions were given to measure the performance of the modulator without being limited by the test setup itself. The first measurement results showed that our IC prototype is functional but the performance was less than expected. The results were analyzed in depth and the ISI combined to the DWA was found to be the main reason of the performance degradation. Concrete solutions were proposed to solve the problem. Also, others source of performance degradation were pointed out.

The characterization results showed that the prototype achieves 11-bit ENOB and 12-bit THD in a signal bandwidth of 40MHz while consuming 87.3mW, which leads to a figure of merit of 533fJ/conversion-step. This value is higher than our original goal but still comparable to commercial pipeline solutions available on the market. On the other hand, the measurement of the anti-aliasing transfer function of the modulator shows that the provided attenuation of the loop filter is equivalent to what would be obtained with a 3rd order Butterworth filter in front of the ΔΣ ADC. This advantage combined with the resistive input impedance of the modulator greatly simplifies the circuit design of the front ΔΣ ADC front-end.

It should be noted that the measured performance was obtained without correction of the mismatch-induced errors in the main DAC (DWA was turned-off). Choosing the appropriate correction method should give a performance close to our initial specifications.

5.7 References

[1] http://cmp.imag.fr/

[2] Hans Tuinhout, et al., “Effects of Metal Coverage on MOSFET Matching,” International Electron Devices Meeting, December 1996.

[3] Tao Shui, Richard Schreier, “Mismatch Shaping for a Current-Mode Multibit Delta-Sigma DAC”, J. Solid State Circuits, vol. 34, NO. 3, pp.331-338, March 1999.

[4] Khiem Nguyen, Robert Adams, Karl Sweetland, Huaijin Chen, “A 106-dB SNR Hybrid Oversampling Analog-to-Digital Converter for Digital Audio”, J. Solid State Circuits, vol. 40, pp.2408-2415, December 2005.

[5] James A. Cherry, W. Martin Snelgrove, “Continuous-time delta-sigma modulators for high-speed A/D conversion, Theory, Practice and Fundamental Performance Limits”, Kluwer Academic Publisher, 1999.

[6] http://www.mathworks.fr/

[7] Lars Risbo, Rahmi Hezar, Burak Kelleci, Halil Kiper, Mounir Fares, “A 108dB-DR 120dB-THD and 0.5Vrms Output Audio DAC with Inter-Symbol-Interference-Shaping Algorithm in 45nm CMOS”, J. Solid State Circuits, vol. 40, pp.2408-2415, February 2011.

Chapter 6

Conclusion

6.1 Conclusion

We have shown the feasibility of a CT ΔΣ modulator with 40MHz of signal bandwidth in 65nm CMOS. The fabricated prototype is part of an IC that includes a digital decimation filter, a voltage reference and high-speed CML buffers. All the calibration circuits needed to compensate for the imperfections of the analog components are embedded on-chip.

After a deep analysis of published wideband ΔΣ modulators the last ten years, we have purposed an architecture that is able to fulfill the specifications of a wide range of applications. The circuit is built around a 5^{th}-order loop filter and a 5-bit quantizer clocked with an OSR of 8 only.
The system-level modeling and simulation of our modulator was detailed. The main imperfections of the building blocks were modeled and simulated to quickly predict the performance degradation and derive the specifications of each sub-blocks of the modulator.
The circuit-level implementation of the loop filter, the quantizer and the feedback DACs were detailed and design guidelines were given to implement a robust circuit while minimizing the power consumption.

Measurement results have shown a performance of 11-bit ENOB and 12-bit THD within 40MHz of signal bandwidth. It must be noted that these dynamic parameters were measured without calibration of the main DAC. The ΔΣ modulator consumes 87.3mW which gives a FoM of 533fJ/conversion-step. This value is in line with the wideband discrete ΔΣ ADC IC of the market [1][2]. The measurement of the anti-aliasing transfer function has shown that the built-in loop filter provides as much attenuation as a 3^{rd} order Butterworth filter placed in front of the ADC. This feature, together with the high input resistive impedance of the modulator (1KΩ) simplify greatly the design of the ADC front-end. This chip may be an alternative to pipeline architecture for applications that require baseband digitization with low noise, low distortion and low power consumption such as medical imaging, wireless and wireline communications, video or instrumentation.

While the targeted dynamic performances were not reached, the choice of the DWA as the correction algorithm in presence of ISI in the main DAC was clearly identified as the limiting factor. Behavioral simulations that take into account the interaction of the ISI with the DWA have proven to be responsible of the gap between the simulated performances and the measurement results. A correction method such as one of those proposed in chapter 5 may improve the performance significantly.

The next chapter concludes with an overview of accomplishments. In addition, we purpose directions to improve the power efficiency and the signal transfer function of our IC prototype. Finally we highlight the future challenges that ΔΣ modulators designers will face.

6.2 Further improvements

6.2.1 Power consumption

As shown in Figure 6-1, the five integrators consume 81% of the overall power consumption of the modulator. The power consumption of the loop filter could be scaled by using Gm-C integrators after the main opamp-RC integrator [3]. As the proposed architecture benefits of very low swing inside the loop filter, using gm-C integrators would greatly improve the power efficiency without affecting so much the overall linearity.
By scaling the power of the subsequent stages of the loop filter, the power consumption of the first integrator would become dominant because it consumes itself one third of the power approximately. The output stage of the main opamp (opamp1) consumes 40% of the power consumption of the integrator. Using a class AB output stage as in [4] may improve the power efficiency (at the cost of linearity).
The second block that contributes mostly to the overall power consumption of the modulator is the quantizer. A highly digital quantizer as presented in [5] could improve the power efficiency compared to a regular FLASH ADC. Furthermore, the reduced number of comparators and the digital implementation of the excess-loop delay compensation could reduce the die area significantly. As an extra DAC is avoided, the capacitance at the virtual ground of the last opamp is reduced which translate to further reduction of power.

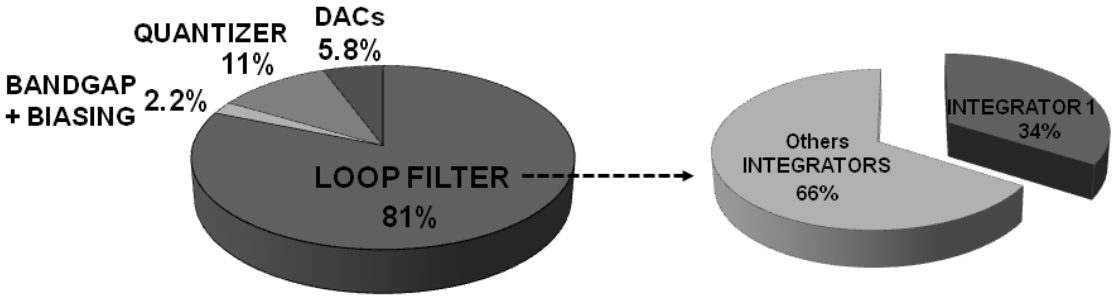


Figure 6-1. Breakdown of the power consumption among the main blocks of the ΔΣ modulator and details of the power consumption inside the loop filter.

6.2.2 STF peaking

Regarding the mitigation of the STF peaking, many solutions were proposed in the literature as expressed in Chapter 2. Recently, an attractive solution which consists in embedding a filter within the loop filter of the modulator was introduced in [6] and detailed in [7]. This technique is shown in Figure 6-2 with a second-order filter as in [6] but it is extensible to higher order filters. As the filter is located after the first stage of the loop filter its noise and distortion are attenuated by the gain of the main integrator which results in a power and area efficient implementation of a ΔΣ modulator with a robust, peaking-free STF.

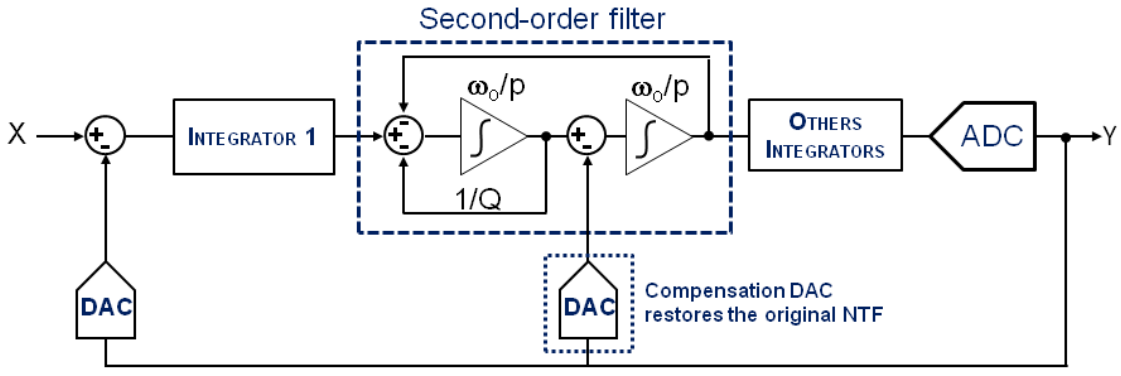


Figure 6-2. Concept of embedding a filter inside the loop filter of a CT ΔΣ modulator [6].

6.3 Challenges

6.3.1 Signal Bandwidth

The time evolution of the signal bandwidth in CMOS LP ΔΣ modulator is shown in Figure 6-3. The first remark is its exponential growth, just like the scaling of MOS transistors dictated by Moore's law. This trend may continue for a few years as the Fully-Depleted (FD) SOI and FINFET technologies allow to maintain the shrink of the MOS transistors. However, for economical consideration, the probability to implement a general purpose ADC IC in these advanced processes is very low. Only ADCs embedded in Application Specific Integrated Circuits (ASICs) that target mass market may benefit of this technological evolution.

CMOS discrete ADC ICs are mainly implemented in 130nm or 180nm process which complicates the implementation of ΔΣ modulators with a clock frequency of several GHz as in [9][10]. For the moment, ΔΣ modulators implemented in commercial products [1][2] have a maximum clock frequency of 640MHz.

The loop-delay is a key challenge to overcome when designing a high-speed CT ΔΣ modulator. Architectural innovations are the only solutions. For example, in [11] authors have proposed a technique to compensate for more than one clock delay which allowed to implement a CT ΔΣ modulator clocked at 800MHz in 180nm CMOS.

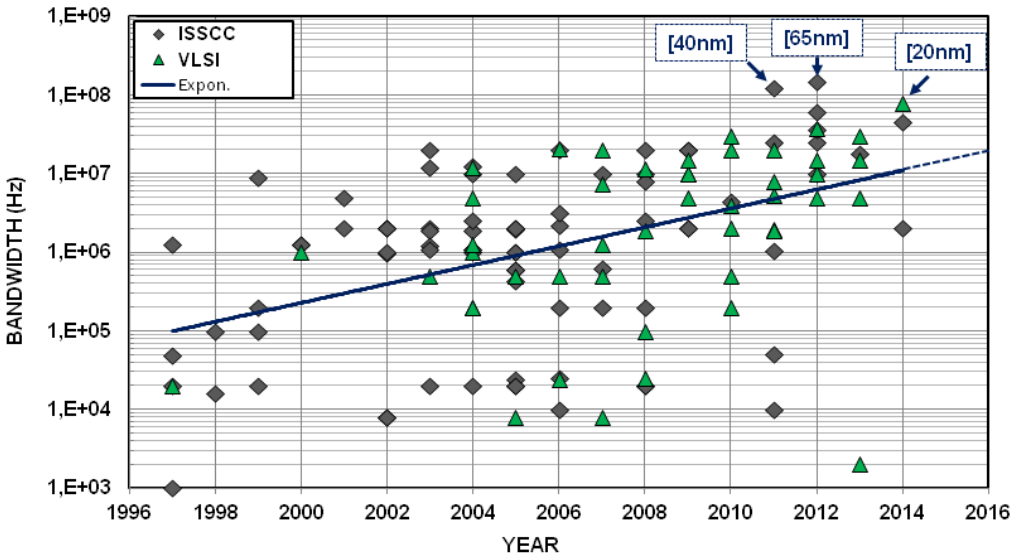


Figure 6-3. Signal bandwidth evolution of low-pass CMOS ΔΣ modulator between 1997 and 2014 [8].

6.3.2 Power efficiency

The evolution of state-of-the-art FoM over time is shown in Figure 6-4. This amazing race toward power saving is mostly driven by ASICs that target mobile application in mass market such as cellular handset.
Regarding general-purpose ADC ICs, the power consumption of I/Os may become more critical than the power consumption of the core. In general, for these non-specific ICs, the performance is privileged over the power consumption. However, designing a low-power I/Os interface may be an interesting research topic in the future.

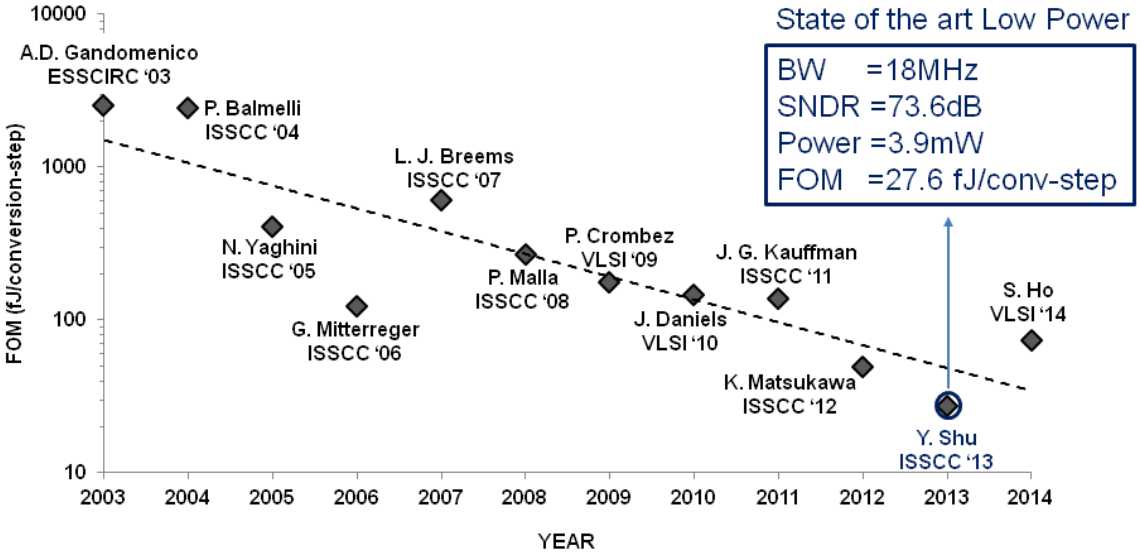


Figure 6-4. Evolution of state-of-the art FoM from 2003 to 2014.

6.3.3 Linearity

Regarding performance, the linearity is limited below 14-bit for signal bandwidth higher than 10MHz as illustrated in Figure 6-5. The design of new corrections techniques to compensate for the mismatch between the unitary cells of the main DAC and ISI in wideband ΔΣ modulators are a subject of future. Implementing a DAC with high output impedance in high-speed applications is also a great challenge to overcome.

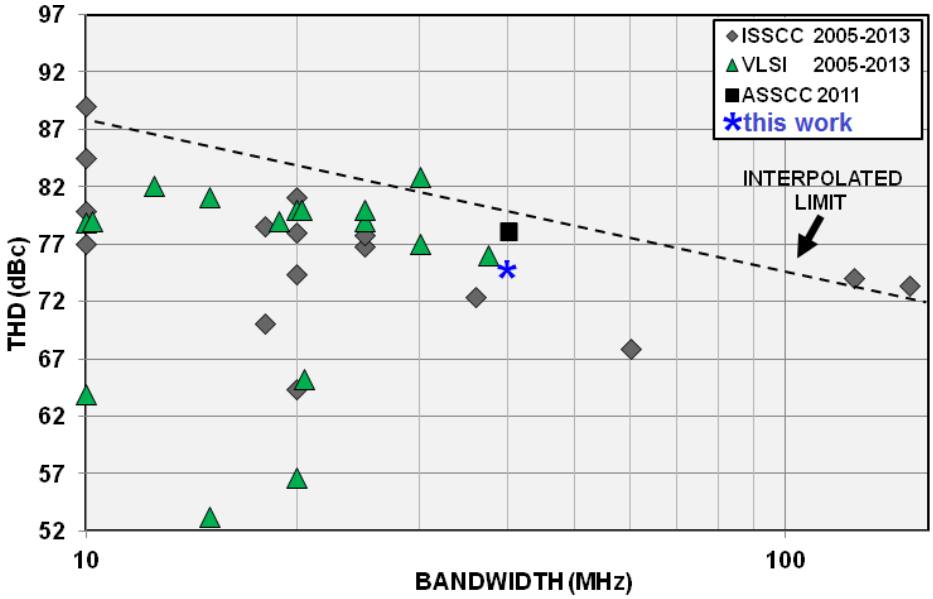


Figure 6-5. State-of-the-art THD as a function of the signal bandwidth of wideband low-pass CMOS ΔΣ modulators.

6.4 References

[1] http://www.ti.com/lit/ds/symlink/adc12eu050.pdf

[2] http://www.analog.com/

[3] Robert van Veldhoven, “A Tri-Mode Continuous-Time ΣΔ Modulator with Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver,” ISSCC Dig. Tech. Papers, pp. 478–480, February 2014.

[4] G. Mitteregger, et al., “A 14 b 20 mW 640 MHz CMOS CT ΔΣ ADC with 20MHz signal bandwidth and 12b ENOB,” IEEE J. of Solid-State Circuits, VOL. 44, NO. 12, December 2006.

[5] Y. SHu et al., “A 28fJ/conv-step CT ΔΣ Modulator with 78dB DR and18MHz BW in 28nm CMOS Using a Highly Digital Multibit Quantizer,” ISSCC Dig. Tech. Papers, pp. 268–270, February 2013.

[6] Radha Rajan, Shanthi Pavan, “A 5mW CT ΔΣ ADC with Embedded 2nd-Order Active Filter and VGA Achieving 82dB DR in 2MHz BW,” ISSCC Dig. Tech. Papers, pp. 478–480, February 2014.

[7] Radha S. Rajan and Shanthi Pavan, “Design Techniques for Continuous-Time ΔΣ Modulators With Embedded Active Filtering,” IEEE J. of Solid-State Circuits, VOL. 49, NO. 10, October 2014.

[8] B. Murmann, "ADC Performance Survey 1997-2014," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

[9] Muhammed Bolatkale et al., “A 4GHz CT ΔΣ ADC with 70dB DR and –74dBFS THD in 125MHz BW,” ISSCC Dig. Tech. Papers, pp. 470-472, February 2011.

[10] Hajime Shibata et. al., “A DC-to-1GHz Tunable RF ΔΣ ADC Achieving DR = 74dB and BW = 150MHz at f_0 = 450MHz Using 550mW,” ISSCC Dig. Tech. Papers, pp. 151–153, February. 2012.

[11] Vikas Singh et al., “A 16MHz BW 75dB DR CT ΔΣ ADC Compensated for More Than One Cycle Excess Loop Delay,” IEEE CICC Dig. Tech. Papers, September 2011.

Appendix A

opamp-rc resonator transfer function

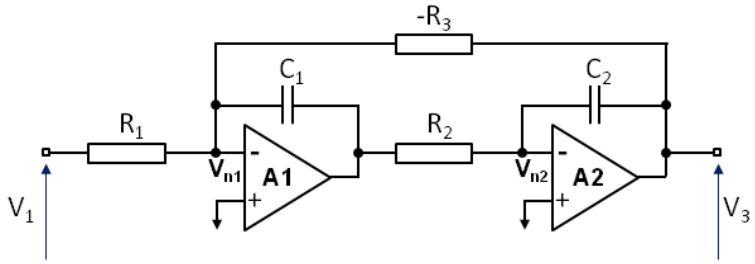


Figure A-1. Schematic of an opamp-rc resonator with finite dc gain in the opamps.

$$(V_1 - V_{n1}) \times g_1 - (V_3 - V_{n1}) \times g_3 = (V_{n1} - V_2) \times C_1 p \quad \text{(A-1)}$$

$$(V_2 - V_{n2}) \times g_2 = (V_{n2} - V_3) \times C_2 p \quad \text{(A-2)}$$

$$V_2 = A_1 \times (V_{p1} - V_{n1}) = -A_1 \times V_{n1} \quad \text{(A-3)}$$

$$V_3 = A_2 \times (V_{p2} - V_{n2}) = -A_2 \times V_{n2} \quad \text{(A-4)}$$

From equations (A-1), (A-2), (A-3) and (A-4):

$$g_1 \times V_1 = g_3 \times V_3 - \left[\frac{(g_1 - g_3 + C_1 p)}{A_1} + C_1 p\right] \times V_2 \quad \text{(A-5)}$$

$$V_2 = -\frac{1}{g_2} \times \left[\frac{(g_2 + C_2 p)}{A_2} + C_2 p\right] \times V_3 \quad \text{(A-6)}$$

By replacing V_2 by the expression of equation (A-4), we find a relation between V_3 and V_1:

$$g_1 \times V_1 = g_3 \times V_3 + \left[\frac{g_1 - g_3 + (A_1+1) \times C_1 p}{A_1}\right] \times \frac{1}{g_2} \times \left[\frac{g_2 + (A_2+1) \times C_2 p}{A_2}\right] \times V_3 \quad \text{(A-7)}$$

$$g_1 \times V_1 = g_3 \times V_3 + g_3 \times \left[\frac{\frac{g_1}{g_3} - 1 + (A_1+1) \times R_3 C_1 p}{A_1}\right] \times \left[\frac{1 + (A_2+1) \times R_2 C_2 p}{A_2}\right] \times V_3 \quad \text{(A-8)}$$

Assuming (A-7) and if equation (A-8) is satisfied then the transfer function of the resonator may be approximated by equation (A-9):

$$b = \frac{g_1}{g_3} \quad \text{(A-9)}$$

$$A_1 A_2 \gg (b - 1) \quad \text{(A-10)}$$

$$H_R = \frac{b}{\frac{b \times (A_1+1) \times (A_2+1)}{A_1 A_2 \omega_{ug1} \omega_{ug2}} p^2 + \left[\frac{(b-1) \times (A_2+1)}{A_1 A_2 \omega_{ug2}} + \frac{b \times (A_1+1)}{A_1 A_2 \omega_{ug1}}\right] p + 1} \quad \text{(A-11)}$$

Where:

$$\omega_{ug1} = \frac{1}{R_1 C_1} \quad \text{(A-12)}$$

$$\omega_{ug2} = \frac{1}{R_2 C_2} \quad \text{(A-13)}$$

Equation (A-9) can be written under the canonical form of equation (A-12)

$$H_R = \frac{b}{\frac{1}{\omega_o^2} p^2 + \frac{1}{\omega_o \times Q} p + 1} \quad \text{(A-14)}$$

Where:

$$\omega_o^2 = \frac{A_1 A_2 \omega_{ug1} \omega_{ug2}}{b \times (A_1+1) \times (A_2+1)} \quad \text{(A-15)}$$

$$Q = \frac{1}{\omega_o} \times \frac{1}{\frac{(b-1)\times(A_2+1)}{A_1 A_2 \omega_{ug2}} + \frac{b \times (A_1+1)}{A_1 A_2 \omega_{ug1}}} \quad \text{(A-16)}$$

Appendix B

opamp-rc integrator transfer function

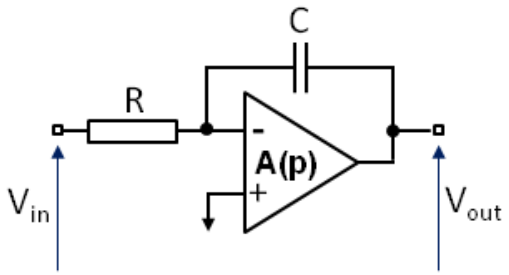


Figure B-1. Schematic of an opamp-rc integrator.

$$(V_{in} - V_n) \times g = (V_n - V_{out}) \times Cp \quad \text{(B-1)}$$

$$V_{out} = A(p) \times (V_p - V_n) = -A(p) \times V_n \quad \text{(B-2)}$$

$$g \times V_{in} = (g + Cp) \times V_n - Cp \times V_{out} \quad \text{(B-3)}$$

$$g \times V_{in} = -\left[\frac{g+Cp}{A(p)} + Cp\right] \times V_{out} \quad \text{(B-4)}$$

$$g \times V_{in} = -\left[\frac{g+Cp}{\frac{A_o}{\frac{1}{\omega_o}p+1}} + Cp\right] \times V_{out} \quad \text{(B-5)}$$

$$g \times V_{in} = -\left[\frac{(g+Cp)\times\left(\frac{1}{\omega_o}p+1\right)+A_o\times Cp}{A_o}\right] \times V_{out} \quad \text{(B-6)}$$

$$\frac{V_{out}}{V_{in}} = -\frac{A_o\times g}{(g+Cp)\times\left(\frac{1}{\omega_o}p+1\right)+A_o\times Cp} \quad \text{(B-7)}$$

$$\frac{V_{out}}{V_{in}} = -\frac{A_o}{(1+RCp)\times\left(\frac{1}{\omega_o}p+1\right)+A_o\times RCp} \quad \text{(B-8)}$$

$$\frac{V_{out}}{V_{in}} = -\frac{A_o}{\frac{RC}{\omega_o}p^2+\left[\frac{1}{\omega_o}+\frac{(A_o+1)}{\omega_{ug}}\right]p+1} \quad \text{(B-9)}$$

Where ω_{ug} is the unit gain frequency of the integrator and is expressed by equation (B-12):

$$\omega_{ug} = \frac{1}{RC} \quad \text{(B-10)}$$

Assuming A_o>>1 and expressing the -3dB bandwidth of the opamp as a function of the GBW and the DC gain, then we can rewrite equation (B-9) into equation (B-10):

$$\frac{V_{out}}{V_{in}} = -\frac{A_o}{\frac{1}{\omega_{ug}\times\omega_o}p^2+A_o\times\left(\frac{1}{GBW}+\frac{1}{\omega_{ug}}\right)p+1} \quad \text{(B-11)}$$

Assuming GBW>>ω_{ug} we deduce from equation (B-10) the expressions of the two poles of the transfer function:

$$\omega_{p1} \approx \frac{\omega_{ug}}{A_o} \quad \text{(B-12)}$$

$$\omega_{p2} \approx GBW \quad \text{(B-13)}$$

$$\frac{V_{out}}{V_{in}} = -\frac{A_o}{\left(\frac{A_o}{\omega_{ug}}p+1\right)\times\left(\frac{1}{GBW}p+1\right)} \quad \text{(B-14)}$$

If the DC gain is infinite the equation (B-10) may be rewritten to see the influence of the finite GBW only:

$$\frac{V_{out}}{V_{in}} = -\frac{A_o}{\frac{A_o}{\omega_{ug} \times GBW} p^2 + A_o \times \left(\frac{1}{GBW} + \frac{1}{\omega_{ug}}\right) p + 1} \quad \text{(B-15)}$$

$$\frac{V_{out}}{V_{in}} = -\frac{1}{\frac{1}{\omega_{ug} \times GBW} p^2 + \left(\frac{1}{GBW} + \frac{1}{\omega_{ug}}\right) p} \quad \text{(B-16)}$$

$$\frac{V_{out}}{V_{in}} = -\frac{\omega_{ug}}{p} \times \frac{1}{\frac{1}{GBW} p + \left(\frac{\omega_{ug}}{GBW} + 1\right)} \quad \text{(B-17)}$$

$$\frac{V_{out}}{V_{in}} = -\frac{\omega_{ug}}{p} \times \frac{\frac{1}{\left(\frac{\omega_{ug}}{GBW} + 1\right)}}{\frac{1}{GBW} p + 1} \quad \text{(B-18)}$$

The transfer function is the ideal transfer function with a gain error given by equation (B-19) and an additive pole whose expression is given by equation (B-13).

$$\varepsilon_{error} = \frac{1}{\left(\frac{\omega_{ug}}{GBW} + 1\right)} \quad \text{(B-19)}$$

Appendix C

Harmonic distortion due to the non-linear input resistors

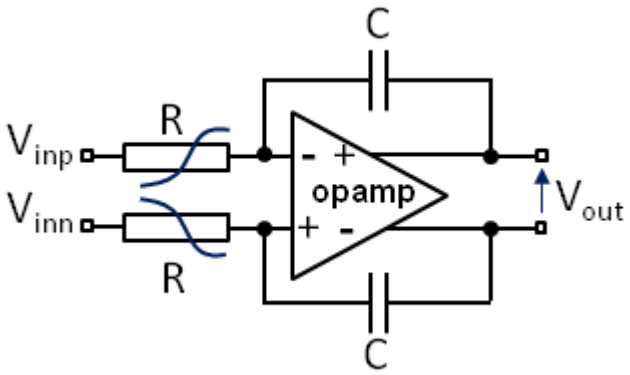


Figure C-1. Schematic of an opamp-rc integrator with non-linear resistors.

$$g_o = \frac{1}{R_o} \quad \text{(C-1)}$$

$$V_{in} = V_{inp} - V_{inn} \quad \text{(C-2)}$$

$$I_{inp} = \frac{V_{inp}}{\left(R_o + \frac{\Delta R}{2}\right) \times \left(1 + \alpha_{1R} V_{inp} + \alpha_{2R} V_{inp}^2\right)} \quad \text{(C-3)}$$

$$I_{inn} = \frac{V_{inn}}{\left(R_o - \frac{\Delta R}{2}\right) \times \left(1 + \alpha_{1R} V_{inn} + \alpha_{2R} V_{inn}^2\right)} \quad \text{(C-4)}$$

Using the Taylor series approximation, equations (1) and (2) can be written as :

$$I_{inp} \approx V_{inp} \times g_o \left(1 - \frac{\Delta R}{2R_o}\right) \times \left(1 - \alpha_{1R} V_{inp} - \alpha_{2R} V_{inp}^2\right) \quad \text{(C-5)}$$

$$I_{inn} \approx V_{inn} \times g_o \left(1 + \frac{\Delta R}{2R_o}\right) \times \left(1 - \alpha_{1R} V_{inn} - \alpha_{2R} V_{inn}^2\right) \quad \text{(C-6)}$$

The differential integrator input current is defined as:

$$I_{in} = I_{inp} - I_{inn} = g_o \times \left(V_{in} + \alpha_{1R} \frac{\Delta R}{R_o} \times \frac{V_{in}^2}{4} - \alpha_{2R} \frac{V_{in}^3}{4}\right) \quad \text{(C-7)}$$

For a sinusoid input of amplitude A and pulsation ω_o we have: $V_{in} = A\sin(\omega_o t)$ (C-8)

$$I_{in} = g_o \times \left[\frac{\alpha_{1R}}{8} \frac{\Delta R}{R_o} + \left(1 - \frac{3\alpha_{2R} A^2}{16}\right) \times A\sin(\omega_o t) - \frac{\alpha_{1R}}{8} \frac{\Delta R}{R_o} \times A^2 \sin(2\omega_o t) + \frac{\alpha_{2R}}{16} \times A^3 \sin(3\omega_o t)\right] \quad \text{(C-9)}$$

Based on equation (9) the second and third harmonic referred to the integrator input

$$HD_2 = \frac{\Delta R}{R_o} \times \frac{\alpha_{1R} A}{8 \times \left(1 - \frac{3\alpha_{2R} A^2}{16}\right)} \approx \frac{\Delta R}{R_o} \times \frac{\alpha_{1R} A}{8} \quad \text{(C-10)}$$

$$HD_3 = \frac{\alpha_{2R} A^2}{16 \times \left(1 - \frac{3\alpha_{2R} A^2}{16}\right)} \approx \frac{\alpha_{2R} A^2}{16} \quad \text{(C-11)}$$

Appendix D

Noise in the modulator front-end

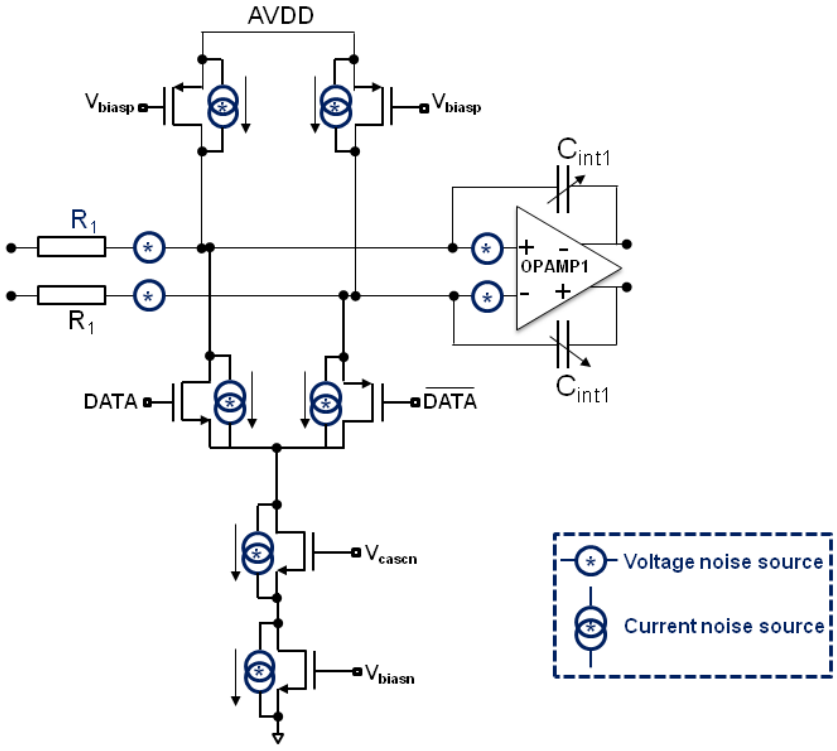


Figure D-1. Noise sources in the front-end of the ΔΣ modulator.

The noise PSD of the front-end referred to the input of the modulator is computed by making the following assumptions:

- The inverting/non-inverting input of the opamp are virtual grounds
- All the noise source are uncorrelated
- The main contributor to DAC noise is the bottom NMOS transistor. The noise contribution of the NMOS cascode transistor and the switching transistors can be neglected.
- The main contributor to the opamp noise is the input transistors pair

k : Boltzmann constant
T : absolute temperature
N : quantizer resolution
R_1 : input resistance of the main integrator
g_{m_bot} : transconductance of a unit current cell in DAC1
g_{m_top} : transconductance of the current cells that control the common-mode
g_{m_opamp} : transconductance of the input transistors of opamp1
I_{LSB} : LSB current of DAC1
I_{cm} : common-mode current
f : frequency
C_{ox} : Gate-oxide capacitance per unit area
KF_N, KF_p : flicker noise constant of the bottom and top current respectively
KF_{opamp} : flicker noise constant of the input transistors of opamp1
L_{top} : channel length of the top PMOS current sources
L_{bot} : channel length of the bottom NMOS current sources
L : channel length of the input transistors of opamp1

Resistors noise

$$\mathrm{PSD}_{R_1} = 8kTR_1 \tag{D-1}$$

Opamp1 noise

$$\mathrm{PSD}_{opamp1} = \left(\frac{8kT\gamma}{g_{m\_opamp}} + \frac{2KFI_1}{fC_{ox}L_1^2 g_{m\_opamp}^2}\right) \tag{D-2}$$

DAC noise

The noise PSD of the main DAC referred to the modulator input is given by equation D-3. The first part of the equation D-3 is related to the noise of the unitary current cells while the second part is the contribution of the top current sources that control the common-mode at the output of the DAC cells. The equation D-3 is rewritten into equation D-4 which separates the thermal noise term and the flicker noise term.

$$\mathrm{PSD}_{DAC1} = R_1^2 \times \left[(2^N - 1) \times \left(4kT\gamma g_{m\_bot} + \frac{KF_n I_{LSB}}{fC_{ox}L_u^2}\right)\right] + R_1^2 \times \left[2 \times \left(4kT\gamma g_{m\_top} + \frac{KF_p I_{cm}}{fC_{ox}L_{cm}^2}\right)\right] \tag{D-3}$$

$$\mathrm{PSD}_{DAC1} = R_1^2 \times \left[(2^N - 1) \times \left(4kT\gamma g_{m\_bot}\right) + 8kT\gamma g_{m\_top}\right] + R_1^2 \times \left[(2^N - 1) \times \frac{KF_n I_{LSB}}{fC_{ox}L_{bot}^2} + \frac{2KF_p I_{cm}}{fC_{ox}L_{top}^2}\right] \tag{D-4}$$

To reduce noise and improve matching, the current cells of the common mode source and the DAC are biased in strong inversion which allows writing equation (D-5), (D-6) and (D-7).

$$g_{m\_bot} = \frac{2I_u}{V_{gt\_dac}} \tag{D-5}$$

$$g_{m\_top} = \frac{2I_{cm}}{V_{gt\_top}} \tag{D-6}$$

$$\mathrm{PSD}_{DAC1} = R_1^2 \times \left[(2^N - 1) \times 4kT\gamma \frac{2I_{LSB}}{V_{gt\_bot}} + 8kT\gamma \frac{2I_{cm}}{V_{gt\_top}}\right] + R_1^2 \times \left[(2^N - 1) \times \frac{KF_n I_{LSB}}{fC_{ox}L_u^2} + \frac{2KF_p I_{cm}}{fC_{ox}L_{cm}^2}\right] \tag{D-7}$$

The LSB current of the DAC and the common-mode current can be expressed as a function of the input resistor of the main integrator (R_1) and the reference voltage of the quantizer (V_{REF}) as expressed by equation (D-8) and (D-9). Assuming the approximation of equation (D-10) valid allows writing equation (D-11).

$$I_{LSB} = \frac{V_{REF}}{2^N \times R_1} \tag{D-8}$$

$$I_{cm} = \frac{(2^N - 1)}{2^{N+1}} \times \frac{V_{REF}}{R_1} \tag{D-9}$$

$$\frac{(2^N - 1)}{2^N} \approx 1 \tag{D-10}$$

$$\mathrm{PSD}_{DAC1} \approx 8kT\gamma R_1 \times \frac{V_{REF}}{V_{gt\_dac}}\left[1 + \frac{V_{gt\_dac}}{V_{gt\_cm}}\right] + \frac{R_1 KF_n V_{REF}}{fC_{ox}L_u^2}\left[1 + \frac{KF_n}{KF_p} \times \left(\frac{L_{bot}}{L_{top}}\right)^2\right] \tag{D-11}$$

Assuming that the drain to source voltage of the top transistors and the bottom transistors is symmetrical, we chose $V_{gt\_dac} = V_{gt\_top} = V_{gt\_bot}$ and equation (D-11) reduces to equation (D-12).

$$\overline{V_{dac}^2}(f) \approx 16kT\gamma R_1 \times \frac{V_{REF}}{V_{gt\_dac}} + \frac{R_1 KF_n V_{REF}}{fC_{ox}L_u^2}\left[1 + \frac{KF_n}{KF_p} \times \left(\frac{L_{bot}}{L_{top}}\right)^2\right] \tag{D-12}$$

The total noise PSD referred to the input of the modulator is given by equation (D-13).

$$\mathrm{PSD} = 8kTR_1 + \left(16kT\gamma R_1 \times \frac{V_{REF}}{V_{gt\_dac}} + \frac{KFI_{LSB}}{fC_{ox}L_u^2}\right) + \left(\frac{8kT\gamma}{g_{m\_opamp}} + \frac{2KFI_1}{fC_{ox}L_1^2 g_{m\_opamp}^2}\right) \tag{D-13}$$

Equation D-13 can be rewritten by separating thermal and flicker noise:

$$\mathrm{PSD} = \left[8\mathrm{kTR}_1 + 16\mathrm{kT}\gamma\mathrm{R}_1 \times \frac{\mathrm{V_{REF}}}{\mathrm{V_{gt\_dac}}} + \frac{8\mathrm{kT}\gamma}{\mathrm{g_{m\_opamp}}}\right] + \left[\frac{\mathrm{KFI_u R_1^2}}{\mathrm{fC_{ox} L_u^2}} + \frac{2\mathrm{KFI_1}}{\mathrm{fC_{ox} L_1^2 g_{m\_opamp}^2}}\right] \quad \text{(D-14)}$$

Appendix E

Common-mode voltage in the front-end

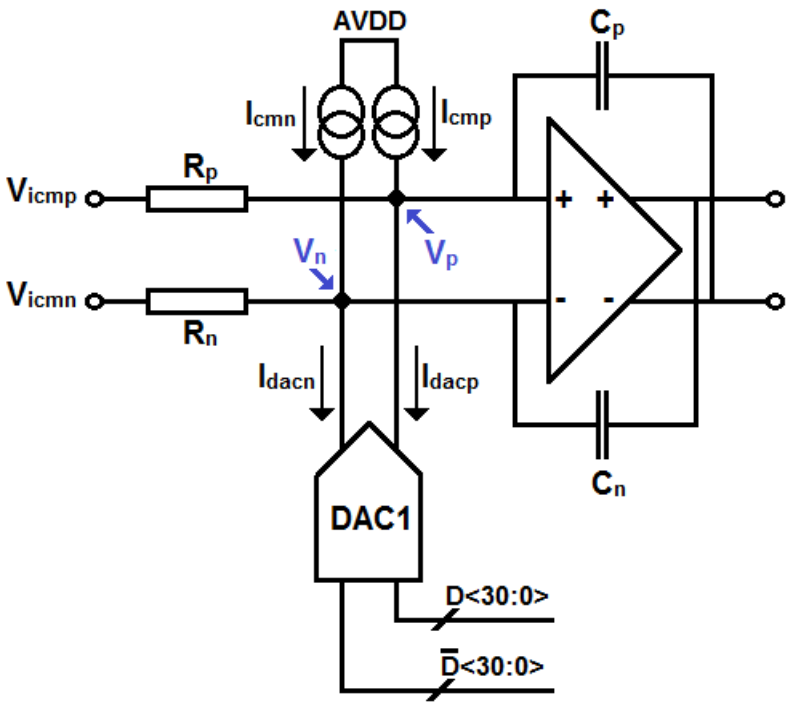


Figure E-1. Common-mode voltage in the Front-End.

Considering the schematic of Figure E-1 and applying the Kirchhoff current law at the non-inverting input of the opamp we can write:

$$\frac{V_{icmp}-V_p}{R_p} + I_{cmp} = I_{dacp} + \frac{V_p - V_{outn}}{Z_p} \quad \text{(E-1)}$$

$$V_{icmp} - V_p + I_{cmp} \times R_p = I_{dacp} \times R_p + R_p C_p p \times (V_p - V_{outn}) \quad \text{(E-2)}$$

$$V_p = \frac{V_{icmp}+I_{cmp}\times R_p - I_{dacp}\times R_p}{1+R_p C_p p} + \frac{R_p C_p p}{1+R_p C_p p} \times V_{outn} \quad \text{(E-3)}$$

$$I_{dacp} = \sum_{n=1}^{2^N-1}(I_{unit} + \delta I_n) \times D_n \quad \text{(E-4)}$$

$$V_p = \frac{V_{icmp}+I_{cmp}\times R_p - R_p \times \sum_{n=1}^{2^N-1}(I_{unit}+\delta I_n)\times D_n}{1+R_p C_p p} + \frac{R_p C_p p}{1+R_p C_p p} \times V_{outn} \quad \text{(E-5)}$$

If we assume that in the band of interest $\frac{1}{R_p C_p} \ll BW$, equation (E-5) becomes equation (E-6)

$$V_p \approx V_{icmp} + I_{cmp} \times R_p - R_p \times \sum_{n=1}^{2^N-1}(I_{unit} + \delta I_n) \times D_n \quad \text{(E-6)}$$

By using the same approach at the inverting input of the opamp we can write the equation (E-7) as:

$$V_n \approx V_{icmn} + I_{cmn} \times R_n - R_n \times \sum_{n=1}^{2^N-1}(I_{unit} + \delta I_n) \times \overline{D_n} \quad \text{(E-7)}$$

We deduce the expression of the common mode at the input of the opamp:

$$V_{icm,opamp} = \frac{V_p+V_n}{2} = \frac{1}{2} \times \left[V_{icmp} + V_{icmn} + I_{cmp} \times R_p + I_{cmn} \times R_n - R_p \times \sum_{k=1}^{2^N-1}(I_{unit} + \delta I_k) \times D_n - R_n \times \sum_{k=1}^{2^N-1}(I_{unit} + \delta I_k) \times \overline{D_k}\right] \quad \text{(E-8)}$$

$$V_{icm,opamp} = \frac{1}{2} \times \left[V_{icmp} + V_{icmn} + I_{cmp} \times R_p + I_{cmn} \times R_n - R_p \times \sum_{k=1}^{2^N-1}(I_{unit} + \delta I_k) \times D_k - R_n \times \sum_{k=1}^{2^N-1}(I_{unit} + \delta I_k) \times \overline{D_k}\right] \quad \text{(E-9)}$$

$$V_{icmp} = V_{icm} + \delta V_{icmp} \quad \text{(E-10)}$$
$$V_{icmn} = V_{icm} + \delta V_{icmn} \quad \text{(E-11)}$$

$$I_{cmp} = I_{cm} + \delta I_{cmp} \quad \text{(E-12)}$$
$$I_{cmn} = I_{cm} + \delta I_{cmn} \quad \text{(E-13)}$$

$$R_p = R + \delta R_p \quad \text{(E-14)}$$
$$R_n = R + \delta R_n \quad \text{(E-15)}$$

$$V_{icm,opamp} = \left[V_{icm} + RI_{cm} - \frac{(2^N-1)}{2} \times RI_{unit}\right] + \frac{1}{2} \times \left[R \times \delta I_{cmp} + \delta R_p \times I_{cm} + \delta R_p \times \delta I_{cmp} + R \times \delta I_{cmn} + \delta R_n \times I_{cm} + \delta R_n \times \delta I_{cmn}\right] - \frac{1}{2} \times \left[\delta R_p \times \sum_{k=1}^{2^N-1}(I_{unit} + \delta I_k) \times D_k + \delta R_n \times \sum_{k=1}^{2^N-1}(I_{unit} + \delta I_k) \times \overline{D_k}\right] \quad \text{(E-16)}$$

$$\overline{D_k} = 1 - D_k \quad \text{(E-17)}$$

$$V_{icm,opamp} = \left[V_{icm} + RI_{cm} - \frac{(2^N-1)}{2} \times RI_{unit}\right] + \frac{1}{2} \times \left[R \times \delta I_{cmp} + \delta R_p \times I_{cm} + \delta R_p \times \delta I_{cmp} + R \times \delta I_{cmn} + \delta R_n \times I_{cm} + \delta R_n \times \delta I_{cmn}\right] - \frac{1}{2} \times \left[\delta R_p \times \sum_{k=1}^{2^N-1}[(I_{unit} + \delta I_k) \times D_k] + \delta R_n \times \sum_{k=1}^{2^N-1}[(I_{unit} + \delta I_k) \times (1 - D_k)]\right] \quad \text{(E-18)}$$

The signal-dependent term is given by equation (E-19):

$$-\frac{1}{2} \times \left[\sum_{k=1}^{2^N-1}\left[\delta R_p \times (I_{unit} + \delta I_k) \times D_k + \delta R_n \times (I_{unit} + \delta I_k) \times (1 - D_k)\right]\right] - \frac{1}{2} \times \left[\sum_{k=1}^{2^N-1}\left[\delta R_p \times (I_{unit} + \delta I_k) \times D_k + \delta R_n \times (I_{unit} + \delta I_k) - \delta R_n \times (I_{unit} + \delta I_k) \times D_k\right]\right] - \frac{1}{2} \times \left[\sum_{k=1}^{2^N-1}\left[(\delta R_p - \delta R_n) \times (I_{unit} + \delta I_k) \times D_k + \delta R_n \times (I_{unit} + \delta I_k)\right]\right] \quad \text{(E-19)}$$