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Nanometer scale point contacting techniques for silicon Photovoltaic devices

Rasha Khoury

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Par

Mme Rasha KHOURY

Nanometer scale point contacting techniques for silicon Photovoltaic devices

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Composition du Jury :

| | | |
|---------------------|---|--------------------|
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Abstract

In this PhD work, I explore the possibility and potential advantages of using nanoscale contact openings in the range of 1 μm or below and, consequently, with a pitch shorter than 10 μm . Indeed, analytic and numerical simulations done with and by our collaborators during the course of this thesis have shown that such nanoscale contacts would result in negligible ohmic losses while still keeping $S_{\text{eff, rear}}$ at an acceptable level, as long as the recombination velocity at the contact (S_{cont}) is in the range from 10^3 - 10^5 cm/s. To achieve such contacts in a potentially cost-reducing way, my experimental work has focused on the use of polystyrene nanospheres as a sacrificial mask.

The thesis is therefore divided into three sections. In the first section, three deposition techniques (spray-coating, spin-coating, and a floating transfer technique) for particles were tested. The first two give poorly controlled distributions of nanospheres on the surface, but with appropriately low values of coverage. The floating transfer technique provided a densely-packed monolayer of NPs on the surface; this process necessitated an additional O_2 plasma step to reduce the coverage area of the sphere; this was performed and studied using a matrix distributed electron cyclotron resonance (MD-ECR) plasma. The removal of the nanospheres after being coated by metals and dielectrics was also studied.

In the second section of this thesis, three different approaches were developed to generate local point contacts on metallic and crystalline silicon surfaces. The first uses the NPs as a direct deposition mask (Approach A), for example by dispersing NPs onto a layer, depositing SiO_2 or Si_3N_4 by PECVD on top of the NPs, and then removing the NPs. The second is by depositing a secondary etching mask layer on top of the NPs. This was done with evaporated Al as a plasma-etching mask for thermally grown SiO_2 (Approach B), and PECVD a- $\text{SiC}_x\text{:H}$ as a wet-etch mask for Al_2O_3 deposited by ALD (Approach C). I have tested nanoholes formed using approach A as point contacts on a NIP a-Si:H solar cell. Homogeneously distributed nano-contacts less than 100 nm as diameter were obtained in the back-reflector layer with an average distance between the contacts of ~ 350 nm. The electrical characteristics of the nano contacted NIP a-Si:H were compared to the same cells done without the dielectric layer, and to a structure with a dielectric layer but without any nanoholes.

In the third section of this thesis, I investigate the use of such nanoholes in crystalline silicon technology by the formation of doped contacts through nanoholes formed by approach B. Boron doping by both thermal diffusion and ion implantation techniques were investigated. A thick thermally grown oxide was used as the diffusion/implantation barrier. Once the NPs and the secondary etch mask were removed, these samples were characterized by secondary electron microscopy (SEM) and conductive probe atomic force microscopy (CP-AFM). Localized doping was indeed observed through CP-AFM by acquiring current-voltage curves both within and beside the doped area, and nanoscale solar cells were observed. For the ion implantation samples, a Rapid Thermal Annealing step dramatically changed the appearance of the samples under SEM, and although diodes were formed, the process needs further refining to produce the same results as diffusion.

In summary, the work presented in this PhD manuscript has developed and explored a potentially low-cost technique of creating nano-scale openings for optoelectronic devices. A number of hole-creating techniques are developed, described, and deployed in test structures involving thin-film and crystalline silicon.

Keywords: Polystyrene Nanoparticles, Nanostructure, Doping, crystalline silicon, thin film, Conducting Probe Atomic Force Microscopy, Secondary electron microscopy.

List of acronyms

AFM: Atomic Force Microscopy

AlCu: Alloy of 98% Aluminum and 2% Copper

ALD: Atomic Layer Deposition

a-Si:H: Hydrogenated Amorphous Silicon

BSE: Backscattered Electrons

BOE: Buffered Oxide Etch

CCP: Capacitively Coupled Plasma

CP-AFM: Conductive Probe AFM

cSi: Crystalline Silicon

CVD: Chemical Vapor Deposition

DI: Deionized

DLS: Dynamic Light Scattering

ECR: Electron Cyclotron Resonance

ECV: Electro-Chemical Capacitance Voltage

FE-SEM: Field-Effect Scanning Electron Microscopy

HF: Hydrofluoric Acid

ICP: Inductively Coupled Plasma

ITO: Indium Tin Oxide

LTO: Low Temperature oxidation

MDECR: Matrix Distributed Electron Cyclotron Resonance

NP: Nanoparticle

PECVD: Plasma Enhanced Chemical Vapor Deposition

PERC: Passivated Emitter and Rear Cell

PERL: Passivated Emitter Rear Locally Diffused Cell

PS: Polystyrene

PV: Photovoltaic

PVD: Physical Vapor Deposition

RF: Radio Frequency

RIE: Reactive Ion Etching

SE: Secondary Electron

SEM: Secondary Electron Microscopy

SCM: Scanning Capacitance Microscopy

SIMS: Secondary Ion Mass Spectrometry

SNDM: Scanning Nonlinear Dielectric Microscopy

SPM: Scanning Probe Microscopy

SSRM: Scanning Spreading Resistance Microscopy

TEM: Transmission Electron Microscopy

TMA: Trimethylaluminum

TMB: Trimethylboron

US: Ultrasonic

UV: Ultra-Violet

“ Un jour je pourrai dire ça n’a pas été facile mais j’ai réussi ”

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Contents

| | |
|---|-----------|
| Chapter 1: Introduction | 1 |
| 1.1 Nanoparticle use in different applications | 2 |
| 1.2 NPs for Photovoltaics | 4 |
| 1.2.1 Light Management | 4 |
| 1.2.2 NPs for Lithography..... | 8 |
| 1.3 Forming point contacts using different techniques in PV devices | 10 |
| 1.3.1 Forming point contacts using lithography in PV devices | 11 |
| 1.3.2 Forming point contacts using laser in PV devices | 14 |
| 1.3.3 Forming point contacts using NPs in PV devices | 16 |
| 1.4 Motivation for nanocontacts in c-Si devices | 19 |
| 1.4.1 Rear surface modelling | 19 |
| 1.4.2 Impact on solar cell efficiency | 21 |
| 1.4.3 Summary and device architectures | 23 |
| 1.5 Summary and Thesis Outline | 25 |
| Chapter 2: Experimental techniques | 27 |
| 2.1 Deposition techniques | 28 |
| 2.1.1 Spin coating | 28 |
| 2.1.2 Radio frequency-Plasma-enhanced chemical vapor deposition..... | 28 |
| 2.1.3 Matrix Distributed Electron Cyclotron Resonance-PECVD..... | 31 |
| 2.1.3.1 Electron Cyclotron Resonance-PECVD | 31 |
| 2.1.3.2 Matrix distributed-ECR PECVD, Venus | 32 |
| 2.1.4 Atomic Layer Deposition (ALD) | 33 |
| 2.1.5 Thermal oxidation | 35 |
| 2.1.6 Thermal evaporation | 36 |
| 2.1.7 RF magnetron sputtering..... | 36 |
| 2.1.8 Reactive Ion Etching (RIE)..... | 37 |
| 2.1.9 Doping..... | 38 |
| 2.1.9.1 Doping by diffusion | 38 |
| 2.1.9.2 Doping by ion implantation | 40 |

| | | |
|--|---|------------|
| 2.2 | <i>Characterization techniques</i> | 41 |
| 2.2.1 | Spectroscopic ellipsometry | 41 |
| 2.2.2 | Secondary electron microscopy (SEM) | 42 |
| 2.2.2.1 | Challenges using different detectors | 44 |
| 2.2.3 | Atomic force microscope (AFM)..... | 47 |
| 2.2.3.1 | AFM..... | 47 |
| 2.2.3.2 | Conductive probe atomic force microscope (CP-AFM) | 50 |
| 2.2.4 | J-V measurements | 51 |
| 2.2.5 | Electro-chemical capacitance voltage (ECV) profiling | 54 |
| 2.2.6 | Dynamic light scattering (DLS)..... | 54 |
| Chapter 3: Nanoparticle Deposition, Etching and Removal | | 55 |
| 3.1 | <i>Nanoparticle deposition</i> | 57 |
| 3.1.1 | Method 1: NP deposition by spraying..... | 57 |
| 3.1.2 | Method 2: NP deposition by spin coating | 59 |
| 3.1.2.1 | 50 nm PS particles..... | 59 |
| 3.1.2.2 | 100 nm PS particles..... | 62 |
| 3.1.2.3 | Role of substrate surface | 64 |
| 3.1.2.4 | Summary-NP deposition by spin coating..... | 67 |
| 3.1.3 | Method 3: NP deposition by floating transfer technique | 67 |
| 3.2 | <i>Nanoparticle etching by O₂ plasma using MDECR</i> | 69 |
| 3.2.1 | Effect of plasma power | 70 |
| 3.2.2 | Role of ions | 72 |
| 3.2.3 | Evolution of particle shapes | 76 |
| 3.2.4 | Summary-NP etching..... | 83 |
| 3.3 | <i>Nanoparticle Removal</i> | 83 |
| 3.3.1 | NP removal via solution..... | 83 |
| 3.3.2 | NP removal by tape stripping..... | 95 |
| 3.3.3 | Summary-NP removal..... | 97 |
| 3.4 | <i>Chapter Summary</i> | 98 |
| Chapter 4: Characterization of nanoholes | | 101 |
| 4.1 | <i>Forming nanoholes in thin dielectric layers</i> | 104 |
| 4.1.1 | Approach A: Covering the NPs with a thin dielectric layer..... | 104 |
| 4.1.1.1 | Electrical characterization using CP-AFM | 104 |

| | | |
|--|--|------------|
| 4.1.1.2 | CP-AFM – Holes in films on c-Si substrates | 105 |
| 4.1.1.3 | CP-AFM – Holes in films on coated glass substrates | 109 |
| 4.2 | <i>Forming nanoholes in thick dielectric layers</i> | 110 |
| 4.2.1 | Approach B: Using aluminum as a mask | 111 |
| 4.2.1.1 | ZnO-glass substrates | 111 |
| 4.2.1.2 | Silicon substrates..... | 113 |
| 4.2.1.3 | Summary-Approach B | 121 |
| 4.2.2 | Approach C: Using a-SiC _x :H as a mask..... | 121 |
| 4.2.2.1 | HF as wet etchant | 122 |
| 4.2.2.2 | RCA "Soft" as wet etchant | 122 |
| 4.3 | <i>a-Si:H test PV devices</i> | 126 |
| 4.3.1 | PIN Structure | 127 |
| 4.3.2 | NIP structure | 128 |
| 4.3.3 | Solar cell Characterization | 129 |
| 4.3.4 | Summary of a-Si:H Solar Cells..... | 135 |
| 4.4 | <i>Chapter Summary</i> | 136 |
| Chapter 5: Localized doped nanocontacts in cSi..... | | 137 |
| 5.1 | <i>Doping through nanoholes</i> | 139 |
| 5.1.1 | Doping by diffusion through nanoholes..... | 140 |
| 5.1.1.1 | Description of masking layer | 140 |
| 5.1.1.2 | Experimental description | 142 |
| 5.1.1.3 | Characterization by SEM and CP-AFM | 145 |
| 5.1.1.4 | Summary – Diffusion results | 170 |
| 5.1.2 | Doping by ion implantation through nanoholes..... | 171 |
| 5.1.2.1 | Overview and Description of Ion Implantation Process | 171 |
| 5.1.2.2 | Experimental description | 174 |
| 5.1.2.3 | Characterization by SEM and CP-AFM | 175 |
| 5.1.2.4 | Discussion and ECV Measurements | 189 |
| 5.1.2.5 | Summary – Ion implantation results | 190 |
| 5.2 | <i>Chapter Summary</i> | 192 |
| Chapter 6: Conclusions and Perspectives | | 193 |
| 6.1 | <i>Conclusions</i> | 193 |
| 6.2 | <i>Perspectives</i> | 195 |

Appendix199
Bibliography I

Chapter 1: Introduction

| | | |
|-------|--|----|
| 1.1 | <i>Nanoparticle use in different applications</i> | 2 |
| 1.2 | <i>NPs for Phtovoltaics</i> | 4 |
| 1.2.1 | Light Management | 4 |
| 1.2.2 | NPs for Lithography..... | 8 |
| 1.3 | <i>Forming point contacts using different techniques in PV devices</i> | 10 |
| 1.3.1 | Forming point contacts using lithography in PV devices | 11 |
| 1.3.2 | Forming point contacts using laser in PV devices | 14 |
| 1.3.3 | Forming point contacts using NPs in PV devices | 16 |
| 1.4 | <i>Motivation for nanocontacts in c-Si devices</i> | 19 |
| 1.4.1 | Rear surface modelling | 19 |
| 1.4.2 | Impact on solar cell efficiency | 21 |
| 1.4.3 | Summary and device architectures | 23 |
| 1.5 | <i>Summary and Thesis Outline</i> | 25 |

Introduction

Nanotechnology is defined as the study and use of structures between 1 nanometer and 100 nanometers in size, including particles of this size that have been named Nanoparticles (NPs). Their preparation is not an exclusive result of modern research nor restricted to man-made materials. NPs have existed in nature for long time, and include organic (proteins, viruses, among others) as well as inorganic compounds and are produced by events such as volcanic eruptions. The use of nanostructured materials is not a recently development either. It dates back to the fourth century AD when Romans were using nanosized metals to decorate glasses and cups. One of the most famous example is the Lycurgus Cup (in the British museum) that was fabricated from gold and silver NPs that were embedded in the glass. It appears with a green color in daylight, but changes to red when illuminated from the inside [1], [2]. From a scientific point of view, the big step forward in NP research was made by Michael Faraday more than 150 years ago. His studies on the interaction of light with metal NPs can be regarded as the beginning of modern colloidal chemistry and the emergence of Nanoscience and Nanotechnology [3].

Manmade nanotechnology has been around for centuries. So why is nanotechnology considered a new subject just now?

Although our ancestors made gold NPs, they were not able to observe them under a microscope, manipulate them, or have much control over them. Developments in the last two decades have produced advanced microscopy where particles down to a single atom can be imaged. Tools than can define structures down to few nanometers in size were developed. Despite how it is shown in the media, nanotechnology is not a new creation that began at a specific time. What used to be microtechnology slowly transitioned to become nanotechnology, just like what used to be macromachining evolved into microfabrication in the 1950s and the 1960s [4].

The principle motivation to further develop research on NPs is because of the so-called quantum size effect, where the properties of materials in the range of 1-100 nm are size-dependent, in contrast to a macroscopic bulk material which has constant physical properties regardless of its size. Consequently, the development of advanced synthesis routes not only offering control over the composition, as already required for traditional bulk synthesis, but also over particle size, size distribution, shape and surface properties became essential on the way to study and apply the size-dependent properties of nanomaterials. There are different methods for synthesis of nanoparticles and can be divided into three main groups:

- Gas phase methods [5] which include vapor deposition, flame pyrolysis and arc discharge.
- Liquid phase methods [6] which include hydrothermal, microemulsion, chemical reduction and sol gel.
- Solid phase mechanical processes [6]including grinding, milling and alloying.

1.1 Nanoparticle use in different applications

NPs in medicine:

In recent years, NPs have emerged as important players in modern medicine, with applications ranging from contrast agents in medical imaging to carriers for drug and gene delivery. This is because many of the inner workings of cells naturally occur at the nanoscale. For instance, hemoglobin, the protein that carries oxygen through the body, is 5.5 nm in diameter, and a strand of DNA is only about 2 nanometers in diameter. Another reason is the important and unique features of NPs, such as their surface to mass ratio, which is much larger than that of other particles and materials, allowing for catalytic promotion of reactions, as well as their ability to adsorb and carry other compounds. This property will allow the NPs to have a

Introduction

large functional surface that can carry drugs, probes and proteins. Drug delivery is the efficient targeting of the drug to cells or tissue of choice. Even though optimal effects would arise from focusing the drug to the target organ, a large percentage of ordinary drugs taken orally are destroyed by the stomach or liver, and then distributed throughout the entire body, which can lead to side-effects in some organs. The therapeutic potential of currently available drugs is masked by local instability issues and difficulties in crossing certain biological barriers such as the blood brain barrier and placenta. Targeted drug-delivery by NPs has the potential to overcome some of these problems, and render the treatment more effective with ensuring cost and safety benefits [7].

Depending on the particle charge, surface properties, and relative hydrophobicity, NPs can be designed to adsorb preferentially on organs or tissues. The effectiveness of these NPs has been demonstrated for mucoadhesive systems by Brannon-Peppas [8] for the gastrointestinal tract and for the blood brain barrier by Gessner et, al [9][10].

NPs in optics:

[Lasers] Using “dark lattice modes” researchers at Aalto University have created a plasmonic nanolaser that operates at visible light frequencies. Normally dark mode lasing can be useless because light is trapped at the NP array and cannot leave. However, in this application, the laser is fabricated using an array of NPs combined with dye molecules. The lasing occurs in a dark mode and the laser light leaks out from the edges of the array. It is based on 100nm silver NPs arranged in a periodic array that act as tiny antennas with the interparticle distance matched with the laser wavelength [11].

[Lighting] Research in solid state lighting (SSL) has the goal of making lighting technologies more energy efficient, longer lasting and cheaper. Instead of using inert gases or vacuum tubes, it relies on light being emitted from a semiconductor. Two of the main related technologies are light emitting diodes (LED) in which the emissive layer is inorganic, and organic light-emitting diodes (OLED) in which the emissive layer is an organic material. OLEDs is a potential technology as it can be made thinner and lighter than comparable LED devices, in addition it can be printed onto almost any substrate which will allow this technology to be used in many applications.

Many methods were proposed for the fabrication of OLEDs such as thermal evaporation, spin coating, ink-jet printing, screen printing, and photolithographic method. However, some problems may occur by using these deposition techniques. For instance, thermal deformation of the mask and substrate can be caused when thermal evaporation is used as the fabrication method. On the other hand, ring strain effect can be observed when liquid-based deposition methods are used.

Nanoparticles-based deposition methods may be a solution for the OLED fabrication problems. Electro spray deposition (ESD) is a method to fabricate thin films of micro or nanoparticles directly from solution. This method is advantageous as it is performed under atmospheric pressure and room temperature, which may lead to low equipment cost. In addition, ring-strain effects will not occur due to the deposition of dried NPs by electrostatic force. Jungmyoung Ju et al have proposed a new method of fabricating thin and regular films for OLEDs using the electro spray deposition method, where the NPs are deposited on the target substrate just before they become completely dry [12]. Gabriel Lozano et al, have as well discussed new methods that enhance the efficiencies of LEDs using metallic nanostructures [13].

It is clear that NPs have applications in many fields, only some of which have been given as examples above. Focusing more on the subject of this thesis, the next part of the chapter (1.2) will discuss their use in the specific application of photovoltaics (PV).

1.2 NPs for Photovoltaics

Photovoltaics (PV) is a fast-growing market. The production volume in 2016 was about 250 times that of 2000, with a compound annual growth rate (CAGR) of over 40 % [14]. Crystalline silicon PV products dominate the solar-cell market, with up to 93% market share and about 75 GW installed in 2016 in total [15].

1.2.1 Light Management

While many technical difficulties with crystalline cells can be overcome or mitigated, cost is still a major factor. One way to reduce the cost is to reduce the quantity of material used by decreasing the cSi thickness. However, the incident light cannot be fully absorbed in cSi thicknesses around 2-3 μm , therefore light trapping is essential for such structures.

Another PV technology, thin film devices, can be attractive in terms of low cost and lower quantity of material used. Since this technology relies on a thin film of weakly absorbing material, light management is a key aspect to improve the efficiency of such device. Both inorganic and organic [16] thin film solar cells can take advantage of light management to enhance their conversion efficiency. Concerning silicon thin films, although a-Si:H absorption coefficient is much higher than that of c-Si, the carrier diffusion length in this material is much shorter than cSi. The thickness of the active layer must thus be less than 1 μm to facilitate carrier extraction before the free carriers recombine. Light trapping techniques are essential for thin film technologies to increase their absorption.

Light trapping by means of light-scattering was demonstrated as early as 1983 by Deckman et al. [17] and light management became an integral part of thin film silicon devices in the decades that followed.

Enhancement of the photo induced charge generation rate in PV device can be done by enhancing the path length of the incident photons within the device. This can be realized by implementing sub-wavelength scattering centers at the front and/or the rear of the cell.

Colloidal particles, which show interaction with electromagnetic radiation at optical frequencies, can be used for this function by tailoring its performance over a broad range via materials selection, particle size and geometry. Structured electrodes have also received much attention due to their dual role as light harvesting systems and conductive electrodes.

[Nanoshells] In 2011, Yao et al. demonstrated a new approach for light management by forming whispering-gallery resonant modes inside a nanocrystalline silicon (nc-Si) spherical nanoshell structure. Silica NPs were assembled into close-packed layers on quartz wafers, and Si was then deposited on the NPs followed by NP removal. The geometry of the structure facilitates the coupling of light into the resonant modes and an enhancement of the light path in the active material, thus an improvement in absorption. It was shown that the absorption of a single layer of 50 nm thick spherical nanoshells is equivalent to a 1 μm thick planar nc-Si film. They also showed that the optical response of the nanoshells can be tuned by changing the thickness. Further enhancement of absorption was demonstrated using multiple layers and an AR coating. Figure 1.1 shows the cross-sectional SEM images of one, two and three layers of nanoshells and the absorption spectrum of each sample. For the short wavelength region ($<500\text{ nm}$), the absorption is independent of the layers number. The reason of this independence is that the absorption coefficient of nc-Si in this region is high ($> 1 \times 10^5\text{ cm}^{-1}$), therefore the light loss is mainly depending of the light reflection. However, for wavelengths above 500 nm, an increase in the absorption is seen with the number of layers. For instance, the absorption increases from 27 % for one layer to 34 % for two layers, and to 41 % for three layers at a wavelength of 900 nm. The integrated absorption increases by 6 % between the single and triple

Introduction

layer samples. An additional coating of the three layers with an AR coating (100 nm thick, tin-doped indium oxide) improves near-infrared absorption with a total absorption of 75 % of the above-bandgap solar spectrum [18].

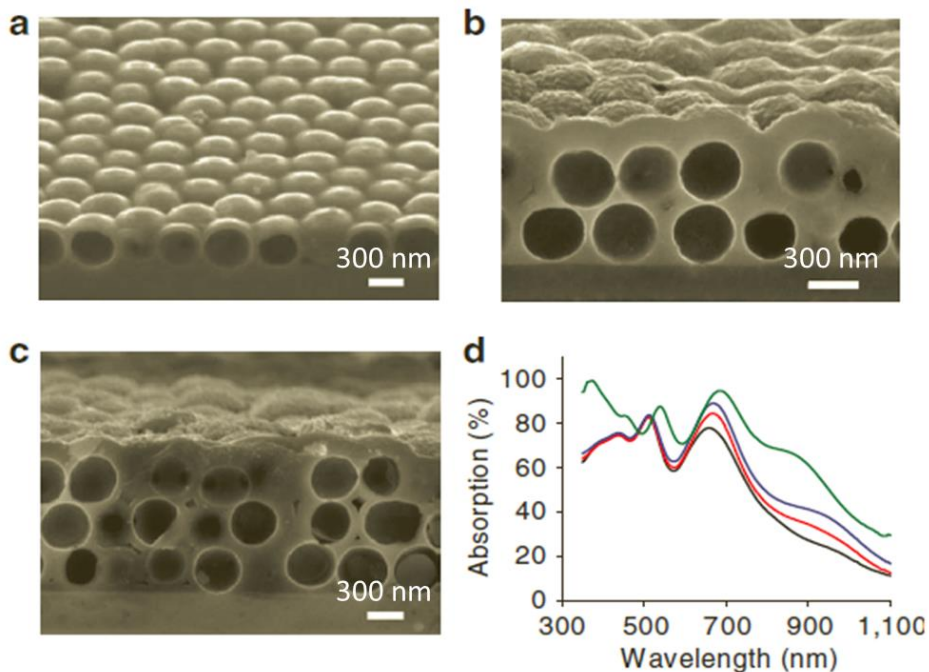


Fig.1.1: (a-c) Cross-sectional SEM images of one to three layers of nc-Si spherical nanoshells. (d) Absorption spectra corresponding to different numbers of layers of spherical nanoshells: one layer (black), two layers (red), three layers (blue). 100-nm thick tin-doped indium oxide (ITO) AR layer coating (dark green) further improves absorption of three-layer film, with a total absorption of 75% of the above-bandgap solar spectrum [18].

[Silica NPs] An experiment twist to this concept has been realized by depositing silica NPs on top of the substrate rather than using it to form nanoshell arrays. In 2011, Grandidier et al. [19] proposed a layer of silica nanospheres in close contact with the active layer of a solar cell which can eventually couple the incident light and could increase the light absorption. Figure 1.2 shows a theoretical approach of wavelength-scaled dielectric spheres, which enhance the solar cell efficiency via excitation of whispering gallery and waveguide modes [20]. The overall integrated current density corresponding to the energy absorbed in the a-Si in the presence of the nanospheres is $J = 13.7 \text{ mA}\cdot\text{cm}^{-2}$, which corresponds to an enhancement of 12 % compared to the case without the sphere array. It can be seen from fig1.2.b that over the entire wavelength range, the spectral current density is higher with the spheres than without the spheres. They demonstrated the possibility to tune the spectral response by varying the particle diameter and the particle spacing in order to enhance the absorption in the a-Si layer and therefore increase the current density. Also, the number of resonances can be increased to make the response more broadband by assembling arrays of spheres with different diameters. In addition, their spherical geometry allows light to be efficiently coupled into the solar cell over a large range of incidence angles. Also, these arrays are deposited on a flat a-Si:H, which has an advantage over cells grown on textured surfaces as surface roughness or topography can create holes or oxidation and therefore reduce the efficiency and lifetime of the solar cell, but this structure features some dependence on the polarization of the light.

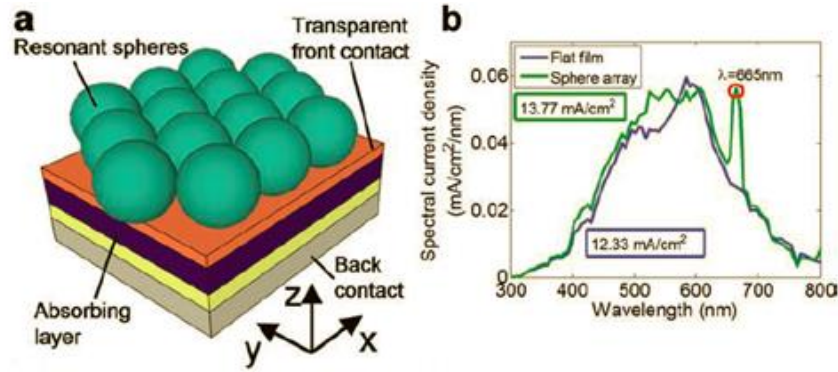


Fig.1.2: (a) Schematic of solar cell with dielectric nanosphere, (b) Current density calculated in amorphous silicon layer with and without the presence of nanospheres [19].

[Metallic NPs] Whereas particles from dielectric materials interact with electromagnetic radiation predominantly via scattering, the situation is different for metallic colloids. When reduced to the nanosize, such metal colloids show strong absorption peaks due to the collective oscillations of the electrons of the conduction band. Due to their plasmon resonance, metal NPs exhibit strong localized electric fields, which are of great interest for enhancing the photon-exciton conversion in PV devices [21][22][23][24]. The type, size and shape of the particle as well as the inter-particle distance affect the magnitude and the number of the near-field resonances [25].

[Au NPs] Early in 2005, Schaadt et al. [26] reported an engineered enhancement of optical absorption and photocurrent in a semiconductor via the excitation of surface plasmon resonances in spherical Au nanoparticles deposited on the semiconductor surface.

The basic device structure is shown schematically in Fig.1.3 Au NPs with diameters of 50, 80, and 100 nm are compared, and the surface coverage range from 0.6 % to 1.3 %. It was shown that the enhancement in absorption within the semiconductor results in increased photocurrent response in Si pn junction diodes over wavelength ranges that correspond closely to the nanoparticle plasmon resonance wavelengths.

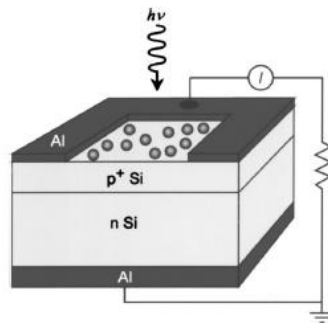


Fig.1.3: Schematic diagram of Si p-n junction diode device structure with metallic nanoparticles [26].

In 2011, Wang et al. [27] have shown that Au nanoparticles incorporated in the photoactive layer of Polymer-fullerene-based bulk heterojunction (BHJ) act as an effective “optical reflector” for solar light, which results in more light harvested in the active layer because of multiple light scattering by the nanoparticles. The Au colloids not only increased the light absorption but also improved the charge transport through the active layer.

Introduction

[Ag NPs] In 2007, S.Pillai et al. [28] investigated the effect of surface plasmons on silver nanoparticles as means of improving the efficiency of thin-film and wafer based Silicon solar cells. They reported an increase in the spectral-response of thin-film cells over almost the entire solar spectrum. At wavelengths close to the band gap of Si, they observed a significant enhancement of the absorption for both thin-film and wafer based structures. This method has the scope of further reducing the thickness of Si to below 1.5 μm with good light trapping provided by the metal nanoparticles. Their findings showed that for front surface application, smaller metal NPs provided the maximum overall enhancement in visible light as well as the near-infrared, but that larger metal NPs would be more beneficial for light emission from both thin and thick Si light emitting diodes (LEDs).

In 2011, Spinelli et al. [29] systematically studied, numerically and experimentally, the coupling of light into a crystalline silicon substrate by scattering light from Ag NPs array geometries placed on top of the substrate. After simulation and optimization, it was found that 200 nm wide and 125 nm high spheroidal Ag particles in a square array with 450 nm pitch on top of a 50 nm thick Si_3N_4 layer provided the best impedance matching for a spectral distribution corresponding to the Air Mass 1.5 solar spectrum. This particle array shows 50 % enhanced incoupling compared to a bare Si wafer, and predict 8 % improvement of light incoupling to Si compared to the best standard interference antireflection (AR) coating. This finding can open new perspectives for AR coating applications in optical devices and for light management in Si solar cells.

Metallic NPs can also be introduced on the back side of the device as was shown by Morawiec et al. [30] in 2014. They have studied the enhancement in the opto-electronic performance of thin a-Si:H solar cells due to the light scattering effects of plasmonic back reflectors (PBRs), composed of self-assembled Ag NPs, incorporated on the rear side of the cell. By placing the NPs on the rear side, the optical losses in the NPs at short wavelengths can be suppressed so they interact only with the long-wavelength photons. As shown in Fig.1.4, the NPs are located between the silicon and the back reflector (BR), forming the so-called plasmonic back reflector (PBR). The optical properties of the PBRs are investigated according to the morphology of the NPs, which can be tuned by the fabrication parameters. It was shown, by analyzing sets of solar cells built on distinct PBRs, that the photocurrent enhancement achieved in the a-Si:H light trapping window (600-800 nm) is linear with the PBRs diffuse reflection and a corresponding J_{sc} enhancement was observed. The best-performing PBRs allow a pronounced broadband photocurrent enhancement in the cells which is related to both the plasmon-assisted light scattering from the NPs and to the front surface texture originated from the conformal growth of the cell material over the particles.

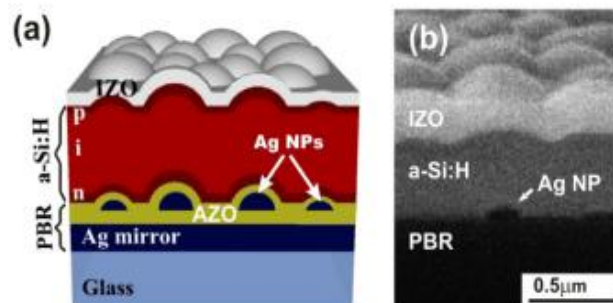


Fig.1.4: Structure of a-Si:H n-i-p solar cell with plasmonic back reflector (PBR) shown (a) schematically and (b) in SEM cross section at a tilt angle of 20° [30].

Similar work have been done by E.Moulin and C.Eminian et al. where they also observed a photocurrent enhancement [31][32].

The previous section was focused on the light management in PV done by assembled colloids. A colloidal particle layer can also be used as template structure for further modification of devices, and this is known as nanosphere lithography.

1.2.2 NPs for Lithography

Nanosphere lithography is also known as colloidal lithography or natural lithography. Fischer and Zinghsheim [33] were the first to report, in 1981, the formation of an ordered monolayer on a glass plate. However, the focus of their work was the replication of submicroscopic patterns using visible light and not fabrication of lithographic colloidal masks.

A year later, Deckman and Dunsmuir [34] extend the scope of Fischer's approach by showing that a monolayer of nanospheres can be used both as an etching or deposition mask. They deposited the monolayer of colloidal particles by random or ordered array over the entire substrate surface and they have named this process as "natural lithography". In the 90s, the method was renamed by the group of Hulteen and Van Duynne [35] and is now commonly called "nanosphere lithography". Their work was not only focused on mono-layers but extends to double layers. Through the years, nanosphere lithography attracted growing interest due to its potential to manufacture a wide variety of one-, two-, or three- dimensional nanostructures [36][37][38][39].

Figure 1.5 shows three simple categories of template electrode designs generated using nanosphere lithography.

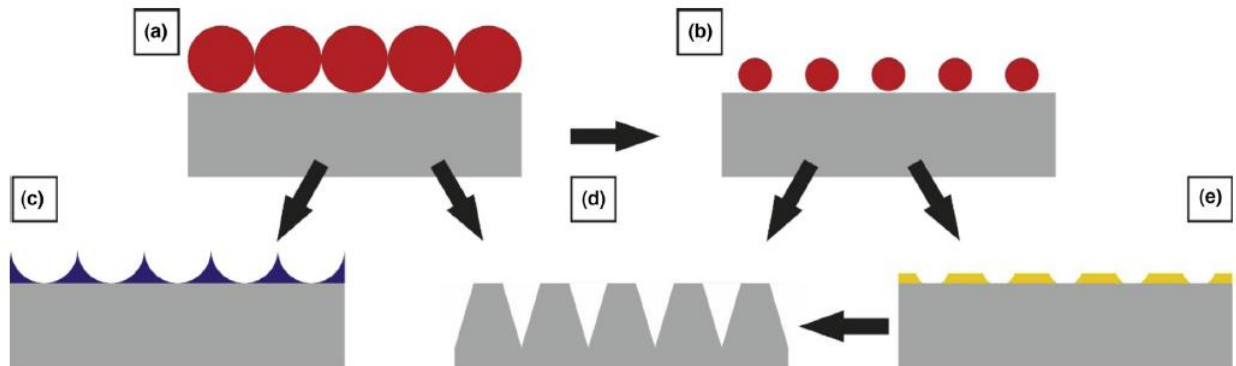


Fig.1.5: (a) Close-packed colloidal monolayer is immobilized on a substrate with spheres typically consisting of polystyrene (PS) or silica. (b) Isotropic etching reduces particle size but retains initial periodicity. (c-e) Range of template motifs is accessible: Isolated pyramids or continuous bowl-like films remain after direct deposition through orifices [25].

The fabrication of templated structures for top or bottom electrodes can either start from close-packed colloidal monolayers or non-close-packed arrays. The latter can be fabricated by doing a plasma etching for the close-packed colloidal monolayer [40]. Figure 1.5.c is obtained from Fig.1.5.a by removing the NPs after depositing a material into the interstitial space of close-packed monolayer [25]. Figure 1.5.d is obtained from Fig.1.5.a by doing an etching of the substrate underneath the NPs in the interstitial space.

[Nanocoones] One of the applications of Fig.1.5.d was done by P Mailoa, et al. [41], where he presented a well-controlled low-cost process to fabricate a periodic nanocone texture optimized for maximum light

Introduction

absorption in thin-film microcrystalline silicon solar cells. The texture is a glass fabricated using nanosphere lithography with the period controlled by the nanospheres diameter and the texture shape and aspect ratio controlled by the reactive ion etching conditions. This was followed by a conformal coating of the TCO layer on the nanotextured glass. Optical absorption measurements show that the same cells fabricated on the optimized nanocone textured substrates exhibit a relative short-circuit current increase close to 30% compared to a reference state-of-the-art cell with a randomly textured zinc oxide layer.

[Nanopatterning] Another application of the structure represented by Fig.1.5.d was shown in 2015 by C.Trompoukis et al. [42] in the frame of “PhotoNVoltaics” project, where he reported on the fabrication, integration, and simulation of both optical and optoelectrical of photonic nanostructures for thin crystalline silicon solar cells. One of the presented methods that is used to fabricate the nanostructures is Hole Mask Colloidal Lithography (HCL). The schematic process flow is shown in Fig.1.6.

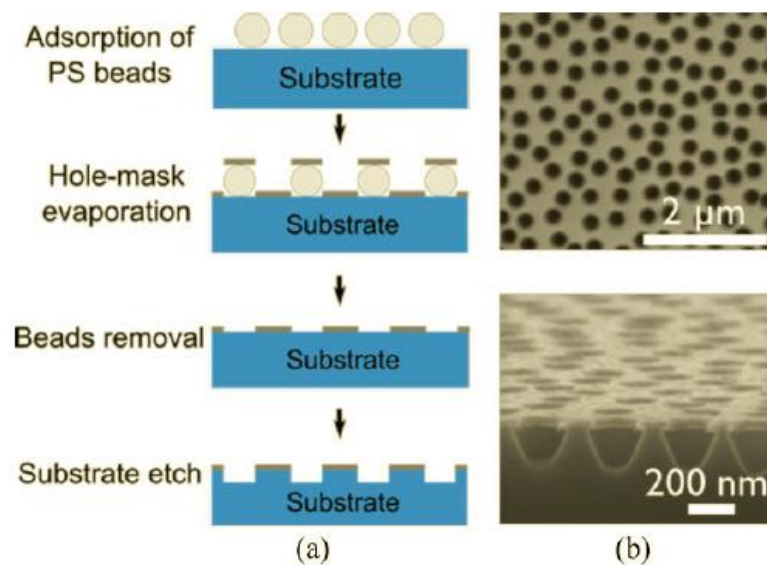


Fig.1.6: (a) Schematic process flow for HCL nanopatterning and (b) HCL-nanopatterned c-Si surface, with 50 nm wide holes: top right-top view of patterned c-Si wafer; bottom right-cross-sectional profile of nanopatterned surface [42].

Two main possibilities of Si etching were presented in that work; dry plasma etching and wet chemical etching. Each features its own resulting profile. Therefore, the nanopatterning possibilities range from periodic to random surface topographies and from nanopyramids to high aspect ratio profiles, each with its own optical and electrical properties. It was shown that optically, the nanopatterning results in better performance than the standard pyramid texturing, showing a more robust behavior with respect to light incidence angle and minimal material consumption. Electrically, wet etching results in higher minority carrier lifetimes compared to dry etching. From the integration of the photonic nanostructures into 1 μm thick c-Si solar cells, certain factors limiting the efficiencies (to ~ 4.8 %) were identified: the parasitic absorption in layers other than the photoactive layers, the conformality of thin-film coatings on top of the nanopattern and the material degradation after etching.

In August 2017, V. Depauw et al. [43], in the frame of the same project “PhotoNVoltaics”, have reported a nanotextured monocrystalline silicon cell with the confirmed efficiency of 8.6 % and an effective thickness of only 830 nm. They have adapted a self-assembled large-area and industry-compatible

Introduction

amorphous ordered nanopatterning, using colloidal lithography, combined with an advanced surface passivation.

[Nanomesh] Another structure that can be obtained using NPs as a mask is a nanomesh, which is obtained after deposition of a material on the NPs followed by NP removal (Fig.1.5.e). Most commonly this formed nanomesh is metallic and can be used as transparent conducting electrode simultaneously.

An application of this structure was done by J. Morfa et al. [44] in 2013, where he studied the potential of 50 nm thick Ag nanomeshes to replace conductive metal oxides as transparent electrode materials. The perforated metal was fabricated using nanosphere lithography by using polystyrene NPs of 756 nm as diameter which represent the periodicity. The inter-aperture spacing was tuned by varying etching times in oxygen plasma, and the effect of inert-aperture “wire” thickness was studied on the optical and electronic properties of perforated silver films. It was shown that optical transmission was limited by reflection and surface plasmons and it didn't exceed 73 % which is smaller than that achieved by ITO. As for the electrical sheet resistance, it can be as low as $3\Omega\text{□}^{-1}$ for thermally evaporated silver films which is smaller than that of ITO. The performance of organic photovoltaic devices comprised of a P3HT:PCBM bulk heterojunction deposited onto the perforated metal arrays was shown. The power conversion efficiency (PCE) of the ITO reference always outperformed the Ag nanomesh devices because of the optical transmission limitation.

It was seen in this part (1.2) that NPs arrays can be implemented at the front or rear side of the cell to improve its absorption or opto-electronic performance. NPs can also be used as masking (NPs lithography) to form template structure in the devices for light management purposes.

The next part of this chapter will be focused on different techniques used to form point contacts for PV devices.

1.3 Forming point contacts using different techniques in PV devices

Due to their simple architecture, the Aluminum back surface field (Al-BSF) silicon solar cells have dominated the PV market for decades. This structure has a high fill factor (FF) because of the one-dimensional current flow pattern in the base. The performance of silicon solar cells was then improved by reducing the carrier recombination velocity at the back contact. Aiming to do so resulted in the passivated emitter and rear cell (PERC) structure, which is an attractive structure for cost-effective high-efficiency devices. The main feature of such solar cell is that the rear surface is partially contacted by periodical openings in a dielectric film that provides surface passivation. As a result, lower effective surface recombination velocity ($S_{eff, rear}$) values compared to the classical Al-BSF solar cell together with a higher rear internal reflectance are obtained and, consequently, short-circuit current (J_{sc}) and open-circuit voltage (V_{oc}) are improved. This type of solar cells was developed by Blakers et al. in 1988 and produced record efficiency for silicon cells at that time of 22.8 % using thermally grown silicon oxide as a passivating layer [45]. In order to passivate the contacts, a local BSF at the contacted regions was introduced leading to passivated emitter rear locally diffused cell (PERL) by the University of New South Wales in Australia in 1999 with a record efficiency of 25 % [46].

Different techniques are used to form the openings in the rear side of the PERC and PERL solar cells. The next section will be focused on different methods that can be used to form patterning.

To replicate arbitrary patterns at low resolution, nanoimprinting [47], or soft lithography can be sufficient. For higher-resolution arbitrary patterns, “parallel” lithographic techniques such as optical, X-ray, UV, deep UV, and extreme UV lithography are more useful. Ultra-high resolution techniques such as electron beam

lithography [48], focused ion beam lithography [49], and scanning probe lithography [50] provide even higher resolution, but are slow and expensive, and therefore inappropriate for mass production due to their “series” nature. However, if the critical aspect of the pattern to be formed is simply its periodic nature, then simpler, more cost-effective techniques can be used, such a laser interference lithography [51].

1.3.1 Forming point contacts using lithography in PV devices

[Shadow mask] One of the simplest ways of forming a pattern is to use a mask that is locally opened as shown in Fig.1.7.

The mask is placed directly on the substrate during the deposition of the layer. This layer will be deposited in the opened zones of the mask. This latter can be fabricated by laser ablation of a metallic substrate [52], however this method has the inconvenience of forming imperfections in the mask, and therefore a non-conformal pattern. Electrodeposition is another method that can be used to form the mask. It allows a maximum flatness of the mask and has a better resolution, but still worse than that obtained with photolithography and nanoimprint [53].

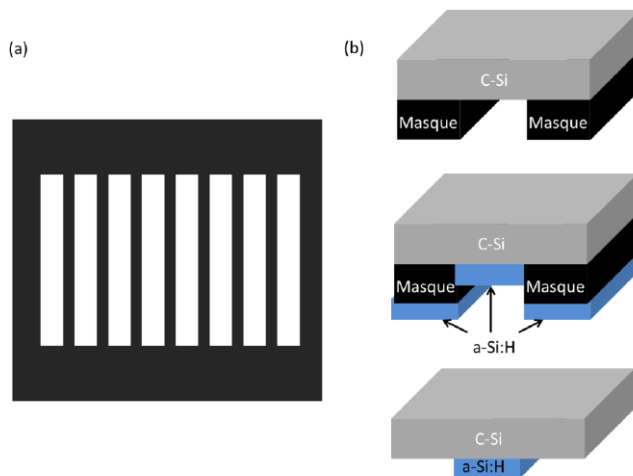


Fig.1.7: (a) Metallic mask used to localized a-Si:H on c-Si substrate, and (b) Schematic illustration of different steps [53].

[Photolithography] Optical lithography has been the mainstay of semiconductor patterning since the early days of integrated circuit production. It has a resolution $\sim 2\text{-}3\ \mu\text{m}$ [54][55]. This technique is based on the use of an UV light, which is illuminated through a mask with a desired pattern to make an exposure on a photo-resist that is coated on the substrate, on which the openings will be formed [55]. Photoresist materials are organic polymers whose chemical characteristics change when exposed to ultraviolet light. When the exposed area becomes more soluble in the developer, the photoresist is positive. While if it becomes less soluble, the compound is considered a negative resist as shown in Fig.1.8 [56].

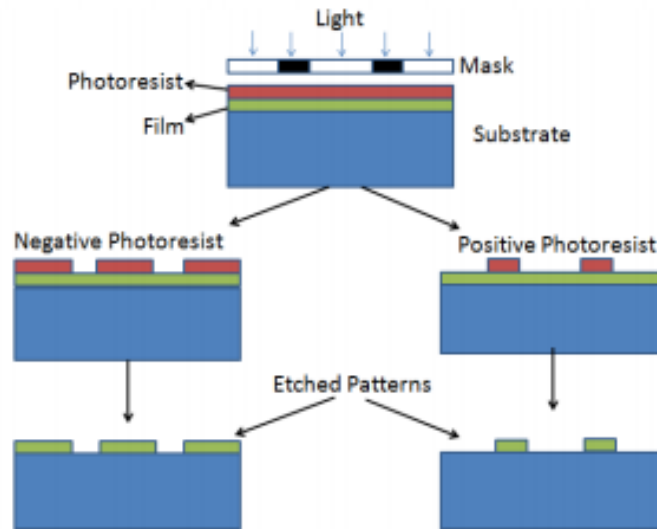


Fig.1.8: Process flow of photolithography process [56].

[Soft lithography] Soft lithography is another technique used to transfer a pattern on a substrate. This is done by using a soft polymer stamp to imprint a solution of molecules with a specific pattern onto a substrate. It requires inexpensive materials and non-specialized equipment. This technique required two main steps: The fabrication of a patterned polymer stamp, and the use of this stamp to transfer molecules within a define geometry on a substrate. Figure 1.9 illustrates the process flow of soft lithography. The advantage of this technique remains on the use of a soft stamp for pattern transferring, which allows a conformal contact between the stamp and the substrate resulting in the capability of patterns transfer on flexible substrates [55]. Its resolution depends on the mask used, but it can be less than 100 nm [57].

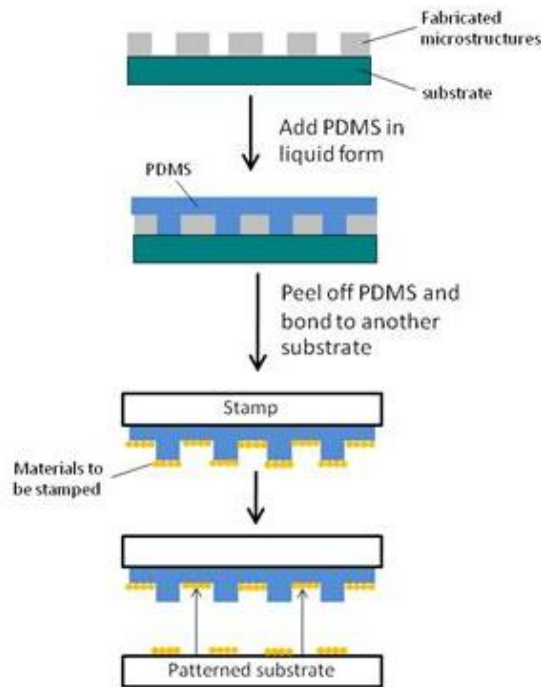


Fig.1.9: Schematic illustration of soft lithography [55].

[Nanoimprint Lithography] Nanoimprint lithography (NIL) has improved a lot since its appearance for the first time in 1995 by Chou, et al. [47], where it mainly targeted micro-electronics. For solar cells, the research using this technique is focused on the optical optimization of the front side of solar cells [58], as well as the back side [59].

NIL is a high-resolution patterning method in which a surface pattern of a stamp is replicated into a material by mechanical contact. It utilizes a hard mold to imprint the pattern into a polymer film by heating it above its glass transition temperature enabling material flow, filling the structure of a mold. This step is followed by a cooling step that solidifies the replicated patterns, after which the mold is removed. The mold is commonly made of quartz and silicon, and the mold features are patterned by conventional lithography techniques such as photolithography and electron beam lithography. A thin residual layer of polymeric material is intentionally left underneath the mold, and acts as a soft layer that prevents direct impact of the hard mold on the substrate and effectively protects the delicate nanoscale features on the mold surface. For most applications, this residual layer needs to be removed by an anisotropic O₂ plasma-etching process to complete the pattern definition [60]. Figure 1.10 shows the schematic illustration of NIL.

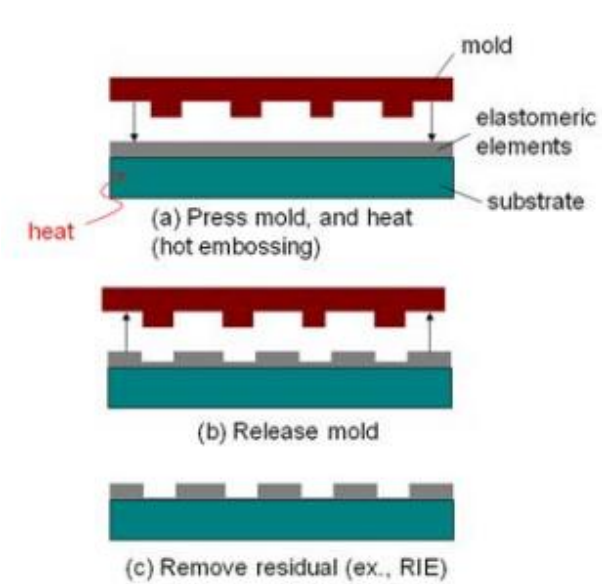


Fig.1.10: Schematic illustration of nanoimprint lithography [55].

Although this technique is considered to be the most cost-effective in producing nanopatterns over large areas with a proven resolution around 20 nm [61], it still has some limitations. It is based on a physical contact of stamps with polymer which can create high pressure on the substrate. Heating and cooling cycles can cause stress on molds, which present problems of alignment for multi-layer fabrication. In addition, surface roughness and defects normally present on the crystalline silicon substrates for PV, can limit its applicability especially when hard stamps are used.

UV-NIL, which appeared in 1996 [62] quickly after the conventional NIL is based on the use of a quartz mold which is transparent to UV light. It is pressed at room temperature with a low pressure on a liquid precursor that can be cured by UV light before the release of the mold. UV-NIL can reduce imprint pressure significantly and avoid time consuming as well as stress induced during high temperature cycle.

Soft UV-NIL, was then proposed to reduce the cost of master fabrication. This technique uses a flexible transparent stamp normally made of poly (dimethylsiloxane) (PDMS) or other flexible polymers that can be easily replicated from a single silicon master mold. This latter is fabricated with conventional lithography

Introduction

techniques. The flexibility of the Polymeric stamp ensures contact with the surface substrate on large surfaces at low pressures, and on flexible substrates [63].

In conclusion, NIL is an interesting technique as it can transfer the pattern on the resist in two steps less than photolithography, if we don't consider the step of mold fabrication.

1.3.2 Forming point contacts using laser in PV devices

Laser has different applications in solar cell fabrication like solar cells edge isolation, and solar modules soldering, welding and ablation. We focus here on their use in forming point contacts.

[Laser ablation] The standard method of producing local openings in the passivation layer is photolithography, which allowed the fabrication of highly efficient cells. However, this technique is not suitable for low-cost mass production. Laser radiation was then used to open locally the passivation layer. Laser has an advantage over mechanical machining as it is a non-contact and chemical free process, however damages on the substrate can result by using this technique.

Short pulse picosecond lasers (~10 ps) are ideal tools for selective patterning of thin films. As the laser-material interaction time is small, this technique eliminates any significant damage to surrounding layers. Engelhart et al. [64] first demonstrated an increased efficiency based on selective removal of the rear surface passivation using ps pulsed laser. They have shown that the direct laser ablation of thermally grown SiO₂ layers using the ultra-short pulse laser permits a complete removal of the dielectric layer with a single laser shot. It also induces a sufficiently small damage level, so that there is no need to etch any damaged Si after laser processing.

Z. Du et al. [65] has confirmed this, by showing that ns and ps lasers processing achieve similar solar cell efficiencies, however a post-laser etching step is crucial to obtain high solar cell efficiency when using ns lasers and can be omitted when ps lasers is being used. In his work, the diameter of the ablated spots was varied between 10 μm and 60 μm with the laser fluence when ns laser was used.

Another way to avoid the damage of silicon underneath the silicon nitride or silicon oxide passivation layer is the use of an a-Si:H layer between the Si and the dielectric to be etched. This a-Si:H layer also plays a role in the passivation. Two studies have shown this structure by using two different types of lasers and by forming ablated spots of 20 μm as diameter. The first study was done by F. Haase, et al. [66] where a layer stack of a-Si:H passivation layer capped with an a-SiN layer was used. A ps laser (λ=355 nm) selectively ablates the a-SiN layer, with a thin layer of a-Si:H left on the Si, avoiding any damage of the substrate.

K. Mangersnes, et al. [67] have used a Q-switched Nd: YVO₄, diode pumped 532 nm laser with ns pulses to ablate a layer of plasma enhanced chemical vapor deposited (PECVD) SiO₂ on silicon. Although ns range laser is believed to be incompatible with processing of high efficiency solar cells, it was shown in this work that by using a PECVD layer of a-Si:H between the Si and the dielectric, it was possible to ablate the SiO₂ in a damage-free way. This is due to the considerable absorption of the laser radiation in the a-Si:H layer.

[Doping by laser] One of the most interesting laser technologies applied in PV materials for PERL structure is the Laser-Fired Contact (LFC) process, in which a metal layer is laser fired through a passivating dielectric film to define ohmic contacts with the semiconductor.

The standard process sequence of contact hole formation following aluminum evaporation and sintering can be replaced by local laser-firing of predeposited aluminum through the dielectric layer. LFC eliminates both the need to open the contact holes in the passivation layer and the sinter step after aluminum deposition.

Introduction

Although the laser ablation process is similar in simplicity, a potential advantage of the new LFC process is the alloying of the aluminum contact into the silicon base, resulting in a beneficial p^+ region. This p^+ region will reduce the recombination in the openings leading to greater solar cell efficiency. The comparison between the LFC process and the standard photolithography process done by E. Schneiderlochner, et al. [68] is sketched in Fig.1.11. In this reference the laser-fired contact diameters are between $80\ \mu\text{m}$ and $100\ \mu\text{m}$ with point pitch set to $1\ \text{mm}$.

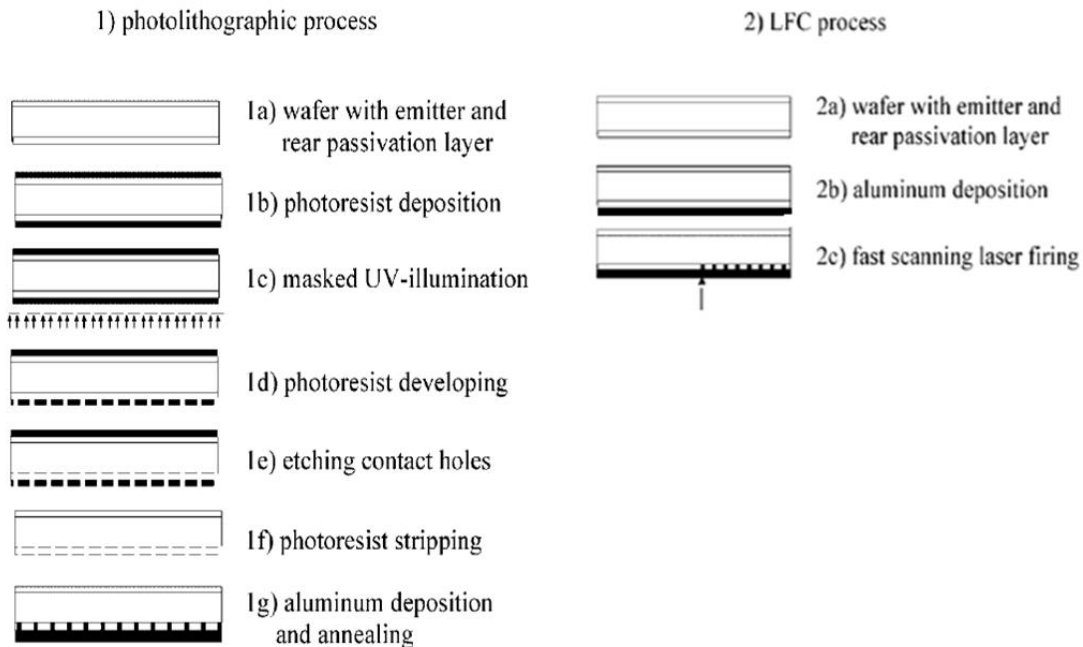


Fig.1.11: Process flow comparison between photolithographic process and LFC process [68].

Different studies have worked on the optimization of the LFC for c-Si solar cells. I. Sanchez-Aniorte, et al. [69] investigated the influence of laser wavelength and fluences on LFC contacts to improve the back contact in c-Si solar cells using fully commercial solid state lasers with pulse width in the ns range. Wavelengths of $1064\ \text{nm}$, $532\ \text{nm}$ and $355\ \text{nm}$ were used in this study to form laser-fired contacts of a diameter between $20\ \mu\text{m}$ and $30\ \mu\text{m}$.

By using only two pulses per point in all cases, it was shown that good electrical conditions can be found at any of the considered wavelengths. Excellent ohmic behavior was achieved for $532\ \text{nm}$ and $355\ \text{nm}$ in a wide parametric range of fluence values, with contact resistance values far below $1\ \text{m}\Omega\text{cm}^2$. As for the laser wavelength of $1064\ \text{nm}$, acceptable conditions were found only in a narrow band of fluence values. $1064\ \text{nm}$ laser showed non negligible potential loss in surface passivation probably due to thermomechanical effects generated in the interaction process [70].

Another study has been published by M. Colina, et al. [71] wherein a comparison between three different strategies to create ohmic micro-contacts was done: 1) evaporated Aluminum LFC, 2) Aluminum foil LFC and 3) Aluminum oxide (Al_2O_3) laser doping (LD). Optimized lasers parameters lead to specific contact resistance in the $1.0\text{-}1.3\ \text{m}\Omega\text{cm}^2$ range for all three strategies with a laser beam radius of $80\ \mu\text{m}$. From the point of view of carrier recombination, best results were obtained for Al_2O_3 LD with an effective contact recombination velocity (S_c) value of $2.5 \cdot 10^3\ \text{cm/s}$, probably due to the lower energy pulse needed to create

the contact. The three strategies were used to contact back side of hetero-junction silicon solar cells, and the electrical response of the fabricated cells confirms that contact quality is good enough to be applied in high-efficiency c-Si cell concepts using any of the three conditions.

In 2015, M. Weizman, et al. [72] have reported the development of a rear-side point-contact scheme for liquid-phase-crystallized silicon on glass solar cells with an amorphous heterojunction emitter, which uses laser for all structuring and contact-post-treatment steps. It was possible to create openings in the back-reflector resist layer by laser ablation, using UV laser, which can enhance the precision and reliability of this process. It was as well possible for both p and n-type absorbers, to use laser firing at the absorber-point-contacts to increase the doping concentration beneath the metal contact, hence decreasing the contact resistance. Using the All-by-Laser Point-Contact Scheme (ALPS) it was possible to reach an efficiency of 11.5 % for a planar n-type absorber, which is close in performance to the currently similar structure prepared by lithography.

The development of LFC process to manufacture PERC solar cells by Fraunhofer ISE in 2016 is a proof that this technique has a potential in industry. For the first time point-contacted solar cells can be manufactured in series using this technique; where the developed LFC procedure can create approximately 100,000 contacts per wafer with a single laser pulse. The laser effect is limited to between 50 and 2,000 nanoseconds to limit the damage in the silicon wafer. Using an innovative system for guiding the laser beams, it was possible to create all the contacts in approximately one second. PERC solar cells made this way, have an improved efficiency level of one percent absolute [73][74].

In the above section, different methods of forming openings in a dielectric were presented. It was seen that the standard method of opening the dielectrics is photolithography. As this technique is not suitable for low-cost mass production, selective laser radiation is used as a cost effective and easy way on the rear side passivation layer to manufacture PERC solar cells. This is due to the unique properties of laser processing; where it eliminates physical contact during processing, thus minimizes the risk of contamination. However, laser ablation can cause damage such as surface melting, head affected zone, micro-cracks, and point defects, which can negatively affect solar cell performance [75]. To achieve damage-free openings, shorter laser pulse widths in the range of ps to femtoseconds are used [76][64][65]. However, these lasers are around seven to ten times more expensive than ns laser systems.

In the next part of this chapter, an alternative, even less precise but more cost-effective approach of forming the openings in the passivation layer will be presented using NPs lithography.

1.3.3 Forming point contacts using NPs in PV devices

[Point contacts for PERC] An innovative way of forming the openings was presented in July 2016 by Chia-Hsun Hsu, et al. which is based on using 40 μm polystyrene spheres spin-coating method for PERC solar cells instead of using the traditional laser ablation process. Effects of PS concentration and post-annealing temperature on PERC performance were investigated. By comparing it to the laser opening technique with the same contact fraction, the PS opening technique can yield a higher minority effective lifetime, a higher implied open-circuit voltage, and a slightly higher short-circuit current. Although the fill factor of the PS opening technique is lower probably due to non-optimized openings distribution, the conversion efficiency of the device is comparable to that prepared via laser opening process [77]. Figure 1.12 shows a diagram comparing both laser and PS spheres opening techniques to form openings in PERC solar cells.

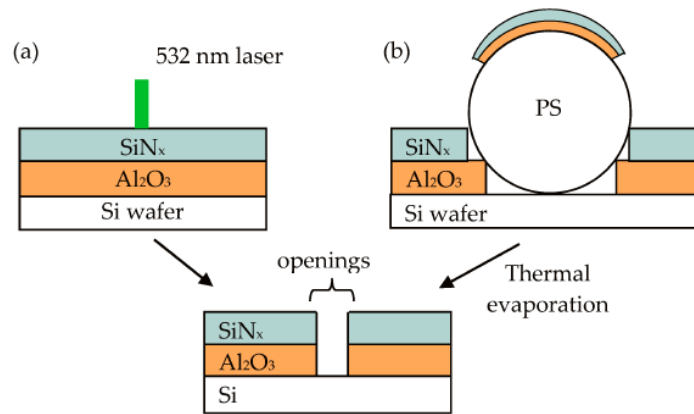


Fig.1.12: Diagram of (a) laser and (b) PS spheres opening technique for PERC [77].

[Point contacts for PERL] One of the main reasons to introduce point contacts in cSi cells is to decrease the rear surface recombination velocity (S_b) and to increase the rear internal reflection (R_b), and consequently enhance the efficiency of the cell. The PERL cSi structure consists of a combination of a highly reflective rear surface passivation layer with micron-sized passivated local point contacts allowing further decrease in the S_b . A novel approach to form the doped openings in PERL solar cells was presented in 2014 by U. Jager, et al., which is a combination of both nanoparticles and laser. A boron doped silicon nanoparticle paste was applied onto the passivation layer and was driven into the wafer by an adapted laser process creating local contact openings in the same step. Sheet resistances $R_{\text{sheet}} < 30 \Omega/\text{sq}$ were observed after laser processing and deep doping up to several microns was realized. These locally doped point contacts allow an excellent ohmic contact, and p-type PERL solar cells with local boron BSF were fabricated, showing efficiencies up to 20.0 % on commercial 6-inch MCz-Si wafers [78].

Another novel approach for doping through the holes of PERC solar cell was done in 2015 by J. Hong et al. [79] using Si paste formed by p-type Si NPs with a diameter of ~ 30 nm and an organic solvent as the source of B. Si paste with different percentages of Si NPs is screen-printed above the openings, and B is diffused into Si through annealing to perform doping through the holes.

[Point contacts for CIGS] It was recently shown by B.Vermang et al. that a similar rear contacting structure can be used to passivate the rear CIGS interface of CIGS solar cells. The advanced cell design, similarly to PERC cSi structure, combines a rear surface passivation layer and a technologically feasible approach to generate nano-sized local point contacts as thin film solar cells have short minority carrier diffusion lengths. Al₂O₃ deposited by atomic layer deposition (ALD) is used to passivate the CIGS rear surface, while the formation of nano-sphere shaped precipitates in chemical bath deposition (CBD) of CdS helps generating point contact openings of about 220 nm in an industrially viable manner [80].

An increase in V_{oc} of 14 mV is observed compared to unpassivated reference cells, due to a decrease in rear surface recombination of a few orders of magnitude [81][82]. Figure 1.13 is a schematic cross-section of the structure with nano-sized local rear point contacts.

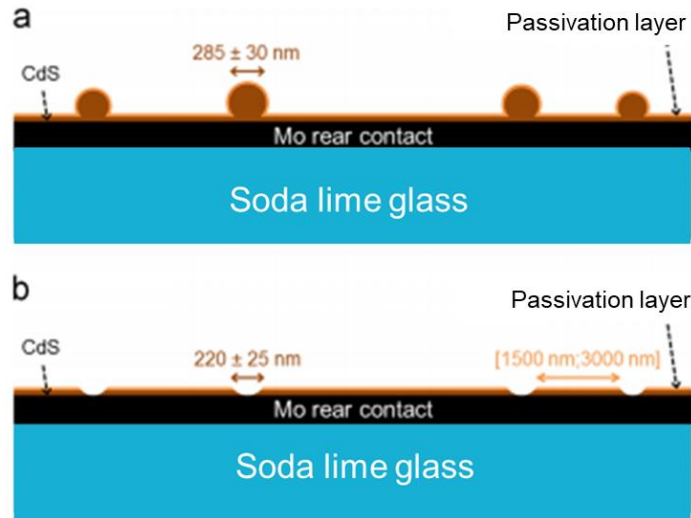


Fig.1.13: Schematic cross-section of (a) surface passivation layer grown on a particle-rich CdS layer, and (b) full SLG/Mo/CdS/passivation-layer substrate having nano-sized point openings after CdS particle removal [81].

Later in 2014, by applying a thick ($\text{MgF}_2/\text{Al}_2\text{O}_3$) rear surface passivation layers, B.Vermang, et al. got an enhancement in reflectivity compared to standard Mo/CIGS rear interfaces. Due to the reflectivity enhancement, an improvement in J_{sc} was seen in addition to the V_{oc} improvement obtained by the decrease in surface recombination. Average solar cell efficiencies of 13.5 % were realized for ultra-thin CIGS absorber layers, compared to 9.1 % efficiency for the matching unpassivated reference cells [80].

It was seen that micro-sized point contacts are normally used for cSi solar cells and nano-sized point contacts can be used for CIGS solar cells to improve their efficiencies. In the next section of this chapter we will explore via analytic and numerical simulations, done by collaboration with MNT group at UPC, the benefits of using nano-sized local point contacts for cSi solar cells instead of micro-sized point contacts.

1.4 Motivation for nanocontacts in c-Si devices

When the rear contact is defined in a point-like pattern (PERC structure), a trade-off between ohmic losses and surface recombination, i.e. between Fill Factor (FF) and V_{oc} is found; the more contacted area fraction (f_c), the lower the ohmic losses, but the higher the surface recombination rate. An optimization is required, trading off recombination losses and resistive losses to maximize the conversion efficiency. Examples of such optimization can be found in the literature [83][84]. Due to the characteristics of the procedure to locally open the contacts in the passivation layer, typical dimensions for the contacts are in the range of tens of microns, while optimized f_c values are well below 10 %. Consequently, the distance between neighboring contacts or pitch (p) is on the order of hundreds of microns, introducing a significant series resistance.

In this section, we will explore the electrical benefits of using contact openings with sizes of 1 μm or below and, consequently, with a pitch shorter than 10 μm . The motivation to do so is that shorter pitches would result in negligible ohmic losses while keeping $S_{\text{eff,rear}}$ under control.

In the first part of this section, a theoretical calculation of this trade-off is done by examining contact geometry and recombination parameters, and will be presented to show the advantage of forming passivated holes in the 1 μm range for PERC/L structure. This is followed by briefly proposing two different device architectures wherein this approach can be applied.

1.4.1 Rear surface modelling

In this section, the rear surface is modelled by studying the variation of the ohmic losses and the $S_{\text{eff,rear}}$ as a function of the contacted area fraction for both microscale and nanoscale openings.

The c-Si substrate characteristics used in the theoretical calculations are a p-type wafer of 1.8 $\Omega\cdot\text{cm}$ with a thickness of 160 μm , which is representative of typical substrates in current commercial devices. For the rear surface modelling, a 3D approach is necessary to define point-like patterns. However, due to the high computational cost of such simulations, we reduce the 3D problem to 1D by applying the equation proposed by Fischer [85], improved by Plagwitz and Brendel [86] and generalized by Saint-Cast et al. [87] that allows us to concentrate the ohmic losses in a condensed parameter R_{base} and an equivalent surface recombination velocity, $S_{\text{eff,rear}}$. Additionally, 3D simulations with ATLAS/Silvaco TCAD were performed at MNT, UPC Barcelona for certain surface configurations to check the analytical results. In particular, R_{base} can be calculated using the following expression [85]:

$$R_{\text{base}} = \rho \cdot \frac{p^2}{2\pi r} \tan^{-1}\left(\frac{2w}{r}\right) + \rho \cdot w \left(1 - e^{-\left(\frac{w}{p}\right)}\right) \quad (1.1)$$

Where r is the contact radius, p is the rear pitch, w is the wafer thickness, and ρ is the substrate resistivity. In Fig.1.14, calculated R_{base} values are presented as a function of f_c for contact radii of 25 and 0.5 μm together with the results of 3D simulations that perfectly agree with the analytical model. In addition, the solid red line indicates the minimum R_{base} value, corresponding to the case where all the current is flowing vertically through the base: $R_{\text{base}} = \rho \cdot w$.

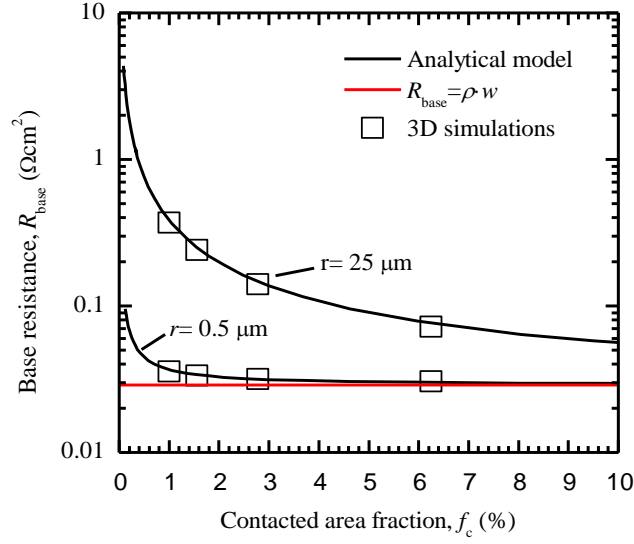


Fig.1.14: R_{base} as a function of the contacted area fraction for $r = 25$ and $0.5 \mu\text{m}$.

As it can be seen, resistance for the case of $r = 0.5 \mu\text{m}$ almost matches this minimum value except for f_c below 2 %. Importantly, these R_{base} values are about one order of magnitude lower than for the case of $r = 25 \mu\text{m}$, introducing a negligible increase in ohmic losses, as expected.

The effective rear surface recombination velocity $S_{\text{eff, rear}}$, is calculated using [85]:

$$S_{\text{eff, rear}} = \left(\frac{R_{\text{base}} - \rho \cdot w}{\rho \cdot D_n} + \frac{1}{f_c \cdot S_{\text{cont}}} \right)^{-1} + \frac{S_{\text{pass}}}{(1 - f_c)} \quad (1.2)$$

Where D_n is the diffusion constant of the minority charge carriers (electrons), S_{cont} is the surface recombination velocity at the contact, S_{pass} is the surface recombination velocity at the dielectrically passivated surface and R_{base} is the base resistance represented by equation (1.1). Since high-efficiency devices are of interest, S_{pass} is kept constant at 1 cm/s while S_{cont} is varied from 5×10^6 cm/s (no passivation at the contacts) to 10^2 cm/s for the two contact radii under study. As it was mentioned, a more sophisticated model is reported in reference [87]. However, under these assumptions, the proposed equation leads to accurate results [87].

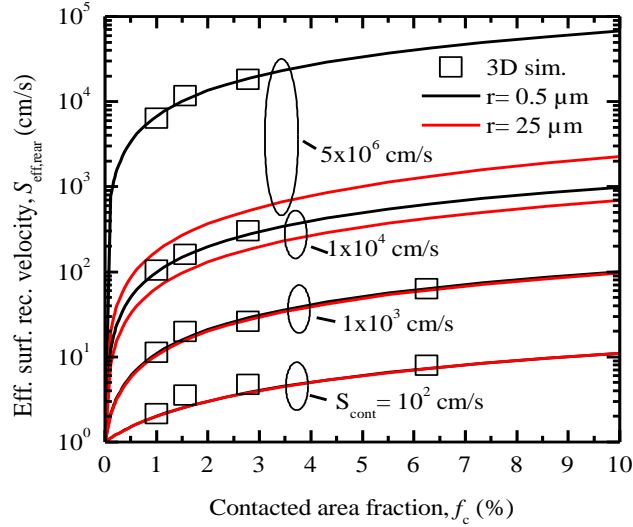


Fig.1.15: $S_{\text{eff,rear}}$ as a function of contacted area fraction for $r = 0.5$ and $25 \mu\text{m}$ and S_{cont} values.

Figure.1.15 shows that for small contacts without passivation, $S_{\text{eff,rear}}$ sharply increases with f_c , while reasonable values can be obtained with $r = 25 \mu\text{m}$. This difference comes from the fact that, despite the percentage of non-passivated surface is the same, for small radius the highly-recombining areas are much closer, less than $10 \mu\text{m}$ compared to $100\text{-}500 \mu\text{m}$ for $r = 25 \mu\text{m}$. As a result, the recombination rate increases, since minority carriers could more easily find contact regions.

The difference in $S_{\text{eff,rear}}$ between both contact sizes decreases when S_{cont} is reduced, being negligible for $S_{\text{cont}} < 1 \times 10^3 \text{ cm/s}$. It can be concluded that from a recombination point of view contact openings in the $1 \mu\text{m}$ range are beneficial for technologies that can achieve passivated contacts. For that cases, similar $S_{\text{eff,rear}}$ than for big contacts can be obtained without significantly increasing the ohmic losses. For example, in these calculations $S_{\text{eff,rear}}$ of 20 cm/s can be obtained for $f_c \approx 2\%$ with a contact technology with $S_{\text{cont}} = 10^3 \text{ cm/s}$ without significantly increasing R_{base} . Obviously, for passivated contacts with very low S_{cont} , a fully contacted area is the best solution, since no additional series resistance is introduced. This is the case of polysilicon contacts [88], tunnel oxide contacts [89] or silicon heterojunction technology [90]. Interestingly, the combination of silicon heterojunction with point-like contacts has already been explored, resulting in an optical improvement in the internal rear reflection, as reported by S. De Vecchi *et al.* in reference [91] for large point contacts.

1.4.2 Impact on solar cell efficiency

In this section, the impact of the rear surface configuration on the solar cell efficiency is explored. Since the 3D problem can be accurately described by $S_{\text{eff,rear}}$ and R_{base} values, as demonstrated in the previous section, PC-1D simulations with a reference PERC/L structure shown in the inset of Fig.1.16 was used. From the optical point of view, as external reflectance (R_{ext}), experimental data shown in Fig.1.16 was used. This data was measured for solar cells developed in MNT group with random pyramid texturized surface and 100 nm SiO_2 passivation [92]. In this measurement, the photons that escape from the semiconductor absorber are also included. Thus, in the simulations, it is considered that no photons are coming out from the solar cell, i.e. a front internal reflection of $R_{\text{in,front}} = 100\%$. At the rear surface, an internal reflectance of $R_{\text{in,rear}} = 94\%$ was considered, which is also a realistic value for a partially contacted surface covered with

a transparent dielectric, for example SiO_2 or SiN_x , covered with aluminum. Finally, a 2.7 % of shadowing was added due to the metal fingers and busbar that introduce $R_{s,\text{front}} = 0.3 \Omega \cdot \text{cm}^2$ in the series resistance [92].

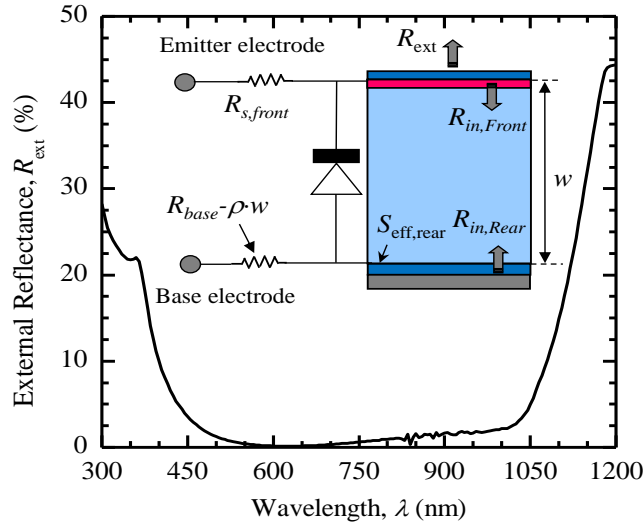


Fig.1.16: Experimental reflectance introduced in PC-1D simulations; (inset) solar cell structure and parameter definition used in PC-1D.

Regarding the front emitter, a Gaussian profile is considered with peak doping density of 10^{19} cm^{-3} and a junction depth of $1 \mu\text{m}$ and a surface recombination velocity of 200 cm/s . This doping profile corresponds to a sheet resistance of $123 \Omega/\text{sq}$ with a saturation current density of 20 fA/cm^2 . This low-doped emitter models the n^+ regions that could be found in-between contacts in a selective emitter configuration. For the contacted regions, a shunt diode is introduced in PC-1D with a saturation current density of 80 fA/cm^2 (see inset of Fig.1.16) resulting in a total saturation current density of the emitter (J_{0e}) of 100 fA/cm^2 . It should be mentioned that different emitter configurations have been tried with different J_{0e} values. Despite the strong impact of this parameter on the maximum V_{oc} values reachable by the device, the main conclusions of the study presented hereby are still valid.

The effect of R_{base} is introduced as a lumped resistor at the rear contact without the $\rho \cdot w$ term (see inset Fig.1.16). Notice that this term corresponding to the geometrical resistance of the base is already included in the calculations done by PC-1D. Finally, $S_{\text{eff,rear}}$ is defined at the rear surface as the Low Level Illumination value in PC-1D.

Simulations with PC-1D were carried out varying the contacted area fraction for the two radii under study. The obtained curves of solar cell efficiency vs. f_c are shown in Fig.1.17.

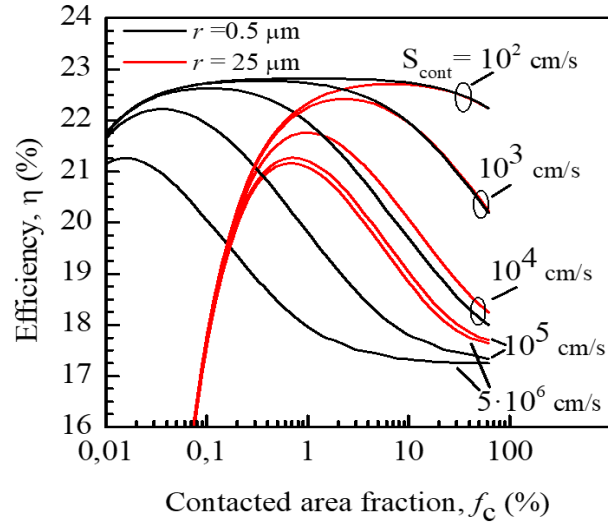


Fig.1.17: Solar cell efficiency vs. contacted area fraction curves obtained by PC-1D simulations.

As it can be seen, due to the trade-off between surface passivation and ohmic losses, an optimum f_c value can be determined in all cases. Additionally, it can be seen that the better the surface passivation at the contacts, the higher the optimum f_c . If the passivation quality at the contacts improves, more area can be contacted without penalizing in surface recombination. Finally, lower S_{cont} values allow higher solar cell efficiencies, as expected.

Focusing on the comparison of small and big contacts, for $S_{\text{cont}} = 5 \cdot 10^6$ cm/s similar maximum efficiencies can be obtained. In the previous section, it was demonstrated that for this case, surface recombination is much higher for small contacts. However, the reduction in ohmic losses due to the short pitches used for such small contacts compensates the poor surface passivation. For S_{cont} values between 10^5 and 10^3 cm/s, the maximum reachable efficiencies are much better for the case of contacts with $r = 0.5$ μm . In this case, the reduction in ohmic losses is a clear advantage, since surface recombination is comparable. Finally, for $S_{\text{cont}} = 10^2$ cm/s similar maximum efficiencies are obtained again. Now, due to the low recombination at the contacts, short pitches, i.e. high f_c values, are not so detrimental for big contacts allowing a compensation of the ohmic losses.

1.4.3 Summary and device architectures

As a summary of this analysis, it can be concluded that the definition of contacts whose size is in the 1 μm range is beneficial for contacts with S_{cont} in the range of 10^5 - 10^3 cm/s, while comparable maximum efficiencies are achievable for small and big contact sizes with both non-passivated and well-passivated contacts. This result demonstrates that small contacts are an attractive solution from the point of view of cell efficiency.

Two different device architectures could be used to form a partially contacted rear surface with such characteristics, and both are shown in figure 1.18. In approach 1 (Fig.1.18 a), conducting passivated contacts formed by a low temperature technique are employed. Good candidates would be transition metal oxides like MoO_x [93] that have demonstrated good carrier selectivity with a low contact resistance. Another feasible possibility is the deposition of boron-doped amorphous silicon films based on silicon

Introduction

heterojunction technology [90]. For this case, aluminum oxide (Al_2O_3) deposited by ALD as the dielectric passivation layer can be a good candidate.

On the other hand (approach 2, in Fig. 1.18 b) a BSF-type structure at the contacts can be obtained by a p^+ region created either by thermal diffusion or ion implantation. Now, a thick thermal SiO_2 simultaneously works as a passivating film and as a mask for the doping process.

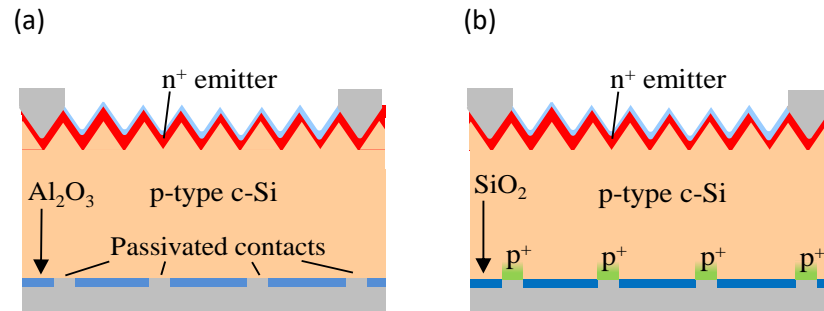


Fig.1.18: Two potential rear contact configurations to define partially contacted surfaces with contacts in $1\ \mu\text{m}$ range; (a) approach 1: low temperature passivated contacts and Al_2O_3 passivation; (b) approach 2: p^+ regions fabricated by either thermal diffusion or ion implantation and thermally grown SiO_2 passivation.

1.5 Summary and Thesis Outline

In this chapter, the importance of NPs for different applications and especially for PV applications was shown. As well, different methods of forming point contacts for PV devices were presented. The conventional methods (Lithography and laser) used to form openings in a dielectric were first presented, followed by a more innovative method based on NPs to form point contacts for cSi and CIGS solar cells.

Numerical simulations were then presented to explore the potential advantages of using nanoscale contact openings instead of microscale opening. It shows that the definition of contacts whose size is in the 1 μm range is beneficial for contacts with S_{cont} in the range of 10^5 - 10^3 cm^2/s , while comparable maximum efficiencies are achievable for small and big contact sizes with both non-passivated and well-passivated contacts.

In this PhD work, I explore the possibility of using **nanoscale contact openings** instead of microscale opening, with an eye towards PERL structures as the final device structure. The thesis is therefore organized as follows:

Chapter 2 presents the experimental tools used during this thesis,

Chapter 3 develops and explores processes to enable the formation of such contacts using various nanosphere dispersion, thin-film deposition, and layer etching processes. It will present the different methods used to deposit the NPs, to etch them and to remove them after being covered by a metallic or a dielectric layer.

Chapter 4 will then present the characterization done on the nanoholes and three different approaches (A, B, and C) used to form the nanoholes in thin (< 50 nm) and thick dielectric layers (≥ 50 nm). In the last part of this chapter, a test structure involving the formation of point contacts on NIP a-Si:H cells will be presented.

Chapter 5 considers the application of nano-sized point contacts on crystalline silicon by exploring localized doping through the nanoholes formed. It will present experimental results demonstrating doping through nanoholes by diffusion and ion implantation.

Chapter 2: Experimental techniques

| | | |
|---------|--|----|
| 2.1 | <i>Deposition techniques</i> | 28 |
| 2.1.1 | Spin coating | 28 |
| 2.1.2 | Radio frequency-Plasma-enhanced chemical vapor deposition..... | 28 |
| 2.1.3 | Matrix Distributed Electron Cyclotron Resonance-PECVD..... | 31 |
| 2.1.3.1 | Electron Cyclotron Resonance-PECVD | 31 |
| 2.1.3.2 | Matrix distributed-ECR PECVD, Venus | 32 |
| 2.1.4 | Atomic Layer Deposition (ALD)..... | 33 |
| 2.1.5 | Thermal oxidation..... | 35 |
| 2.1.6 | Thermal evaporation | 36 |
| 2.1.7 | RF magnetron sputtering..... | 36 |
| 2.1.8 | Reactive Ion Etching (RIE)..... | 37 |
| 2.1.9 | Doping..... | 38 |
| 2.1.9.1 | Doping by diffusion | 38 |
| 2.1.9.2 | Doping by ion implantation | 40 |
| 2.2 | <i>Characterization techniques</i> | 41 |
| 2.2.1 | Spectroscopic ellipsometry | 41 |
| 2.2.2 | Secondary electron microscopy (SEM) | 42 |
| 2.2.2.1 | Challenges using different detectors | 44 |
| 2.2.3 | Atomic force microscope (AFM)..... | 47 |
| 2.2.3.1 | AFM..... | 47 |
| 2.2.3.2 | Conductive probe atomic force microscope (CP-AFM) | 50 |
| 2.2.4 | J-V measurements..... | 51 |
| 2.2.5 | Electro-chemical capacitance voltage (ECV) profiling | 54 |
| 2.2.6 | Dynamic light scattering (DLS)..... | 54 |

Experimental techniques

In this PhD work, different experimental setups were used to form holes in dielectric layers and dope the substrate through them. Three different approaches (detailed later in ch.4), were used to form holes in the dielectrics. After fabricating the samples, a number of characterization tools were used to analyze the formed holes, the doping through the holes, and the devices employing the holes.

In the first part of this chapter, I present the techniques used to deposit the dielectrics and the masking layers, and those used to perform the plasma etching and the doping through the holes. In the second part the characterization tools used to characterize the formed holes before and after doping are presented.

2.1 Deposition techniques

2.1.1 Spin coating

Spin coating is one of the most common techniques for applying thin films to substrates. The advantage of this technique is its ability to quickly and easily produce uniform films, ranging from a few nanometers to a few microns in thickness.

The working principle of a spin coater is simple. The substrate is fixed on a substrate holder by vacuum suction. A small quantity of the coating material is dropped in the middle of the sample. The substrate is then simply rotated at very high speed and the film spreads homogeneously under the action of centrifugal forces as shown in Fig.2.1.

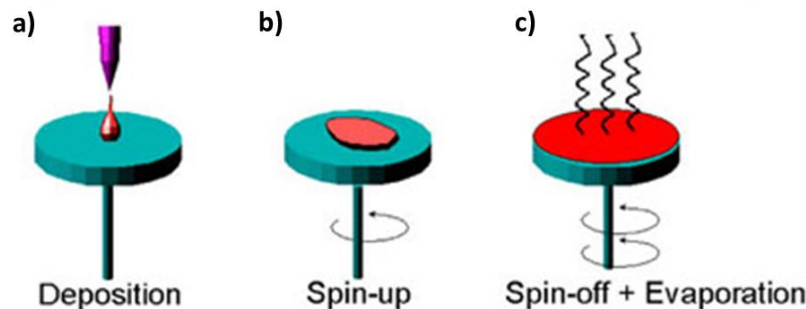


Fig.2.1 : Schematic illustrating spin coating technique key steps [94].

[In this thesis] Spin coating was used in this PhD to deposit NPs on Si and metallic substrates. Details are shown in ch.3.

2.1.2 Radio frequency-Plasma-enhanced chemical vapor deposition

Vacuum-based thin film deposition techniques can be divided in two main categories: i) depositions based on a physical process such as evaporation and sputtering; and ii) depositions based on chemical processes, known as chemical vapor deposition (CVD).

Plasma-enhanced chemical vapor deposition (PECVD) is a sort of CVD. In a CVD process, gas precursors are decomposed and react on a hot substrate via chemical reactions which require quite high temperatures (500-800 °C) to take place. In the PECVD process, an electrical discharge is used to decompose the precursors, generating reactive species such as radicals or ions which will induce chemical reactions and

Experimental techniques

result into the growth of a film at lower temperature (100-350 °C). The PECVD technique is therefore low temperature process which enables the growth of films with good adhesion and uniformity properties.

The plasma in the PECVD deposition is generally created by a voltage at RF (AC) frequency or DC, creating a discharge between two electrodes. A simple DC discharge can be created at a few torr between two conductive electrodes, and may be suitable for deposition of conductive materials. However, insulating films will quickly extinguish this discharge as they are deposited. The RF-PECVD has an advantage over the DC-PECVD in its capacity of depositing insulating films and to perform depositions on insulating substrates.

Plasma deposition of thin films covers a wide range of materials and applications [95][96]. More particularly, PECVD is widely used for the growth of dielectric films like Si_3N_4 and SiO_2 [97] a-Si:H [98]. It can also be used for more exotic depositions like $\mu\text{c-Si:H}$ [99], and c-Si epitaxy [100]. For a-Si:H deposition, the dissociation of silane was first reported by Ogier in 1879 [101]. However, the interest for this material started after hundred years later after discovering the possibility of doping it, by Chittick and Spear and Le Comber [102], [103]. Using RF-PECVD at a 13.56 MHz frequency is today the most common way to deposit a-Si:H thin films and have allowed for uniform a-Si:H deposition on a substrate up to 5.7 m². A schematic diagram of a PECVD deposition reactor is shown in Fig.2.2.

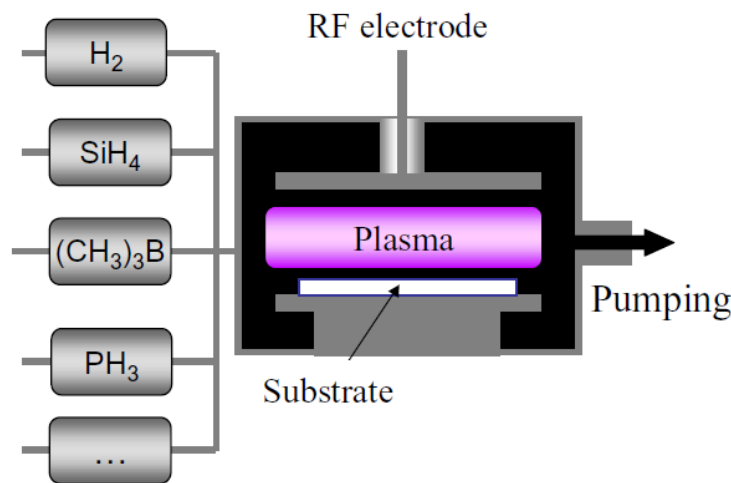


Fig.2.2: Schematic diagram of plasma enhanced chemical vapor deposition reactor [104].

The deposition reactor consists of a gas injection system, a vacuum chamber and of a parallel plate, capacitively coupled plasma (CCP) system; one electrode is RF powered and the other is a grounded and heated substrate holder.

This method is advantageous compared to other CVD deposition techniques because of the following benefits:

- Deposition at low temperature can be done, because the dissociation of gas precursors occurs due to collisions with high-energy electrons.
- Dense and smooth films can be deposited due to the energy brought to the growth zone by accelerated ions present in the plasma.
- a-Si:H can be easily doped p or n type or even transformed into alloys (a-SiC:H, a-SiO_x:H, etc.) by adding other gases.

Experimental techniques

-Stacks can be easily deposited by varying the gas content and plasma parameters without having to remove the sample outside the reactor between two different film depositions.

Even though a wide choice of gas precursors exists for the a-Si:H deposition (Si_2H_6 , SiF_4 , SiCl_3H , etc...), SiH_4 has been and is still the most widely studied.

The plasma formed between the two electrodes is an ionized gas which is macroscopically neutral. A transition region arises between the plasma and the electrodes and it is called sheath. As the energy of the power supply is mostly coupled to electrons, they are the most energetic species in the discharge and would just move out of the plasma if there wasn't a potential barrier preventing them from leaving the plasma. On the other hand, ions are much less mobile because of their higher mass. They only experience an average potential, whose distribution is shown in Fig.2.3. This potential distribution implies that negatively charged species in the plasma (electrons, negative ions and negatively charged powders) experience a potential barrier which prevents them from leaving the plasma. On the other hand, positively charged ions and particles will be accelerated to the walls, thus leading to the so-called ion bombardment [104].

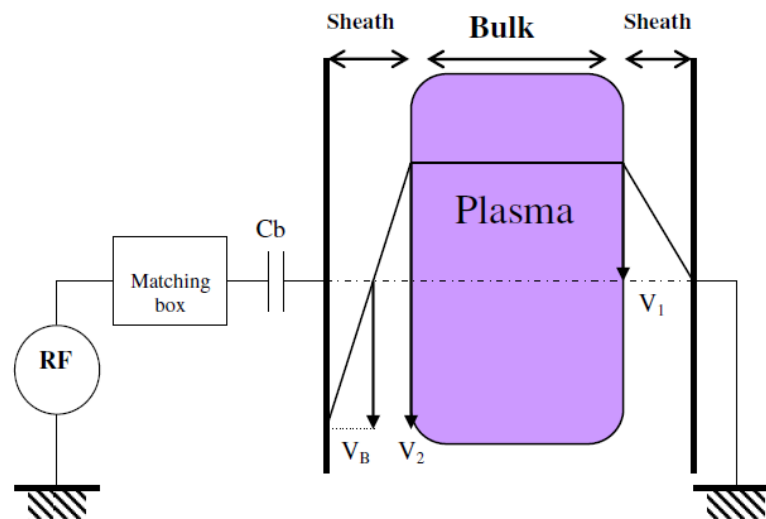


Fig.2.3: Average potential distribution in capacitively coupled RF glow discharge reactor [104].

It can be seen from Fig.2.3 that the potential in the plasma discharge is positive. This potential drop in the region of the sheath and becomes zero at the grounded electrode. However, if the area of the grounded electrode is much larger than the RF electrode, the plasma discharges becomes asymmetric and the RF electrode will be negatively biased ($-V_B$). This will lead to a difference in the energy of the impinging ions if the substrate is placed on the powered or grounded electrode.

However industrial systems become more symmetric as the size of the substrates and consequently that of the RF electrode increases. The self-bias on the RF will then tends to zero, while the plasma potential will increase, leading to higher ion energy and possible damage of the substrates used and the growing films. This damage will be more serious if RF power is increased to increase more the deposition rate.

To avoid this effect, other deposition techniques, hot-wire CVD, photo-CVD and microwave plasmas can be used to decrease ion energy. However to achieve an increase in the deposition rate, the power coupled

to the discharge should be increased, and this will lead to the formation of powders [105] A compromise should be found in order to achieve high deposition rate while keeping low ion energy without powder formation. More information on this deposition can be found in this reference [104].

[In this thesis] ND200, NEXTRAL [106] in Thales was used during this PhD to deposit intrinsic a-Si:H and n-a-Si:H. as well as p-aSiC to create a-Si:H cells. More details on this deposition will be shown in chapter 4.

Another RF-PECVD reactor was used in the Micro and Nano Technologies research group (MNT), Polytechnic University of Catalonia (UPC), Barcelona-Spain from Elettrovava S.p.A to deposit intrinsic a-SiC_x:H at room temperature. More details on this deposition will be shown in chapter 3.

2.1.3 Matrix Distributed Electron Cyclotron Resonance-PECVD

In this section, we describe the working principle of the Matrix Distributed Electron Cyclotron Resonance Plasma Enhanced Chemical Vapor Deposition (MDECR-PECVD). We first review the working principle of the (ECR-PECVD) before introducing the MDECR-PECVD reactor “Venus” that we have used in our experiments.

2.1.3.1 Electron Cyclotron Resonance-PECVD

In this section, the basic principal of the Electron cyclotron resonance (ECR) is first reviewed.

The trajectory of an electron in a uniform static magnetic field of strength B_0 without the presence of an electric field is a helicoidal trajectory with a constant radius around the magnetic lines. This cyclotronic motion of the charged particle in the magnetic field is characterized by the radius and the frequency f_{Larmor} and r_{Larmor} respectively, given by:

$$f_{Larmor} = \frac{q_e B_0}{2\pi m_e} \quad (2.1)$$

$$r_{Larmor} = \frac{m_e v_e}{q_e B_0} \quad (2.2)$$

Where q_e is the electron charge, m_e is the electron mass and v_e is the electron velocity in the plane perpendicular to the magnetic field.

By supplying microwave power to the plasma, a linearly polarized electric field is superimposed on the magnetic field and will contribute to the electron motion. With its frequency in the microwave range $f_{MW}=2.45$ GHz, a resonance will exist when the electric field frequency is equal to the Larmor frequency:

$$f_{Larmor} = f_{MW} \quad (2.3)$$

This means that the motion of the electron in the field created by the magnets is resonant with the electric field generated by the microwaves and that the resonant absorption will take place at the specific value of the magnetic field of 875 Gauss. The electric field will constantly increase the electron velocity, and so its energy. When the electron energy exceeds the excitation, dissociation or ionization threshold of gas molecules, inelastic collision will happen and will result in creation of the reactive species (excited molecules, radicals or ions, respectively). To effectively couple electric field energy from the field to the

Experimental techniques

electrons in resonant regime, the pressure should be low, typically below 10 mTorr to decrease the collision frequency to allow electrons to gain enough energy. On the other hand, at very low pressures, below 1 mTorr, production rate of active species drops as well, so optimal pressure range for ECR-PECVD is considered to be between 1 and 10 mTorr.

Electron Cyclotron Resonance Plasma Enhanced Chemical Vapor Deposition (ECR-PECVD) is a high plasma density, low-pressure deposition technology used for the deposition of dielectric, functional and optical thin films for different applications. It offers fast growth rates due to high ionization and gas dissociation levels at low pressures. It can also perform film depositions at low temperature (below 100°C) with good quality, due to considerable ion flux of low energy ions, which differentiates it from the RF-CCP. The most common geometry, called divergent ECR (or NTT type) consists in injecting the microwaves by a waveguide through a dielectric window in a cylindrical chamber surrounded by electromagnets. A magnetic confinement is provided by the axial magnetic field and the microwave power is absorbed in the resonant region where the electron cyclotron frequency matches the microwave frequency. The ion energy can be as well independently controlled by biasing the substrate holder.

To apply ECR technology for thin film fabrication, several different designs of ECR reactors have been developed [107], including divergent ECR, microwave plasma disk reactors, distributed ECR, integrated ECR and multi-dipolar (or matrix distributed) ECR reactors.

2.1.3.2 Matrix distributed-ECR PECVD, Venus

The idea of multipolar magnetic field confinement was first proposed by Sadowski in 1967 in a spherical configuration for controlled thermonuclear reactions [108]. Its first realization for the production of large uniform low temperature plasmas is attributed to Limpaecher and MacKenzie in 1972 [109].

MDECR reactors were developed as a combination of multipolar magnetic confinement and microwave plasma in order to overcome the difficulties of DECR [110]. They use microwave antenna applicators equipped with SmCo magnets integrated into the antennas' ends, which are installed in a matrix configuration, providing multipolar confinement. This reduces the losses of energetic electrons creating zone of uniform intense plasma in front of the wafer. It allows deposition on large surfaces, and can be expanded to larger areas by increasing the number of antennas.

[In this thesis] An MDECR reactor, Venus, was used in this PhD. The microwave discharge, at 2.45 GHz, is sustained by a set of sixteen water-cooled linear antennas in a four by four matrix, each carrying on its end a permanent rare-earth magnet, with S and N polarities alternating in rows and columns. To power the microwave antennas, two magnetron generators generating up to 2000 watts each were used, each one supplying eight antennas via waveguide-to-coaxial 8-way splitters. This reactor is shown schematically in Fig.2.4. More information can be found in ref [111].

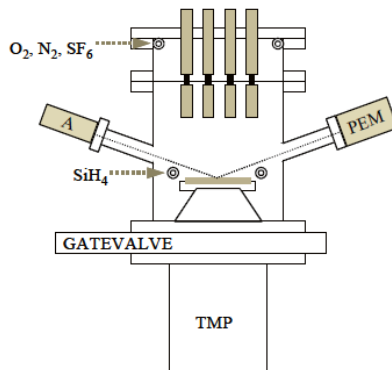


Fig.2.4 : Schematic of Venus reactor [111].

The Venus reactor was used in this PhD to deposit dielectrics of SiO_2 and SiN_x at room temperature, with deposition rates of 4.8 \AA/s and 6.8 \AA/s respectively. More details about these depositions will be given in chapter 3. It was also used as a tool to etch polystyrene nanoparticles using O_2 plasma. More details about this etching using Venus will be given in chapter 3.

2.1.4 Atomic Layer Deposition (ALD)

Atomic Layer Deposition (ALD) offers precise thickness control, in theory down to the atomic scale. It is designed to deposit perfectly uniform thickness films, even deep inside pores, trenches and cavities of surfaces. It can be used to deposit passivation layers for cSi samples, such as Al_2O_3 . The main difference of Al_2O_3 in comparison to other passivation schemes is its high fixed negative charge density (10^{12} - 10^{13} cm^{-2}) located at the $\text{Al}_2\text{O}_3/\text{Si}$ interface, which produces effective field-effect passivation by repelling electrons from the interface [112]. A post-deposition annealing step is required to reduce the interface defect density D_{it} (10^{10} - $10^{12} \text{ eV}^{-1}\text{cm}^{-2}$) and achieve a good cSi surface passivation performance. Al_2O_3 has acted as a good surface passivation for both lightly and highly doped n- and p- type cSi substrates [112], [113] where S_{eff} values below 3 cm/s have been achieved [114], [115], [116].

The principle of this deposition is like CVD except that the precursors are never present simultaneously in the reactor as in the CVD case. These precursors react with the substrate surface one at a time in a sequential, self-limiting, manner. A thin film is slowly deposited through the repeated exposure to separate precursors. Fig.2.5 illustrates one ALD reaction cycle for Al_2O_3 deposition.

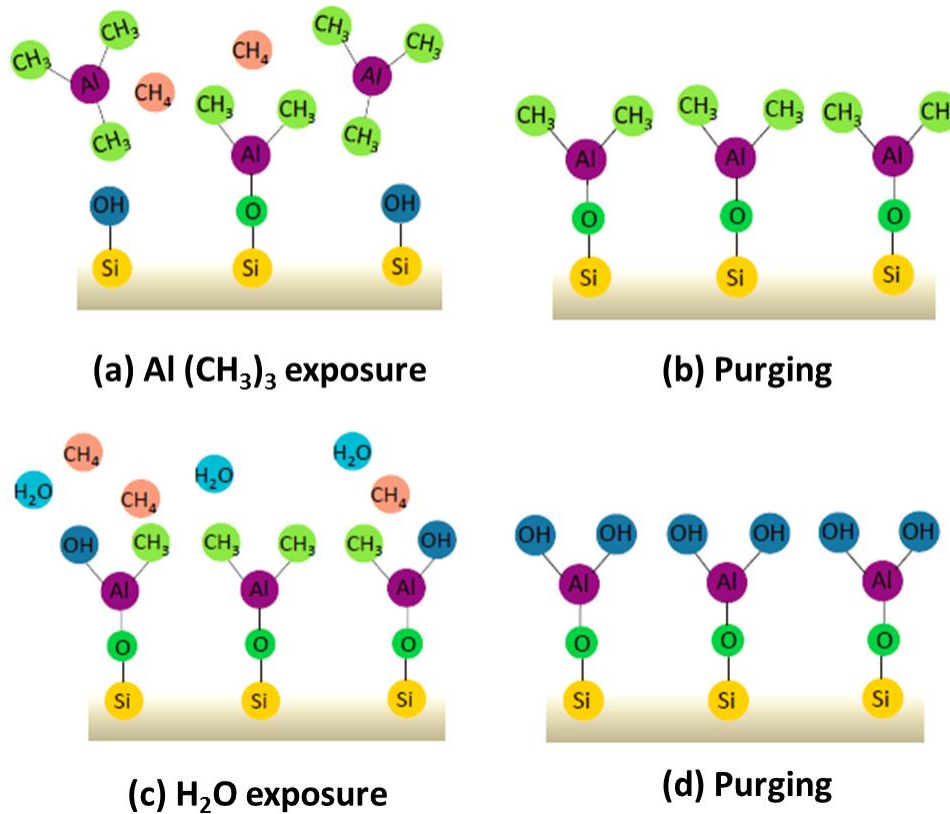


Fig.2.5: Schematic illustration of one Al₂O₃ ALD reaction cycle [116].

H₂O is adsorbed on the sample surface and with silicon form: Si-O-H. The four steps defined in the reactor are:

- A 0.005 sec pulse of an aluminum precursor, trimethylaluminum ($[Al(CH_3)_3]$, TMA), reacts with hydroxyl groups –OH.
- The excess precursor and reaction products (CH₄) are purged out of the deposition chamber via a 5 sec purge with inert N₂.
- The co-reactant, H₂O, is introduced into the chamber and reacts with the adsorbed TMA molecules during 0.015 sec to form a monolayer of Al-O bridges and hydroxyl surface groups
- Non-reacted H₂O and CH₄ are purged out of the deposition chamber via a 5 sec purge with N₂.

The amount deposited per cycle (step 1 to 4) is expressed as growth rate, GPC (Growth per cycle) and is 1.1 Å. Reaction cycles are repeated until the desired amount of material is been deposited.

[In this thesis] The ALD machine used in this PhD is a Savannah S200 from Cambridge Nanotech and is in the MNT lab at UPC, Barcelona.

2.1.5 Thermal oxidation

Thermal oxidation is a way to passivate silicon wafer by growing a thin layer of silicon dioxide. This technique forces an oxidizing agent to diffuse into the wafer at high temperature and react with it. It is usually performed at a high temperature between 800 and 1200 °C.

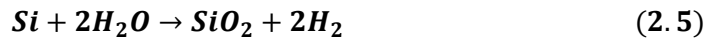
It allows an excellent surface passivation which is mainly attributed to high quality of the cSi/SiO₂ interface that reduces the density of states at the interface (~10⁹ cm⁻²eV⁻¹). Furthermore positive charge densities within the dielectric layer (up to 10¹¹ cm⁻²) [117] cause a weak field effect passivation [118] and lead to S_{eff} values as low as 2 cm/s (substrate n-type) and 12 cm/s (p-type) [119].

There are two methods of thermal oxidation:

Dry oxidation, wherein the wafer is exposed to oxygen at 1000 °C, and a high quality oxide is produced. The oxidation reaction is the following:



Wet oxidation, when a mixture of high-purity oxygen and hydrogen at 1000 °C is used, giving water vapor environment. A higher growth rate can be achieved in this case, but with a lower quality compared to dry oxidation, therefore this oxide can be used to form thicker oxide layers. The oxidation reaction is the following:



Thermal oxide incorporates silicon consumed from the substrate and oxygen supplied from the gas phase. Therefore, it grows both down into the wafer and up out of it. If a bare silicon surface is oxidized, 44 % of the oxide thickness will lie below the original surface, and 56 % above it, as can be shown on Fig.2.6.

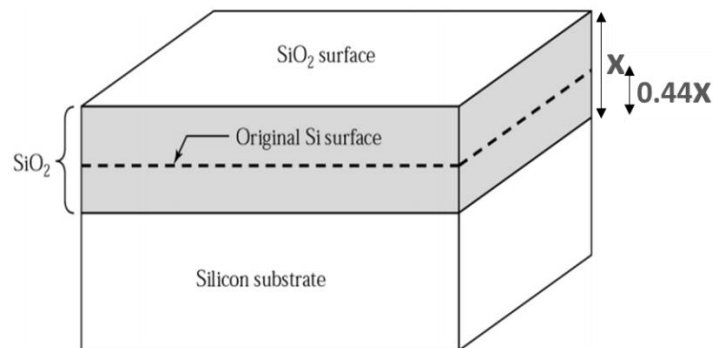


Fig.2.6 : Growth of silicon dioxide by thermal oxidation [120].

Thermal oxidation can also be used as a good diffusion mask for common silicon dopants like Boron (B), Phosphorous (P), Arsenic (As) and Antimony (Sb).

[In this thesis] In this PhD, dry thermal oxidation is carried out to grow a SiO₂ layer that is mainly used to mask the boron diffusion, as will be seen in chapter 5.

2.1.6 Thermal evaporation

Thermal evaporation is a physical vapor deposition that allows depositing materials, mostly metals, at relatively high deposition rate (up to 1 $\mu\text{m}/\text{min}$).

Evaporation involves two basic processes: a hot source material evaporates and condenses on the substrate. The evaporation takes place in a vacuum, which means that vapors other than the source material are almost entirely removed before the process begins.

The evaporator consists of a vacuum vessel where the samples are facing down, in front of a crucible filled with small pieces of the metal that will be evaporated. The vessel is later pumped down to a pressure around 5×10^{-6} mbar. This process is based on Joule-effect to heat the source material by applying a high current on the crucible, until the metal pieces melt (around 660 $^{\circ}\text{C}$ for Al), evaporate and condense on the surface of the sample. Since this process occurs in vacuum, the particles have a long mean free path allowing them to reach the sample surface directly without reacting with the background gas. The thickness of the deposited metal is controlled by a quartz crystal microbalance.

[In this thesis] Thermal evaporation was used in this PhD to evaporate aluminum on NPs of polystyrene, as will be shown in chapter 3. As this technique is an anisotropic deposition, this will result in a shading effect when evaporated on the NPs, which will lead to an easier removal of the NPs afterwards.

2.1.7 RF magnetron sputtering

Sputtering deposition is a physical vapor deposition (PVD) method of thin film that involves ejecting material from a "target" onto a substrate. The power is supplied by a RF generator operating at a frequency of 13.56 MHz, connected to the cathode with an impedance matching network with variable capacitors. It is based on the creation of a plasma between a cathode which is the target and an anode which is the vacuum chamber. The plasma is created by applying a voltage to the target, as seen in Fig.2.7.

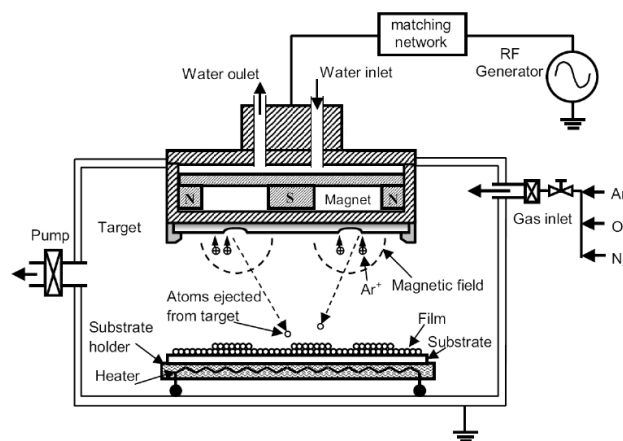


Fig.2.7: Schematic representation of RF magnetron sputtering system [121].

The ionized gas usually used is inert such as Ar for a non-reactive sputtering deposition, or a mixture of Ar+O₂ for a reactive sputtering deposition. The feature of the magnetron discharge is the use of a closed magnetic field to trap electrons, enhancing both the efficiency of the initial ionization process and allowing a plasma to be generated at lower pressures.

Experimental techniques

The Ar^+ ions are accelerated towards the cathode by the electric field and bombard the target. The neutral species sputtered from the target are deposited on the substrate after a straight-line trajectory.

[In this thesis] This technique was used to deposit indium tin oxide (ITO), silver (Ag) and ZnO using an Alliance concept DP650 sputtering system.

2.1.8 Reactive Ion Etching (RIE)

Reactive Ion etching (RIE) is a high resolution (when a mask is used) dry etching technique for material etching using a chemically reactive plasma. It is a highly controllable process that can process a wide variety of materials, including semiconductors, dielectrics, and some metals. The advantage of RIE, compared to other etching techniques, is that this process can be highly anisotropic due to the vertical delivery of reactive ions that reach the sample, allowing for much finer resolution and higher aspect ratios.

A typical RIE system may use an inductively coupled plasma (ICP) to generate the ions. ICP provides a high ion density; hence fast etch rates, while allowing separate control of ion density and ion energy, giving a low damage capability. One such system is the Oxford Instruments Plasma Technology Plasmalab System 100 ICP etcher in ICFO, the institute of Photonic Sciences, Spain. A schematic of this etch chamber is given in Fig.2.8.

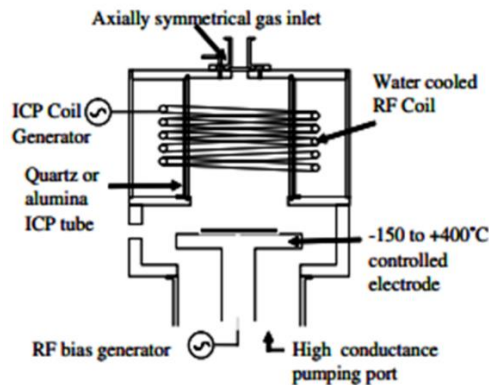


Fig.2.8: Schematic of Plasmalab System100 ICP180 tool [122].

RF power of 13.56 MHz is applied to both the ICP source (up to 3000 Watts) and the substrate electrode (600 Watts) to generate the etch plasma. By measuring the DC bias generated on the lower electrode, the ion energy at the substrate is monitored, and it is further controlled by the RF power supplied to this electrode. The lower electrode holding the sample can be thermally controlled. The substrate temperature can be controlled to an accuracy of $\pm 1^\circ\text{C}$ over a temperature range of -5°C to 400°C . This range can be extended to -150°C to 400°C with the addition of a supply of liquid nitrogen. The etch result is affected by the substrate temperature as it controls the volatility of the etch species, affecting the etch rate, selectivity, profile and the surface roughness. The pressure range of the system can be varied between 1 mT and 100 mT [123].

[In this thesis] The above ICP etcher was used to etch the SiO_2 locally by masking it with an aluminum layer; more details will be found in chapter 4.

Another RIE system was also used, namely a Nextral NE 110 located in the Thales Laboratory in Palaiseau, France. It was used to etch local dielectrics of silicon oxide and silicon nitride. It is a CCP reactor with

almost equal area electrodes, and a plasma source generated at 13.56 MHz. Its maximal power is 300 W and the pressure range is from 10 to 100 mTorr. More details about the etching will be present in chapter 4.

2.1.9 Doping

Doping refers to the process of intentionally introducing impurities into a semiconductor to change its electrical properties, namely to vary the number of electrons and holes.

Doping creates n-type material when semiconductor materials from group IV are doped with group V atoms. The materials from group V elements in the periodic table have 5 valence electrons in their atoms. As only 4 valence electrons are needed from each atom to form the covalent bonds around the silicon atoms, there will remain an extra free valence electron. Thus, the number of electrons present will increase. Phosphorous, Arsenic, Antimony, Bismuth, and Lithium can be used as n-type dopant of silicon. The schematic of the n-doped silicon is present in Fig.2.9.a.

Doping creates p-type material when semiconductor materials from group IV are doped with group III atoms. The materials from group III elements in the periodic table have 3 valence electrons in their atoms. As not enough electrons are present to form 4 covalent bonds around silicon, there will remain an extra hole. Thus, the number of holes present will increase. Boron, Aluminum, Nitrogen, Gallium, and Indium can be used as p-type dopant of silicon. The schematic of the n-doped silicon is present in Fig.2.9.b.

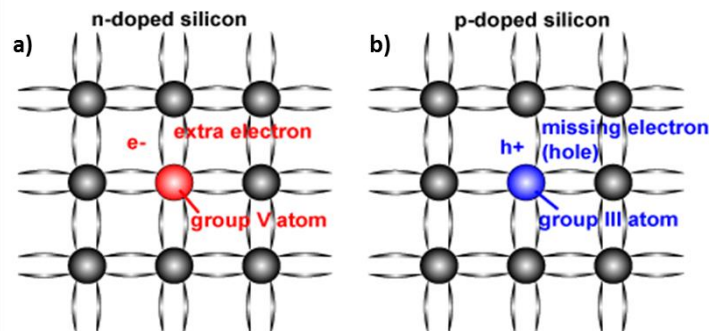


Fig.2.9: (a) Schematic of n doped silicon, and (b) of p doped silicon [124].

Doping was done during this PhD by both diffusion and ion implantation.

2.1.9.1 Doping by diffusion

Diffusion of impurities is typically done by placing semiconductor wafers in a high-temperature quartz-tube furnace. The dopants can be introduced in several ways, including solid sources, liquid sources and gaseous sources. The process temperature usually ranges between 800 °C and 1200 °C for Si.

Diffusion in a semiconductor can be visualized as the atomic movement of the dopant atoms in the crystal lattice by vacancies or interstitials. Figure 2.10 shows the two basic atom diffusion models in a solid (The open circles represent the host atoms occupying the equilibrium lattice positions, and the solid dots represent the impurity atoms).

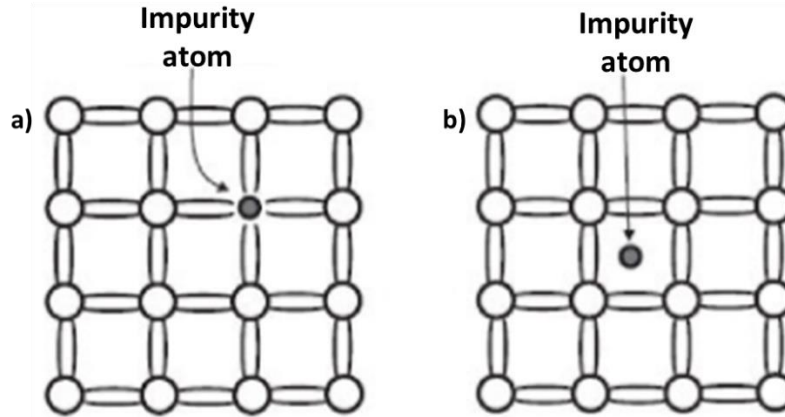


Fig.2.10: (a) Substitutional and (b) interstitial impurity atoms [4].

At elevated temperatures, the lattice atoms vibrate around the equilibrium lattice sites. There is a finite probability that a host atom will acquire sufficient energy to leave the lattice site and become an interstitial atom, thus creating a vacancy. When a neighboring impurity atom occupies the vacancy site, as shown in Fig.2.10.a, the mechanism is called vacancy diffusion. If an interstitial atom moves from one place to another without occupying a lattice site, as shown in Fig.2.10.b, the mechanism is called interstitial diffusion [4].

In both cases, the diffusion is governed by Fick's law of diffusion, which can be written as:

$$F = -D \left(\frac{\partial C}{\partial x} \right) \quad (2.6)$$

Where F is the number of dopant atoms passing through a unit area in a unit time, C is the dopant concentration per unit volume, and D is the diffusion coefficient or diffusivity. D is a strong function of temperature:

$$D = D_0 e^{-\frac{E_a}{kT}} \quad (2.7)$$

Where D_0 is the diffusion coefficient in cm^2/s and E_a is the activation energy in eV. For the interstitial diffusion model, E_a is related to the energy required to move dopant atoms from one interstitial site to another (between 0.5 eV and 2 eV in Si). For the vacancy diffusion model, E_a is related to both the energies of motion and the energies of formation of vacancies (between 3 and 5 eV) [4].

The maximum dopant concentration is limited by the solid solubility limit of the dopant atoms in the substrate [4]. Boron has a solubility limit of 10^{20} cm^{-3} in silicon, and phosphorous has a limit of 10^{21} cm^{-3} . As a result, depending on the number of dopants produced by the precursors and the length of the subsequent drive-in, excess boron or phosphorous can be left behind on the surface. This can produce a boron-silicon or phosphorous-silicon phase that may be difficult to remove. This is most easily handled by performing an oxidation to convert boron-silicon and phosphorous-silicon to borosilicate or phosphosilicate glass, which can then be easily etched away later by an HF step [125].

[In this thesis] Solid dopant sources were used, which consist of slices of boron nitride containing the dopants (planar diffusion sources (PDS) from Saint-Gobain Advanced Ceramics) and placed in-between

Experimental techniques

the wafers to perform boron doping. This diffusion was performed in MNT lab at UPC, Barcelona. To mask the dopants from some regions of the sample, a SiO_2 layer was used as a mask.

2.1.9.2 Doping by ion implantation

Ion implantation is the introduction of energetic, charged particles into a substrate such as silicon. Implantation energies are between 1 keV and 1 MeV, resulting in ion distributions with average depths ranging from 10 nm to 10 μm .

Ion implantation can be used for semiconductor doping, where the main advantages are in its more precise control and reproducibility of impurity doping and its lower processing temperature compared with those of the diffusion process.

A representative schematic of an ion implantation system is shown in Fig.2.11.

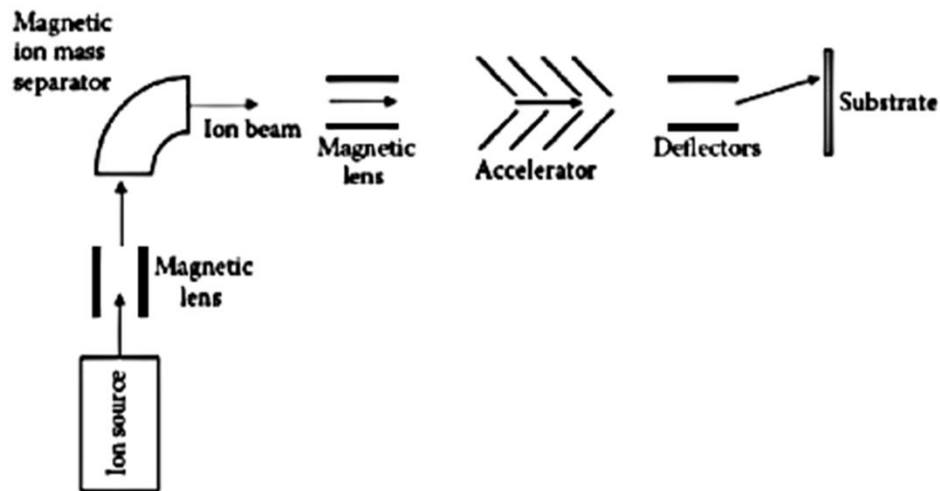


Fig.2.11: Schematic of an ion implantation system [4].

The ion source is generated by vaporizing the source atoms, ionizing them in a plasma and accelerating them. An extraction voltage, around 40 kV, causes the charged ions to move out of the ion-source chamber into a mass analyzer. The magnetic field of the analyzer is chosen such that only ions with the desired mass-to-charge ratio can travel through it without being filtered. The ion beam is then collimated, focused, and accelerated by a large voltage (typically several hundred kV). Deflectors are used to fine tune the beam position before it exits the gun and bombards the front face of the substrate [4].

The energetic ions lose energy through collisions with electrons and nuclei in the substrate and finally come to rest at some depth within the lattice. The average depth can be controlled by adjusting the acceleration energy. The dopant dose can be controlled by monitoring the ion current during implantation. The principle side effect is the damage of the semiconductor lattice caused by ion collisions since silicon atoms are knocked from their sites. In this stage of the process, a small percentage of the dopants are active. To recover the crystal lattice and activate the dopants, a high temperature annealing step is required, which will as well lead to dopant diffusion.

[In this thesis] IRMA in CSNSM was the ion implantation equipment used for the implantation of boron in Si in chapter 5. The type of ion source used is Bernas-Nier; the elements to be ionized are introduced in the source in the form of gases or vapors and the ionization is achieved in a plasma maintained by electrons emitted by a hot cathode, allowing the ionization of almost all the elements. This equipment allows material modification at depths less than 500 nm. It operates from 5 to 190 kV, and produces an ion current that varies from few tens to few hundred microamperes [126][127].

2.2 Characterization techniques

2.2.1 Spectroscopic ellipsometry

Spectroscopic Ellipsometry (SE) is an optical, non-destructive, and contactless technique for investigating the optical properties of thin films, giving their refractive index and the dielectric function. By modelling the data acquired from SE, it is possible to characterize the composition, roughness, thickness, crystalline nature, and uniformity of the layer, as well as other materials properties. It can be used either in-situ, or ex-situ.

SE is based on the principle of detecting the change in the polarization state of the light upon reflection on the surface of a medium. Modelling is used to interpret this change as a stack of materials. In perfect conditions, SE is able to estimate thin film thickness with a precision of $\pm 0.3 \text{ \AA}$ [128]. Figure 2.12 shows a schematic representation to explain the principle of ellipsometry.

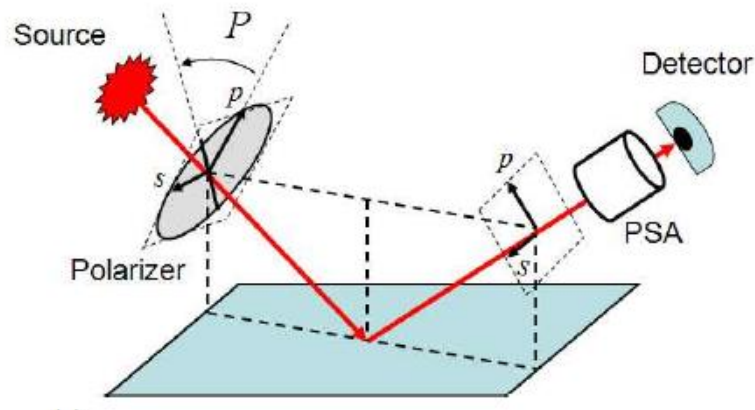


Fig.2.12: Schematic representation of a standard ellipsometry [121].

A source of light sends a linearly polarized signal with a specific incident angle on the substrate. The reflected light from the substrate passes through an analyzer and then a detector to determine its polarization. The light polarized parallel to the plane of incidence is said to be p-polarized while the light polarized perpendicular to this plane is called s-polarized.

This polarization change is quantified by the amplitude ratio, ψ and the phase difference, Δ . Those two parameters are defined using this formula:

$$\rho = \frac{r_p}{r_s} = \tan(\psi) \exp(i\Delta) \quad (2.8)$$

Where r_p and r_s are the complex Fresnel reflection coefficient of the parallel (r_p) and perpendicular (r_s) components of the light in the plane of incidence and ρ is called the complex reflectance ratio.

[In this thesis] The SE used during this PhD (shown in Fig.2.13) is an ex-situ, UVISEL, and phase modulated spectroscopic ellipsometer with a scanning range going from 1.5 to 4.7 eV. It was used to check the thickness of the dielectric deposited by PECVD.



Fig.2.13: UVISEL based at LPICM.

2.2.2 Secondary electron microscopy (SEM)

Secondary electron microscopy (SEM) is based on focusing a high energy beam of electrons on the sample to create an image. The electron beam with an energy ranging from 0.2 KeV to 40 KeV is focused by one or two condenser lenses to a spot about 0.4 nm to 5 nm in diameter. The electrons in the beam interact with the sample, producing various signals that can be used to obtain information about the surface topography and composition.

The energy exchange between the electron beam and the sample results in the reflection of high-energy electrons by elastic scattering, and emission of secondary electrons (SE), X-Ray emission and Auger electrons by inelastic scattering. Each of these dissipated electrons can be detected by specialized detectors, and all these phenomena are illustrated in Fig.2.14 with the depth of the different responses.

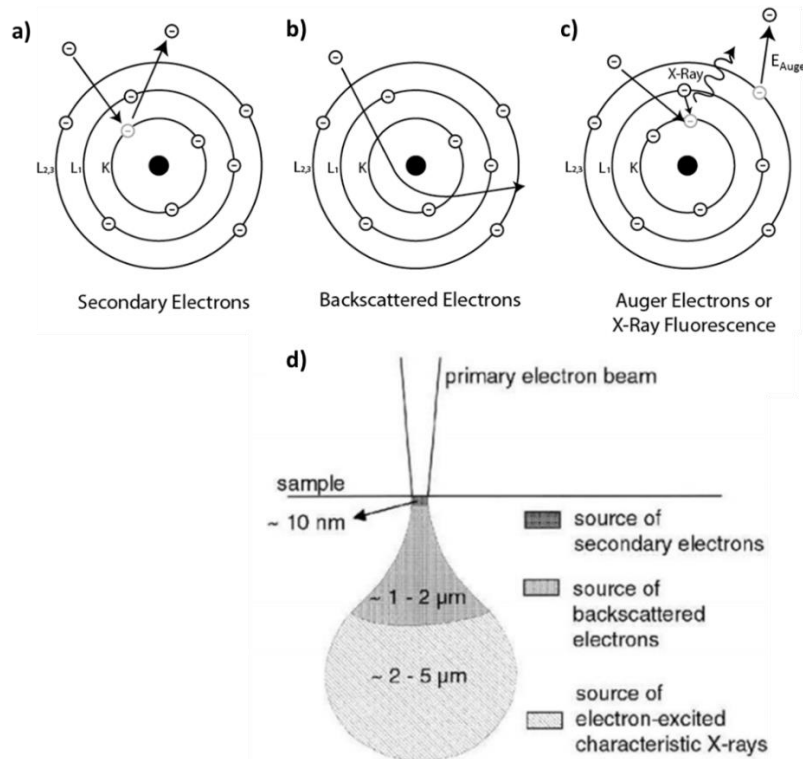


Fig.2.14 : Mechanisms of emission of (a) secondary electrons, (b) backscattered electrons and (c) Auger electrons or X-ray, and (d) Excitation volume showing how deep common interactions can take place [129].

[Secondary Electrons, SE] Inelastic scattering occurs when an electron is ejected from the K-shell of the sample atoms and emitted outside of the sample. This is called a secondary electron (SE) and they have low energies ($< 50\text{eV}$) and therefore would originate within a few nanometers from the sample surface. Steep surfaces and edges tend to be brighter than flat surfaces, because the emission of SE is much higher when the electron beam hits the surface obliquely than when it hits it perpendicularly. Therefore, SEM is routinely used to image the size, shape, texture of three dimensional objects. Using the signal of secondary electrons, an image resolution less than 0.5 nm is possible.

[Backscattered Electrons, BSE] Elastic scattering occurs when the electron interacts with the electric field of the atom without losing a significant amount of energy but changing its direction. Backscattered electrons (BSE) consist of high-energy electrons originating in the electron beam that are reflected or back-scattered out of the specimen interaction volume. Since heavy elements backscatter electrons more strongly than light elements, they appear brighter in the resulting image, and BSE can be used to analyze chemical composition of the sample.

[X-Ray emission and Auger electron] Another way of dissipating the extra energy resulting from the interaction between the electron beam and the sample is through X-Ray emission. After expelling an electron from the low orbital of the atom, an electron from a higher orbital will take its place and lose energy through X-ray emission. Although most often this energy is released in the form of an emitted photon, the energy can also be transferred to another electron, which is ejected from a high orbital of the atom; this second ejected electron is called an Auger electron.

Both X-Ray emission and Auger electrons are used to perform elemental composition analysis.

2.2.2.1 Challenges using different detectors

Hitachi S-4800 (at Ecole Polytechnique, France) is the main SEM setup used in this thesis. This SEM has two secondary electron detectors; the upper and the lower.

The upper detector (SE(U)) is placed above the objective lens and secondary electrons (SE) are detected through the magnetic field of the lens. The lower secondary electron detector (SE(L)) is placed in the specimen chamber, where a large amount of the signal is due to backscattered electrons (BSE). Signals from these two detectors can be selected individually, or mixed together (SE(M)).

Figure 2.15 shows a simplified schematic illustration of a SEM setup with the position of the detectors already mentioned above. In this figure, "SE" indicates the "SE(U)" detector, and "SE+BSE" indicates the "SE(L)" detector.

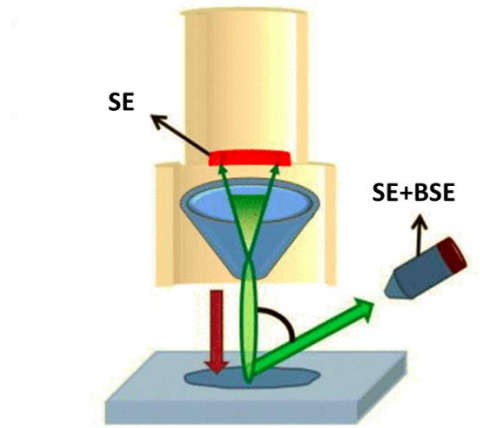


Fig.2.15: Schematic illustration showing detectable signals by SEM.

[SE(U) detector] This upper detector (indicated as SE) is primarily used to detect secondary electrons. It should be mentioned that there is a possibility to also detect BSE with the upper detector using the Hitachi S-4800; however, in our case, we have chosen the option of detecting a pure SE signal, as this gives high resolution surface information, voltage contrasts, high edge contrasts, but is sensitive to specimen charging.

[SE(L) detector] The lower detector signal contains secondary electrons and very low angle back scattered electrons. Images formed with this detector show a natural surface topography, less sensitive to specimen charging with less edge contrast. Spatial resolution is generally lower than that given by the upper detector because backscattered electrons are generated from a wider and deeper specimen area [130].

The "SE (M)" setting, which is a mixture of both detectors, was as well used in chapter 5 together with the SE(U) detector to scan the same area of cSi samples locally doped with boron.

Another SEM setup was used during this PhD, a Zeiss Neon 40, located in CRNE, Barcelona, Spain. This SEM also has two main detectors. The detector that is perpendicular to the sample surface and which detect pure SE is called the "inLens" detector. A second detector, which is mounted to the chamber wall and which detects both SE and BSE is called the SE2 detector [131]. This setup was used to scan some samples shown in ch.3.

Two examples are presented in Fig.2.16. The first one is cSi on which PS NPs were heated after being covered with 30 nm a-SiC_x:H taken at the same spot by Zeiss Neon 40 SEM setup using both inLens (detecting SE) and SE2 (detecting SE+BSE) detectors. Another cSi sample consists of holes formed on its

surface and which are locally doped with boron. The SEM images are taken by Hitachi S-4800 SEM using both detectors: SE(U) (detecting SE) and SE(M) (Detecting SE+BSE). (More details on this sample will be shown in ch.5).

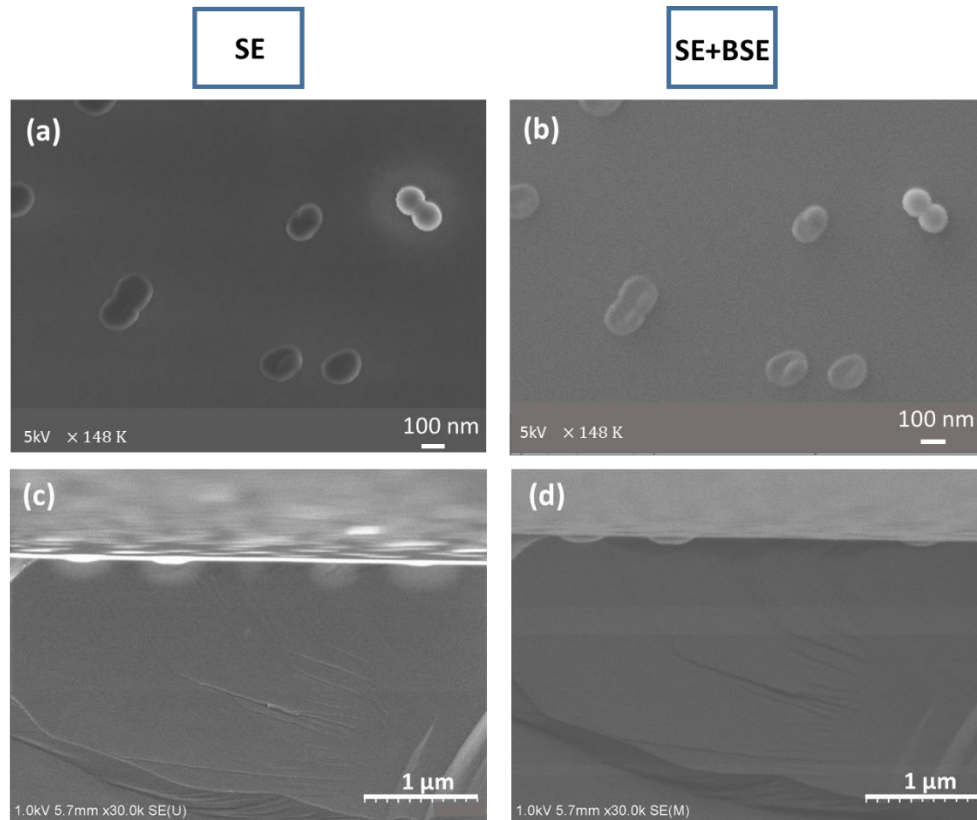


Fig.2.16: SEM images taken by Zeiss Neon 40, using (a) inLens detector (detecting SE), (b) SE2 detector (detecting SE+BSE). SEM images taken by Hitachi S-4800, using (c) SE(U) detector (detecting SE) and (d) SE (M) detector (detecting SE+BSE).

On the SEM images taken by the detectors for SE, the edges appear clearer. Furthermore, there is more contrast between the heated NPs and the surrounding for Fig.2.16.a and between the doped holes and the surrounding for Fig.2.16.c. On the SEM images taken by the detectors detecting SE+BSE, one can only see the topography with a small contrast between the different parts due to their different composition.

[p and n type contrast] Other than the topographical and composition contrast, surface potential contrast has also been studied using SEM, because of the sensitivity of the SE to the electrostatic and chemical potential of the sample. The contrast between p and n doping observed by SEM was reported by many groups, where they observed p-type regions brighter than n-type or intrinsic regions [132][133] [134] [135] [136][137][138] [139] [140] [141].

Previous work had aimed at explaining why the intensity of SEs emitted from a semiconductor is a sensitive function of the doping. El-Gomati et al. [142] have argued that doping contrast is due to a polymerized hydro-carbon contamination layer on the surface of samples in the SEM. However, this explanation is not relevant to the majority of the works as surfaces are instantly covered with water.

Howie et al. [143], and Sealy et al. [144] proposed that local external electric fields are important for doping contrast. This theory was as well re-explained by Tsurumi et al. [138]. The model is that the contrast is caused by local external electric fields above the sample surface, called patch field, due to carrier

concentration. This electric field is positive above the n-type region and negative above the p-type region. Hence, the SEs above the n-region experience acceleration toward the specimen by electrostatic force, whereas those above the p-region are accelerated away from the specimen. Therefore, the collection efficiency of the SEs from the p-type region increases and that from the n-type region decreases. This explains the brighter p-type contrast and the darker n-type contrast observed across the p-n junction in the SEM images. However, upon consideration, this explanation is not supported by experimental evidence, as samples should appear “grey” far from the junction due to a weak electric field there, which is not what we observe in reality.

Castell et al. [145] and Perovic et al. [132] [146] proposed a more plausible explanation that attributes this phenomenon to escape energy difference for valence electrons and to surface band-bending. The explanation proposed by Perovic et al. is shown in Fig.2.17.

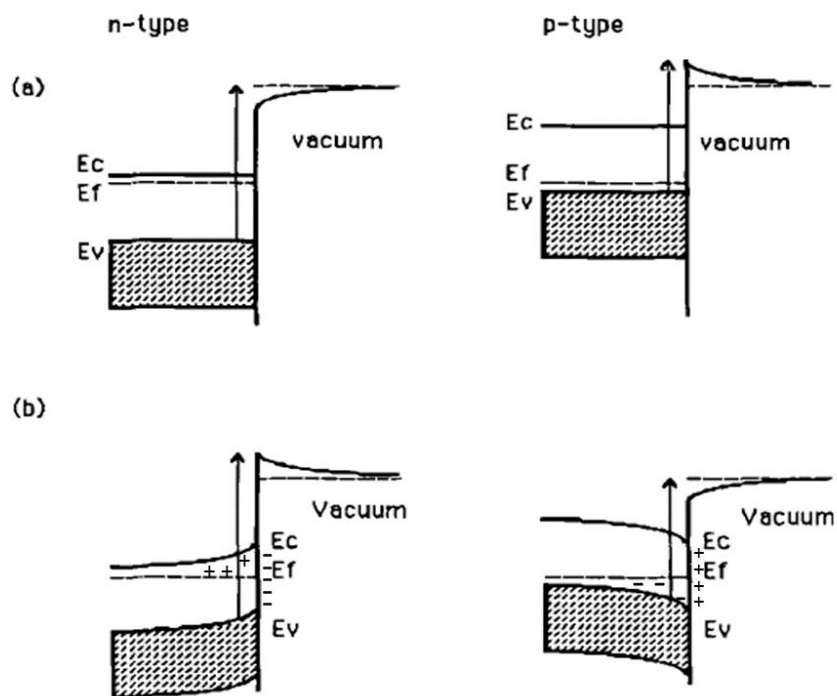


Fig.2.17: Energy band diagrams comparing energy barriers for SE emissions in n-type versus p-type material in (a) case of no surface pinning of the Fermi level and (b) that when pinning occurs [143].

In the case where there is very low density of surface states, an electronic flat band condition exists resulting in a bulk-like band structure at the surface (Fig.2.17.a). Although the barrier height outside the p-region is somewhat higher than the potential at infinity, its height above the densely occupied valence states is less than it is in the n-type regions. SE can then be excited above the barrier with less energy transfer from the primary beam in the p regions which thus appear bright.

However, under normal conditions, semiconductor surfaces are not “clean” but contain surface defects and adsorbates following cleavage in air giving rise to surface states. This will result in band-bending near the surface leading to Fermi level pinning within the band-gap. This effect accentuates that of the energy barrier for valence electrons. This case is presented in Fig.2.16.b for both n-type and p-type materials.

Experimental techniques

As the depletion length depends on the doping concentration in the material, two cases were presented by Perovic et al. [132]:

In the small depletion length limit ($L < \lambda$), where λ is the penetration depth of primary electrons, the height above the densely occupied valence states in p-type regions is less than it is in the n-type regions. Therefore, a smaller energy transfer is required to excite an electron from the valence band into the vacuum in p-type material. The energy required for SE emission in p-type material is thus decreased so that the total SE yield is increased relative to the n-type material.

In the opposite limit, where the depletion length is large ($L > \lambda$), the minimum excitation energy remains less in the p regions than in the n regions, but two further factors (the band bending effect and the graded barrier effect) additionally reinforce the effect of the energy barrier for valence electrons.

The first effect is explained by the internal electric fields near the surface having opposite polarities as seen in Fig.2.16.b. In the p-type semiconductor, the electric field tends to accelerate electrons towards the surface while the electric fields in the n-type material tend to push the electrons back into the semiconductor.

The second effect is explained by the height and shape of the surface barrier in the vacuum which is different for p and n-type materials, where in the p-doping case the barrier is lower (Fig.2.16.b).

As these two effects presented above, for the case where ($L > \lambda$), reinforce the brighter contrast observed for the p-type region, the use of small voltages during the SEM images capture will make a stronger contrast between the p and n-type regions

The advantage of SE images remains in its immediate generation of useful two-dimensional dopant information without complex sample preparation or damaging of the surface. SEM images can give an indication of dopant type and location, but it is not capable of extracting quantitative information. However, Chee et al. [147] have established a quantitative model for doping contrast where he took into consideration both surface band-bending and the effects of patch fields.

[In this thesis] SEM is one of the characterization tools used in chapter 5 to analyze boron doping through nanoholes formed in a silicon substrate (one example was already seen in Fig.2.16.c and d).

2.2.3 Atomic force microscope (AFM)

2.2.3.1 AFM

The atomic force microscopy (AFM) belongs to a series of scanning probe microscopes invented in the 1980s. This series started with the scanning tunneling microscope (STM), which allowed the imaging of surfaces of conducting and semiconducting materials. AFM was the last one of the series, invented by Binnig, et al. [148]. This setup allows the imaging of the topography of conducting and insulating surfaces, in some cases with atomic resolution. A lateral resolution as low as 30 Å and a vertical resolution less than 1 Å have been reported [148][149][150]. However, the radius of the tip used to scan the sample surface can limit the lateral resolution of the measurement making it in the order of tens of nanometers. The tip has a nano-scale apex curvature that varies between 1 and 100 nm. It is at the extremity of a micro-scale probe that is at the end of a cantilever. Figure 2.18 represents a schematic of basic AFM operation.

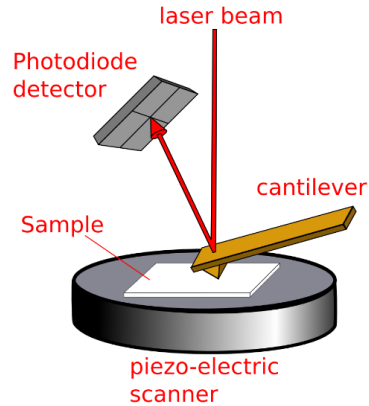


Fig.2.18: Schematic of basic AFM operation [151].

While scanning, the interaction between the tip and the sample can be analyzed by the cantilever motion. This motion can be detected, by focusing a laser on the flat top of the cantilever, which is reflected on a four-quadrant photo-detector. Any bending or oscillation of the cantilever will cause changes in the direction of the reflected beam, and these direction changes will be tracked by the detector.

To measure the height at the nano-scale, the AFM requires a feedback signal. This latter can be either the cantilever deflection if a contact mode is chosen, or the amplitude/frequency of the cantilever oscillation if a tapping or non-contact mode is being used. The signal must be maintained constant during the scans, and this is done using a vertical piezoelectric scanner.

AFM measurements can be done in three different modes: a contact mode, a tapping mode, and a non-contact mode. The interaction forces between the tip and sample in all the three modes can be identified in a force displacement curve as a function of the distance from the sample at which they operate, as shown in Fig.2.19. When the interatomic distance is quite large, weak attractive forces are generated between the tip and the sample. The attractive forces increase gradually as the atoms are brought closer to each other's until the atoms become so close that the electron clouds begin to repel each other electrostatically. Because of this repulsive force between the atoms, the attractive forces diminish until it becomes zero when the distance between the atoms reaches a couple of angstroms.

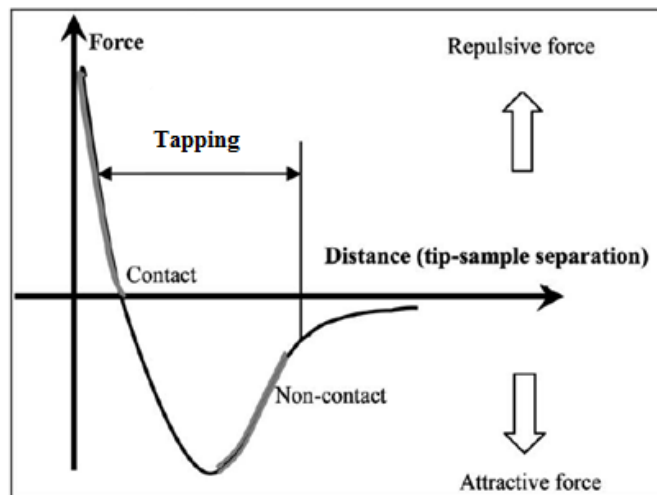


Fig.2.19: Interatomic force variation versus distance between AFM tip and sample[152].

[Contact mode] The contact mode was used in the first AFM in 1986 [148]. In this mode, the tip is in contact with the sample through the whole scan. The interaction forces between the tip and the sample are mainly repulsive and the motion of the cantilever can be modeled using Hooke's law. As the cantilever is brought even closer to the surface, increasingly repulsive force takes over and causes the cantilever to deflect away from the surface. The feedback signal in this case, is the bending of the cantilever, also called deflection.

[Non-contact mode] The non-contact mode was invented in 1987 [153]. In this mode, the cantilever is oscillating without touching the surface. It is about 50-150 Å above the surface, therefore the tip only interacts through Van der Waals forces with the sample and this can be an advantage of degrading neither the tip nor the sample. The cantilever is oscillating, and the amplitude or frequency of its oscillations is the feedback signal that is used to know the distance to the sample.

However, because of the low intensity of Van der Waals force and the sensitivity to the water adsorbed on the surface, the non-contact mode is usually used under ultra-high vacuum (UHV), making it a less versatile AFM mode.

[Tapping mode] The tapping mode was invented in 1993 [154]. This mode is a compromise between non-contact and contact modes because the tip is oscillating and touching the surface of the sample. During tapping mode, the oscillation amplitude is kept constant through a feedback loop. When the tip passes over a bump, its vibration amplitude decreases due to less vibrating space available. Whereas, when it passes over a hole, its vibration amplitude increases. This change in oscillation amplitude is generated as an error signal that actuates the piezoelectric element to adjust the tip-sample separation in order to maintain a constant amplitude and force on the sample [152][155].

[Advantages of tapping mode] Compared to contact mode, it has the advantage of being more stable on highly textured surfaces and decreases the friction force, hence avoiding the tip and sample degradation. Compared to non-contact mode, it has the advantage of interacting with a strong contact force and not being sensitive to water meniscus, so it can operate in ambient environment.

[AFM vs SEM] If compared to SEM, AFM provides a true physical three-dimensional surface profile, unlike the SEM which provides two-dimensional projection. In addition, samples viewed by AFM do not suffer from charging artifacts in the scanned image, therefore they do not need some special treatments like covering the sample with metal or carbon layers that can be used in SEM to avoid charging effects. AFM measurement can work properly in ambient air, unlike SEM which needs a vacuum environment.

However, small scanned area is a disadvantage of AFM compared to SEM. SEM can image an area on the order of square millimeters with a depth of field on the order of millimeters, whereas the AFM can only image a maximum scanning area of about 150×150 μm and a maximum height on the order of 10-20 μm. Although AFM can provide higher resolution than SEM in term of topography, the measurement can be limited by tip convolution. The SEM remains a more complicated tool that can give more information on the electrical behavior and topography of the sample depending on the voltage and detector used. Furthermore, the scanning speed of AFM is smaller than that of SEM. It requires several minutes for a typical scan in AFM, while it is possible to scan during that same time many areas of the sample in SEM.

[In this thesis] In this manuscript, the AFM used for checking some of the topography images of the samples with nanoholes was an Agilent 5500 (in LPICM, Ecole polytechnique) and the wavelength of the AFM laser is 680 nm. It was used in tapping mode using silicon, n-type tips from APPNANO, with a radius smaller than 10nm, and frequency between 200 and 400 KHz.

Experimental techniques

Conductive Probe AFM (CP-AFM) is a mode in AFM that simultaneously measures the topography of a material and the electric current flow at the contact point of the tip with the surface of the sample. It will be presented in the next part of this chapter.

2.2.3.2 Conductive probe atomic force microscope (CP-AFM)

In this thesis, we need a technique capable of characterizing electrically our samples with nanometer scale resolution, therefore the CP-AFM was used due to its capability of performing localized resistance measurements using a conducting probe.

The CP-AFM was firstly developed by John O'Shea and co-workers at the University of Cambridge in 1993. It had the goal of studying the local tunneling currents through 12 nm thick SiO₂ films [156]. In that same year, the first local resistivity cartographies appeared in the literature by Shaifa, et al. It was used for the delineation of semiconductor doping with a lateral resolution better than 35nm by measuring the topography and resistivity topographies at the same time [157].

In 1995 and 1996, O'Shea [158] and Ruskell [159] further improved the lateral resolution of the CP-AFM technique, achieving values of 10 nm and 8 nm, respectively.

In 1996, a French team in the “Laboratoire de génie électrique et électronique de Paris” (LGEP, now called GeePs,) demonstrated a significant improvement in this technique capable of performing a localized resistivity measurement with a conductive probe. This was achieved through the modification of a commercial system of force microscopy (apparatus and probes). The core of the additional circuit inserted in the commercial configuration is a logarithmic current amplifier intended for a wide range of variations [160]. In the beginning of 2000s, this resulted in the commercialization of an AFM extension called “Resiscope” that can be implemented on a commercial AFM to perform local resistance measurements. This setup allows one to apply a stable DC bias voltage (from -10 to +10 V with 0.01 V resolution) to the device and to measure the resulting current flowing through the tip as the sample surface is scanned in contact mode. It allows resistance measurements over ten orders of magnitude: from 10²-10¹² Ω with a few per cent accuracy (below 3 % in the range of 10²-10¹¹ Ω, and it can reach 10 % for higher resistance values [161]). The measurement of a large range of resistances allows this technique to be used in investigating a variety of materials such as metals [162], semi-conductors [163], conducting polymers [164], or composites [165].

Figure 2.20 is a schematic of basic CP-AFM operation; a voltage is applied between the tip and the substrate holder. The generated current is measured, and the resistance of the layer is estimated. The current passes vertically in the sample and therefore allows the estimation of the out-of-plane resistance of the layer. The tip and the cantilever are made either of a highly conducting material such as doped silicon, doped diamond, or of silicon nitride coated with metal film for conduction. Platinum iridium and diamond are two examples of coating materials for conductive AFM tips.

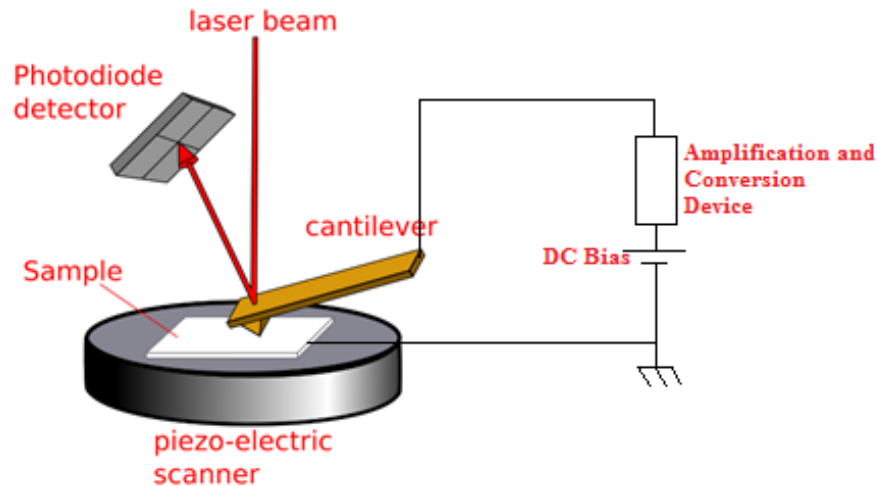


Fig.2.20: Schematic of basic CP-AFM operation.

The resistance measured by a Resiscope is the sum of several resistances in series: the resistance of the probe itself, the sample resistance (between the back contact and the probe), the back-contact resistance and the tip-sample contact resistance. In most of the cases, the tip-sample resistance is much higher than the other resistances because of the area of contact is nano-metric. This implies that the resistance measured by the Resiscope is dominated by the current spreading through this nanocontact and so called spreading resistance (SR). However, in the case of heavily doped samples (typically for active dopant concentration above $5E19 \text{ cm}^{-3}$) the SR decreases, and as the resistivity of the analyzed semiconductor approaches the one of the tip material (typically B-doped diamond). The resistance of the probe (R_{probe}) can then dominate over the SR and saturate the total measured resistance [166].

[In this thesis] The resistance mapping done in this PhD were measured at GeePs using a Digital instrument Nanoscope IIIa Multimode AFM associated with the “Resiscope” for which the AFM laser wavelength is 670 nm. A second setup was used as well, a Combiscope (AIST-NT), for which the AFM laser wavelength is 1300 nm. They are used in chapter 5 to characterize the locally doped samples, where the effect of the laser wavelength will be also studied. The AFM tip used for these two setups are purchased from Nanosensors (CDT-FMR-20), and are n^+ Si coated with polycrystalline diamond doped with boron at the tip side of the cantilever and having a radius around 100 nm.

2.2.4 J-V measurements

The equivalent circuit of a solar cell is a current source in parallel with a diode and a shunt resistance, and all in series with a series resistance. The series resistance is caused by the movement of current through the emitter and base of the cell and by the contact resistance between the metal contact and the silicon. As for the shunt resistance, it results in a leakage current and is mainly due to alternative current paths between the electrodes. This equivalent circuit is present in Fig2.21.

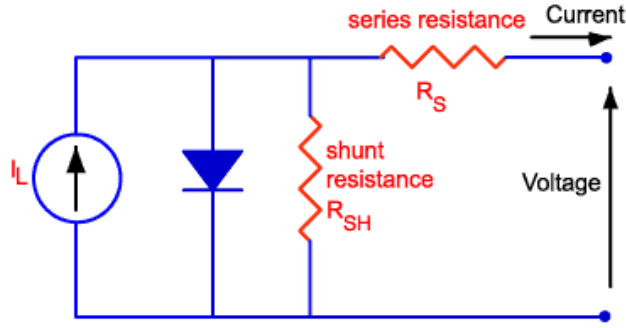


Fig.2.21: Equivalent circuit of a solar cell [167].

In the dark, an ideal solar cell with no resistances behaves exactly like a diode. Its $J(V)$ curve is ideally given by this expression:

$$J = J_{dark} = J_0 \left[\exp\left(\frac{qV}{nKT}\right) - 1 \right] \quad (2.9)$$

Where q is the electron charge, K the Boltzmann constant, J_0 is the dark saturation density of current, and n is the ideality factor of the diode.

As soon as the solar cell is illuminated, a photo-generated current density J_{ph} will be superimposed on the dark current J_{dark} . The equation becomes:

$$J_{illum} = J_{ph} - J_{dark} = J_{ph} - J_0 \left[\exp\left(\frac{qV}{nKT}\right) - 1 \right] \quad (2.10)$$

There is a negative sign in front of J_{dark} , because the photo-generated current and the diode forward current flow in opposite directions. The photo-generated current is composed of holes flowing to the p-side and electrons flowing to the n side, whereas in the forward operation of a dark diode, the flow of carriers is just the opposite.

If the series and shunt resistance will be taken in consideration, the equation will become:

$$J(V) = J_{ph} - J_0 \left[\exp\left(\frac{q(V - JR_s)}{nKT}\right) - 1 \right] - \frac{V - JR_s}{R_{sh}} \quad (2.11)$$

Concerning pin thin film silicon solar cells, the transport of carriers within the intrinsic layer is mainly by drift due to the presence of an electrical field. However, when a voltage is applied, the electrical field decrease and hence the recombination increases. The major part of the recombination takes place in the “bulk” of the i-layer, but there can be additional enhanced recombination at the p/i- and i/n- interfaces [168]. This leads to the following expression for the illuminated pin- or nip- type solar cell:

$$J_{illum} = J_{ph} - J_{dark} - J_{rec} \quad (2.12)$$

The equivalent electrical circuit will be represented by Fig.2.22.

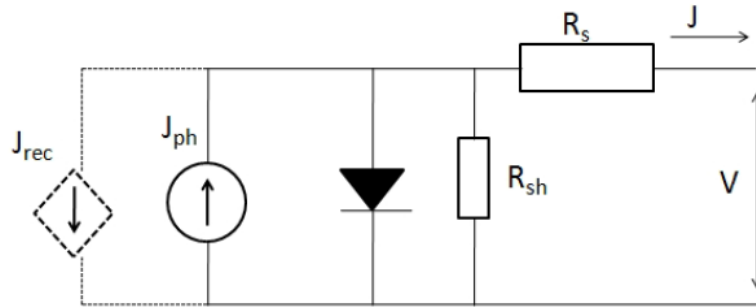


Fig.2.22: Equivalent electrical circuit of a pin or nip solar cell.

The measured J-V curves for a crystalline silicon solar cell and a thin film silicon solar cell is represented in Fig.2.23.

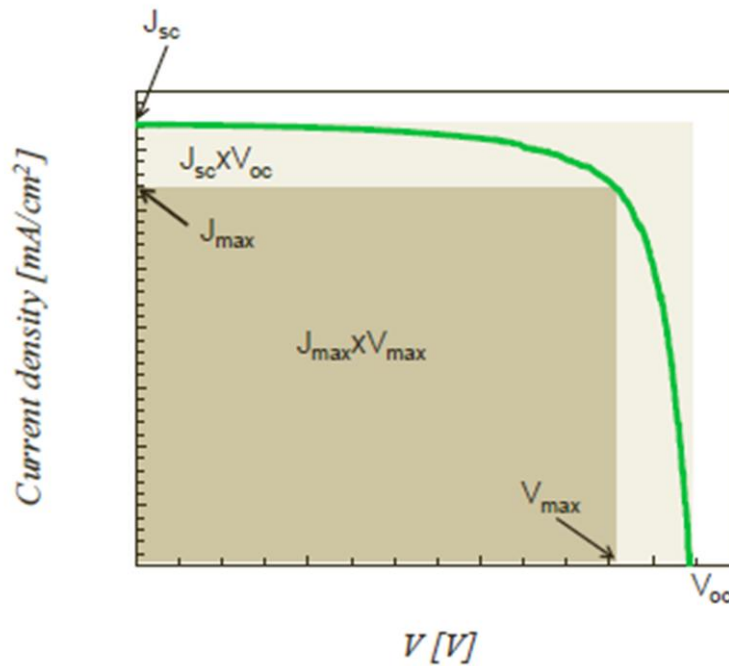


Fig.2.23 : Typical J-V curve of a solar cell [116].

This graph indicates three important points used to evaluate the performance of a solar cell. Firstly, the open circuit voltage (V_{oc}), that is the voltage when $J=0$. Secondly the short-circuit current (J_{sc}), that is the current when $V=0$. The location of the maximum power point determines the fill factor (FF), which indicates the squareness of the J-V curve. This parameter is the ratio between the area of the rectangle formed by the maximum power point ($J_{max} \times V_{max}$) and the one formed by V_{oc} and J_{sc} (Fig.2.23). It is given by this equation:

$$FF = \frac{V_{mp}J_{mp}}{V_{oc}J_{sc}} \quad (2.13)$$

Finally, the parameter that is most commonly used to compare the performance of one solar cell to another is the efficiency (η). It is defined as the ratio of energy output from the solar cell to input energy from the sun. As this factor depends on the spectrum and the intensity of the incident sunlight and the solar cell

temperature, it should be measured under AM1.5 conditions and at 25°C. The efficiency is given by the following equation:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{FF \cdot J_{sc} \cdot V_{oc}}{P_{in}} \quad (2.14)$$

[In this thesis] During this PhD, the J-V characteristics were measured using an Oriel sol 3A [169] and a homemade solar simulator for the dark I-V measurements.

2.2.5 Electro-chemical capacitance voltage (ECV) profiling

ECV is a destructive technique used to measure the active carrier concentration profiles in semiconductor layers. An electrolyte-semiconductor Schottky contact is used to form a depletion region, which is empty of conducting electrons and holes, but contains ionized donors and electrically active defects or traps. The depletion region with its ionized charges inside behaves like a capacitor. The measurement of the capacitance provides information of the doping and electrically active defect densities. Depth profiling is achieved by electrolytically etching the semiconductor between the capacitance measurements using a solution of HCl 0.5 m/l + NH₄HF 0.1 m/l. More details about this technique can be found here [170].

[In this thesis] In this PhD, the measurement of active boron dopants after implantation and annealing (ch.5) was done at Probion Analysis, using Biorad PN 4300, with a modulation frequency of 3 kHz.

2.2.6 Dynamic light scattering (DLS)

DLS is a technique that can be used to determine the size distribution profile of small particles in suspension or polymers in solution.

The principle of dynamic light scattering is that particles and molecules that are in constant random thermal motion, called Brownian motion, diffuse at a speed related to their size, smaller particles diffusing faster than larger particles. To measure the diffusion speed, the speckle pattern produced by illuminating the particles with a laser is observed. The Brownian motion of particles or molecules in suspension causes laser light to be scattered at different intensities. The scattering intensity at a specific angle will fluctuate with time, and this is detected using a sensitive avalanche photodiode detector (APD). The intensity changes are analyzed with a digital autocorrelator which generates a correlation function. This curve can be analyzed to give the size distribution.

[In this thesis] DLS measurements were performed in this PhD with a Malvern Nano ZS ZetaSizer [171], located at “Laboratoire de Physique de la matière condensée (PMC)”- Ecole Polytechnique, to check the polydispersity of a NP suspension (Ch.3).

Chapter 3: Nanoparticle Deposition, Etching and Removal

| | | |
|---------|---|----|
| 3.1 | <i>Nanoparticle deposition</i> | 57 |
| 3.1.1 | Method 1: NP deposition by spraying..... | 57 |
| 3.1.2 | Method 2: NP deposition by spin coating | 59 |
| 3.1.2.1 | 50 nm PS particles..... | 59 |
| 3.1.2.2 | 100 nm PS particles..... | 62 |
| 3.1.2.3 | Role of substrate surface | 64 |
| 3.1.2.4 | Summary-NP deposition by spin coating..... | 67 |
| 3.1.3 | Method 3: NP deposition by floating transfer technique | 67 |
| 3.2 | <i>Nanoparticle etching by O₂ plasma using MDECR</i> | 69 |
| 3.2.1 | Effect of plasma power | 70 |
| 3.2.2 | Role of ions | 72 |
| 3.2.3 | Evolution of particle shapes | 76 |
| 3.2.4 | Summary-NP etching | 83 |
| 3.3 | <i>Nanoparticle Removal</i> | 83 |
| 3.3.1 | NP removal via solution..... | 83 |
| 3.3.2 | NP removal by tape stripping..... | 95 |
| 3.3.3 | Summary-NP removal..... | 97 |
| 3.4 | <i>Chapter Summary</i> | 98 |

The aim of this chapter is to present all the steps done in this thesis to deposit NPs of different diameters, as well to remove them after being covered with a masking layer (Al evaporated, SiO_2 and SiN_x deposited by MD-ECR and a- $\text{SiC}_x\text{:H}$ deposited by PECVD). Figure 3.1 summarizes the three different ways that will be used in this thesis to form holes in dielectrics.

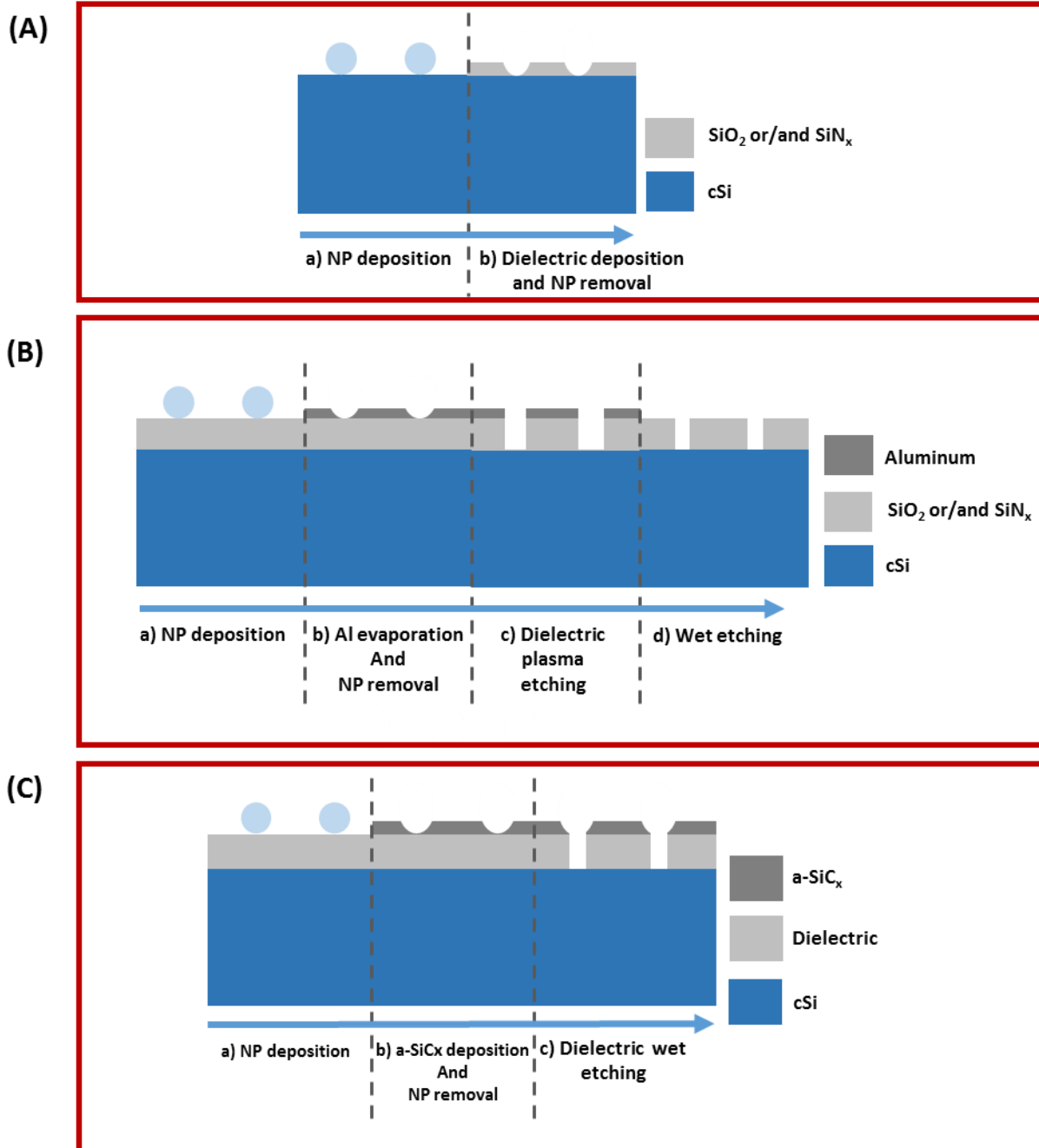


Fig.3.1: Schematic illustration showing three different approaches developed in this chapter; (A) approach A, direct mask, consists of forming holes in thin dielectric layer, (B) approach B, metal mask, consists of forming holes in thick dielectric layer by using evaporated Al as a masking layer, and (C) approach C, a- $\text{SiC}_x\text{:H}$ mask, consists of forming holes in thick dielectric layer by using a- $\text{SiC}_x\text{:H}$ as a masking layer.

These three approaches and the tools needed to execute them will be developed in detail in this chapter. The goal is a controllable method of NP deposition with a NP coverage below 10 % on the substrate surface and to achieve 100 % NP removal after covering them with a masking layer.

NPs were deposited on the sample using three different methods; NPs spraying, NPs spin coating and floating a NP monolayer on a liquid surface then transferring it to the sample surface. After the floating transfer technique, an additional process step (etching by O₂ plasma) is needed to reduce the NP's diameter and achieve lower coverage. The etching of arrays of polystyrene nanoparticles (NPs) in the O₂ plasma generated by a matrix distributed electron cyclotron resonance (MDECR) plasma source will be investigated.

3.1 Nanoparticle deposition

Many different methods of NP deposition have been used in the literature, such as solution-casting [172], [173], ink-jet [174], spin-coating [175][176], dip-coating, spray coating [177][178][179][180] soft lithography [181] and the floating transfer technique [182][183][184].

In this work, three different methods were attempted to deposit the NPs; spraying, spin coating and floating a NP monolayer on a liquid surface then transfer it to the sample surface.

3.1.1 Method 1: NP deposition by spraying

The first trial of NP deposition on a substrate was done using a homemade atomizer where an aqueous suspension of 1/100 diluted 100 nm polystyrene (PS) NPs was used. The substrates used for this trial are AlCu (alloy of 98% Al and 2% Cu) deposited on glass.

A NP aqueous suspension of 2 ml was sprayed on 4 AlCu samples. The samples were put on a hot plate at 95 °C while spraying the solution to accelerate the solution drying. SEM images of the resulting surfaces are shown in Fig.3.2.

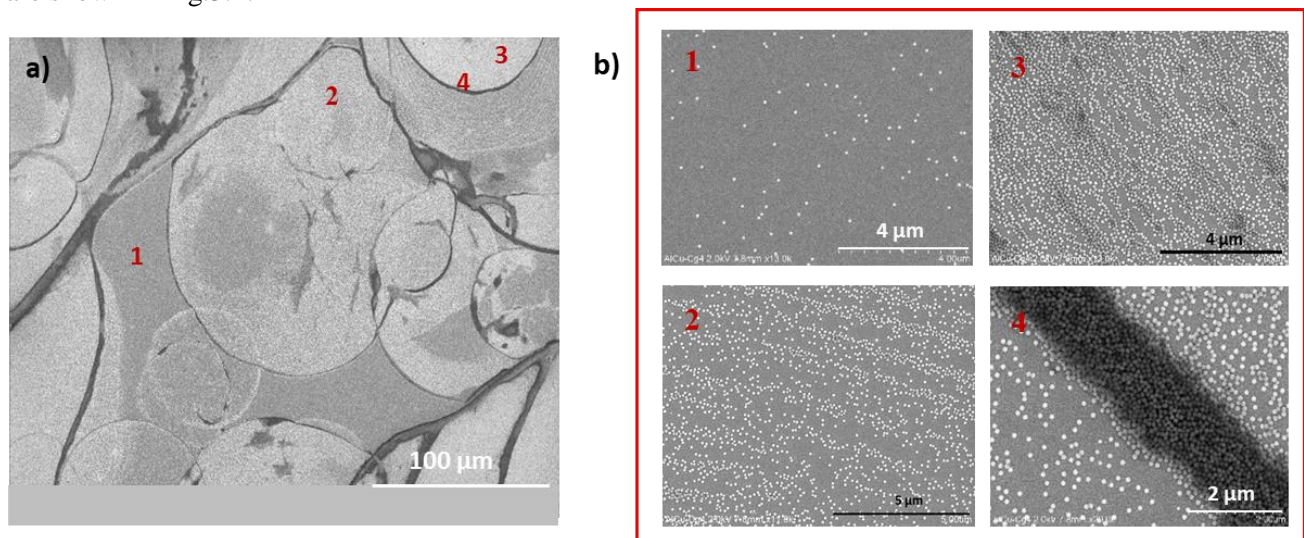


Fig.3.2: SEM top view images of sprayed NP on AlCu sample, (a) at low magnification, and (b) at high magnification where zones 1, 2, 3, and 4 correspond to same zones number seen on Fig.3.2 (a).

Nanoparticle Deposition, Etching and Removal

By using this method, different overlapping zones with different NP density are obtained on the sample surface. One can notice that the density is the highest at the edge of the zones as can be seen in zone 4 of Fig.3.2.b (black part).

The NPs aqueous suspension was further diluted to 1/1000. Around 1.1 ml of this solution was sprayed on two AlCu samples while keeping them on the hot plate. The NPs aqueous suspension was sprayed one time on one of the samples, while it was sprayed around 50 times on the second. Images of the samples are presented in Fig.3.3 and Fig.3.4, respectively.

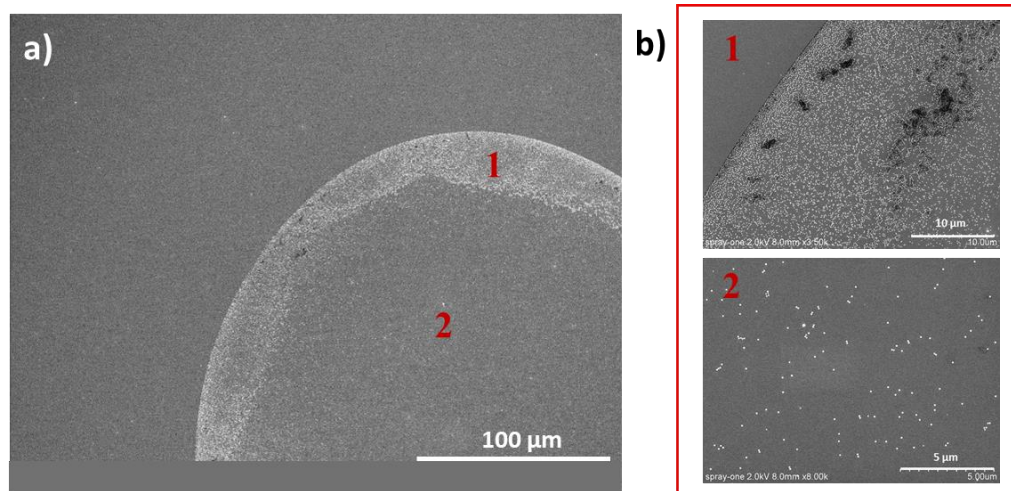


Fig.3.3: SEM top view images of NPs sprayed on AlCu sample, (a) at low magnification, and (b) at high magnification where zones 1, 2 correspond to same zones number seen on Fig.3.3(a).

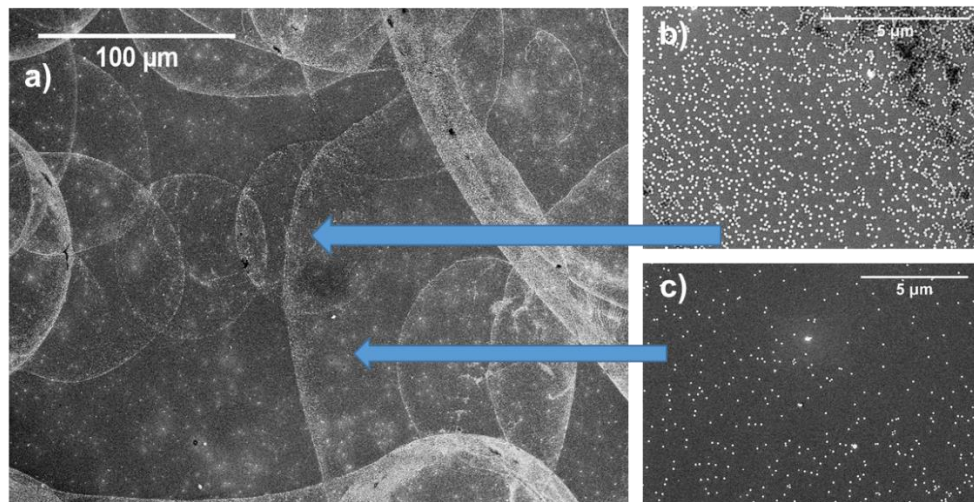


Fig.3.4: (a) SEM top view images corresponding to sample where NP aqueous suspension was sprayed 50 times (low magnification), (b) and (c) SEM top view image taken at high magnification.

For the sample shown in Fig.3.3, on which the NPs aqueous suspension was sprayed one time, it can be seen from the SEM image on the left at low magnification that a round shape appears on the sample. By looking at a higher magnification, the NPs density on the edge of the spherical shape is greater than that inside the sphere.

For the sample shown in Fig.3.4, on which the NPs aqueous suspension was sprayed 50 times, it can be seen from the SEM left image (at low magnification) that there is a “coffee ring effect”. This effect has been documented in the literature for micrometer-sized particles [185], [186].

Again, a higher NP density appears on the edge of the round shapes or in the intersection between two as can be seen from Fig.3.4.b and a lower NP density distribution appears in the middle of the round shape (Fig.3.4.c).

This method of NP deposition was abandoned as we require a homogenous NP distribution on the whole sample surface.

3.1.2 Method 2: NP deposition by spin coating

Spin coating is one of the most common techniques for producing thin films on substrates. It is used in a wide variety of industries and technology sectors. Spin coating was as well used to deposit densely packed or separated NP on the surface [176][175], where the colloidal dispersion spreads out on the substrate and forms a film. This latter spreads outward and thins, controlled primarily by centrifugal force and viscous shear force. When the film becomes sufficiently thin, evaporation dominates, further thinning the film. The evaporation step depends on the volatility and other properties of the coating liquid. For colloidal suspensions, the film thickness during this stage can be reduced to the same order as the particle size, here point capillary forces at the liquid-gas interface can have significant effect on particle aggregation, depending on the spin rate [187][188]. The advantage of this method is its ability to quickly and easily produce a coating on a sample surface. As it’s an easy, straight forward method which allows one to deposit well-separated NPs on a sample surface, it was used in this thesis to deposit NPs on cSi and metallic substrates. The distribution of the NPs also depends on the concentration of the NP suspension [189]. In this part of the thesis, the NP distribution on the surface has been studied by varying the rotational and acceleration speed as well as the NP density and size and the sample roughness.

3.1.2.1 50 nm PS particles

The first trials were done using ~ 50 nm NP diameter with an aqueous suspension of 1 %¹. The initial suspension of NPs contains a small amount of surfactant and 2 mM of sodium azide as an anti-microbial agent. The crystalline silicon (c-Si) samples were cleaned with an ultrasonic (US) bath of acetone or isopropanol and were exposed to UV ozone for around 15 min.

For the spin coated samples, the spin coating was usually done with 6000 rpm as rotational speed, 2000 rpm/s as acceleration and 30 s as spin coating time (The rotation and acceleration will be mentioned when varied). The calculated NP density (by Image J) in all the next part approximates the NP density on the whole surface.

[Undiluted aqueous NP suspension] These first trials were done on different substrates: Si, glass and a-Si:H. The first trial was focused on studying the spin coater speed on the NP distribution. Figure 3.5 shows the NP distribution on c-Si samples using three different speeds: 500 rpm, 3000 rpm and 6000 rpm. The samples were heated at 80 °C on a hot plate after spin coating.

¹ Purchased from Phosphorex.

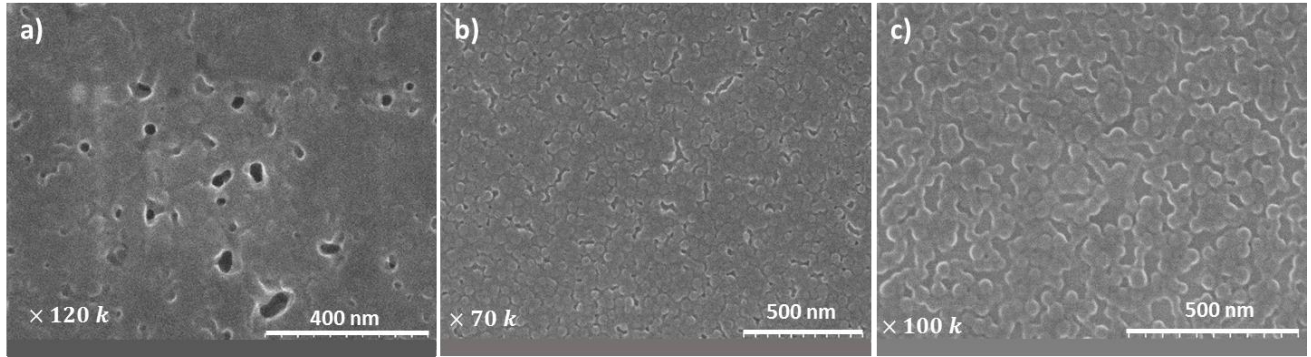


Fig.3.5: SEM images of cSi samples on which 50 nm PS NPs are spin coated using as accelerations (a) 500 rpm, (b) 3000 rpm and (c) 6000 rpm.

A densely packed NP layer is observed when the undiluted aqueous NP suspension is spin coated. The NPs can be seen more clearly when increasing the spin coater speed with more voids in between.

Similar observations were seen when repeating the same experiment on glass and a-Si:H substrates.

[Diluted aqueous NP suspension] As densely packed films were observed by using the aqueous NP suspension as it is, this latter was diluted with de-ionized water (DI) to obtain a lower coverage of NPs on the sample surface. The NP aqueous suspension was diluted with DI to 1/40. Different rotation speeds were used: (2500 rpm and 6000 rpm²) and the diluted NP suspension was spin coated on c-Si samples before and after US bath for 30 min. The corresponding SEM images are shown in Fig.3.6. The temperature of annealing used was 60 °C.

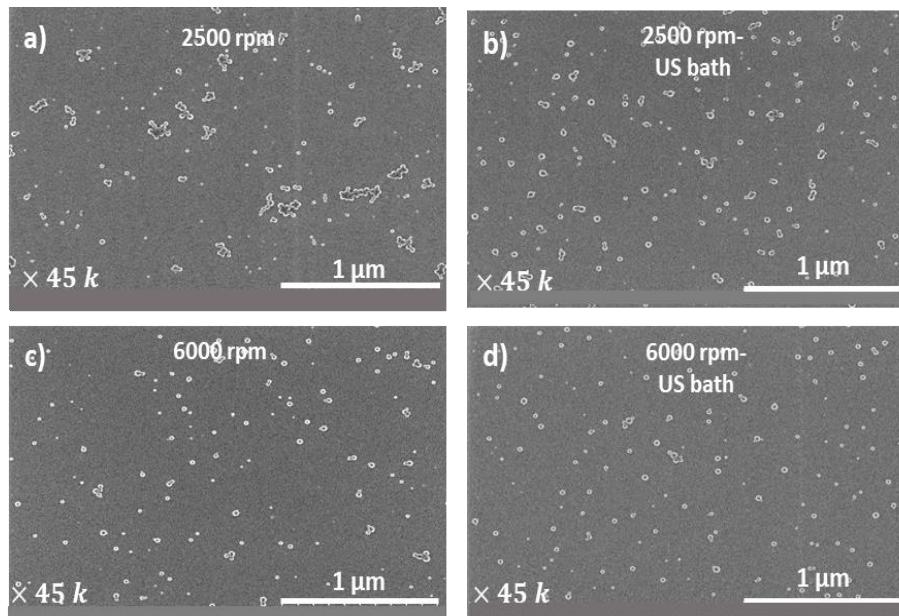


Fig.3.6: SEM images of 50 nm NPs spin coated at (a) 2500 rpm, (c) 6000 rpm. Spin coated NPs solution after ultrasonic bath for 30 min at (b) 2500 rpm, (d) 6000 rpm.

The NPs density decreased after diluting the NPs aqueous suspension (Fig.3.5.c and Fig.3.6.c) By comparing images 3.6.a and 3.6.c, it can be seen that increasing the spin coating speed diminish the NPs

² 6000 rpm is the highest speed available for the spin coater used.

aggregations. The same was observed when the solution that had an US bath was spin coated (comparing Fig.3.6.b, and 3.6.d).

It was seen that spin coated NPs are more distributed with less aggregations if the solution had an ultrasonic bath prior to spin coating when 2500 rpm is used as rotation speed. However, little difference is seen for higher speeds.

The NPs density is around 20 NPs/ μm^2 when 6000 rpm is used, and it is around 30 NPs/ μm^2 when 2500 rpm is used and an US bath is included (Fig.3.6.b). It was reported by Z. Yenice et al. that independent of the substrate type, the amount of particles deposited decreases with increasing spin rates because of the centrifugal forces increasing and the faster film thinning for higher spin rates [189].

It was seen in this part that by diluting the NPs aqueous suspension, the density of the spin coated NP will be decreased. By increasing the spin coating rotation speed, fewer NP aggregations will be observed on the surface, and by putting the NPs suspension in an ultrasonic bath, NPs will be less aggregated when spin coated at 2500 rpm. In the next section, we study the effect of the annealing temperature on the NP shape.

[Annealing temperature effect] The results shown below aim to study the effect of the annealing temperature on the spin coated NP. Different temperatures between 30 °C and 120 °C were used after spin coating. The SEM tilted view of the samples annealed at 30 °C, 60 °C, 90 °C and 120 °C are shown in Fig.3.7.a, 3.7.b, 3.7.c and 3.7.d respectively.

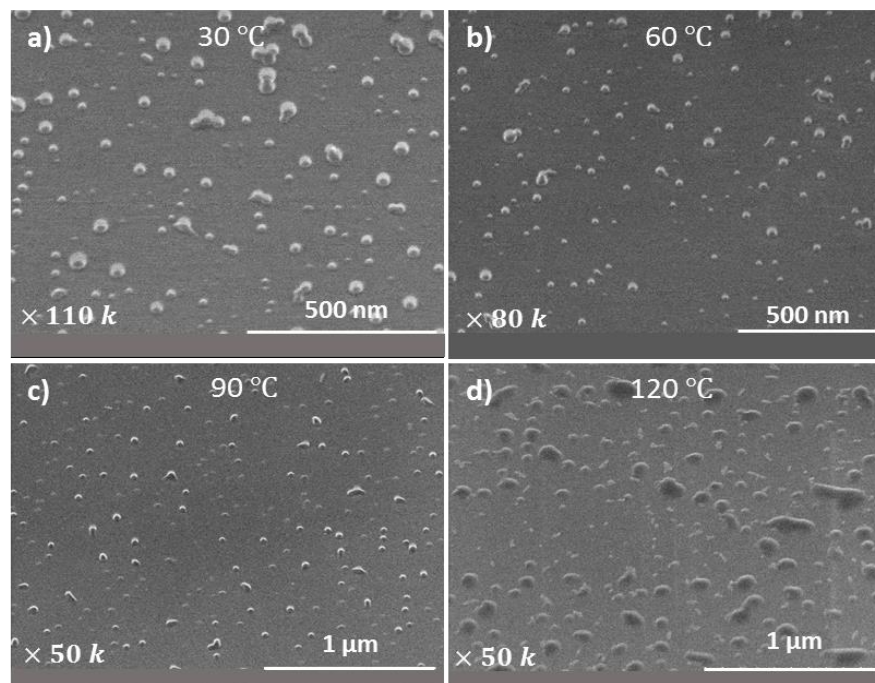


Fig.3.7: 50 nm NPs spin coated and annealed at (a) 30 °C, (b) 60 °C, (c) 90 °C and (d) 120 °C.

It can be seen that a softening (larger contact area between the NPs and the substrate) of the NPs starts to be observed when the samples are annealed at 90 °C, and it is more severe when they are annealed at 120 °C. This is reasonable as the polystyrene glass transition temperature is around 100 °C. To avoid NP softening, 50 °C will be used as annealing temperature for the next spin coated samples.

[Effect of time] After few months of using the same suspension, more aggregation appeared when spin coated. A study of checking the influence of the dilution on the NP aggregations were done by diluting the

suspension as previously done for Fig.3.6 (1/40 with DI), as well with a dilution of 1/10 and 1/100. Fig.3.8 shows the SEM images for all the different dilutions used.

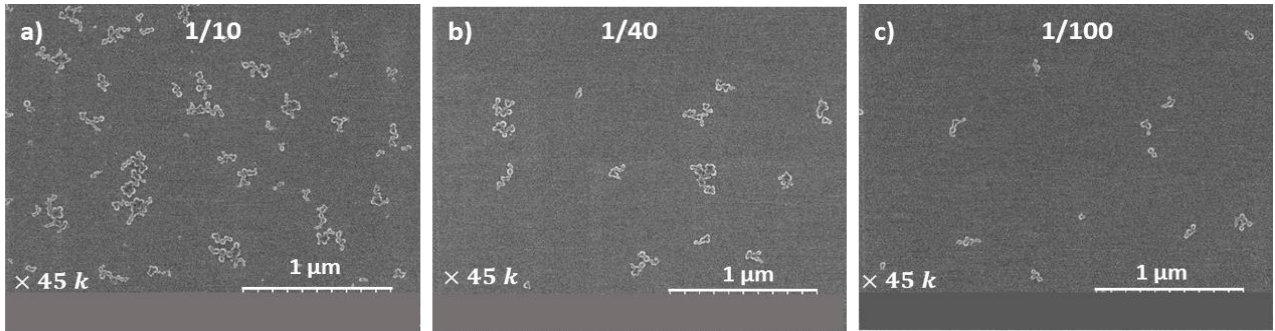


Fig.3.8: SEM images of 50 nm spin coated NPs on cSi samples using as dilution (a) 1/10, (b) 1/40 and (c) 1/100.

It was seen that the NP density decreases by increasing the NP suspension dilution due to the smaller number of NPs in the suspension after dilution. However, all samples showed significant aggregation.

3.1.2.2 100 nm PS particles

Another aqueous suspension consisting of 100 nm NPs was spin coated on c-Si samples. The NPs had a nominal diameter of 100 ± 4 nm and the original suspension had a concentration of 5 %³. This solution was diluted to 1/10 and 1/100, and SEM images of the corresponding NP distributions are shown in Fig.3.9.

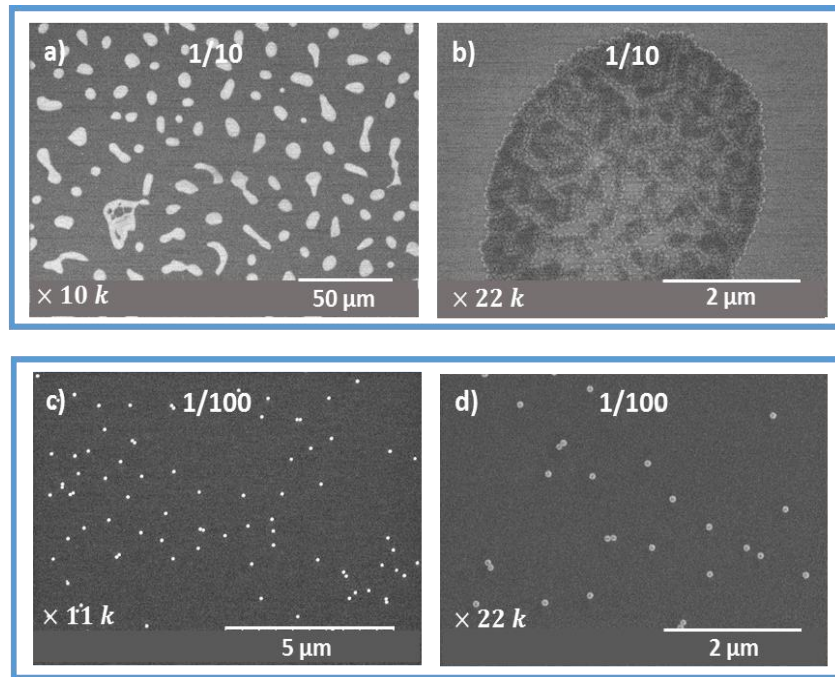


Fig.3.9: SEM images of c-Si samples where the dilution of the spin coated suspension is (a), (b) 1/10 and (c),(d) 1/100, where (c) and (d) are scans at higher magnification of (a) and (b), respectively.

³ Purchased from microparticles GmbH in berlin, Germany.

It is seen that by using 1/10 as dilution, NP clusters appear on the sample surface. However, by using a dilution of 1/100, no aggregations are seen, and a density of around 0.9 NPs/ μm^2 is achieved. It was noted that the 100 nm NPs tend to aggregate less compared to the 50 nm ones previously used. This is presumably due to a different composition and stability of the two suspensions, bought from two different companies.

As the 1/100 dilution of the suspension gave a better NP distribution, it will be used in the next part to study the influence of the spin coater acceleration on the NP distribution.

[Acceleration] The spin coater acceleration was varied between 500 rpm/s, 2000 rpm/s, and 6000 rpm/s, by keeping a speed of 6000 rpm during 30 s. The SEM images corresponding to the sample where the spin coating was done at 500 rpm/s and 6000 rpm/s are shown in Fig.3.10.

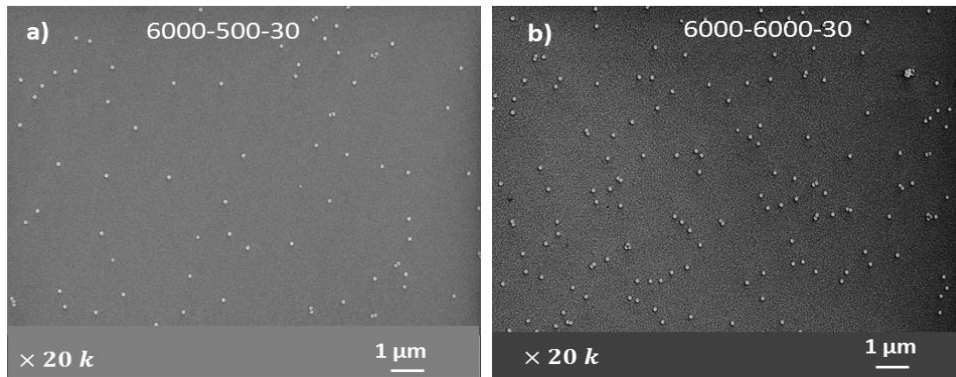


Fig.3.10: SEM images of c-Si samples on which 100 nm NPs are spin coated using 6000 rpm as rotation speed during 30 s with an acceleration of (a) 500 rpm/s, (b) 6000 rpm/s.

It was seen that the NP density is 0.47 NPs/ μm^2 when 500 rpm/s is used as spin coating acceleration. This density increases to around 1 NPs/ μm^2 when the acceleration is increased to 2000 rpm/s or 6000 rpm/s.

[NP size and coverage] In Fig.3.11, the NP coverage of the sample surface is plotted as function of NP diameter for a diameter of 50 nm⁴, 100 nm, 425 nm, and 784 nm.

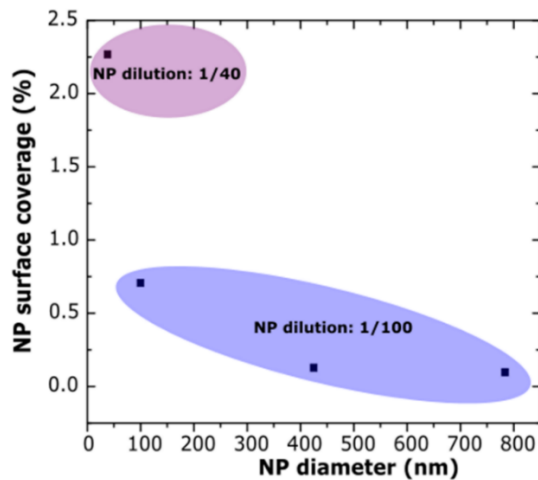


Fig.3.11: NP coverage as function of NP diameter.

⁴ Considering 38 nm as average NP diameter (Fig.3.45) due to the polydisperse NP suspension.

NP surface coverage is higher for smaller NPs. This graph gives a good idea of the range of surface coverage that is directly available through the NPs spin coating.

3.1.2.3 Role of substrate surface

100 nm NPs were also spin coated onto metallic surfaces, namely glass covered with 100 nm AlCu (alloy of 98 % Al and 2 % Cu). These substrates will be used as a back reflector for the Si thin film device in chapter 4.

To study the influence of NP aqueous dilution on the NP density, the suspension was diluted to 1/100, 1/70, 1/50 and 1/30. The corresponding SEM images are shown in Fig.3.12.

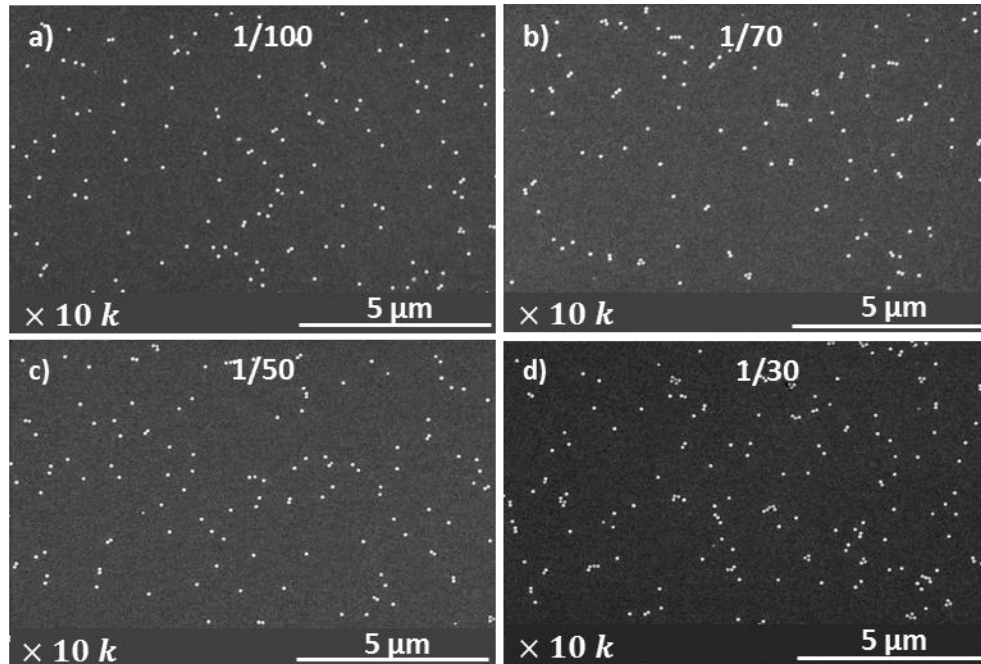


Fig.3.12: SEM images of AlCu samples, NP suspension dilutions of (a) 1/100, (b) 1/70, (c) 1/50, and (d) 1/30.

It was seen that there is little difference in the NP density for the different dilutions used (between 1 and 2 NPs/ μm^2). It was verified that there is also little difference in the NP density if the diluted NP suspension is spin coated 1, 2, or 3 consecutive times on the AlCu sample (in Appendix).

The NPs suspension was also spin coated onto different substrates: 100 nm AlCu , 100 nm AlCu covered with 100 nm ITO, 300 nm AlCu covered with a PIN stack, and 100 nm Ag covered with 100 nm ITO. The suspension was spin coated two consecutive times on these samples and the NP distribution for the different layers is shown in Fig.3.13.

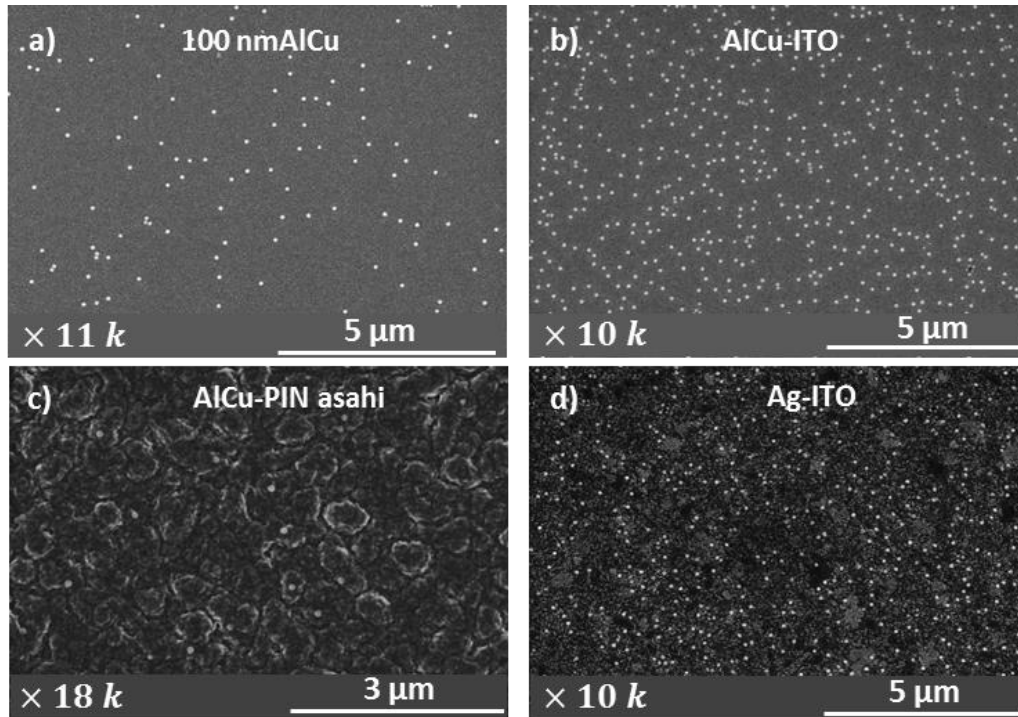


Fig.3.13: SEM images of 100 nm spin coated NP on (a) AlCu, (b) AlCu-ITO, (c) AlCu-PIN asahi, and (d) Ag-ITO.

It is seen from Fig.3.13 that NP density differs from one substrate to another. The NP density is $1.35 \text{ NPs}/\mu\text{m}^2$, $5.49 \text{ NPs}/\mu\text{m}^2$, $0.52 \text{ NPs}/\mu\text{m}^2$, and $5.59 \text{ NPs}/\mu\text{m}^2$ on AlCu, AlCu-ITO, AlCu-PIN asahi, and Ag-ITO respectively. (AlCu-ITO was used as the back reflector for a-Si:H in chapter 4)

The NPs were then spin coated onto a thicker AlCu thickness (300 nm). The SEM images of the NP dispersion on 100 nm, and 300 nm AlCu is shown in Fig.3.14.

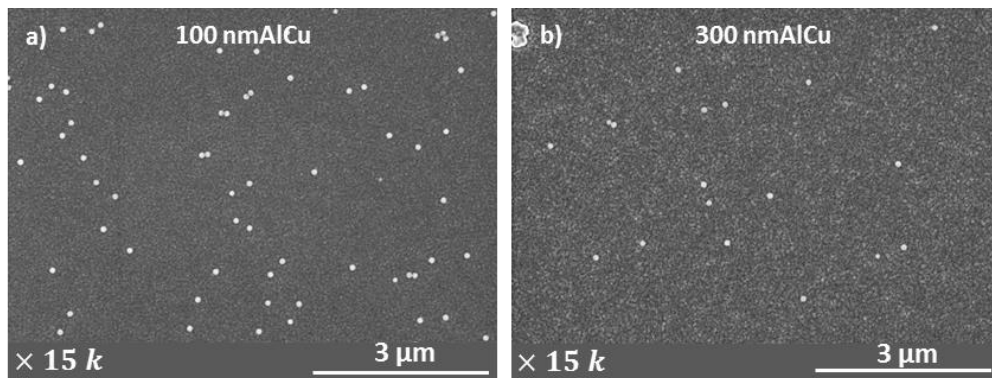


Fig.3.14: SEM images of 100 nm spin coated NPs on (a) 100nm AlCu and (b) 300nm AlCu.

It is seen that by increasing the AlCu thickness from 100 nm to 300 nm, the NP density decreases from $1.35 \text{ NPs}/\mu\text{m}^2$ to $0.5 \text{ NPs}/\mu\text{m}^2$. This is probably due to the modification of the surface roughness with the layer thickness. To see if there is a general trend, the average surface roughness is calculated for each of the samples using AFM. The NP density is plotted as function of this roughness and is shown in Fig.3.15.

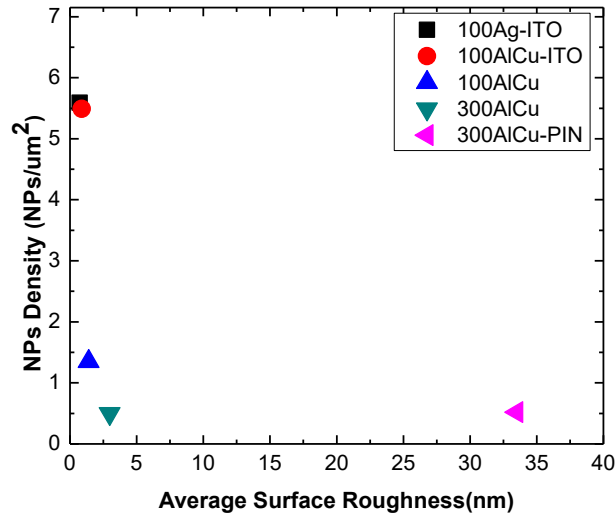


Fig.3.15: NP density as function of the surface roughness.

It is seen that the NP density decreases when the surface roughness increases. Depositing 100 nm layer of ITO decreases slightly the surface roughness but increases significantly the NP density.

[Monolayer on Si] As it is difficult to form a monolayer with the floating transfer technique that will be presented in section 3.1.3 when the NP diameter is around 100 nm, a trial was done to form one through spin coating. The solution of 100 nm NPs was diluted with the same volume of ethanol. Two drops of the diluted solution were spin coated using 2000 rpm as spin coating speed, 300 rpm/s as acceleration and 45 s as the spin coating time. The corresponding SEM image is shown in Fig.3.16.

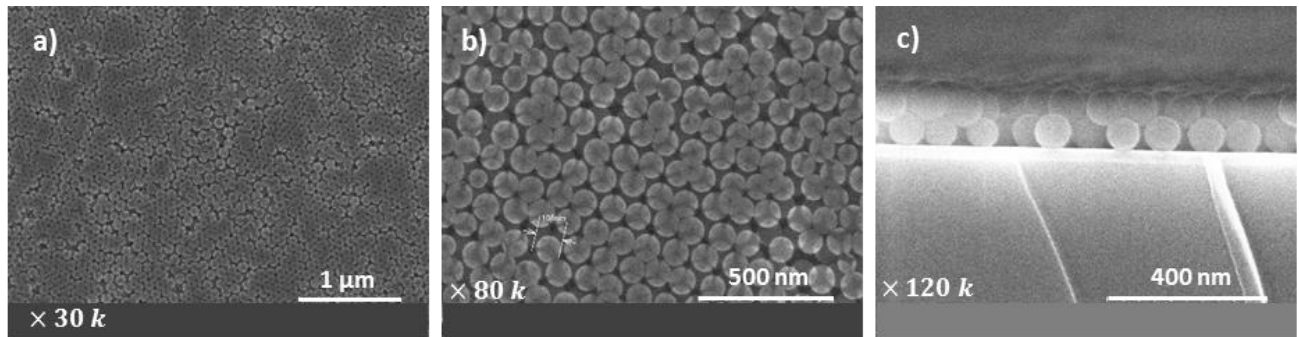


Fig.3.16: (a),(b) SEM top view images and (c) SEM cross section of cSi sample on which 100 nm NPs are spin coated using 2000 rpm, 300 rpm/s during 45s.

It is seen that a bilayer of NPs was formed using these conditions. It is not of interest to use O₂ plasma on this sample to etch the NPs, as it will be shown in part 3.2, because of the formation of two layers and not one. To form a monolayer, the spin coating speed should be further decreased.

3.1.2.4 Summary-NP deposition by spin coating

In this section, NPs were deposited by spin coating and the effect of the rotation, acceleration speed, NPs size and sample surface was studied. Some key lessons can be learned:

- By diluting the NPs aqueous suspension, the density of the spin coated NP will be decreased.
- By increasing the spin coating rotation, fewer NP aggregations was observed for the 50 nm NPs on the surface.
- By using an annealing temperature higher than 90 °C, the NPs will be softened.
- 100 nm NPs tend to aggregate less than the 50 nm NPs.
- NP coverage is higher when smaller NPs are spin coated.
- NP density decreases with the increase of the surface roughness.
- It was possible to form a bilayer of 100 nm NPs by spin coating.

Although spin-coating is an extremely rapid and simple fabrication method, careful adjustments of concentration, rotation speed, substrate surface and other parameters must be carried out for each single type of particle and substrate used. In addition, problems of aggregations, inhomogeneity can be observed on the substrate surface when spin coating is used as the NP deposition method. A more controllable and homogenous method will be used in the next part of this chapter, namely forming a NP monolayer on the substrate followed by an O₂ plasma to etch the NPs to reduce coverage.

3.1.3 Method 3: NP deposition by floating transfer technique

Different methods have been developed to assemble nanospheres with high order on various substrate types. The 2D colloidal crystal self-assembly can be divided into two categories: 1) direct assembly on the target substrate and 2) pre-assembly on an intermediate surface followed by a transfer onto the target. In the first case (1) monolayer deposition was often achieved by drying the colloidal suspension on a vertical substrate or by vertical lifting deposition. Thickness control is achieved in this case by adjusting the dispersion concentration and substrate lifting speed. However, stripes may be formed with this method limiting the vertical lifting deposition for large area samples. Micheletto et al. [190] has demonstrated a monolayer formation method on tilted substrates in order to improve the final monolayer quality. More elaborate equipment has been designed by Picard et al. [191]. They designed a small cylinder system that can prepare monolayers continuously and transfer them onto a hydrophobic and hydrophilic sample surfaces. However, these reported methods provide monolayers of only limited quality in terms of sample area size, defect density, and controllability; voids or multilayered regions are formed with the monolayer areas.

Therefore, indirect fabrication methods were formulated; they consist of first forming a high-quality monolayer on an intermediate surface like water that allows a better particle ordering, followed by transferring the monolayer to the target substrate. These approaches are normally based on the well-established Langmuir-Blodgett technique [192][193], where the floating monolayer is compressed by a barrier that promotes the assembly of the nanospheres in close-packed lattices. Usually, specific setups are used for the Langmuir-Blodgett technique to ensure that the pressure remains constant as the substrate is being withdrawn.

In this section, floating transfer technique [182] is used as an indirect fabrication method to form a NP monolayer on cSi substrate. It doesn't require a specific setup. The polystyrene (PS) nanospheres used in this work had nominal diameters of 425 ± 10 nm, 607 ± 15 nm, and 784 ± 23 nm and were obtained as an aqueous suspension of 5 wt.-%⁵. For simplicity, these will be referred to as 400 nm, 600 nm, and 800 nm NPs. The suspension was mixed with an equal amount of ethanol as a spreading agent. The initial solution had an US bath for 15 min prior to dilution.

The floating-transfer technique was used to deposit a compact monolayer of PS NPs on a c-Si substrate. The NPs monolayer was first formed on a water surface in a petri dish with inner diameter of 15 cm. To do so, the petri dish was washed with soap, cleaned with acetone, isopropanol and DI water and followed with UV ozone treatment for 15 min to achieve a highly hydrophobic surface.

Then the petri dish was halfway filled with DI water, and the diluted NPs suspension was spread slowly to the surface of the DI water through the sidewall of the petri dish using a syringe with a needle until it covers the majority of the water surface. It is important to delicately control the process of adding the NP solution onto the water surface to avoid possible sediment of colloidal spheres into the liquid phase [194]. The Spreading of the particle suspension uses the Marangoni effect in which a surface tension gradient causes the liquid surface to be pushed away from the regions of low surface tension. In the present case the Marangoni flow is induced by the difference of surface tension between Ethanol and water; it is 72 mN/m for water and 22 mN/m for ethanol. This difference causes the NP suspension added to rapidly spread outwards, thus covering the surface with particles [195][196].

While PS NPs were floated and spread on water surface, a monolayer of self-assembled, hexagonal and closely packed PS NPs film was formed [197]. The cSi substrates (100) (unless otherwise indicated, only coated with their native oxide) were cleaned with acetone, isopropanol and DI water prior to use, and put in a UV ozone chamber for around 15 min to ensure a hydrophilic surface. During the film transfer process, the substrates were first immersed below the water surface and under the PS NPs film, then lifted upward slowly so that the PS NP monolayer was transferred onto the substrate surface. After taking the substrates from petri dish and with PS NPs monolayer on top, they were dried in air naturally for around one hour. The process of floating transfer technique is presented in Fig.3.17 [182].

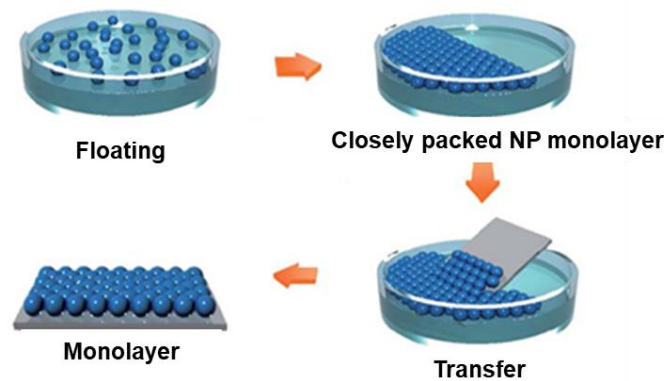


Fig.3.17: Schematic of floating-transfer technique to achieve hexagonal monolayer of NPs on cSi substrate.

⁵ Purchased from microparticles Germany.

Figure 3.18 shows SEM top view images of the monolayers, obtained using the floating-transfer technique, for NP diameters of a) 400 nm, b) 600 nm and c) 800 nm.

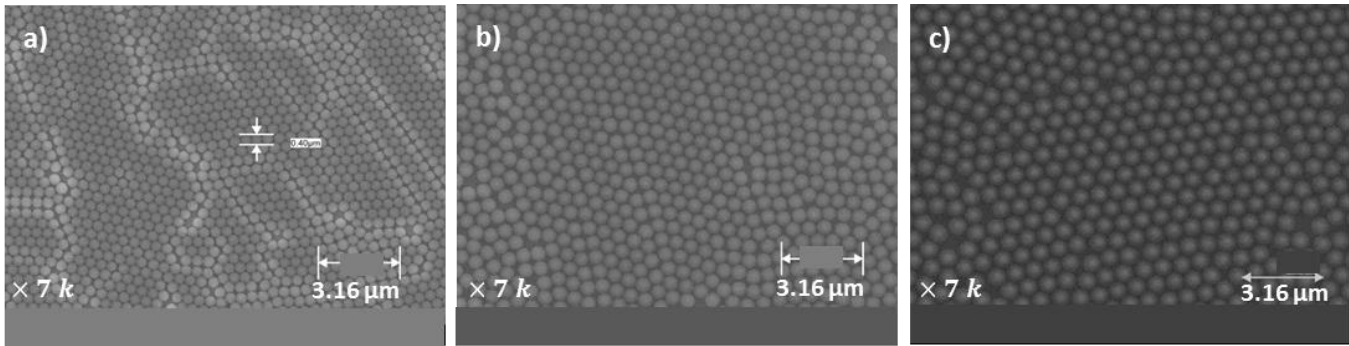


Fig.3.18: SEM images showing monolayer of NPs with diameters of (a) 400 nm, (b) 600 nm and (c) 800 nm.

3.2 Nanoparticle etching by O₂ plasma using MDECR

As these c-Si samples will be used in ch.5 as a doping mask for point contacts, a far lower surface coverage is required. Hence a non-close-packed (NCP) array is required. An additional process step is therefore needed to etch the NPs.

To do so, one can combine colloidal lithography with an additional process step, such as electron irradiation [198], ion polishing [199], or reactive ion etching (RIE) to shrink the NPs after forming a monolayer [200][201][202][203]. In particular, RIE almost inevitably roughens the sphere surfaces and distorts their shapes and positions, especially when the size-reduction reaches 65 % [204][205][206]. In many cases, it can even roughen the substrate surface, although this effect varies depending on the RIE system that is being used. M.Domonkos, et al. have processed polystyrene (PS) microspheres in two different RIE systems: capacitively coupled radiofrequency plasma (CCP) and a dual plasma system which combines CCP and pulsed linear-antenna microwave plasma (PLAMWP). It was reported that the PLAMWP system is less aggressive and allows smoother etching steps than CCP-RIE [207].

Other groups have studied the use of electron cyclotron resonance (ECR) oxygen plasmas to etch continuous polymer and photoresist films [208], [209]. Electron cyclotron resonance (ECR) plasmas offer several advantages in etching, including low ion energy for low damage and low pressure for an anisotropic profile. It also allows one to decouple the ion energy from the plasma parameters by biasing the substrate holder. In one such ECR O₂ plasma studies [208], it was reported that the polymer etch rate is unchanged by the presence of molecular oxygen, whereas it increases proportionally with the atomic oxygen concentration and with the ion current density. Other reports using ECR O₂ plasmas for photoresist etching have indicated a fast etch rate, smooth morphology with no damage to the resist, and good uniformity when a short distance to the ECR source was used [210].

In this work, we study the use of a matrix-distributed (MD-) ECR oxygen plasma source to process PS NP arrays, specifically observing the melting, etching, and deformation of the NPs. We aim to isolate the role of the mean plasma power (in both continuous and cycling mode), of ions, and of the radicals in said particle evolution.

Etching of polymer materials, like etching in general, is done in plasma by two mechanisms: physical sputtering and chemical etching. Physical sputtering is due to simple ion bombardment, while chemical etching is due to surface reactions and gasification of polymers particularly provided by atomic oxygen. Treatment of polymers in oxygen-containing plasma initially leads to the formation on the surface of atomic oxygen functional groups. Further interaction of the polymer with non-thermal oxygen-containing plasma can result in further oxidation, formation of CO₂ and H₂O, and their transition to the gas phase [211].

The etching process for this work was developed using an MD-ECR reactor, VENUS, already described in chapter 2. For the plasma etching, 40 sccm of O₂ was used, with 2 mTorr of pressure, and a plasma power of 500 W and 1 kW. The plasma was used in continuous and cycling mode.

The samples were studied in a high resolution field enhanced scanning electron microscope (FE-SEM, Hitachi S-4800) using the Secondary electron upper detector (SE(U)) which detects only secondary electrons. A free image processing software, “Image J” was used to extract quantified information from the SEM images.

3.2.1 Effect of plasma power

[Plasma power study-Continuous mode] To study the effect of microwave power on NP etching, two power values were used: 500 W and 1 kW. SEM top and side view images of the NPs after processing are shown in Fig.3.19.

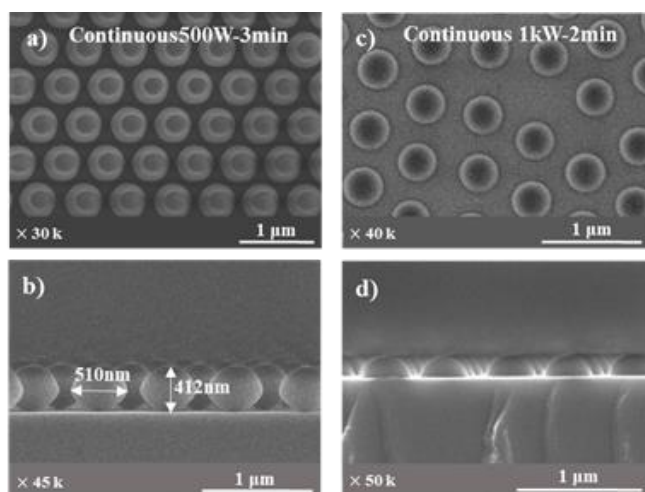


Fig.3.19: SEM images of 600 nm NPs etched by continuous plasma. 500 W for 3 min (a) top view, (b) side view, and 1 kW for 2 min (c) top view, and (d) side view.

After exposure to 500 W continuous plasma power for 3 min, the SEM top and side views (Fig.3.19.a and b) show no NP melting. The particles have adopted a slightly hexagonal shape, and have been etched to 64 % of their initial area (Seen from top view SEM images). However, after exposure to 1 kW of continuous plasma for 2 min, the NPs were completely melted (Fig.3.19.c and d). They therefore appear rounded from the SEM top view (Fig.3.19.c) and their area has been reduced to 42 % of its initial value.

In both cases, we can successfully etch PS NPs and yet retain their periodic arrangement. However, once the PS spheres are melted onto the substrate, depending on the melting severity and further manufacturing steps, one might lose the patterning capability of this technique. For instance, Fig.3.20 shows a case where

400 nm NPs were etched for 2 min in a continuous mode O₂ plasma at 1 kW followed by covering them with an aluminum layer in order to pattern it.

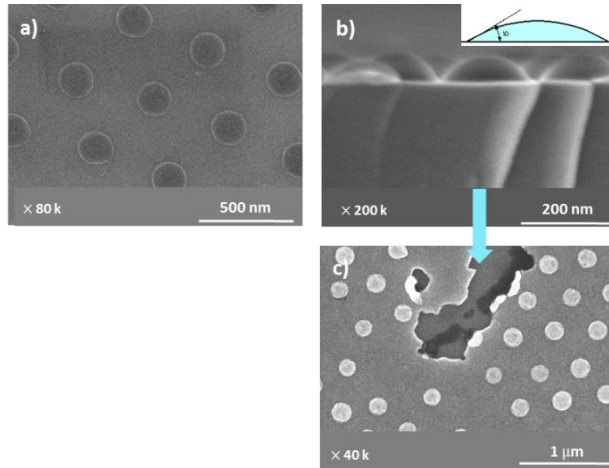


Fig.3.20: SEM images of cSi sample on which 400 nm NPs were etched after 2 min in an O₂ plasma at 1 kW (a) top view, (b) cross section. (c) top view images after a NP removal trial.

The NPs are completely melted, and it wasn't possible to remove the NPs using a toluene US bath (detailed later in section 3.3.1, Fig.3.40). To avoid the PS sphere melting issue and still be capable of etching the NPs, an alternative etching methodology was investigated in this work.

[Plasma power study-Cycling mode] To highlight the role of plasma heating on the etching and melting behavior of the particles, a cycled mode was also used in the plasma treatment. In cycling mode, the plasma etching process was carried out in multiple cycles, with each cycle comprising of 15 s of plasma ON and 30 s of plasma OFF. The applied plasma power and the total ON time was kept the same as for the continuous mode. 600 nm and 800 nm NPs deposited on a cSi substrate were used for the experiment. SEM images of the particles after exposure to the cycled plasma are shown in Fig.3.21.

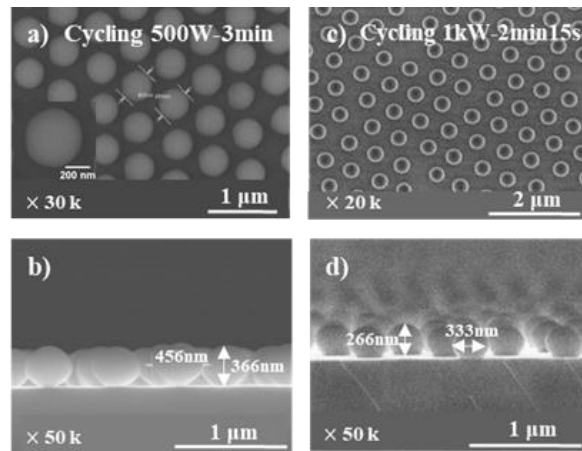


Fig.3.21: SEM images of 600 nm NPs etched by a cycled plasma. 500 W for 3 min (a) top view, (b) side view. 1 kW for 2 min 15 s (c) top view and (d) side view.

From Fig.3.21.a, it can be seen that the NPs subjected to the 500 W cycled plasma for 3 min have a slightly hexagonal shape (inset of fig.3.21.a), and have been etched to 60 % of their initial area. However, the

particles that were etched using the 1 kW cycled plasma for 2 min 15 s have been reduced to 34 % of their initial area and have maintained a round shape. The areal etching rate of the NPs in the cycled plasma is higher for both 500 W and 1 kW compared to the continuous plasma presented in Fig.3.19. This is possibly due to a longer exposure time to oxygen radicals in the cycled plasma. Comparing Fig.3.21.d to Fig.3.19.d, it can be seen that the NPs are not melted by the cycled plasma, but they do appear to have a greater contact area with the substrate.

To better compare these two processes, another set of experiments was performed on 800 nm NPs for 2 min 45 seconds, using either continuous or cycled mode (15 s ON/30 s OFF) at the same power of 1 kW. The corresponding SEM images are shown in Fig.3.22.

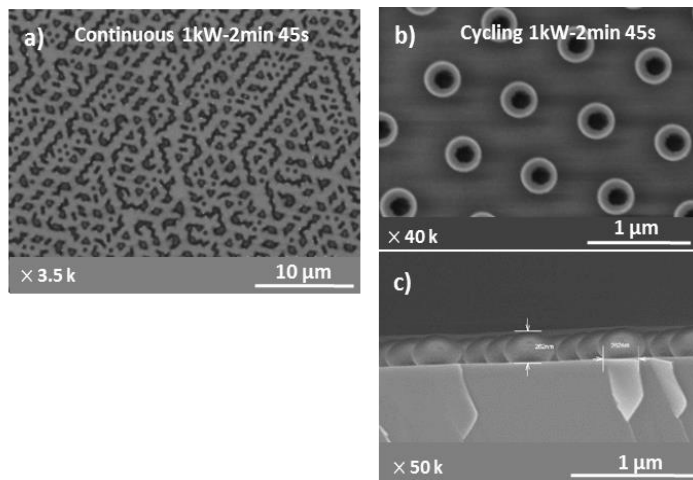


Fig.3.22: SEM images of 800 nm NPs etched at 1 kW power plasma for 2 min 45 s. (a) Continuous plasma, (b) cycled plasma top view and (c) side view.

Figure 3.22.a clearly shows that the NPs have fused together, indicating a rapid melting process for the longer continuous process. In contrast, after the cycled plasma, the NPs retain their round shape (Fig.3.22.b) despite being etched to 20 % of their initial area. However, the side-view image (Fig.3.22.c) again shows an increased contact area with the substrate.

To better understand and control this melting/softening behavior, the effect of different species in the O_2 plasma during PS NPs etching and melting shall be further investigated and understood.

3.2.2 Role of ions

In order to decouple the effect of ions from that of the oxygen radicals during etching, as well as to better understand the reason behind the NP melting, a stainless steel cage was used to reduce the ion flux on the samples. The ion flux for an Ar plasma was measured both inside and outside the cage (mesh transparency of 78 %, cell size of 1 mm) using a flat Langmuir probe with an area of 1 cm^2 . The test plasma conditions were 2 mTorr and 500 W or 1 kW. At 1 kW of microwave power, the ion current density onto the grounded probe outside of the cage was 1.32 mA/cm^2 , while inside the grounded cage it dropped to 0.06 mA/cm^2 . At 500 W of microwave power, it dropped from 0.6 mA/cm^2 to 0.03 mA/cm^2 . Floating potentials were +3 Volts and +8 Volts for 500 W and 1 kW, respectively. From this, we estimate that the stainless steel cage reduces the ion flux by around 95 % (The transparency of the cage is also expected to reduce the radical flux by around 20 % at most).

A set of experiments was then performed by placing samples inside and outside the metal cage, and exposing them to different plasma power conditions in either cycled or continuous plasma modes. Figure 3.23 shows the SEM images of the resulting samples placed either inside or outside the cage (1 kW continuous plasma, 2 min).

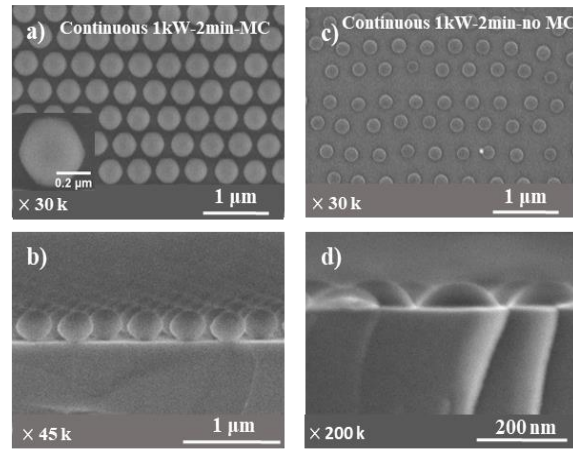


Fig.3.23: SEM images of 400 nm NPs etched by 1 kW continuous plasma for 2 min. Sample inside cage (a) top view, and (b) side view. Sample outside the cage (c) top view, and (d) side view.

It can be seen from Fig.3.23 that the NPs are not melted when placed inside the cage, but they are completely melted when placed outside. Furthermore, from the SEM top view (Fig.3.23.a vs c), the NPs placed inside the cage have acquired a hexagonal shape (inset of fig.3.23.a), and have been etched to only 74 % of their initial area, while those on the outside of the cage are now rounded (due to having melted) and have been etched to 24 % of their initial area. This experiment (samples placed inside and outside the cage) was repeated using 600 nm particles: first at 1 kW continuous plasma power for 3 minutes, then at 500 W for either 3 mins or 5 mins. The resulting SEM images for 1 kW experiment are shown in Fig.3.24.

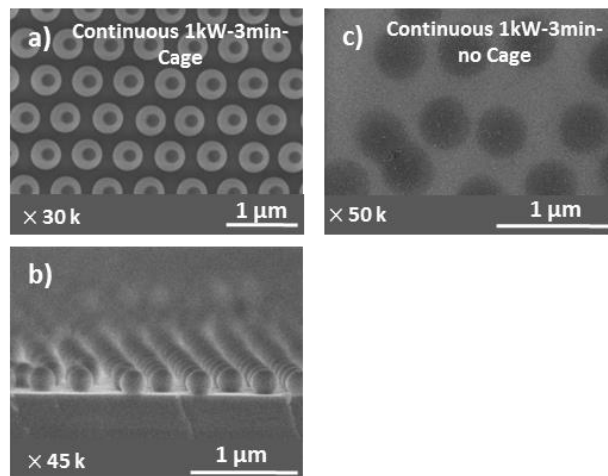


Fig.3.24: SEM images of the 600 nm NPs etched at 1 kW continuous for 3 min. Inside the cage (a) top view, and (b) side view. Outside the cage (c) top view.

It can be seen from Fig.3.24 that the NPs placed outside the cage are completely etched away, whereas

those placed inside the cage remain spherical, have a greater contact area with the surface, and have been etched to 50 % of their initial area.

Figure 3.25 presents the SEM images for the equivalent samples etched continuously at 500 W in O₂ plasma for 3 min and 5 min.

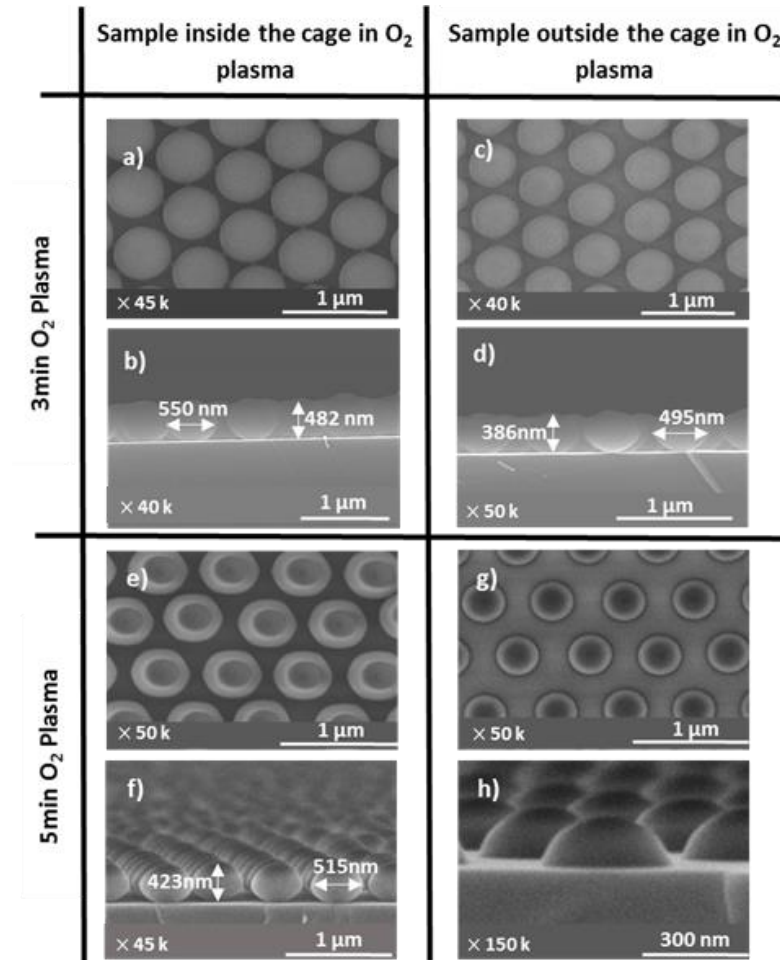


Fig.3.25: SEM images of 600 nm NPs etched at 500 W continuous O₂ plasma. 3 min plasma for sample inside cage (a) top view, and (b) side view, and for sample outside cage (c) top view, and (d) side view. 5 min plasma for sample inside cage (e) top view, and (f) side view, and outside cage (g) top view image and (h) side view.

It can be seen that for the shorter plasma etching time of 3 min, (as in Fig.3.24) and when decreasing the plasma power by half, no melting is observed, neither inside nor outside the metal cage (Fig.3.25.a, b, c, and d). However, the areal etching rate does vary; from the SEM top view, the spheres inside the cage are reduced to 80 % of their original area, while this value is 65 % for the spheres outside. From the SEM side view images (Fig.3.25.b, d, and f) one notes that the vertical etching rate of the samples is higher than the lateral rate and therefore the spheres take on ellipsoid shapes. This shape is slightly more pronounced outside the metal cage; the height of the spheres (now ellipsoids) inside the cage is 482 nm (~80 %), whereas it is 386 nm (~64 %) outside the cage. However, both outside and inside the cage, the ratio of vertical-to-lateral etching rate is similar (2.2 vs 2.0).

Using the images of Fig.3.25.a-d, one can make some comments about the role of ions and radicals in the process, observing that the cage decreases the vertical etching rate of the NPs by around 43 % and the lateral rate by 49 %. Due to the transparency of the cage (78 %), at least 22 % fewer etching radicals would arrive on the caged sample (if the radical flux was one dimensional), whereas 95 % fewer ions arrive (as measured). It can therefore be stated that it is the radicals that are primarily responsible for the sample etching.

In order to check if any NP melting can be observed at 500 W, the plasma duration was increased further to 5 min and the corresponding SEM images are shown in Fig.3.25.e, f, g, and h. The NPs placed outside the cage are indeed melted (reduced to 39 % of initial area) but not the ones inside (74 %). Using a metal cage therefore prevents NPs melting, at the cost of a decreased etching rate.

The technique of cycling the plasma was then combined with the use of the metal cage, and NPs were exposed to plasma powers of 500 W for 3 min and 1 kW for 2 min. The corresponding SEM images are shown in Fig.3.26.

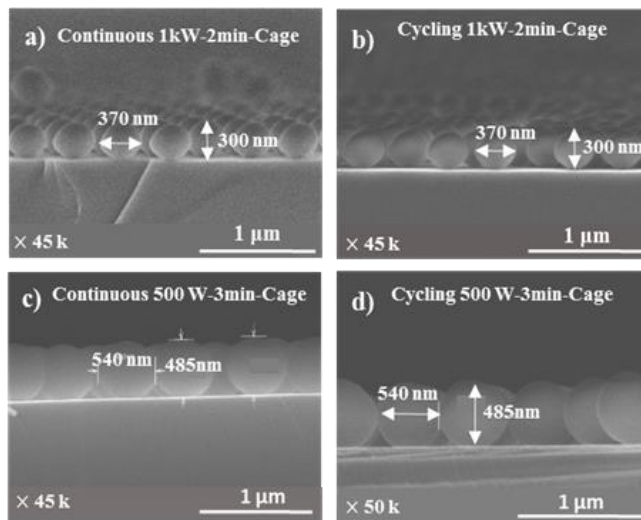


Fig.3.26: SEM cross section of 400 nm NPs etched inside metal cage using a plasma power of 1 kW for 2 min, (a) continuous and (b) cycling, and 500 W plasma for 3 min, (c) continuous and (d) cycling.

It can be noted from the SEM side-view images of Fig.3.26.a and 3.26.b that no difference in etching rate is observed between the cycled and continuous 1 kW plasma. The same is observed for the lower plasma power of 500 W for 3 min (Figs.3.26.c and 3.26.d). This supports the view that radicals are principally responsible for etching, while the ions are responsible for heating and melting. However, it contradicts the case presented in Fig.3.19 and 3.21 where the etching rate of the NPs in the cycled plasma is higher compared to the continuous plasma. This is probably because of the larger surface area provided by the metallic grid (Fig.3.26) in close vicinity of the sample, which may induce faster drop of oxygen radical concentration in the plasma-off phase due to enhanced recombination.

In order to study the role of ions in NP melting independently of the etching process, a known O₂ plasma treatment was followed by an Ar plasma (40 sccm of Ar, 2 mTorr pressure and 500 W power were used). This set of processes was applied to NPs placed on silicon substrates. First, the NPs were partially etched using O₂ plasma. Figures 3.27.a and b show the top- and side- view, respectively, of the etched NPs on silicon. The samples were then placed outside the metal cage, and an Ar plasma at 500 W was applied to the etched NPs for 5 min. SEM images of the resulting samples are shown in Fig.3.27.c, and d.

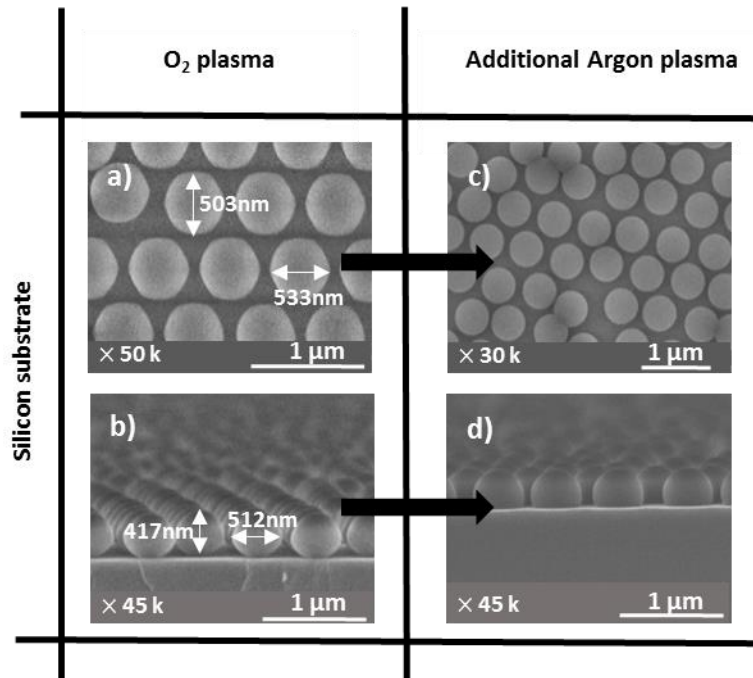


Fig.3.27: SEM images of 600 nm NPs etched in a continuous O₂ plasma at 500 W for 5 min inside metal cage. Si substrate (a) top view, (b) side view. SEM images after an additional 5 min 500 W Ar plasma without metal cage, (c) top view and (d) side view.

Comparing Fig.3.27.a and b to c and d, a few changes can be noted. Although NPs are not further etched, and have not taken on a “melted” appearance, the Ar plasma exposure does lead the NPs to have a greater contact with the silicon substrate (Fig.3.27.d) as though they had “softened”, and some of the NPs (Fig.3.27.c) seem to have almost fused together. This confirms that mainly the ions are responsible for NP heating, which can eventually lead to softening or melting.

3.2.3 Evolution of particle shapes

In this section, the evolution of the shape of the NPs during etching is discussed in more detail. A number of different characteristic “shapes” can be noted from the experiment results of this study. At the first steps of etching, a hexagonal shape is observed, regardless whether or not the sample is placed inside the metal cage. This shape is presumably due to a shadowing effect by nearest neighbors; a lower flux of etching radicals will arrive at the point of the particle in contact with another (from the directions of its nearest neighbors), and a greater flux from the direction of the second nearest neighbors (the largest gap). We quantify this evolution by plotting the aspect ratio (ratio of the largest width to smallest width when viewed from above in SEM) for all 600 nm NPs as a function of O₂ plasma etching time (Fig.3.28) and NP etching percentage (Fig.3.29). It should be noted that a large value of this ratio will also be observed if the particle takes on an ellipsoid shape. The type of shape adopted is indicated on the figures.

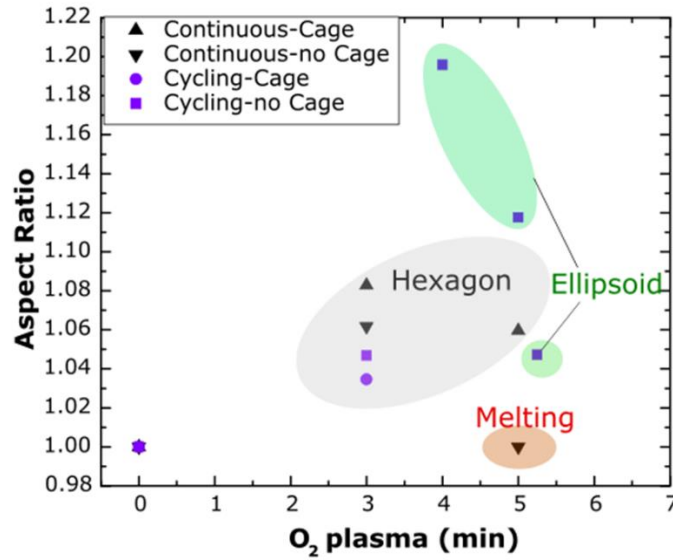


Fig.3.28: Aspect ratio between largest and smallest width observed by SEM top view images as a function of O₂ 500 W plasma exposure time.

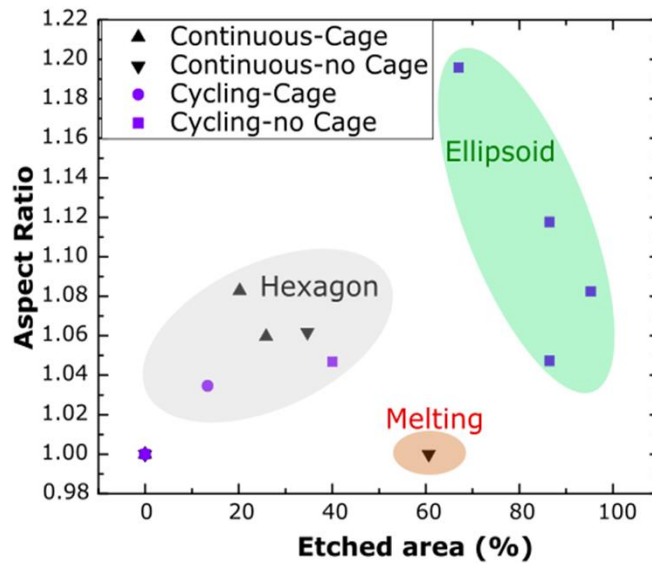


Fig.3.29: Aspect ratio between largest and smallest width observed by SEM top view images as a function of NPs etched percentage area at 500 W plasma.

It is seen from figs.3.28 and 3.29 that for all cases using 500 W plasma (continuous or cycles, cage or not) the hexagonal shape eventually disappears as the samples either melt or become ellipsoids. This is consistent with the “nearest neighbor shadowing” model proposed- once the NPs are sufficiently far apart, the shadowing effect becomes negligible. For the greatest amount of etching, the degree of departure from a perfect circle (even for no melting) is strongly dependent on the process used.

The origin of the ellipsoid shape and how much it can be minimized was therefore then explored through two sets of experiments, performed on 600 nm and 800 nm NPs. For both sets of experiments, a cycled 500

W O₂ plasma was used, and for times up to more than 5 min. The SEM top view images for the 600 nm particles are shown in figs.3.30.a to d, and those for the 800 nm particles in figs. 3.31.a and 3.31.b.

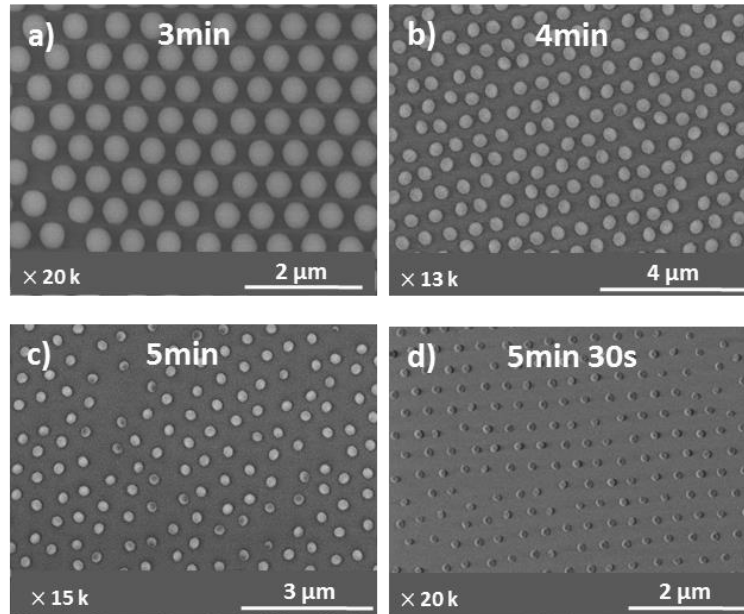


Fig.3.30: SEM top-view images of 600 nm NPs etched using 500 W cycled O₂ plasma for (a) 3 min, (b) 4 min, (c) 5 min, and (d) 5 min 30 s.

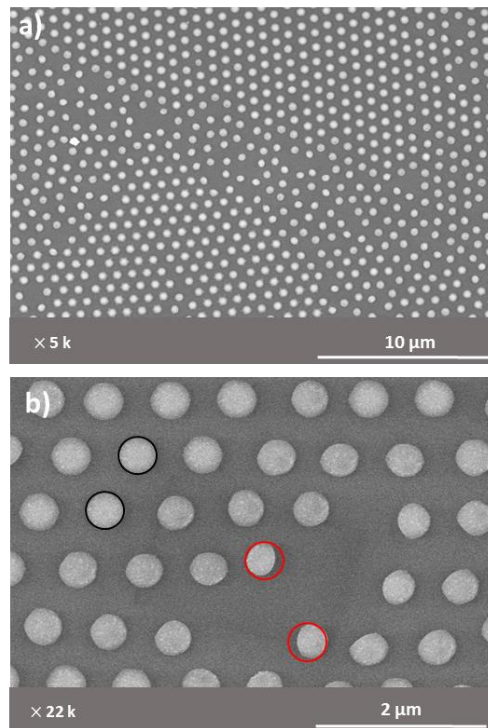


Fig.3.31: SEM images of 800 nm NPs showing the top view of the Si sample etched in cycling O₂ plasma at 500 W for 5 min 15 s (a) at low magnification and (b) high magnification on which two of the spherical NPs shapes are marked in black circles and two of the ellipsoid NPs shape are marked in red.

In figs.3.30 and 3.31, both spherical and ellipsoid shapes can be observed in top view. Such ellipsoid shapes have been previously reported in the literature [205] [204], wherein it was attributed to NPs shifting positions when toppling over. In Fig.3.31.a, it can additionally be seen that the ellipsoid shape is most likely to appear between two highly ordered domains. This can be probably attributed to asymmetric etching of the NPs due to a greater flux of etching radicals from the gap between two ordered domains. This asymmetric flux could accelerate the occurrence of toppling.

To further investigate this phenomenon, SEM top- and side- view images were acquired on samples using the conditions of Fig.3.31, for both a shorter (4 min, Fig.3.32.a and b) and similar (5 min 15 s, Fig.3.32.c and d) time.

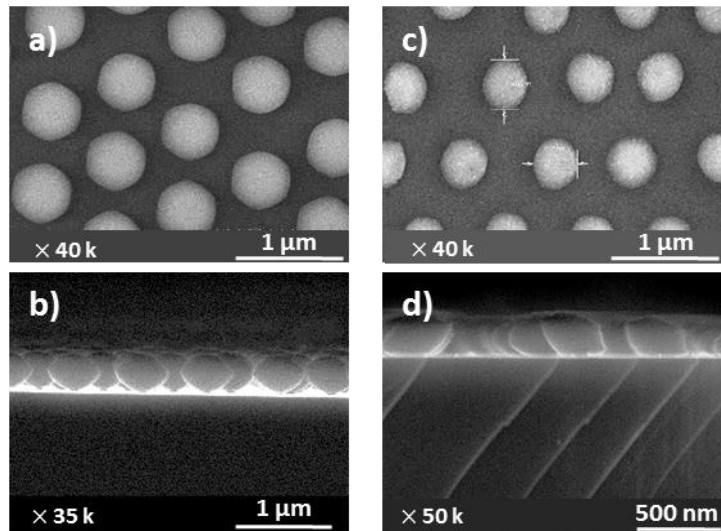


Fig.3.32: SEM images of 800 nm NPs etched using 500 W cycled O₂ plasma. After 4 min (a) top view, (b) side view, and after 5 min 15 s (c) top view, and (d) side view.

After an etching time of 4 min, the NPs have a hexagonal form when viewed from above (Fig.3.32.a), but a diamond-like shape with a small footprint in contact with the substrate when viewed from the side (Fig.3.32.b). Further etching of the NPs (5 min 15 s) causes some of them to topple over (Fig.3.32.d). This toppling probably occurs when the apex of the diamond-like shape becomes very sharp, creating a very unstable structure, pulled down either by gravity or attractive forces between the NP and the surface.

The diamond-like shape observed in Fig.3.32.b is an unexpected outcome. This shape is observed even more clearly when the NPs being etched have been deposited on a Si sample covered with ~120 nm of thermally grown SiO₂. A side view SEM image is shown in Fig.3.33 (this is the same sample shown in top-view in Fig.3.30.a).

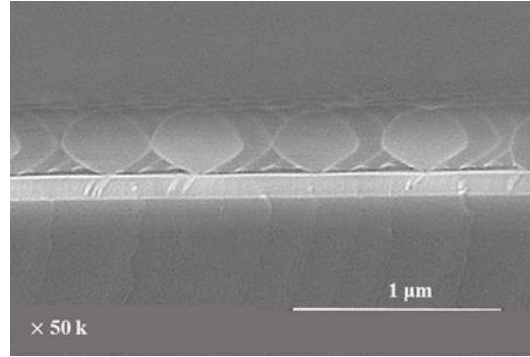


Fig.3.33: SEM cross section image of 600 nm NPs etched by 500 W cycled O₂ plasma for 3 min.

One explanation for this diamond-like shape may be that the NPs have reached their glass transition temperature during the plasma-on period, and are pulled up toward the plasma due to electrostatic forces, then solidify again during the plasma-off period. The electrostatic force may be due to the electric field in the plasma sheath pulling negatively charged objects on the surface back into the plasma. The cycled plasma plays a key role in allowing the NPs to approach their glass transition temperature, without continuing to heat and melting completely (the melting point of bulk polystyrene is around 240 °C).

It is clear then that the ellipsoidal shape when viewed from above is simply due to a NP toppling over. The more relevant observation is therefore the ellipsoid shape observed in the side view SEM images of figs.3.23.b, 3.25.(b,d,f), 3.26, and 3.27.b as also previously described in the literature [204][205][212].

To quantify this ellipsoid shape, the ratios between the horizontal and vertical dimensions are plotted with the percentage of the etched area as a function of the etching time in Fig.3.34. NPs that have completely melted and wetted the surface are indicated.

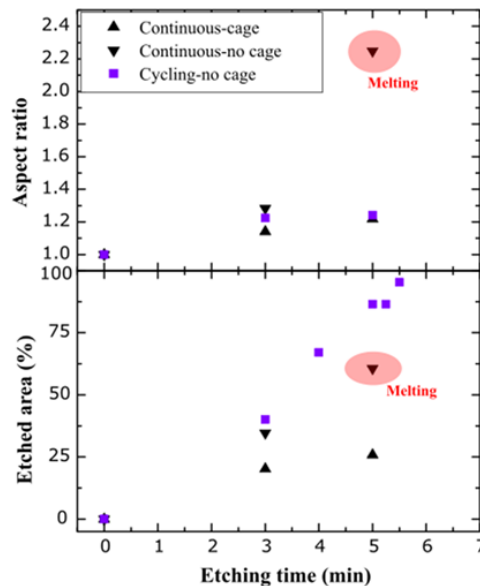


Fig.3.34: Aspect ratio (ratio of horizontal to vertical dimensions) of the etched NPs (calculated from the SEM side-view images), and their percentage of etched area (calculated from the SEM top view) plotted as a function of etching time (500 W O₂ plasma power).

It can be seen in Fig.3.34 that the degree of this ellipsoid shape is dependent on the details of the process used. The ratio is slightly smaller for samples inside the metal cage, and is lowest for the samples where the glass transition temperature was approached but the NPs did not completely melt. For the NPs that did experience melting (continuous with no cage after 5 min etching), aspect ratios greater than 2 are observed. These data provide a good guide for processes, depending on the needs of the application (perfect arrays vs non-melted spheres vs very open areas, etc.).

It can furthermore be seen that the cycling mode produces the highest etching rate, followed by the continuous mode where no cage is used, and the lowest etching rate is observed when the continuous mode is used with the cage. As previously stated, this is probably due to exposure to O radicals during the "plasma off" time (the etching time for the cycled plasma neglects this period).

Finally, it should be noted that the cycling technique allows almost complete etching of the NPs without causing melting. We therefore detail the limits of size reduction for NPs of various sizes using this process that never causes melting. This limit is important information for our application of forming point-contacts in solar cells, where a very small coverage is required [84][83][68]. A Cycled O₂ plasma at 500 W was used for varying times to etch 400 nm, 600 nm, and 800 nm NPs, and the results are in Fig.3.35.

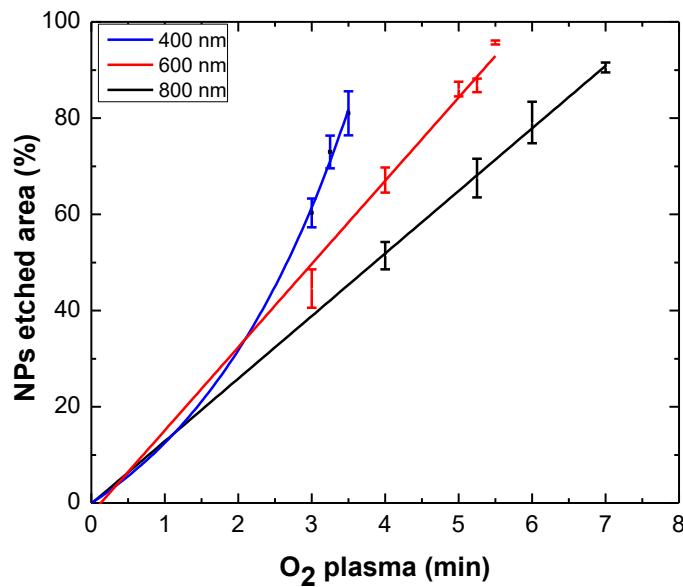


Fig.3.35: Etched area of NPs with initial diameters of 400 nm, 600 nm, and 800 nm as a function of etching time, using a 500 W cycled plasma.

As shown in Fig.3.35, by cycling the plasma, it was possible to reduce the areas of the 400 nm, 600 nm, and 800 nm NPs to 19 %, 4 %, and 9 % of their initial areas, respectively without melting them or having them to leave the surface. Using the precise values of NP initial sizes, the 425 nm, 607 nm, and 784 nm NPs were etched to diameters of 185 ± 21 nm, 125 ± 17 nm, and 240 ± 13 nm, respectively. The SEM images corresponding to these minimal final coverages are shown in Fig.3.36.

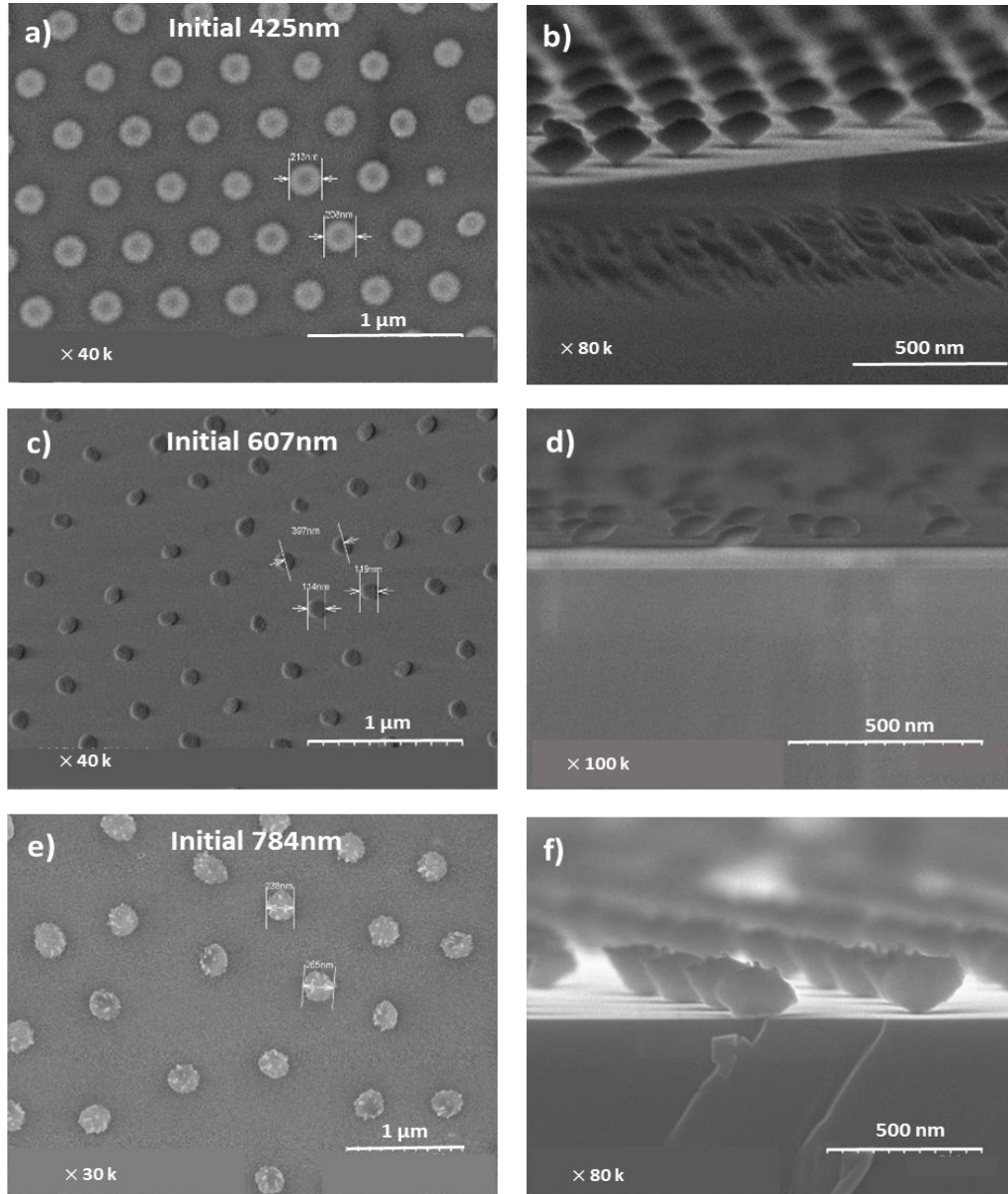


Fig.3.36: SEM images (a), (b) of 400 nm NPs etched to 19 % of their initial diameter, (c), (d) 600 nm NPs to 4 % and (e), (f) 800 nm NPs to 9 %.

In Fig.3.36, it is seen that the initially 400 nm, 600 nm and 800 nm etched NPs have spherical shapes in the SEM top view images, and that the surface of the 800 nm etched NP appears rough (Fig.3.36 (e) and (f)). Such a porous surface can appear after a long plasma treatment due to the difference in etching rates for the amorphous and crystalline phases of polystyrene [211]. This roughness was also previously observed by other groups using different plasma etching durations [203],[200] ,[204] and [212]. In tilted view, the 400 nm NPs have a diamond like shape, and toppled ellipsoid shapes for the 600 nm and 800 nm NPs

3.2.4 Summary-NP etching

The etching of polystyrene NPs using MD-ECR O₂ plasma was investigated. The use of a high-power, 1 kW continuous plasma caused the NPs to melt and wet the surface. This effect could be mitigated by cycling the plasma, reducing the power, or placing the particles behind an ion shielding metal cage, indicating that it is the energetic ions that are the main source of heating.

A hexagonal shape was observed in top-view at the beginning of all the etching processes, regardless the conditions used, most likely due to geometrical shadowing of radical fluxes. An ellipsoid shape was also observed from the SEM side view images, presumably due to a higher vertical etching rate than horizontal one.

For longer etching times under conditions that avoided melting, a “toppling” effect was observed, making the array of nanoparticles less regular. However, if one is interested in avoiding the toppling effect of the NPs and conserving the initial periodic distribution, then the sequential use of processes may be of interest. One may first use a process that partially melts or softens the NP, before using a low-heating process to etch them down.

Concerning our application, what matters is to have NPs as distanced as possible to achieve coverage percentages suitable for point contacts application (below 10 % which is achievable using the 600 nm NPs), to reduce lateral diffusion by doping which is detailed in ch.5. Therefore, using cycling plasma was of interest to our application as it was possible to shrink three sizes of NPs diameter down to between 4 % and 19 % of their original areas without causing melting, giving a certain level of control over hole pitch and coverage. Using the precise values of NP initial sizes, the 425 nm, 607 nm, and 784 nm NPs were etched to diameters of 185 ± 21 nm, 125 ± 17 nm, and 240 ± 13 nm, respectively.

3.3 Nanoparticle Removal

Different layers were used to cover the NPs in this work: evaporated Al, SiO₂ and SiN_x deposited by MD-ECR PECVD, a-SiC_x:H deposited by RF-PECVD (all the deposition steps will be more detailed in the next part of this chapter). This is done in order to form holes in the dielectric layers using three different approaches as was seen in Fig.3.1 of this chapter.

The difficulty of removing the NPs depends mainly on the layer covering them. When evaporated aluminum was used, the NP removal was not difficult because of the shading effect. However, when more conformal layers were deposited by PECVD, the NP removal became more difficult. Therefore, different methods have been tried to remove the NPs like ultrasonic bath of toluene and acetone, 1-methyl-2-pyrrolidone, tape stripping, high temperature heating, and O₂ plasma. Some of these methods were more successful than others; the successful ones will be presented in this chapter and the others will be added to the appendix.

3.3.1 NP removal via solution

The goal of this part is to remove the NPs after being covered with a masking layer either by washing away the NPs physically or dissolving them chemically.

[Evaporated Al] In this part, the masking used is evaporated Al. NPs of 100 nm diameter are first deposited on the c-Si substrate by spin coating. Then around 20 nm Al is evaporated on the NPs, followed by NP removal. The evaporated Al will not be deposited everywhere on the substrate; because of the shadowing

effect, the Al will be deposited just in between and on top of the NPs as shown in Fig.3.37. This effect will facilitate the NP removal by toluene as there will be more NP surfaces exposed to the solution.

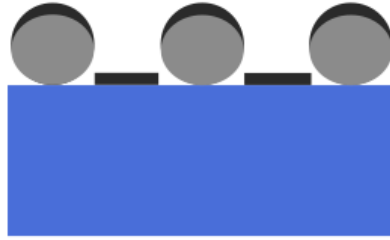


Fig.3.37: Schematic illustration of Al evaporated on NPs.

The SEM images corresponding to the aluminum covered surface both before and after NP removal (using a toluene US bath) are shown in Fig.3.38. It can be seen that the holes are completely opened, and they conserve a diameter close or higher than the NPs size used due to the shading effect.

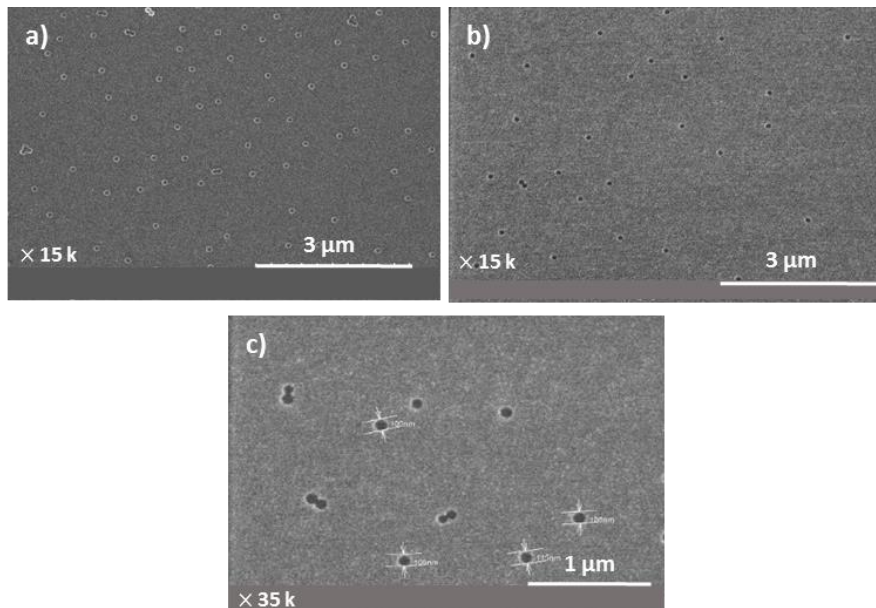


Fig.3.38: (a) 100 nm NPs deposited on c-Si substrate, (b) and (c) Holes in evaporated Al after NP removal.

[Evaporated Al on softened NP] Although using Al as a mask can facilitate NP removal, it can become limited if the NPs used are melted. For instance, if the floating transfer technique is used to disperse the NPs, an etching step can be needed to etch the NPs, which can also result in their melting depending on the O₂ plasma parameters used (as was seen in the previous part of this chapter). Two cases of NPs softening are presented in Fig.3.39 and Fig.3.40.

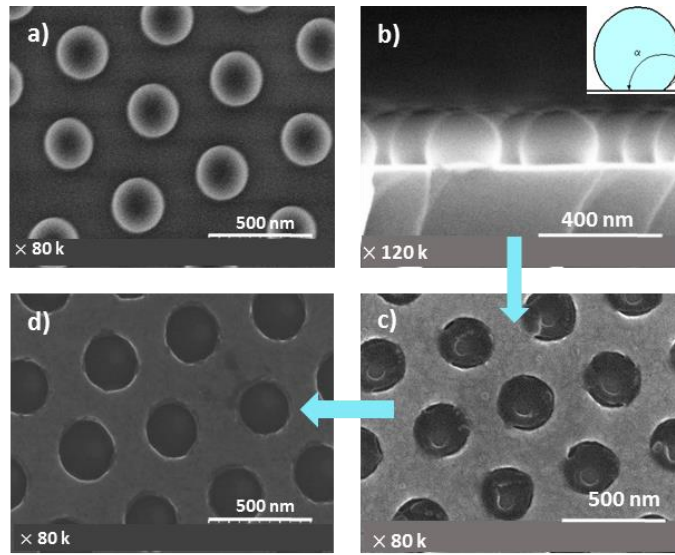


Fig.3.39: SEM images of cSi sample on which 400 nm NPs were etched after 1.5 min in an O₂ plasma at 1 kW (a) top view image, (b) side view. (c) and (d) top view images after NP removal.

A monolayer of 400 nm NPs was first deposited by the floating transfer technique and then the NPs were etched for 1.5 min in an O₂ plasma at 1 kW. The SEM top view and cross section of the sample after NP etching are shown in Fig.3.39.a and Fig.3.39.b. A slight NPs softening occurs on this sample as it can be seen from Fig.3.39.b.

A mixture of chlorobenzene and isopropanol ultrasonic (US) bath was applied on this sample during 20 min. The sample state, after this treatment is shown in Fig.3.39.c. NP residues remain inside the holes because of NP softening. It was possible to get rid of these residues by applying an additional 30 min of toluene US bath as shown in Fig.3.39.d.

An example of more significant NP melting is shown in Fig.3.40 (already shown in Fig.3.20).

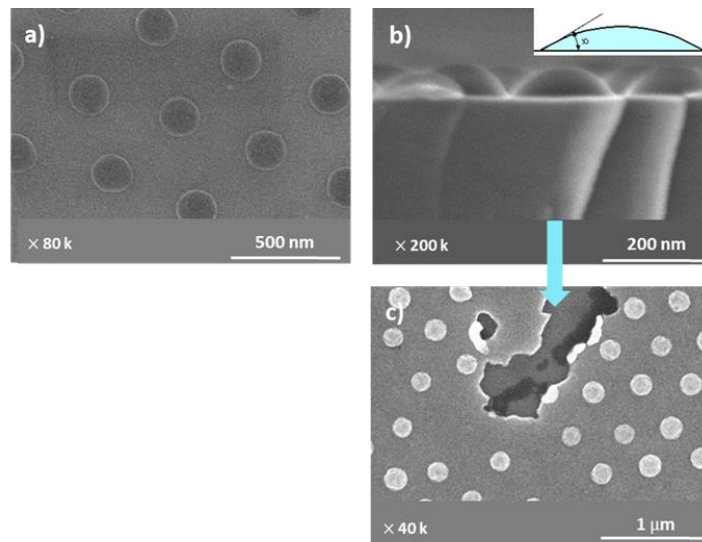


Fig.3.40: SEM images of cSi sample on which 400 nm NPs were etched after 2 min in an O₂ plasma at 1 kW (a) top view, (b) cross section. (c) top view images after a NP removal trial.

Nanoparticle Deposition, Etching and Removal

The NPs are more severely melted after an O₂ plasma of 2 min. The evaporated Al will therefore totally cover the NPs, and it becomes difficult to remove them via solution etching. After applying 20 min of toluene US bath it wasn't possible to remove any of the NPs. A more aggressive method is needed to remove the NPs in this case.

In summary, if the contact angle between the NP and the surface form an obtuse angle as in Fig.3.39.b it will be possible to etch the NPs via solution after aluminum evaporation. However, if this angle is an acute angle, then it will become more difficult to do so.

[Less severe softening case] Another example of NP removal on cSi sample after 600 nm NP etching in a cycling plasma at 500 W for 5 min is shown in Fig.3.41.

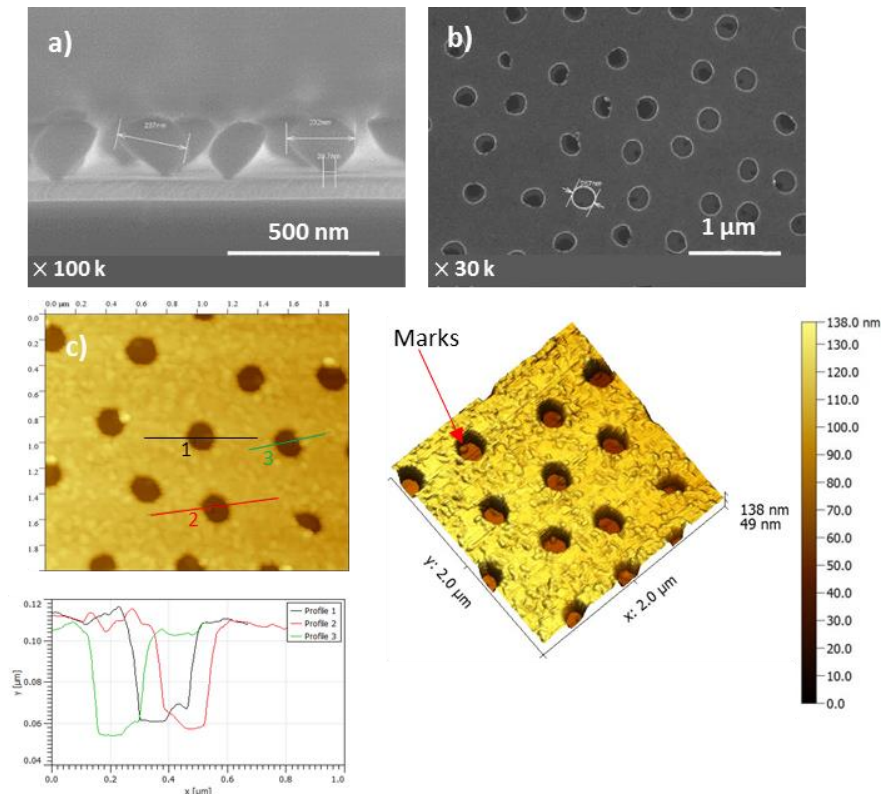


Fig.3.41: SEM images of cSi sample covered with evaporated Al after etching the 600 nm NPs in a cycling plasma at 500 W for 5 min. (a) side view of cSi sample before Al evaporation, (b) top view of cSi sample after NP removal. (c) AFM topography and 3D view corresponding to Fig.b.

It can be seen from Fig.3.41.a that the contact area between the NPs and the substrate is small. The sample underwent 30 min US bath of toluene in order to remove the NPs after Al evaporation. Despite that this trial is successful some marks from the NPs remain inside the holes. This is confirmed from the surface line profiles as well as the 3D AFM image shown in Fig.3.41.c where the bottom part of the holes is not flat.

Even after an additional 30 min of toluene US bath, it was still not possible to get rid of these marks. O₂ plasma of 7 min was applied on the sample shown in Fig.3.41 and the corresponding AFM images are shown in Fig.3.42.

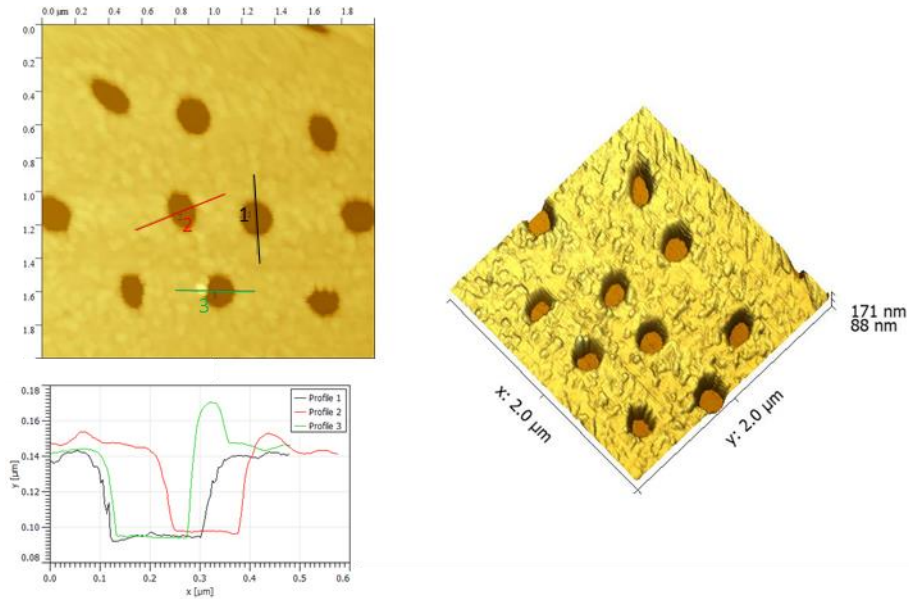


Fig.3.42: AFM images of the sample of Fig.3.41 after applying an additional 7 min of O₂ plasma. AFM topography image with surface profile lines (left), and sample 3D view (right).

As it was possible to remove these marks after applying ~7 min of O₂ plasma (the holes bottom becomes straight), this suggests that these marks are residues from the PS NPs due to their softening during the initial O₂ plasma.

[cSi + SiO₂ sample] On another cSi sample, 600 nm diameter NPs are deposited on a cSi sample covered with a thick SiO₂ layer. After etching the NPs by O₂ plasma in a cycling plasma at 500 W for 5 min and 30 s, 30 nm Al was evaporated on this sample. 30 min toluene US bath followed by 12 min isopropanol US bath was used on this sample to remove the NPs. The sample SEM image is shown in Fig.3.43.a.

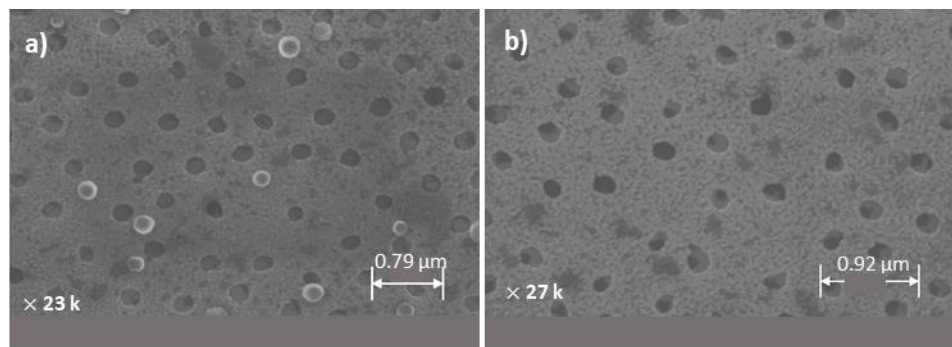


Fig.3.43: SEM images of the sample where 600 nm etched NPs were used. (a) After applying 30 min toluene US bath and (b) an additional 30 min toluene US bath.

It was shown that the NPs are not totally removed on this sample. An additional similar US bath was needed in order to remove the majority of the NPs and this is shown in Fig.3.43.b.

Some residues are as well seen in this case, similarly to Fig.3.41. As an SiO₂ layer is deposited on the cSi substrate prior to NP deposition, this sample will undergo a plasma etching of the oxide through the holes before doping (in ch.5). It is expected that these residues will be removed during this process.

[SiO₂ as NPs masking layer] A SiO₂ layer was also deposited by MD-ECR PECVD on NPs using 40 sccm O₂, 5sccm SiH₄ at 1 kW and 1 mTorr. The NP removal in this case becomes more difficult as the deposition by PECVD is isotropic compared to the aluminum evaporation which is more anisotropic.

The deposition of 18 nm and 10 nm of SiO₂ was done on 50 nm and 100 nm spin coated NPs on cSi samples, respectively. The SEM of the samples before and after 100 nm NP removal are shown in Fig.3.44.a and b, respectively. Fig.3.44.c and Fig.3.44.d show the same results for the 50 nm NPs.

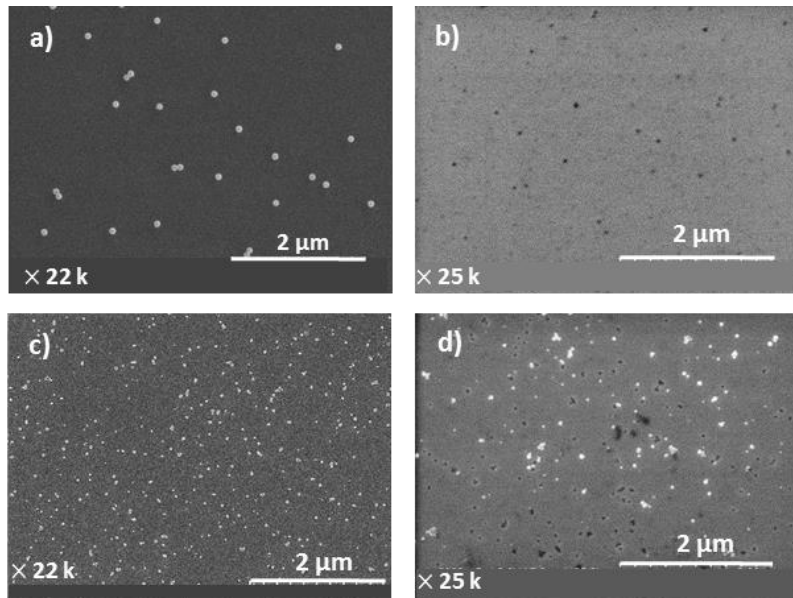


Fig.3.44: SEM top view images where (a) 100 nm NPs are spin coated on cSi sample, (b) 100 nm NPs are removed after covering them with 10 nm SiO₂. (c) 50 nm NPs spin coated on the cSi sample, and (d) 50 nm NPs removed after covering them with 18 nm SiO₂.

It can be seen that the 100 nm NPs were totally removed after 30 min of toluene US bath, but only partially removed for the 50 nm NPs. It is more difficult to remove the smaller NPs, especially in this case as a thicker SiO₂ thickness was deposited on them. Furthermore, it was confirmed that the 50 nm NPs solution is polydisperse. The distribution in NP diameters can be seen from the higher magnification SEM image (Fig.3.45.a), and was confirmed using Malvern Nano ZS ZetaSizer measurements (Fig.3.45.b).

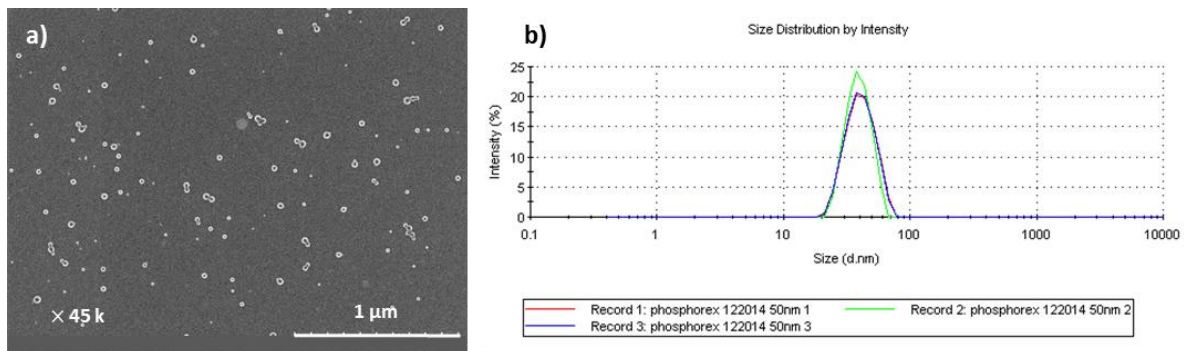


Fig.3.45: (a) SEM top view image of 50 nm NP spin coated on cSi sample, (b) size distribution of 50 nm NPs suspension.

The Zaverage value measured (the mean value of the NPs diameter) is 38.3 nm which is smaller than the nominal one (50 nm). The polydispersity (Pdi) is 0.082, where Pdi is calculated as the square of the standard deviation/mean diameter. Hence the standard deviation in our case is 10.97 nm. This means that some particles are much smaller than 50 nm which can make the NP removal after covering them with 18 nm SiO₂ even more difficult or impossible.

[DI US bath] An US bath of DI water of 45 min was also applied on a cSi sample where 12 nm SiO₂ was deposited by MD-ECR PECVD on 100 nm spin coated NPS. The SEM after NP removal is shown in Fig.3.46.

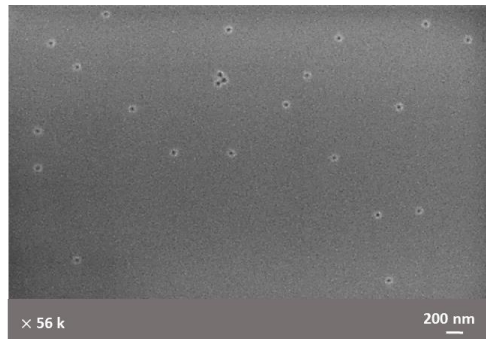


Fig.3.46: SEM top view of the sample covered with 12 nm SiO₂ after NP removal by H₂O US bath.

It is seen from Fig.3.46 that all the NPs are removed due to the physical vibrations of the US bath itself. This is an encouraging result, as it shows NP removal without using aggressive solvents.

[SiN_x as NPs masking layer] SiN_x was also deposited as a mask by MD-ECR PECVD using 80 sccm N₂, 10 sccm SiH₄ at 1 kW and 2 mTorr. Around 12 nm SiN_x was deposited on 100 nm spin coated NP on cSi and it was removed using a 30 min toluene US bath followed by 12 min isopropanol US bath, as shown in Fig.3.47.

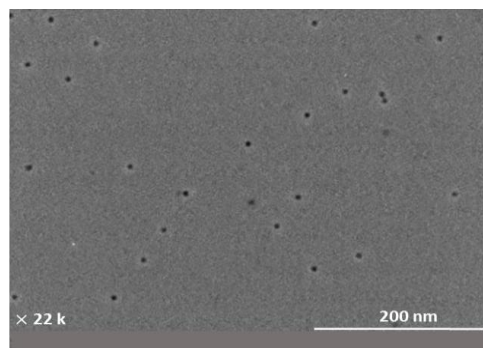


Fig.3.47: SEM top view of cSi sample covered with 12 nm SiN_x after NP removal by toluene US bath.

It can be seen from Fig.3.47 that the NPs are completely removed, and the holes are well defined.

[SiO₂ and SiN_x masking layer on metallic substrate] As NPs will be used in ch.4 to form point contacts for thin film solar cells, these NPs were as well deposited on metallic substrate in this part of the chapter. SiO₂ and SiN_x were used as a mask on the NPs deposited on metal-coated glass substrates.

The NPs are dispersed on glass samples covered with aluminum or silver. ITO is used between the metal-coated glass and the PIN junction in order to avoid the diffusion of the metal into silicon and to improve

the back-reflector reflectivity. Different trials of NP removal (after dielectric coverage) were performed on metal-coated glass substrates with and without ITO.

[Glass-Al substrate] We first present the results for samples where the NPs and dielectric were deposited directly on the Al-glass substrate (no ITO). The SEM images of samples using both SiO₂ and SiN_x are shown in Fig.3.48.

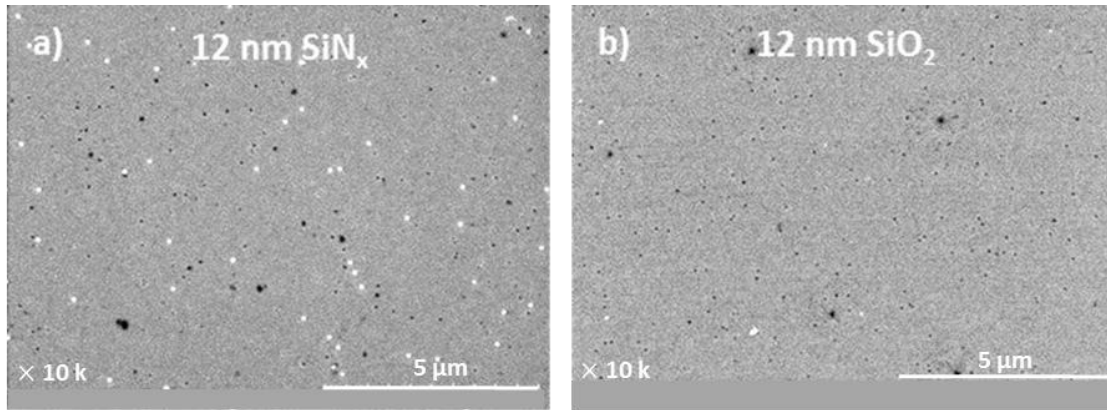


Fig.3.48: SEM images of Al-coated glass where 100 nm NPs are spin coated and removed after being covered with (b) 12 nm SiN_x and (d) 12 nm SiO₂.

Using a toluene US bath, it is easier to remove the NPs covered with SiO₂ than with SiN_x. A toluene US bath of 30 min followed by a 12 min isopropanol US bath was more than enough to remove the majority of the NPs covered with SiO₂ (Fig.3.48.b), whereas three trials of the same cycle (30 min Toluene US bath + 12 min isopropanol US bath) was not enough to remove the NPs covered with SiN_x (Fig.3.48.a).

[Glass-Al-ITO substrate] NPs of 100 nm diameter were also spin coated on glass-Al substrates on which 100 nm ITO is deposited. The samples underwent a 30 min toluene US bath followed by 12 min isopropanol US bath after being covered by SiO₂ and SiN_x. The SEM images corresponding to these samples after NP removal are shown in Fig.3.49.

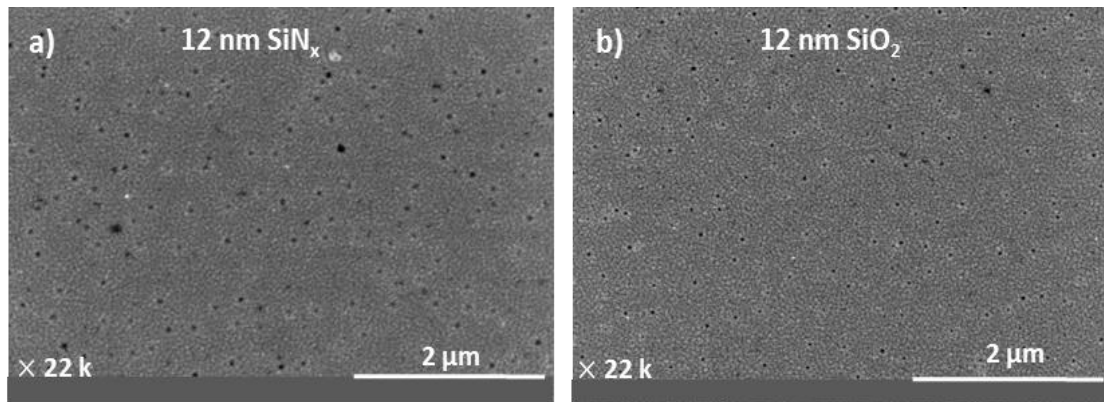


Fig.3.49: SEM images after NP removal on the Al-ITO sample (a) covered with 12 nm SiN_x and (b) 12 nm SiO₂.

The NPs were totally removed for both samples after the same duration of US bath. It was notable that the removal of the NPs on the sample covered with SiN_x layer, where no ITO was used (Fig.3.48), was more difficult than the case where ITO was used (Fig.3.49).

[Glass-Ag] The same steps were done on a substrate where Ag-ITO is deposited on the glass instead of Al-ITO, 12 nm SiN_x and SiO_2 were again used as a mask on the spin coated NPs. The SEM images in Fig.3.50 show the case before and after NP removal by applying 30 min US bath of toluene and 12 min US bath of isopropanol.

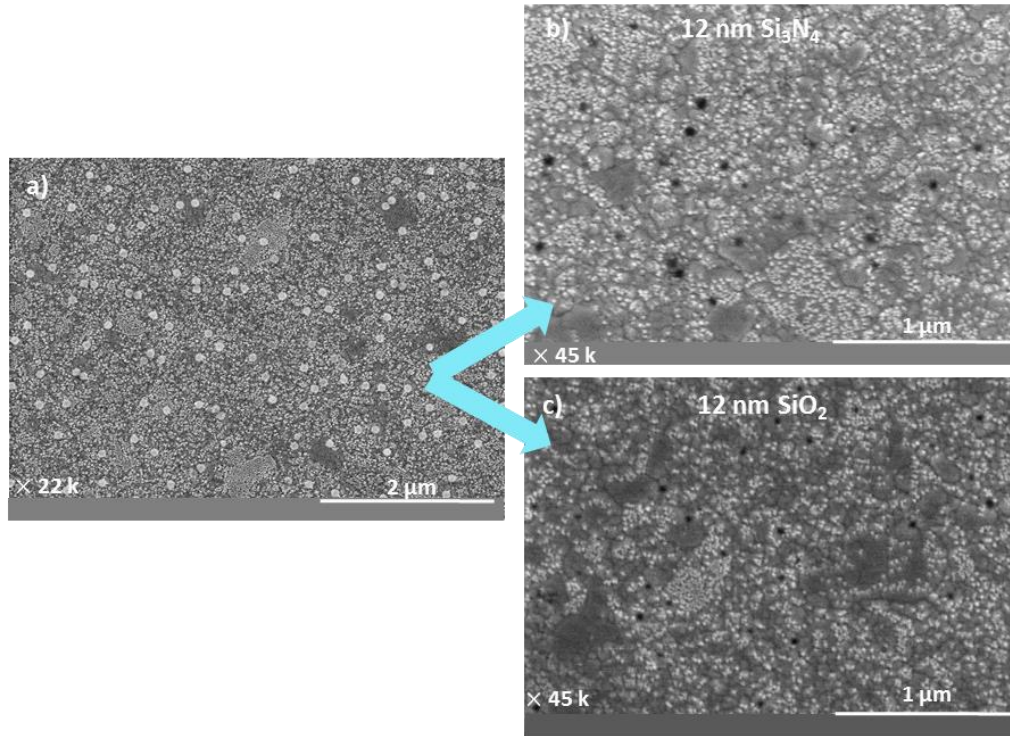


Fig.3.50: SEM images of the Ag-ITO sample (a) where 100 nm NPs are spin coated, (b) where NPs are removed after being covered with 12 nm SiN_x , and (c) where NPs are removed after being covered with 12 nm SiO_2 .

It was seen from Fig.3.49 and Fig.3.50, that the holes formed in the SiN_x layer appear bigger than those formed in the SiO_2 layer knowing that the same NPs diameter and dielectric thickness were used.

[a-SiC_x:H as NPs masking layer] a-SiC_x:H will be used as a mask in approach C (Fig.3.1) to locally etch the Al_2O_3 through the Al masking holes, which will be detailed in ch.4. Therefore, a-SiC_x:H is used as NP masking layer in this section. It was deposited by RF-PECVD (Elettrorava S.p.A) at room temperature by using 1.2 sccm of SiH_4 , 60 sccm of CH_4 , at 1 mbar and 18 W. The NPs were first dispersed on a cSi sample with native oxide, and later on a layer of Al_2O_3 or thick SiO_2 covering the cSi substrate. The thickness used of a-SiC_x:H was between 20 nm and 30 nm.

[cSi substrate] NPs of 100 nm were spin coated on a cSi sample and then covered with 30 nm a-SiC_x:H. The sample underwent 45 min of toluene US bath followed by 15 min of isopropanol US bath. The corresponding SEM image is shown in Fig.3.51.a.

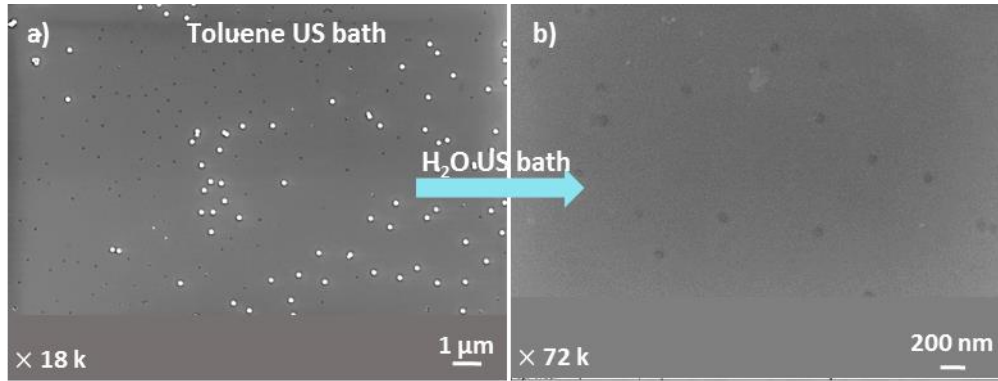


Fig.3.51: SEM images of cSi sample where the NPs are (a) partially removed after toluene US bath and (b) totally removed after an additional H₂O US bath.

This US bath was capable of partially removing the NPs. However by applying an additional 45 min of DI US bath on the same sample (Fig.3.51.b), it was possible to remove the remaining NPs on the sample (here we show a zoomed image of one area of the surface).

[cSi-SiO₂ sample] On another sample of cSi covered with SiO₂, 100 nm NPs were spin coated and covered with 30 nm of a-SiC_x:H. This sample underwent 1 hour of toluene US bath followed by 15 min isopropanol US bath and the corresponding SEM image is shown in Fig.3.52.a.

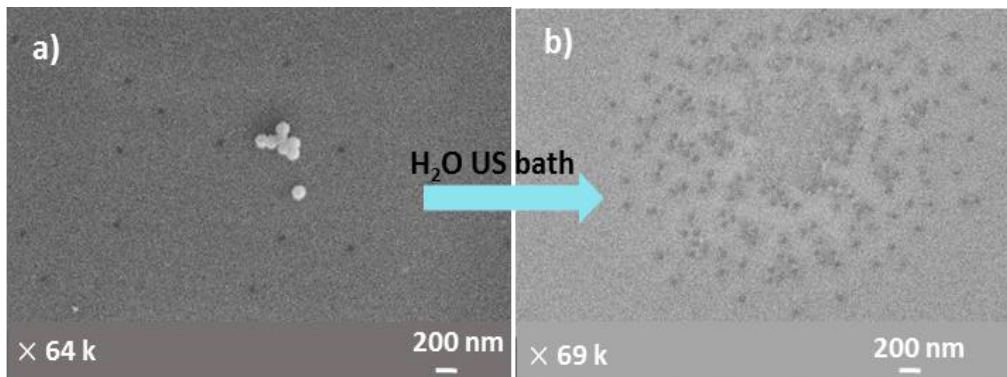


Fig.3.52: SEM images of cSi-SiO₂ sample where NPs are (a) partially removed after toluene US bath and (b) totally removed after an additional H₂O US bath.

It was seen that the toluene + Isopropanol US bath only partially removed the NPs. However by applying an additional 45 min of DI US bath it was again possible to remove the majority of the NPs as shown in Fig.3.52.b.

[cSi-Al₂O₃ sample] A reduced thickness (20 nm) of a-SiC_x:H was deposited on 100 nm NPs spin coated on 50 nm of Al₂O₃ covering a cSi sample. 1hour US bath of DI water was applied on this sample and the SEM image is shown in Fig.3.53.a.

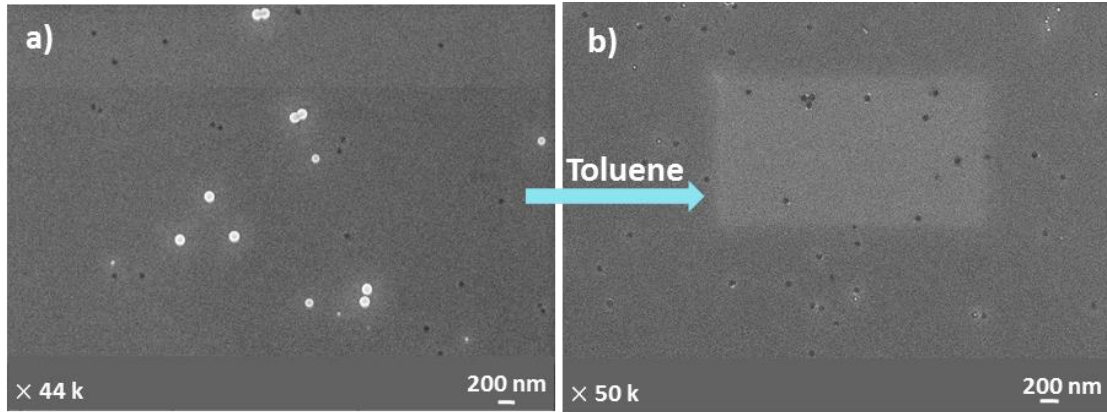


Fig.3.53: SEM images of cSi-Al₂O₃ sample where NPs are (a) partially removed after H₂O US bath and (b) totally removed after an additional toluene US bath.

It was seen (Fig.3.51 and Fig.3.52) that an additional H₂O US bath was needed in order to remove the majority of the NPs. However, applying a H₂O US bath alone was not enough to remove the NPs as can be seen from Fig.3.53.a. An additional 1h toluene US bath followed by 15 min isopropanol US bath was needed to remove the majority of the NPs as can be seen from Fig.3.53.b.

Two other similar samples to the one shown in Fig.3.53 (20 nm deposited a-SiC_x:H) underwent 1 hour toluene US bath followed by 15 min isopropanol US bath was applied on them. The corresponding SEM images are shown in Fig.3.54.

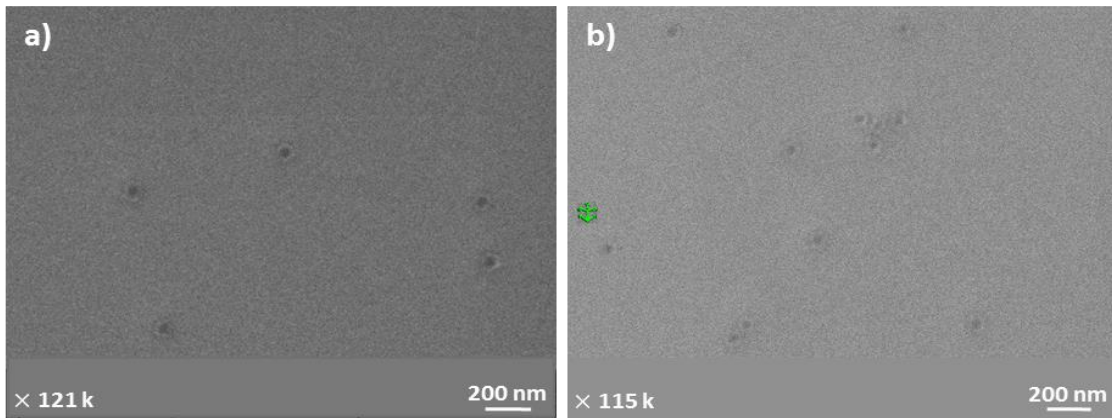


Fig.3.54: (a) and (b) SEM images of cSi-Al₂O₃ samples where the NPs are removed after toluene US bath.

In this case the toluene US bath alone was enough to remove most of the NPs on these samples, probably because of the thinner a-SiC_x:H thickness used. The diameters of the opened holes are around 50 nm. Comparing the mask materials of a-SiC_x:H (Fig.3.51 to Fig.3.54) to SiO₂ or SiN_x deposited by MD-ECR (Fig.3.44 to Fig.3.50), it can be seen that US baths of ~30 min of toluene or 45 min of H₂O are sufficient enough to remove the NPs when the mask is SiO₂ or SiN_x, whereas 1h of toluene or toluene followed by DI was necessary to remove the NPs covered with a-SiC_x:H mask.

It was previously seen in Fig.3.38, 42, 43, 44 that it was easier to remove the Al-covered NPs when they are spin coated than when they are deposited by floating transfer technique and etched in an O₂ plasma. In

order to see if it this holds when using a-SiC_x:H as a mask, it was deposited on NPs deposited by floating transfer.

A monolayer of 800 nm NPs was deposited on a cSi sample, etched (Fig.3.36.e and f) and covered with a-SiC_x:H (25-30 nm). The sample underwent 1 h toluene US bath followed by isopropanol and DI water rinsing. The SEM images are shown in Fig.3.55.

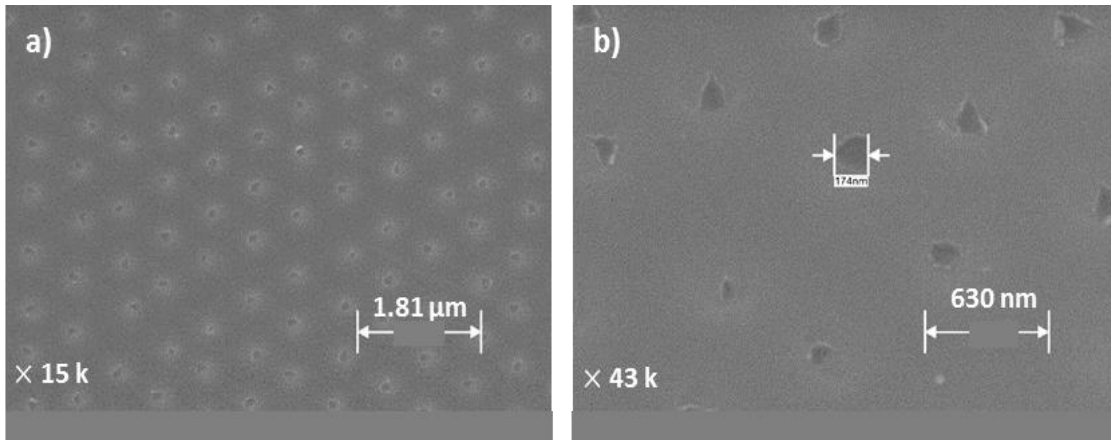


Fig.3.55: (a) and (b) SEM images of cSi sample where the 800 nm etched NP are removed after toluene US bath.

It is seen that toluene US bath was enough to remove the NPs in the samples shown in Fig.3.55. The same was observed when 600 nm NPs were used. AFM measurements were also done on the same sample to confirm that the holes are opened, and are shown in Fig.3.56.

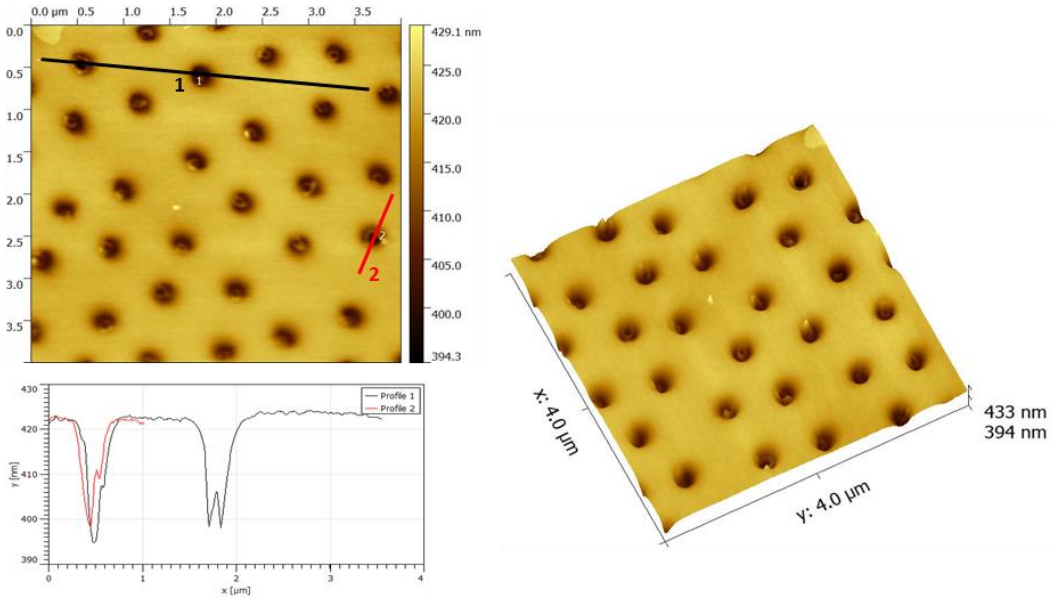


Fig.3.56: AFM images of the sample of Fig.3.55. AFM topography image with surface profile lines (left), and sample 3D view (right).

It is observed that the holes are opened; however, there are some residues inside the openings probably due to the imperfect NP removal.

[Summary] In this section, different cases of NP removal via solution have been presented. Some key lessons can be stated:

- When Al is used as a mask, it was easier to remove the spin coated NPs than those deposited by floating transfer technique and etched by O₂ plasma.
- It was more difficult to remove the 50 nm polydisperse NPs than the 100 nm NPs when SiO₂ MDECR is used as a mask.
- It was easier to remove the NPs when SiO₂ and SiN_x are used as the masking layer compared to the case where a-SiC_x:H is the mask.

In the next section, an alternative technique using Kapton tape will be used to remove the NPs.

3.3.2 NP removal by tape stripping

It was seen in the previous section that removing the NPs by US bath was effective, but time-consuming and occasionally imperfect. A physical NP removal method using kapton tape was tried as this method is straight forward and time saving. Results are presented in this section

[SiO₂ as NPs masking layer] The kapton tape was used on a cSi sample where 100 nm NPs are spin coated and covered with 12 nm SiO₂ deposited by MD-ECR PECVD. The tape was stuck on the sample surface and then removed. The SEM images after NP removal is shown in Fig.3.57.

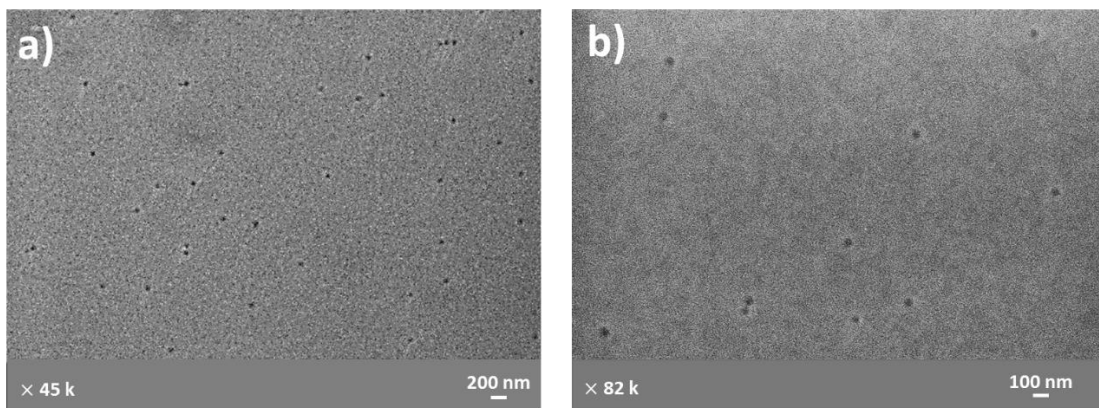


Fig.3.57: a) and b) SEM top view of the cSi sample covered with 12 nm SiO₂ after NP removal by Kapton tape.

As shown in Fig.3.57, the NPs were efficiently removed using this method. However, this method remains limited by the possibility of breaking the sample while removing the tape, and the adhesive residue that can be left behind requires an additional cleaning step.

A substrate of Si on which 50 nm AlO_x is deposited was covered with 600 nm etched NPs and coated with 30 nm a-SiC_x:H. The kapton tape method was applied on this sample followed by 15 min isopropanol US bath and DI rinsing to make sure that no residues from the kapton tape remain on the sample surface. The corresponding SEM image is shown in Fig.3.58.

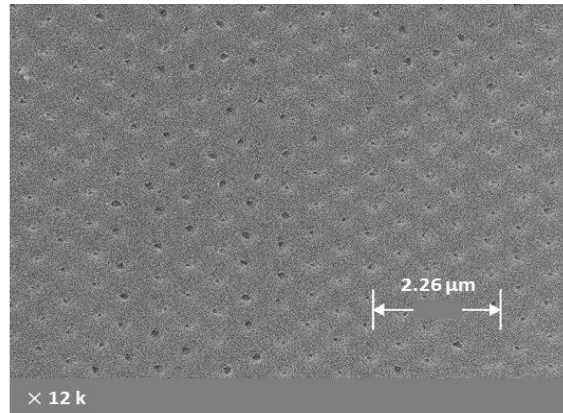


Fig.3.58: SEM image of the cSi- AIO_x sample where 600 nm etched NPs are removed by using kapton tape.

It is again seen that the NPs are efficiently removed from the sample, as shown in Fig. 3.58.

[Comparison] Another similar substrate was covered with 800 nm etched NPs and coated with 30 nm a-SiC_x:H. It was cut into three pieces, and on each of them a different method was used to remove the NPs: toluene US bath, kapton tape, and soft silicon tape, and SEM images of the results are shown in Fig.3.59.a, 3.59.b and 3.59.c, respectively.

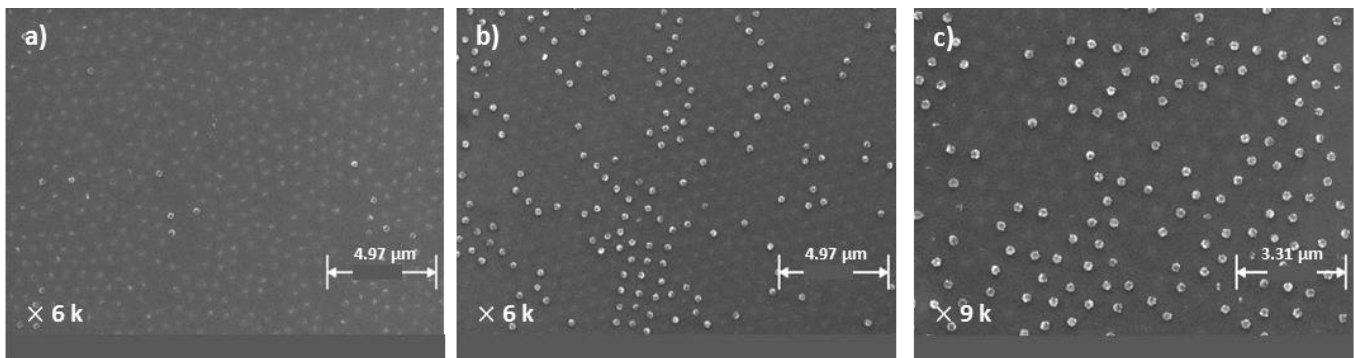


Fig.3.59: SEM images of the cSi-AIO_x sample where 800 nm etched NPs are removed after applying (a) toluene US bath, (b) Kapton tape and (c) soft silicon tape.

It is clearly seen that by applying US baths of 45 min of toluene followed by 15 min of isopropanol, it was possible to remove most of the NPs. However, the mechanical removal by both types of tape was much less efficient. (*The holes are not seen clearly in these images; however one should note that the initial NPs distribution is periodic, thus the areas where no NPs are seen should be related to NP removal.*)

We can now compare these three cases where kapton tape was used to remove the NPs (Fig.3.57, Fig.3.58, and Fig.3.59). It can be noted that only the sample shown in Fig.3.59 had poor NP removal. This is probably due to the difference in these three cases in the NPs morphology and not size. Cross-sectional images of the NPs in all three cases are shown in Fig.3.60.

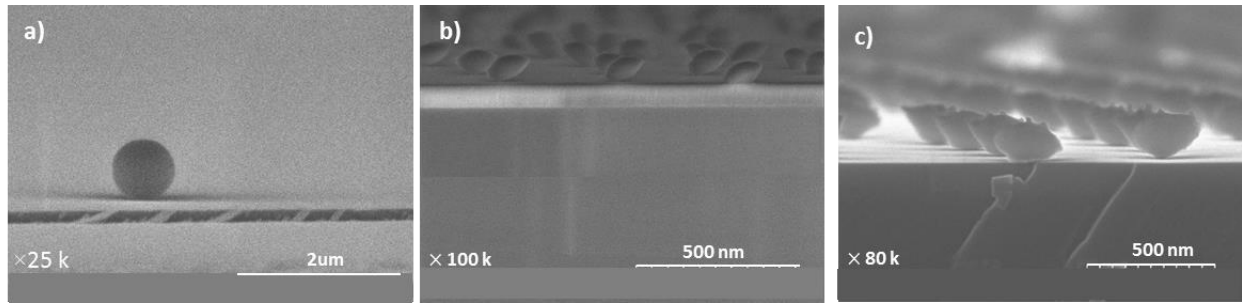


Fig.3.60: SEM cross section images of (a) 100 nm spin coated NPs, (b) 600 nm etched NPs and (c) 800 nm etched NPs.

It can be seen that the etched NPs are no longer spheres (as are the spin coated ones). However, the 600 nm etched NP remained smoother than the 800 nm etched NPs, which may aid in having a better contact between the tape and the NPs.

Other less efficient methods were attempted to remove the NPs, such as annealing the sample at a temperature of 300 °C and 400 °C after covering the NPs with SiO₂ or a-SiC_x:H, putting the sample in an O₂ plasma, or in a 1-methyl-2-pyrrolidone solution at 120 °C after covering it with the dielectric. These trials were mostly unsuccessful, and are presented as an appendix.

3.3.3 Summary-NP removal

In the previous section, two main techniques were used to remove the NPs; solution US bath and tape stripping.

For the US bath removal, the following points were observed:

- It was easier to remove the NPs when using Al as the masking layer compared to the other cases. However, it was easier to remove the spin coated NPs compared to these deposited by floating transfer technique and etched by O₂ plasma.
- It was more difficult to remove the 50 nm polydisperse NPs than the 100 nm NPs when SiO₂ by MDECR is used as a mask.
- It was easier to remove the NPs when SiO₂ and SiN_x are used as the masking layer compared to the case where a-SiC_x:H is the mask.

When using the tape stripping method, the following points were observed:

- By using tape stripping, it was more difficult to remove the 800 nm etched NPs than the 600 nm etched NPs and the 100 nm spin coated NPs. This is probably due to a smoother contact area between the NPs and the tape.
- This method is efficient and time saving. However, it can lead to sample breakage during the removal and residues on the sample surface because of the tape.

Although the US bath technique was more time consuming than the tape stripping, it will be used to remove the NPs in the next part of this thesis. This is to avoid sample breakage, contamination, and incomplete NP removal for unusual etching conditions.

3.4 Chapter Summary

[NP deposition] In this chapter three NP deposition techniques were used; spraying, spin coating and floating transfer technique.

The spraying technique was discarded in this thesis as it forms many zones of deposited NP with different densities on the same sample which is not adequate for solar cells application.

The spin coating technique gives higher NP surface coverage when smaller NPs are spin coated. The deposited NP density decreases when the surface roughness of the sample increases. This deposition method will be used in ch.4 to deposit NPs on AlCu-ITO-glass sample which showed a NP density of $5.49 \text{ NPs}/\mu\text{m}^2$.

The floating transfer technique was used to form NP monolayers. This technique required an additional O_2 plasma etching step to get the low surface coverage required. The pitch between holes is fixed by the initial NPs diameter used.

[NP etching] The etching of polystyrene NPs using MD-ECR O_2 plasma was investigated. The use of a high-power, 1 kW continuous plasma caused the NPs to melt and wet the surface. This effect could be mitigated by cycling the plasma, reducing the power, or placing the particles behind an ion shielding metal cage, indicating that it is the energetic ions that are the main source of heating.

A hexagonal shape was observed in top-view at the beginning of all the etching processes, regardless the conditions used, most likely due to geometrical shadowing of radical fluxes. An ellipsoid shape was also observed from the SEM side view images, presumably due to a higher vertical etching rate than horizontal one.

For longer etching times under conditions that avoided melting, a “toppling” effect was observed, making the array of nanoparticles less regular.

It was shown to be possible to shrink three sizes of NPs diameter down to between 4 % and 19 % of their original area without causing melting, giving a certain level of control over hole pitch and coverage.

[NP Removal] The last part of this chapter presented the two main methods used to remove the NPs after covering them with evaporated Al, SiO_2 , SiN_x and a- $\text{SiC}_x\text{:H}$ deposited by PECVD. It was seen that by using Al evaporated as a mask it was easier to remove the NPs using a toluene US bath compared to the other cases. It was also easier to remove the NPs covered with SiO_2 and SiN_x deposited by MD-ECR compared to those covered with a- $\text{SiC}_x\text{:H}$ deposited by RF-CCP. It was as well easier to remove the spin coated NPs compared to these deposited by floating transfer technique followed by O_2 plasma etching when toluene US bath or tape stripping is used to remove the NPs. A toluene US bath will be used in the next chapters to remove the NPs for issues of reproducibility.

The main result of this chapter is a set of recipes to produce holes in layer stacks to use in the next chapters of the thesis. These are summarized using the images of Fig.3.61. The holes were obtained by using a mask of 30 nm of a- $\text{SiC}_x\text{:H}$ or evaporated Al, and either 100 nm spin coated NPs, or 600 nm / 800 nm NPs by floating transfer and etching.

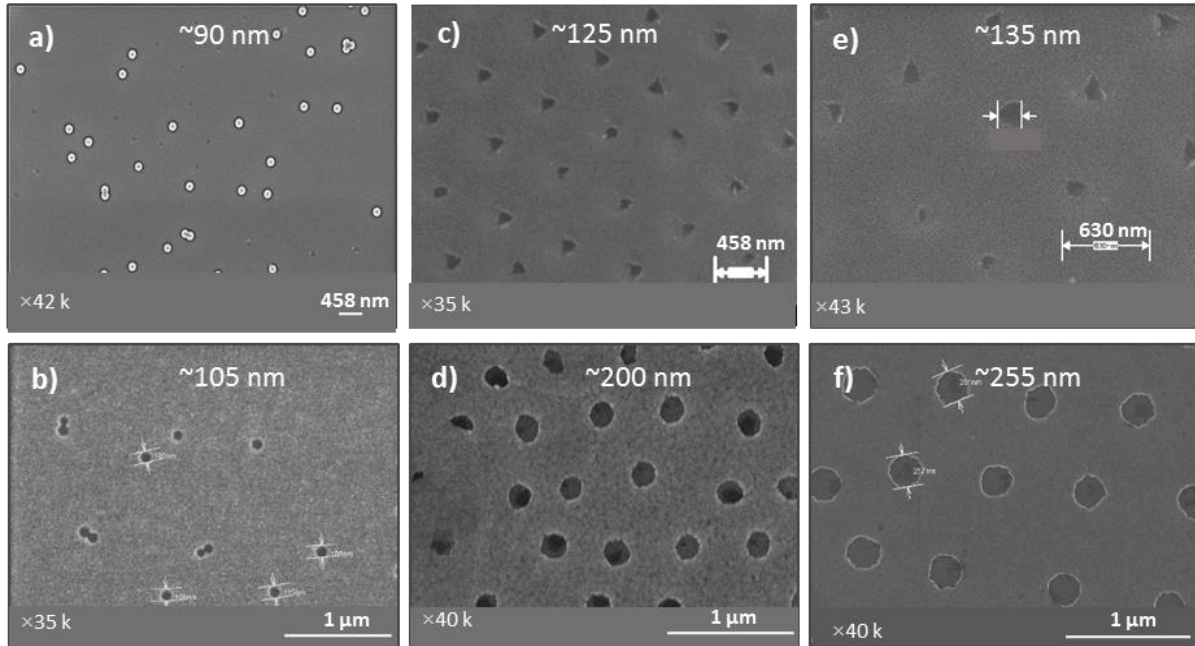


Fig.3.61: SEM images of cSi samples after NP removal. 100 nm spin coated initially covered with (a) 30 nm a-SiC_x:H and (b) 30 nm evaporated Al. 600 nm etched NPs initially covered with (c) 30 nm a-SiC_x:H and (d) 30 nm evaporated Al. 800 nm etched NPs initially covered with (e) 30 nm a-SiC_x:H, and (f) 30 nm Al.

It can be seen that when using a mask layer of 30 nm a-SiC_x:H the holes formed after NP removal have diameters of 90 ± 12 nm, 125 ± 35 nm and 135 ± 25 nm when using 100 nm spin coated NPs, 600 nm etched NPs, and 800 nm etched NPs, respectively. Bigger holes were observed for the mask of 30 nm evaporated aluminum: 105 ± 21 nm, 200 ± 18 nm and 255 ± 28 nm for 100 nm spin coated, 600 nm etched NPs and 800 nm etched NPs.

All of the parts presented in this chapter will be used in the next chapter as tools to develop three different approaches used to form holes in passivation or dielectric layers with thicknesses varying from 10 nm to 240 nm for solar cell applications.

Chapter 4: Characterization of nanoholes

| | | |
|---------|--|-----|
| 4.1 | <i>Forming nanoholes in thin dielectric layers</i> | 104 |
| 4.1.1 | Approach A: Covering the NPs with a thin dielectric layer..... | 104 |
| 4.1.1.1 | Electrical characterization using CP-AFM | 104 |
| 4.1.1.2 | CP-AFM – Holes in films on c-Si substrates | 105 |
| 4.1.1.3 | CP-AFM – Holes in films on coated glass substrates | 109 |
| 4.2 | <i>Forming nanoholes in thick dielectric layers</i> | 110 |
| 4.2.1 | Approach B: Using aluminum as a mask | 111 |
| 4.2.1.1 | ZnO-glass substrates | 111 |
| 4.2.1.2 | Silicon substrates..... | 113 |
| 4.2.1.3 | Summary-Approach B | 121 |
| 4.2.2 | Approach C: Using a-SiC _x :H as a mask..... | 121 |
| 4.2.2.1 | HF as wet etchant | 122 |
| 4.2.2.2 | RCA "Soft" as wet etchant | 122 |
| 4.3 | <i>a-Si:H test PV devices</i> | 126 |
| 4.3.1 | PIN Structure | 127 |
| 4.3.2 | NIP structure | 128 |
| 4.3.3 | Solar cell Characterization | 129 |
| 4.3.4 | Summary of a-Si:H Solar Cells..... | 135 |
| 4.4 | <i>Chapter Summary</i> | 136 |

Characterization of nanoholes

The previous chapter (Chapter 3) was focused on NP deposition, coating, etching, and removal. Three different NP deposition techniques were shown: spraying, spin coating and floating transfer technique. The spraying technique was discarded in this thesis as it is uncontrollable and would create different zones of dispersed NPs with different densities. As our goal is to have well separated NPs on the sample surface, spin coating and floating transfer techniques followed by O₂ etching will be used in this chapter to deposit the NPs. Spin coating will be used in this chapter to form holes in thin dielectric layers, whereas the floating transfer technique (plus etching) will be used to form holes in thicker layers. Both techniques allow the low surface coverage we require for our application.

Also, different methods of removing the NPs after covering them with thin layers were shown. It was concluded that toluene US bath remained the best one to remove the NPs, therefore it will be used in this chapter.

The aim of this chapter is to characterize nanoholes formed in a dielectric layer, of a thickness varying from 10 nm to 250 nm, on silicon and coated glass samples. Three approaches will be used to form the nanoholes: approach A consists of forming holes in thin dielectric layers by first dispersing the NPs on the cSi substrate and then depositing the thin dielectric layer on the NPs before removing them. In contrast, approaches B and C consist of first depositing the dielectric on the sample, then dispersing the NPs, before depositing a second masking layer. For approach B, an Al mask was evaporated on the NPs, and for approach C, an a-SiC_x:H masking layer was deposited by PECVD. These steps will be followed by NP removal and plasma or wet etching through the holes formed in the masking layer.

Four kinds of dielectric layers will be used; SiN_x and SiO₂ deposited by MD-ECR PECVD at RT, thermally grown SiO₂, and Al₂O₃ deposited by ALD.

These three approaches are summarized in Fig.4.1.

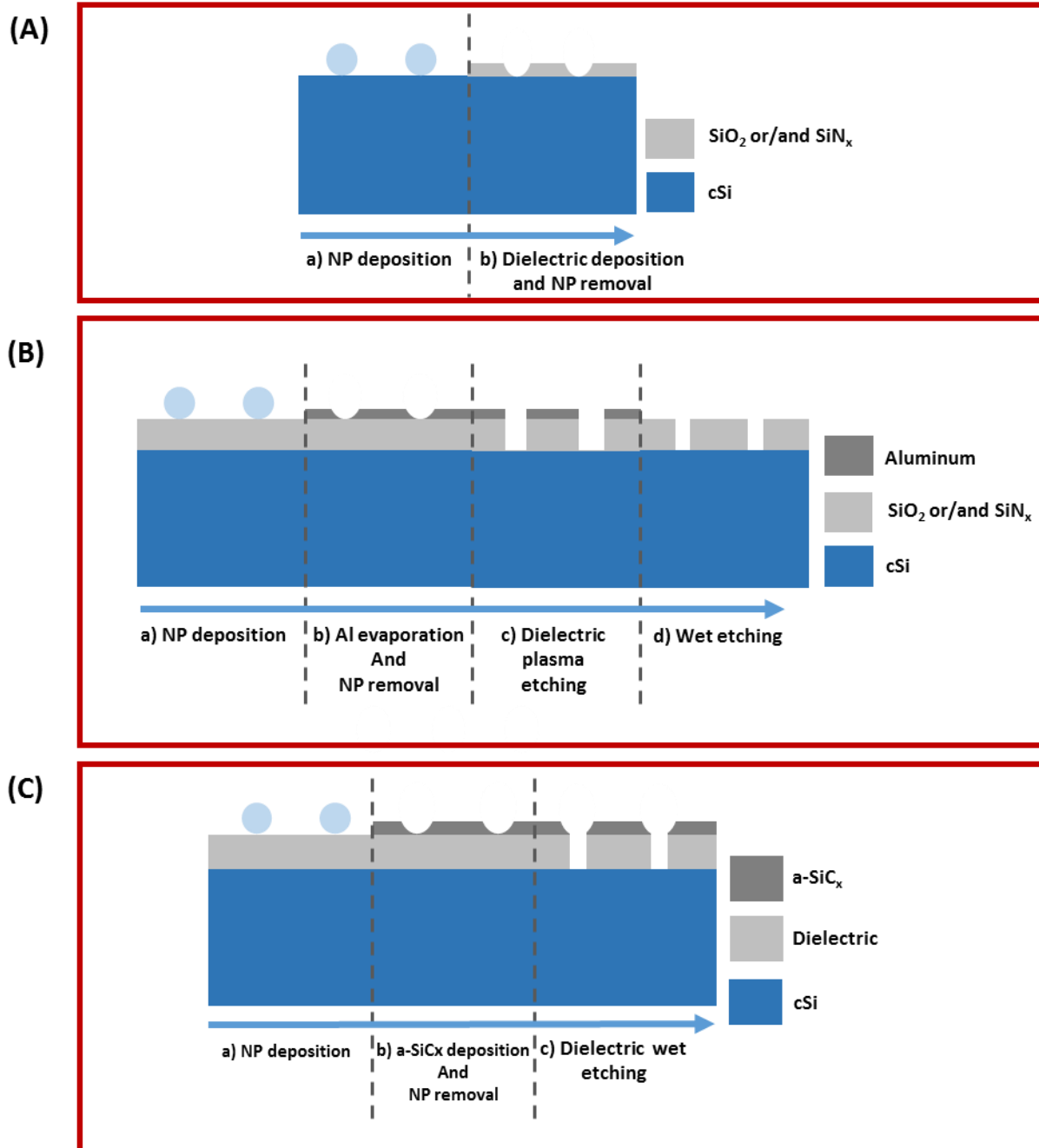


Fig.4.1: Schematic illustration showing three different approaches developed in this chapter; (A) forming holes in thin dielectric layer, (B) forming holes in thick dielectric layer by using evaporated Al as a masking layer, and (C) forming holes in thick dielectric layer by using a-SiC_x:H as a masking layer.

4.1 Forming nanoholes in thin dielectric layers

4.1.1 Approach A: Covering the NPs with a thin dielectric layer

Approach A consists of covering the dispersed NPs with a thin dielectric layer deposited at room temperature. The dielectric thickness in this case should be less than half the diameter of the deposited NPs in order to be able to remove the NPs in the next step.

In this work, the NPs were dispersed on a c-Si substrate as well as on metal-coated glass. The goal of forming a dielectric layer with holes on c-Si is to be able to use this approach for nanosized point contacts in solar cells. As for the dielectric layer with holes on a conducting substrate, it can be used as a back reflector for thin film solar cells. This application will be tested at the end of this chapter.

Approach A was first applied on a c-Si substrate with all the steps presented in Fig.4.2.

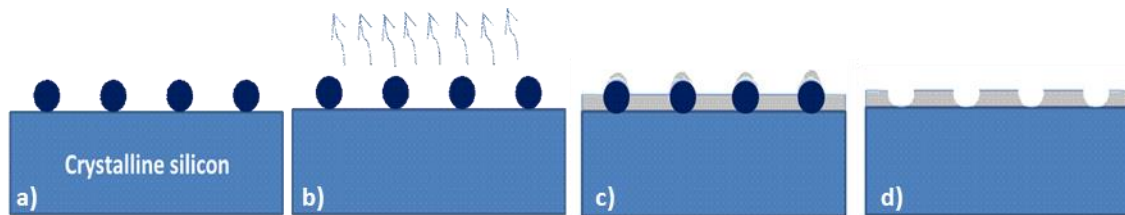


Fig.4.2: Schematic illustration of different steps of approach A; (a) Deposition of polystyrene NPs, (b) Substrate annealing at 50 °C, (c) Dielectric deposition at room temperature (RT) and (d) NP removal.

The 100 nm polystyrene NPs were first spin coated on a c-Si substrate followed by an annealing at 50 °C. A 10 nm thick layer of SiO₂ was then deposited at RT by MD-ECR on the NPs, which were then removed using US baths (30 min toluene + 12 min isopropanol). The SEM images of this sample before and after forming the holes in the dielectric layer were already shown in Fig.3.44.a and b of Chapter 3.

4.1.1.1 Electrical characterization using CP-AFM

To confirm that the holes formed in the dielectric layer can be electrically contacted and that this approach can be used to form point contacts in PERL cSi structures, a local resistance mapping by conductive probe atomic force microscopy (CP-AFM) was done on this sample.

The CP-AFM measurements were done in the GeePs laboratory, and a schematic of the CP-AFM setup is shown in Fig.4.3. The AFM tip is n⁺ Si coated with polycrystalline diamond doped with boron at the tipside of the cantilever (CDT-FMR-20), and has a radius around 100 nm. The polycrystalline diamond coating has a nanoroughness in range of 10 nm which reduces the tip radius to a few nm, leading to good resolution measurements. A DC voltage bias is applied on the sample side, as shown in Fig.4.3.b, resulting in the opposite bias on the surface. This setup allows one to measure the resulting current flowing through the tip as the sample surface is scanned in contact mode. With this technique, one can simultaneously examine the topography and conductive properties of the measured layers (as described in chapter 2).

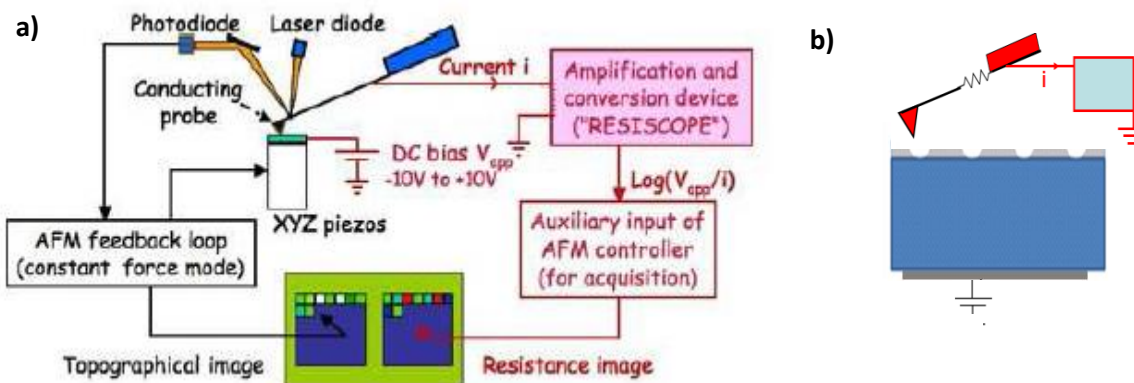


Fig.4.3: Sketch of CP-AFM measurement; (a) setup at GeePs with resiscope extension[213], (b) sample configuration and applied bias.

In most of the measurements, a positive bias was applied on the sample, hence a negative bias on the tip. A water meniscus is formed under the tip, and by applying a negative bias on the tip, water molecules are broken (H^+ , O^- , OH^-) and the anions (OH^- , O^-) move to the silicon surface, oxidizing it [213]. This effect is more important for high voltages. The measurements were performed in nitrogen (N_2) atmosphere to minimize the effects of tip induced oxidation.

It should be mentioned that there are two ranges of resolution for the measurements done by CP-AFM; a high-resolution measurement is obtained when the voltage bias used is smaller than 1 V. For this range of voltage, small current values can be measured ($\sim 10^{-13}$ - 10^{-14} A), hence higher values of resistance ($\sim 10^{13}$ - 10^{14} Ω). However, when higher voltages (~ 8 - 10 V) are used to electrically contacting the holes, the measurement resolution is reduced.

4.1.1.2 CP-AFM – Holes in films on *c*-Si substrates

In the very first trial, no electrical contact was made through the holes between the AFM tip and the silicon substrate when using large applied biases of ± 9 V in most of the parts of the sample. However, it was possible to contact through a few holes in some parts of the sample using 2 V (Fig.4.4). Being able to contact some holes at 2 V and not ± 9 V is probably due to inhomogeneity in the deposited oxide layer.

Characterization of nanoholes

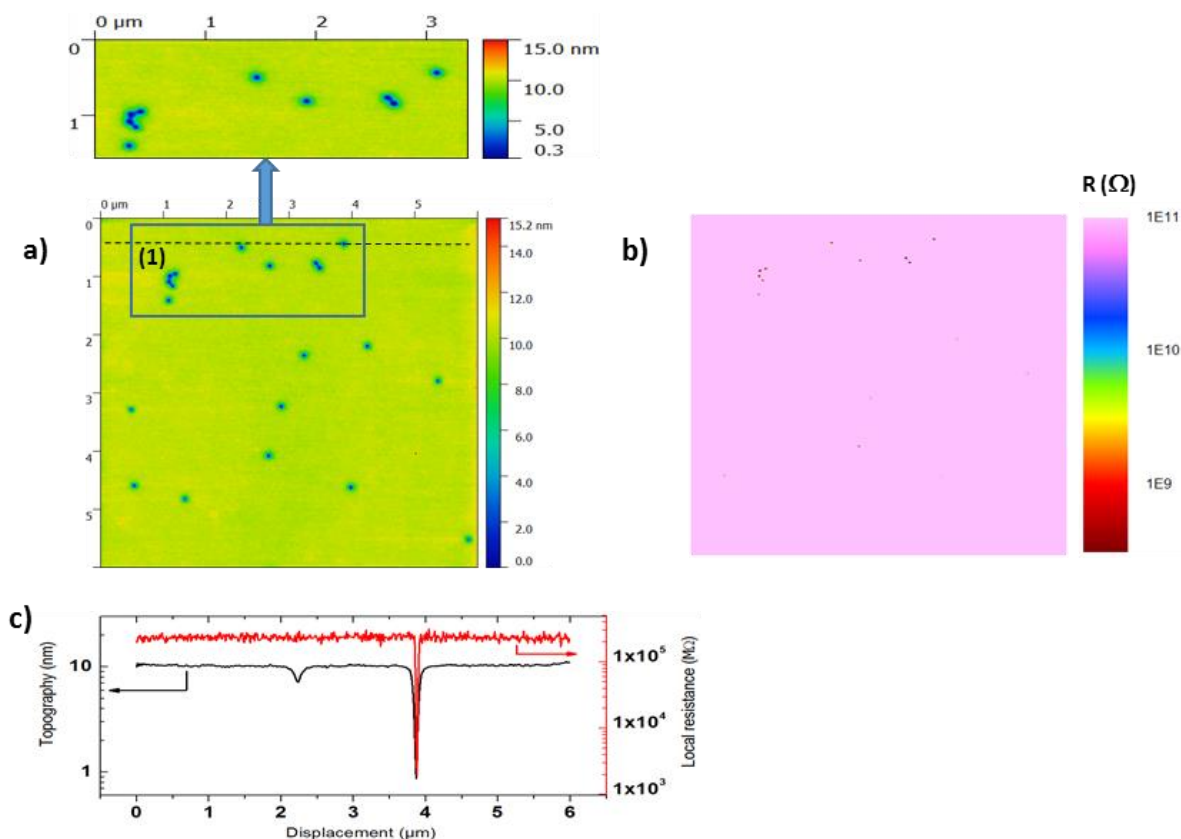


Fig.4.4: (a) Topographic image of silicon sample covered with 10 nm SiO₂ with holes. (Zoom: area that was successfully contacted). (b) Local resistance mapping done with an applied bias of +2 V on same sample and (c) topography and local resistance profile corresponding to line chosen in Fig.4.4.a.

It can be seen from Fig.4.4.b that it was possible to electrically contact some of the holes seen in Fig.4.4.a with a resistance inside the holes around $10^9 \Omega$. This contact is made through the native oxide present inside the holes, and since this native oxide is present everywhere on the substrate, it cannot be blamed for the poor contact elsewhere.

By looking at the zoomed view of the area that was the best contacted (zoom in Fig.4.4.a), it can be seen that the hole edges are not abrupt, but that there is a gradient of oxide thickness inside the holes; the top side diameter of the hole is around 120 nm and the bottom side diameter is around 50 nm (measured from the AFM topography scan). Not being able to contact all the holes is therefore likely due to an incomplete contacting of the bottom of the hole by the AFM tip as the tip radius is around 100 nm. The partial contacting was possible due to the roughness of the tip coating which is in the 10 nm range and knowing that the thickness of the oxide deposited (10 nm) is in the same range of the tip coating roughness.

To enlarge the diameter of the holes, this sample was dipped in 1% HF for 4 seconds. The resulting topography measurements and the local resistance mapping are shown in Fig.4.5.

Characterization of nanoholes

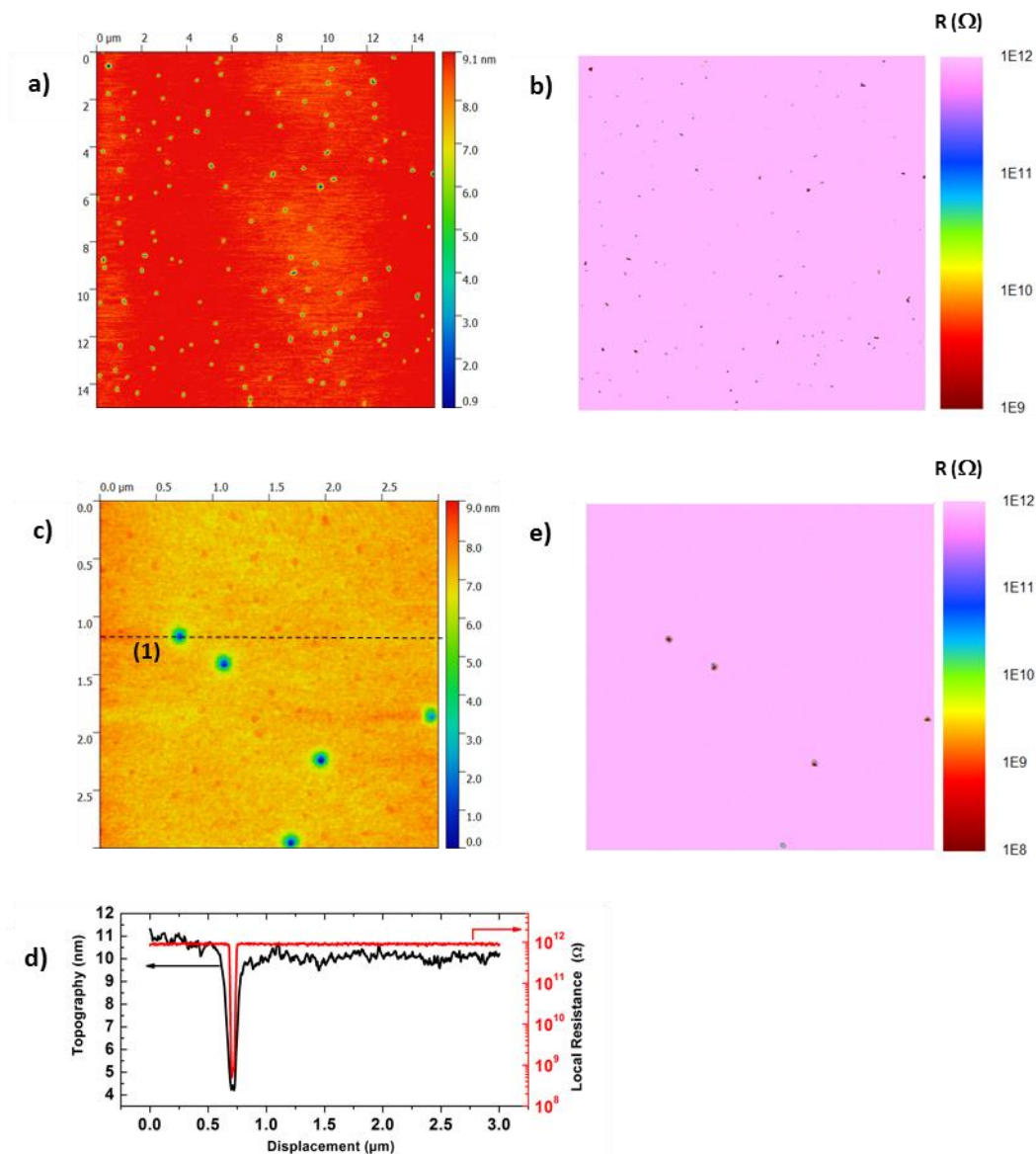


Fig.4.5: Topography images of the silicon sample covered with 10 nm SiO₂ with holes around 100 nm diameter after applying HF (a) scan size of 15 μm×15 μm and (c) scan size of 3 μm×3 μm. (b) and (e) Local resistance mapping done with an applied bias of +8 V, corresponding to measurements (a) and (c) respectively. (d) Topography and local resistance profile along the line (1) from Fig.4.5(c).

The HF treatment was beneficial to electrically evidence almost all of the holes seen in the topography images (Fig.4.5.a and Fig.4.5.c), by applying 8 V, as seen from Fig.4.5.b and Fig.4.5.e. The resistance of the contacted holes is between 10⁸ and 10⁹ Ohms. This can be understood as due to the HF dip, around 3-4 nm of the 10 nm SiO₂ deposited by MD-ECR was etched and the holes become wider; their top side diameters become around 210 nm and the bottom side diameters around 70 nm. This increased hole size makes it possible for the 100 nm radius tip to contact the bottom of the hole and thus make good electrical contact.

Approach A was applied on another Si sample by depositing 330 nm NPs by floating transfer technique instead of spin coating. The monolayer deposition was followed by NP etching by 1 min of O₂ plasma at 1

Characterization of nanoholes

kW, resulting in NP diameters of ~ 200 nm. A 10 nm SiO_2 layer was deposited by MD-ECR room temperature, and followed by NP removal.

The SEM images corresponding to each of the steps are shown in Fig.4.6.

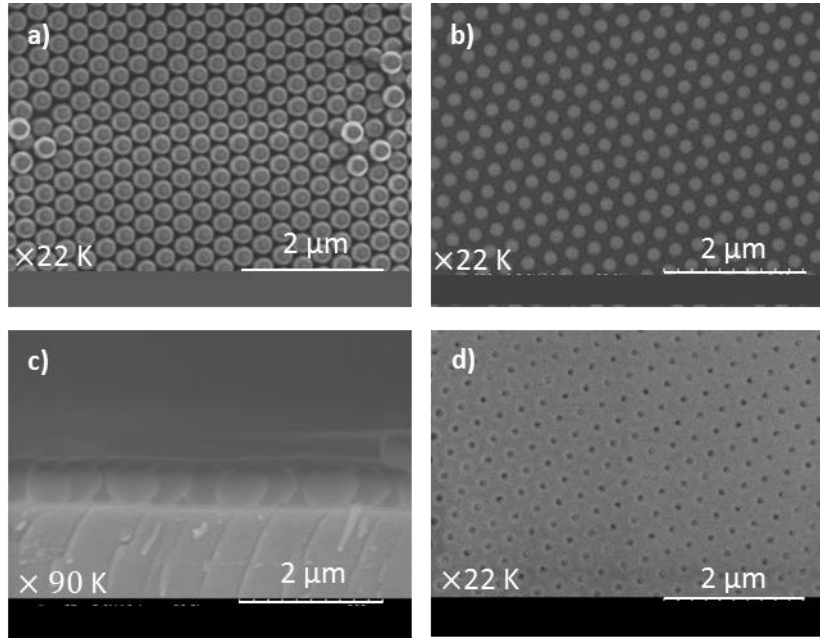


Fig.4.6: (a) SEM top view image of 330 nm diameter NPs on silicon substrate, (b) SEM top view after shrinking NPs of Fig.4.6.a, (c) SEM cross section of etched NPs covered with 10 nm SiO_2 layer, and (d) SEM top view of 10 nm SiO_2 sample with holes.

It can be seen from Fig.4.6.d that holes were indeed formed in the SiO_2 layer. To confirm that electrical contact can be made through these holes and that it will be possible to use this approach to form point contacts to cSi, local resistance mapping was done on this sample by CP-AFM and is shown on Fig.4.7.

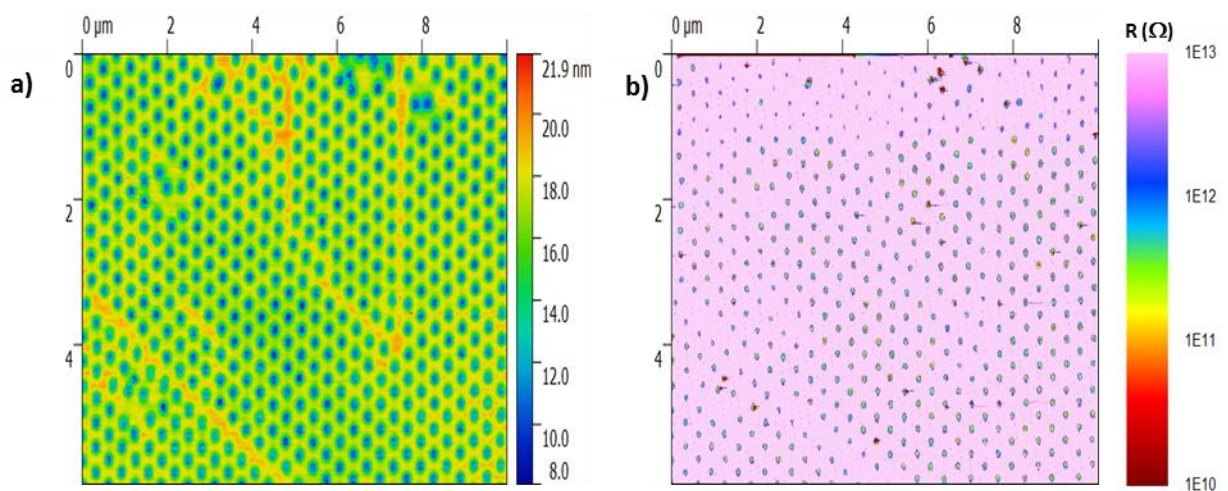


Fig.4.7: (a) Topography image of sample shown on Fig.4.6.d, and (b) Local resistance mapping corresponding to sample shown in Fig.4.7(a).

Characterization of nanoholes

By applying a voltage of + 8V, it was possible to make electrical contact through all the holes. No HF treatment was necessary as the NPs diameter initially used and the holes diameter formed are larger than the previous case. However, the resistance inside the holes measured in this case is between 10^{11} and 10^{12} Ohms, much higher than the previous case (Fig.4.4 and Fig.4.5). This may be due to a thicker oxide in the holes or incomplete removal of the NPs, both due to the O_2 plasma etching, which can lead to softening of the NP on the sample surface and/or oxide growth. This effect could be reduced using an additional toluene and/or HF step on the sample just before CP-AFM.

4.1.1.3 CP-AFM – Holes in films on coated glass substrates

Approach A was then applied on conductive thin-film stacks, namely ITO deposited on an Al layer on glass, which can act as a back reflector for thin film solar cells. NPs with a diameter of 100 nm were spin coated on the 100 nm thick ITO layer, followed by a room temperature deposition of SiO_2 or SiN_x by MD-ECR. The schematic illustration presenting all the steps is shown in Fig.4.8.

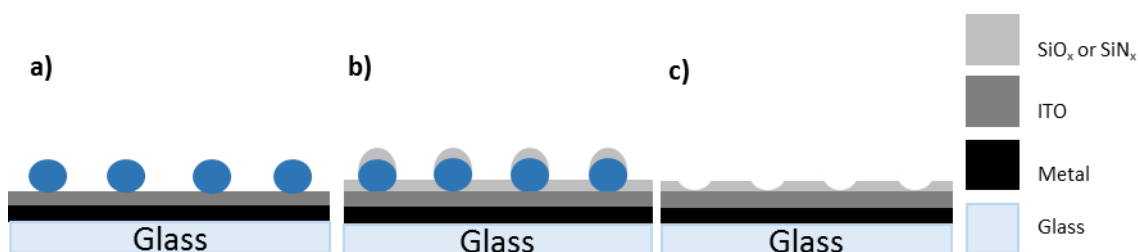


Fig.4.8: Schematic illustration of different steps of approach A applied on conductive-layer coated glass substrate. (a) Deposition of PS NPs, (b) deposition of SiO_2 or SiN_x by MD-ECR high density plasma, and (c) NP removal.

The corresponding SEM images for the first step of the NP deposition are shown in Fig.4.9.

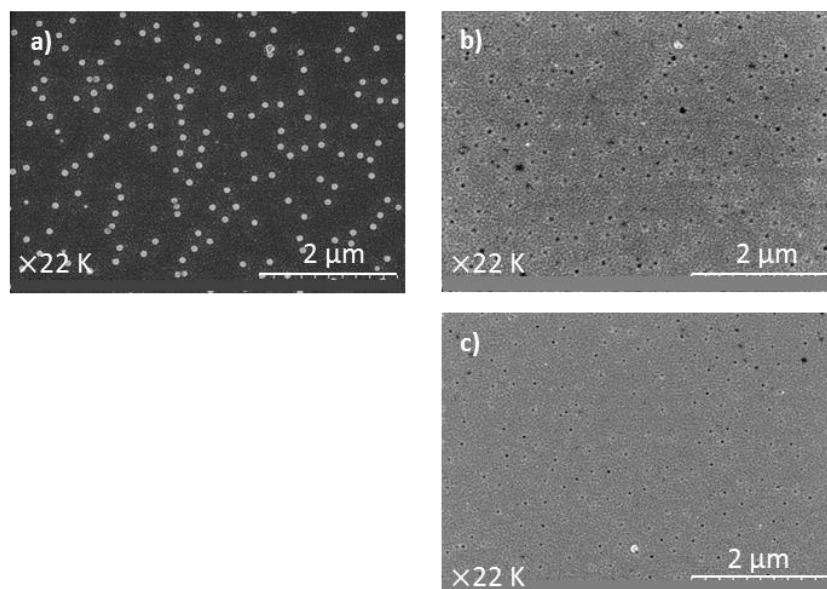


Fig.4.9: SEM images showing (a) NP deposited on ITO/Al, (b) 13 nm SiN_x with nanoholes, after NP removal, and (c) 13 nm SiO_2 with nanoholes, after NP removal.

By comparing Fig.4.9.b and Fig.4.9.c, it can be seen that the hole diameters formed in the SiN_x is 53 ± 10 nm compared to 40 ± 10 nm formed in the SiO_2 layer.

These samples were then characterized using the CP-AFM, by applying a voltage bias of -8V, as shown in Fig.4.10.

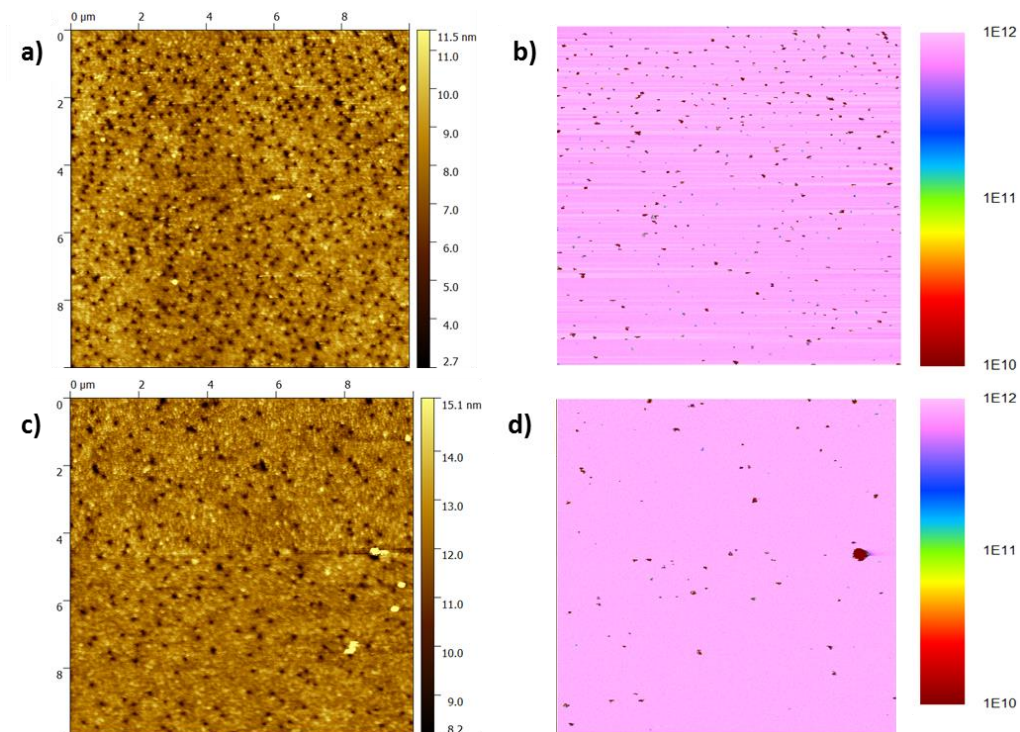


Fig.4.10: (a) Topography image and (b) local resistance mapping of 13 nm SiN_x layer deposited on ITO-metallic stack. (c) Topography image and (d) local resistance mapping of 13 nm SiO_2 deposited on ITO-metallic stack.

It can be seen from Fig.4.10 that it was possible to make electrical contact through the holes formed in the oxide and nitride layers, with resistances between 10^{10} and 10^{11} Ohms measured inside the holes. Note that lower value is saturated on the resistance mapping scale, and may be even lower.

The "electrical" hole map in the SiN_x layer (Fig.4.10.b) is close to its corresponding topography image (Fig.4.10.a), that is to say, contact is made through all the holes. However, a lower fraction of the holes in the SiO_2 layer allow electrical contact (Fig.4.10.c and 4.10.d). This can be attributed to the fact that bigger holes are formed in the SiN_x than in SiO_2 (Fig.4.9.), making tip contact with the opening more probable. The phenomenon of larger holes in SiN_x than SiO_2 was previously noted on Ag-glass stacks in Chapter 3 (Fig.3.50). This is probably related to different deposition physics for the SiN_x and SiO_2 , where there is more surface diffusion during the SiO_2 deposition.

4.2 Forming nanoholes in thick dielectric layers

Using approach A to form nanoholes is not feasible in many situations. Firstly, if the dielectric layer used is thicker than half of the NPs diameter, the removal of the NPs by toluene US bath can become difficult. As well, this approach cannot be used if the dielectric covering the NPs is deposited at a temperature higher than the polystyrene glass transition temperature of 100°C . In this case, the NPs can be deformed or melted

during the dielectric deposition, and either won't act as a rigid mask or will be difficult to remove without leaving residues. Finally, if a highly uniform and conformal dielectric layer is deposited on the NPs, the removal of the NPs will require more complex techniques.

In these cases, it would be better to use another approach, where NPs are deposited on the dielectric layer to be patterned, and then a masking layer is deposited on the NPs.

In this thesis, two masking layers were successfully used to cover the NPs; an aluminum layer and an a-SiC_x:H layer. Therefore, Al will be used as a mask for oxide layer patterning (named Approach B), whereas a-SiC_x:H is used as a mask for patterning an Al₂O₃ layer (Approach C).

4.2.1 Approach B: Using aluminum as a mask

4.2.1.1 ZnO-glass substrates

The first trial to demonstrate Approach B was done with the goal of forming nanoholes in a 50 nm SiN_x layer covering a film of ZnO:Al. First, 500 nm of ZnO:Al was deposited on a Corning Glass substrate at 325 °C. The deposition conditions were 30 sccm Ar flow, deposition time of 15 min, and 250 W RF power. This was followed by the deposition of 50 nm SiN_x by PECVD (in the Nextral ND200 reactor). Then, 100 nm NPs were spin coated on the dielectric layer, and then covered by a 35 nm layer of evaporated aluminum. The NPs are then removed by toluene US bath, leaving an Al layer with nanoholes. The NP removal in this case is easy because of the anisotropic type of the Al deposition, which creates a shading effect when evaporated on the NPs. The steps of this approach are summarized in Fig.4.11.

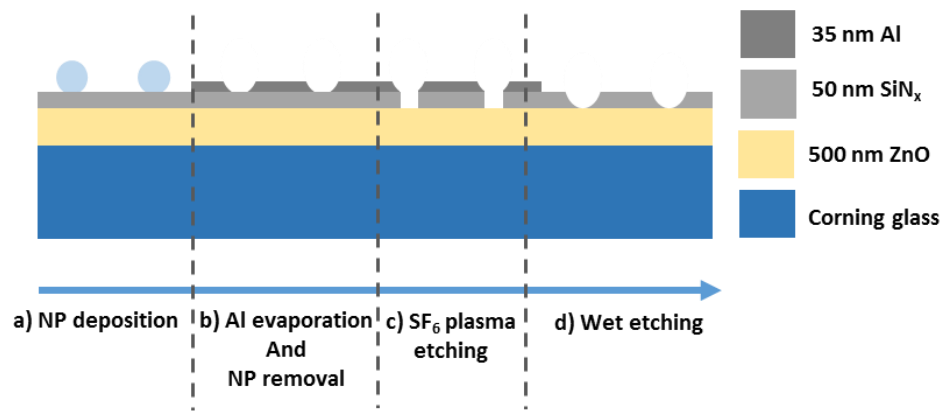


Fig.4.11: Schematic illustration of steps done to form nanoholes in SiN_x layer. (a) NP deposition on dielectric layer, (b) Al evaporation on NPs followed by NP removal, (c) Plasma etching of SiN_x layer by SF₆ through aluminum holes, and (d) Wet etching, by transene, of Al layer.

Nextral NE110 RIE reactor was then used to locally etch the SiN_x through the holes formed in the Al by using 30 sccm of SF₆ at a power of 20 W. Finally, a wet etching by transene was done to remove the Al layer. This solution contains 80 wt% Phosphoric acid, 5% Nitric acid, 5% Acetic acid, and 10% DI.

SEM images corresponding to the first (a) and last (d) step of Fig.4.11 are shown in Fig.4.12.

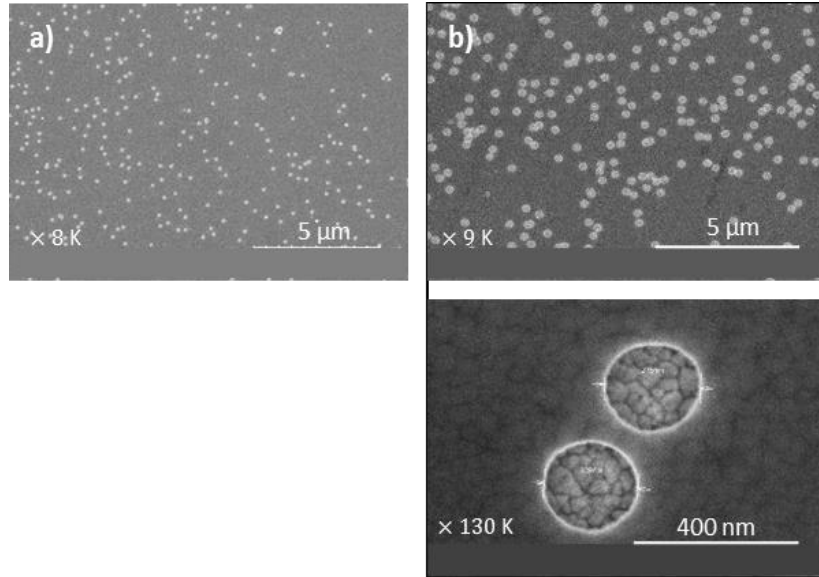


Fig.4.12: SEM images showing (a) 100 nm NPs spin coated on SiN_x , and (b) nanoholes formed in SiN_x layer (with zoom).

It can be seen from Fig.4.12.b that the holes diameter formed in the SiN_x layer is around 230 nm, which is double the initial diameter of the NPs deposited on the dielectric. This is probably due to an undercutting etch of the SiN_x during the SF_6 plasma etching.

Local resistance mapping was also done by CP-AFM on this sample in order to confirm that the holes are completely opened in the SiN_x layer, and good contact is made to the underlying ZnO:Al layer. Applying 1 V was enough to electrically contact the holes. The topology and CP-AFM mapping is presented in Fig.4.13.

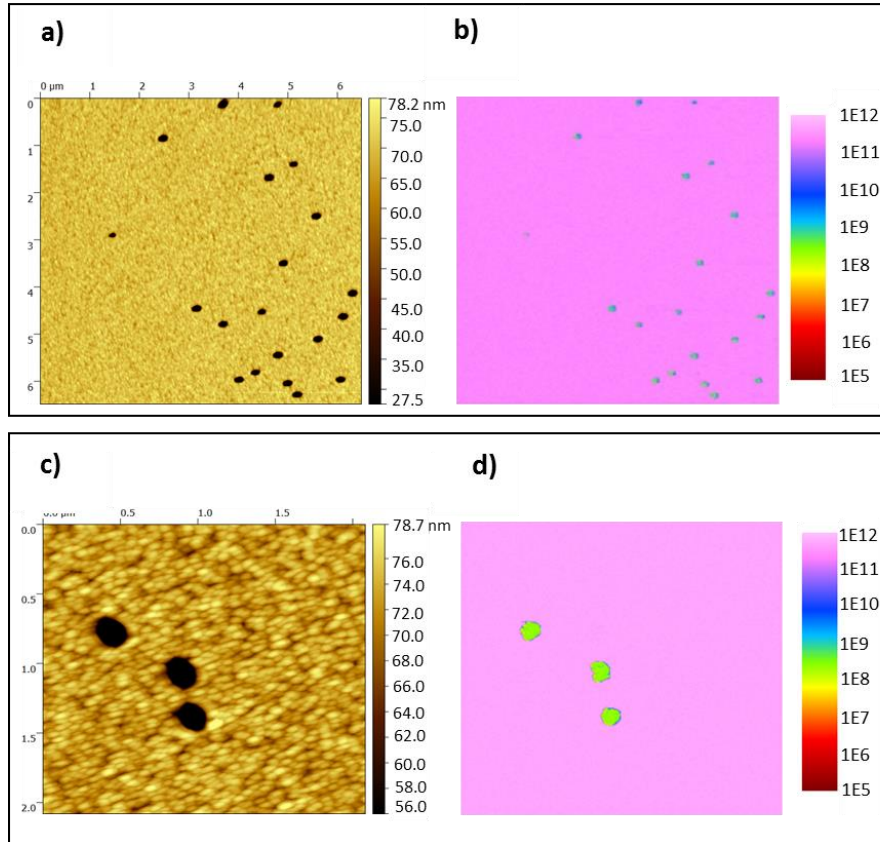


Fig.4.13: (a) Topography (scan of $6\ \mu\text{m} \times 6\ \mu\text{m}$) and (b) local resistance map of sample with nanoholes in SiN_x . (c) Zoomed topography (scan of $2\ \mu\text{m} \times 2\ \mu\text{m}$) and (d) local resistance map of same sample.

It can be seen that the resistance inside the holes is around $10^8\ \Omega$, therefore at least four orders of magnitude lower than the SiN_x layer (saturated at $\sim 10^{12}\ \Omega$) in which the holes are formed. It was easy to contact the holes formed in this case as they are bigger (230 nm) than the holes formed with approach A, allowing the tip to fully contact the ZnO.

4.2.1.2 Silicon substrates

The same approach was used to form nanoholes in a dielectric layer covering a silicon substrate, with an eye towards forming nanoholes in dielectric passivation layers. NPs are first deposited on a dielectric layer, followed by Al evaporation and NP removal. The dielectric is then plasma etched through the holes, and the Al is finally removed using a wet-etching solution. All the steps are presented in Fig.4.14.

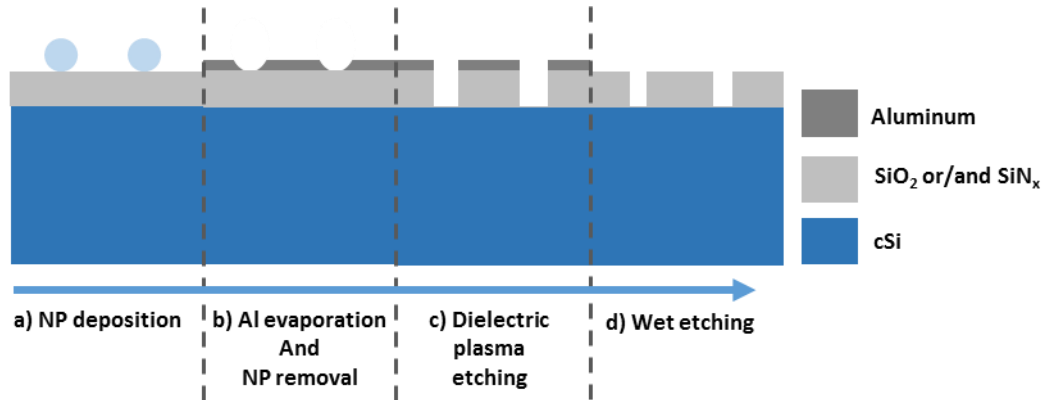


Fig.4.14: Schematic illustration of steps done to form nanoholes in dielectric layer covering silicon. (a) NP deposition on dielectric layer or dielectric stack, (b) Aluminum evaporation on NPs followed by NP removal, (c) Plasma etching of dielectric layer through aluminum holes, and (d) wet etching of aluminum layer.

4.2.1.2.1 SF₆ etching and transene

For these experiments, the dielectric etching through the holes was done using the Oxford Instruments PlasmaLab ICP system, using 30 sccm of SF₆, at 30 mTorr, and 20 W RF power applied to the substrate holder. The ICP coil was either switched on to make the plasma denser, or the system was operated in CCP mode (no ICP power). The Al was removed using a transene solution.

The steps shown in Fig.4.14 were applied on two different structures:

(a) Varying thicknesses of SiO₂ deposited by MD-ECR on the silicon substrate. The deposition of the SiO₂ was done at room temperature using 40 sccm of O₂ and 5 sccm of SiH₄.

(b) A stack of a sub-stoichiometric 30 nm SiO₂ (close to aSi:H because of low O content) passivation layer deposited by PECVD on the silicon substrate, covered with different thicknesses of SiN_x. The SiN_x was deposited by PECVD in the Nextral ND200 reactor using N₂=300 sccm, He=100 sccm, NH₃=54 sccm, and SiH₄=12 sccm at 0.5 Torr and 200 W.

Around 30 nm of Al was evaporated on the NPs, and the NPs were removed by toluene forming an Al layer with holes with diameters around 100 nm (see Fig.3.38.b and c in ch.3).

[Structure (a) - ICP source ON] The first etching trial was done while applying 300 W to the ICP coil. A higher etching rate was expected due to the denser plasma.

Structure (a) was the first used, with the following stack: Al/ 66 nm SiO₂ (MD-ECR)/c- Si. An SEM image acquired after etching through the holes in the Al is shown in Fig.4.15.a, and after Al removal in Fig.4.15.b and c.

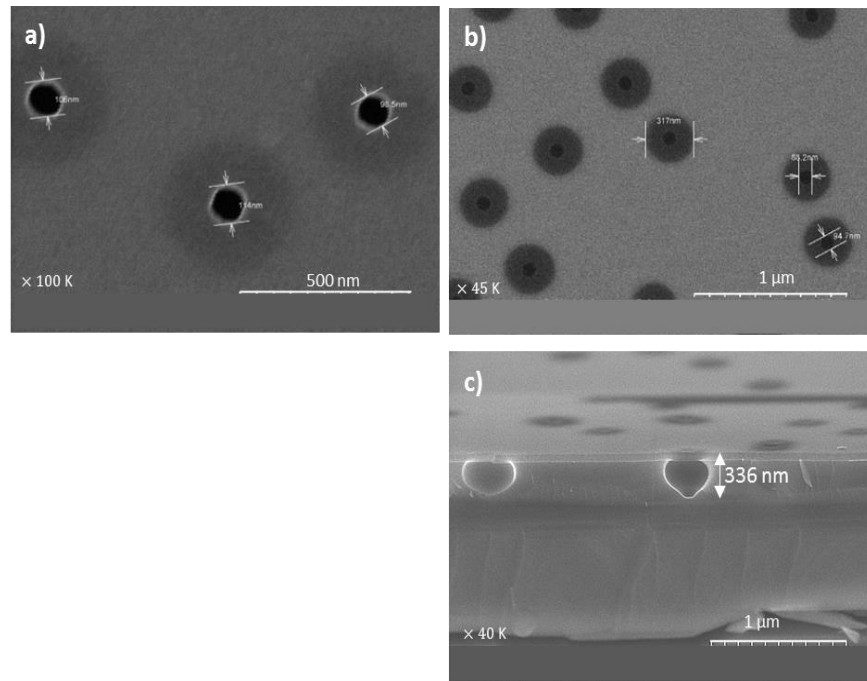


Fig.4.15: (a) SEM top view of Al/66 nm SiO₂/Si sample after plasma etching (step Fig.4.14.c), (b) SEM top view and (c) SEM cross section of same sample after Al removal (step Fig.4.14.d).

Figure 4.15 shows that not only was the SiO₂ etched, but an isotropic etching of the underlying c-Si substrate also occurred; a vertical etching of around 270 nm and an undercutting etch of 100 nm (in each direction) was observed. However, the SiO₂ layer was only etched in the area under the hole. This indicates a higher etching rate for c-Si than for SiO₂ when using SF₆ as etchant. Indeed, a high Si:SiO₂ selectivity has been observed using a SF₆ plasma etching by S. Frederico et al. [214]. S. Avertin has also observed that an increase of the SF₆ flux in a SF₆/BCl₃ and SF₆/O₂ plasma leads to an increase of the selectivity of Si:SiO₂ when SiO₂ is used as a mask [215].

[Structure (a) - ICP source OFF] For the subsequent trial, the ICP source was switched off, leading to a decrease in the plasma density. The SiO₂ (MD-ECR) thickness used for this trial is 30 nm, less than half of the previous case. The corresponding SEM images after Al etching (step Fig.4.14.d) are shown in Fig.4.16.

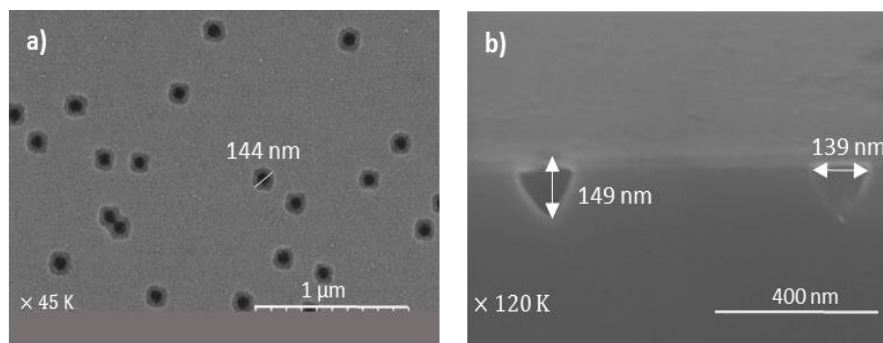


Fig.4.16: SEM (a) top view and (b) cross section of c-Si sample with 30 nm SiO₂ layer after Al mask removal (step Fig.4.14.d).

One can notice the slightly "square" shape of the hole (Fig.4.16.a), presumably related to the wafer orientation. A vertical etching around 119 nm and an undercutting etch of around 40 nm (in each direction)

of the silicon under the SiO₂ layer was observed. Due to the lower plasma density, the c-Si etching was reduced more than in the case presented in Fig.4.15.

[Structure (b) (SiO₂) - ICP source on] The dense SF₆ plasma (with the ICP source on) that was applied on the sample shown in Fig.4.15 was also applied on a sample of Si on which 30 nm of sub-stoichiometric SiO₂ (almost aSi:H like) was deposited. The corresponding SEM images after Al removal (Fig.4.14.d) are shown in Fig.4.17.

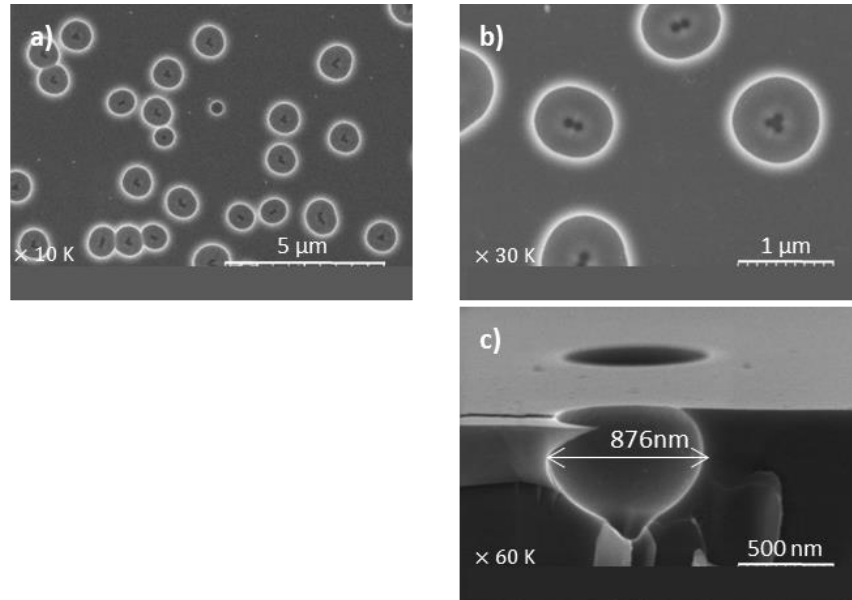


Fig.4.17: (a), (b) SEM top view, and (c) SEM cross section of the sample having 30 nm of a-Si:H-like layer on Si corresponding to the step shown in Fig.4.14.d.

One can note in Fig.4.17.a that in contrast to when stoichiometric SiO₂ was used, the diameter of the hole openings (i.e. in the a-Si:H-like layer) is much greater than the initial diameter of the NPs used (100 nm). Also, the hole openings have different diameters depending on the number of particles forming the NP cluster that was initially covering the SiO₂.

The diameter of the holes is around 490 nm, 780 nm, 940 nm, and 1050 nm for clusters of one, two, three, or four NPs, respectively. A vertical etching of Si around 640 nm was observed from Fig.4.17.c. The shape of the etched silicon seen from the cross section image is similar to what was observed earlier in Fig.4.15.c.

[Structure (b) (SiO₂ + SiN_x) - ICP source on] A 70 nm layer of SiN_x was added on top of the 30 nm SiO₂ layer (aSi:H like) and the same conditions of plasma etching as for Fig.4.17, was applied to the sample. The corresponding SEM images after Al removal (Fig.4.14.d) are shown in Fig.4.18.

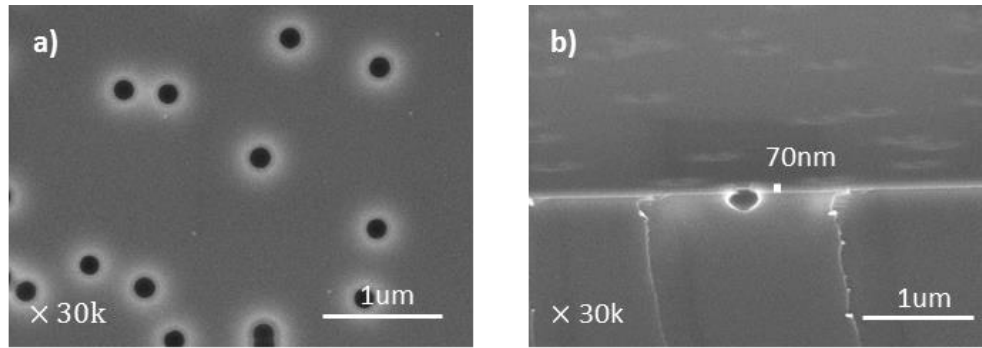


Fig.4.18: (a) SEM top view, and (b) SEM cross section of cSi sample having 30 nm of a-Si:H-like layer covered with 70 nm SiN_x on Si corresponding to the step shown in Fig.4.14.d.

A reduced vertical etching (190 nm) of the silicon was observed, with the possible observation of the SiN_x layer from the SEM cross section image. The hole opening diameter is around 229 nm, which is smaller than half of the smallest diameter observed in Fig.4.17 where no SiN_x layer was used. It seems that the SiN_x layer is more robust, but still does not prevent the etching of the c-Si substrate.

[Structure (b) (SiO₂ + SiN_x) - ICP source off] To reduce the over etching, the plasma density was decreased as in the case of Fig.4.16 by switching the ICP source off. This was applied on a Si sample with 30 nm SiO₂ (a-Si:H like) covered with 20 nm or 40 nm SiN_x. The SEM images after Al etching (Fig.4.14.d) are shown in Fig.4.19.

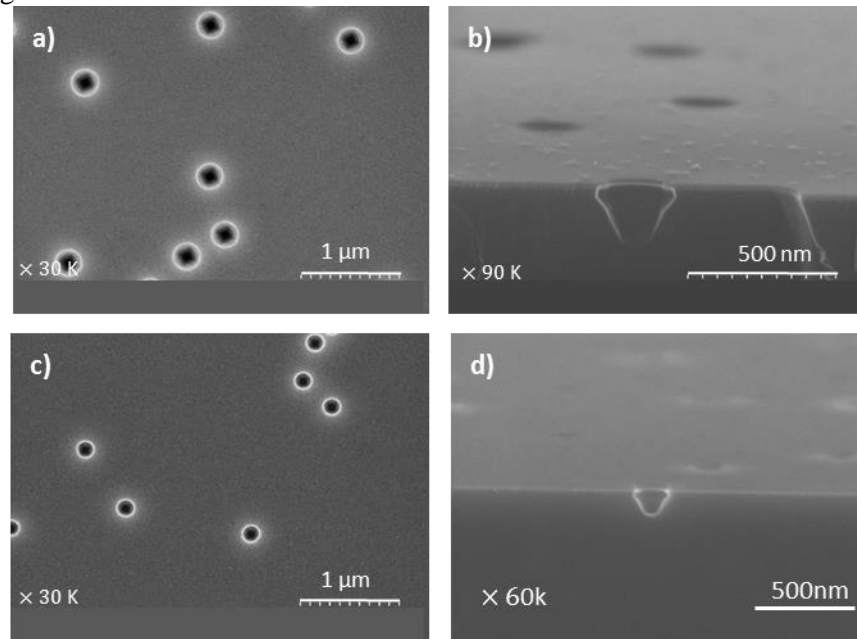


Fig.4.19: SEM images (a) top view, and (b) cross section of following stack: 20 nm SiN_x/30 nm a-Si:H-like layer /c-Si substrate. (c) Top view, and (d) cross section of 40 nm SiN_x/30 nm a-Si:H-like layer /c-Si substrate. All images are after Al removal (step Fig.4.14.d).

One can notice a “square” shape in the holes (Fig.4.19.a, and 19.c) as previously noted in Fig.4.16, when the ICP source was also switched off. For the sample with 20 nm of SiN_x, the hole opening diameter is around 270 nm and a Si vertical over etching of 195 nm is observed (Fig.4.19.a and b). For the sample with

40 nm of SiN_x (Fig.4.19.c and d), the hole opening diameter is around 170 nm with a vertical Si etching of 110 nm.

Of all the samples in this section, it was seen that the smallest Si over etching (110 nm) was obtained for Fig.4.19.d, when the SiO₂ was covered by a 40 nm layer of SiN_x and the plasma density was decreased by switching the ICP source off.

However, for our first trials, the etching of the c-Si substrate should be completely eliminated in order to avoid creating damages on the Si surface, especially considering that our final goal is to form passivated contacts.

4.2.1.2.2 CHF₃ plasma and Orthophosphoric acid etching

The origin of the c-Si substrate etching observed in the previous section is not completely clear – it could be due to the SF₆ plasma etching, or to the transene wet etching solution. With the aim of eliminating this undesired c-Si etching, both of these etching steps were changed. The SF₆ etchant gas was replaced by a mixture of **CHF₃ and argon**, and a mixture of **orthophosphoric acid (H₃PO₄) and isopropanol** will now be used to etch the Al.

The samples using this new process were prepared following a slight variation of the same steps of Fig.4.14. The NPs were deposited onto thermally grown SiO₂ layers (120 nm and 240 nm) using the floating transfer technique (section 3.1.3 of ch.3) and then etched by an O₂ plasma. NPs with diameters of 607 nm and 784 nm were deposited, and their diameters were reduced by O₂ plasma etching to 125±17 nm and 240±13 nm, respectively (see Fig.3.36.c, d, e and f from Chapter 3). This was followed by the evaporation of 30 nm of Al, and then NP removal. Holes with diameters around 200±18 and 255±28 nm were formed in the Al from initial NP diameters of 607 nm and 784 nm, respectively (see Fig. 3.61.d and f of Chapter 3). RIE etching was then done on the samples to locally etch the SiO₂ through the holes. This was done using the Oxford Instruments Plasma technology Plasmalab System 100 ICP etcher in ICFO, the institute of photonic sciences, Spain. It was done using a RF power of 275 W, a pressure of 30 mTorr, 50 sccm of CHF₃ and 50 sccm of Ar (ICP coil OFF).

The plasma etching was done during 2 min and 30 s for the samples with a SiO₂ thickness of 120 nm, and during 4 min and 30 s for the samples with 240 nm of SiO₂. After performing this etching, the Al etching step (Fig.4.14.d) was not done, as the evaporated aluminum had already been removed during the oxide plasma etching, which is unusual. SEM images of these samples were acquired after the plasma etching to further understand the reason for the Al removal. SEM tilted view images of the samples are shown in Fig.4.20.

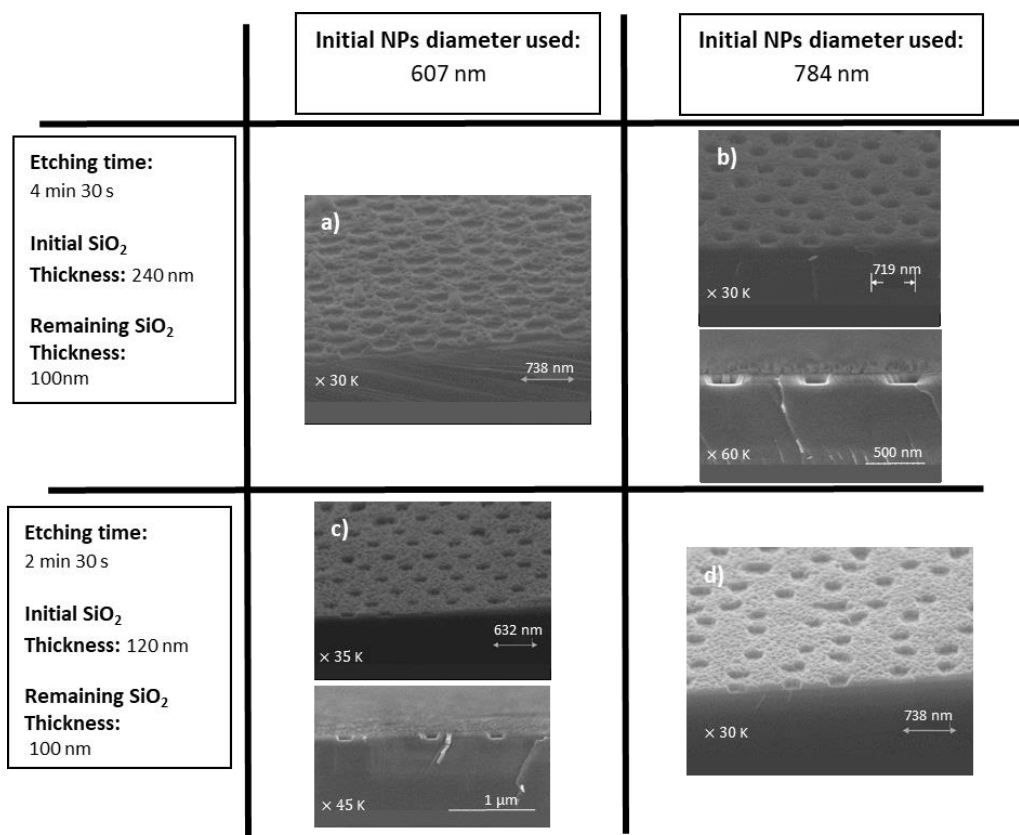


Fig.4.20: SEM tilted view images acquired after plasma etching of Si samples with different initial SiO₂ thicknesses. **240 nm**, with initial NP diameters of (a) 607 nm, and (b) 784 nm, and **120 nm**, with initial NP diameters of (c) 607 nm, and (d) 784 nm.

It can be seen for the samples with an initial SiO₂ thickness of 240 nm, only half (100 nm) remains. In addition, the SiO₂ remaining is rough and no longer uniform. This suggests that the SiO₂ was also etched outside the holes, which might be the reason for the aluminum lift off. For the samples with an initial SiO₂ thickness of 120 nm, the etching is less serious; only 20 nm of the SiO₂ was removed outside the holes. However, at first view, the crystalline silicon substrate does not appear to have been etched by this process at all.

As this undesired etching of the oxide outside the holes was attributed to a lifting off of the aluminum masking layer, the plasma etching time was further reduced. Both etching times (for thicknesses of 120 nm and 240 nm) of SiO₂ were decreased by ~1 min. After doing so, it was confirmed that the aluminum masking layer was still present after plasma etching. A mix of 250 ml of orthophosphoric acid (H₃PO₄) and 100 ml of isopropanol was then heated to around 65 °C to etch the aluminum. SEM images of the resulting samples after Al etching are shown in Fig.4.21.

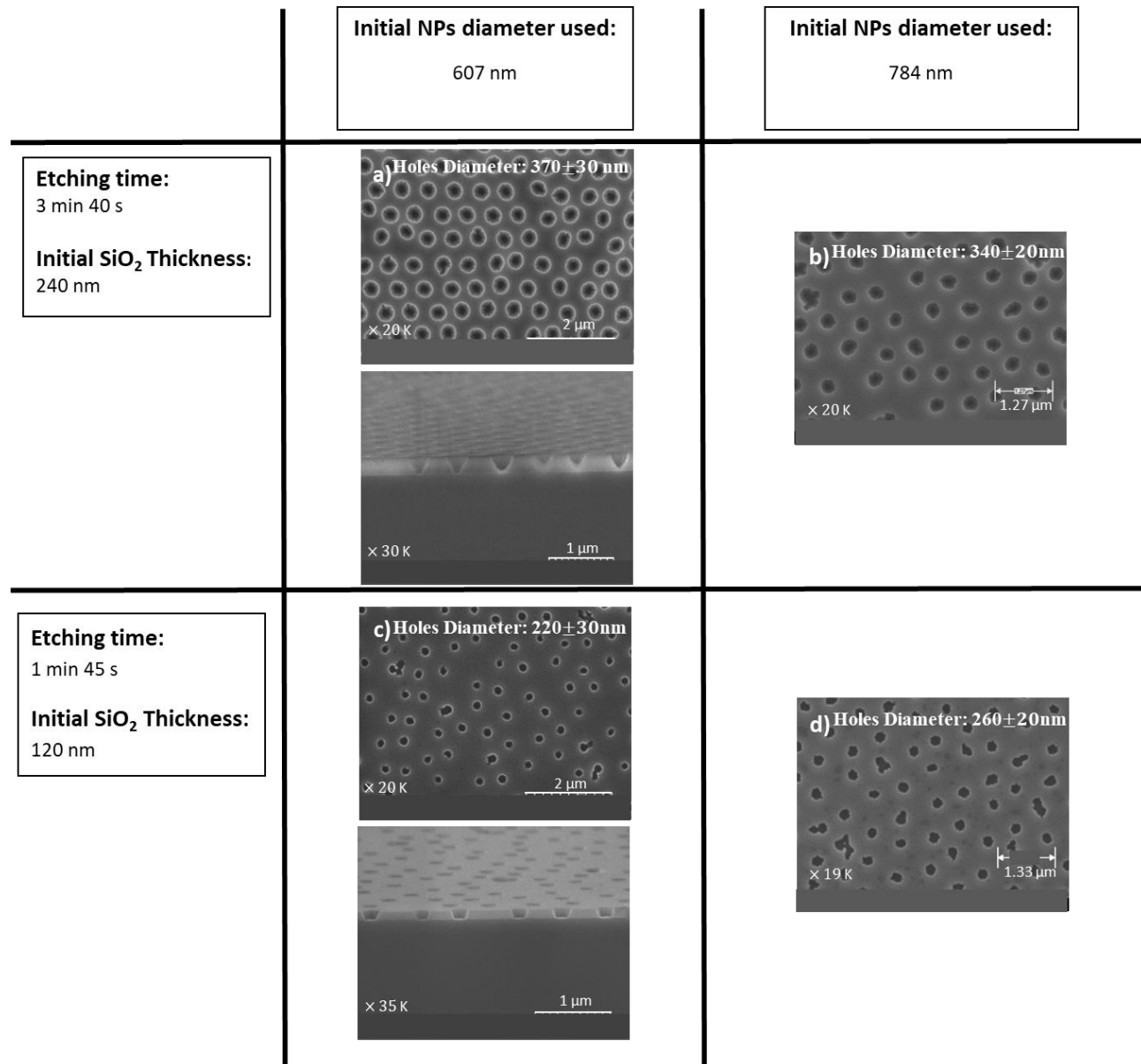


Fig.4.21: SEM top and tilted view images acquired after plasma etching of Si samples with different initial SiO₂ thicknesses. **240 nm**, with initial NP diameters of (a) 607 nm, and (b) 784 nm. **120 nm**, initial NP diameters of (c) 607 nm, and (d) 784 nm.

It is seen that the SiO₂ layer after etching appears less rough than the previous case (Fig.4.20). The holes formed in the oxide are homogeneously created, and the SiO₂ layer is totally removed inside them, with no visible etching of the c-Si substrate. For the samples where 607 nm NPs were used, the hole diameter has increased during etching. For the 120 nm thick oxide, the holes increased from 200 nm in the Al layer to 220 nm in the SiO₂. For the 240 nm thick oxide, the hole diameters increased even more, to 370 nm.

For the samples using larger NP diameters (784 nm), the hole diameters also increased by almost identical amounts. For the 120 nm thick oxide, the hole diameter increased from 255 nm to 260 nm. In the 240 nm thick oxide, the hole diameters further increased to 340 nm. This hole enlargement is attributed to SiO₂ undercut etching during the plasma treatment, and depends mostly on the oxide thickness.

Characterization of nanoholes

To quantify any etching of the c-Si substrate through the holes, an AFM measurement was done on the sample after completely etching away the oxide. These measurements have shown an etching of only 5 nm of the c-Si inside the holes. This can be considered negligible, compared to the over etching of more than 100 nm observed when SF₆ was used in the plasma etching. This result is due to the higher SiO₂ to Si etch selectivity with the (CHF₃, Ar) compared to the previous case etched with SF₆. This favorable selectivity was reported by G.S.Oehrlein et al., and attributed to the presence of a fluorocarbon film (5.5 nm) on the Si surface during the steady-state etching which decreases the Si etch rate [216].

It should also be noted that the oxide used with the (CHF₃, Ar) plasma etching is a thermally grown oxide, whereas that used with the SF₆ etching is a PECVD deposited oxide. The better quality of the thermally grown oxide could be a factor in reducing the hole opening expansion when (CHF₃, Ar) was used for the oxide etching. However, it **cannot have played a significant role** in reducing the c-Si etching.

Although two different Al etchants were used after SF₆ and (CHF₃, Ar) plasma etching, there is **no direct evidence** either way if the Al transene etchant used after the SF₆ plasma etching is contributing to the Si etching. However, it is confirmed that the orthophosphoric acid solution etches only the Al, and so is adopted as the preferred choice.

4.2.1.3 Summary-Approach B

We have herein shown that by using the (CHF₃, Ar) plasma etching chemistry, ~200 nm holes can be formed in a 120 nm thick thermally grown oxide, wherein the diameter of the holes formed in the oxide layer is close to those formed in the Al mask layer. Using a 240 nm thick SiO₂ layer, the hole sizes increased due to undercut etching. However, very little impact on the underlying Si surface was observed during this process. As well, the use of a monolayer of NPs followed by O₂ plasma etching provides the opportunity to obtain a wide range of hole pitch and size, where the initial NP diameter controls the pitch of the patterned formed, and the diameter after etching, the hole size.

4.2.2 Approach C: Using a-SiC_x:H as a mask

The aim of the work in this section is to try to form holes in a passivation layer by wet etching instead of plasma etching. To do so, a 30 nm thick a-SiC_x:H layer is used as a mask for the wet etching.

An advantage of this approach is that it doesn't require one to remove the mask as a last step, because the a-SiC_x:H layer shouldn't affect the performance of the final device (in contrast to the Al masking layer that may diffuse into the Si when the sample is heated). In addition, this approach could be applied on samples where the dielectric to be patterned can't be used with an Al mask, such as in the case of Al₂O₃, where the Al₂O₃ etchant will also etch the Al.

In Approach C, NPs are first deposited on the dielectric, followed by a-SiC_x:H deposition by PECVD, and NP removal. This is followed by wet etching of the dielectric through the a-SiC_x:H holes. All the steps of this approach (C) are summarized in Fig.4.22.

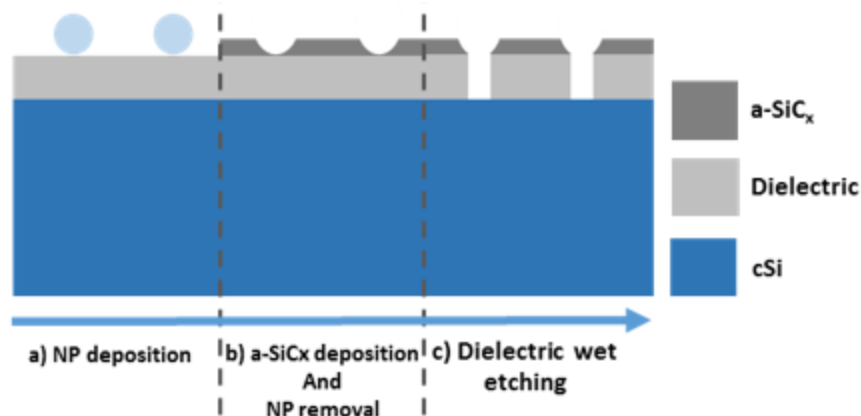


Fig.4.22: Schematic illustration of steps done to form nanoholes in dielectric layer covering silicon. (a) NP deposition on dielectric layer, (b) a-SiC_x:H deposition followed by NP removal, (c) Dielectric wet etching through a-SiC_x:H holes.

4.2.2.1 HF as wet etchant

Before beginning, it was checked that the films of a-SiC_x:H deposited on Si are resistant to HF and buffered oxide etch (BOE) solution (a mixture of ammonium fluoride and HF). This latter solution is used to etch oxides, providing a more stable etch rate compared to HF alone.

Approach C was first applied on a sample having 240 nm of thermally grown oxide on Si covered with a-SiC_x:H with holes formed by NPs and the BOE was used to etch the oxide through the holes. However, this trial wasn't successful as the a-SiC_x:H didn't resist the etching (See appendix). Approach C was therefore instead used to form holes in an Al₂O₃ passivation layer deposited by ALD.

The first experiment used a Si sample covered with 50 nm of Al₂O₃, and then 30nm of a-SiC_x:H, in which the holes have been formed. HF was used as an etchant for the Al₂O₃ through the holes. However, after only 1 min of immersing the sample in 1 % HF, the a-SiC_x:H mask could barely be seen by eye. The Al₂O₃ was almost totally removed after 4 min of HF, the time usually needed to etch a 50 nm thick layer of Al₂O₃. This test shows that the HF is an aggressive etchant for the Al₂O₃ and should be replaced by a softer etchant.

4.2.2.2 RCA "Soft" as wet etchant

A less aggressive, "softer" etchant was therefore used, based on the well-known RCA1 cleaning, a mixture of NH₄OH, H₂O₂ and H₂O (1:1:8) [217]. The etching rate for Al₂O₃ of the diluted RCA1 based solution increases with the temperature; it is around 3 nm/min at a temperature of 45 °C, and 10 nm/min at a temperature around 60 °C [218]. It was again verified that the a-SiC_x:H can resist the RCA soft etching done at 50 °C when being used as a mask on the Al₂O₃.

When performing another test on a c-Si sample covered with 50 nm Al₂O₃, it was noticed that the layer was completely etched, but the sample remain hydrophilic. This is probably due to the presence of a native oxide layer underneath the Al₂O₃ deposition. In fact, prior to Al₂O₃ growth the c-Si samples are cleaned with RCA1. Silicon oxide etching by 1% HF for 1 min is then performed to remove the oxide that was grown during the RCA1 cleaning. This is followed by RCA2 cleaning where ~15 Å of oxide is grown. This

oxide is kept on the Si surface prior to Al_2O_3 deposition as this film leads to a better interface than a H-terminated surface for its electronic passivation [116].

In order to completely remove this native oxide remaining in the holes after our RCA "soft etch", a final ~5 second dip in the BOE was done. After doing all these steps (RCA soft etching on a sample stack of a-SiC_x:H mask/ Al_2O_3 /c-Si, followed by BOE dip), it was noted that this last oxide etching step also removed the a-SiC_x:H masking layer. Thus, the final oxide etching step has dual function; both to etch the SiO_2 left underneath the Al_2O_3 layer, and to remove the a-SiC_x:H mask layer.

This approach was applied to Al_2O_3 covered c-Si samples, on which 607 nm and 784 nm NPs were deposited (floating-transfer technique and O_2 plasma etch). The samples were covered with around 30 nm a-SiC_x:H and then NPs were removed. The corresponding SEM images for the cases before and after NP removal as well as the diameters of the etched NPs and the holes formed in the a-SiC_x:H are shown in Fig.4.23.

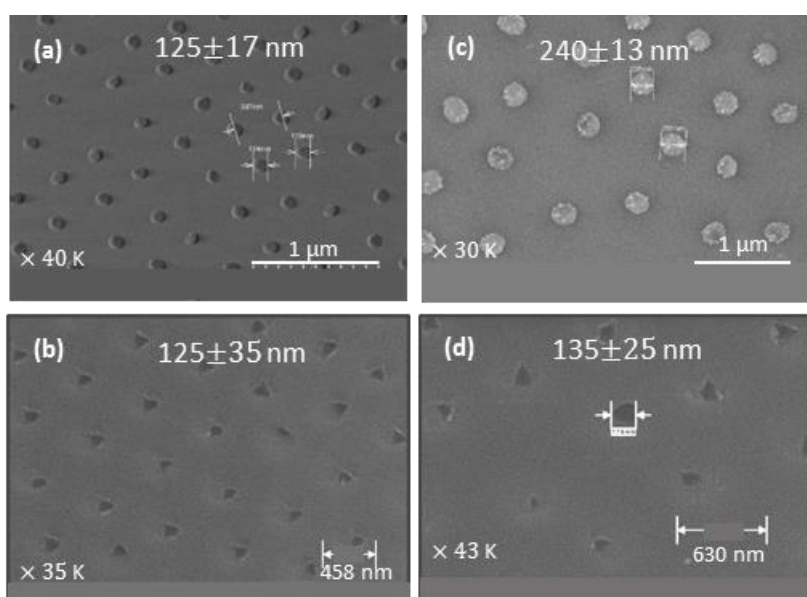


Fig.4.23: SEM images of (a) 607 nm NPs after etching, (b) after being covered with a-SiC_x:H and removed. (c) 784 nm NPs after etching, (d) after being covered with a-SiC_x:H and removed.

The density of the NPs on the samples of Fig.4.23.a and b are around $7.4 \text{ NPs}/\mu\text{m}^2$ and $2.3 \text{ NPs}/\mu\text{m}^2$, respectively.

After opening the holes in the a-SiC_x:H, a variety of different wet etching conditions for the underlying Al_2O_3 film have been explored. All the etching solutions are based on RCA1 soft etching, and the ramp up time (3.5 minutes for RCA1-3 and RCA1-5 and 9 minutes for the rest) and the final temperature were changed. The total etching time for all samples was 20 minutes, except for RCA1-7 with 23 minutes and RCA1-8 with 30 minutes. All the trials are summarized in table.4.1 showing the different temperatures reached by each RCA1 trial after ramp up and the total time of the soft RCA including ramp up time. These trials were done on sample having an initial spheres diameter of 784 nm for the RCA1-3, RCA1-5 and RCA1-6, and an initial spheres diameter of 607 nm for the RCA1-7 and RCA1-8.

| | Initial sphere diameter used to form holes (nm) | Ramp up time (min) | Final Temperature (°C) | Total time (including ramp up) (min) |
|---------------|---|--------------------|------------------------|--------------------------------------|
| RCA1-3 | 784 | 3.5 | 47 | 20 |
| RCA1-5 | 784 | 3.5 | [46-47] | 20 |
| RCA1-6 | 784 | 9 | [55-58] | 20 |
| RCA1-7 | 607 | 9 | [46-48] | 23 |
| RCA1-8 | 607 | 9 | [48-50] | 30 |

Table 4.1: Summary of RCA soft conditions used including ramp up time, final temperature reached after ramp up, and total time of the RCA soft including ramp up time.

The minimum total time was at least 20 min as the etching rate of Al_2O_3 by RCA soft is around 3 nm/min at a temperature of 45 °C [218]. However, this etching rate was calculated in the following reference [218], on samples of Al_2O_3 covered Si samples with no a-SiC_x:H having holes. The etching rate through the holes may be different as the solution may not get freely in contact with the Al_2O_3 through the tiny holes formed in the a-SiC_x:H.

The resulting SEM images from these different trial conditions are shown in Fig.4.24 and 4.25.

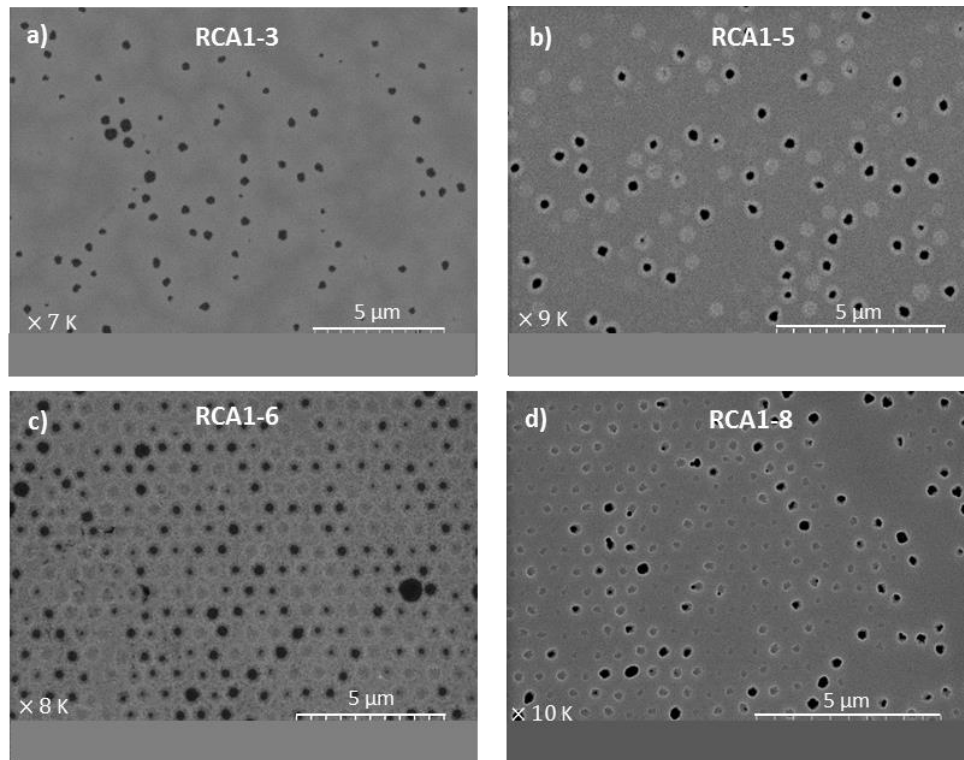


Fig.4.24: SEM top view images of (a) RCA1-3, (b) RCA1-5, (c) RCA1-6 and (d) RCA1-8.

Characterization of nanoholes

It can be seen from these figures that only some of the holes are completely opened and some others are not. The most complete openings are for the highest temperature sample (RCA 1-6). As for the RCA1-7 trial, examination of the surface shows areas where the Al_2O_3 is completely etched through, and others where only partially etching occurred. Fig.4.25 shows examples of these two different zones.

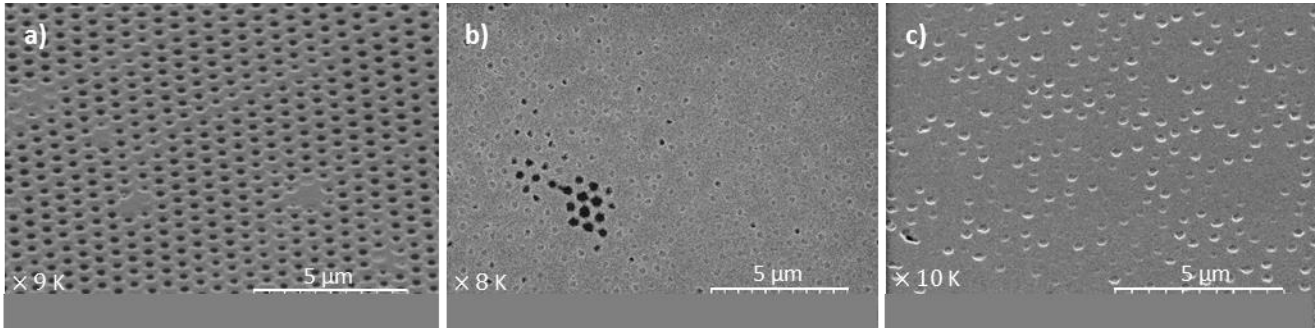


Fig.4.25: (a) SEM image where holes are completely formed in Al_2O_3 film and (b) and (c) SEM images taken in different part of the sample showing nanoholes partially formed.

Analyzing the surface as seen through SEM images, the percentage of opened holes is calculated for each of the RCA1 conditions. The results are shown in Fig.4.26.a, plotted as a function of maximum temperature, as well as the vertical and horizontal errors. Additionally, the size of the opened holes are plotted in Fig.4.26.b.

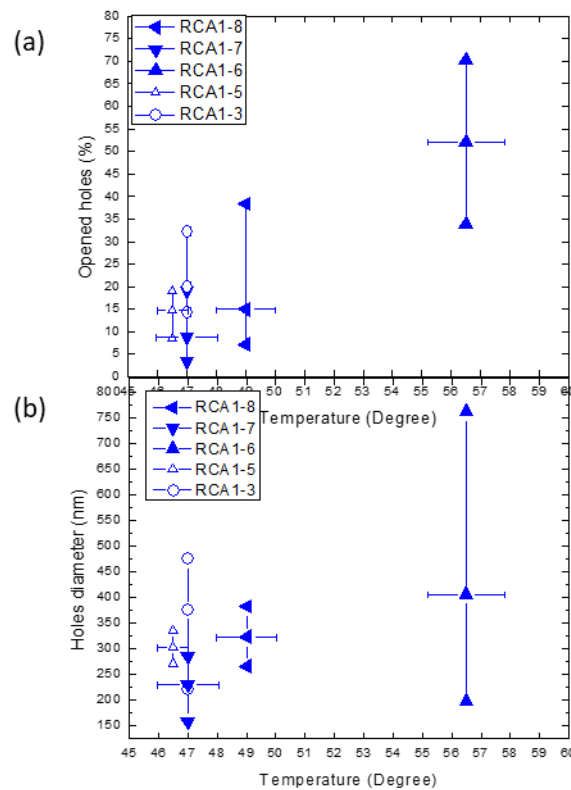


Fig.4.26: (a) Opened holes percentage for all RCA1 trials and (b) opened holes diameter as function of temperature used.

Characterization of nanoholes

It is seen from Fig.4.26.a that by keeping the temperature lower than 50 °C, the opening percentage remains lower than 38 %, independent of all other parameters. However, by increasing the temperature to around (55-58 °C) the open hole percentage achieves values between 34 % and 70 %. Higher temperatures also lead to larger holes with more dispersion in their sizes.

Finally, AFM topography measurement is done on the sample etched by RCA1-7 and it is shown in fig4.27.

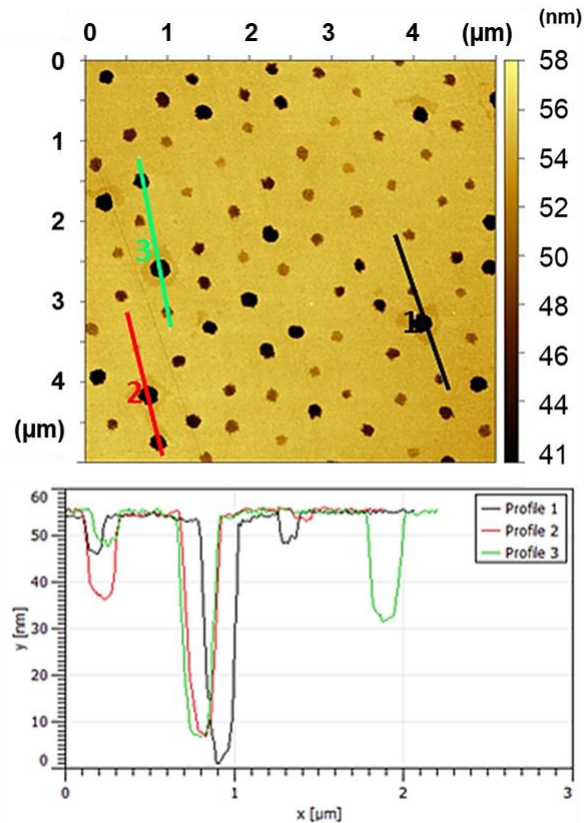


Fig.4.27: AFM topography images corresponding to Fig.4.25, showing a part of the sample after a-SiC_x:H etch.

It is seen from Fig.4.27 that the holes are not homogeneously opened in the Al₂O₃. The deepest holes observed are between 40-50 nm of depth. This is consistent with the Al₂O₃ thickness measured on this sample (after a-SiC_x:H etching) through ellipsometry (48 nm).

In conclusion, although good candidates for the masking layer and the etching chemistry were identified, further research is needed to refine the technique to improve the yield of hole opening in the Al₂O₃ film.

4.3 a-Si:H test PV devices

In this chapter, three approaches used to form holes in different dielectrics have so far been presented. To form holes in thin dielectric layers, approach A is used by covering the NPs by the dielectric itself as the masking layer followed by NP removal. On the other hand, to form holes in thick dielectric layers, approach B and C are used by using aluminum and a-SiC_x:H as the masking layers, respectively.

In this part of the chapter, NIP a-Si:H devices are used as a testing solar cell with point contacts to make sure that the holes formed in the dielectric are electrically contacting. a-Si:H was chosen to be used as the

Characterization of nanoholes

testing cell as it is easy to fabricate and is not as sensitive to critical cleaning and preparation steps (compared to μcSi or c-Si solar cells).

The method used in this chapter can be as well considered as a low-cost technique to form nano-contacts on thin-film silicon solar cells. This is because the distance between the contacts is very small (a few hundred nanometers) for low-diffusion length technologies such as thin-film silicon and would be very expensive if done with traditional lithographic techniques.

In this work, point contacts are formed for a-Si:H devices starting by the back-reflector layer, which consist of a metallic layer covered by an ITO layer and by a dielectric layer with holes.

Spin coating was used as the method of NP deposition and approach A (explained earlier in this chapter) was used to form the holes in the dielectric layers. The dielectric layers used are SiO_2 and SiN_x deposited at room-temperature by MDECR PECVD. After removing the NPs, the samples are characterized by using SEM, and CP-AFM.

NIP a-Si:H Stacks are then deposited on these structures using RF-PECVD, their electrical characteristics are compared to the same cells done without the dielectric layer, and to a structure with a dielectric layer but without any nanoholes.

4.3.1 PIN Structure

The first trial of forming point contacts on a-Si:H consisted of applying approach A on the PIN stack itself. This method starts by first depositing the NPs on the a-Si:H layer followed by covering the NPs with the room temperature deposited dielectrics by MD-ECR, followed by removing them and then evaporating the metal. These steps are shown in Fig.4.28.

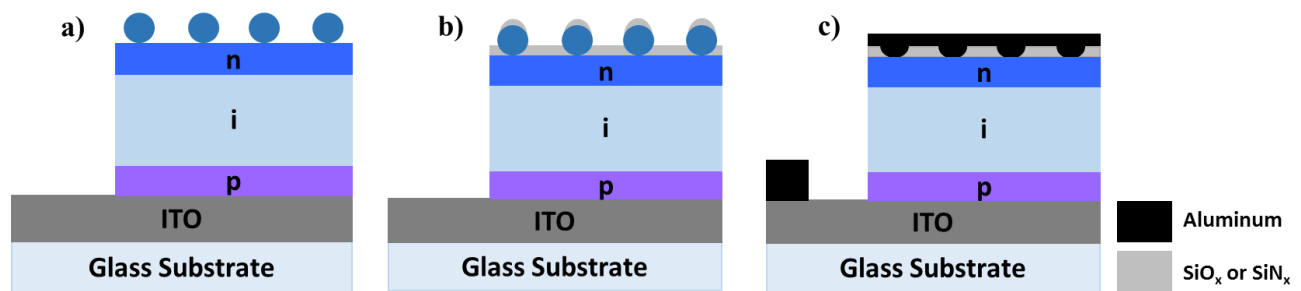


Fig.4.28: Schematic illustration of first trial used to form point contacts in aSi:H devices.

The first step of spin coating 100 nm NPs on the PIN aSi:H stack was done, and the SEM image is shown in Fig.4.29.

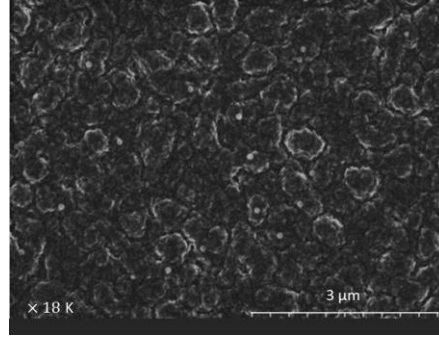


Fig.4.29: SEM image of 100 nm spin coated NPs on a PIN aSi:H stack.

It is seen that the NPs can be barely seen in Fig.4.29 because of the high relative roughness of the PIN surface, whereas $0.52 \text{ NPs}/\mu\text{m}^2$ was previously measured in chapter 3 as the NP coverage on such stacks. Such a vanishingly small coverage was not useful for these trials, and as the roughness of the surface may be a contributing factor, the inverted architecture was instead chosen.

4.3.2 NIP structure

The second trial consisted of depositing the NPs on the back reflector instead of directly on the PIN stack. The device is thus formed in the opposite order to the one seen in Fig.4.28. This will also avoid depositing the polystyrene NPs directly on the n-layer, which can make the process cleaner as the organic particles are not in direct contact with the sensitive area of the solar cell.

Approach A was therefore applied to stacks of ITO/Al/Corning glass, which can act as a back reflector for thin film solar cells. NPs with diameters of 100 nm were spin coated onto a 100 nm thick ITO layer, followed by a room temperature deposition of SiO_2 or SiN_x by MD-ECR. The SEM images corresponding to the step after NP removal were shown earlier in this chapter in Fig.4.9.

The NP density on the Al-ITO is around $5.5 \text{ NPs}/\mu\text{m}^2$, much higher than when deposited on the PIN stack (Fig.4.29). The average distance between the spin coated NPs is around 350 nm (between NP centers) calculated using the following equation:

$$S_{\text{avg}} = \frac{1}{n} \sum_{i=1}^n \frac{(d_{i1} + d_{i2} + d_{i3} + d_{i4})}{4} \quad (4.1)$$

Where n is the total number of NPs and d_{i1} , d_{i2} , d_{i3} , and d_{i4} are the distances between a PS and its four nearest neighbors [77]. The minimal distance between the NPs is 265 nm. CP-AFM measurements for these samples have already been presented in this Chapter (Fig.4.10). These results confirmed that it is possible to make electrical contact through the holes formed in the oxide and nitride

An NIP stack was then deposited using the Nextral PECVD reactor (ND200) at 175°C on the structure of Al-ITO covered with the SiN_x shown in Fig.4.10.a and 10.b. The stack consists of 20 nm n-aSi:H ($\text{SiH}_4=50$ sccm, 2% $\text{PH}_3/\text{H}_2=10$ sccm, 120 mTorr, RF=10 W), 180 nm i-aSi:H ($\text{SiH}_4=50$ sccm, 120 mTorr, RF=6 W) and 10 nm p-aSiC ($\text{SiH}_4=10$ sccm, 2% $\text{TMB}/\text{H}_2=4$ sccm, $\text{CH}_4=5$ sccm, Ar=100 sccm, 300 mTorr, RF=2 W). The schematic illustration of the cell formed is shown in Fig.4.30. ITO was then deposited on the p layer through a mask, forming circular solar cells with diameters of 2 mm and 4 mm.

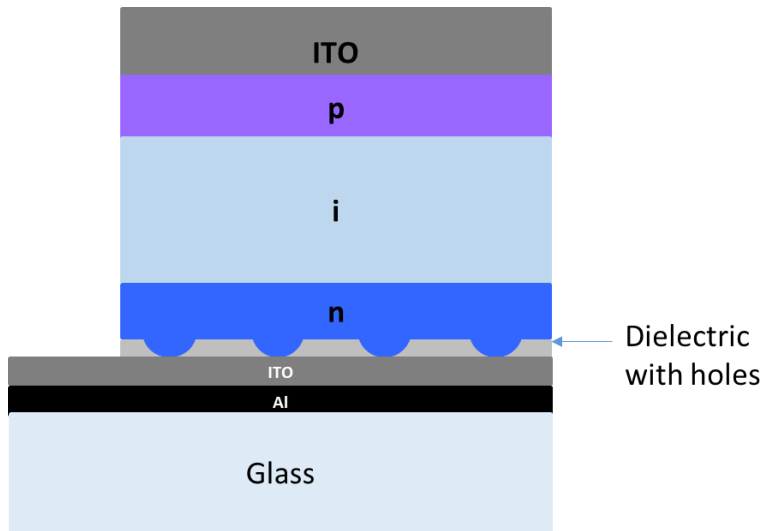


Fig.4.30: Schematic illustration of the a-Si:H cell formed with point contacts.

4.3.3 Solar cell Characterization

The solar cells with point contacts are compared to similar cells fabricated without the dielectric layer, and to a structure with a dielectric layer but without any nanoholes, to prove that the effect of the nanosized local point contacts is different than that of any pinholes present in the dielectric.

The dark J-V curves for three such sample cells are presented in Fig.4.31.

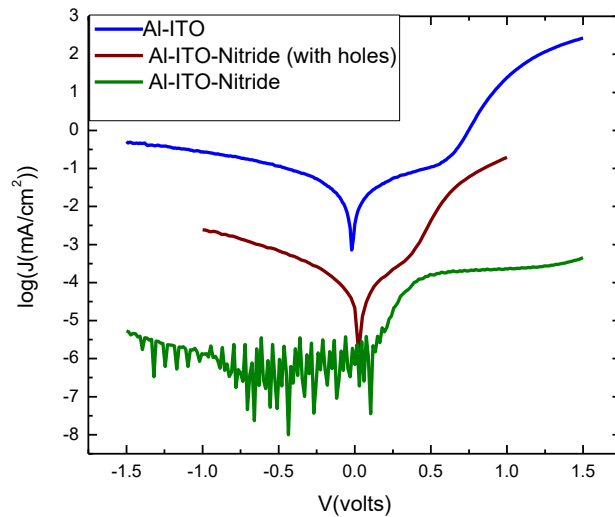


Fig.4.31: Comparison of logarithmic dark J-V of three cells having as a back reflector Al-ITO (blue), Al-ITO-covered with 13 nm of nitride having holes (wine) and Al-ITO- covered with a full 13 nm layer of nitride (green).

Firstly, the Al-ITO-Nitride sample (with no holes) shows only a very tiny current. However, the dark J-V curves of the device with point contacts and the fully contacted device both show diode shapes (with clear

evidence of R_p and R_s). A smaller (worse) R_p is observed for the fully contacted device compared to the one with nanoholes. R_p is due to ohmic shunts through the diode. Shunts can be formed due to pinholes or to dust particles sitting on the underlying layer before and during plasma deposition of the thin-film silicon layer. These shunts can result in actual short circuits and, thus, completely disable the whole solar cell; more frequently they simply lead to a very low value of R_p . Some of these shunts may have been blocked by the dielectric (with holes) used for the point contacted devices. This explains the higher R_p obtained for the locally contacted devices. A schematic illustration representing the local shunts formed for the case of fully contacted and locally contacted devices is shown in Fig.4.32.

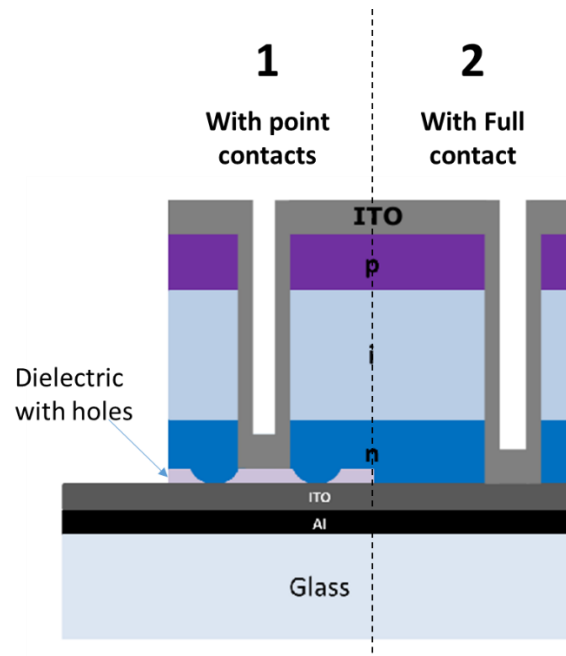


Fig.4.32: Schematic illustration representing local shunt occurring for point contacted device (on the left half) and for fully contacted device (on the right half).

It can be seen from Fig.4.32 that a local shunt can more easily occur for the fully contacted device because of a local short-circuit between the front and back side contact. However, this short circuit can be blocked by the dielectric covering the back contact for the locally contacted device.

The second observable point from the dark J-V curves is that the point-contacted cells display a higher value of R_s . This will be examined in more detail later.

J_0 was extracted from the dark J-V curves (Fig.4.31). 1.34×10^{-5} mA/cm² and 1.24×10^{-6} mA/cm² was obtained for Al-ITO and Al-ITO-nitride with holes, respectively. As J_0 is smaller for the case with point contacts, one could expect an improvement in the cell V_{oc} . An improvement in V_{oc} has already been reported by B.Vermang, et al. for point contacted thin-film CIGS solar cells, compared with unpassivated reference cells [82][81]. To check if it's the case here, the dark and light (at AM 1.5) J-V of the three cells are plotted in Fig.4.33.

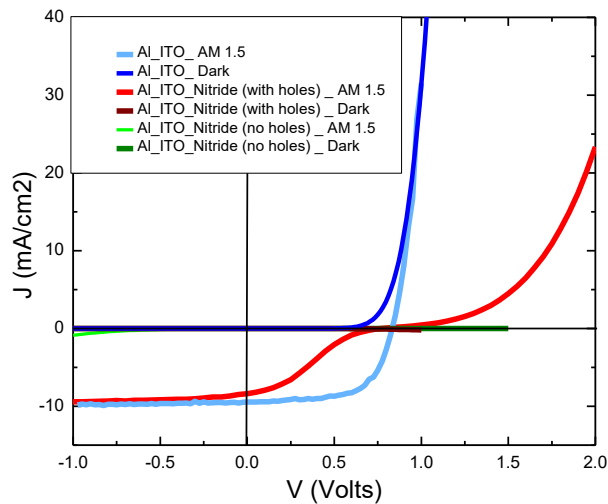


Fig.4.33: (a) Comparison of light and dark J-V curves of the three cells with back reflectors of Al-ITO (blue), Al-ITO covered with 13 nm nitride having holes (red) and Al-ITO covered with a full 13 nm layer of nitride (green).

Figure 4.33 shows a working cell for the device without nitride (Al-ITO) with an R_s of $4.9 \Omega \cdot \text{cm}^2$. It shows as well that the nanocontacts indeed allow the passage of photocurrent, thus a working solar cell is formed on the back-reflector with point contacts. However, an S-type current-voltage curve is observed, reducing the fill-factor, and overshadowing any beneficial impact of the point contacts on a-Si:H cells (and making it tricky to calculate the true series resistance).

This result (S-curves) is similar to one observed in a previous attempt to use point contacts for $\mu\text{cSi:H}$ solar cells [219]. In their case, however, it was observed when no point contacts were formed. The S shape, also called the “roll-over” effect was as well observed for point contacted CIGS solar cells lacking Na. This effect was suppressed by adding an NaF layer evaporated on top of the Al_2O_3 , acting as a passivation layer for CIGS [81], [82], [220].

As the same PIN stack was deposited on the three different cells and the S shape was only observed for the sample having point contacts, this shape is indeed caused by the interface between the back reflector and the n layer. The factors that could affect this interface are therefore either the density of the holes and the distance between them, or the contact between the n layer and the back contact which is an intrinsic feature of the hole formed in the dielectric.

To check if the problem is caused by the high resistance of the carriers passing through the n layer before being collected through the holes, the sheet resistance of this path is calculated by using the illustration shown in Fig.4.34.

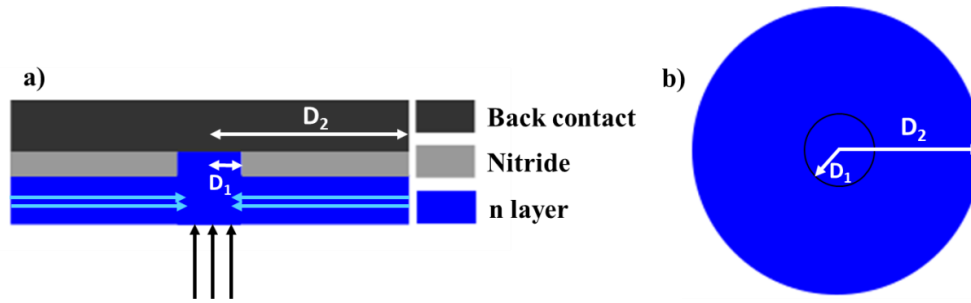


Fig.4.34: Schematic illustration showing (a) cross section of one period representing one hole from the back side of the point contacted device and (b) the top view illustration representing the area of carrier's collection.

Figure 4.34.a shows two different possibility for the carrier's path before being collected by the back contact. The cyan colored arrows represent the lateral carrier's path through the n layer before being collected through the hole, and the black arrows represent the vertical carrier's path without having to pass laterally through the n layer.

D_1 presents the radius of one hole which is 25 nm in this case and D_2 presents the distance from the middle of the hole shown in Fig.4.34 to the edge of the closest hole to it, which is around 240 nm⁶ in this case. The resistance (R) of the n layer (for carriers arriving at the edge) is calculated by representing each section of the circle by a rectangle with a length $L=dr$, a width $W = 2\pi r$ and a thickness $t = 20$ nm (the thickness of the n layer). The calculation is done by solving this integral between the radius of 25 nm and 240 nm:

$$R = \int_{25}^{240} \frac{\rho L}{Wt} = \int_{25}^{240} \frac{\rho dr}{2\pi r t} \quad (4.2)$$

By considering ρ for the n layer equals to 100 Ω .cm [221].

After solving the integral, a value of $180 \times 10^5 \Omega$ is obtained for R . This value is multiplied by the collection area which is πr^2 where r equals 240 nm. The obtained value is 0.032 Ω .cm².

This calculated value remains much smaller compared to the "true" R_s of the point contacted device as 4.9 Ω .cm² was measured as R_s for the device without point contacts (Fig.4.33), and R_s for the device with point contacts is higher compared to that without (Fig.4.31).

This calculation shows that the S shape is not due to the NPs density and distance between them. It is rather due to the intrinsic characteristics of the holes opened in the dielectric layer. Therefore, the NIP stack was again deposited on back reflectors having different thicknesses of SiN_x and SiO₂ with openings. The corresponding J-V curves are shown in Fig.4.35.

⁶ The minimal distance between the NPs (from center to center) is 265 nm.

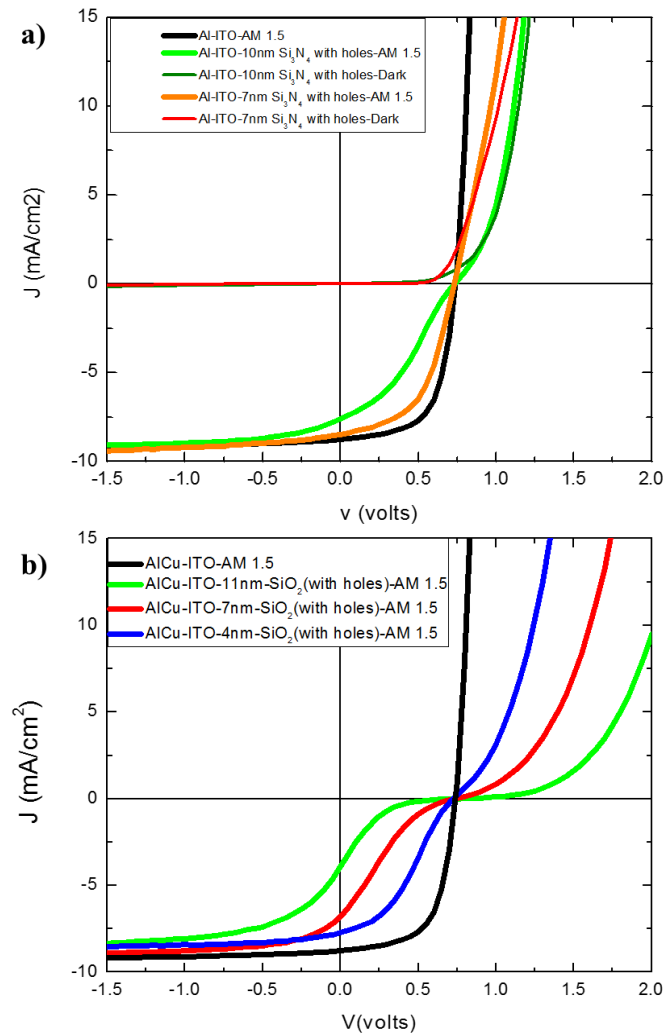


Fig.4.35: Comparison of J-V curves of the cells having as a back-reflector Al-ITO (black) and (a) Al-ITO covered with different nitride thicknesses having holes (green and red for 10 nm and 7 nm nitride, respectively). (b) with Al-ITO covered with different oxide layer thicknesses having holes (green, red and blue for 11 nm, 7 nm and 4 nm oxide, respectively).

It can be seen from Fig.4.35 that the S-curve shape diminished when reducing the SiN_x thickness from 10 nm to 7 nm (Fig.4.35.a), and that of SiO₂ from 11 nm to 4 nm (Fig.4.35.b). The reduction in the S shape is more effective in the case of SiN_x compared to that with SiO₂, probably because of the bigger holes formed in the nitride layer compared to these formed in the oxide layer (Fig.4.9).

The logarithmic dark J-V curves are as well plotted for the three devices whose J-V curves are shown in Fig.4.35.a. These curves are shown in Fig.4.36.

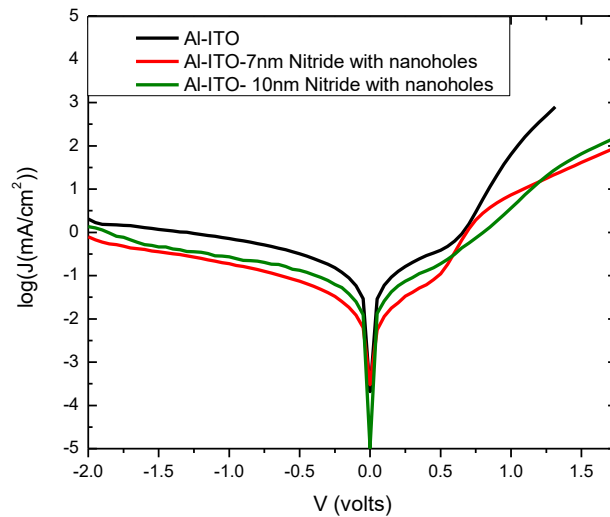


Fig.4.36: Comparison of dark J-V of the three cells having as a back-reflector Al-ITO (black), Al-ITO-7 nm covered with 7 nm nitride having holes (red) and Al-ITO-10 nm covered with 10 nm nitride having holes (green).

All three of these devices display a classical diode shape, with the obvious effects of an R_p and an R_s . A better (higher) R_p but worse (larger) R_s was observed for the point contacted devices compared to the fully contacted device, similar to the results of Fig.4.31. The values of J_0 for the Al-ITO and Al-ITO-7nm nitride samples are similar (both around 28×10^{-5} mA/cm²).

As the S curve shape wasn't completely suppressed, even after reducing the dielectric thickness, it may be due to imperfect masking, non-perfect removal of the NP's or the inability to fully contact through the nanoholes in the dielectric with the n-type layer. As reducing the dielectric thickness reduced the S shape, this suggests that one of the factors causing this shape is the effect of the thin dielectric layer remaining around the hole. Figure 4.37 presents a schematic illustration showing the two possible paths for the carriers to be collected through the oxide with nanoholes.

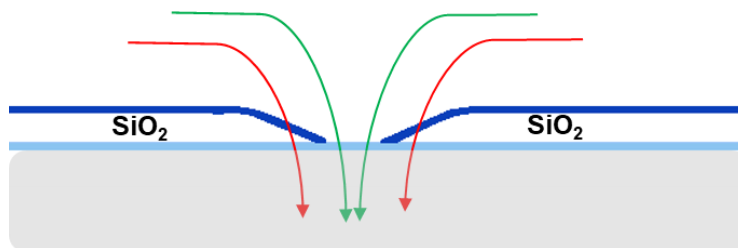


Fig.4.37: Schematic illustration of the two possible paths for the carriers to be collected through the oxide having holes (the grey area representing the metal).

The green arrows of fig.4.37 represent the ohmic path where the substrate is in contact with the metallic layer through the hole. The red arrows represent the path through the oxide, where the carriers will be collected through tunneling effect.

The thin dielectric gradient formed could add an additional resistance to the carrier's path. This resistance would probably decrease with the decrease of the dielectric gradient thickness; thus, the carriers would be collected easier. By decreasing the dielectric thickness, a more conformal contact could be achieved

between the n layer and the back reflector. The ideal case would be to do an isotropic etching in order to get rid of this gradient, thus to obtain a more defined hole. However, it would be tricky to control the etching of the dielectric for approach A, because of their small thicknesses where we will probably end up etching the whole dielectric.

To form well-defined holes in the dielectric, it would be better to use approach B or C instead of approach A, which enable a better control of the openings formed in the dielectric with more flexibility. For this and other practical reasons, approach B was used in the next chapter.

4.3.4 Summary of a-Si:H Solar Cells

It was seen in this section that:

- It is better to deposit the NPs on the back reflector (Al-ITO) rather than depositing them on the PIN stack in order to get a higher NP coverage.
- It was easier to electrically contact the holes formed in the SiN_x by CP-AFM rather than those formed in the SiO_2 , probably because of the larger holes formed in the SiN_x .
- It was possible to make electric contact with the solar cell using the nanocontacts formed in the back reflector, which have a better R_p and worse R_s compared to the fully contacted device. However, an S shape was observed for the light J-V curve for the point contacted cell.
- The interface between the point contacted back reflector and the n layer is the reason why an S shape was only observed for the point contacted device.
- It was possible to decrease the S shape effect by decreasing the dielectric thickness. This decrease was more important for the sample where SiN_x was used as the dielectric compared to the case where SiO_2 was used.
- Approach A should be replaced by approach B or C to get a more controllable process with more defined holes.

4.4 Chapter Summary

Three different approaches based on polystyrene NPs were detailed in this chapter to form holes in a dielectric layer. Approach A consists of forming holes in a thin dielectric layer by covering the NPs with said layer to be patterned followed by NP removal. As for approaches B and C, they consist of forming holes in thicker dielectric layer by depositing the NPs on the layer and using Al as a mask followed by dielectric plasma etching in approach B and a-SiC_x:H as a mask followed by dielectric wet etching in approach C.

Approach A:

- By using this approach, it was possible to form holes in dielectrics covering c-Si and metal-coated glass substrates. However, contacting holes formed in Si samples by CPAFM was tricky due to the small diameter of holes relative to the tip radius.
- This approach was applied to form point contacts for a nip a-Si:H test structure. It was possible to make electrical contact to the solar cell through the nanocontacts formed in the back reflector. However, an S shape was observed for the light J-V curve for the point contacted cell, which was possible to decrease by decreasing the dielectric layer thickness.
- Approach A remains limited in term of controllability, as well as the temperature, the conformity and the dielectric thickness that can be deposited on the NPs. This approach should be replaced by approach B and C.

Approach B:

- An etching of the underlying c-Si substrate was observed when using SF₆ as oxide etchant through nanoholes formed in an Al layer, whereas it wasn't the case when (CHF₃, Ar) was used.
- It was possible to form holes in 120 nm and 240 nm thermally grown oxide. Bigger hole diameters were formed in the oxide compared to the ones formed in the Al masking layer, because of undercut etching. This undercut etching increases with the thickness of the dielectric to be etched.

Approach C:

- This approach wasn't successful when using SiO₂ and Al₂O₃ as the dielectric and using HF or BOE as the wet etching solution.
- It was possible to form holes in the Al₂O₃ by using a "soft" RCA1 etching. However, SEM images show that the holes formed in the Al₂O₃ are not homogeneously defined nor completely etched.
- Further research is needed to refine this technique to achieve good hole opening in the Al₂O₃ film over large areas and with a high yield.

As the best results are obtained for SiO₂ films on c-Si samples using an Al mask (approach B), this method will be used in chapter 5 to act as the doping mask, with the eventual goal of forming point contacts for c-Si solar cells.

Chapter 5: Localized doped nanocontacts in cSi

| | | |
|---------|--|-----|
| 5.1 | <i>Doping through nanoholes</i> | 139 |
| 5.1.1 | Doping by diffusion through nanoholes..... | 140 |
| 5.1.1.1 | Description of masking layer | 140 |
| 5.1.1.2 | Experimental description | 142 |
| 5.1.1.3 | Characterization by SEM and CP-AFM | 145 |
| 5.1.1.4 | Summary – Diffusion results | 170 |
| 5.1.2 | Doping by ion implantation through nanoholes..... | 171 |
| 5.1.2.1 | Overview and Description of Ion Implantation Process | 171 |
| 5.1.2.2 | Experimental description | 174 |
| 5.1.2.3 | Characterization by SEM and CP-AFM | 175 |
| 5.1.2.4 | Discussion and ECV Measurements | 189 |
| 5.1.2.5 | Summary – Ion implantation results | 190 |
| 5.2 | <i>Chapter Summary</i> | 192 |

In chapter 1, the potential advantages of using nanoscale contact openings instead of microscale opening, for cSi technology, was explored by numerical simulations. In Chapter 3, different methods were shown for nanoparticle (NP) deposition and removal after being covered by a metallic or dielectric layer. This was followed in Chapter 4 by three different approaches (A, B, and C) to form nanoholes in thin (<50 nm) and thick (≥ 50 nm) dielectric layers. In the last part of chapter 4, the formation of point contacts for NIP a-Si:H cells was done by testing approach A (removing the NPs after being covered by a thin dielectric). Through this test, it was concluded that approach A is not a controllable method and is limited to forming holes in thin dielectrics. Therefore, approach B (Al used as a mask on the NPs followed by plasma etching of the dielectric through the holes in the Al) will be used in this chapter to form nanoholes, through which local doping will be done. This approach is more flexible and allows one to form holes in thicker dielectrics that are critical to mask the doping.

However, from a practical standpoint, holes formed in Al_2O_3 are not homogeneously defined nor completely etched using the techniques we developed (as seen in Chapter 4 of this thesis). On the other hand, much better results are obtained for SiO_2 films.

Therefore, in the remainder of this chapter, experimental techniques developed in chapters 3 and 4 will be developed to form nanoscale contacts in SiO_2 , followed by results showing localized doping through the contacts by diffusion and ion implantation. Finally, characterization of the local doping will be done by SEM and CP-AFM.

5.1 Doping through nanoholes

Two doping techniques will be explored to form doped areas through the nanoscale holes; doping by thermal diffusion will be developed in the first part of this chapter (5.1.1), and doping by ion implantation in the second part (5.1.2).

Both local doping techniques will use nanoholes formed in SiO_2 . Approach B was used to form holes in 120 nm and 240 nm thermally grown oxide on n type cSi samples using 607 nm and 784 nm PS NPs. Boron doping was done through the holes of the passivation layer and the local doping have been characterized using SEM and CP-AFM. The choice of using a diffusion dopant which is opposite to the doping type of the substrate was to make the characterization easier. However, the same local doping techniques could be used for the same doping type as that of the wafer in order to form PERL structure with openings in the 1 μm range.

The different steps are summarized in the schematic illustration shown in Fig.5.1.

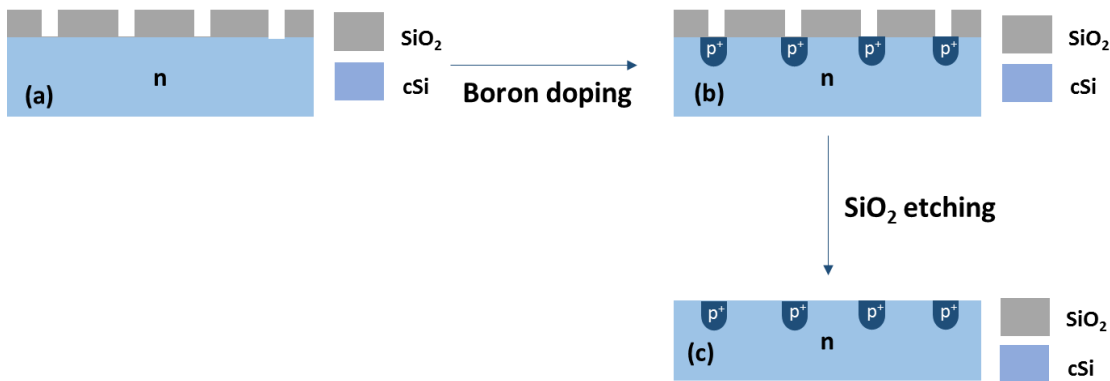


Fig.5.1: Schematic diagram of local doping fabrication process. (a) Forming holes in SiO_2 using approach B (ch.4), (b) Boron doping by thermal diffusion or ion implantation, and (c) SiO_2 etching.

After performing the boron doping, the SiO_2 is removed to perform electrical measurements by CP-AFM.

Diffusion and ion implantation which are the two key methods of impurity doping, are used in this work to dope through the holes of the passivation layer. Generally, the diffusion is used to form deep junction whereas ion implantation is used to form shallow junction.

During diffusion, the dopant atoms are placed on or near the surface of the wafer by deposition from the gas phase of the dopant or by using doped sources. The doping concentration in this case decreases monotonically from the surface and the profile of the dopant distribution is determined mainly by the temperature and diffusion time.

As for the process of ion implantation, the dopant ions are implanted into the semiconductor by means of an ion beam. In this case, the doping concentration has a peak distribution inside the semiconductor, and the profile of the dopant distribution is determined mainly by the ion mass and the implanted-ion energy. The doping profiles of the dopant using both methods are shown in Fig.5.2.

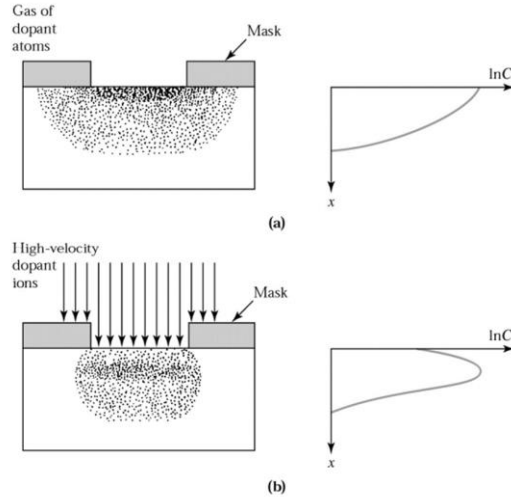


Fig.5.2: Comparison of (a) diffusion and (b) ion-implantation techniques for selective introduction of dopants into semiconductor substrate [4].

5.1.1 Doping by diffusion through nanoholes

5.1.1.1 Description of masking layer

To achieve selective doping on the c-Si substrate, a masking of the unwanted areas with a suitable material should be done before the doping process. Photoresist is not a good option due to the high temperatures used during the diffusion. Metals will also be unsuitable because they can diffuse in the silicon at high temperature. The most commonly used materials are dielectrics such as SiO_2 and Si_3N_4 . These materials are good candidates to be used as a mask for the diffusion as the diffusion coefficient of typical dopant atoms through these dielectrics is several orders of magnitude smaller than that through silicon. For example, the diffusion coefficient of boron through thermally grown SiO_2 is $3.4 \times 10^{-17} \text{ cm}^2/\text{s}$ at $1100 \text{ }^\circ\text{C}$, which is about 3-4 orders of magnitude smaller than the diffusion through silicon. The diffusion profiles of boron through thermally grown SiO_2 and Si at $1100 \text{ }^\circ\text{C}$ for 7200 s is shown in Fig.5.3.

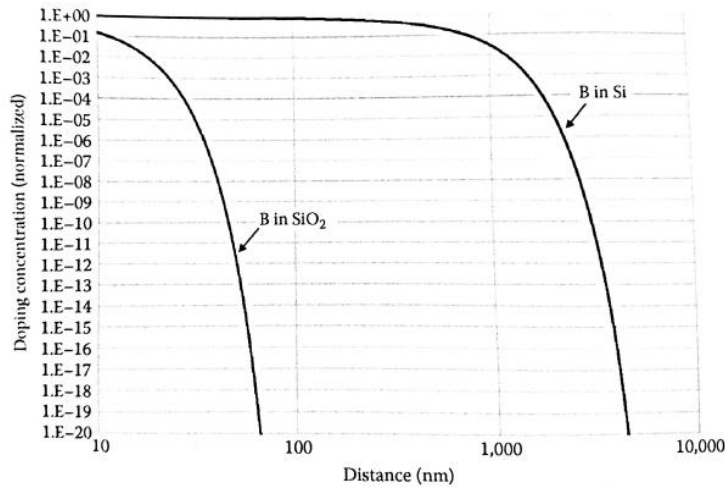


Fig.5.3: Comparison of boron diffusion in Si and SiO_2 at $1100 \text{ }^\circ\text{C}$ [4].

Noticing the difference of the boron diffusion in Si and SiO₂, few nanometers of dielectric thicknesses can be used to prevent diffusion. However, the thickness of the dielectric masking layer chosen at the beginning should be several times larger than the minimum required value because of other mechanisms besides diffusion that can reduce the effectiveness of these masking materials. For instance, the inclusion of sufficient quantities of boron or phosphorous will reduce the dielectrics glass transition temperatures and the films could potentially melt at the diffusion temperatures used, which can eventually consume a small fraction of these masking layers [4]. The author of this graph has normalized the value of the dopant concentration at the surface to 1, and has plotted the graph on log-log scale for clarity. The penetration depth (for 10⁻¹⁵ concentration) in SiO₂ is only 30 nm whereas it is 2060 nm in Silicon. Even by taking in consideration the formation of borosilicate glass, which will be mentioned in the next part of this chapter, and its consumption by melting, a mask thickness of 150 nm can be considered a safe practical value especially when thermal grown oxide is used as a mask as it is more robust than these deposited by PECVD. In the latter case, an even thicker value of SiO₂, such as 250 nm, can be used.

The thickness of the oxide that should be used to mask the dopant from diffusion depends mainly on the temperature and the time of the diffusion. Figure.5.4 shows a plot of the minimum oxide mask thickness needed for a given diffusion time for boron and phosphorous diffusion [222]. The masking oxide was considered to have failed if the impurity level under the mask were to reach a significant fraction (10%) of the background concentration in the silicon.

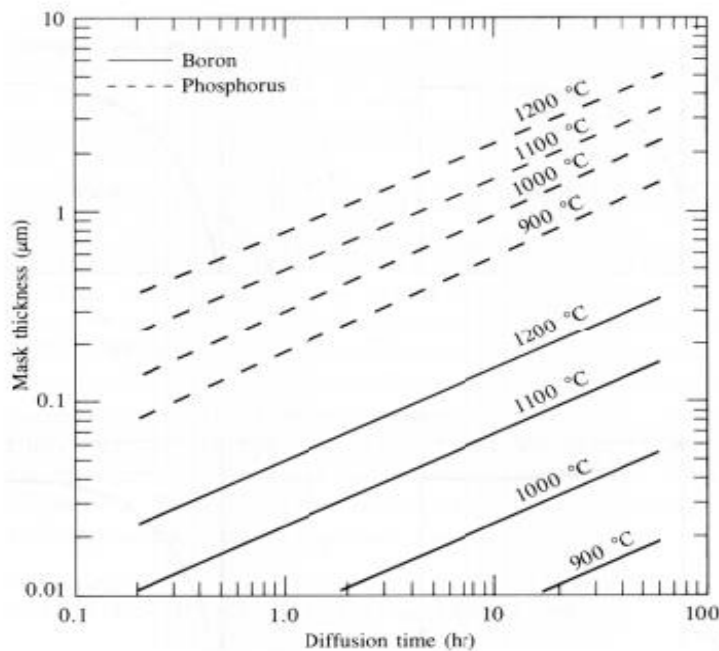


Fig.5.4: Minimum SiO₂ mask thickness needed for successful diffusion of boron and phosphorous in silicon for given temperature and time [222].

The oxide used for masking is usually grown by wet oxidation since the SiO₂ growth rate is much higher when water is used as the oxidant. However, dry oxidation results in a higher-quality oxide that is denser and has a higher breakdown voltage (5-10 MV/cm). Oxide grown by dry oxidation was used in this work as the masking layer.

There are two ways for performing diffusion, depending on the state of the dopant on the wafer surface: (1) constant-source diffusion, also called predeposition or thermal predeposition, in which the concentration of

the desired impurity at the surface of the semiconductor is kept constant; and (2) limited-source diffusion, or drive-in, in which a fixed total quantity of impurity is diffused and redistributed into the semiconductor to obtain the final profile. In our case, the diffusion **was only performed by predeposition** where a solid source of boron was used.

5.1.1.2 Experimental description

The experiment of boron doping by diffusion through the holes will be described in this part. The diffusion was done at the MNT lab at UPC.

N-type doped cSi wafers with a resistivity between $2 \times 10^{15} \Omega \cdot \text{cm}$ and $5 \times 10^{15} \Omega \cdot \text{cm}$ were used in this work. The samples are cleaned, prior to oxidation, with RCA1 ($\text{H}_2\text{O}_2\text{-NH}_4\text{OH-H}_2\text{O}$) to remove organic contaminants from the c-Si surface followed by DI rinsing. Silicon oxide etching by 1% HF for 1 min is then performed to remove the oxide that was grown during the RCA1 cleaning. This is followed by RCA2 cleaning ($\text{H}_2\text{O}_2\text{-HCL-H}_2\text{O}$) to remove heavy metals, alkali ions, and metal hydroxides followed by DI water rinsing. 1% HF for 1 min was again done to remove the oxide that was grown during the RCA2 cleaning.

Thermal oxides of 120 nm and 240 nm thickness were grown on the Si samples in O_2 /dichloroethylene (DCE) ambient at 1060 °C (dry oxidation).

The passivation by thermal oxide gives excellent results on n-type c-Si and poorer on p-type c-Si and p-type emitters. The excellent surface passivation achieved with this film is mainly attributed to a high quality of the cSi/SiO₂ interface that reduces the density of states at the interface. This high-quality interface is due to the growth of SiO₂ onto the Si wafer by oxidation at elevated temperature (800-1200°C). In addition, positive charge densities within the dielectric layer cause a weak field effect passivation [118][223] and contribute to lead to S_{eff} values as low as 2 cm/s (substrate n-type) and 12 cm/s (p-type) [224][116] as was already mentioned (Section 2.1.5 in ch.2). Due to the positive sign of these charges, electrons are attracted to the c-Si surface and holes are repelled. Thus, at the surface of low resistivity p-type c-Si, electron density approaches hole density resulting in an increasing in surface recombination. In contrast, the rejection of holes by the positive charges would be beneficial for n-type cSi, as holes are the minority carriers in this case.

The last step of this approach consists of applying (H_3PO_4 , IPA) to etch the aluminum (Al) masking layer. This is followed by an RCA2 cleaning to make sure that no metals are left on the samples, followed by 1 min dip in 1 % HF.

The thermal diffusion steps consist of cleaning the oven first during 1 h at 830°C . In parallel, the samples received yet another RCA1 and RCA2 cleaning. Each of these cleaning was followed by a 20 s dip in HF (2 %). Boron diffusion was then performed at 875°C in an N_2 ambient during 2 hours and 30 minutes in a quartz tube furnace using planar diffusion sources (PDS) (from Saint Gobain Advanced Ceramics) of boron nitride between the wafers to be doped [225].

During the diffusion, a boron rich layer (BRL) is grown on the sample surface as shown in Fig.5.5.

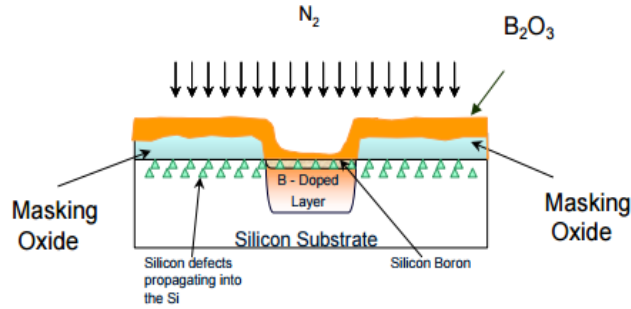


Fig.5.5: Schematic illustration of silicon cross section after boron diffusion [226].

The BRL formed on the SiO_2 can be removed by doing an HF dip step (2% for 1 minute), followed by a special RCA1 (45 minutes) and another HF dip (2% for 1 minute). This will also etch some of the oxide masking layer. However, it is more difficult to remove the Si-B layer formed on the Si interface (inside the SiO_2 holes in our case), which is around 20 nm thick.

A low temperature oxidation step (LTO) is required to oxidize the Si-B layer and a thin layer of Si below it as shown from Fig.5.6.

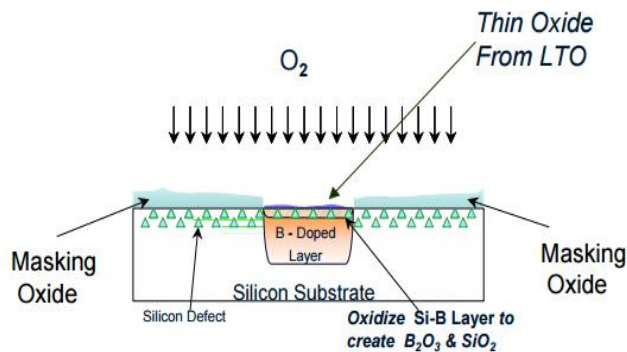


Fig.5.6: Schematic illustration of Si cross section after LTO where Si-B and thin layer of Si is oxidized.

In this work, the LTO was done in a pure O_2 ambient at a temperature of 650 °C for 1 hour. Around 2 min of 5% HF dip is normally enough to remove the $\text{B}_2\text{O}_3/\text{SiO}_2$ layer created by oxidizing the silicon boron (Si-B) layer.

As we are interested in doing a characterization by CP-AFM on the sample without the SiO_2 layer, the last HF dip in our case was long enough to remove completely the thermal masking oxide layer that was used.

All the steps done during the diffusion and the LTO step are summarized in Fig.5.7.

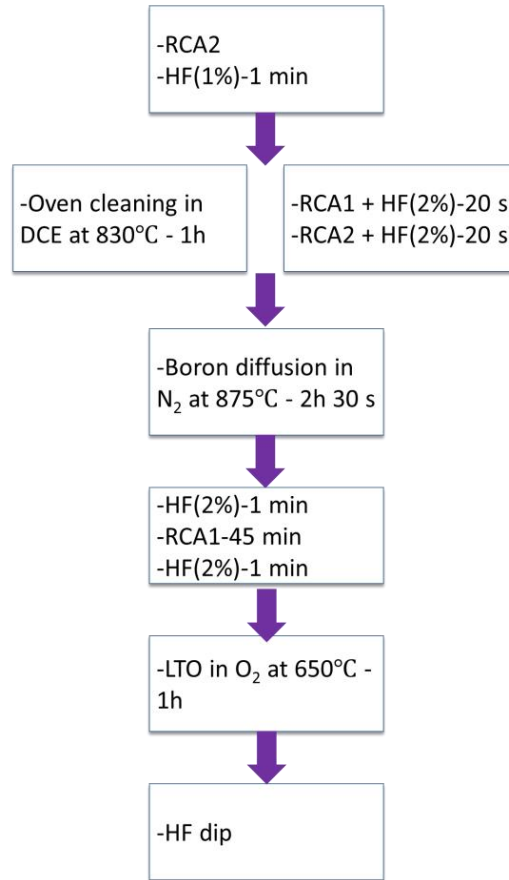


Fig.5.7: Diagram summarizing diffusion and LTO steps.

For the doping by diffusion, two n-doped Si substrates were used, with initial resistivities of 1.03 ohm.cm and 2.2 ohm.cm (initial phosphorous doping concentrations of $5 \times 10^{15} \text{ cm}^{-3}$ and $2 \times 10^{15} \text{ cm}^{-3}$ respectively). “1N” will refer to the sample with smaller resistivity and “2N” will refer to that with higher resistivity.

Oxide layers of 120 nm thickness were grown on the 1N wafers, and 240 nm layers on the 2N wafers. 1N was then cut into two pieces; on the first piece, 600 nm NPs were used to form the holes in the oxide layer and on the second piece, 800 nm NPs were used⁷.

We will first start by presenting the case of the 1N-600 nm, followed by 1N-800 nm, and finally 2N-800 nm will be presented.

Silvaco technology computer-aided design (TCAD) simulation tools was used to simulate the boron concentration as a function of depth in our samples, with and without the 110 nm thermally grown oxide by considering the same dry oxidation process done experimentally to grow the oxide. We have considered 110 nm instead of 120 nm to very roughly consider the oxide etching caused by the HF cleaning steps before the diffusion.

Figure 5.8 displays the boron profile generated by diffusion through the holes in red, and in green, the case outside the holes where a masking oxide was present.

⁷ For simplicity in this chapter, we will refer to 607 nm and 784 nm NPs as 600 nm and 800 nm, respectively.

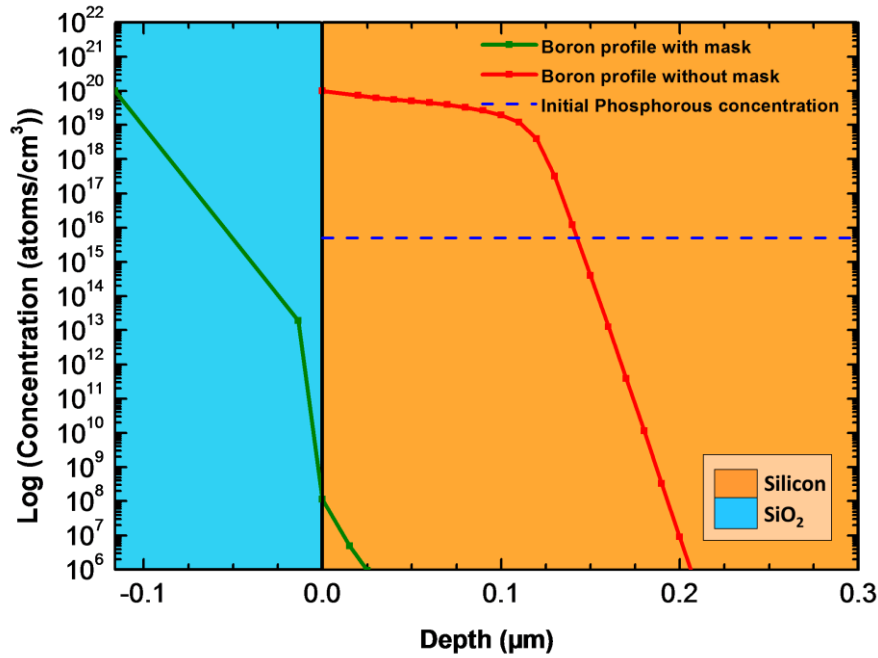


Fig.5.8: Boron and phosphorous concentrations simulated as a function of sample depth with and without 110 nm thermally grown masking oxide.

By considering the case without the thermally grown oxide presented in Fig.5.8, the junction depth is around 142 nm. However, the 110 nm thermally grown oxide will mask the boron diffusion in the silicon substrate. We define efficient masking as a thickness sufficient to keep the part outside of the holes n-type doped, thus the impurity level under the mask smaller than the background concentration (phosphorous concentration) in Si. By this definition, the 120 nm thick thermally grown oxide used for our samples should act as an efficient mask for the boron diffusion.

5.1.1.3 Characterization by SEM and CP-AFM

The importance of developing nanometer-scale measurements of carrier concentration has been highlighted by different roadmaps [227][228] as a critical measurement need for the development of next generation semiconductor and PV devices.

Several groups have compared the techniques which can perform two-dimensional dopant profiling [229][230]. De Wolf et al. have divided these techniques into four categories: (i) 2D techniques based on 1D technique such as secondary ion mass spectrometry (SIMS), (ii) Electron microscopy-based techniques including field-effect scanning electron microscopy (FE-SEM) and electron holography, (iii) inverse modeling techniques, and (iv) Scanning Probe Microscopy (SPM) based techniques. These studies have shown that among the SPM based techniques, scanning Capacitance Microscopy (SCM) and Scanning Spreading Resistance Microscopy (SSRM) are promising tools for quantitative 2D carrier profiling with nanometer resolution [230], [231]. Both techniques can measure the carrier concentration with a resolution below 10 nm within the dynamic range of interest (10^{15} - 10^{20} cm⁻³).

The 2D analysis of carrier distribution in a P-implanted emitter has also been performed using SCM [232], which detects the variation of tip-sample capacitance. Scanning Nonlinear Dielectric Microscopy (SNDM) is another scanning probe microscopy technique that can also measure the variation of tip-sample capacitance but with a higher sensitivity compared to SCM [233]. Super-higher-order (SHO-) SNDM which is an extended version of SNDM, can measure local capacitance-voltage (C-V) curve [234]. It was used by K. Hirose et al. to analyze two-dimensional carrier distributions in Phosphorous (P)-implanted and P-diffused emitters [235].

As for SSRM, extensive works have been published proving that this was the technique of reference to investigate doping at the nano-scale [236][237][238][239]. SSRM and Resiscope (an updated version of the CP-AFM) are very similar techniques; they consist of a conducting probe AFM setup with a logarithmic current amplifier to investigate a large range of resistance. Despite these similarities, the Resiscope is not well known for studying doping levels.

In 2016, P. Narchi has presented proof of concept work on the measurement of doping levels at the nanoscale on calibration samples using the resiscope. He detected doping levels at the nano-scale with a good sensitivity and with a good match to the SSRM profiles for low doping levels (10^{15} - 10^{18} atoms.cm⁻³). However for higher doping levels (10^{18} - 10^{20} atoms.cm⁻³), the sensitivity is degraded [155].

In this work, we will use the SEM and CP-AFM to characterize the samples prepared as described in the experimental description part (Section 5.1.1.2).

Through SEM, we will compare the contrast observed between the boron- doped and the undoped areas. As with CP-AFM, we will do local resistance mapping measurements and local I-V curves that can give information about the performance of the electrical doped holes relatively to the masked part of the substrate.

[Sample 1N-600 nm] Figure 5.9 shows the SEM top view and cross section images of the sample 1N- 600 nm before the doping by diffusion, as well after the diffusion (and the LTO), both before and after the last HF step. All these images were taken at a voltage between 1kV and 5kV by the SE (U) detector (detecting pure secondary electrons (SE)), as previously explained in chapter 2 in section 2.2.2.1.

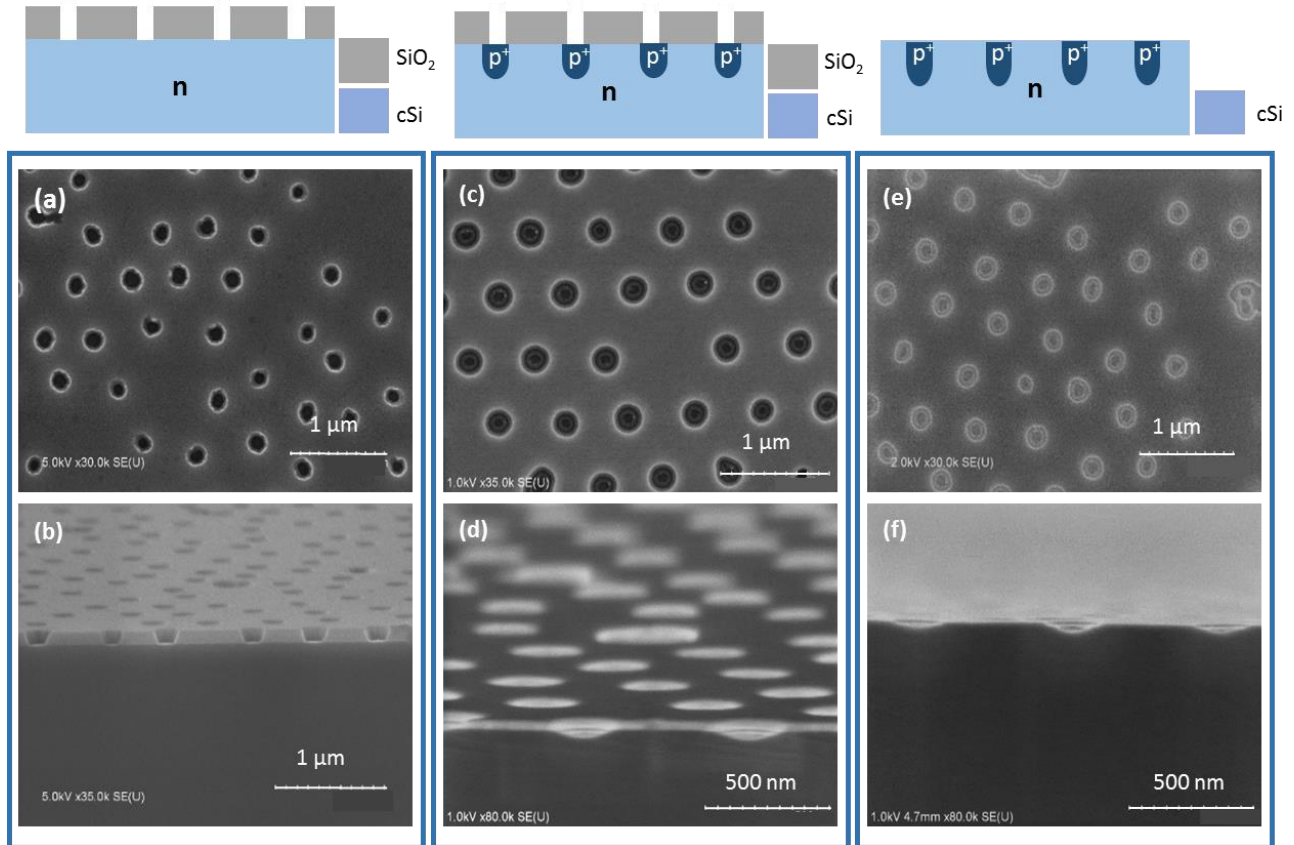


Fig.5.9: SEM images of sample 1N-600 nm showing oxide with holes before diffusion (a) top view and (b) side view. Images showing the remaining oxide after diffusion and LTO with holes (c) top view, and (d) side view. Images showing the doped samples after oxide removal, (e) and (f).

Figure 5.9.a and 5.9.b were already shown in chapter 4 (Fig.4.21.c). They show holes diameter around 220 ± 30 nm and a fraction of opening around 10%.

Figs. 5.9.c and 5.9.d show the sample after diffusion and LTO. It is seen from the SEM cross section that around 33 nm of thermal oxide remained on the sample, of an original oxide layer of 120 nm. This is due to two reasons: (1) the HF steps done to clean the sample before diffusion and those between the diffusion and the LTO to remove the boron layer formed on the oxide during the diffusion, and (2) the oxide etching that occurs during the diffusion. Despite the presence of holes in the oxide, an ellipsometry measurement was also performed on this sample and modelling of the result shows a thickness of remaining oxide of around 25 nm.

Figures 5.9.e and 5.9.f show the sample after SiO_2 removal. From the top view image, the holes appear brighter than the part around it. This can be an indication of the formation of p-doped regions inside the holes, as p-type regions appear brighter than n-type regions in SEM, as explained in chapter 2 in section 2.2.2.1.

In addition, it can be seen that there are holes formed in the Si. From SEM cross section, the depth of this hole is around 35 nm. We can notice that these holes are not smooth, but have a “dinner plate” shape. The silicon etching and the “dinner plate” are due to the process of boron glass formation and etching inside the hole. A schematic illustration to explain the origin of this shape is shown in Fig.5.10.

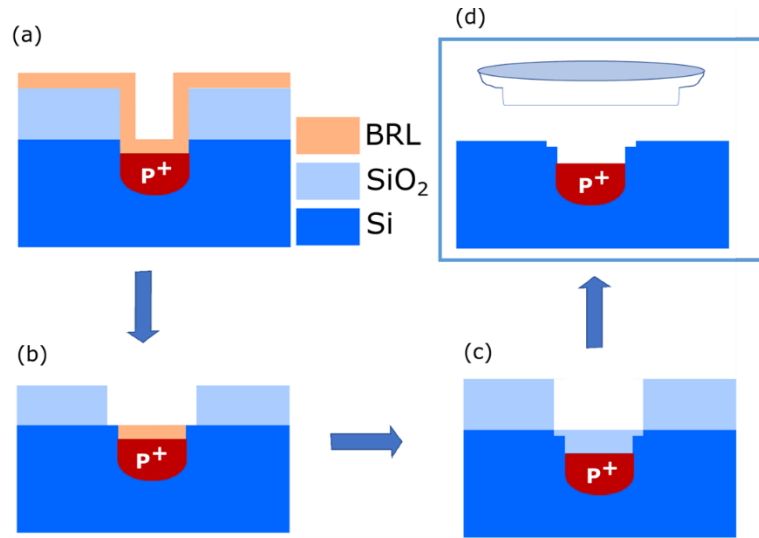


Fig.5.10: Schematic illustration of steps leading to “dinner plate” shape formation inside holes. (a) Cross section of the substrate after boron diffusion, (b) etching of BRL formed on the oxide, (c) oxidation of the Si-B layer and a thin layer of Si below it after the LTO, and (d) etching of the oxidized layer by HF.

Figure 5.10.a represents the cross section of the sample after the boron diffusion, during which a BRL is formed on the sample surface (also shown in Fig.5.5). Figure 5.10.b represents the structure after an HF dip, an RCA1 clean, and a second HF dip, which were done in order to etch the BRL formed on the oxide layer. This step removes a thin layer of the oxide masking layer that was underneath the BRL. Figure 5.10.c is after the LTO step, during which the Si-B formed at the Si interface as well as a thin layer of Si below it are oxidized. Finally Fig.5.10.d represents the structure after the last HF dip that etches away all the oxidized parts, leading to the formation of the shape shown in Fig.5.10.d, similar to what was observed by SEM.

The same shape was observed on 1N-800 nm and 2N-800 nm, which will be presented later in this part of the chapter.

It is noted that only around 30 nm of thermally grown oxide remain after the LTO step. By taking in consideration that two HF dips were done between the diffusion and the LTO step, we can estimate that around 50 nm of oxide were present at the end of the diffusion. It was also visually noted at this point that that the oxide color seen corresponded to a thickness around 50 nm. This is much less than the 110 nm assumed in the simulation of Fig.5.8. TCAD simulation tools were therefore again used to simulate the boron profile that would be generated if the oxide thickness was only around 50 nm. This profile is shown in Fig.5.11.

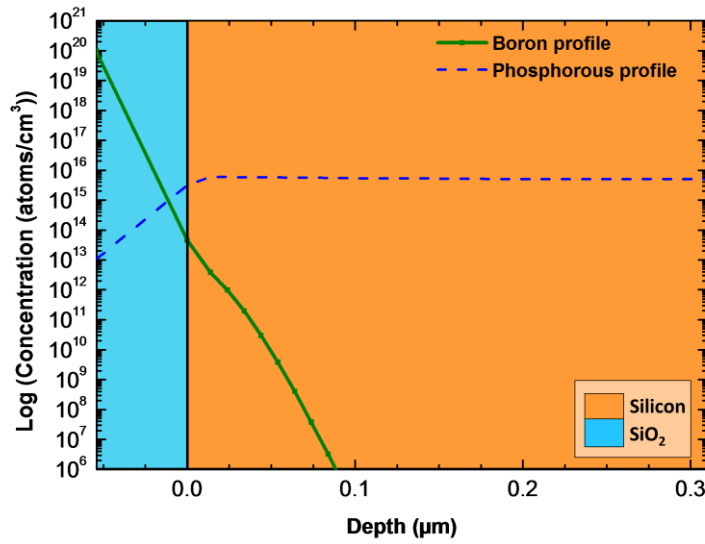


Fig.5.11: Boron and phosphorous concentrations simulated as a function of sample depth for a 50 nm thick masking oxide.

For a 50 nm thick (Fig.5.11) masking oxide, the boron concentration in the Si substrate after diffusion still remains smaller than the initial phosphorous concentration. This shows that despite the thickness reduction due to processing steps, the 120 nm thick oxide chosen as a mask should still provide efficient masking.

The cross sections shown in Fig.5.9.d and 5.9.f were checked more closely and the SEM images are shown in Fig.5.12 using different detectors SE(U) (pure SE) and SE(M) (mixture of SE and back scattered electrons (BSE)).

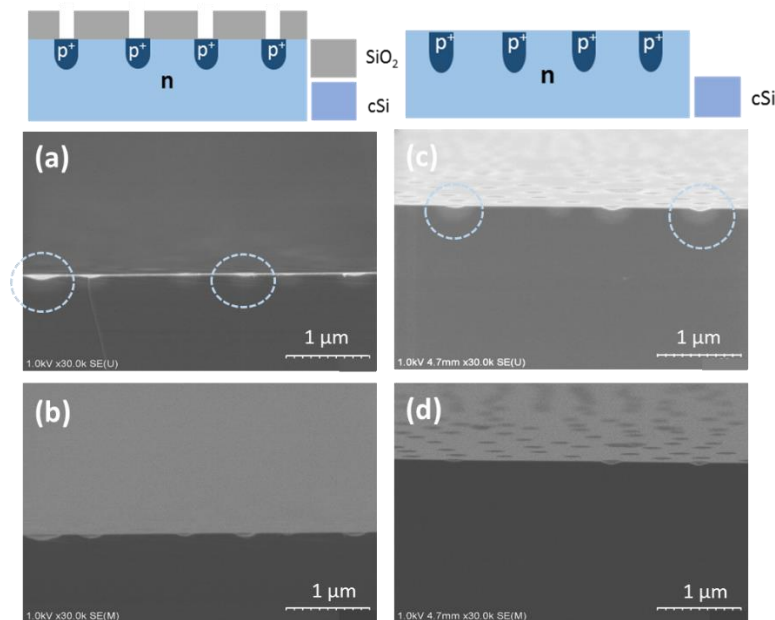


Fig.5.12: SEM cross section images of sample 1N-600 nm after LTO step taken by (a) SE (U) detector, (b) SE (M) detector. After SiO₂ removal taken by (c) SE (U) detector and (d) SE (M) detector.

Localized doped nanocontacts in cSi

Figure 5.12.b and d present the same spots observed in figs.5.12.a and c, but taken using the SE (M) detector. The bright areas under the holes (surrounded by blue circles) appear only when the SE (U) detector is being used, while the SE (M) detector gives only topographical information.

The bright areas correspond to p doped Si in the locations under the holes, this is consistent with previous reports where a brighter image was seen for p-type material compared to n-type regions at low voltages (as discussed in section 2.2.21) [132][133] [134] [135] [136][137][138] [139] [140] [141].

It has a similar shape to the profile shown in Fig.5.2(a). The same effect was observed on samples 1N-800 nm and 2N-800 nm, which will be presented later in this part of the chapter.

It should also be noted that the SEM images shown in Fig.5.9.d and Fig.5.9.f were taken with the same detector as these presented in Fig.5.12.a and 5.12.c and at the same voltage of 1kV. However, no contrast is observed in Fig.5.9.d and Fig.5.9.f between the regions under the holes and the rest of the surface. This difference is due to the difficulty of reproducing the contrast in SE imaging during continuous electron irradiation, which cause surface contamination. Repeated observation of the same area increases the influence of contamination and decreases the dopant contrast. Some groups have proposed solutions to overcome this obstacle. For instance, Tsurimi et al. [137], have revealed that secondary electron (SE) high-pass energy filtering can significantly reduce the influence of contamination, and thus the dopant contrast remains stable during observation. Rodenburg et al. [240], on the other side, have shown that by selecting secondary electrons of low energy, dopant contrast can be enhanced.

In our case, the images shown in Fig.5.12 were taken immediately after cleavage of the samples and by changing often the spots seen on the SEM screen. It was observed during the SEM measurement that if few minutes passed before acquiring the SEM image, this effect is no longer observed.

The SEM images can also differ greatly depending on the detector used. For instance, different levels of contrast are obtained when the SE (U) and SE (M) detectors were used, even at the same voltage of 2 kV. The SEM images are shown in Fig.5.13.

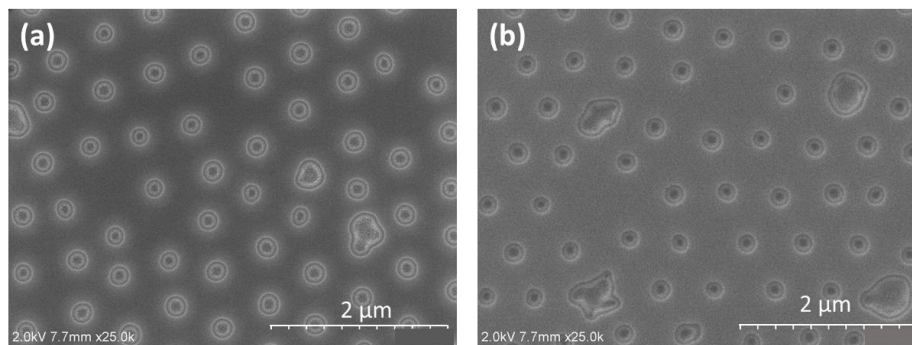


Fig.5.13: SEM images of sample 1N-600 nm taken at 2kV with (a) SE (U) detector and (b) SE (M) detector.

One can see that the holes appear brighter with a bright area appearing around the holes when the SE (U) detector was used, in contrast to when the SE (M) detector is used. However, the same hole diameter is obtained when extracted from both images, ($\sim 225 \pm 30$ nm).

SEM images were taken with the SE (U) detector but at different voltages (1 kV, 2 kV, 5 kV and 10 kV) and at the same magnification and working distance to check if the contrast between the holes and the surrounding area will remain the same. The corresponding SEM images are shown in Fig.5.14.

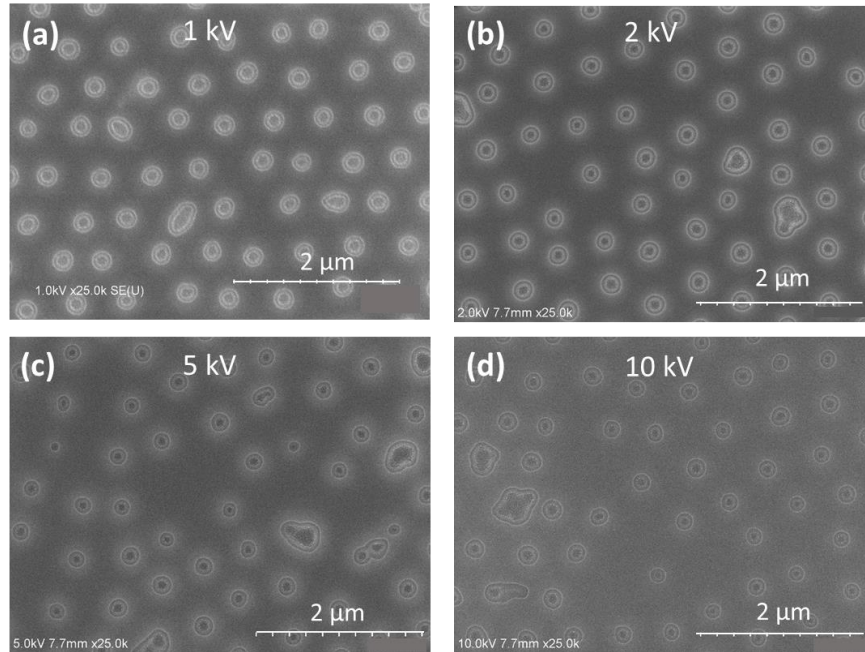


Fig.5.14: SEM images of sample 1N-600 nm taken with the SE (U) detector at (a) 1 kV, (b) 2 kV, (c) 5 kV, and (d) 10 kV.

It can be seen that the contrast between the holes and the surrounding areas decreases when the voltage increases, still showing similar diameters to the one measured previously with the SE (M) detector in Fig.5.13.b. However, the bright area around the holes can be observed in (a), (b) and (c), but fades in (d).

[Characterization by CP-AFM] CP-AFM measurements were done on this sample to obtain the local resistance mapping of the sample surface. The AFM tip used is n⁺ Si coated with polycrystalline diamond doped with boron at the tip of the cantilever (CDT-FMR-20). A schematic illustration of the CP-AFM setup as well of the sample measured are shown in Fig.5.15. The voltage bias is applied on the back side of the sample, allowing measurement of the resulting current flowing through the tip as the sample surface is scanned in contact mode. Measurements are therefore presented as a resistance R (ohms), simply calculated from the voltage and the current.

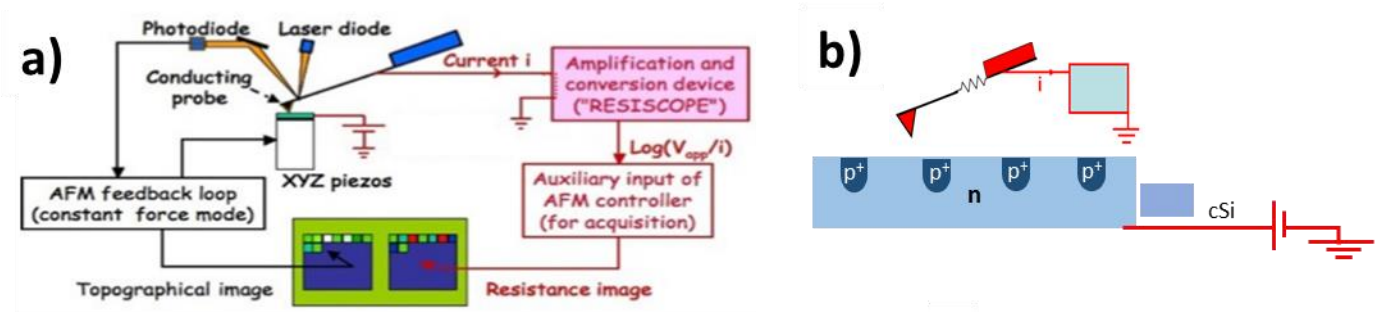


Fig.5.15: Sketch of the CP-AFM measurements; (a) setup at GeePs with the resiscope extension, (b) sample configuration and applied bias.

[Applied voltage of +1 V] Figure 5.16 presents measurements obtained on sample 1N-600nm using a bias of +1 V.

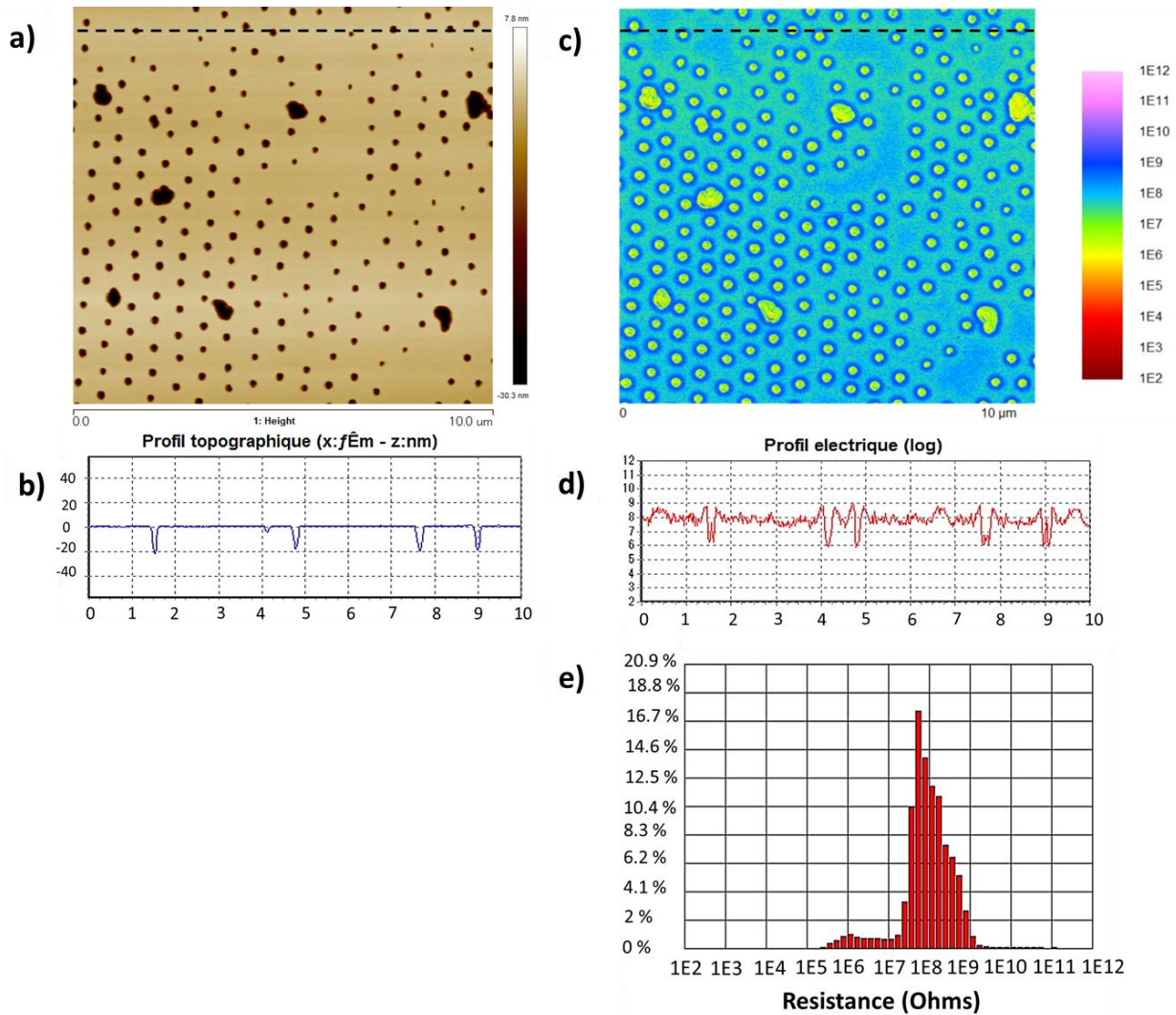


Fig.5.16: (a) Topography image of sample 1N-600 nm, and (b) topography profile corresponding to line selected in (a). (c) Local resistance mapping of the sample while applying a bias of +1 V and (d) the local resistance profile corresponding to line selected in (c) and (e) the total resistance distribution of Fig.5.16.c.

The topography image confirms that there are holes in the Si layer with a mean depth of 27 nm which is smaller than what was measured by SEM in Fig.5.9 (around 35 nm). The mean value of the holes diameter is around 210 nm, which is close to the value seen from the SEM images in Fig.5.13. Using the electrical measurements (fig 5.16.c), the diameter of the hole including the dark blue halo becomes 420 ± 30 nm. However, excluding the dark blue halo, it is 230 ± 30 nm, closer to that measured from the topography image and the SEM image in Fig.5.13 (225 ± 30 nm).

From the local resistance mapping, there is between two and three orders of magnitude of resistance difference between the area inside and that outside of the holes. However, the halo region around the holes (dark blue) appears more resistive than both areas inside and outside the holes. From Fig.5.16.e, it can be

seen that the mean value of the resistance is around 5×10^6 Ohms inside the holes and 2×10^8 Ohms outside the holes.

As for the dark blue halos that appear in Fig.5.16.c, one may wonder if they represent the space charge regions between the p and n regions. To check if this is the case, an approximate value for the thickness of the space charge region was calculated by using the following formula:

$$W_D = \sqrt{\frac{2\epsilon}{q} \left[\frac{1}{N_A} + \frac{1}{N_D} \right] \times (V_b)} \quad , \quad \text{where } V_b = \frac{kT}{e} \ln \left(\frac{N_A N_D}{n_i^2} \right), \quad (5.1)$$

With $\epsilon = 1.04 \times 10^{-12}$ F/cm, $q = 1.6 \times 10^{-19}$ C, $\frac{kT}{e} = 0.025$ V, $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$,

$N_A = 10^{20} \text{ cm}^{-3}$ and $N_D = 5 \times 10^{15} \text{ cm}^{-3}$.

By using this formula, the V_b obtained is 0.88 V and W_D obtained is 480 nm. However, the width of the dark blue halo from Fig.5.16 is 90 ± 16 nm, inconsistent with the hypothesis that it is the space charge region (at least for the values estimated).

Another reasonable explanation for this halo is that it is a topographical feature probably related to oxide. Therefore, a 1 min dip of the sample in 1 % HF was done followed by a repetition of the CP-AFM measurement by applying a bias of +1 V, the results of which are shown in Fig.5.17.

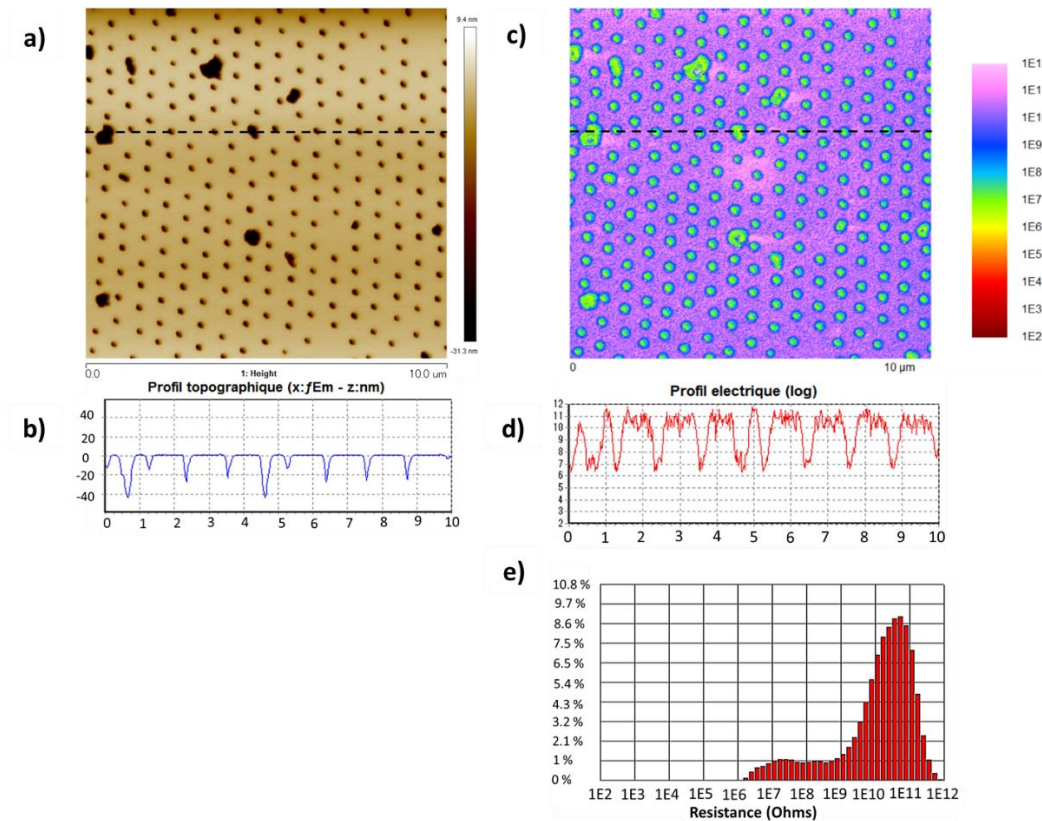


Fig.5.17: (a) Topography image of sample 1N-600 nm after HF dip, and (b) topography profile corresponding to line selected in (a). (c) Local resistance mapping after HF dip while applying a bias of +1 V, (d) local resistance profile corresponding to line selected in (c) and (e) total resistance distribution of fig(c).

After the HF dip, it was seen from the topography measurements that the hole diameters increased to 240 nm (compared to 210 nm before HF dip) but with similar depths. As for the local resistance measurement, the mean value of the resistance increased to 4×10^{10} Ohms outside the holes (2×10^8 Ohms before HF dip). Inside the holes, it remained like the previous case: resistance between 6×10^6 Ohms and 2×10^7 Ohms was measured.

In addition, it was seen that the width of the dark blue halo in the resistance measurement decreased from 90 ± 16 nm (Fig.5.16) to around 60 ± 16 nm (Fig.5.17), while the area of the inside green part remained the same.

[Comparing -1 V to +1 V] Another area from the same sample was checked after HF dip by applying +1 V while measuring the first half of the image and switching to -1 V while measuring the second half. The corresponding topography and electrical measurements are shown in Fig.5.18.

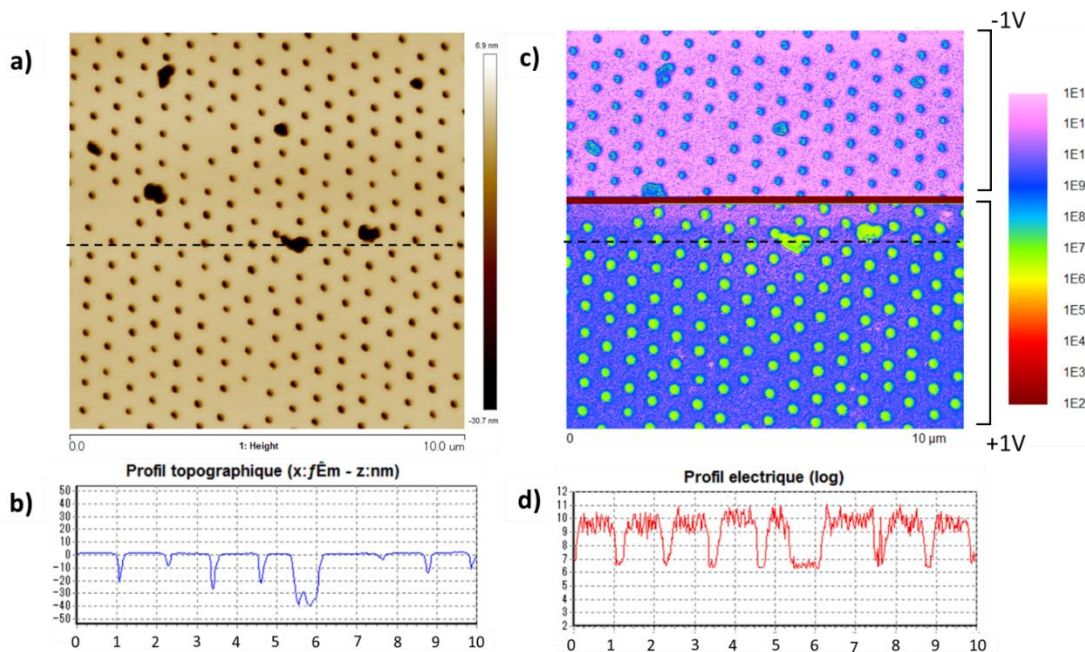


Fig.5.18: (a) Topography image of sample 1N-600 nm after HF dip, and (b) topography profile corresponding to line selected in (a). (c) Local resistance mapping of sample 1N-600 nm after HF dip while applying a bias of -1 V (upper part) and +1 V (lower part), (d) local resistance profile corresponding to line selected in (c).

Importantly, the sample is more resistive, both inside and outside the holes, when -1 V was applied then when +1 V was applied.

As different conductivity behavior is observed when -1 V and +1 V was applied on the sample, one can state that the sample is not acting as a simple resistance (for which the same behavior is expected regardless of the electrical polarity). Local I-V measurements were therefore done on the sample to analyze the electrical behavior difference between the part inside and outside the holes.

[I-V curve] Current voltage (I-V) curves were measured locally both inside and outside the holes, and they are shown in Fig.5.19 in linear (Fig.5.19.a) and logarithmic scale (Fig.5.19.b). These curves confirm an important insight: **we should not be analyzing these samples using resistance mapping, but rather by considering them as the p-n junctions that we were aiming to form.**

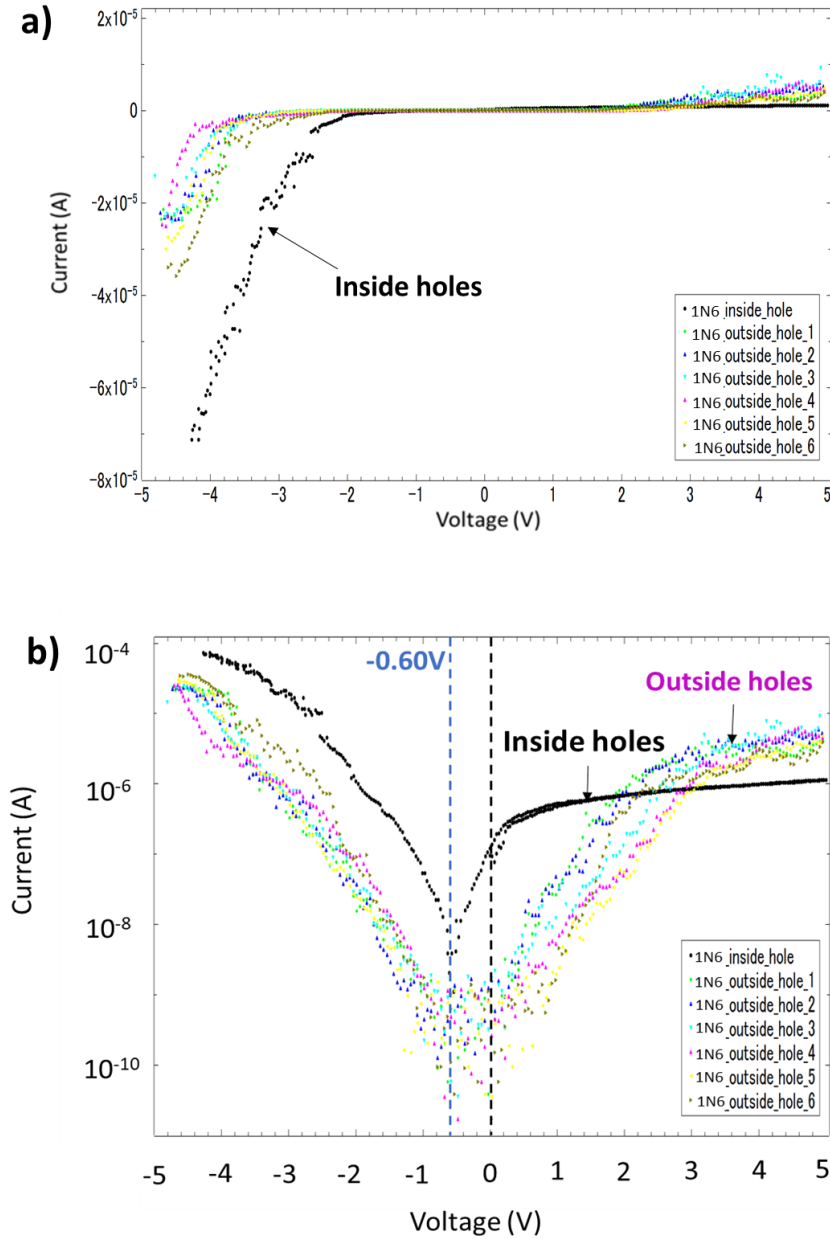


Fig.5.19: I-V curves measured locally inside and outside 1N-600 nm holes in (a) linear scale and (b) log scale.

An asymmetric, p-n junction-like behavior was observed for areas inside the holes. Furthermore, these curves display a shift in the zero-crossing of 0.6 V, i.e. giving a V_{OC} . This - along with a clear value of J_{SC} - confirms that a solar cell is indeed formed inside the holes. This is the strongest possible confirmation of successful boron doping inside the holes. As an additional note of how resistance mapping could be extremely misleading for such devices, note that if a CP-AFM mapping was done at +2 V and -2 V, no significant difference would be observed in the conductivity as similar current is measured at both voltages.

In further analyzing these I-V curves, one notes that a higher current is observed for the areas inside the holes compared to that outside the holes at negative voltages (forward bias). Nevertheless, the areas outside the holes do display a diode-like behavior. However, due to the noise observed for these I-V curves, it is

not clearly seen if the curves intersect the x-axis at 0 V or if there is a voltage offset. Therefore, no photovoltaic device behavior is observed for the areas outside the holes.

Attributing the presence of a V_{oc} for the areas inside the holes to a photovoltaic effect requires a source of illumination. This is provided by the red laser spot in the AFM used to measure the position of the tip (chapter 2). In fact, the parasitic effect of this red laser does not allow one to perform the I-V measurements in real dark conditions. In fact several groups have reported this artefact for solar cells [241][242][243][244]. Some other groups have also reported techniques to avoid this artefact. For instance, Jae S. Yun et al. have used 1300 nm as the laser light wavelength used for the AFM beam deflection, which is higher than the crystalline silicon bandgap [245]. Yanfeng Ji et al., have avoided this parasitic effect by performing the measurement without the AFM laser on. Two-pass measurements were performed; on the first pass the AFM laser was on and only the topography was recorded and on the second pass the AFM laser was off, the tip follows the topography recorded and measures the current and resistance without the influence of the laser illumination [246].

To confirm that the laser is the source providing a V_{oc} , an I-V measurement will be presented later in this chapter on the same sample by using an AFM having a laser head of 670 nm as wavelength and another of 1300 nm.

After having presented the resistance mapping measurements and the I-V local measurements, we can conclude that a p-type doped region was successfully formed inside the holes. An illustration of a spot of the cross section of the sample 1N-600 nm is presented in Fig.5.20.

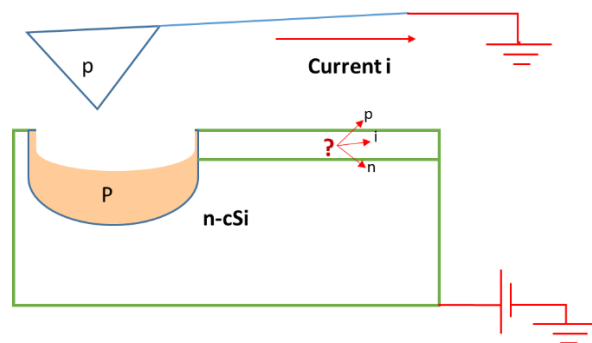


Fig.5.20: Cross section schematic illustration of sample 1N-600 nm showing expected doping type of both inside and outside the hole.

Although we are certain that p-type doping occurring within the area under the hole, we are not sure about the doping outside the holes. Three situations may arise: an n-type surface (no diffused doping), compensation (giving an intrinsic layer at the surface, very improbable) or a lightly p-type surface.

If we expect that the masking by SiO_2 was efficient and no boron dopants penetrated in the part outside the holes (as was shown by the TCAD simulation done in the first part of this chapter), this part should remain n-type doped. Nevertheless, a junction could form between the AFM tip (p-type diamond) and the n-type sample surface. This is consistent with the diode performance observed for the part outside the hole, which is a sign of a p-n junction formation. However, the area of this junction would be determined by the contact area of the tip, so far smaller in area compared to the junction formed under the holes. This explains the higher current (both collected and driven) when measuring the part inside the holes (Fig.5.19.b).

If, however, the area outside the holes was to become lightly p-doped by boron dopants diffusing through the masking SiO_2 , a junction could form between the top part of the sample that is lightly p-doped and the

n type underneath it. However, given that no V_{oc} is seen outside the holes, and that the current is far smaller, this situation does not seem to be the one supported by experimental evidence.

[1N-800 nm] 1N-800 nm was another piece of “1N” (resistivity of $5 \times 10^{15} \text{ cm}^{-3}$) on which 800 nm NPs were used to form the holes in the 120 nm oxide masking layer. The same steps were done on this sample as for 1N-600nm; they are summarized in Fig.5.21, which also shows the SEM images of the sample at various points in the process.

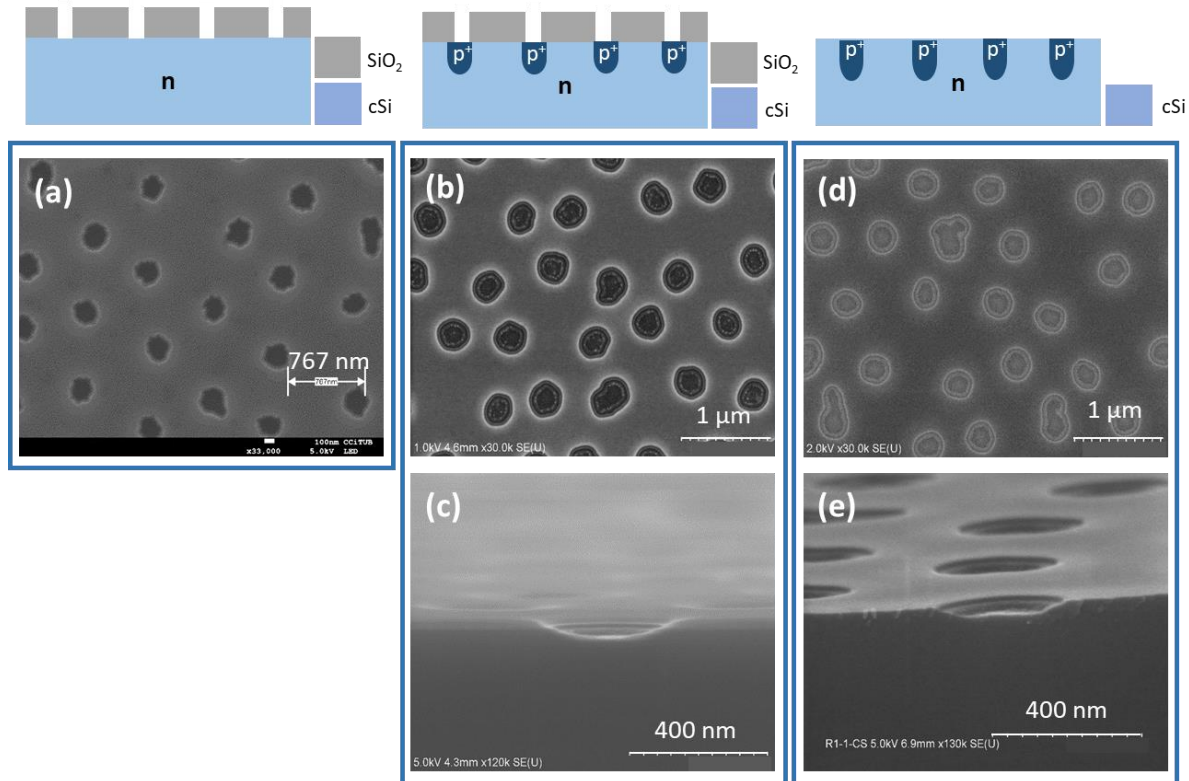


Fig.5.21: SEM images of sample 1N-800 nm showing oxide with holes before diffusion (a) top view. Images showing remaining oxide after diffusion and LTO with holes (b) top view, and (c) Side view. Images showing the doped samples after oxide removal (d) top view and (e) Side view.

Figure 5.21.a was already shown in chapter 4 (Fig.4.21.d). It shows hole diameters around $260 \pm 20 \text{ nm}$ with opening fractions around 8.5 %. Figures 5.21.b and 5.21.c correspond to the step after LTO. It is seen from the SEM cross section that around 33 nm of thermal oxide remained on the sample. Ellipsometry measurements show around 20 nm thickness of remaining oxide. Figures 5.21.d and 5.21.e show the surface after SiO_2 removal. From the top view image, the holes appear brighter than the part around it. The hole diameters are around $350 \pm 20 \text{ nm}$.

It can as well be seen from the cross section shown in Fig.5.21.e that the holes have a “dinner plate” shape, similar to the one explained previously in Fig.5.9(f) and Fig.5.10.

The cross-sections of sample 1N-800 nm after LTO (Fig.5.21.b and 5.21.c) and after SiO_2 removal (Fig.5.21.d and 5.21.e) were again characterized with SEM by observing the same locations with both SE (U) and SE (M) detectors at a beam energy of 1kV. The resulting images are shown in Fig.5.22.

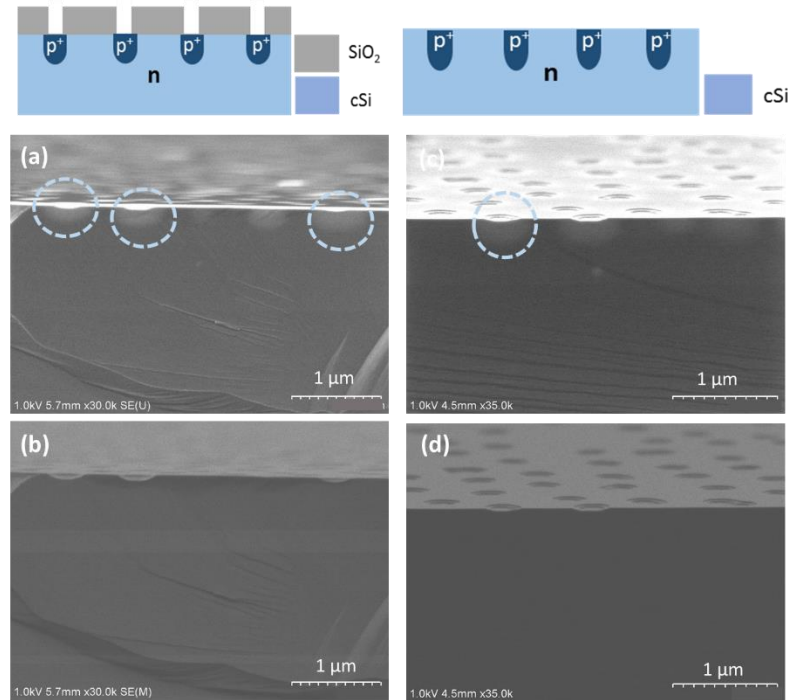


Fig.5.22: SEM cross section images of sample 1N-800 nm after LTO step taken by (a) SE (U) detector, (b) SE (M) detector. After SiO₂ removal taken by (c) SE (U) detector and (d) SE (M) detector.

The small parts under the holes appear brighter than the other parts of the images, as observed for the previous sample (Fig.5.12).

[Characterization by CP-AFM] CP-AFM measurements were also done on this sample before and after a dip in 1 % HF during 1 min and the results are shown in Fig.5.23.

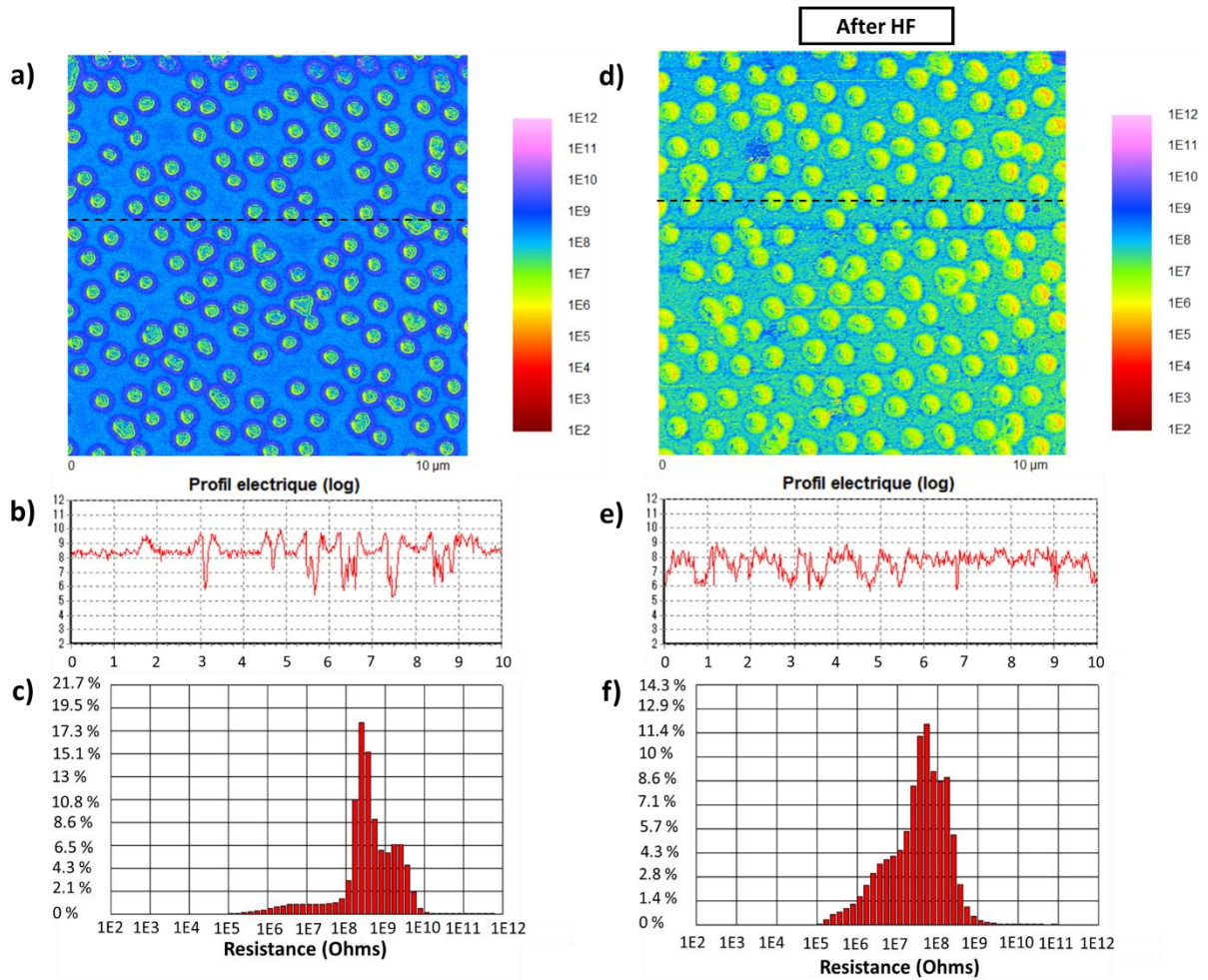


Fig.5.23: (a) Local resistance mapping of sample 1N-800 nm while applying a bias of +1 V (b) local resistance profile corresponding to line selected in (a) and (c) total resistance distribution of fig(a). (d) Local resistance mapping at +1 V after HF dip, (e) local resistance profile corresponding to line selected in (d) and (f) total resistance distribution of fig(d).

It is seen from the topography image (not shown in Fig.5.23) that the mean holes diameter is 390 nm with a mean depth of 32 nm, and they increased to 445 nm after HF.

As for the local resistance measurement inside the holes, we find 4×10^7 Ohms as mean value of the resistance (Fig.5.23.a), which slightly decreased to 1×10^7 Ohms after HF dip (Fig.5.23.d). Outside the holes, 3×10^8 Ohms was measured as mean value (Fig.5.23.a), which decreased to 6×10^7 Ohms after HF dip (Fig.5.23.d).

The width of the dark blue halo is 140 ± 15 nm in the case of Fig.5.23.a, whereas it is barely seen for the case after HF dip (Fig.5.23.d). The hole diameter measured from the electrical image (Fig.5.23.a) by including the dark blue halo is 635 ± 40 nm as for that measured by excluding the dark blue halo, it is 350 ± 25 nm. This latter is closer to the holes diameter measured from the AFM topography image and that measured from the SEM image in Fig.5.21.d (350 ± 20 nm).

As for the case after HF dip (Fig.5.23.d), the hole diameter measured from the electrical measurement is 560 ± 50 nm, which is considered as an increase of the green part of the holes observed before HF dip (350 ± 25 nm).

The decrease in the halo width after HF dip was as well observed for the previous sample 1N-600 nm after HF dip, however the area of the green part of the holes remained the same in that case (1N-600) contrary to the increase of that area which is observed here for 1N-800 nm.

[I-V curve] The local I-V measurements were also done in this sample both inside and outside the holes. The I-V in log scale is shown in Fig.5.24.

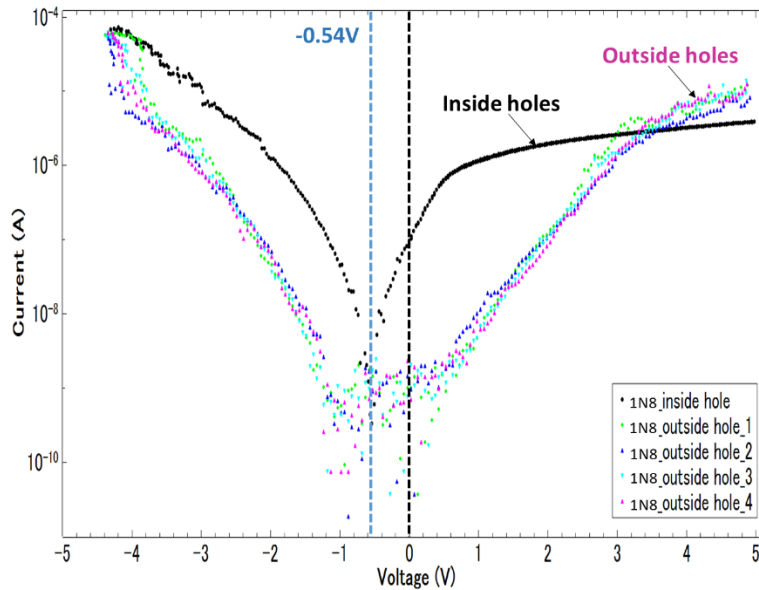


Fig.5.24: I-V curves measured locally inside and outside holes for 1N-800 nm in log scale.

A solar cell behavior was also observed for the area inside the holes (as was seen for sample 1N-600 nm in Fig.5.19), but with a V_{oc} of 0.54 V in this case. The current measured inside the holes is also higher compared to that outside the holes at negative voltages (forward bias), which is similar to Fig.5.19. As for the part outside the holes, noise is observed in the I-V curves which make uncertain the presence of a voltage offset in this case, thus uncertain if the laser is photogenerating in this part. Therefore, it can't be confirmed if a p-n junction is formed outside the holes (as for sample 1N-600 nm).

[2N-800 nm] Sample 2N (resistivity of 2×10^{15} cm^{-3}) was covered with 240 nm SiO_2 and 800 nm NPs diameter were used to form holes in the oxide.

TCAD simulation tools was used to simulate the boron concentration as a function of depth in "1N" without the thermally grown oxide. 142 nm was obtained as junction depth. As the TCAD shown in Fig.5.8 shows that 110 nm thick oxide could mask efficiently the boron from diffusing to the part underneath the mask, then 240 nm will surely be an even more efficient masking.

The same steps done on the previous two samples were also done on 2N and summarized in Fig.5.25, which also gives the SEM images after various steps.

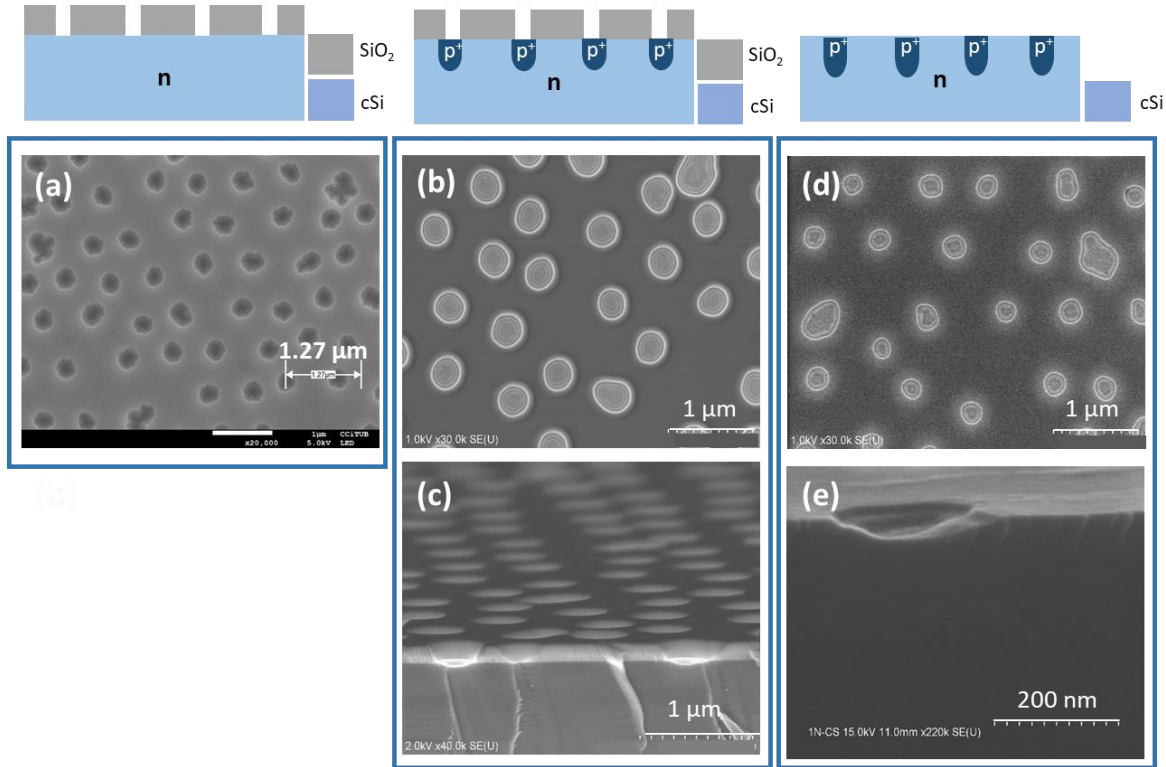


Fig.5.25: SEM images of samples 2N-800 nm showing oxide with holes before diffusion (a) top view. Images showing remaining oxide after diffusion and LTO with holes (b) top view, and (c) Side view. (d) and (e) Images showing doped samples after oxide removal.

Figure 5.25.a was already presented in chapter 4 (Fig.4.21.b). They show hole diameters of 340 ± 20 nm with opening fractions of 15 %. The thickness of the remaining oxide layer was determined from the SEM cross section of the sample after LTO and from ellipsometry measurements. Although ellipsometry measurements are only appropriate for the thickness measurement of conformal and continuous oxide layers (and therefore not our layers) there was only 10 nm difference between the thickness measured by ellipsometry (130nm) and that measured by the SEM cross sections (143nm).

From Fig.5.25.d, it can be seen that the holes appear brighter than the area surrounding them. As well, from Fig.5.25.e it can be seen that the holes have similar shape (“dinner plate”) to the two samples seen earlier (1N-600 nm and 1N-800 nm).

The top view of the sample after LTO was taken at different spots using both detectors SE (U) and SE (M) at the same voltage of 2 kV and at the same working distance of 9 mm. These images are shown in Fig.5.26.a and Fig.5.26.c, respectively. Another SEM image was taken by the SE (U) detector at 1kV and 8 mm of work distance, and is shown in Fig.5.26.b.

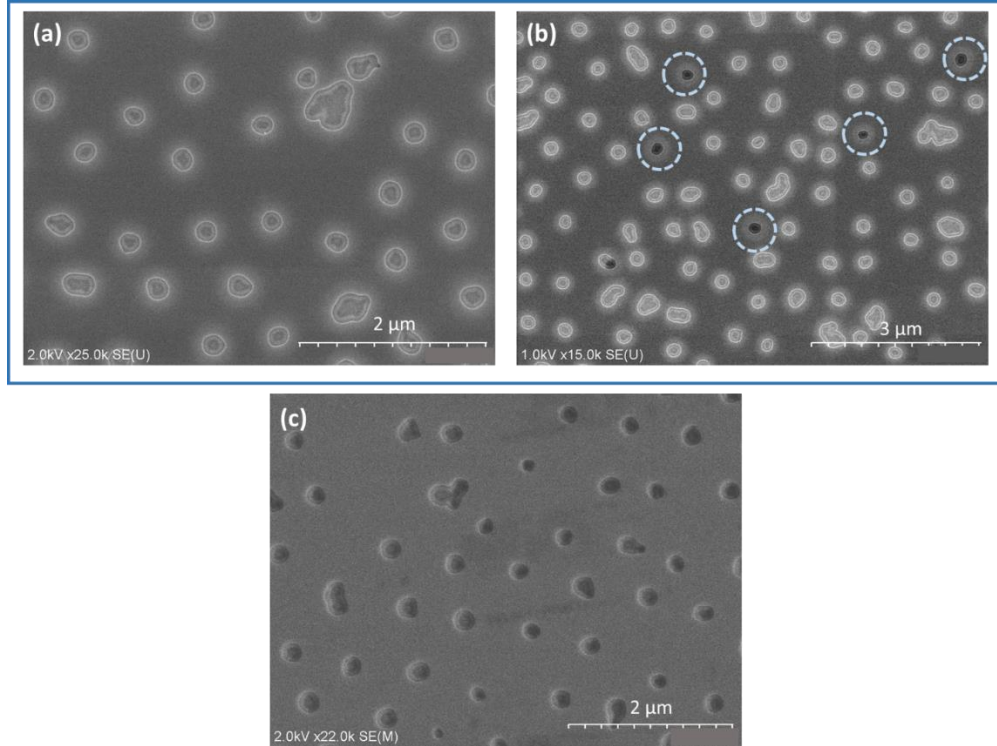


Fig.5.26: SEM images of sample 2N-800 nm taken with SE (U) detector at (a) 2 kV and (b) 1 kV and (c) with SE (M) detector at 2 kV.

Comparing Fig.5.26.a and 5.26.c, it can be seen that the holes appear brighter when the SE (U) detector was used than for the SE (M) detector, although similar hole diameters of 235 ± 30 nm are observed. This observation concerning the contrast is consistent with the observations seen for the two previous samples.

However, it can be seen from Fig.5.26.b that some of the holes (circled by dashed line) appear dark. This can be attributed to the absence of active boron inside the holes due to an incomplete NP removal in these locations, leading to a non-etching of the SiO_2 . It could also be attributed to an incomplete diffusion of boron in these spots.

The cross section of the sample 2N-800 nm after LTO (Fig.5.25.b and 5.25.c) and after SiO_2 removal (Fig.5.25.d and 5.25.e) were again characterized with SEM by taking the same spots with both SE (U) and SE (M) detectors at 1kV. These images are shown in Fig.5.27.

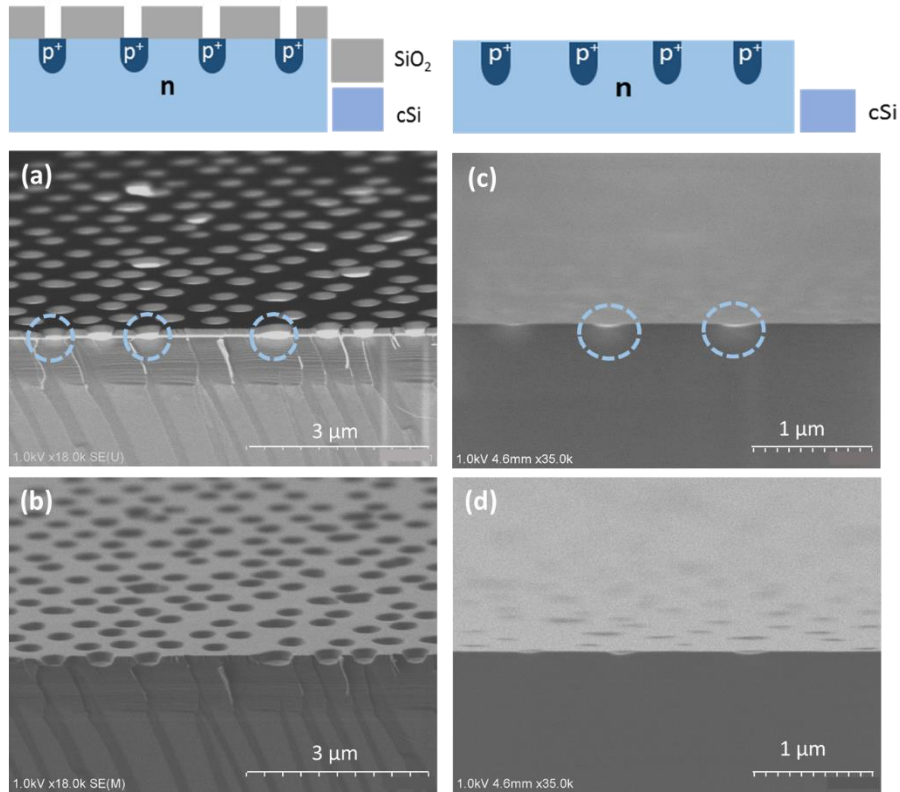


Fig.5.27: SEM cross section images of sample 2N-800 nm after LTO step taken by (a) SE (U) detector, (b) SE (M) detector. After SiO₂ removal taken by (c) SE (U) detector and (d) SE (M) detector.

The areas under the holes appear bright while using the SE (U) detector, which is consistent with the observations seen with both detectors for sample 1N-600 nm (Fig.5.12) and 1N-800 nm (Fig.5.22).

[Characterization by CP-AFM] The CP-AFM measurements were done as well on this sample. They are presented in Fig.5.28.

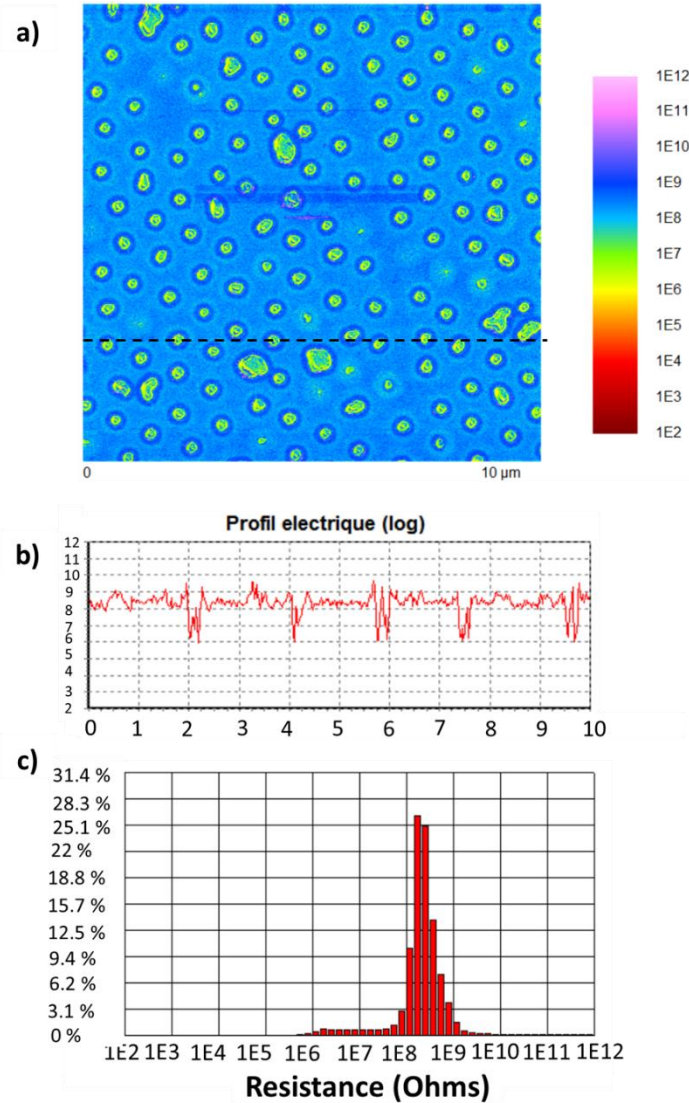


Fig.5.28: (a) Local resistance mapping of sample 2N-800 nm while applying a bias of +1 V, (b) local resistance profile corresponding to line selected in (a) and (c) total resistance distribution of fig(a).

From the topography image (not shown in this figure), the mean hole diameter measured is 300 nm with a mean depth of 30 nm, which is a bit higher than as observed by SEM image in Fig.5.26 (235 ± 30 nm). As for the local resistance measurement, 2×10^7 Ohms is measured as mean value of the resistance inside the holes, and 2×10^8 Ohms outside the holes, thus a difference in resistance of one order of magnitude inside and outside the holes (although from the previous discussion, it should now be understood that such measurements hold little useful information).

The width of the dark blue halo is 120 ± 20 nm in this case. By using equation 5.1, the expected space charge region or this sample is 724 nm, which is again bigger than the width of the dark blue halo. As for the diameter of the hole measured from the electrical measurement by including the dark blue halo, it is 485 ± 60 nm and for that measured by excluding the dark blue halo it is 250 ± 45 nm. We can see that the hole measured by excluding the dark halo is closer to the diameter measured from the topography image as well to that measured from the SEM image from Fig.5.26.

The CP-AFM measurement was repeated after an HF dip on this sample as was done for samples 1N-600 nm and 1N-800 nm, but it isn't presented here as marks due to contamination appeared on the local resistance measurement.

[I-V curve] I-V measurements were taken inside and outside the hole of this sample after the HF dip. The resulting curves are shown in Fig.5.29.

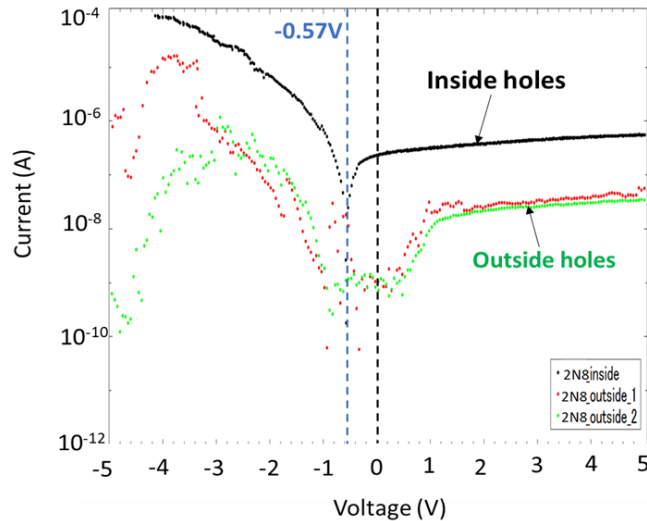


Fig.5.29: I-V curves measured locally inside and outside holes of sample 2N-800 nm in logarithmic scale.

A solar cell behavior was also clearly observed on this sample for the areas inside the holes (as was seen for sample 1N-600 nm and 1N-800 nm in Fig.5.19 and Fig.5.24, respectively) but with a V_{oc} of 0.57 V in this case. The current measured inside the holes is also higher compared to that outside the holes at negative voltages (forward bias). As for the area outside the holes, the shapes of the I-V curves are unusual, possibly due to residues observed in the areas outside the holes.

[Infrared laser] Local I-V measurements were repeated inside the holes using two AFM setups. One setup uses a 670 nm wavelength laser (Bruker) and has been used for all measurements to this point. The second AFM setup uses a 1300 nm wavelength laser (Combscope). The results of these measurements are shown in Fig.5.30 (*NB: The polarity of the applied voltage is opposite to that applied for the measurement of Fig.5.29*).

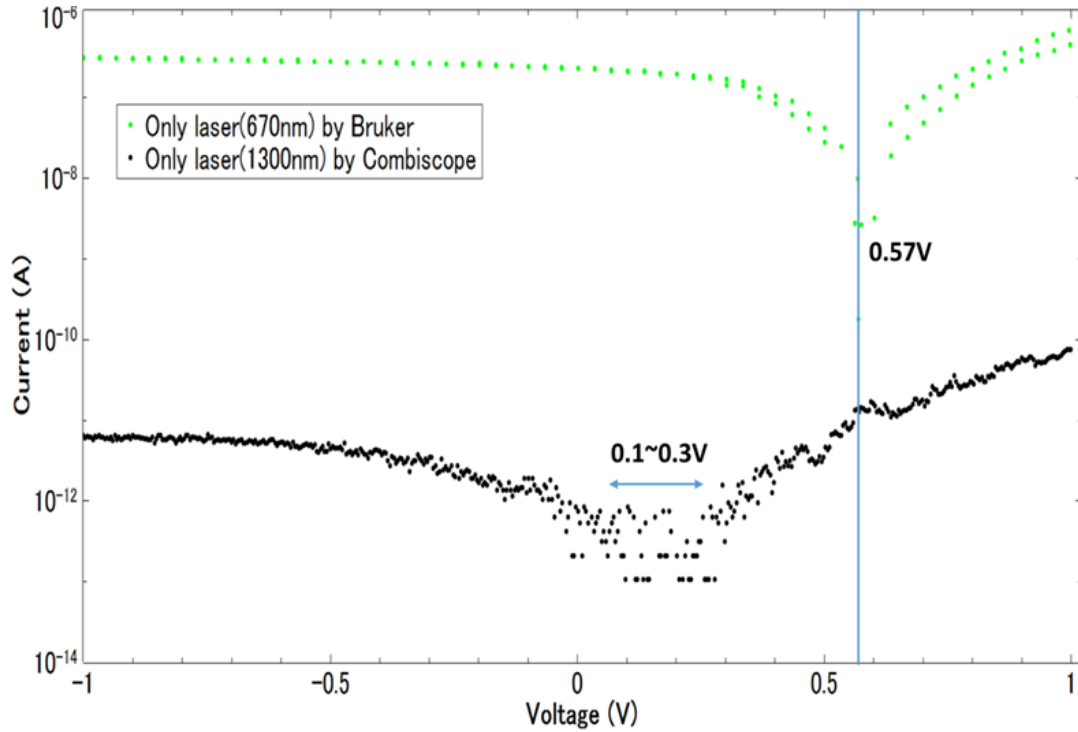


Fig.5.30: I-V curves measured on sample 2N-800 nm using Combiscope AFM (black curve), and Bruker AFM (green curve).

The V_{oc} of 0.57 V that is observed using the Bruker AFM setup decreases to around 0.1-0.3 V by using the Combiscope AFM setup. This observation again confirms that the V_{oc} observed for our samples is due to a photovoltaic effect driven by the red laser, and measured only for the nanosized solar cells formed in the holes.

[Device Comparison] Table 5.1 summarizes the hole dimensions measured for each of the three samples using the SEM images, both before the diffusion and after the diffusion/oxide removal. It also shows the hole dimensions as measured by CP-AFM after the diffusion/oxide removal and after an additional HF dip.

Table 5.2 summarizes (for all three samples, both before and after HF dip) the resistance measurements, substrate doping, and the V_{oc} and I_{sc} extracted from the I-V curves. J_{sc} is then calculated by dividing I_{sc} with the area measured by the CP-AFM after the HF step (shown in table 5.1).

| | Hole diameter before diffusion by SEM (nm) | Hole diameter after diffusion and oxide removal by SEM (nm) | Hole diameter after diffusion and oxide removal by CP-AFM (nm) | Hole diameter after diffusion and oxide removal by CP-AFM after HF (nm) |
|------------------|--|---|--|---|
| 1N-600 nm | 220±30 | 225±30 | 420±30 (including halo) | 230±30 |
| | | | 230±30 (excluding halo) | |
| 1N-800 nm | 260±20 | 350±20 | 635±40 (including halo) | 560±50 |
| | | | 350±25 (excluding halo) | |
| 2N-800 nm | 340 ± 20 | 235±30 | 485 ±60 (including halo) | 390±45 |
| | | | 250 ±45 (excluding halo) | |

Table 5.1: Summary of holes diameter in oxide for samples 1N-600 nm, 1N-800 nm and 2N-800 nm, before diffusion (measured using SEM images), holes diameter in Si substrate after diffusion and oxide removal (measured using SEM and CP-AFM images (before and after HF)).

| | Substrate doping (cm ⁻³) | R inside hole Before HF (Ohms) | R inside hole After HF (Ohms) | R outside hole Before HF (Ohms) | R outside hole After HF (Ohms) | V _{oc} (Volts) | I _{sc} (mA) | J _{sc} (mA/cm ²) |
|------------------|--------------------------------------|--------------------------------|--------------------------------------|---------------------------------|---------------------------------------|-------------------------|----------------------|---------------------------------------|
| 1N-600 nm | 5×10 ¹⁵ | 5×10 ⁶ | 6×10 ⁶ -2×10 ⁷ | 2×10 ⁸ | 5×10 ⁹ -4×10 ¹⁰ | 0.6 | 9×10 ⁻⁵ | 2×10 ⁵ |
| 1N-800 nm | 5×10 ¹⁵ | 4×10 ⁷ | 1×10 ⁷ | 3×10 ⁸ | 6×10 ⁷ | 0.54 | 8×10 ⁻⁵ | 3×10 ⁴ |
| 2N-800 nm | 2×10 ¹⁵ | 2×10 ⁷ | 1×10 ⁸ | 2×10 ⁸ | (Contamination on the sample) | 0.57 | 2×10 ⁻⁴ | 2×10 ⁵ |

Table 5.2: Summary of initial doping of samples 1N-600 nm, 1N-800 nm and 2N-800 nm, mean value of samples resistance under an applied voltage of +1 V inside and outside holes (before and after HF dip), and V_{oc} and J_{sc} under laser illumination measured from I-V measurements.

From table 5.1, it can be seen that the "electrical" hole diameter in SiO₂ for samples 1N-600 nm and 1N-800 nm (measured by SEM) becomes greater in the Si after diffusion and oxide removal. Furthermore, the increase in diameter is greater for the sample with bigger holes in the oxide (1N-800 nm). This increase in diameter could be caused by the lateral diffusion of boron. However, the hole diameter of sample 2N-800 nm is less after diffusion and oxide removal. This could be attributed to the fact that a thicker mask could shadow the arrival of gas phase dopant atoms to the surface.

Localized doped nanocontacts in cSi

As we have previously shown, the devices formed should not be considered as resistances, but rather as p-n junctions, and only analyzed through I-V measurements. Table 5.2 shows that the V_{oc} observed due to the red laser photogeneration in silicon is similar for all three samples. It is 0.60 V, 0.54 V and 0.57 V for 1N-600 nm, 1N-800 nm and 2N-800 nm, respectively. As for the J_{sc} under laser illumination, it is 2×10^5 mA/cm², 3×10^4 mA/cm², and 2×10^5 mA/cm² for 1N-600 nm, 1N-800 nm and 2N-800 nm, respectively. These enormous values (compared to one-sun illumination) are due both to collection from outside the hole area, as well as the extremely high laser power density.

In Fig.5.31, all the I-V curves shown in figs.5.19, 5.24 and 5.29 are plotted on the same graph (except for the I-V curves measured outside the holes for sample 2N-800 nm).

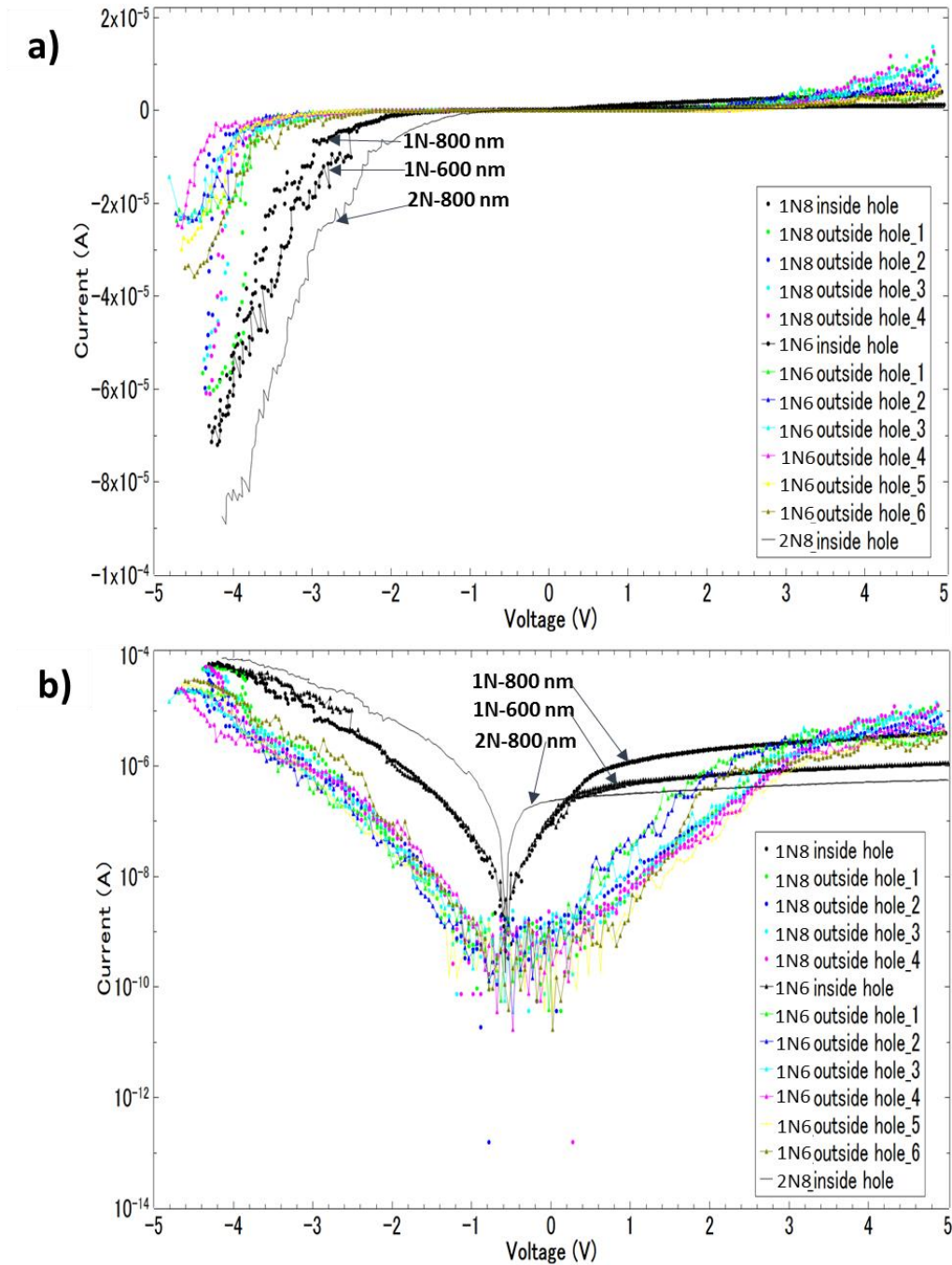


Fig.5.31: IV curves of samples 1N-600 nm (1N6), 1N-800 nm (1N8) and 2N-800 nm (2N8) in (a) linear scale and (b) log scale.

We can first compare the curves of samples 1N-600 nm and 1N-800 nm, which have the same initial doping concentration ($5 \times 10^{15} \text{ cm}^{-3}$) and the same initial thickness of the oxide masking layer (120 nm). For positive (reverse bias) voltages, the current is higher for sample 1N-800 nm compared to 1N-600 nm. This can be attributed to greater hole diameters (as observed from both SEM images and CP-AFM images).

Comparing the samples at negative voltages (forward bias), a higher value of reverse-saturation current (J_0) can be observed for the sample 2N-800 nm compared to the two other samples. This can be probably due

to the lower initial doping of $2 \times 10^{15} \text{ cm}^{-3}$ for the sample 2N-800 nm (compared to $5 \times 10^{15} \text{ cm}^{-3}$ for the other two). A lower doping implies a smaller barrier in the junction, thus a higher J_0 . However, as the J_0 is higher for the sample 2N-800 nm, its V_{oc} should be smaller compared to the two other samples. A smaller V_{oc} is observed for the sample 1N-800 nm, for unclear reasons. The measured values of V_{oc} may contain some errors due to the position of the laser spot on the cantilever. Furthermore, the values of V_{oc} given are far from one-sun, and are somewhat arbitrary in value.

5.1.1.4 Summary – Diffusion results

In this section, Approach B (using Al as a mask followed by oxide plasma etching through the Al holes), was used to form holes in 120 nm and 240 nm thermally grown oxide. Then, boron doping by diffusion was done through the oxide with nanoscale holes. This was followed by oxide removal and sample characterization by SEM and CP-AFM.

It was seen from the SEM images that a “dinner plate” shape is seen from the cross section images, and is caused by the etching of the boron glass layer. In addition, a significant contrast was seen in SEM images using top and side view of the boron doped parts by the SE(U) detector.

Using CPAFM measurements, a higher conductivity was seen inside the holes compared to outside, with a resistive halo observed around the holes. This halo is most probably related to a topographical feature, as its width decreased after an HF dip. By doing local I-V measurements, solar cell behavior was observed inside the holes with a V_{oc} caused by the photogeneration by the red AFM laser. To prove this assumption, it was shown that the V_{oc} was almost completely eliminated through the use of an infrared laser. This observation confirms that a solar cell is formed inside the holes, thus a successful local boron doping in the nanoscale range.

In the next section of this chapter, ion implantation will be used instead of diffusion to dop through the holes.

5.1.2 Doping by ion implantation through nanoholes

One of the major disadvantages of doping by thermal diffusion is the isotropic nature of the diffusion process. This is underlined in Fig.5.2, which compares the profiles that result from doping both by diffusion and ion implantation.

When the unmasked doped areas are spaced close to each other, the lateral diffusion between two adjacent regions could overlap and diminish the effect of local doping. As the size of the contacts we are using in this work is in the order of hundreds of nanometers (as is the distance between them), this could become a limitation. Ion implantation is an alternative doping technique that could help overcome this limitation, and reduce the steps needed to form doped regions.

5.1.2.1 Overview and Description of Ion Implantation Process

During the ion implantation process, ions are directed towards the sample with a given energy. At the sample surface, ions can be back-scattered or stopped in the Si matrix by losing this energy via two phenomena; nuclear stopping (involving energy transfer to matrix atoms) and electronic stopping (related to interactions with electrons). However, the latter process does not displace semiconductor atoms from their lattice positions. Nuclear transitions can transfer sufficient energy to the lattice resulting in implant damage. If the ion energy is above the binding energy of matrix atoms (15 eV for Si-Si bonds in c-Si), then matrix atoms can be displaced. Depending on the ion energy and the surface atom density, species can also be expelled from the matrix, resulting in a surface etch.

Displaced matrix atoms can cause cascades of secondary displacements of nearby atoms to form a tree of disorder along the ion path. This tree of disorder is different when light or heavy ions are being implanted. For instance, electronic collisions are mostly responsible for energy loss for light ions, such as boron when implanted in silicon. The ions lose their energies as they penetrate deeper into the substrate. When the ion energy is reduced below the crossover energy (10 keV for boron), nuclear stopping becomes dominant and lattice damage can occur, therefore most of the lattice disorder occurs near the final ion position as presented in Fig.5.32.a. For heavy ion implantation (for instance Arsenic (As)) the energy loss is primarily due to nuclear collisions, therefore the resulting lattice disorder originates close to the sample surface as seen in Fig.5.32.b [4].

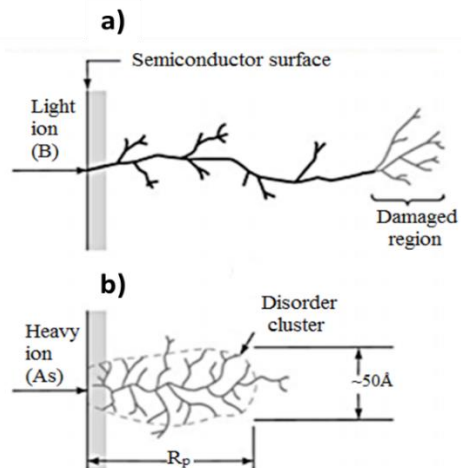


Fig.5.32: Implantation disorder caused by (a) light ions and (b) heavy ions [4].

Because of these damaged regions and the disorder clusters that result from ion implantation, semiconductor parameters such as mobility and lifetime are degraded. The term “damage” is used because atomic displacement leads to point defects, i.e. the creation of self-interstitial Si_{Si} and Si vacancies V_{Si} (called Frenkel pairs). However, most of the Frenkel pairs recombine instantaneously and only a small fraction of them remains. After the implantation step, most of the dopant atoms are located at random positions in the c-Si network and are not electronically active.

[Dopant Activation through Annealing] The implanted atoms should be “activated” (i.e. moved in substitutional position) to perform their electrical functions of doping. Some dislodged silicon atoms at interstitial sites also have to be returned to their lattice positions. Therefore, it is required to reconstruct the c-Si crystalline structure and move dopant species into substitutional positions to allow the release of free carriers. To achieve these two functions, a large amount of energy is required in order to allow atoms to diffuse. This is achieved through an activation annealing step. However, only a limited amount of dopant atoms can be “activated”. The threshold is called the solubility limit $C_{\text{Sol}}^{\text{limit}}$. This factor in Si varies as a function of the dopant used and temperature. Its variation as a function of temperature is represented by table.5.3 and Fig.5.33 for the dopants usually used in Si [247].

| Dopant | $C_{\text{Sol}}^{\text{limit}} [\text{cm}^{-3}]$ | Ref. |
|--------|---|-------|
| B | $9.2 \times 10^{22} \exp\left(-\frac{0.73 \text{ eV}}{kT}\right)$ | [248] |
| As | $1.3 \times 10^{23} \exp\left(-\frac{0.42 \text{ eV}}{kT}\right)$ | [249] |
| P | $2.5 \times 10^{23} \exp\left(-\frac{0.62 \text{ eV}}{kT}\right)$ | [250] |

Table.5.3: Solubility limit equations for B, As, and P species [251].

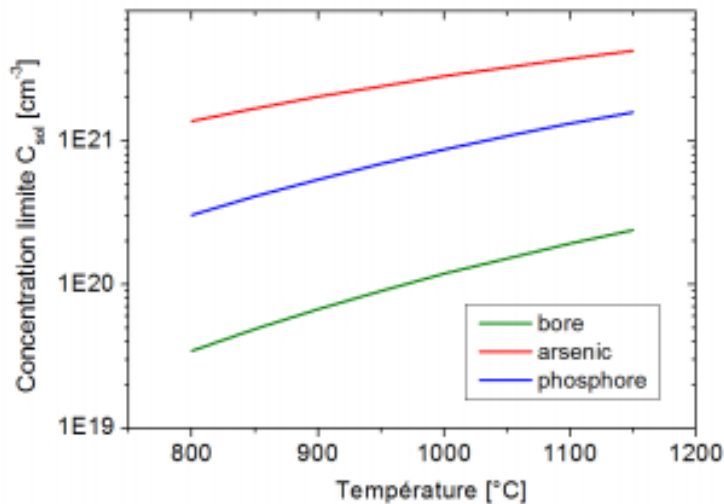


Fig.5.33: Solubility limit of B, As, and P between 800 and 1200 °C [251].

Any concentration of B and P above the solubility limit leads to species precipitation during the annealing step.

The high temperatures required for dopant activation also results in the diffusion of species. Therefore, the as-implanted depth profile of dopants has its maximum concentration peak decreased and lies more deeply in the substrate after annealing.

Thermal annealing allows point defects to recover, and it also allows them to aggregate to form persistent extended defects as self-interstitial aggregates, {133} defects (i.e. planar chain of Si_{Si}) and dislocation rings [251].

The annealing temperature should be high enough to cause diffusion of the atoms from their interstitial positions into lattice positions. As one of the key benefits of implantation (compared to thermal diffusion) is the tight spatial distribution of the implanted atoms, introducing a long anneal in a furnace which produce significant thermal diffusion of the implanted profiles, would defeat this advantage.

To limit dopant diffusion, rapid thermal annealing (RTA) can be used as an annealing method. The wafer is heated quickly to a temperature ranging from 600 °C to 1100 °C during brief duration ranging from several minutes to few seconds. RTA is performed by placing the wafer on a quartz tray designed to have a very low thermal conductivity and thermal mass, and illuminating both with high-intensity halogen lamps. The low thermal mass of the wafer combined with the high incident radiation allows the wafer to rapidly heat up, usually at rates close to 100-200 °C/s. A pyrometer or a thermocouple is used to measure the wafer temperature and adjust the lamp intensity to maintain the desired temperature profile.

The RTA used during this thesis is a halogen oven from AET technologies⁸, where the annealing was performed under reduced pressure (pumping till 10⁻¹ mbar before introducing the flow) with 5 sccm of argon-hydrogen flow. The ramp up rate is around 10 °C/s under an argon-hydrogen flow and the ramp down rate is between 1-2 °C/s under N₂ ambient.

The success of annealing is often assessed by the fraction of dopant that is electrically active, as found experimentally using the Hall Effect technique or the ECV measurement. The annealing characteristics depend on the dopant type and the dose implanted. Seidel's results indicate that boron will reach 100 % activation at temperatures as low as 800 °C if annealed for a long enough time. As for the annealing time, he have shown that the time for a complete anneal increases with increasing ion dose [252]. Mokhberi et al. have studied dopant activation in silicon by doing the rapid thermal annealing in the temperature range of 900 °C-1050 °C. As the 4.7 eV activation energy of boron electrical activation is greater than its 3.46 eV activation energy for diffusion, he suggests that it is beneficial to use a higher-temperature and shorter-time anneal in order to maximize activation and minimize diffusion [253].

To further suppress dopant diffusion by annealing at lower temperatures, the Si should be amorphized prior to the dopants implantation. Csepregi et al., reported on the recrystallization of silicon amorphous layers implanted with P, As, and B ions in the 400°C - 600°C range by solid phase epitaxy (SPE) [254]. Tsai et al. also reported that B⁺ ions could be activated at the low temperature region around 550°C by forming an amorphous layer with Si⁺ implantation [255][256].

In this work, the samples were annealed in the AET-zirst RTA at 800°C, 900°C , and 1000°C during 5 minutes after boron implantation.

[Masking Materials] Another advantage of doping by ion implantation is the flexibility to use a variety of masking materials when doing a selective doping. As ion implantation can be done at room temperature, it becomes possible to use masking layers that are sensitive to temperature, such as photoresist. Other films

⁸ Located at “Centre de Nanosciences et Nanotechnologies” (C2N)

such as SiO_2 , Si_3N_4 , can also be used, as well as metals. Unlike in doping by diffusion, masking materials do not generally act as a barrier, but instead they act as a sacrificial absorber. Therefore, the selectivity between the masking material and the substrate is not large. To act as an effective mask, the film thickness just has to be greater than the penetration depth of the dopants in the substrate. In general, this is not a limitation as the implant depths of the dopants by ion implantation are usually not more than few hundred nanometers [4].

A thin dielectric layer could be as well used to move the peak location of the doping profile closer toward the sample surface. **In our work, thermally grown oxide was used as the masking layer similarly to the case of doping by diffusion previously presented in this chapter.**

[Channeling effect] An effect known as channeling occurs when implanting ions into certain orientations of crystalline substrates. The stopping power of the substrate depends on the ions randomly colliding with the substrate atoms. If the ions are incident along one of the crystal axes where all the atoms line up one behind the other, it is probable that the ions will avoid these atoms and travel between them through the voids, thus the stopping range of the ions becomes large and unpredictable. This effect is illustrated in Fig.5.34, which also present the two ways usually used to overcome it [4].

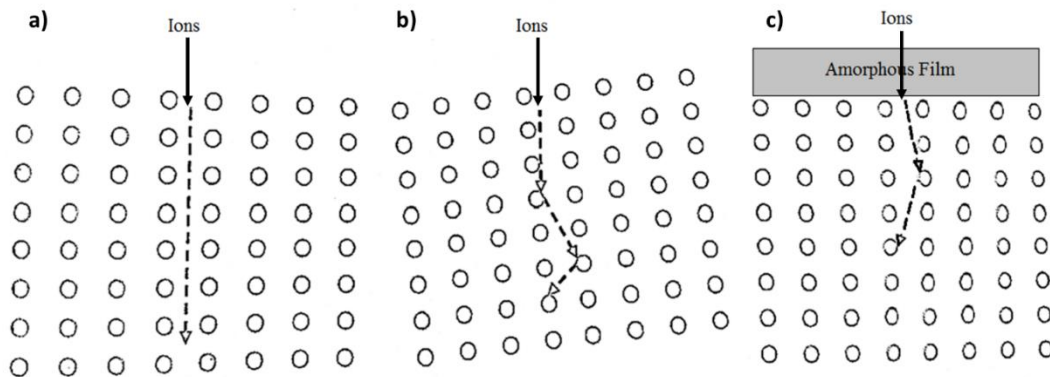


Fig.5.34: Ion channeling effect and techniques used to mitigate it: (a) ion channeling through crystal voids, (b) tilted substrate to avoid channeling, and (c) a thin film used to disperse incident ions [4].

The first way to overcome the channeling problem is presented in Fig.5.34.b and it consists of tilting the substrate during implantation. This will ensure that none of the crystal voids line up and allow channels to appear. The second way to overcome this problem is presented in Fig.5.34.c and it consists of using an amorphous film in order to introduce a very small but random angular deviation to the arriving ions.

In this work, we tilted the sample by 7° to mitigate the channeling effect.

5.1.2.2 Experimental description

A part of sample 1N-600 nm (a piece of the same sample that was doped by diffusion in part 5.1.1.2) was also doped by boron implantation. TCAD simulation was again used to check if the masking oxide layer of 120 nm can block the boron implanted at 10 keV and 20 keV with a dose of 8×10^{13} at/cm² and 1.5×10^{14} at/cm², respectively.

This simulation was done for both the cases with and without the oxide. Figure 5.35 presents both cases and for implantation energies of 10 keV and 20 keV.

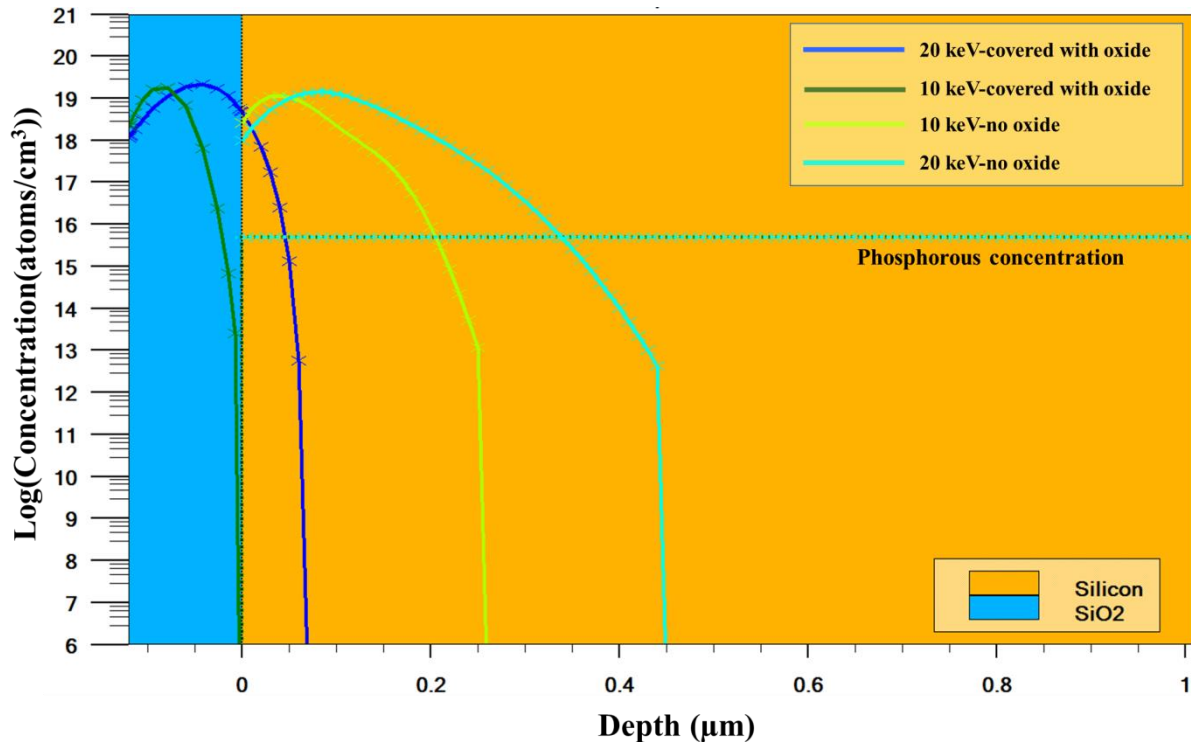


Fig.5.35: Simulated boron concentration (log scale) in samples (1N-600 nm) implanted at 10 keV and 20 keV as a function of sample depth. Dark blue and dark green curves correspond to doping profile through 120 nm SiO₂, and light green and cyan curves correspond to doping profile through holes.

It can be seen from Fig.5.35 (without a masking oxide) that the junction depths are around 200 nm and 340 nm for boron implanted at 10 keV and 20 keV, respectively. For the profile deposited through 120 nm thick masking oxide, we can predict that an efficient masking for the implanted boron occurs at 10 keV. However, insufficient masking would probably occur when the boron is implanted at 20 keV.

After performing the experimental procedure described above, the oxide mask was then completely etched before performing an RTA annealing at 800°C, 900°C, and 1000°C for 5 minutes. The oxide was removed prior to annealing to prevent the boron implanted in the oxide to further diffuse into the Si during the annealing. In the next part of this chapter, the implanted samples will be characterized after oxide removal, using SEM, CPAFM and ECV measurements. SEM will characterize the samples implanted at 10 keV and 20 keV, whereas CPAFM and ECV will be only characterizing the samples implanted at 10 keV.

5.1.2.3 Characterization by SEM and CP-AFM

5.1.2.3.1 Characterization by SEM

The SEM images of the sample implanted at 10 keV and 20 keV before and after annealing (after oxide removal) are shown in Fig.5.36 by using the SE (U) detector (detecting pure secondary electrons (SE)) at a beam voltage of 1 and 2 kV, as earlier used in this chapter to detect boron doping by diffusion.

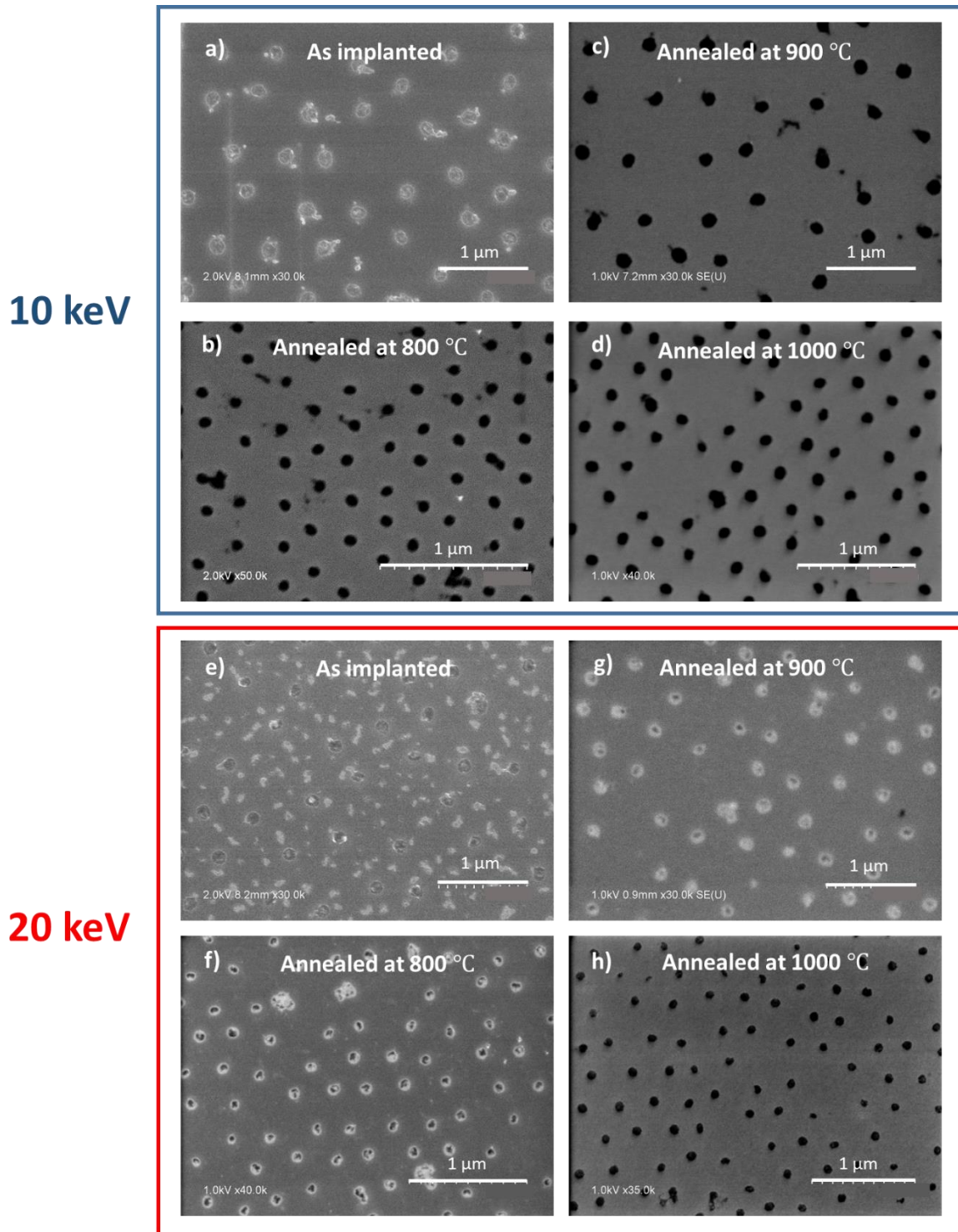


Fig.5.36: SEM images of 1N-600 nm after 10 keV and 20 keV boron implantation (a), (e) as implanted, annealed at (b), (f) 800 °C, (c), (g) 900 °C and (d), (h) 1000 °C.

The holes appear bright for the as implanted case and become black after an annealing at 800 °C for the samples implanted at 10 keV. When the boron is implanted at 20 keV, the holes are not well defined, with

white residues in between them for the as-implanted case and they become black after an annealing at 1000 °C.

One might expect that boron is activated in the samples annealed at high temperature, and therefore a brighter color should be seen in the SEM images when the SE(U) detector is used (as was already seen for the sample locally doped by diffusion). However, in Fig.5.36, a bright color appears for the as implanted samples and a darker one for the implanted one. Due to this observation, one can expect that the bright color in this case is probably not related to the boron activation, but to some features inside the holes or to damages caused by ion implantation.

Comparing the hole diameters for the samples annealed at 1000 °C after implantation at 10 keV and 20 keV, 100 ± 8 nm is observed for the sample implanted at 10 keV (Fig.5.36.d) and 84 ± 8 nm for the one implanted at 20 keV (Fig.5.36.h). Smaller hole diameters are then observed for the samples implanted at higher energy. Note that these "holes" are in fact leftover effects on the c-Si surface after the masking oxide is removed.

We expect to have physical holes in the Si substrate of ~5 nm depth caused by the plasma etching step of approach B (Ch.4) during which the oxide is locally etched through the Al masking.

The same steps were done on another n-type sample "3N- 600 nm" with an initial phosphorous concentration of 4.06×10^{15} cm⁻³, and having a thicker masking oxide of 240 nm, where the holes are formed using 600 nm NPs. The initial sample with the oxide layer and the holes before ion implantation is shown in Fig.4.21.a which have shown an initial diameter of 370 ± 30 nm and an opening fraction of 29 %. The SEM images of the samples implanted at 10 keV and 20 keV after an annealing at 800 °C, 900 °C and 1000 °C are shown in Fig.5.37.

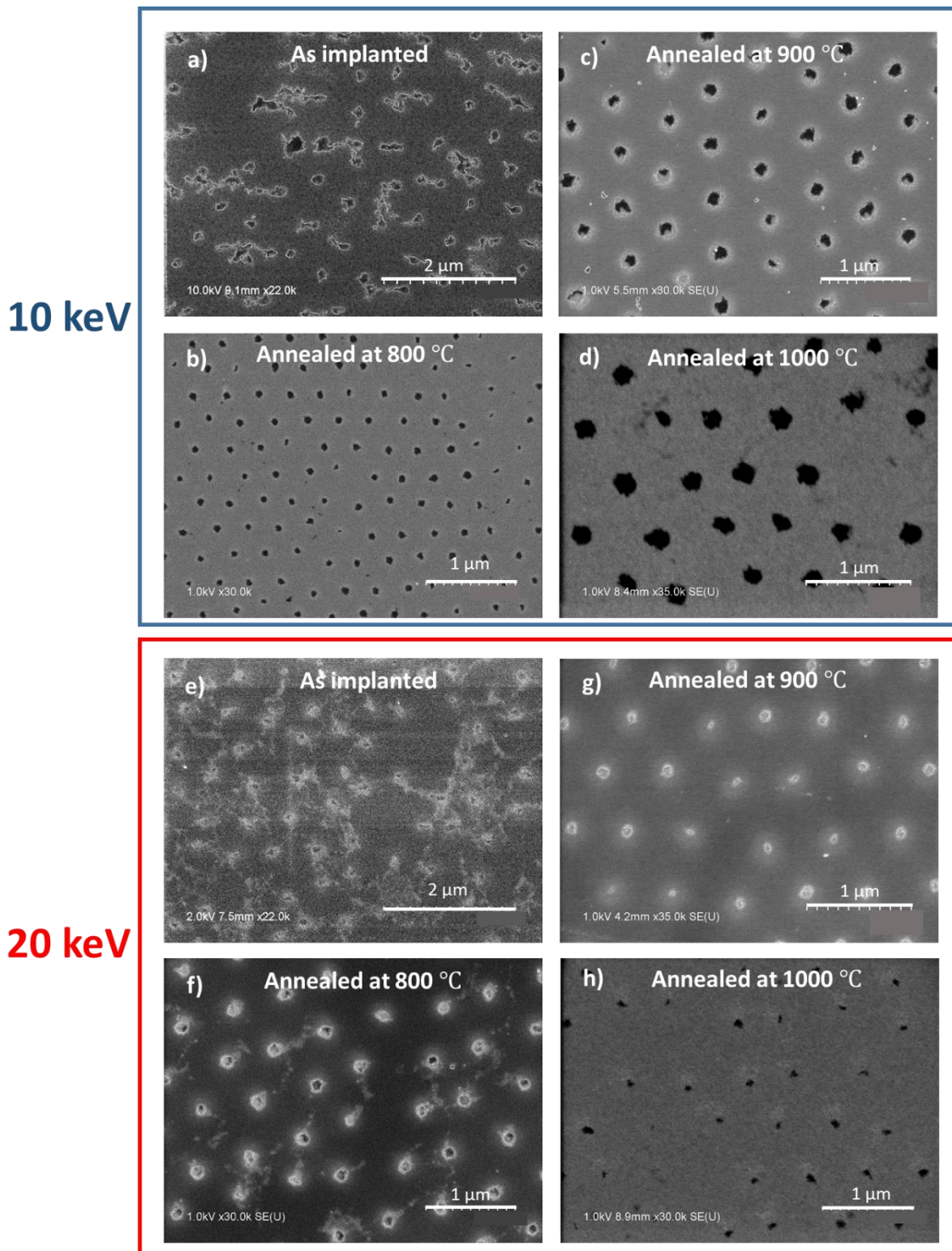


Fig.5.37: SEM images of 3N-600 nm⁹ after 10 keV and 20 keV boron implantation (a), (e) as implanted, annealed at (b), (f) 800 °C, (c), (g) 900 °C and (d), (h) 1000 °C.

⁹ Having a thicker masking oxide of 240 nm.

It can be seen in Fig.5.37 that for the samples implanted at 10 keV, the holes become black and the white features are gone after an annealing at 800 °C, whereas, for the samples implanted at 20 keV, the holes become black after an annealing at 1000 °C. By comparing the holes diameter observed after an annealing at 1000 °C, it can be seen that $192 \pm 20 \text{ nm}$ is observed for the sample implanted at 10 keV (Fig.5.37.d), whereas $118 \pm 16 \text{ nm}$ is observed for the sample implanted at 20 keV (Fig.5.37.h). Smaller hole diameters are observed for the samples implanted at 20 keV compared to those implanted at 10 keV, which is similar to the observation seen for sample 1N-600 nm in Fig.5.36.

5.1.2.3.2 Characterization by CP-AFM

The CP-AFM measurements in this part was mainly focused on the samples “1N-600 nm” and “3N-600 nm” implanted at 10 keV. It was previously predicted from the TCAD simulation shown in Fig.5.35 that 120 nm masking oxide used for 1N-600 nm could mask the boron implanted at 10 keV, therefore a thicker mask of 240 nm used for 3N-600 nm would be expected to mask the same implantation.

[CPAFM-1N-600 as-implanted] CP-AFM measurements were first done on 1N-600 nm implanted at 10 keV and which SEM images were shown in Fig.5.36. The CP-AFM measurements of the sample as implanted done at +2 V are shown in Fig.5.38 before and after an HF dip of 30 s.

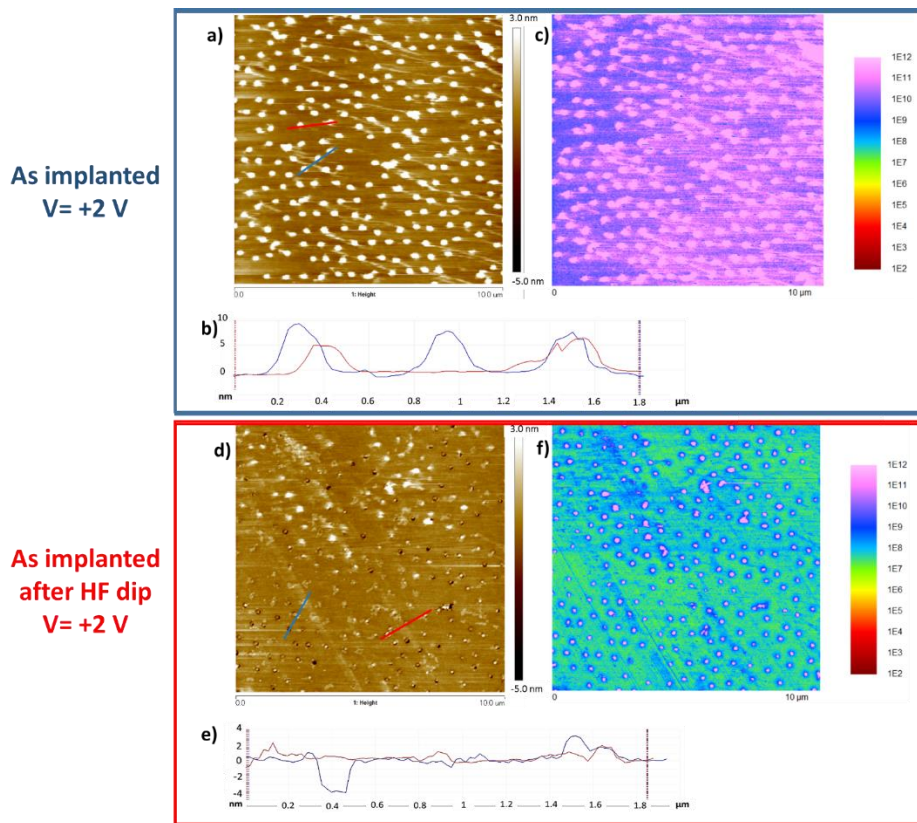


Fig.5.38: (a) Topography image of sample 1N-600 nm and (d) that after HF dip, (b) and (e) topography profile corresponding to blue and red lines selected in (a) and (d), respectively. (c) Local resistance mapping of sample 1N-600 nm while applying a bias of +2 V, and (f) that after HF dip.

From the topography image of sample 1N-600 nm, it can be seen that there are some bumps on the sample surface with a height between 7 and 10 nm. This is in correlation with the features seen on the SEM image

of Fig.5.36.a. These bumps are reduced in number after the HF dip (Fig.5.38.d) and some holes are seen, the resistance inside the holes remains similar to that before the HF dip (pink color). The resistance outside the holes becomes smaller after HF dip compared to that before HF dip; however this resistance remains in both cases smaller than that inside the holes.

Having different resistances inside the holes for the samples measured at both +2 V and -2 V could be an indication that the doped holes are not acting as a simple resistance and that a diode behavior could be seen. Therefore, the sample shown in Fig.5.38 is again measured at -2 V and the resistance mapping measurements are presented in Fig.5.39 before and after HF dip.

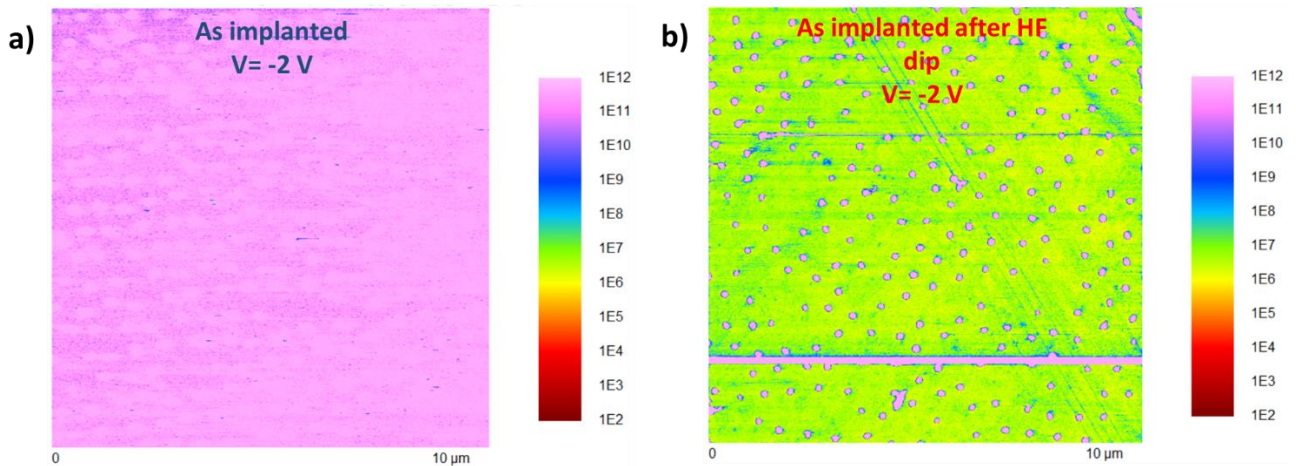


Fig.5.39: Local resistance mapping of sample 1N-600 nm while applying a bias of -2 V (a) before HF dip and (b) after HF dip.

Similar observations are seen in this measurement (when applying -2 V) compared to Fig.5.38 where +2 V is applied. However in this case the holes were not seen clearly before HF probably because of a thicker oxide inside the holes (Fig.5.39.a).

In summary, the holes appear resistive by applying both + 2V and -2 V (Fig.5.38.f, and Fig.5.39.b). This is probably because the parts of the sample that were exposed to boron implantation are amorphized and an annealing is needed to recrystallize them.

[CPAFM-1N-600-annealed at 800°C] CP-AFM measurements were also done on the same samples annealed at 800 °C at +2 V and -2 V before and after HF. The corresponding measurements are seen in Fig.5.40.

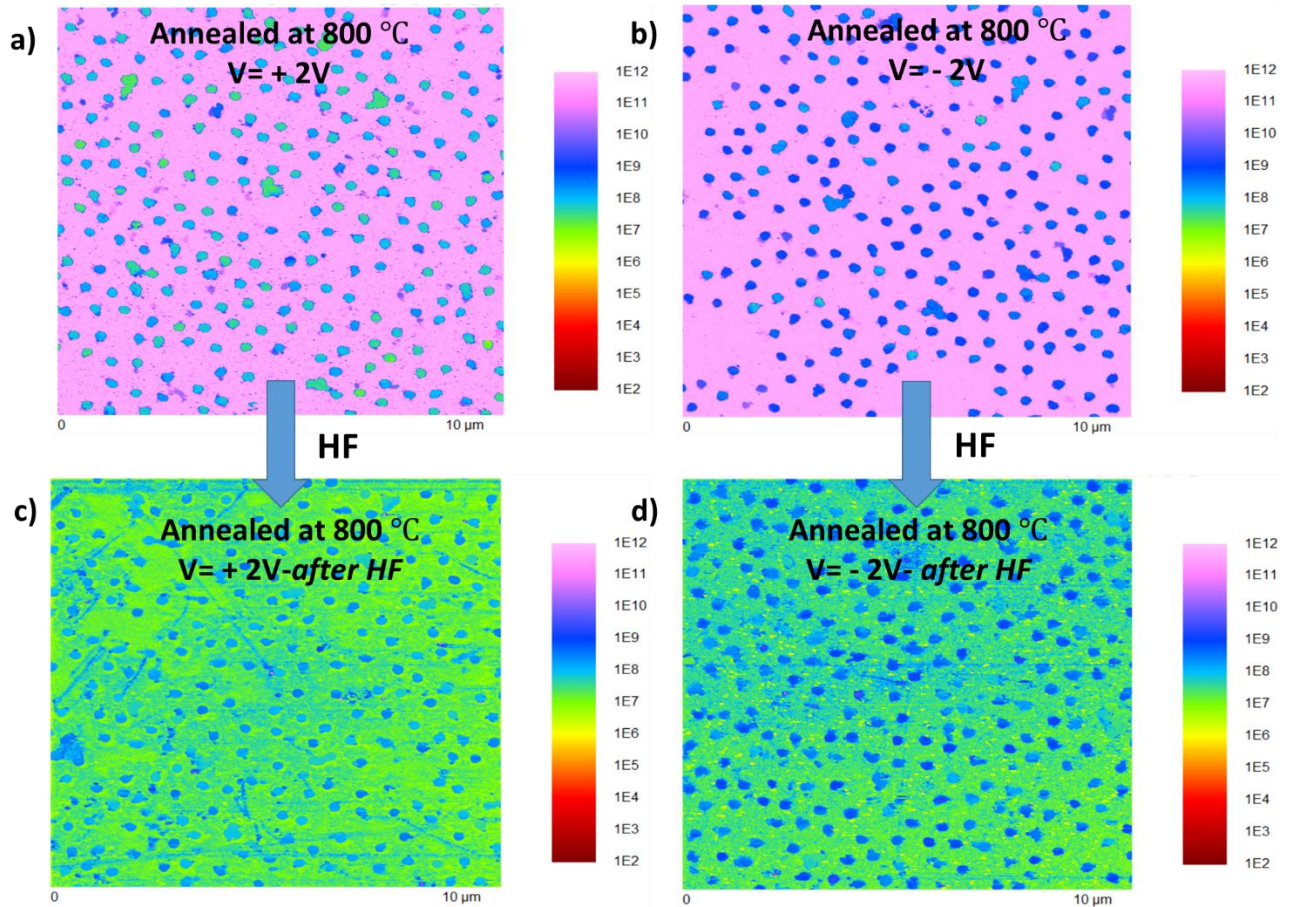


Fig.5.40: Local resistance mapping of sample 1N-600 nm annealed at 800 °C while applying a bias of (a) +2 V, (b) -2 V, and that after HF dip at a bias of (c) +2 V and (d) -2 V.

Before HF dip, the holes appear more conductive than the surrounding area both when +2 V or -2 V is applied. However the resistance inside the holes is slightly higher at -2 V (Fig.5.40.b) than at +2 V (Fig.5.40.a).

After HF dip, the resistance of the area inside the holes changes little. However, the area outside the holes becomes conductive and even more conductive than the part inside the holes. This increase in conductivity for the outside part was as well seen for the as implanted sample in Fig.5.38 and Fig.5.39. One is tempted to attribute this increase in conductivity by the HF dip to the removal of a remaining oxide layer from the mask on the sample surface. However, it was confirmed by an ellipsometry measurement that there is no oxide remaining on the surface from the masking layer. As this increase in conductivity was just seen for the outside part and didn't affect the holes, we can't relate it just to the native oxide etching. Therefore it is most probable to be due to some HF passivation effect on the cSi surface [257][258][259].

However, as seen previously, such surfaces cannot be fully understood by simply examining resistance mapping, as they consist of non-linear devices. I-V curves must be used to truly understand what is occurring.

[I-V curves] Local I-V measurements were done on this sample both inside and outside the holes, after HF dip. These measurements are shown in Fig.5.41.

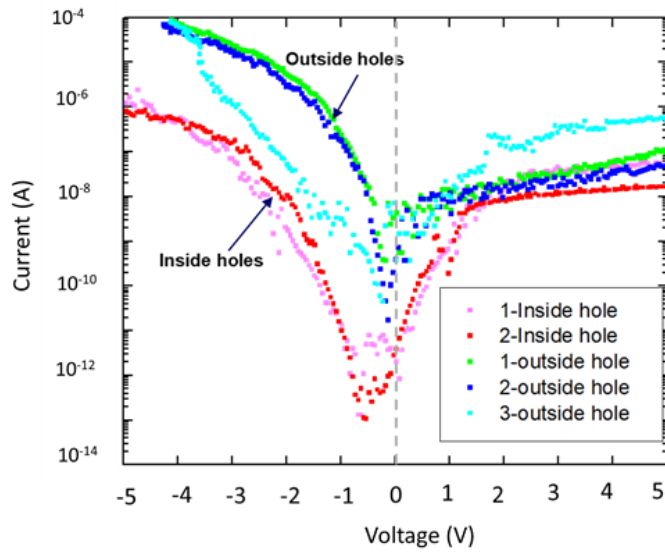


Fig.5.41: Logarithmic IV curves of samples 1N-600 nm inside and outside holes after HF dip.

Both curves measured inside and outside the holes have a diode shape. A V_{oc} of around 0.5 V is observed inside the holes and around -0.1 V outside the holes, confirming that a photodiode is only formed inside the holes. One can notice that outside the holes, the three plotted curves have similar V_{oc} , but the cyan curve is coherent with the CP-AFM measurements (Fig.5.40) where we observe a similar resistivity at both -2 V and +2 V. One can also note a very low or non-existent value of J_{SC} , indicating extremely poor collection by these nanoscale PV devices.

[Shifting laser position for I-V measurement] To further study the occurrence of a V_{oc} inside the holes, the I-V curves were repeated after shifting the laser position from its regular one (focused on the tip) toward the back of the tip, as shown in Fig.5.42. This is done to confirm if there is photogeneration by the red laser. The corresponding I-V curves are presented in Fig.5.43.

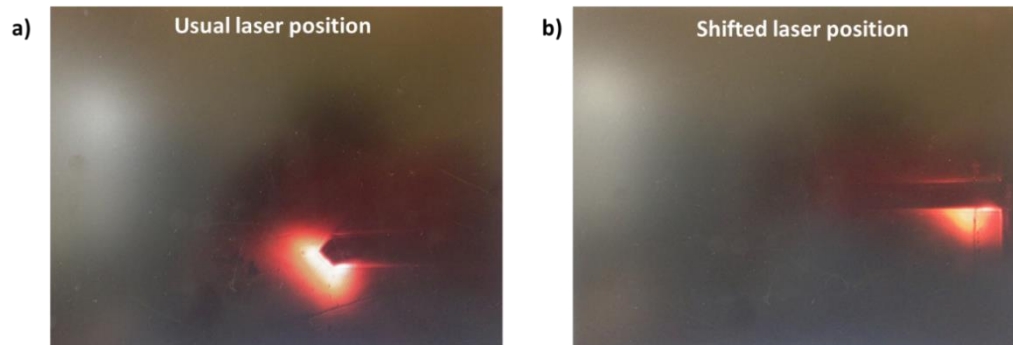


Fig.5.42: (a) regular laser position, (b) modified laser position.

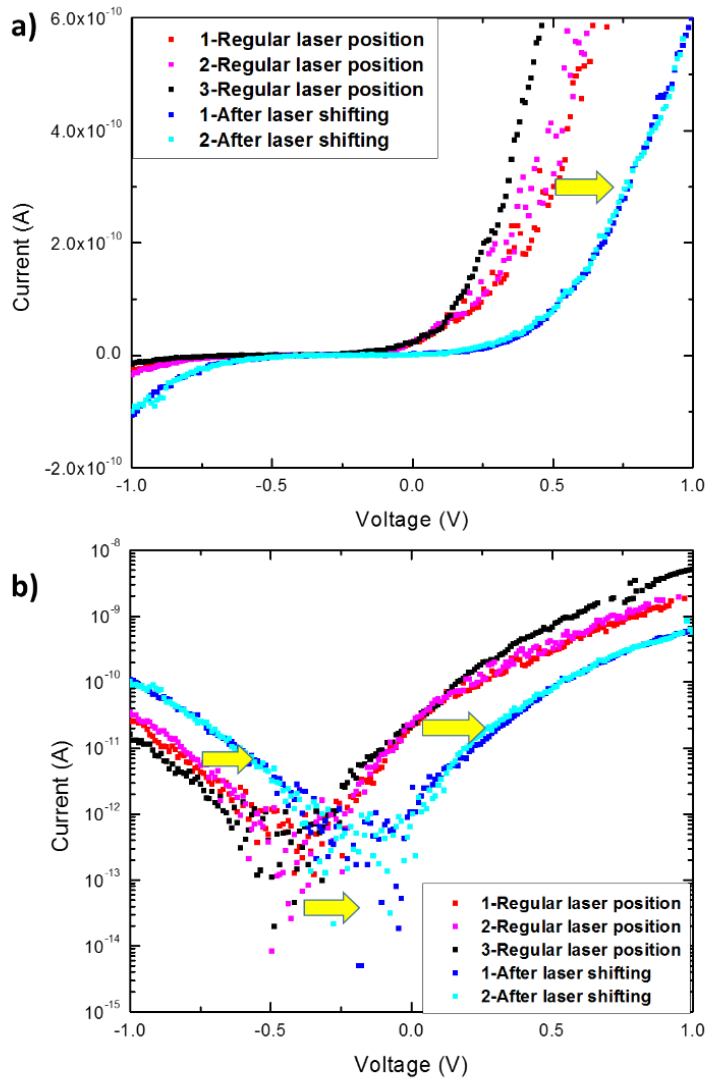


Fig.5.43: I-V curves of sample 1N-600 nm measured inside holes with red laser focused in two different positions (Fig.5.42) in (a) linear scale and (b) logarithmic scale.

Fig.5.43 confirms that the V_{oc} decreases when shifting the laser position. The difference measured in V_{oc} before and after shifting the laser is around 0.3 V. A value of J_{sc} of 41.6 mA/cm^2 was measured when the laser was in its usual position, and it decreased to 2.5 mA/cm^2 after shifting the laser. Thus a difference in J_{sc} of around 39 mA/cm^2 .

Although these measurements confirm that a photodiode is formed inside the holes, one should note the extremely low J_{sc} measured compared to the diffused junction case. This indicates that although a nanoscale photovoltaic device is indeed formed, recombination and/or resistive losses reduce the photocurrent to almost nil.

[Comparing 1N-600 nm and 3N-600 nm annealed at 800 °C] CP-AFM measurements were done on sample 3N-600 nm implanted at 10 keV after HF treatment and compared at the same scale to 1N-600 nm (already shown in Fig.5.40). The difference between these two samples is therefore just the thickness of the

masking oxide, which is 120 nm and 240 nm for 1N-600 nm and 3N-600 nm, respectively. The measurements are shown in Fig.5.44.

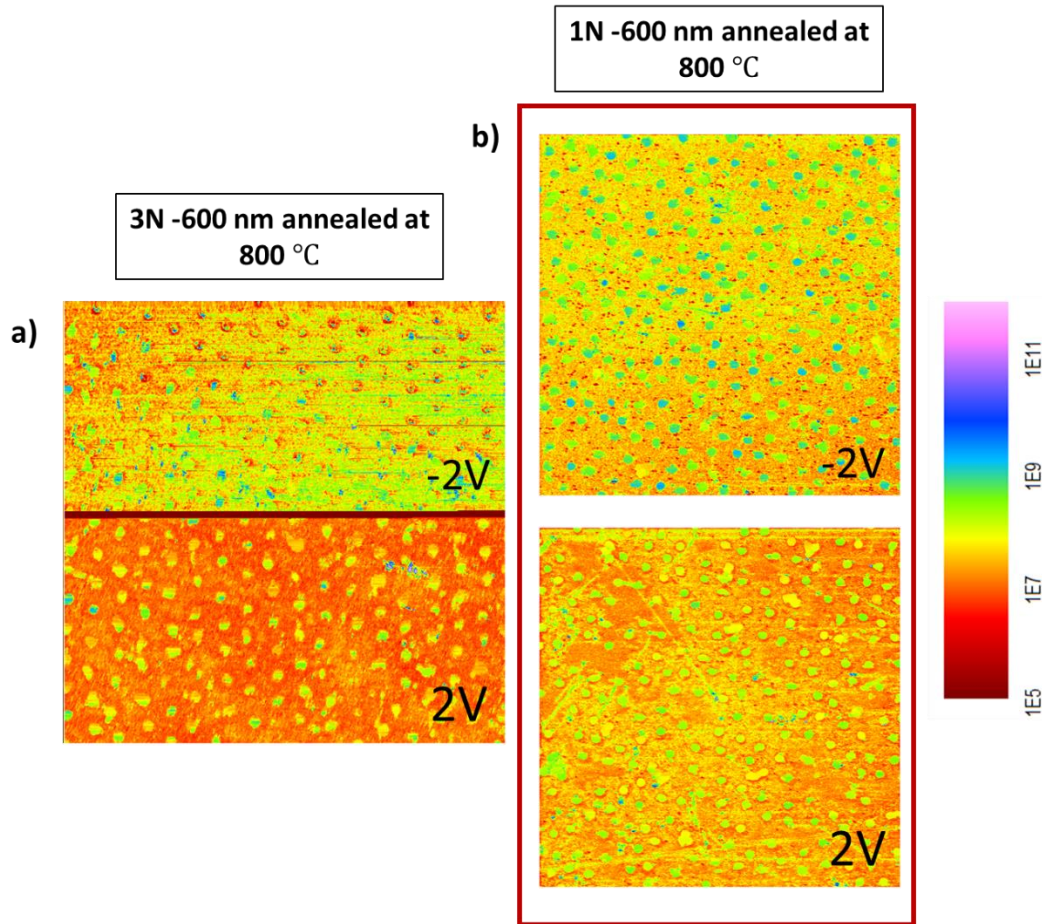


Fig.5.44: Local resistance mapping at the same scale of a) 3N-600 nm annealed at 800 °C done half at -2 V and half +2V and of b) 1N-600 nm annealed at 800 °C done at -2 V and +2 V.

Similar mappings are measured for both samples 1N-600 nm and 3N-600 nm, despite the very different masking oxide thickness used. For both samples, the area outside the holes is more conductive than that inside the holes, while the resistivity inside the holes is slightly higher at -2 V compared to +2 V.

[Shifting laser position] In order to check if there is a laser effect also during the scan of the CP-AFM measurement, the images shown in Fig.5.44.a (sample 3N-600 nm-annealed at 800 °C) were redone two days after the HF treatment on the same AFM setup but with the laser head moved 200 μm behind the AFM tip. These measurements are shown in Fig.5.45.

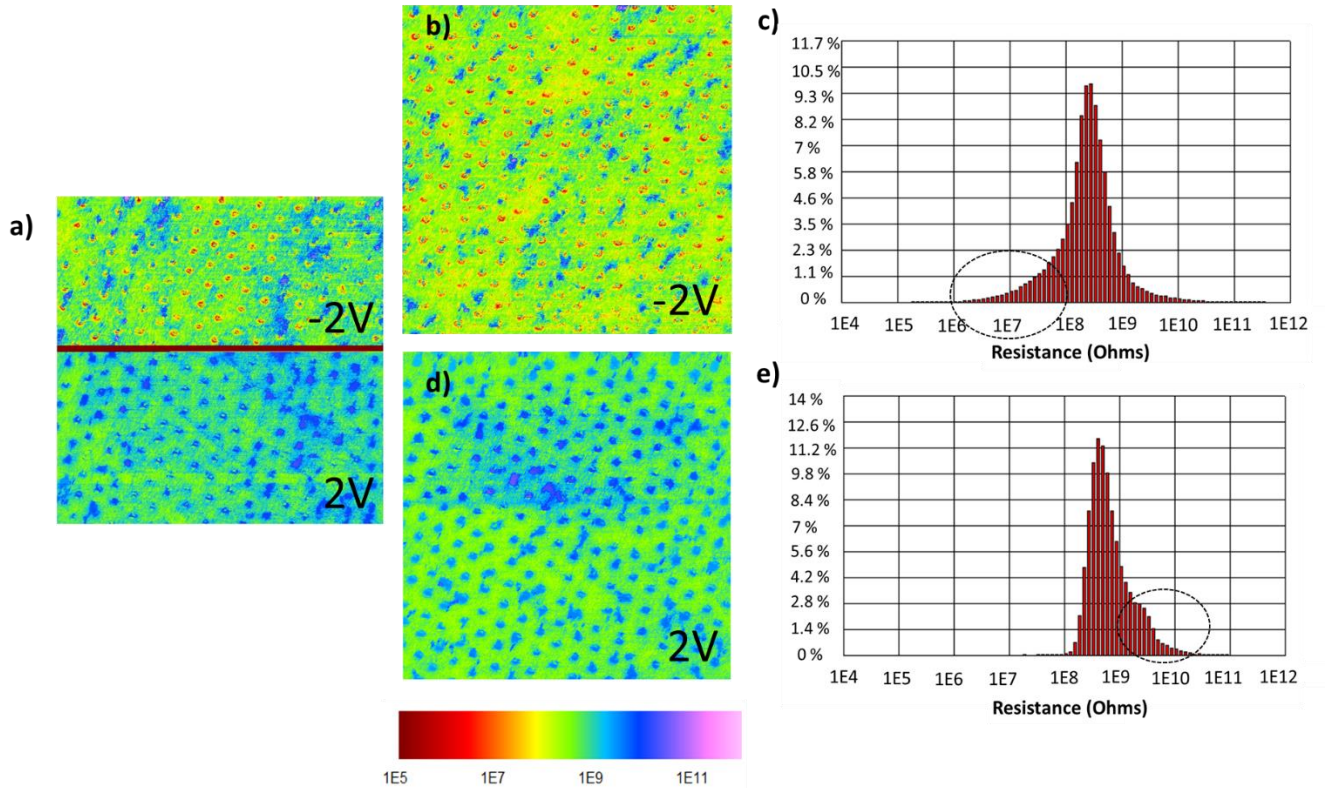


Fig.5.45: a) Local resistance mapping of 3N-600 nm annealed at 800 °C done half at -2 V and half at 2V, b) full scan done at -2 V and d) +2 V, c) and d) total resistance distribution of Fig.5.45.b and Fig.5.45.d, respectively.

In comparison with Fig.5.44, one can clearly see that inside the holes, the devices behave differently at forward and reverse bias (confirming the presence of a diode). Whereas the resistance of the part inside the holes (circled in Fig.5.45.c) decreased between 1 or 2 orders of magnitude when -2 V is applied. In contrast, an increase of around 2 orders of magnitude is observed in the holes (circled in Fig.5.45.e) when +2 V is applied. In Fig.5.44, similar behavior is observed at both forward and reverse bias, which unfortunately neither confirms nor disproves the presence of a diode under illumination.

[CPAFM using 1300 nm laser] To even further confirm the effect of the laser on the CPAFM measurement, it was repeated after few days using the Combiscope AFM (laser wavelength of 1300 nm). The images are shown in Fig.5.46 at -2 V and +2 V.

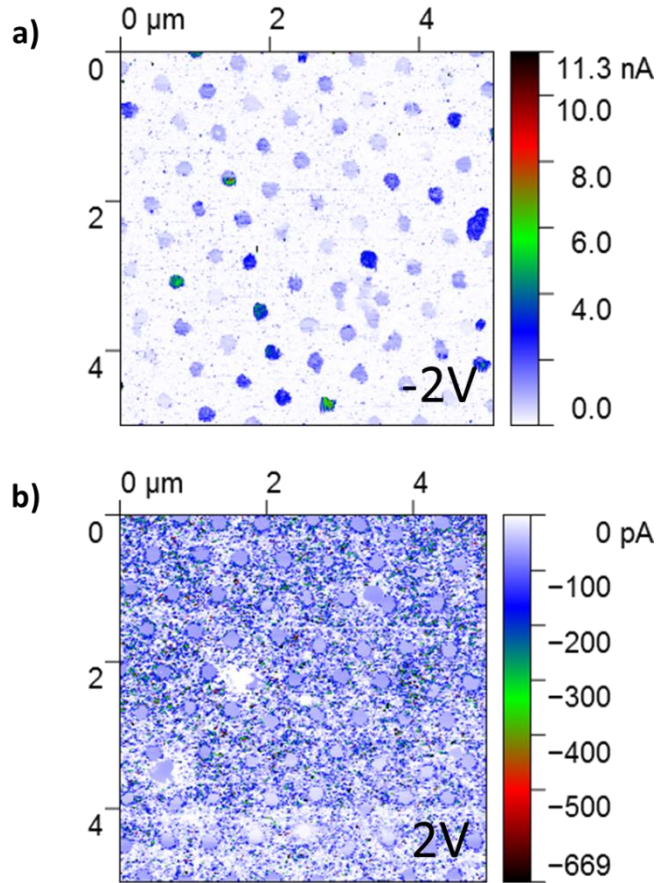


Fig.5.46: Local resistance mapping of 3N-600 nm annealed at 800 °C done at (a) -2 V and (b) +2 V with the Combiscope AFM (having a laser of 1300 nm as wavelength).

It can be seen that outside the holes, no current passed regardless of polarity. Inside the holes, a higher current pass through the holes at -2 V compared to +2 V. These measurements are consistent with the CPAFM measurement presented earlier in Fig.5.45 where the laser was shifted from its usual position. However the value of current observed at -2 V (Fig.5.46.a) is smaller than 4 nA, whereas that observed in Fig.5.45.b at -2 V is around 200 nA (by considering the resistance inside the holes around 10^7 Ohms). This is reasonable as the laser used in this case doesn't photogenerate in the Si and the surface oxidation (few days after HF dip), could further decrease the values of the current both inside and outside the holes. This decrease in current was earlier observed for the diffused sample when the combiscope AFM setup was used (Fig.5.30).

I-V measurements were as well done on this sample using the combiscope inside and outside the holes. The I-V curves in linear scale are shown in Fig.5.47.

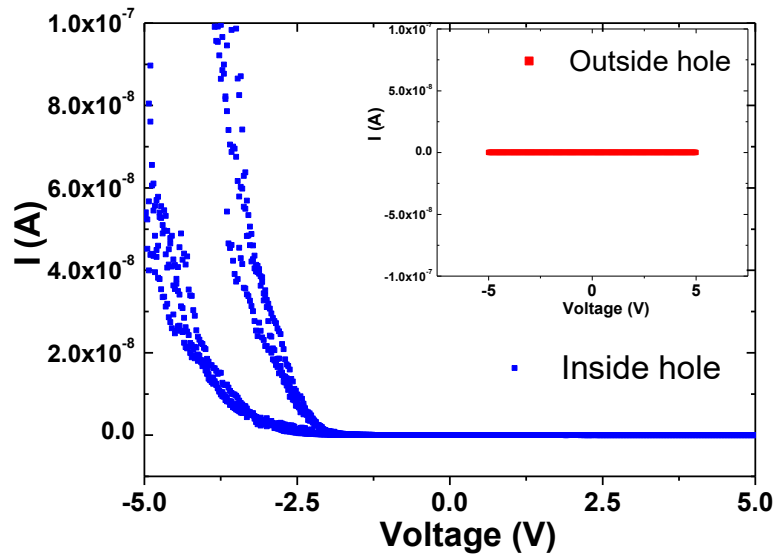


Fig.5.47: I-V measurements inside and outside holes done using combiscope AFM (laser of 1300 nm).

The I-V measurements are consistent with the CP-AFM done using the same Combiscope setup (Fig.5.46). A diode curve can be seen inside the holes and no current is measured outside the holes.

[1N-600 nm annealed at 1000 °C] CP-AFM measurements were done on sample 1N-600 nm annealed at 1000 °C after HF. In these measurements, the Bruker AFM setup was used, the red laser was focused at its usual position, and measurements were taken at -2 V and +2 V. The corresponding measurements are presented in Fig.5.48.

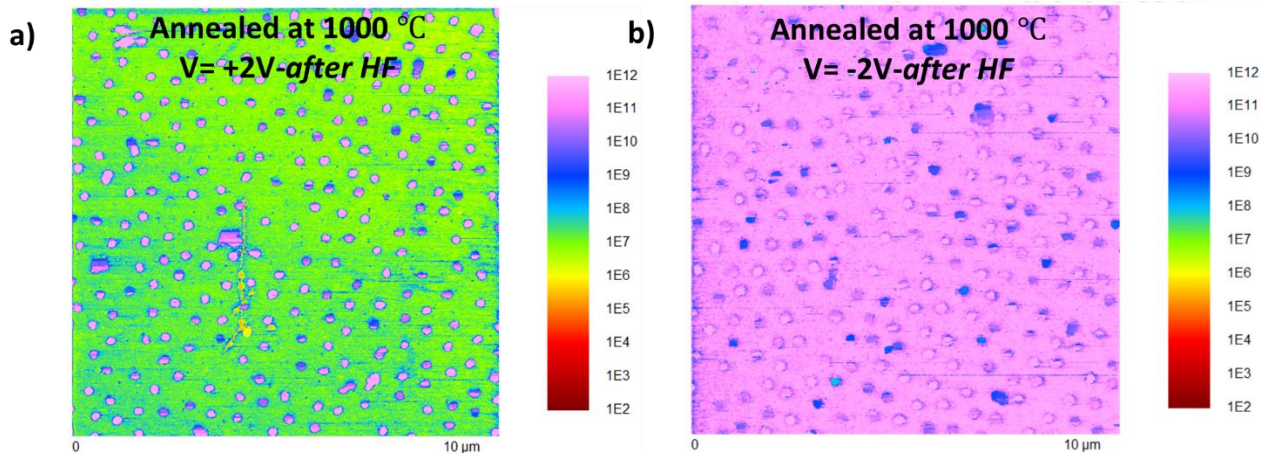


Fig.5.48: Local resistance mapping measurement of 1N-600 nm annealed at 1000 °C after HF at (a) +2 V and (b) -2 V using Bruker AFM (red laser).

It was seen that the holes appear more resistive than the surrounding area when applying a bias of +2 V (Fig.5.48.a), whereas the opposite effect was observed for some of the contacted holes when applying a bias of -2 V (Fig.5.48.b). This is in contrast to the as-implanted samples (Fig.5.38.f and Fig.5.39.b) and those annealed at 800 °C (Fig.5.40.c and Fig.5.40.d), wherein similar resistance was seen inside the holes when +2V or -2V is applied with the Bruker AFM while focusing the laser in its usual position.

[Comparing 1N-600 nm and 3N-600 nm annealed at 1000 °C] CPAFM measurement was as well done on sample 3N-600 nm having a thicker oxide thickness (240 nm) and implanted at 10 keV after HF treatment and compared at similar scales to 1N-600 nm which was already shown in Fig.5.48. The measurements are shown in Fig.5.49.

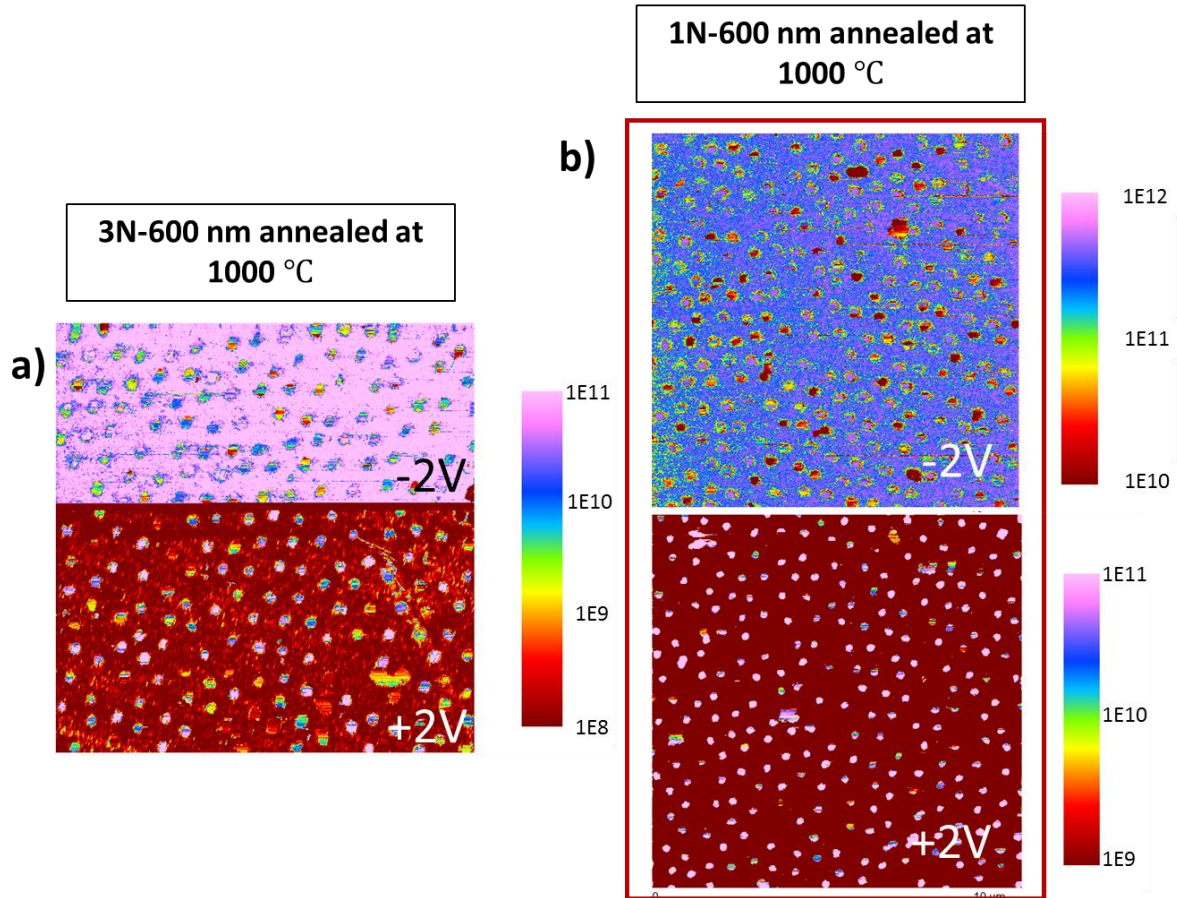


Fig.5.49: Local resistance mapping at similar scales. a) 3N-600 nm annealed at 1000 °C done half at -2 V and half at 2V. b) 1N-600 nm annealed at 1000 °C done at -2 V and +2 V.

Similar mappings are seen for both samples 1N-600 nm and 3N-600 nm annealed at 1000 °C despite the different masking oxide thickness. The areas inside the holes are more conductive compared to the surrounding areas when -2 V is applied, but less conductive when +2 V is applied, confirming the presence of a diode. These observations are similar to what was observed earlier in Fig.5.45 for sample 3N-600 nm. However, it was necessary to shift the laser from its usual position in that case (annealed at 800 °C) to observe this effect, whereas this effect is observed here (annealed at 1000 °C) while keeping the red laser in its usual position. This suggests that although a diode-like behavior is present, almost no photovoltaic effect is present.

[CP-AFM and I-V using 1300 nm laser] The CP-AFM measurement was redone on sample 3N-600 nm annealed at 1000 °C by using the combiscope AFM (1300 nm laser wavelength) to check the electrical behavior of the part inside and outside the holes in the absence of photogenerating light. This measurement and an I-V curve measured inside a hole are shown in Fig.5.50.

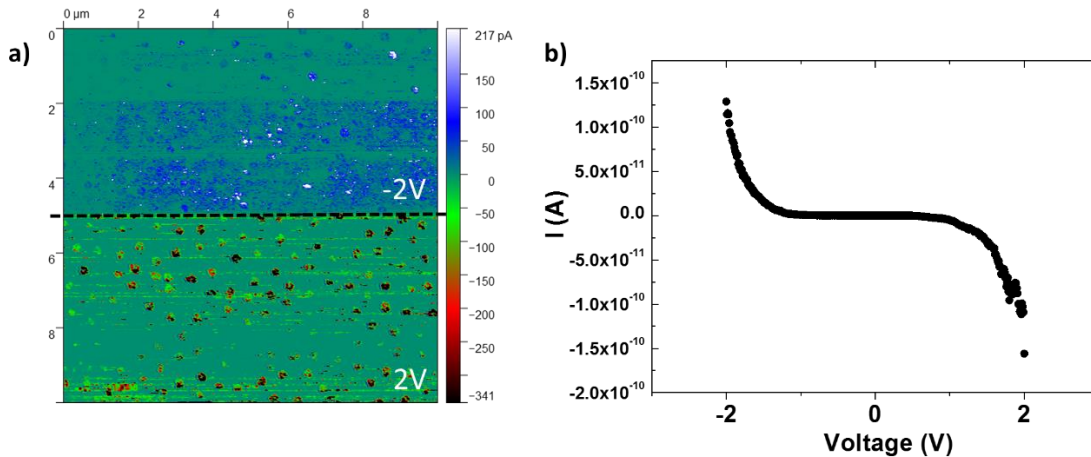


Fig.5.50: Local resistance mapping of 3N-600 nm annealed at 1000 °C done (a) half at -2 V and half at +2 V using the Combiscope AFM (laser wavelength 1300 nm) and (b) I-V curve measured inside the hole with Combiscope AFM.

One can notice a noisy mapping seen at -2 V due to pollution which appears after a few HF treatments. The areas outside the holes are extremely resistive, while a very slight diode-like behavior is seen inside the holes (just slightly more conductive at +2V than at -2V). The I-V curve measured inside the hole shown in Fig.5.50.b is consistent with the CPAFM measurements (Fig.5.50.a). Only a very slight difference between forward and reverse bias is observed.

One can notice that the same conductivity is measured for the outside part when Combiscope AFM setup is being used (1300 nm laser) in Fig.5.50.a, whereas different resistivity is measured for the outside part when Bruker AFM is being used (670 nm laser) in Fig.5.49.a. This observation is for sure due to the presence of the red laser. However, this difference in conductivity for the outside part wasn't seen at -2 V and +2 V for the sample annealed at 800 °C (Fig.5.44. and 5.45) when both the Bruker and the Combiscope were used.

5.1.2.4 Discussion and ECV Measurements

The annealing temperature is an important factor in these results, as seen in the different behavior when the sample is annealed at different temperatures (800 °C and 1000 °C). The annealing temperature usually plays a role on the doping activation, damage recovery and diffusion. One can expect an enhancement of these three phenomena when 1000 °C is used as annealing temperature instead of 800 °C.

As a mask is being used for the part outside the holes, the damage on that part should be less than the part exposed directly to the implantation, therefore the temperature is probably influencing more the boron activation in the part outside the holes. If the masking is not perfect and some boron is implanted in the Si underneath the mask, this implanted boron in the Si is expected to diffuse more when the sample is annealed at 1000 °C compared to the case annealed at 800 °C. This can lead to a boron doping of the Si part that was masked for the sample annealed at 1000 °C, thus the formation of a p-n junction that is sensitive to the presence of the red light. The boron should be less in the masked part compared the unmasked part, therefore we were still able to see difference in the electrical behavior between the inside and the outside parts.

To understand if the boron doping done by implantation was successful, ECV measurements were done on two reference Si samples (parts of the same wafer of sample 1N-600 nm) without a masking layer: one annealed at 800 °C and the other at 1000 °C by RTA during 5 minutes after 10 keV boron implantation. The

measurements are shown in Fig.5.51 and they are compared to the one simulated by TCAD, As implanted without masking oxide, which was previously shown in Fig.5.35.

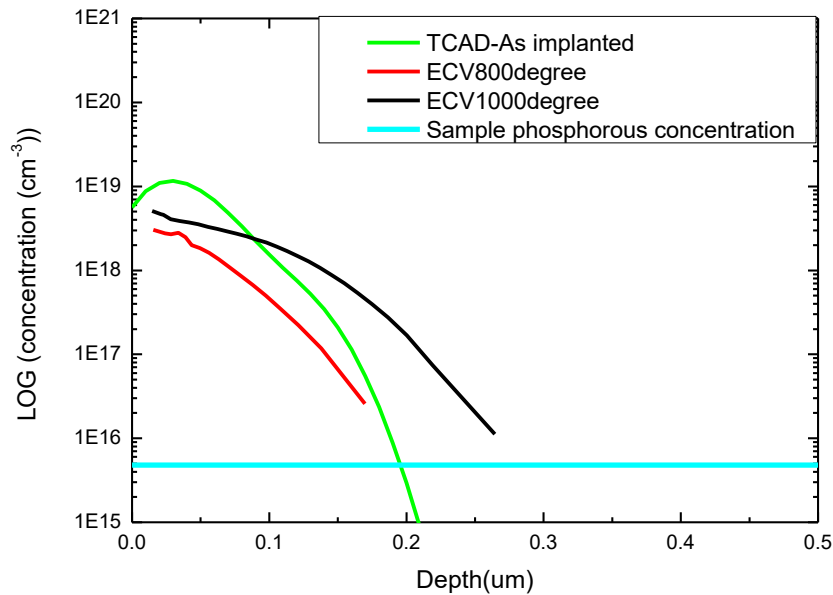


Fig.5.51: Initial phosphorous concentration and boron profile of the “as implanted” sample simulated by TCAD, and that measured by ECV for the reference samples implanted at 10 keV without oxide layer and annealed at 800 °C and 1000 °C.

It can be seen from ECV measurements that the boron is active for the reference samples that are unmasked and annealed at 800°C and 1000°C. This suggests that a successful boron doping was achieved inside the holes for these samples. More ECV measurements should be done in the future on reference samples masked with SiO₂ during the implantation and later annealed at 800 °C and 1000 °C in order to confirm the efficiency of the masking thickness used.

5.1.2.5 Summary – Ion implantation results

The results for the doping through holes using ion-implantation were less conclusive than when diffusion was used.

Even after annealing, the samples implanted at 10 keV didn't appear bright in the SEM images (using the SE (U) detector) in contrast to the samples doped by diffusion, even though ECV measurements have shown that the boron is activated when the sample was annealed at 800 °C and 1000 °C. However, the areas implanted at 20 keV appeared bright for the samples annealed at 800 °C and 900 °C, although they become black when annealed at 1000 °C.

The holes of the as-implanted samples were resistive at both -2 V and +2 V, probably because of amorphization or damage caused by the implantation. The surrounding areas of the as-implanted sample and the one annealed at 800 °C become conductive after an HF dip, where it becomes even more conductive than the implanted holes in the case of 800 °C.

For the samples annealed at 800 °C, the presence of a V_{oc} (which decreased when shifting the position of the laser on the tip) confirmed that a photodiode is formed inside the holes. The CP-AFM mapping was therefore sensitive to the presence of the red laser; where the same resistance was observed inside the holes annealed at 800 °C at -2 V and +2 V when the red laser is in its usual position on the AFM tip and more conductive holes were seen at -2 V (forward bias) after shifting the laser position. Having a higher conductivity when forward biased and a smaller one when reverse biased suggests the formation of a diode inside the holes. This observation was confirmed by doing the CPAFM measurement with the setup having an infrared laser. A diode behavior was observed inside the holes by doing the I-V curves in this setup while no current was measured outside the holes.

For the sample annealed at 1000 °C, no photovoltaic behavior was observed. The holes were more conductive at -2 V (forward bias) when doing the CPAFM using the red laser. The areas surrounding the holes measured with the red laser setup appear more conductive at +2 V than at -2 V, whereas they showed similar conductivity at -2 V and +2 V with the infrared laser setup. This contrasts with the as-implanted sample and the one annealed at 800 °C, for which the same conductivity was observed outside the holes regardless of the laser used during the measurement.

More investigation should be done for the Si part that was masked and later annealed at 800 °C and 1000 °C (after etching the masking oxide) by using other characterization tools. This investigation is needed in order to understand the reason of the high conductivity observed at +2 V for the part outside the holes for the sample annealed at 1000 °C when measured with the AFM having a red head laser.

5.2 Chapter Summary

The results of this chapter can be summarized as follows:

- Approach B (using Al as a mask followed by oxide plasma etching through the Al holes), was used to form holes in 120 nm and 240 nm thermally grown oxide. This was followed by performing a doping through the oxide with nanoscale holes by diffusion and ion implantation.

For the diffusion doped samples:

- The doped holes in the Si have a “dinner plate” shape, seen by SEM, caused by the process of etching the boron glass formed during diffusion.
- A brightness contrast was seen from SEM top and side view for the boron doped parts when using the SE(U) detector.
- A higher conductivity was seen inside the holes compared to the outside part by CPAFM measurements with a resistive halo observed around the holes. This halo is most probably related to a surface feature as its width decreased after an HF dip.
- Solar cell behavior was observed inside the holes through the presence of a V_{oc} and a J_{sc} in the I-V curves caused by the photogeneration of the AFM red laser.

For the ion implantation samples:

- No brightness contrast in SEM (SE(U)) was seen for the annealed samples at 800 °C and 1000 °C after implantation at 10 keV, although the ECV measurements have shown that the boron is activated at these conditions.
- The holes of the as-implanted samples were resistive at both -2 V and +2 V, probably because of amorphization or damage caused by the implantation.
- A V_{oc} was observed for the implanted holes annealed at 800°C, and which decreased when shifting the position of the laser on the tip, confirming that a photodiode is formed inside the holes. However, only a very small photocurrent is observed.
- The CP-AFM mapping was sensitive to the red laser position on the tip; where the same resistance was observed inside the holes annealed at 800 °C at -2 V and +2 V when the red laser is in its usual position on the AFM tip and more conductive holes were seen at -2 V (forward bias) after shifting the laser position on the tip. This was confirmed by repeating the measurement with an infrared laser.
- The samples annealed at 1000 °C were more conductive at -2 V (forward bias) when doing the CPAFM with the red laser.
- Doping by implantation was more complicated to analyze compared to the doping by diffusion as the implantation was followed by an annealing step at different temperature which can affect the degree of damage recovery and doping activation. A better process to produce working photovoltaic devices must be developed.

Chapter 6: Conclusions and Perspectives

6.1 Conclusions

What was done in this thesis?

In this PhD work, local doping in the nanoscale was performed. It initiated by the deposition of a PS NP monolayer on an n-type cSi substrate. The deposited NPs were used as a mask to form holes in the nanometer scale in the passivation oxide layer. P-type doping was then performed through the holes of the oxide masking layer and finally the doping was characterized by SEM and CP-AFM. The first and last state of the process are summarized in Fig.6.1.

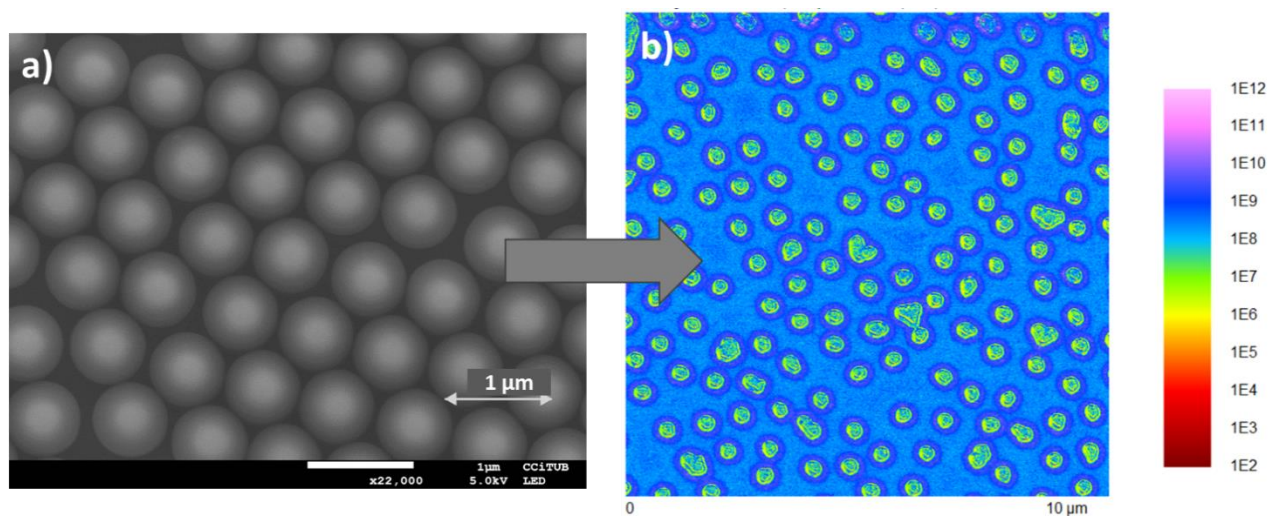


Fig.6.1: a) Monolayer of 600 nm NPs and b) Mapping resistance by CP-AFM of doped holes formed using 600 nm NPs.

By doing local I-V measurements, in the presence of a red laser, photogeneration effect was seen inside the holes which confirmed the formation of a solar cell in the nanometer scale. Hence, this observation confirms the successful local doping done in the nanometer scale.

How was the doping done experimentally in the nanoscale?

Holes are first formed in the oxide followed by doping through the holes:

[Holes in the oxide] A monolayer of PS NPs with diameters of 600 nm and 800 nm was first deposited by floating transfer technique on a cSi sample coated with a thermal oxide passivation layer. PS NPs was then etched, in an O₂ MD-ECR plasma, down to between 4 % and 9 % of their initial areas (see Chapter 3). Evaporated Al was used as a mask on the etched NPs; it was evaporated on the NPs followed by NP removal. Plasma etching was performed to etch the oxide through the holes of the Al masking layer which was then etched away (Approach B, see Chapter 4). By doing all these steps, holes were formed in the oxide layer, ready for the doping step.

[Doping through the holes] Boron doping in the holes was performed by diffusion and ion implantation by using the oxide layer as the doping mask (see Chapter 5). The oxide was then removed, and samples were characterized by SEM, CP-AFM, and ECV.

Doping by implantation was more complicated to analyze compared to the doping by diffusion as the implantation was followed by an annealing step at different temperature which can affect the degree of damage recovery and doping activation.

What are the key lessons of this thesis?

The key lessons can be divided in three different parts. The first one is related to **NP etching** (floating transfer followed by O₂ plasma etching), the second one is about **nanoscale contacts for cSi solar cells** and the third one is focused on the **characterization of doping in the nanoscale**.

[NP etching] The NP etching study by MD-ECR (ch.3) was performed using different plasma modes.

It was seen that by using a high-power, 1 kW continuous plasma, the NPs are melted and wetting the surface. This effect was mitigated by cycling the plasma, reducing the power, or placing the particles behind an ion shielding metal cage. However, by performing longer etching times under conditions that avoided melting, a “toppling” effect was observed, making the array of the NPs less regular.

These results can add a flexibility to the nanosphere lithography technique depending on the final structure desired. If one is interested in avoiding the toppling effect of the NPs and conserving the initial periodic distribution, then the sequential use of process may be of interest. One may first use a process that partially melts or softens the NP, before using a low-heating process to etch them down.

If one is interested in a smaller NP etched size and a higher distance between them, the use of the cycled plasma is of interest. By using this mode, it was seen that the NPs were etched down to between 4 % and 19 % of their original area without causing melting, and by conserving its patterning capabilities. If one is interested in forming point contacts for instance (similarly to our application), this plasma mode can give a certain level of control over hole pitch and coverage.

In summary, this study has shown that depositing NPs by floating transfer technique followed by etching them in a cycled plasma, can lead to a NP coverage lower than 10 %, which is adequate for point contacts application.

[Nanoscale contacts for cSi solar cells] Nanoscale local doping through the holes could be interesting for cSi solar cells application in two different ways:

By performing local doping opposite to the doping type of the substrate (done in Chapter 5), solar cells in the nanoscale are formed. The distribution of the formed solar cells and their dimensions could be controlled to a certain level by choosing the initial NP diameter and the O₂ plasma conditions used.

Performing same doping type as that of the wafer in nanoscale contacts could be interesting for PERL solar cells.

It was seen by simulation (in ch.1) that the definition of contacts whose size is in the 1 μm range for PERL structures is more advantageous compared to micro-contacts when S_{cont} in the range of 10⁵-10³ cm/s. Therefore, having doped contacts in the nanometer is promising for PERL solar cells. Such openings dimension was achieved in this thesis by using a cost-reducing way, focused on the use of polystyrene

Conclusions and Perspectives

nanospheres as a sacrificial mask. To form the PERL doped contacts, the same type of doping as that of the substrate should be performed through the holes in a future work (More developed in “perspective” part).

[Characterization]

[SEM] It was seen that the SEM is a potential tool to visualize the contrast between the p formed in the holes and the n type substrate. A good contrast was observed inside and outside the holes for the samples locally doped by diffusion.

[CP-AFM] Having different conductivity inside the holes during the resistance mapping measurement when changing the polarity of the applied voltage was an indication of the existence of a diode in the measured spot.

To confirm the existence of a photodiode, a local I-V measurement was done. Observing a diode shape with a V_{oc} shift in the local I-V measurement confirmed the existence of a solar cell in the measured spot. This characterization tool is potential for solar cells characterization at the nanoscale. Some modifications can make it even more coherent (More developed in “perspective” part).

6.2 Perspectives

Characterizing more in detail the samples locally doped by implantation in Chapter 5.

As the implantation was followed by an annealing step at different temperature which can affect the degree of damage recovery and doping activation, it was more complicated to analyze the samples locally doped by implantation compared to those doped by diffusion.

To produce working photovoltaic devices with the nanoscale locally implanted samples, a better process must be developed. To do so, a better understanding of these samples should be first done by using other characterization tools.

These tools could be:

-**ECV measurements** These measurements were done in Chapter 5 only on the reference samples without the masking oxide. To have a complete study, these measurements should be done as well on the reference samples covered with a full masking oxide layer during the implantation.

The reference samples are the as implanted sample, those annealed at 800 °C and 1000 °C after the mask removal. This measurement can help confirming the efficiency of the mask thickness used during the implantation.

-**Nanosims measurement** that can be compared with the values obtained from the ECV measurements done on the reference samples.

-A characterization of the amorphous and cSi phase of the implanted sample inside and outside the holes. This can be done by **TEM measurements** for the as implanted sample and that annealed at 800 °C and 1000 °C. This can help in observing the effect of the annealing temperature on the damage recovery of the implanted samples.

Repeating the same process with the same doping type as that of the wafer and scaling up

-In order to confirm the simulation done in Chapter 1 for PERL application, the same type of doping as that of the substrate should be done and characterized by CP-AFM. However, the local I-V curves won't be interesting in this case (as no p-n junctions are formed), therefore another characterization tool like **nanosims** could be used to complete the study.

-This process should be scaled up to at least $\frac{1}{4}$ of a wafer which should undergo series resistance and lifetime measurement. These measurements should be compared to another sample from the same wafer, having the same percentage of openings with micro-scaled openings.

-This process could be later applied to fabricate a solar cell with the architecture presented in Fig.6.2.

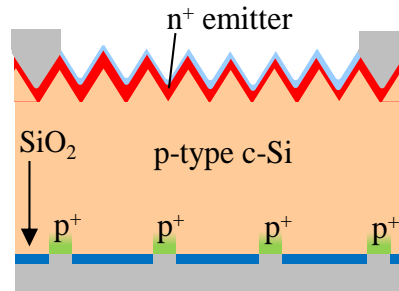


Fig.6.2: Considered rear contact configurations to define partially contacted surfaces with contacts in 1 μm range with p^+ regions fabricated by thermal diffusion and thermally grown SiO_2 passivation.

Improving the method of opening holes in the Al_2O_3 passivation layer and scaling up

-Improving the RCA soft method used in ch.3 to form holes in the Al_2O_3 layer. To improve the yield in the fabrication process of the nanoholes in the Al_2O_3 , a reduction of the Al_2O_3 layer thickness from 50 nm to 20 nm could be an option. It was verified that this thickness reduction does not impact the surface passivation quality [260] and it is possible that this thinner Al_2O_3 film will facilitate nanoholes formation. Once succeeded, a solar cell can be fabricated with the architecture presented in Fig.6.3.

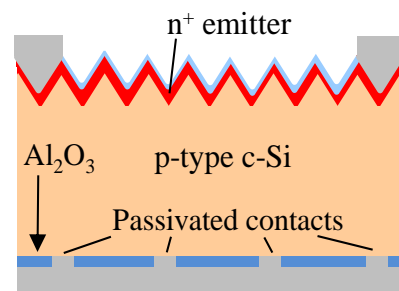


Fig.6.3: Considered rear contact configurations to define partially contacted surfaces with contacts in 1 μm range with low temperature passivated contacts and Al_2O_3 passivation.

In this cell architecture, the passivated contacts can be done by a low temperature technique. Good candidates are transition metal oxides like MoO_x [93] that have demonstrated a good carrier selectivity with a low contact resistance. Another feasible possibility is the deposition of boron-doped amorphous silicon films based on silicon heterojunction technology [90].

Conclusions and Perspectives

-Once the cells shown in Fig.6.2 and 6.3 are fabricated, their performance should be compared with similar solar cells having the same percentage of point contacts with the openings dimension in the micro-scale.

Investigating local doped epitaxial growth through the nanoscale openings

Doping by diffusion is known to be a high temperature process. Although the implantation can be done at room temperature, it requires high temperature annealing step after implantation to activate the dopants. Therefore, both process (diffusion and implantation) used in this thesis can be considered as high temperature process.

To reduce the thermal budget, one can think about doped Si epitaxial growth to passivate the contacts.

A trial of Si growth was done during this thesis on cSi samples where holes were already formed in the thermally grown oxide using approach B (ch.4).

This growth was done, after 30 s HF, in RF-PECVD at 175 °C, using (500/35/0.8) sccm of ($H_2/SiH_4/Trimethylboron(TMB)$) at 2 mBar and 31 mW/cm². The growth was followed by an annealing at 300 °C during 10 min. The masking oxide was then etched with an HF dip of 15 min.

The schematic illustration of the different steps with the corresponding SEM images are shown in Fig.6.4.

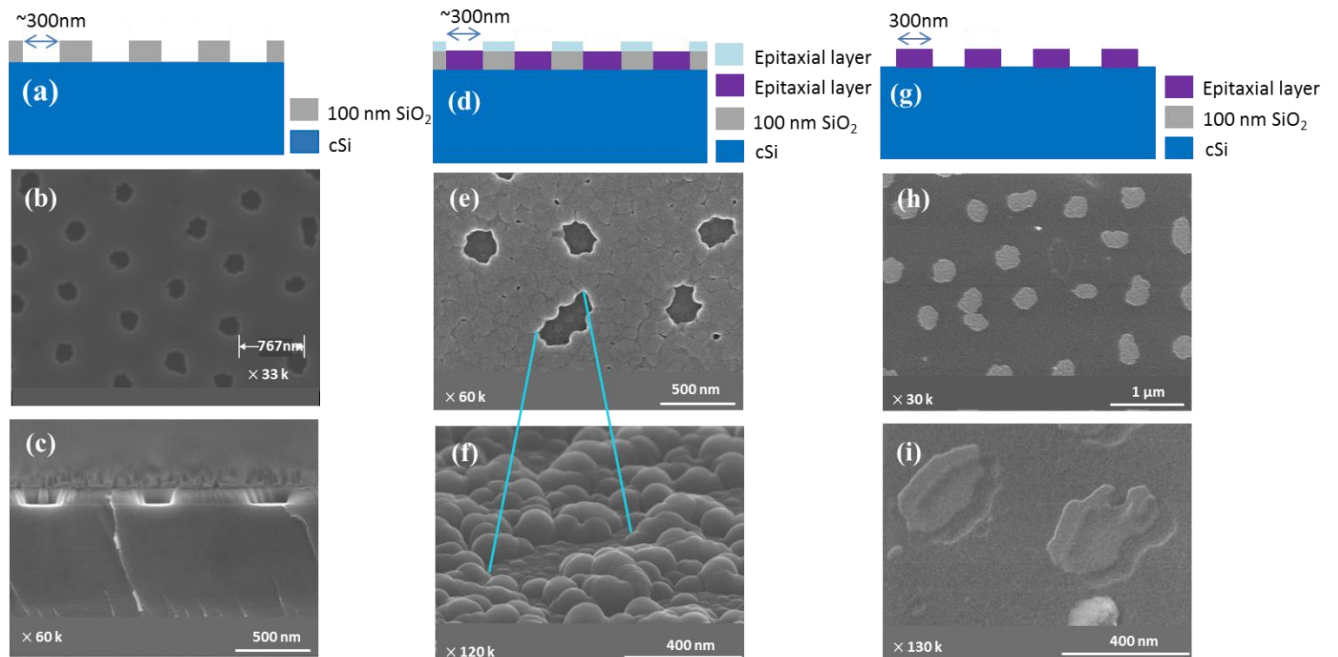


Fig.6.4: Schematic illustration of (a) cSi covered with patterned SiO₂, (d) After epitaxial growth and (g) After SiO₂ etching. (b), (e) and (h) SEM top view of (a), (d) and (g), respectively. (c), (f), and (i) SEM side or tilted view of (a), (d) and (g), respectively.

In the ideal case, a growth of cSi is expected inside the holes and a growth of a-Si:H on the oxide masking layer.

Conclusions and Perspectives

A growth can be seen inside and outside the holes from the SEM image of Fig.6.4. Even after removing the oxide, the layer grown inside the holes remained on the surface following the same shape and distribution as that of the initial holes in the oxide (Fig.6.4.h and Fig.6.4.b).

More analysis (like **Nanoraman or TEM**) should be done on this sample to confirm if the layer grown inside the holes is crystalline.

As the part inside the holes appear brighter compared to the surrounding in Fig.6.4.h taken using the SE(U) detector (Detecting only SE) at 1 kV, one can expect that the growth is successfully doped with boron. More analysis should be done in order to confirm this point and to confirm if the passivation would be successful by using the epitaxial grown layer as the passivation layer.

Once the boron doped epitaxial cSi is confirmed inside the holes, this process can be later used with an Al₂O₃ passivation layer instead of a thermally grown oxide to further reduce the thermal budget of the whole process.

Improving the CP-AFM setup for coherent solar cell measurement in the nanoscale

V_{oc} shift was observed in the I-V measurements done in ch5, due to the photogeneration of the red laser in the formed solar cells. However, this V_{oc} can't be considered as a characteristic of the solar cell measured as it is not done at AM1.5.

To get trustable values (V_{oc} , J_{sc} , FF) for the formed solar cells using the CP-AFM, a classical lamp used for solar simulator could be added to the AFM setup that operate with a laser of 1300 nm. The laser of 1300 nm will allow to control the distance between the probe and the measured sample without photogenerating in cSi and the added lamp will allow the cell to be measured at AM 1.5. This combination will permit I-V measurements to be performed locally at the nanoscale.

Appendix

Related to chapter 3:

[Effect of Ethanol as solvent for 50 nm spin coated NP] To see the ethanol effect on the NP aggregation, the NP suspension was diluted with ethanol instead of DI with the same dilution fraction of 1/40 (0.1ml of the NP suspension with 4 ml of ethanol) used with dilution by DI water. The SEM images are shown in Fig.A.1.

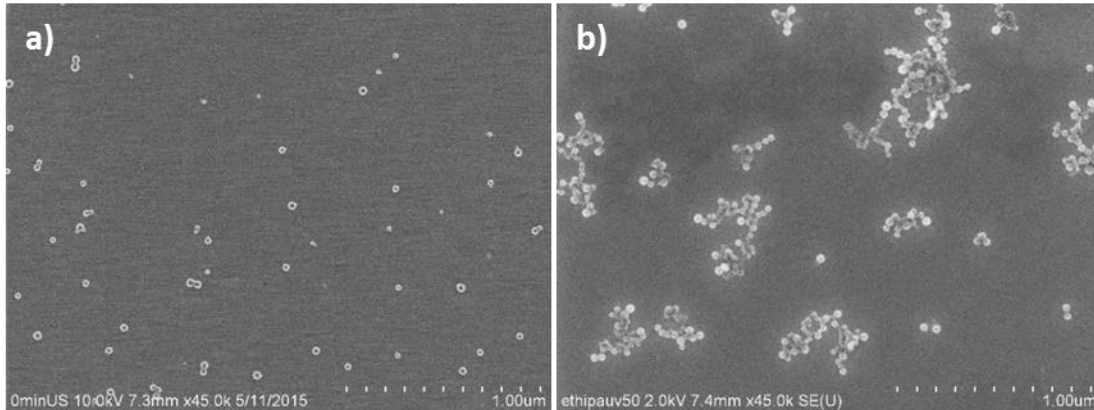


Fig.A.1: SEM images of 50 nm spin coated solution diluted (a) with DI and (b) with ethanol.

It was seen that ethanol increases the NPs aggregations compared to the solution diluted with DI.

[Effect of the number of consecutive spin coating on NP density] NPs of 100 nm were as well spin coated on metal-coated glass (glass covered with 100 nm AlCu (alloy of 98 % Al and 2 % Cu)). Two and three consecutive spin coatings were done on these samples to see if a series of spin coating could affect the density of distributed NPs. All the spin coating trials were done using 6000 rpm as speed, 2000 rpm/s as acceleration, and 4 s 30 s as spin coating time. The corresponding SEM images are seen on Fig.A.2.

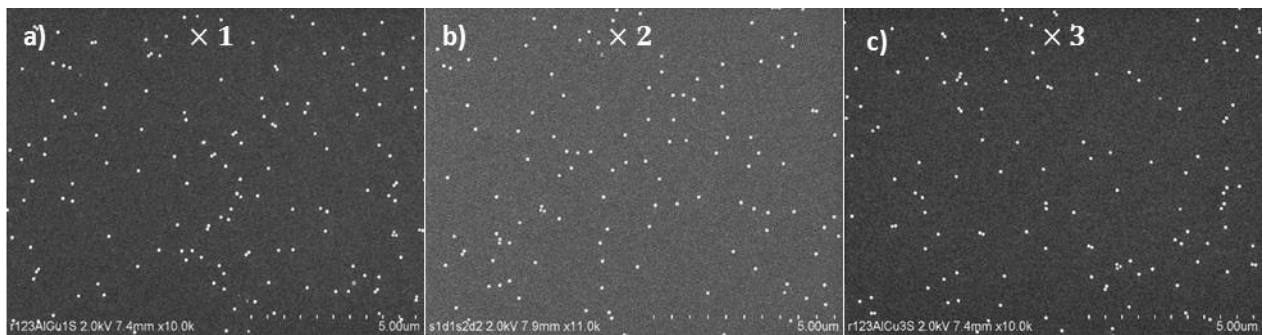


Fig.A.2: SEM images of AlCu samples on which the NPs were spin coated (a) one time, (b) two consecutive times and (c) three consecutive times.

It was seen that there is no much difference in the NPs density between the three cases shown in Fig.A.2. The density was between 1 and 2 NPs/ μm^2 .

[Other ways tried to remove the NPs]

[Acetone] US bath of Acetone was used on metal-coated glass (glass covered with 100 nm AlCu) covered with ITO to remove the NPs after depositing 12 nm SiO₂. This was followed by 12 min US bath of isopropanol. The corresponding SEM images, before and after NP removal, are shown in Fig.A.3.

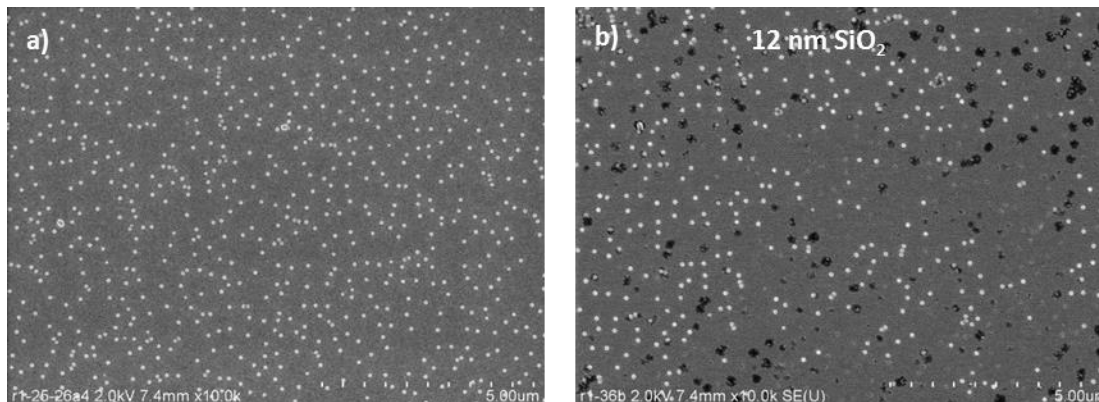


Fig.A.3: SEM images of the Al-ITO substrate (a) before and (b) after acetone -isopropanol US bath.

It was seen that after applying 30 min of acetone US bath on this sample, NPs were partially removed with an appearance of some black marks.

[Trial of burning out the PS] Another trial of NP removal was done by heating the substrate to burn out the polystyrene NPs. An annealing at 300 °C during 20 min was done on cSi sample having 50 nm NPs covered with 5 nm and 10 nm SiO₂. The SEM images are shown in Fig.A.4.a and A.4.b.

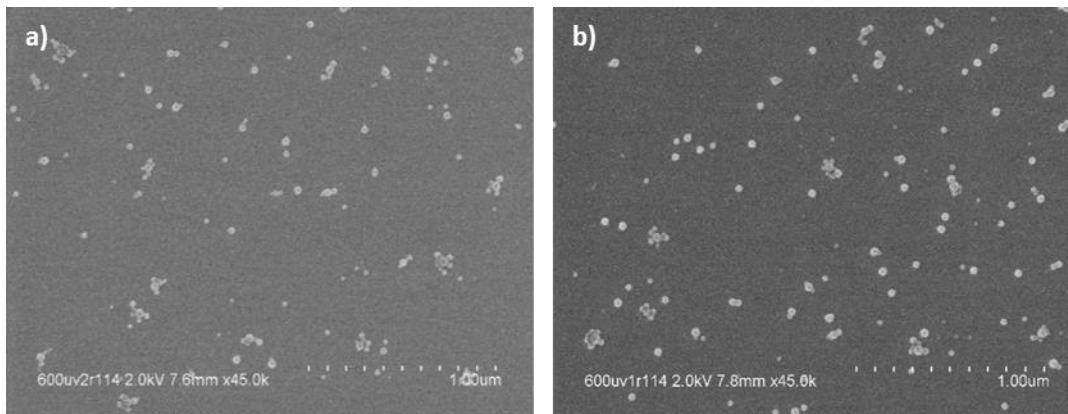


Fig.A.4: SEM top view images where the annealing was done at 300 °C during 20 min on (a) a sample covered with 50 nm NPs and 5 nm SiO₂ and (b) on a sample covered with 50 nm NPs and 10 nm SiO₂.

The NPs weren't removed probably because the annealing time and duration were not enough to completely melt the NPs.

A cSi sample having 100 nm spin coated NPs was covered with 30 nm a-SiC_x:H and put on a hot plate having a cover. The sample was kept at 400 °C for 1 hour in a 250 sccm nitrogen flow.

The corresponding SEM image is shown in Fig.A.5.

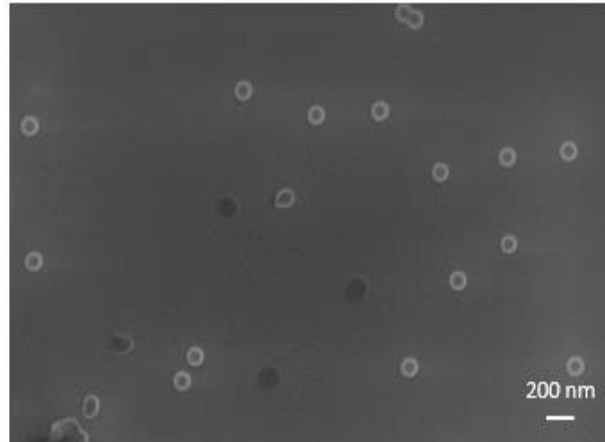


Fig.A.5: SEM image of the cSi sample covered with 100 nm spin coated NPs and 30 nm a-SiC_x:H after putting it on a hot plate for 1 hour.

It was seen that very few NPs were removed. The annealing time was further increased to 1 hour 30 min using a similar sample. The corresponding SEM image is shown in Fig.A.6.

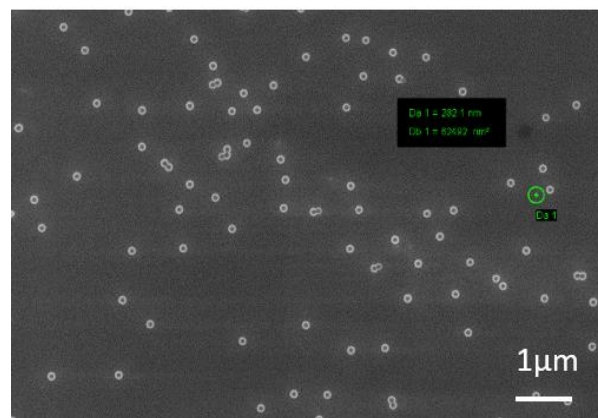


Fig.A.6: SEM image of the cSi sample covered with 100 nm spin coated NPs and 30 nm a-SiC_x:H after putting it on a hot plate for 1 hour and 30 min.

Even after increasing the annealing time, this method remains inefficient to remove the NPs.

Another trial of annealing with N₂ was done in the PECVD reactor immediately after the a-SiC_x:H deposition to remove the NPs. This method can be efficient in term of reducing the steps needed to form the nanoholes in the a-SiC_x:H layer. Therefore, after the a-SiC_x:H deposition at room temperature inside the RF-PECVD, the sample with NPs was kept inside the reactor in order to perform an annealing at a temperature of 350 °C.

This annealing was done at 1 mbar by adding 25 sccm of N₂ during 2 hours. This trial was done on two samples, one having 800 nm etched NPs and the other having 600 nm etched NPs deposited on 50 nm Al₂O₃ covering the cSi samples.

The SEM images of the samples after annealing are shown in Fig.A.7.

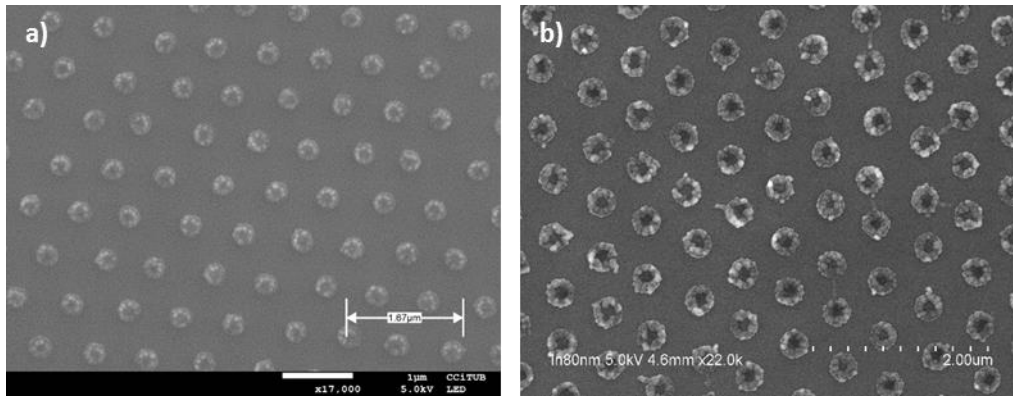


Fig.A.7: SEM image of the sample after an annealing at 350 °C during 2 hours in a N₂ flow in the PECVD reactor of (a) 800 nm etched NPs and (b) 600 nm etched NPs.

It was seen that this method doesn't burn out the NPs, but it melts them. 45 min Toluene US bath followed by 15 min isopropanol US bath was applied on the samples. The corresponding SEM images are shown in Fig.A.8.

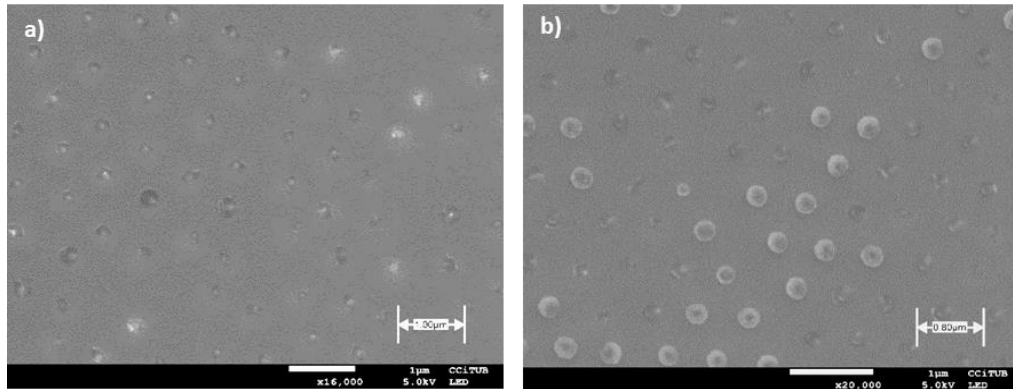


Fig.A.8: (a) and (b) SEM images of the samples corresponding to Fig.A.7.a and Fig.A.7.b respectively, after toluene US bath.

It was seen that the annealing in RF-PECVD at 350 °C was not enough to burn out the NPs. An additional step of toluene US bath was required to remove some of the NPs.

As 1-methyl-2-pyrrolidone is known to dissolve a wide range of polymers, a trial to remove the 100 nm spin coated NPs covered with 20 nm a-SiC_x:H was done by immersing the sample in the heated solution at 120 °C for 15 min. The SEM image is shown in Fig.A.9.

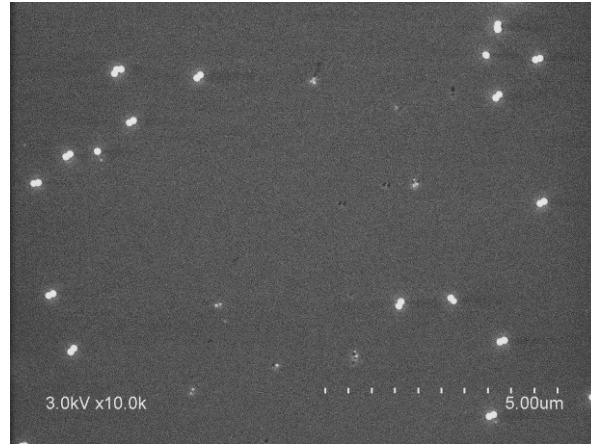


Fig.A.9: SEM image after applying 1-methyl-2-pyrrolidone on the sample having 100 nm spin coated NPs covered with 20 nm a-SiC_x:H.

It is seen that some NPs were removed, and others have a size reduction.

Another way to try to remove the NPs was applied on the sample having 50 nm NPs; it consists of exposing the NPs to an O₂ plasma. 30 min O₂ plasma was applied on the samples after covering the NPs with 5 nm and 10 nm SiO₂. The SEM images are shown in Fig.A.10.a and Fig.A.10.b respectively.

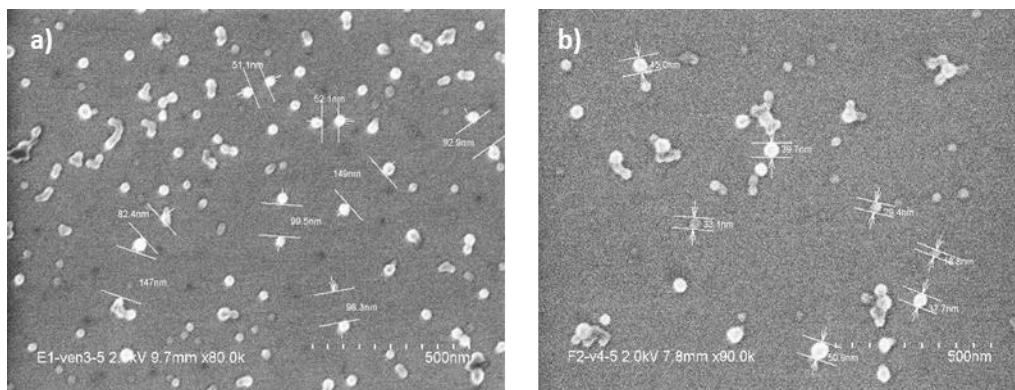


Fig.A.10: SEM top view images of (a) 50 nm NPs covered with 5 nm SiO₂ after 30 min O₂ plasma, (b) 50 nm NPs covered with 10 nm SiO₂ after 30 min O₂ plasma.

Some of the NPs are removed, and others are etched and are barely seen from the SEM images. It seems that NP melting took place during the O₂ plasma as some aggregations appear smoother. NPs melting is probable to occur during O₂ plasma as was explained in chapter 3, especially that the O₂ plasma duration was relatively high (30 min) in this case. In fact, the NP melting is not significant as seen from the SEM top view images. This is probably related to the presence of the SiO₂ layer on the NPs that could diminish the direct NP exposition to the oxygen ions.

Related to chapter 4:

[Approach C-SiO₂ as dielectric] Approach C was applied on a cSi sample covered with thermally grown oxide. The steps of approach C are presented in Fig.A.11.

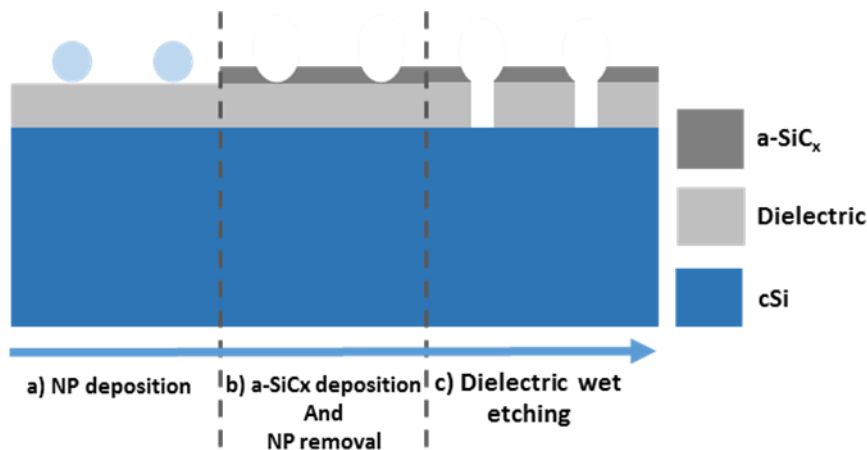


Fig.A.11: Schematic illustration of steps done to form nanoholes in dielectric layer covering silicon. (a) NP deposition on dielectric layer, (b) a-SiC_x:H deposition followed by NP removal, (c) Dielectric wet etching through a-SiC_x:H holes.

The SiO₂ wet etching was done by buffered oxide etch (BOE) solution (a mixture of ammonium fluoride and HF). a-SiC_x:H deposited by RF-PECVD seems to be an adequate mask to use in approach C, as it was checked that the a-SiC_x:H is not etched by the BOE solution even after applying 9 min of this solution on a sample of Si covered with 30 nm a-SiC_x:H.

To confirm that this mask will remain intact if used on a SiO₂ layer, 30 nm a-SiC_x:H was deposited on a sample having 30 nm thermally grown oxide and another having 120 nm SiO₂.

After doing some tests, it was confirmed that the a-SiC_x:H can be used as a mask for the SiO₂ etching if the exact etching rate of the dielectric layer is known prior to the etching. This is because by applying a higher etching time than needed to etch the SiO₂ thickness under the mask, this latter will be etched.

The next trial was done on a sample where holes are already formed in the a-SiC_x:H layer. The SiO₂ thickness used is around 240 nm covered with 30 nm a-SiC_x:H. After applying half of the time needed to etch the total layer of oxide by the BOE solution, the etching was stopped because the color of the sample was modified. The corresponding SEM images are shown in Fig.A.12.b and c.

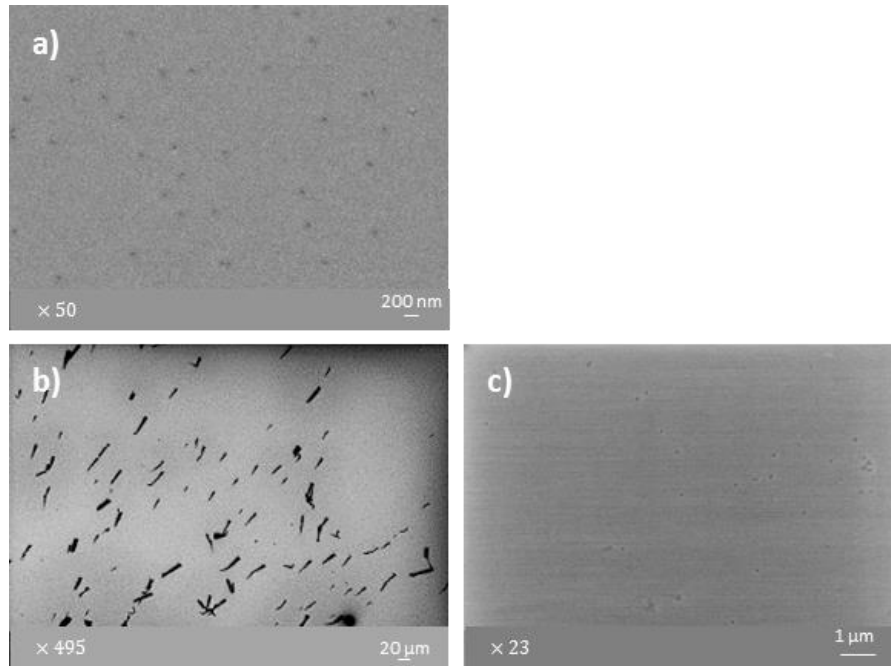


Fig.A.12: (a) SEM top view images corresponding to the step shown on Fig.A.11.c.

It is seen that there are some stiction on the sample surface mainly related to the a-SiC_x:H etching. As from Fig.A.12.c, it is seen that there are some features on the oxide surface following the shape and dispersion of the spin coated NPs. This is probably due to a higher etching of the SiO₂ thickness through the a-SiC_x:H holes. From the ellipsometry measurement, it was seen that the remaining thickness of SiO₂ is around 164 nm. As the a-SiC_x:H couldn't protect the SiO₂ from etching by BOE during half of the time needed to etch completely the 240 nm of oxide, it can't be used as an efficient mask for approach C.

Approach C is not a good choice to form holes in an oxide layer. Approach B remains the most suitable one to form holes in different oxide thickness by using plasma etching to etch the oxide through the Al holes.

Related to chapter 5:

To evaluate the effect of the red laser spot of Bruker AFM setup on V_{oc} , a planar silicon photodiode (SLCD-61 N8) was used. The measurement of I-V curves were done on this photodiode by using two different AFM setups; the usual AFM Bruker laser 670 nm (red) and the Combiscope AFM AIST-NT laser 1300 nm (infrared).

The measurement on the AFM Bruker was done by putting the sensitive area of the photodiode in two different positions; (A) the sensitive area was not covered by a sample holder, and (B) the sensitive area was covered by a sample holder and a cantilever. The schematic illustration of the photodiode and photos taken in its position (A) and (B) are shown in Fig.A.13.

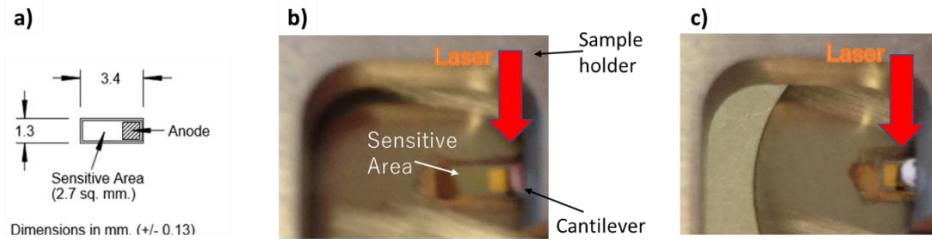


Fig.A.13: (a) Schematic illustration of photodiode (SLCD-61 N8), (b) Position A where photodiode’s sensitive area is not covered with sample holder, and (c) Position B where its sensitive area is covered by sample holder and cantilever.

The I-V curves measured on the photodiode by using Bruker AFM while putting the photodiode in both position A (red curve) and B (green curve) and that measured by Combscope (black curve) without covering the photodiode are shown in Fig.A.14.

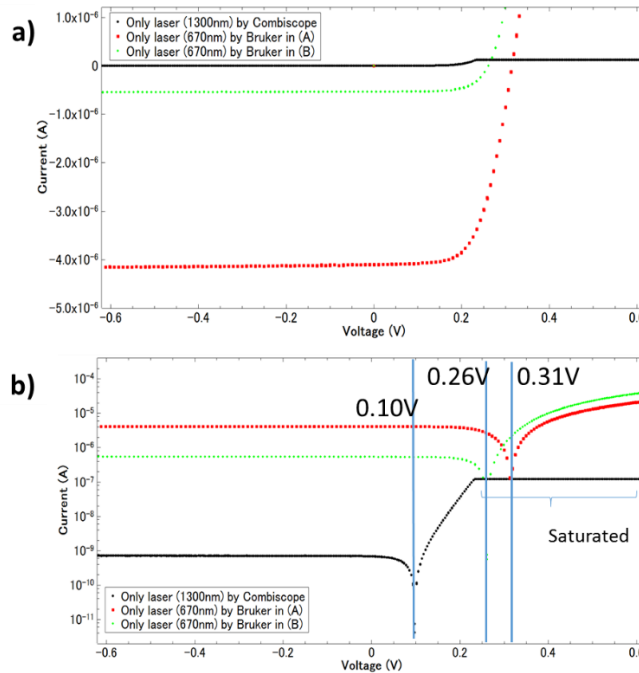


Fig.A.14: I-V curves measured on photodiode by using Combscope AFM (black curve), Bruker AFM while photodiode is in position (A) (red curve) and in position (B) (green curve) in (a) linear scale and (b) log scale.

It was seen from Fig.A.14 that the V_{oc} measured by Bruker AFM while the photodiode is in position A and B is 0.31 V and 0.26 V, respectively. It decreases to 0.10 V when the V_{oc} is being measured by the combscope AFM.

The shift in V_{oc} is related to the red laser photogeneration effect in the photodiode. This effect decreased after putting the photodiode in position B where the laser intensity is less. It was further decreased after replacing the red laser by an infrared one.

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Résumé en Français

Durant cette thèse, j'ai étudié la possibilité et les avantages d'utiliser des contacts nanométriques au-dessous de $1\ \mu\text{m}$, et avec un pas inférieur à $10\ \mu\text{m}$. Des simulations analytiques et numériques ont montré que ces contacts nanométriques sont avantageux pour les cellules en silicium cristallin. En effet ces contacts peuvent entraîner une résistance ohmique négligeable tout en gardant des valeurs acceptables de $S_{\text{eff, rear}}$ du moment que la vitesse de recombinaison dans le contact (S_{cont}) est entre 10^3 et 10^5 cm/s.

Mon travail expérimental était focalisé sur le développement de ces contacts en utilisant des nanoparticules de polystyrène comme un masque afin de pouvoir former ces contacts nanométriques à moindre coût.

La thèse a été divisée en trois parties. Dans la première partie, trois méthodes de déposition (spray-coating, spin-coating, et floating transfert technique) de particules étaient testées. Les deux premières méthodes de déposition donnent une distribution mal contrôlée de particules avec des faibles taux de couverture. En utilisant la technique de floating transfert, une monocouche dense de nanoparticules s'est formée. Cela nécessite une gravure par plasma de O_2 afin de réduire les taux de couverture. Cette gravure était faite et étudiée en utilisant la technique de plasmas matriciels distribués à résonance Cyclotronique Electronique (MD-ECR). De même, le retrait des particules, après avoir déposé une couche métallique ou diélectrique, était étudié.

Dans la deuxième partie de la thèse, trois approches différentes ont été développées pour former des contacts locaux sur des substrats métalliques et de silicium cristallin. La première approche (Approche A) utilise les nanoparticules comme un masque direct, par exemple en dispersant les NPs sur un substrat, suivi par un dépôt de SiO_2 ou Si_3N_4 par PECVD sur les NPs, et enfin le retrait des particules. La deuxième approche consiste à déposer un deuxième masque sur les NPs. Cela a été fait en évaporant de l'aluminium sur le SiO_2 thermique comme un masque pour gravure plasma (Approche B), et le $\text{a-SiC}_x\text{:H}$ déposé par PECVD sur l' Al_2O_3 comme un masque pour gravure chimique humide (Approche C). J'ai testé les nanotrous formés par approche A sous forme de contacts nanométriques pour des cellules solaires NIP a-Si:H. Des contacts nanométriques, de diamètre inférieur à $100\ \text{nm}$, étaient répartis de façon homogène dans le réflecteur arrière de la cellule solaire avec une distance moyenne de $350\ \text{nm}$ entre les contacts. Les propriétés électriques des NIP a-Si:H avec des contacts nanométriques étaient comparés à la même cellule solaire faite avec un diélectrique sans nanotrous et à celle faite sans la couche de diélectrique.

Dans la troisième partie de la thèse, j'ai étudié l'usage des nanotrous pour la technique de silicium cristallin qui a provoqué la formation de contacts dopés à travers les nanotrous en utilisant l'approche B. Un dopage de bore était fait par diffusion thermique et implantation ionique. Une couche épaisse d'oxyde thermique était utilisée comme une barrière pour la diffusion et l'implantation. Ces échantillons étaient caractérisés par la microscopie électronique à balayage (MEB) et par la microscopie à force atomique à pointe conductrice (CP-AFM). Un dopage local a été observé par CP-AFM en mesurant des courbes de courant-tension à l'intérieur et à proximité des zones dopées. Ce dopage local été davantage mis en évidence en observant des cellules solaires nanométriques. Pour les échantillons implantés, un procédé de recuit rapide (RTA) a changé radicalement l'apparence des échantillons vue par MEB. Malgré la formation des diodes, le processus d'implantation ionique a besoin d'être optimisé afin de produire des résultats similaires aux échantillons ou le dopage a été fait par diffusion.

Pour conclure, le travail présenté dans ce manuscrit consiste à développer et à explorer une technique à bas coût afin de pouvoir former des contacts nanométriques pour des dispositifs optoélectroniques. Des techniques de création de trous ont été développés, décrits et testés dans des structures de silicium cristallin et de couches minces.

Titre : Mise en œuvre de procédés de contacts nanométriques pour des dispositifs photovoltaïque à base de silicium

Mots clés : Nanoparticules de polystyrène, Nanostructures, Dopage, Silicium cristallin, Couches minces, La microscopie à force atomique à pointe conductrice.

Résumé: Au cours de cette thèse, j'ai étudié la possibilité et les avantages d'utiliser des contacts nanométriques au-dessous de 1 μm . Des simulations analytiques et numériques ont montré que ces contacts nanométriques sont avantageux pour les cellules en silicium cristallin comme ils peuvent entraîner une résistance ohmique négligeable. Mon travail expérimental était focalisé sur le développement de ces contacts en utilisant des nanoparticules de polystyrène comme un masque. En utilisant la technique de floating transfert pour déposer les nanosphères, une monocouche dense de nanoparticules s'est formée. Cela nécessite une gravure par plasma de O_2 afin de réduire la zone de couverture des NPs. Cette gravure était faite et étudiée en utilisant la technique de plasmas matriciels distribués à résonance cyclotronique

Electronique (MD-ECR). Une variété de techniques de créations de trous nanométriques était développée et testée dans des structures de couches minces et silicium cristallin. Des trous nanométriques étaient formés dans la couche de passivation, de SiO_2 thermique, du silicium cristallin pour former des contacts nanométriques dopés. Un dopage local de bore était fait, à travers ces trous nanométriques par diffusion thermique et implantation ionique. En faisant la diffusion, le dopage local était observé par CP-AFM en mesurant des courbes de courant-tension à l'intérieur et à l'extérieur des zones dopées et en détectant des cellules solaires nanométriques. Par contre le processus de dopage local par implantation ionique a besoin d'être amélioré afin d'obtenir un résultat similaire à celui de diffusion.

Title : Nanometer scale point contacting techniques for silicon Photovoltaic devices

Keywords : Polystyrene Nanoparticles, Nanostructure, Doping, crystalline silicon, Thin film, Conducting Probe Atomic Force Microscopy.

Abstract: In this PhD work, I explore the possibility and potential advantages of using nanoscale contact openings in the range of 1 μm or below. Analytic and numerical simulations have shown that such nanoscale contacts are advantageous for crystalline silicon technology as it would result in negligible ohmic losses. My experimental work has focused on achieving such contacts using polystyrene nanospheres as a sacrificial mask. The floating transfer technique provided a densely-packed monolayer of NPs on the surface which necessitated an additional O_2 plasma step to reduce the coverage area of the spheres. This was performed and studied using a matrix distributed electron cyclotron resonance (MD-ECR) plasma.

A number of hole-creating techniques are developed, described, and deployed in test structures involving thin-film and crystalline silicon. I investigate the use of such nanoholes in crystalline silicon technology by the formation of doped contacts through nanoholes. Boron doping by both thermal diffusion and ion implantation were used to dop locally through the nanoholes. For the diffused samples, localized doping was indeed observed through CP-AFM by acquiring current-voltage curves both within and beside the doped area with the observation of nanoscale solar cells. For the ion implantation samples, the process needs further refining to produce the same results as diffusion.