# III-V/Si tandem solar cells : an inverted metamorphic approach using low temperature PECVD of c-Si(Ge)

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Par

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## III-V/Si tandem solar cells: an inverted metamorphic approach using low temperature PECVD of c-Si(Ge) on GaAs

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| | | | |
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# Abstract

Combining silicon with III-V materials represents a promising pathway to overcome the ~29% efficiency limit of a single c-Si solar cell. While the standard approach is to grow III-V materials on Si, this work deals with an innovative way of fabricating tandem solar cells. We use an inverted metamorphic approach in which crystalline silicon or SiGe is directly grown on III-V materials by PECVD. The low temperature of this process (<200 °C) reduces issues due to the difference in thermal expansion coefficient. Also, growing the group IV material on the III-V prevents polarity issues.

The realization of the final tandem solar cell made of SiGe/AlGaAs requires the development and optimization of various building blocks. First, we develop the epitaxy at 175°C of Si(Ge) on (100) Si substrates in an industrial standard RF-PECVD reactor. We prove the promising electrical performances of such grown Si(Ge) by realizing heterojunction solar cells with 1.5 µm epitaxial absorber leading to a $V_{oc}$ up to 0.57 V. We show that the incorporation of Ge in the layer increases the $J_{sc}$ from 15.4 up to 16.6 A/cm² ($SiGe_{25\%}$).

Then, the hetero-epitaxy of Si on GaAs by PECVD is studied. c-Si exhibits excellent structural properties, and the first stages of the growth are investigated by X-ray diffraction with synchrotron beam. We find an unexpected behavior: the grown Si is fully relaxed, but tetragonal. While the GaAs lattice parameter is higher than that of silico, we find a higher out-of-plane Si parameter ($a_{\perp}$), due to the high hydrogen content in the layer, but also a smaller in-plane parameter ($a_{//}$) than the theoretical one. This low $a_{//}$ is probably due to thermal stress induced by the substrate, and led us to the hypothesis that the temperature during the growth is well above the nominal value. Hereby, we may have found an experimental proof that PECVD growth happens thanks to local heating during the growth.

Meanwhile, we built a know-how in a new technological field in the III-V Lab: photovoltaics. We developed materials for AlGaAs solar cells by MOVPE, as well as their full grid design and process flow in clean rooms. We could reach a high efficiency of 17.6 % for a $Al_{0.22}Ga_{0.78}As$ solar cell, being thus suitable for its integration in the tandem solar cell. Also, materials to grow tunnel junctions (TJ) were studied, and in particular the n-doping of GaAs with DIPTe precursor to obtain doping levels above $2.7x10^{19}$ $cm^{-3}$. While good TJs were obtained with standard n-doping with Si, Te doping led to TJs with peak tunneling currents up to 3000 A/cm², reaching state-of-the art. Moreover, by studying the integration of PECVD with III-V materials, we found that hydrogen plays a strong role in GaAs: its doping level is decreased by one order of magnitude when exposed to a $H_2$ plasma, due to the formation of complexes between H and the dopants (C, Te, Si). Fortunately, this behavior can be recovered after 3 minutes annealing at 350°C.

Finally, the last step of device fabrication is studied: the bonding on a host substrate. We successfully bonded an inverted AlGaAs cell, removed it from its substrate, and processed a full 2" wafer. We succeeded in growing our first tandem solar cells by growing thick layers (> 1 µm) of Si on inverted AlGaAs solar cells followed by a TJ. Finally, we study the bonding and substrate removal of this final device, being the first tandem solar cell grown by inverted metamorphic growth of Si on III-V.

**Keywords: Epitaxy, PECVD, MOVPE, Heteroepitaxy, Tandem Solar Cells, III-V/Si, Tunnel Junctions**

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# Résumé

La limite théorique d'efficacité d'une cellule solaire simple jonction est de ~29 %. Afin de dépasser cette limite, une des moyens les plus prometteurs est de combiner le silicium avec des matériaux III-V. Alors que la plupart des solutions proposées dans la littérature proposent de faire croître directement le matériau III-V sur substrat silicium, ce travail présente une approche innovante de fabriquer ces cellules solaires tandem. Nous proposons une approche inverse métamorphique, où le silicium cristallin ou SiGe est cru directement sur le matériau III-V par PECVD. La faible température de dépôt (< 200 °C) diminue les problèmes de différence de dilatation thermique, et le fait de croître le matériau IV sur le matériau III-V élimine les problèmes de polarité.

La réalisation de la cellule tandem finale en SiGe/AlGaAs passe par le développement et l'optimisation de plusieurs briques technologiques. Tout d'abord, nous développons l'épitaxie à 175 °C de Si(Ge) sur des substrats de Si (100) dans un réacteur de RF-PECVD industriel. La réalisation de cellules solaires à hétérojonction à partir de ce matériau Si(Ge) crû par PECVD montre que ses performances électriques s'avèrent prometteuses. Nous obtenons pour un absorbeur de 1.5 µm des Voc qui atteignent 0.57 V. L'incorporation de Ge permet d'augmenter le $J_{SC}$ de 15.4 % jusqu'à 16.6 A/cm² pour $Si_{0.72}Ge_{0.28}$.

En parallèle, la croissance de cellules solaires AlGaAs a été développée, ainsi que sa fabrication technologique. Nous obtenons une efficacité de 17.6 % pour une cellule simple en $Al_{0.22}Ga_{0.78}As$. Nous développons aussi des jonctions tunnel, parties essentielles d'une cellule tandem dans une configuration à deux terminaux. Nous développons notamment le dopage n du GaAs en utilisant le précurseur DIPTe, et obtenons des jonctions tunnel ayant des courants pic atteignant jusqu'à 3000 A/cm², rejoignant ainsi les résultats de l'état de l'art.

Ensuite, nous étudions l'hétéro-épitaxie de Si sur GaAs par PECVD. Le c-Si montre d'excellentes propriétés structurales. Les premiers stades de croissance sont étudiés par diffraction des rayons X avec rayonnement synchrotron. Nous trouvons un comportement inattendu : le Si est relâché dès les premiers nanomètres, mais sa maille est tétragonale. Alors que le GaAs a un paramètre de maille plus grand que le Si, le paramètre hors du plan ($a_{\perp}$) du Si est plus élevé que son paramètre dans le plan ($a_{//}$). Nous trouvons une forte corrélation entre cette tétragonalité et la présence d'hydrogène dans la couche de silicium. D'autre part, nous montrons que le plasma d'hydrogène présent lors du dépôt PECVD affecte les propriétés du GaAs : son dopage diminue d'environ un ordre de grandeur lorsque le GaAs est exposé au plasma H2, dû à la formation de complexes entre le H et le dopant (C, Te ou Si). Le dopage initial peut être retrouvé après un recuit à 350 °C. Enfin, nous étudions la dernière étape de fabrication de la cellule tandem : le collage. Nous avons pu reporter une cellule simple inversée en AlGaAs sur un substrat hôte (en Si), retirer le substrat GaAs et effectuer les étapes de microfabrication sur un substrat 2 pouces. Des couches épaisses de Si (>1 µm) ont été crues avec succès sur une cellule AlGaAs inversée suivie d'une jonction tunnel. Le collage de cette cellule tandem, et le processus de fabrication technologique du dispositif final sont ensuite étudiés, afin de pouvoir caractériser électriquement la première cellule solaire tandem fabriquée par croissance inverse métamorphique de Si sur III-V.

**Keywords: Epitaxie, PECVD, MOVPE, Heteroepitaxie, Cellules solaires tandem, III-V/Si, Jonctions tunnel**

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Merci à tous, et bonne lecture

Gwen

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**Chapter III: PECVD heteroepitaxy of Si on GaAs**



**Chapter IV: Tunnel junctions**

**Chapter V: III-V processing and bonding: towards inverted metamorphic tandem solar cells**

# List of Acronyms

| Acronym | Unit | Definition |
|---|---|---|
| $a_{\perp}$ | | Out-of-plane lattice parameter |
| $a_{//}$ | | In-plane lattice parameter |
| AFM | | Atomic Force Microscopy |
| ARC | | anti-reflective coating |
| As, P | | Arsenide, Phosphorus (group V) |
| a-Si:H | | Hydrogenated amorphous silicon |
| BCB | | Benzocyclobutene |
| BSF | | Back surface field |
| c-Si | | c-Si crystalline silison |
| CTE | | Coefficient of thermal expansion |
| CPV | | Concentrator PhotoVoltaics |
| DETe | | DiEthyl-Telluride |
| DIPTe | | DIPTe diisopropyl telluride |
| FF | % | Fill factor |
| FWHM | | Full width at half maximum |
| Ga, In, Al | | Gallium, Indium, Aluminium (group III) |
| GI-XRD | | Grazing Incidence X-ray diffraction |
| HR-XRD | | High Resolution X-ray diffraction |
| IBE | | Ion Beam etching |
| ICP | | Inductively Coupled Plasma |
| ITO | | Indium Tin Oxide |
| $J_{peak}$ | $A/cm^2$ | Peak Tunneling Current |
| $J_{SC}$ | $A/cm^2$ | Short-circuit Current |
| J-V | | Current Density versus Voltage |
| MBE | | MBE : Molecular beam epitaxy |
| MJSC | | Multijunction Solar Cells |
| MOVPE | | Metalorganic Vapor Phase Epitaxy |
| $N_{eff}$ | $cm^{-3}$ | Effective Doping Level |
| PECVD | | Plasma-Enhanced Chemical Vapor Deposition |
| PV | | Photovoltaic |
| RIE | | Reactive Ion Etching |
| RMS | | Root Mean Square |
| $R_s$ | Ω | Series Resistances |
| $R_{sh}$ | Ω | Shunt Resistances |
| RSM | | Reciprocal Space Mapping |
| RTA | | Rapid Thermal Annealing |
| sccm | | sccm : Standard Cubic Centimeters per Minute |
| SEM | | Scanning Electron Microscopy |
| SIMS | | SIMS : Secondary Ion Mass Spectrometry |
| Surfactant | | Surface Activating Agent |
| TDD | $cm^{-2}$ | Threading Dislocation Density |
| TJ | | Tunnel Junction |
| TMB | | Tri Methyl Boron |
| $V_{OC}$ | V | Open-Circuit Voltage |
| µc-Si:H | | Hydrogenated microcrystalline silicon |

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Chapter I

# Introduction

## Content

In this introduction chapter, we present today's new challenges in photovoltaic technologies for reaching high efficiencies. We focus on the multi-junction solar cells (MJSC), and the main laboratory records up to now. We then present the various approaches for fabricating tandem solar cells using a Si subcell: growth of III-V on Si substrate, bonding of the 2 subcells… Among the various pathways that are explored in literature, we present the innovative approach of this PhD thesis, its advantages, and its challenges that are the subject of this manuscript.

# I.1. PV technologies

## I.1.1. Introduction

Since the very first silicon solar panel manufactured by Bell Labs in 1954 that reached 5 % efficiency, lots of progress have been done in the photovoltaic (PV) field. Silicon-based technologies have always been and remain the most important player of the PV industry. In 2015, 93 % of the total PV production comes from Si-wafer based PV technology[1]. The efficiency record for c-Si solar cells has not substantially evolved since the 90's, but the drastic cost reductions due to mass production and technological improvements led to a strong and cheap industry, and an energy that starts being competitive with conventional energies. While nowadays, efforts are still done to improve Si cells efficiency by minimizing the shadow losses due to front contacts and reducing the surface recombination losses, the technology has almost reached its maximum theoretical efficiency. The most recent record reported is of 26.7 %[2] under AM1.5G, approaching the 29% theoretical maximum efficiency stated in 1961 by Shockley and Queisser[3]. AM1.5G is a reference used as a standard irradiance to compare terrestrial solar cells and modules. It corresponds to the terrestrial sun irradiance at an angle elevation of 48.2°, as depicted in Figure 1.1.a. The atmosphere at this elevation absorbs and scatters the solar radiation, and attenuates the solar spectrum to an irradiation of 1000 $W.m^{-2}$. The AM1.5 Global spectrum is designed for flat plate. The AM1.5 Direct spectrum is defined for solar concentrator work. It includes the direct beam from the sun plus the circumsolar component in a 2.5 degrees disk around the sun. The AM1.5D spectrum has an integrated power density of 900 $W.m^{-2}$. AM0 is the convention for spatial applications. The solar power density in space is roughly 1350$W.m^{-2}$. In this work, we will mainly use the AM1.5G spectrum.

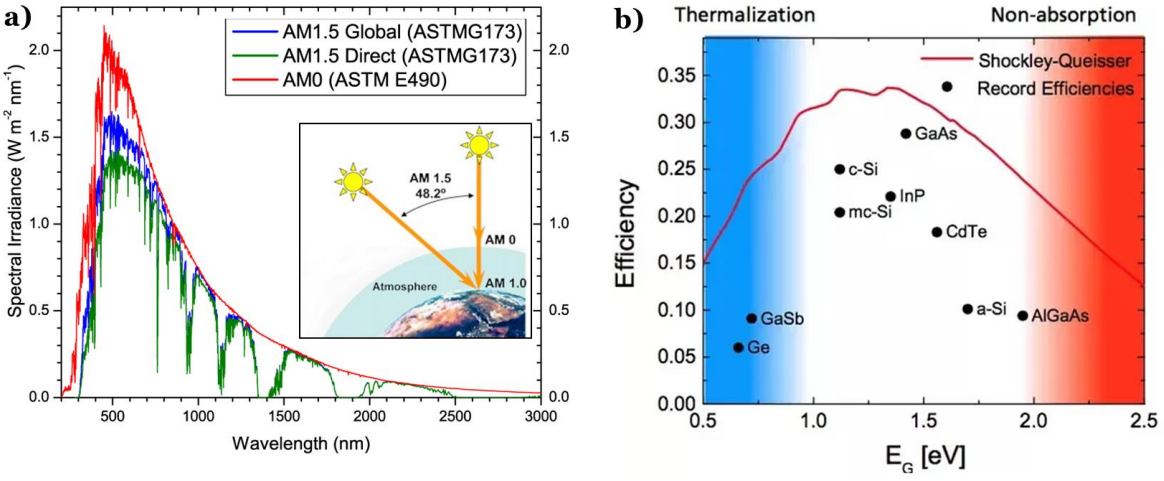



**Figure 1.1 - a) Incident spectral irradiance from the sun for terrestrial applications (AM1.5G and AM1.5D) and space applications (AM0). b) Schockley-Queisser limit: maximum theoretical efficiency of a solar cell as a function of its bandgap, along with the best experimental efficiencies**

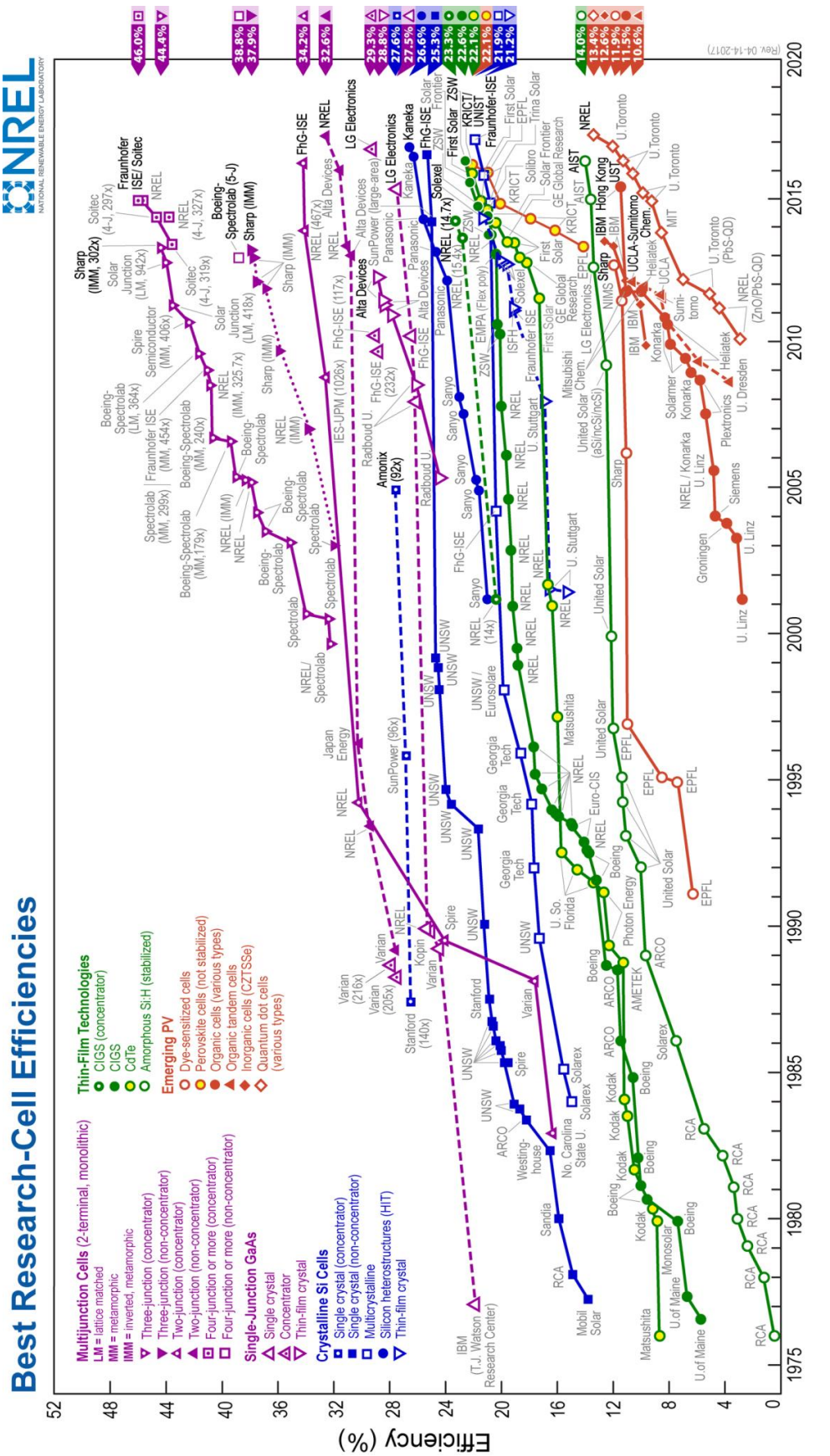



**Figure 1.2 - NREL chart with time evolution of best research cell conversion efficiency for different technologies**[4]

However, when commenting the cells manufactured for spatial application, AM0 will be used. Shockley-Queisser (SQ) limit is illustrated in Figure 1.1.b. It shows the maximum theoretical efficiency as a function of the material bandgap. The best experimental single-junction solar cells are reported on the graph. It shows that solar cells with a bandgap between 1 and 1.5 eV are theoretically well suited for high efficiency. This includes Si, GaAs and InP materials. Experimental solar cells are still way below their theoretical efficiencies, mainly because of issues due to series resistance, contact shadowing, or parasitic recombination.

The evolution of the record conversion efficiency of solar cells since 1975 up to now is pictured in the NREL chart[4] Figure 1.2. Silicon technology is plotted in blue. Many new technologies are being explored, such as the promising perovskites, or thin film technologies (CIGS, CdTe, amorphous Si…). Thin films are now getting close to 25 % energy conversion efficiency, but the drawbacks of these materials remain their scarcity, and in some case their toxicity. Perovskites show a spectacular progression rate, but are limited by their stability over time and light degradation.

## I.1.2. Overcoming Shockley-Queisser limit: multi-junction solar cells (MJSC)

Figure 1.3.a. shows the AM1.5G spectrum irradiance of the sun, along with the part of the spectrum that is actually absorbed by a Si single solar cell. Shockley-Queisser limit is explained by two main types of losses. First, the transmission losses, that corresponds to the photons for which Si is transparent. All the photons with energy lower than the semi-conductor bandgap energy (i.e. a higher wavelength) will not be absorbed. Second, the thermalization losses are due to the photons that have a too high energy compared to the bandgap, and thus dissipate the extra energy into heat. In order to overcome the Shockley-Queisser[3] theoretical limit of a single junction from, several concepts have been proposed, such as the use of intermediate band and hot carrier solar cells. But one of the most efficient concepts to go beyond the 30 % limit is the multi-junction solar cell (MJSC)[5]. Concentrating the light on a solar cell by adding lenses could lead to even higher conversion efficiencies. MJSC consist in using several absorbers with different bandgaps. The highest bandgap cell (i.e. the most transparent) is placed on top of the smaller bandgap solar cells. That way, each solar subcell is dedicated to harvest one part of the solar spectrum, thus minimizing the thermalization[6]. As an example, Figure 1.3.b. shows the AM1.5G solar spectrum along with the part of the spectrum that can be absorbed by a triple junction GaInP/GaInAs/Ge. The transmission

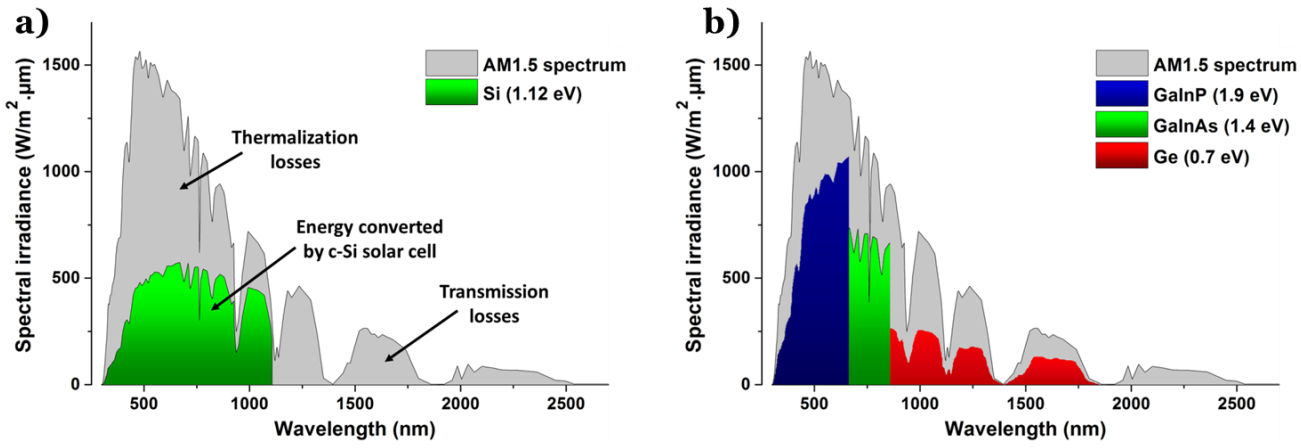



**Figure 1.3- AM1.5G spectrum and the fraction theoretically converted by a) a Si solar cell, b) a triple junction GaInP/GaInAs/Ge (from ref [9])**

losses are lowered due to the use of Ge which has a lower bandgap than Si (0.67 eV instead of 1.12 eV). Only the photons with energy below 0.67 eV will be transmitted. The thermalization losses are reduced thanks to the sorting of the photons by their energies. First, the photons of energies above GaInP bandgap (1.9 eV) will be absorbed by the first subcell. Then, the photons with energies above 1.4 eV will be absorbed by the GaInAs subcell, and finally, Ge will absorb the rest of the photons with energies above its bandgap. Thus, it is not likely that a high energy photon (> 1.9 eV) reaches the Ge subcell and thermalizes.

Two main ways of connecting the subcells can be distinguished: the two-terminal approach, and the four-terminal one. In the two-terminal stacking, the subcells are connected in series, and the current is collected only at the front and at the back of the solar cell. In this configuration, the two subcells are electrically connected in series, by means of tunnel junctions (TJ). TJ are highly doped p-n junctions that will allow the carriers to flow from one subcell to the other by tunneling effect. TJ should be as transparent as possible, thus very thin (a few tens of nanometers), with the highest bandgap. As the subcells are connected in series, particular attention needs to be paid on the current matching. Indeed, if a subcell has a smaller current than the other, it will limit the whole multi-junction solar cell current. Thus, the bandgap and thickness of each subcell has to be carefully adapted in order to obtain the best current matching, leading to the best efficiency. Furthermore, this approach requires a monolithic integration of the materials. Thus, the crystalline lattice-matching of the materials is another important issue, which will be discussed in the following sections. In the four-terminal approach, the carriers generated by each subcell are independently collected. It allows a wider choice of materials, because it allows stacking materials with different lattice parameters without introducing losses due to dislocations. However, it requires the addition of a conductive layer in the middle of the solar cell, which will add some absorption losses. Recently it has also been proposed to perform three-terminal multi-junctions[7].

Theoretically, the more subcells with different bandgaps, the higher the efficiency. For infinite number of junctions, the theoretical efficiency of multi-junction solar cells reaches 86.8%[8–10]. Figure 1.4 shows the theoretical efficiency as a function of the number of subcells, along with the bandgap combination to reach such efficiency (from an NREL lecture[11]). A 4-junction solar cell can theoretically reach an efficiency above 55 %, we must find the adequate 4 materials that have the right 4 bandgaps. But in real configuration, materials with different bandgaps do not necessarily have similar lattice parameters.

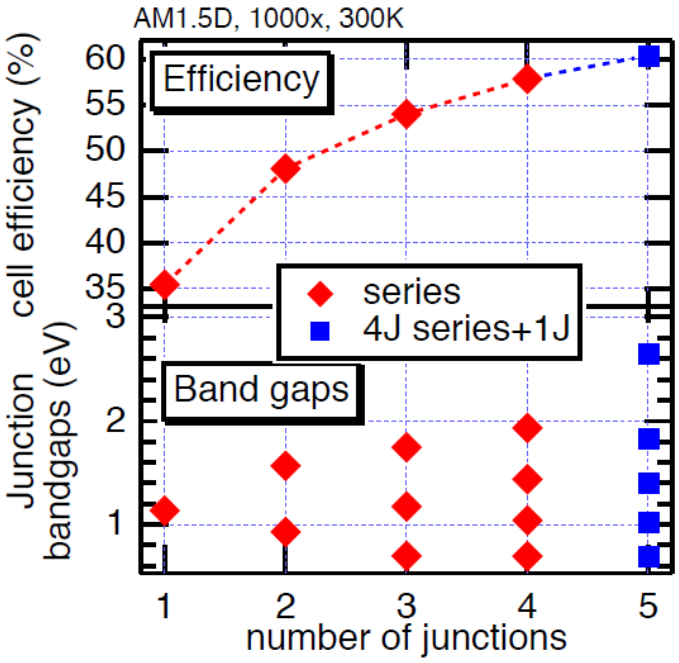



**Figure 1.4 - Theoretical maximum efficiency of a multijunction as a function of the number of junctions, along with the corresponding bandgaps (NREL) [11]**

Figure 1.5 shows a list of available materials, with their lattice parameters and their bandgap, including the main III-V alloys, as well as Si and Ge. One can notice a wide disparity in bandgaps and lattice parameters. We see that Ge is almost lattice-matched with GaAs, hence the use of Ge as a substrate for most multi-junction solar cells based on GaAs family compounds. By following the vertical line between GaAs and AlAs, the $Al_xGa_{1-x}As$ family allows tuning the bandgap, while remaining almost lattice-matched with GaAs and Ge. However, most of the other materials have their own lattice parameter. Lattice-mismatch induces dislocations, grain boundaries or other types of impurities, that will highly reduce the efficiency [9].

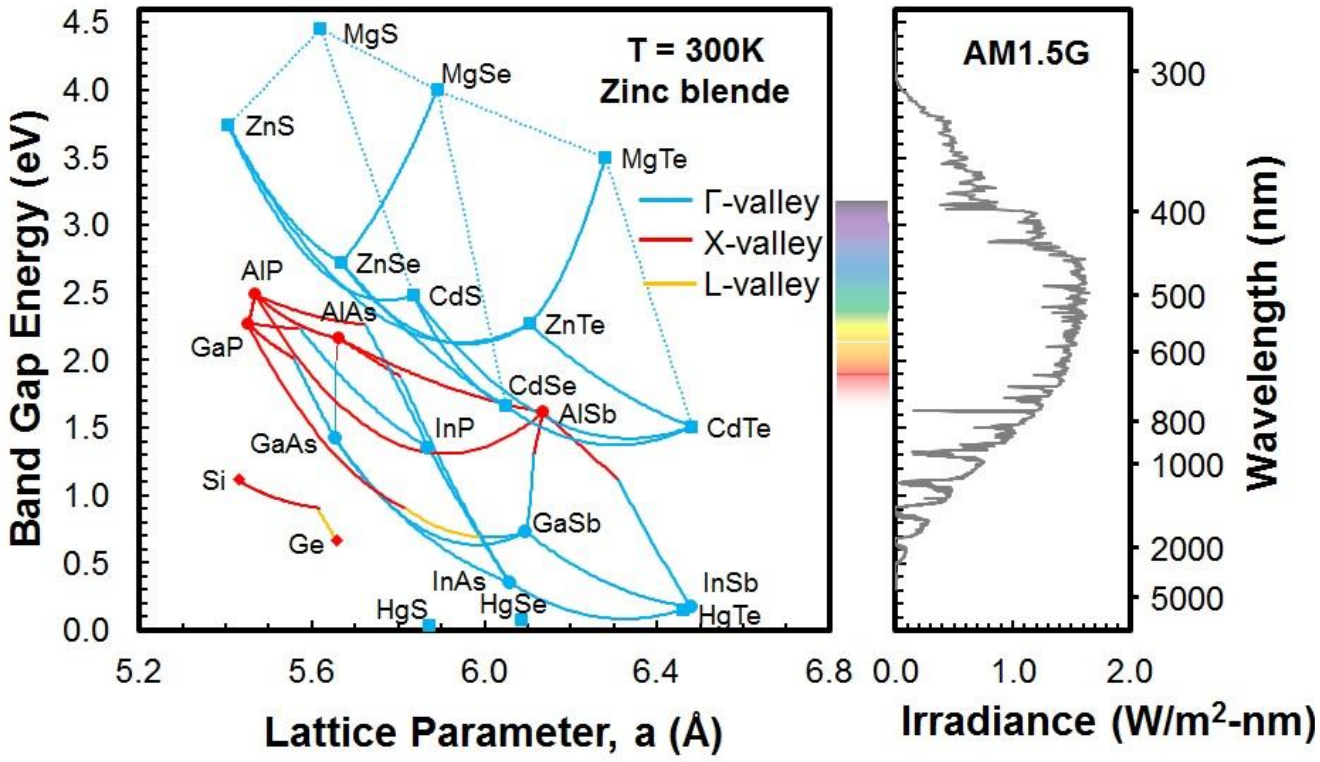



**Figure 1.5 - Bandgap versus lattice constant at room temperature for various materials including Si, Ge, GaAs.**

Most of the research has been focused on the growth of lattice-matched materials, which are the easiest to manufacture. The very mature industry of high quality of III-V materials along with their strong absorption due to their direct bandgap gives to this type of materials the best properties for MJSC. It is also possible to use lattice mismatched materials by means of wafer bonding, or by using buffer layers. These technical paths are discussed in the following part.

## I.1.2. Multi-junction solar cells: review

Multi-junction solar cells based on III-V materials hold the highest efficiency record. They correspond to the purple data plot in the NREL efficiency chart presented in Figure 1.2. It is the only technology that reached and overcame 30 % of efficiency. For example, 3-junction solar cells efficiency has increased by about 1% absolute per year since 2002. The graph also shows how using concentrating photovoltaics can boost the conversion efficiency of a III-V MJSC. The last 3-JSC record at one sun is reported to be 37.9 %[12], while under concentration (302 sun) it reached 44.4%[13].

This latest record uses an inverted metamorphic triple junction of InGaP/GaAs/InGaAs. 4-junction solar cells from NREL reached 45.7% for a monolithic GaInP/GaAs/GaInAs/GaInAs[14], and was recently overpassed by Fraunhofer ISE/CEA/Soitec that reached 46.0 % by bonding monolithic GaInP/GaAs with monolithic GaInAs/GaInAs[15]. The record multi-junction solar cells are gathered in Table 1.1. In terrestrial and space industry, the most widely manufactured triple junction is grown on a Ge substrate. Among the commercialized MJSC, the record is held by Spectrolab with an efficiency of 41.3% under 364 suns[16]. It consists of a lattice matched GaInP/GaInAs/Ge solar cell grown on a Ge substrate by metalorganic vapor phase epitaxy (MOVPE). GaInP and GaInAs are lattice-matched with Ge, leading to a high quality III-V material. The bandgap combination is however not optimal, as the Ge cell generates more current than the two upper cells, but it remains the easiest MJSC to produce for concentrator photovoltaic (CPV) applications. The use of concentration not only enables to enhance the efficiency of the cells, but also to reduce their size, thus the amount of material needed to harvest solar energy. However, in addition to the high price of Ge or GaAs substrate and of deposition and manufacturing of the cell, the optics and tracking systems are also quite expensive[17]. Thus, multi-junction III-V solar cells under concentration hold by far the records in efficiency, but remain very expensive. That is the reason why alternative ways of manufacturing high efficiency solar cells at lower cost must be investigated. The most significant contributors to the cost are the substrate used, which are made of Ge or GaAs. To reduce cost, the use of a most common and much cheaper material would be required.

| #Junctions | Substrate | Ref | Materials (From bottom to top) | Approach | #Suns | Efficiency |
|---|---|---|---|---|---|---|
| 3 | Ge | Guter | Ge/InGaAs/InGaP | Lattice-matched | 454 | 41,1 % |
| 3 | InP | Lumb | InGaAsNSb/GaAs/GaInP | Upright lattice-matched | 690 | 44,1% |
| 3 | GaAs | Sharp | InGaAs/GaAs/InGaP | Inverted metamorphic | 306 | 44,4 % |
| 4 | GaAs | NREL | GaInAs/GaInP/GaAs/GaInP | Inverted metamorphic | 234 | 45,7 % |
| 4 | GaAs + InP | Fraunhofer ISE+ SOITEC+CEA LETI | GaInAs/GaInAsP // GaAs/GaInP | Wafer-bonded | 508 | 46 % |

**Table 1.1 - Summary of III-V 3-junction and 4-junction solar cells records.([16,13,14,15])**

# I.2. Integration of III-V with Si:

## I.2.1. Motivations for the integration on Si

The use of a Si substrate for III-V materials, together with the mature technology of Si PV industry would considerably reduce the costs. Besides the use of a Si substrate as a non-active material, using a Si active subcell would be of high interest for multi-junction solar cells. With a bandgap of 1.12 eV, a theoretical efficiency over 42 % can be expected for a tandem structure. Figure 1.6.a., from Connoly *et al.*[18], shows the theoretical efficiencies for a tandem junction as a function of top cell and bottom cell bandgaps, when connected in series. Two main maxima are observed: for a bandgap combination of 0.96eV/1.64 eV, 42.2% is expected. Interestingly, the second optimum corresponds

to the combination of Si (bandgap of 1.12 eV) with a material that has a 1.74 eV bandgap. The resulting tandem solar cell would have a conversion efficiency of 41.9%. Among the assumptions of the model, it is supposed that the bottom Si cell has a quantum efficiency of 1, meaning that it absorbs all the photons whose energy is above Si bandgap. Figure 1.6.b. shows the calculations for a 3-junction solar cell with a Si middle cell. The ideal bottom cell and top cell bandgap are found to be 1.74 eV and 0.53 eV for an efficiency of 45.4%.

While looking at the possible materials gathered in Figure 1.5, there is unfortunately no material with a bandgap around 1.74eV that is lattice matched with Si. GaP has a lattice parameter close to that of Si, however its bandgap is too high (2.26 eV). Thus, the integration of III-V materials with the right bandgaps with Si is a challenging issue. While various top cell candidates have been discussed in literature[19], the main current research focuses on perovskites and III-V materials. Furthermore, lattice-mismatch is not the only practical challenge faced in III-V/Si integration. Those challenges are detailed in the next section, together with the different pathways that are being investigated in the field of III-V/Si integration.

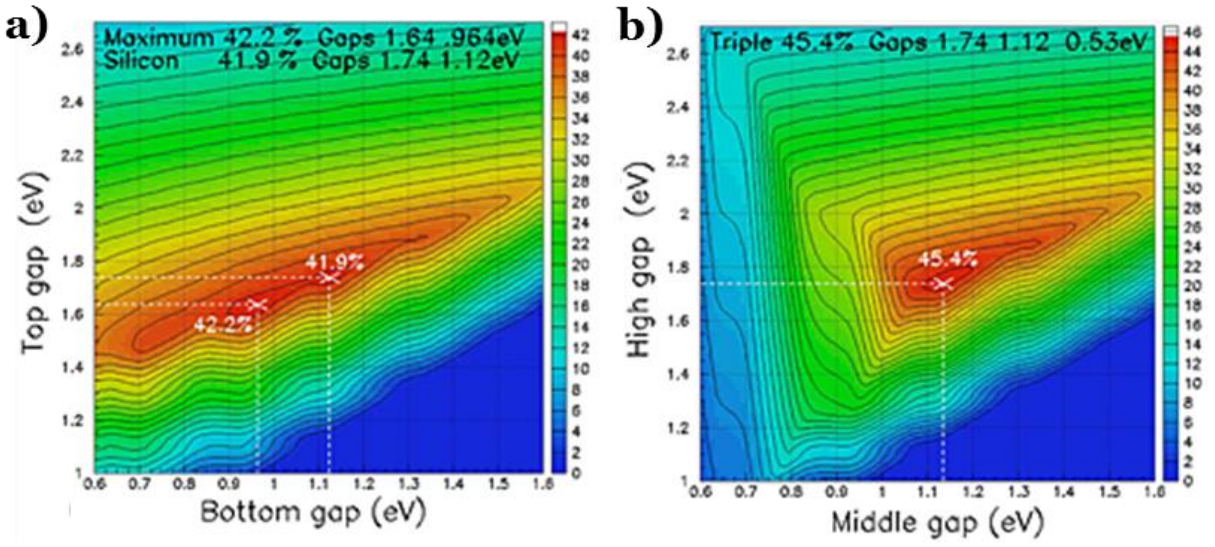



**Figure 1.6 - a) Theoretical efficiencies for a tandem junction as a function of top cell and bottom cell bandgaps, when connected in series b) Theoretical efficiencies for a triple junction as a function of top and middle bandgap subcells. (Connolly et al. [18])**

## I.2.2. Main challenges of integrating III-V on Si

The research on integration of III-V on Si is has been a dream for semiconductor industry for the past 30 years. Lots of work have been performed for various applications, such as optoelectronics integrated circuits[20] by combining the optical advantages of III-V along with the mature technology of Si integrated circuits. Of course, the low cost of Si is also a way to produce lower cost devices such as LED or lasers[21]. In the photovoltaic field, the use of Si-based multi-junction solar cell will allow manufacturers to reach high efficiency while taking advantage of the low cost of Si, but also of their well-established expertise in Si production. But integrating III-V on Si is not that easy for three main reasons: first, the lattice mismatch between the considered materials, second the fact that III-V are polar materials while Si is non-polar, and third, the difference in thermal expansion.

***Lattice-mismatch:***

The III-V materials that have the optimum bandgap of 1.74 eV for a high performance tandem solar cell have, have the same cubic structure as Si, but they unfortunately have different lattice parameters, as deduced from Figure 1.5. Thus, growing a III-V epitaxial film on top of a Si substrate is challenging. In the case of GaAs material family, a lattice mismatch of 4% makes the epitaxy on Si very challenging due to the formation of defects and dislocations. Epitaxy refers to the formation of a new single crystal on top of a crystalline substrate. Two types of epitaxy can be distinguished: homoepitaxy, in which the grown layer is made of the same material as the substrate material, and heteroepitaxy, in which the grown material is different from the substrate. Figure 1.7.a. from a presentation of University of Waterloo[22], shows the case of homo-epitaxy, or heteroepitaxy with lattice-matched materials. In this case, no strain is induced, and the deposited atoms arrange perfectly on the atoms of the substrate. Figure 1.7.b. and c. show the possible configurations in case of epitaxy of a material that has a higher lattice-parameter than the substrate (as it is the case for GaAs on Si). If the epitaxial layer has a larger (respectively smaller) lattice parameter than the substrate, the layer can grow under in-plane compressive (resp. tensile) strain. Consequently, the out-of-plane parameter will be larger (resp. smaller) to ensure volume conservation. This is called pseudomorphic growth. However, after a critical thickness, the layer will relax into its stable configuration by creating crystalline defects. In this case, we talk about metamorphic growth. The relaxation of the epitaxial film induces dislocations and defects that will be responsible for a loss in crystalline quality and of electrical performances of the resulting solar cell. But the lattice mismatch is not the only issue in the growth of III-V materials on top of Si.

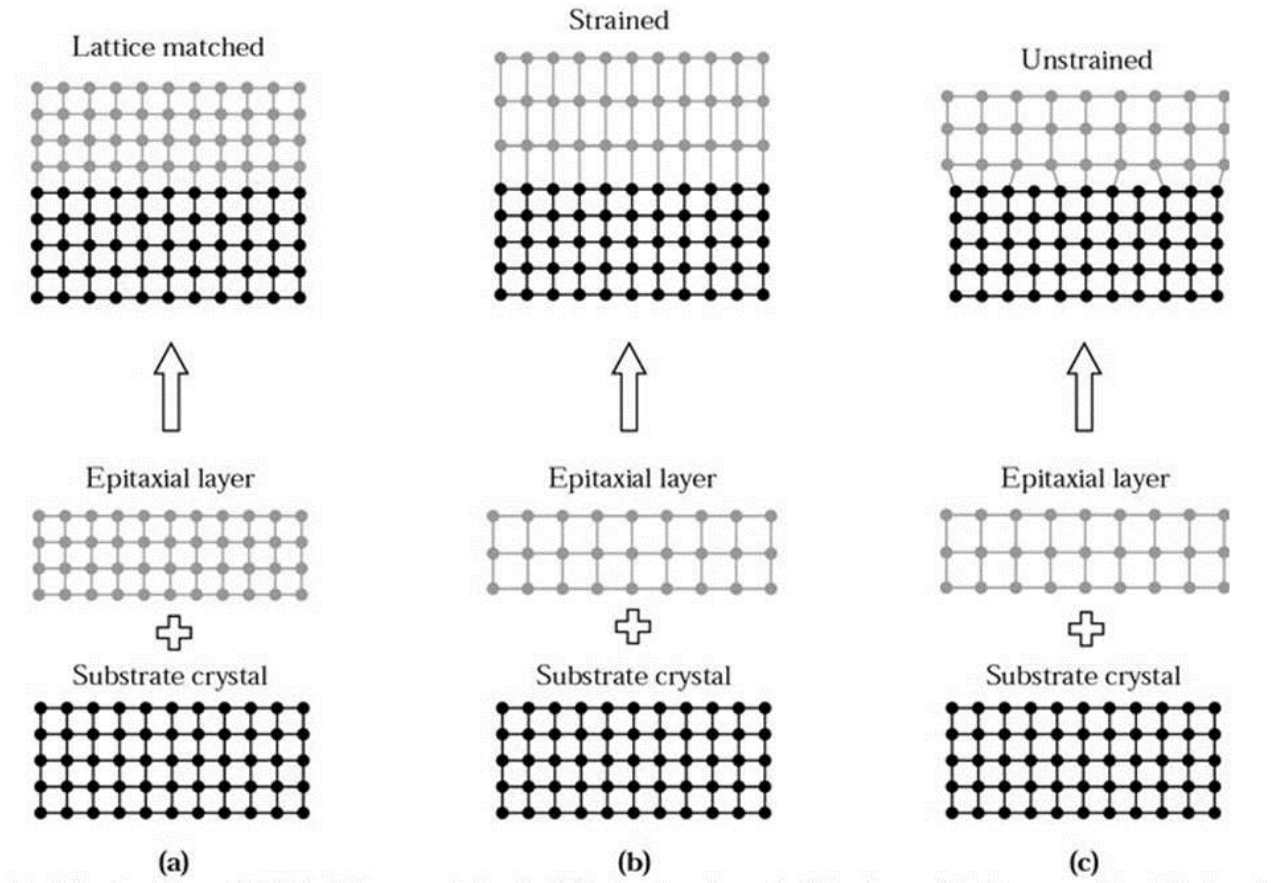



**Figure 1.7 - Schematic illustration of (a) lattice-matched, (b) strained and (c) relaxed hetero-epitaxial structures. (b) and (c) are shown in case of $a_{substrate} < a_{layer}$ ([22])**

***Polarity: growth of a polar III-V material on a non-polar Si substrate.***

Growing III-V materials, which consist of a superposition of a monoatomic layer of group III atoms followed by a monoatomic layer of a group V material, on a non-polar material such as Si, leads to the formation of antiphase domains (APDs). This is due to the fact that a (100) Si substrate surface does not consist of a perfectly flat surface. Figure 1.8 .a. from Freundlich[23] shows the case where a monoatomic step is found on the Si substrate. Monoatomic steps of Si are unavoidable at the surface of a substrate. During GaAs growth, first a monoatomic layer of As is deposited, followed by a Ga layer. Where the substrate contains a monoatomic step, it shifts the III and V steps, As covers one monoatomic step of the Si. The next Ga monolayer will thus lead to the formation of a Ga-Ga bond close to the step. During the growth, more Ga-Ga and As-As bonds will be formed, forming lines called antiphase boundaries (APB). Those electrically doubly charged defects are obviously not desired for the solar cell operation. It occurs when there is a single step on Si substrate, but not when there is an even step, as pictured in Figure 1.8 .b. When a step is actually a two-monolayer step, the alternation between Ga layer and As layer is respected. A solution that has been found is to use offcut Si substrate (4° - 6 °), to force the formation of double-layer steps instead of single layers[24].

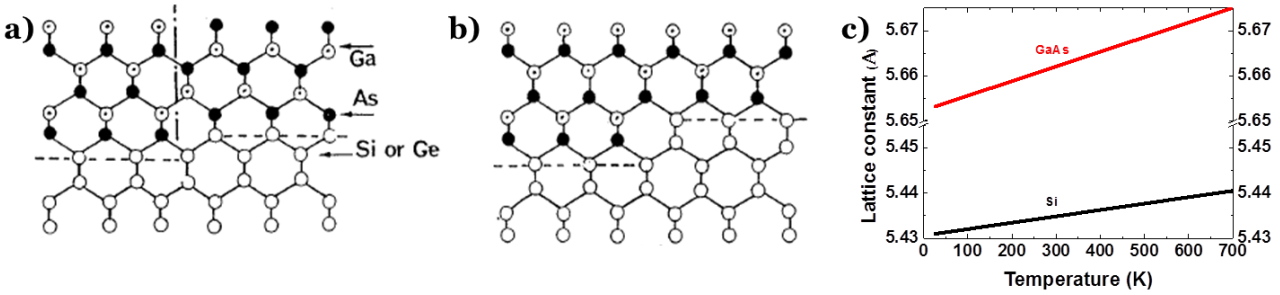



**Figure 1.8 - (a) Mechanism of APB formation during the growth of zinc blende structure on (100) non polar surface presenting single-atomic high step, (b) Growth of a single domain zinc blende structure on a (100) non polar surface presenting double-atomic high step (from Freundlich [23]) (c) lattice constant of GaAs and Si as a function of temperature**

***Thermal mismatch:***

In addition to the lattice parameter mismatch, and the APB formation, GaAs and Si also suffer from a difference in thermal expansion coefficient[25]. While GaAs has a coefficient of $5.73 \times 10^{-6}$ °C$^{-1}$, the value for Si is $2.6 \times 10^{-6}$ °C$^{-1}$. As the typical growth temperature for III-V epitaxy is rather high (above 600 °C for MOVPE), cooling down to room temperature after growth will induce thermal stress in the bulk heteroepitaxial layer, thus leading to the formation of additional defects and dislocations that lower the crystalline quality. Figure 1.8.c shows the lattice parameters of Si and GaAs as a function of temperature: GaAs varies more with temperature than Si. To reduce the formation of cracks, a good control of the cooling down is required, or to lower the growth temperature.

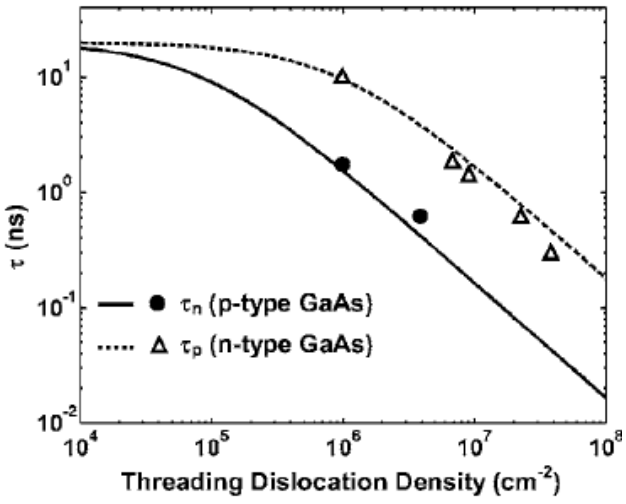



**Figure 1.9 - minority carrier lifetime in GaAs as a function of threading dislocation dislocation density (Andre et al. [26])**

Lattice mismatch combined with thermal mismatch leads to the formation of dislocations in the III-V material. Threading dislocations drastically reduce carrier mobility, as they act as recombination centers. Thus, solar cell performances are strongly reduced by the presence of threading dislocations. Figure 1.9 (from Andre *et al.*[26]) shows the minority carrier lifetime in GaAs as a function of threading dislocation density (TDD) in n-type GaAs and p-type GaAs. It shows that for a good solar cell operation, TDD should be kept below $10^6$ $cm^{-2}$. In case of p-type GaAs, TDD should even be lower than $10^5$ $cm^{-2}$ to ensure good minority carrier lifetime. Thus, reducing TDD is the main challenge in integrating III-V and Si. In the next section we will present the different pathways to reduce TDD and enhance III-V material quality.

# I.3. Integration approaches for III-V on Si solar cells

The three main challenges in integrating III-V on Si have been presented. This section focuses on the different approaches that have been studied in literature in the photovoltaic field, along with their advantages and drawbacks. It will deal with the epitaxial approaches and the way to avoid the above-mentioned difficulties, but also with alternative approaches for multi-junction solar cell using wafer bonding. The best results obtained in the photovoltaic field will be presented.

## 1.3.1. Epitaxial approaches

For more than 30 years, researchers have attempted to combine Si and GaAs. Many paths have been, and are still being investigated to reduce the formation of antiphase boundaries on a (100) Si substrate, such as the insertion of dislocation filter layers[27], or the selective growth in trenches using aspect ratio trapping (ART)[28]. The issue of antiphase boundaries has been successfully solved using offcut Si substrates with an angle of 4-6° from the (100) plane[24,29]. However, the lattice and thermal mismatches are more serious issues that result in a high density of dislocations and a high stress, especially at the typical growth temperatures of GaAs (above 600 °C by MOVPE) that give rise to more cracking.

***Direct hetero-epitaxy of GaAs on Si:***

The earlier approach that was naturally experimented was to directly grow GaAs on top of Si substrates. The large lattice mismatch between GaAs and Si (4%) results in strain, and defects such as lattice distortion, stacking faults, misfit dislocations, and threading dislocations, that extend in the whole epitaxial layer. The direct growth of GaAs on Si commonly leads to threading dislocation density (TDD) as high as $10^8$-$10^9$ $cm^{-2}$. As an example, a TEM image of a GaAs grown on Si is pictured in Figure 1.10.a. (from Luxmoore *et al.*[30]), revealing the high density of dislocations, visible in darker lines spreading in the GaAs layer. The most efficient technique to reduce this TDD is to perform thermal cycle annealing (TCA)[31]. GaAs-on-Si epitaxy has also been performed by using thick GaAs buffer layers (Vernon *et al.*[32]). After a low temperature nucleation of GaAs at 400 °C, the GaAs is grown by standard MOVPE at 700°C. They deposited a 7 µm thick buffer layer before growing the structure of a single junction GaAs solar cell, with TDD of $8.10^6$ $cm^{-2}$. An efficiency of 17.6 % was obtained with such structure under one sun[33], and 21.3 % under 200 suns[32]. However, this approach is not suitable in case of a tandem approach. The buffer layer being thick and defective, the Si cannot serve as an active subcell. Using $In_{0.1}Ga_{0.9}As$/GaAs strained layer super-lattice (SLSs) in combination with TCA, Yamaguchi *et al.*[34] reached a threading dislocation density of $1\times10^6 cm^{-2}$ for upper GaAs layer grown on (100) Si substrate with 2° offcut, demonstrating 20%

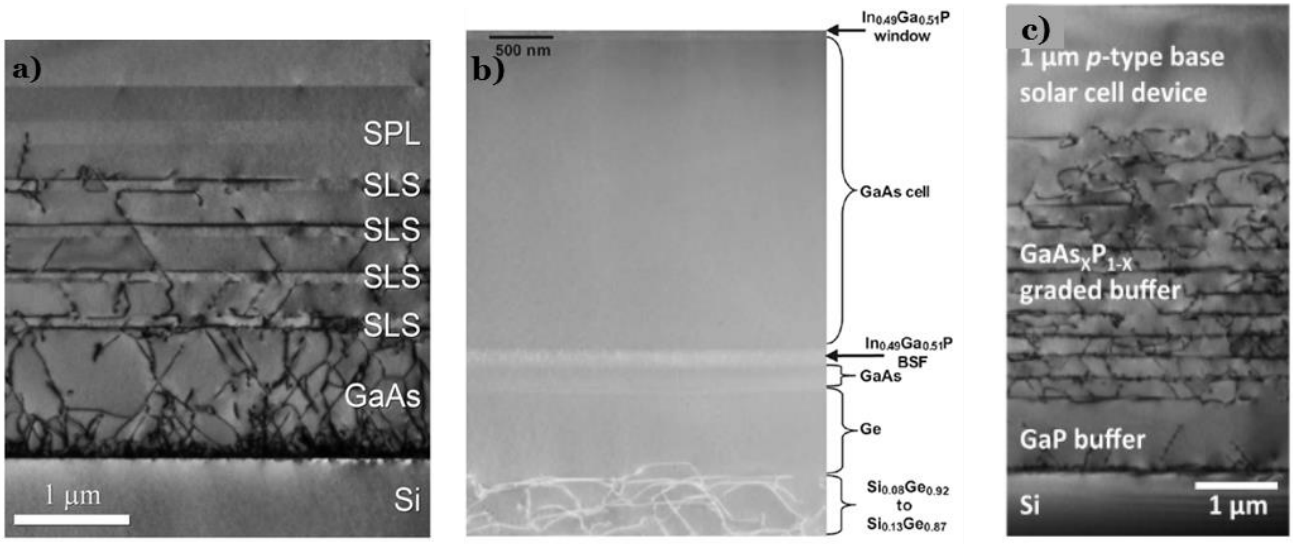



**Figure 1.10 - TEM analysis of a) direct growth of GaAs on Si (Luxmoore et al. [30]), b) SiGe graded layers (Andre et al. [37]) (c) GaP buffer layer (Lang et al. [39])**

efficiency under AM1.5G and 18.3% under AM0 for a single GaAs solar cell grown on Si, the highest efficiency reported up to now for a single GaAs junction grown on Si. To compete with lattice-matched GaAs on GaAs solar cells, further improvement in TDD (below $1\times10^6$ cm$^{-2}$) would be required. In 1997, Soga *et al.*[35] grew an $Al_{0.22}Ga_{0.78}As$ solar cell by MOVPE on top of an active Si substrate. On Si (100) substrates with 2° offcut toward [110], they grew AlGaAs by MOVPE at 950 °C using five TCA iterations. They managed to have a dual junction solar cell of $Al_{0.15}Ga_{0.85}As$ with Si with 21.2% under AM0, which is up to now the best efficiency reported for 2J III-V/Si solar cell using direct hetero-epitaxy.

***Growth using buffer layers:***

To limit the effects of dislocations that appear during direct growth of GaAs on Si, using buffer layers with progressive change in lattice parameter is a solution to accommodate the mismatch strain. Figure 1.11 shows the different pathways to accommodate gradually from Si lattice parameter to III-V lattice parameter with the right bandgap.

To pass from a Si substrate to the lattice parameter of GaAs, a first way is to use a SiGe graded buffer until Ge which has the same lattice parameter as GaAs (Path a in Figure 1.11). It enables to realize low TDD relaxed Ge layers on Si substrates. The realization of a Ge virtual substrate has been a topic of interest since the late 90's. Carlin *et al.*[36] grew single junction InGaP by MOVPE and MBE on a GaAs/SiGe/Si virtual substrate using a thick graded buffer layer on top of a 6° offcut Si substrate. A TDD slightly above

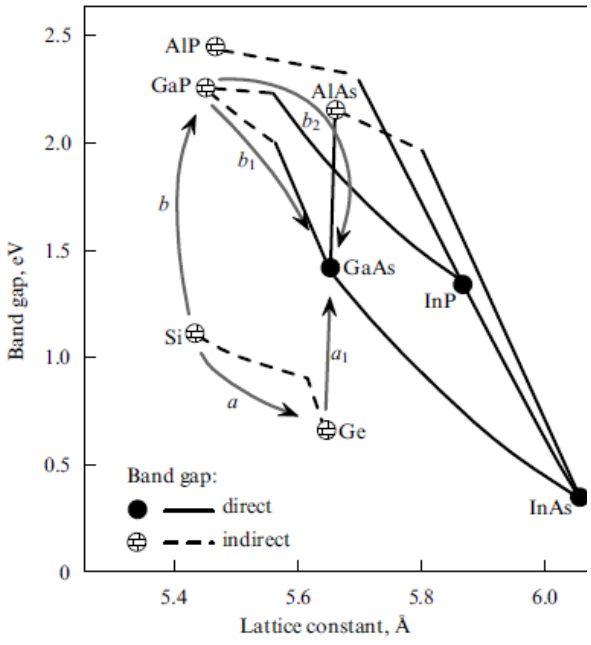



**Figure 1.11 - Bandgap versus lattice constant for Si, Ge, and III-V compounds. Arrows indicate the possible pathways for integrating III-V on Si.**

$10^5$ $cm^{-2}$ was reported in their GaAs. They measured an efficiency of 18.5% under AM0 conditions and 15.5 % under AM1.5G[37]. A cross sectional micrograph of their 1J GaAs solar cell grown on Ge/SiGe/Si substrate is shown in Figure 1.10.b.

However, even though SiGe graded buffer layers can be used to produce a virtual Ge substrate, their bandgap is lower than the underlying Si, and thus not transparent to the subcell. This technique is suitable for using a cheaper substrate for III-V solar cells, but is not adapted in case of the use of an active Si subcell because it limits optical transparency. With an active Si subcell, the buffer layers should be more transparent than Si. GaP, whose parameter is close to that of Si (Figure 1.11, path b), can be a good candidate for graded buffers[38]. Its high bandgap of 2.26 eV ensures a good transparency of the buffer layer. The lattice mismatch between GaP and Si is of only 0.37 %. The addition of As enables to move from GaP to GaAs by slowly decreasing the bandgap and increasing the lattice parameter. Figure 1.11.c. shows a cross sectional SEM image of a solar cell grown on Si after GaP buffer and GaAsP graded buffers, from Lang *et al.*[39] Their solar cell is made of $GaAs_xP_{1-x}$ with a bandgap of 1.7eV, which is adapted for a tandem configuration with Si. They reported a TDD of $1\times10^7$ $cm^{-2}$, which is higher than the TDD obtained when using $Si_xGe_{1-x}$ graded layers, but was the best reported for GaAsP buffer. An efficiency of 6.88% was disclosed, with a good $V_{oc}$ of 1.12 eV, exceeding the $W_{oc}$ (= $E_g$ - $V_{oc}$) of the previous reported solar cells. Efforts are still being made to reduce the threading dislocation density, and to minimize the issues during GaP nucleation, such as antiphase domains (APDs), stacking faults and microtwins[40]. The first GaAsP/Si tandem solar cell revealed an efficiency of 10.65 % under AM1.5G spectrum, with a limiting FF of 61 %. They attribute this to the poor characteristics of their $GaAs_{0.75}P_{0.25}$ tunnel diode that induced losses at the interconnection between the two subcells. In 2016, Yaung *et al.*[41] used MBE to further optimize GaP/Si templates and minimize TDD. They reported TDD down to $4\times10^6$ $cm^{-2}$. Their best single GaAsP solar cell grown on a GaP/Si template reached 12% efficiency. Dimroth *et al.*[42] used $GaAs_xP_{1-x}$ buffer layers on silicon to grow a GaInP/GaAs dual-junction. It yielded an efficiency of 16.4 % (while the same dual-junction on GaAs exhibits a 27.1 % efficiency). The main limit comes from the still too high TDD in the GaAs subcell reducing carrier lifetime.

Among the different routes, the use of III-V-N (dilute nitride) on Si is also being explored[43]. Figure 1.12 shows the bandgap versus lattice constant graph, that includes this time the dilute nitride materials. The main advantages are that they can be lattice matched with Si, and quaternary compounds such as $GaAs_xP_{1-x-y}N_y$ or $In_xGa_{1-x}P_yN_{1-y}$ are good options for lattice-matched top-cells in III-V/Si tandem solar cells, but also for 3 junction solar cells[44,45]. The buffer layer is transparent to the subcell. However, this technique is limited due to the poor diffusion lengths in dilute nitride materials, along with the difficult control of the composition of the quaternary alloys. A 5.2% $GaAs_{0.10}P_{0.86}N_{0.04}$/Si tandem solar cell has been reported using dilute nitride after a GaP nucleation[46]. Lattice-mismatched InGaN on Si is also explored, with its tunable direct bandgap ranging from 0.65 eV to 3.4 eV. The main challenges are

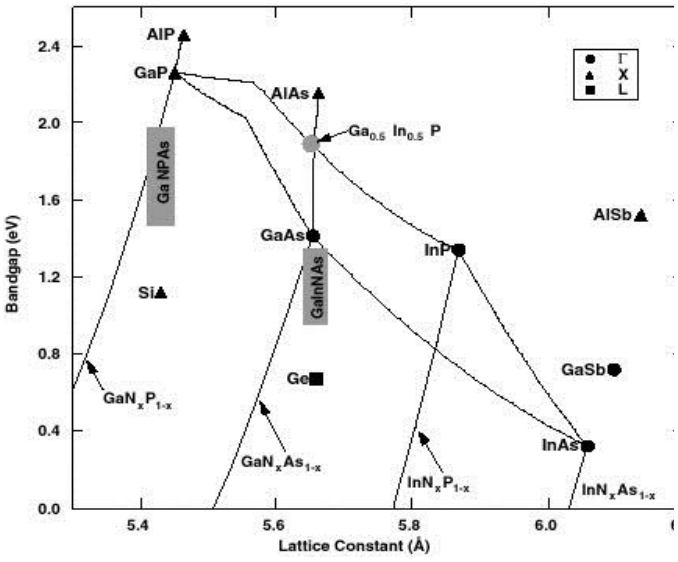



**Figure 1.12 - Bandgap versus lattice constant including dilute nitride materials**

| Path | Advantages | Challlenges | Efficiency (AM1,5G) | Cell | Reference |
|---|---|---|---|---|---|
| **Direct GaAs on Si** | • Conventional path | • High thermal mismatch<br>• Thick GaAs buffer layer | ▪ 20 % | ▪ 2J AlGaAs/Si | ▪ Soga et al. 1997 |
| **$Si_xGe_{1-x}$ graded buffer** | • Low dislocation density ($<1.10^6 cm^{-2}$) | • Not transparent for Si bottom cell<br>• Thick graded buffer<br>• High thermal mismatch | ▪ 18,1 %<br>▪ 18,9 % | ▪ 1J GaAs cell<br>▪ 2J GaAsP/SiGe | ▪ Andre et al. 2005<br>▪ Diaz et al. 2014 |
| **GaAsP graded buffer** | • Transparent for Si subcell<br>• GaP layer lattice-matched to Si | • Thick graded buffer<br>• High dislocation density ($4.10^6 cm^{-2}$) | ▪ 16,4 % | ▪ 2J GaInP/GaAs | ▪ Dimroth et al. 2014 |
| **GaAsPN on Si** | • Lattice-mtched<br>• Transparent and thin buffer layers | • Poor diffusion length in dilute nitride materials<br>• Control of the composition of quaternary alloys | ▪ 5,2 % | ▪ 2J GaAsPN/Si | ▪ Geisz et al. 2005 |
| **InGaN on Si** | • Wide range of bangaps (0.65 eV → 3.4 eV) | • Large lattice and thermal mismatch<br>• Poor structural quality %N>30% | ▪ 7,12 % | ▪ 1J InGaN//Si heterostructure | ▪ Tran et al. 2012 |

**Figure 1.13 - Summary of epitaxial pathways for integrating GaAs on Si, their advantages and challenges, and the best solar cell efficiencies reported**

the poor structural quality for an N content above 30 %. However, a single InGaN junction grown on Si has been reported with an efficiency of 7.12% under AM1.5G[47].
Several paths for growing III-V on top of Si have been presented. To summarize this section, the advantages and drawbacks of each of these techniques are summarized in Figure 1.13, along with the reported record solar cells using each technique.

### 1.3.2. Non epitaxial methods (bonding)

Even if direct growth would be the easiest technique to implement in industry, hetero-epitaxial grown Si-based MJSC efficiencies are still limited by the defects in the III-V cells, along with the degradation of the Si cell during high-temperature III-V epitaxy. Thus, non-epitaxial approaches are also investigated. The term of "wafer bonding" refers to the fact of attaching a bulk or thin film (III-V) to a substrate (Si). The first way of attaching them is to directly press the two surfaces, leading to the creation of Van Der Waals bonds. This direct bonding requires perfect surfaces on both wafers: no roughness, perfectly flat mirror polished surfaces, and careful removal of surface contamination. Another approach is the mechanical stacking, which consists of using "glue". The two wafers are coated with a film, then put into contact together, heated and pressed. This approach implies the introduction of a gluing film between the two wafers, potentially introducing some electrical resistance or some optical absorption. Recently, several records have been beaten in the field of Si-based multi-junction solar cells, by means of wafer bonding or mechanical stacking. Up to now, the only tandem solar cells that reached 25 % were achieved by separately manufacturing the two subcells, and bonding them afterwards. A monolithic two-terminal triple-junction of GaInP/AlGaAs//Si solar cell was fabricated using surface-activated direct wafer bonding, leading to a conversion efficiency of 30.1 % under one sun[48] (Figure 1.14.b). Also, a four-terminal junction using mechanical stacking avoids the need for a tunnel junction and reduces the requirements of perfectly flat polished surfaces. It is also more tolerant to the slight bandgap variations, as there is no need for current matching. In this configuration, a GaInP/Si dual-junction solar cell on a silicon heterojunction has achieved an efficiency of 29.8% in 2016[49,50] and more recently 32.8 % in August 2017[51] (Figure 1.14.a). On the same Si heterojunction, they stacked a GaInP/GaAs dual junction

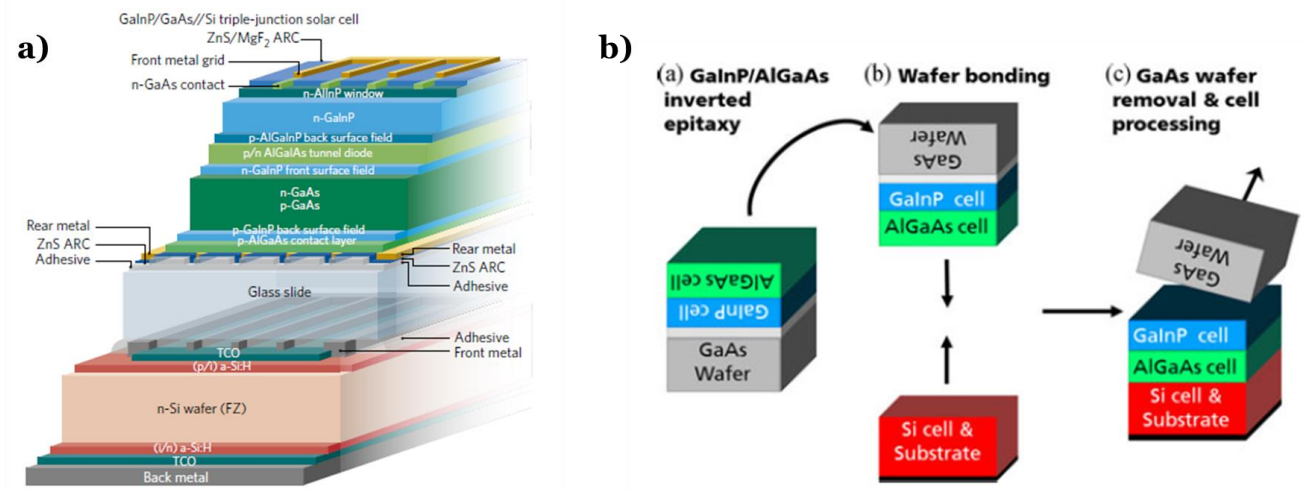



**Figure 1.14 - a) Design of the four-terminal GaInP/GaAs//Si triple junction solar cell with 35.9 % efficiency (Essig et al. [50]) b) Design and process flow of GaInP/AlGaAs//Si triple junction wafer-bonded solar cell with 30.1% efficiency (Cariou et al. [47])**

leading to a 3-junction solar cell with a record efficiency of 35.9 %[51]. The structures of the record triple junction solar cell using Si as a bottom cell are presented in Figure 1.14.

This section presented the different paths to integrate III-V and Si for tandem solar cells. On the one hand, direct growth methods are the easiest to implement industrially, however the solar cells are highly limited by a high threading dislocation density, which is inherent to the technique. If the anti-phase boundary issues are yet controlled, the lattice mismatch, combined with the thermal expansion mismatch are up to now the main challenging issues for this approach. On the other hand, wafer bonding offers promising pathways to perform multi junction solar cells based on Si. 4-terminal triple junctions using conductive glue have shown efficiencies up to 35.9%. However, these techniques remain expansive and need further reduction in the production costs before considering reaching their industrial deployment.

# I.4. An innovative approach for III-V/Si integration

## I.4.1. IMPETUS project: principle

Now that all the routes currently studied in the research labs have been presented with their respective advantages and drawbacks, we propose here an innovative approach for combining III-V and Si. In LPICM lab, a very strong know-how has been developed for years: crystalline silicon homoepitaxy at low temperature (below 200°C) using conventional radio frequency-PECVD (RF-PECVD) reactors. It proved the possibility of growing good quality crystalline silicon by using standard PECVD reactors usually used for amorphous deposition. A detailed overview and presentation of this technique for silicon epitaxy will be given in the next chapter. This thesis is led within the framework of an ANR project which has been initiated by several laboratories that allied their know-how. The IMPETUS project (Innovative Multi-junction combining MOVPE and PECVD Epitaxy at low-Temperature for Solar applications) gathers four partners: the LPICM (laboratory of physics of interfaces and thin films from Ecole polytechnique), the III-V Lab (joint laboratory between Thales, Nokia Bell Labs and CEA Leti), Total (its PV research branch from Total Gas and Power), and the GeePs (Group of Electrical Engineering of Paris, from Centrale Supélec). The III-V lab has a strong knowledge in III-V materials epitaxy and processing for optoelectronic and photonic devices. The LPICM and especially its common team with Total Gas and Power, has a robust know-how in Si photovoltaics. The GeePs added its strong expertise in electrical characterizations, as well as solar cell modelling.

The idea of the impetus project is to explore the path of using low temperature PECVD to grow crystalline Si on GaAs. In this inverted metamorphic approach, the Si growth occurs at a temperature below 200 °C. In this way, the growth of the group IV material on top of the polar III-V material avoids the antiphase boundary issues presented above. Also, the hetero-epitaxy occurring at such low temperature drastically reduces the issues due to thermal expansion mismatch when cooling down the bulk heteroepitaxial layer. Figure 1.15 shows the principle of the IMPETUS project and the targeted final device. It consists of a 2-terminal tandem solar cell. The material chosen for the top cell is AlGaAs. $Al_xGa_{1-x}As$ bandgap can be tuned ranging from 1.42 eV (GaAs) to 2.12 eV (AlAs) while staying lattice-matched with GaAs. In our inverse metamorphic approach, AlGaAs is first grown above 540 °C by metal organic vapor phase epitaxy (MOVPE) on a (100) GaAs substrate. Then, a tunnel junction is grown. Subsequently, the group IV cell (Si or SiGe) is obtained via

heteroepitaxial deposition by low temperature plasma-enhanced chemical vapor deposition (LT-PECVD), which occurs below 200°C. After the growth of both subcells, the tandem solar cell must then be inverted, by transferring it to a low cost carrier. Following the removal of the GaAs substrate, which would ideally be reclaimed, the device process is finished on the host carrier involving metal contacts deposition at the front. The back contact must also be taken, either at the back of the host carrier if it is conductive, or from the front. Antireflection coating will be deposited, and the cells will be separated via mesa etching.

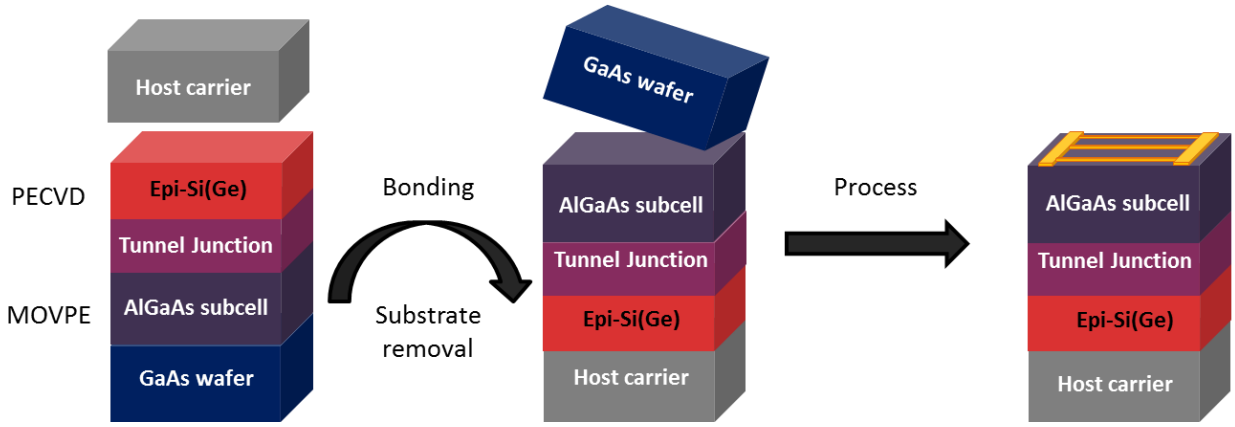



**Figure 1.15 - Principle of the IMPETUS project. AlGaAs is grown on a GaAs substrate by MOVPE, followed by a tunnel junction and crystalline Si or SiGe grown by PECVD below 200 °C. The structure grown is then transferred to a low-cost carrier, the substrate removed, and the device is fabricated by standard clean room processes.**

## I.4.2. Realistic simulations of IMPETUS tandem solar cell

The intended tandem solar cell has been presented, but many obstacles will of course be faced. The first challenge that had to be assessed and studied was the thickness of group IV material that could experimentally be grown. Indeed, in an epitaxial approach, it is highly time consuming to grow the material, and it is hardly conceivable to grow absorbing Si as thick as 100 µm. Thus, simulations studies were performed within the frame of the IMPETUS project in order to adapt the simulations from Figure 1.6 with the experimental reality of a thinner Si subcell, so as to determine the optimum structure to grow. The main results of this study are presented here, but more information can be found in Lachaume *et al.*[52,53]

For the final tandem cell, the III-V cell needed would be made of AlGaAs. As the two subcells are connected in series we have to carefully match the current of each individual cell. In standard tandem configurations, the bottom cell is composed of a thick Si wafer, and it is considered that it has a QE of 1. In our specific case, the bottom cell will be a thin film, epitaxially grown by PECVD. Consequently, the bottom cell made of Si will not be fully absorbing because of its small thickness. The simulations state that thinning the bottom cell significantly modifies the optimum design of the top cell. The simulated structure is shown in Figure 1.16.a. A Si subcell with variable thickness is simulated using parameter extracted from previous experimental data on epi-Si material[52,54]. It is passivated by an amorphous n-doped layer and contacted with a flat aluminum mirror. It is worth

noticing that at this stage, no particular light trapping scheme is considered in the simulation, meaning that there is still room for improving this tandem cell.

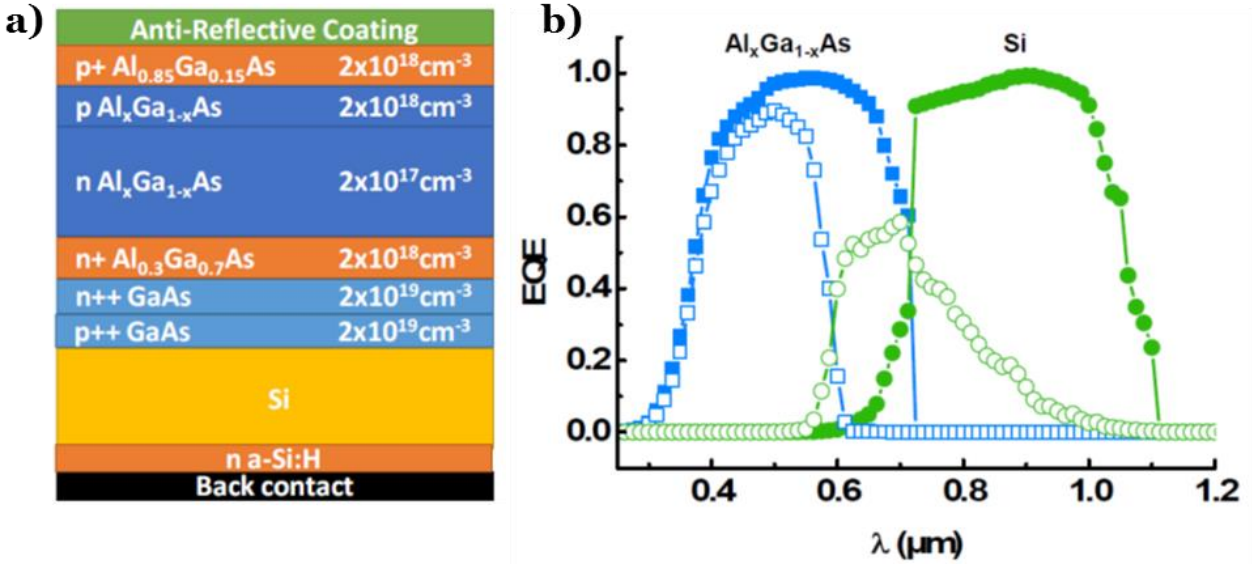



**Figure 1.16 - a) Details of the simulated tandem solar cell b) External Quantum Efficiency (EQE) of current-matched AlGaAs/Si tandem solar cell with thick Si (full symbols) and thin Si (open symbols).**

The considered tunnel junction is a non-optimized GaAs/GaAs TJ doped at $2\times10^{19}$ $cm^{-3}$. Then, the AlGaAs subcell consists of an AlGaAs back surface field, base and emitter with variable Al content, and a window layer with high bandgap. An antireflective coating is also considered on top of this cell. Figure 1.16.b. shows the external quantum efficiency (EQE) versus photon wavelength of two current matched AlGaAs/Si tandem solar cells. The filled symbols correspond to the EQE in case of a full absorption of the Si subcell, while the open symbols represent the EQE if we consider a 5 μm thick Si bottom cell. As we can see, there is a huge drop in quantum efficiency of the Si subcell compared to a 500 μm thick Si wafer. To get the optimum efficiency, the AlGaAs top cell must be

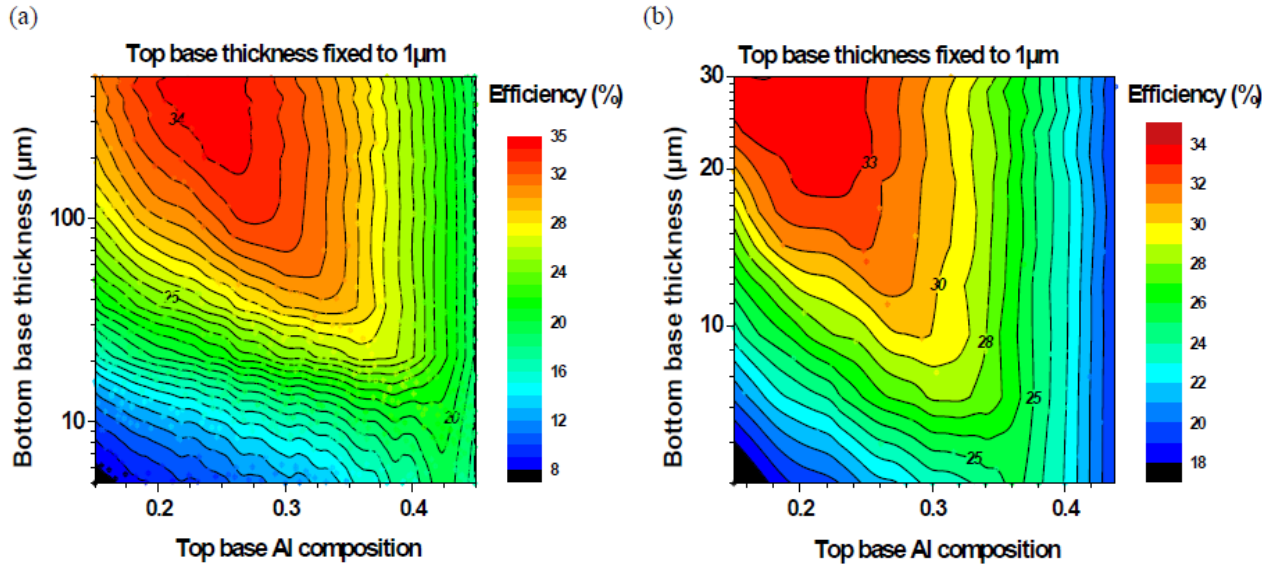



**Figure 1.17 - Maps of tandem cell efficiencies simulated for different combinations of top base Aluminum compositions and bottom base thicknesses: (a) for a bottom cell in epi-Si and (b) for a bottom cell in epi-$Si_{0.63}Ge_{0.27}$**

current matched. The maximum efficiency achievable for tandem cell with 5 µm epi-Si is η~17%, which is lower than that of a single GaAs solar cell. We can thus wonder what could be the minimum thickness of Si and the optimum Al composition to get a best realistic efficiency. Pictured in Figure 1.17.a. is the map of tandem cell efficiencies simulated for different combinations of top base aluminum compositions and bottom base thicknesses for an epi-Si bottom cell. The AlGaAs top cell thickness is fixed at 1 µm. We see that to get a minimum efficiency of 25%, we need to have at least 30 µm of epitaxial silicon. For the time being, growing such a thick layer by PECVD is not realistic. But PECVD reactor also allows growing crystalline $Si_{1-x}Ge_x$, which opens up the path of integrating III-V with SiGe. The addition of Ge highly enhances the absorption of the subcell. SiGe bandgap will be lower than Si, thus the Al composition for optimum current matching will be modified. In Figure 1.17.b, similar simulations have been done replacing the epi-Si bottom base by a $Si_{0.63}Ge_{0.27}$ layer. The use of SiGe allows us to use much less thickness of PECVD grown material for the same resulting efficiency. Namely, 25% efficiency can still be reached with only 5 µm of epi-$Si_{0.63}Ge_{0.27}$ and 33% with 20 µm. Moreover, an optical model[52] showed that the addition of a light-trapping scheme would divide by a factor of 2 the required thickness for achieving the same efficiency. Thus, less than 10 µm of $Si_{0.73}Ge_{0.27}$ material would be sufficient to reach >30 % efficiency.

This innovative approach suggests using the advantages of low temperature PECVD in order to fabricate tandem solar cells. The promising theoretical analysis shows that this approach could lead to efficiencies above 30 %. This PhD has been an exploratory work, devoted to prove the experimental feasibility of such approach and to pave the way towards the realization of tandem solar cells using low-temperature PECVD.

## I.5. Building blocks and outline of this PhD

This PhD thesis, at the interface between the two worlds of III-V and group IV materials, is divided into 4 main chapters, after this introduction chapter. Many steps had to be developed and mastered to lead to the final device. At the beginning of the project, a lot of choices were possible, and the feasibility of several technological challenges had to be proved. What is the maximum thickness of Si that can be grown by PECVD? Can we grow good crystalline SiGe, and with which Ge content? Is PECVD grown material suitable for good tandem solar cells? The III-V know-how in photovoltaics had also to be developed. Can we grow a good quality III-V solar cell and process it with the right design, ohmic contact etc..? Should we use a n-type base or a p-type base solar cell? Also, the tunnel junction needs to be developed. Should it be made of III-V materials? of Si? or hybrid III-V/Si tunnel junction? The growth of Si on GaAs also has to be understood. How does epitaxy happen at such low temperature? As this combination of processes and materials are not standard, we must also wonder what the impact of the PECVD process on the underlying III-V layers is. Is there any effect of PECVD on the structural or electrical properties of GaAs? And finally, how can we bond the full tandem device to the host carrier? What are the technological requirements and issues? What is the impact of the strain in the layers, when the substrate is removed? These are some of the numerous questions that had to be assessed during this PhD. In this manuscript, we try to answer gradually to most of these questions, in order to progressively make the right technological choices. Each of the following chapters will successively deal with different building blocks necessary to develop the whole final tandem device.

Indeed, before trying to grow and process directly, it is of high importance to characterize separately each material, and to understand at best the physics involved. The electrical properties of the separated devices will be studied, so as to validate their right operation, or in some case, to bring to light some unexpected effects due to our non-conventional approach. With this methodology, we will be able to first assess and solve the essential challenges inherent to our approach and second, to reveal some compatibility issues, along with their solutions. This doctoral work is articulated so as to focus on the constituting blocks and progressively lead to the final targeted device. Figure 1.18 pictures the different building blocks of the tandem solar cell, corresponding to the different chapters of this manuscript.

As the targeted tandem device includes the growth of thick Si(Ge) material by PECVD, ***Chapter 2*** will deal with the epitaxial growth of Si and SiGe on Si substrates by PECVD. We will present the main growth and characterization techniques used, as well as the different PECVD reactors available in the lab: a homemade PECVD reactor (Arcam) and a large industrial reactor (Octopus). In this chapter, the study of the Si material properties, the ability to grow thick layers and its evolution with annealing will be assessed. The growth of $Si_{1-x}Ge_x$ with increasing Ge content on top of Si will be studied. The crystal quality, Ge content and layer relaxation will be assessed by means of XRD measurements. Finally, Si and SiGe heterojunction solar cells will be fabricated and characterized on a solar simulator, to validate the use of this material as an optical absorber in the tandem device.

Once the Si subcell had been separately grown and characterized, we focus on the integration of PECVD Si grown on GaAs by heteroepitaxy in ***Chapter 3***. Structural studies of the early stages of the growth will be performed in order to have a better insight on the growth mechanisms involved in low temperature PECVD. To do so, we used X-Ray diffraction with synchrotron beam and studied the strain in the Si layer. Also, the effect of PECVD (mainly the hydrogen plasma) on the electronic properties of GaAs will be assessed.

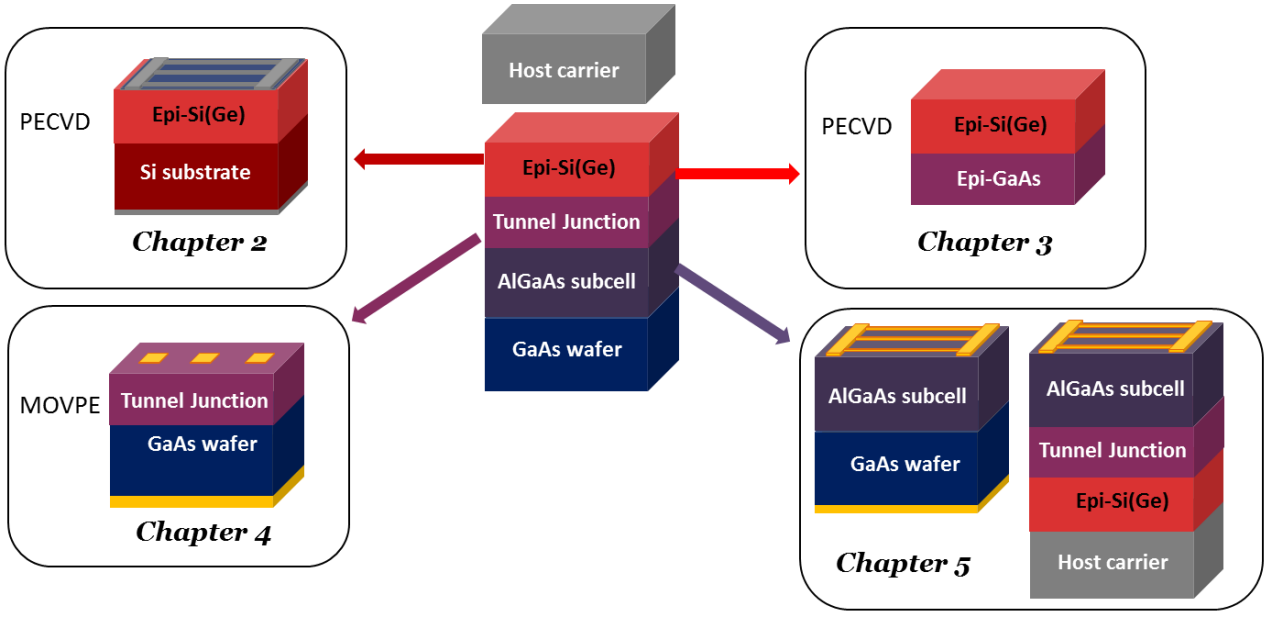



**Figure 1.18 - Different building blocks of the tandem solar cell**

In ***Chapter 4,*** we will study in details one essential part of our 2-terminal targeted tandem solar cell: the tunnel junction. Theoretical explanations and our requirements for the tandem device will

be presented, along with the basics of MOVPE and clean room technologies used in this PhD. After presenting our first tunnel junctions grown in the lab with conventional GaAs dopant, we will present the further improvement of these tunnel junctions by developing Te-doped GaAs. Doping level optimization of GaAs doped with Te will be discussed, and we will measure tunnel junctions with electrical characteristics highly suitable for our tandem solar cell. The development of heteroepitaxial doped c-Si on GaAs will also be presented, to open the path towards hybrid tunnel junctions.

Finally, ***Chapter 5*** will focus on the process of single III-V sub-cells as well as the tandem device after bonding. We will present the path to reach a state-of-the-art AlGaAs solar cell grown by MOVPE that will serve as the tandem sub-cell. The realization of the IMPETUS tandem solar cell also includes the bonding of the multi-junction. We will thus present the bonding and processing of a full 2 inches inverted III-V solar cell in order to master this technique and validate the steps. Finally, a Si on GaAs tandem solar cell will be bonded.

Chapter 2

# Low Temperature PECVD epitaxial growth of Si(Ge)

## Contents

In this chapter, we present homoepitaxy by low temperature Plasma Enhanced Chemical Vapor Deposition (LT-PECVD). We will first introduce PECVD growth of crystalline silicon, along with the reactors used in this manuscript. After a brief introduction of material characterization tools, we will present the growth of Si and SiGe materials on (100) Si substrates in the industrial reactor Octopus. These layers will then be integrated in heterojunction solar cells whose electrical performances will be characterized.

# II.1. PECVD and characterization tools

## II.1.1. Epitaxy using low-temperature PECVD

### II.1.1.1. PECVD: principle

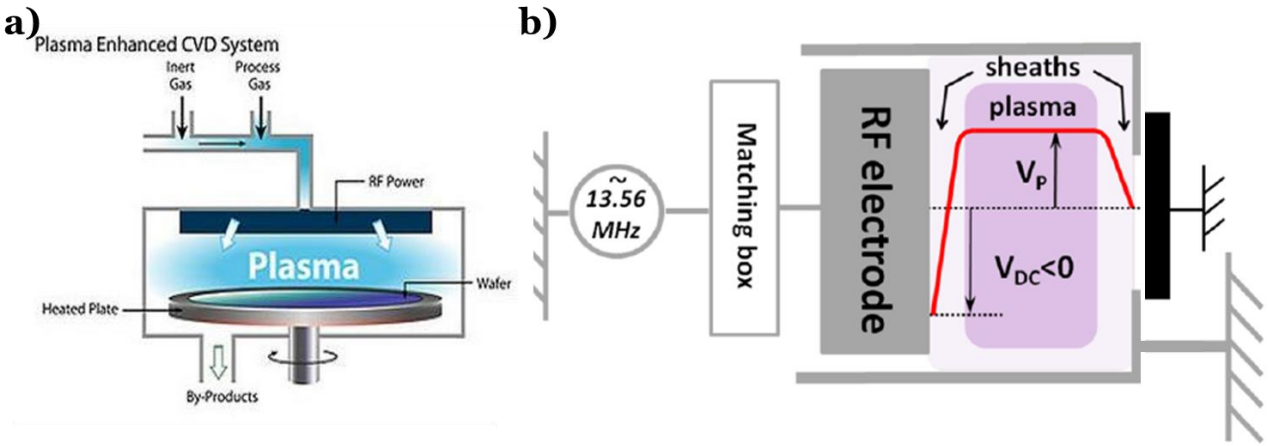



**Figure 2.1 - a) Schematics of a PECDV reactor b) Schematic of the potential distribution in a RF discharge where the substrate is grounded and the RF voltage applied to the RF electrode**

This part describes the technique used in this PhD to grow crystalline silicon and silicon-germanium: plasma enhanced chemical vapor deposition. This technique was also used to deposit amorphous layers to perform the stacks of an heterojunction solar cell, or to deposit $SiO_2$ on top of III-V materials. It is widely used in industry for various applications: surface treatment, thin film deposition in microelectronics ($SiO_2$, SiN …). PECVD technique utilizes a plasma to provide energy for the deposition reaction to take place. The presence of a plasma allows to deposit at lower temperatures than in standard CVD techniques. The typical operating temperatures are between 150 °C and 400 °C. A detailed description of PECVD can be found in Liebermann et at[55]. We will here describe the basics principle. A plasma is a gas in which some atoms or molecules are ionized. In a PECVD reactor, the plasma is created by introducing gas between two electrodes that are supplied by radio frequency (RF) power, at 13.56 MHz in our case. One of the electrodes is grounded, and the other is connected to the RF power through a matching box, to ensure an optimized power coupling between the generator and the reactor. The grounded electrode often corresponds to the substrate holder. The RF power gives the energy necessary to ionize the gas mixture, thus creating a plasma containing positive and negative ions, electrons, but also neutral species such as radicals, nanoparticles, neutral atoms and molecules. The potential profile is plotted as a red line in Figure 2.1.b. The plasma bulk corresponds to the region where the potential is constant. In contrast, the electron density strongly decreases in the sheath region. Electrons have a lower mass and therefore

a higher mobility. Thus, they will be lost to the electrodes, leaving behind a region (the sheath) that is not neutral anymore, containing positive ions and radicals that can interact with the substrate. Neutral and positive ions can take part in the deposition process, while negative ions are trapped inside the bulk plasma by the repulsive forces arising from the sheath.

In a RF-PECVD, several parameters are of high importance. First, the geometry of the plasma chamber is of prior importance. The frequency of the plasma will also determine the behavior of the electrons and ions. In our case, the frequency is 13.56 MHz. The power applied also influences the deposition. Increasing the power of the excitation will enhance the dissociation and thus increase the quantity of reactive species. The substrate temperature is also crucial when it comes to controlling the reactions that occur on the substrate. A higher temperature will enhance surface mobility and desorption of the impinging species. The pressure must be high enough to enable reactions in gas phase, but not too high because it would favor the formation of powders by nucleation in gas phase.

#### II.1.1.2. Presentation of the two reactors used

During this work, two PECVD reactors have been used. The first one is a home-made PECVD reactor ARCAM shown in Figure 2.2.a (from outside) and b (open). This reactor was designed and built in the early 80's. A lot of details regarding the design of this reactor can be found in Roca i Cabarrocas *et al*[56]. This reactor contains no load lock and consists of one single vessel kept at a constant temperature, typically between 150°C and 250 °C. The plasmas are confined in the 3 plasma boxes that constitute the 3 different PECVD chambers, avoiding cross contamination. This reactor can be therefore described as a multiplasma monochamber reactor. The samples are located in the same "oven" but placed on a rotating plate which allows placing the sample above the desired plasma box shown in Figure 2.2.b. We can thus start the plasma on an empty position of the plate, stabilize the pressure and optimize the "load" capacitor and the "tuning" capacitor of the plasma to minimize reflected power, before turning the plate to place the sample (that lies face down), above the plasma box. The three chambers enable to process several type of materials in a single pump down process. During this PhD we usually used one chamber to perform the in-situ $SiF_4$ cleaning of samples, and one chamber to perform the epitaxial growth of intrinsic silicon, or SiGe. The third one enables to add another step such as the growth of doped c-Si, or the deposition of doped a-Si:H for the passivation. The typical limit vacuum obtained is in the range of $10^{-6}$ or a few $10^{-7}$ mbar.

The second reactor has been acquired in summer 2016 during this PhD by IPVF (Institut Photovoltaïque d'Ile de France) and hosted by LPICM (Figure 2.2.c). This is an industrial reactor provided by IndeoTec[57], that has a fully automated operation mode, along with an automatic plasma match box. It can host up to 7 process modules, but is only equipped with two of them yet. Dedicated to PECVD epitaxy of silicon, our two chambers can be used at temperatures ranging from 150 °C up to 400 °C, thus at higher temperature than in Arcam reactor. It exhibits a loadlock that ensures very low base pressure in the chambers around $10^{-8}$ mbar, which results in less impurities than in Arcam reactor (O, C…). It ensures homogeneous deposition on 450*350 mm, enabling to process at the same time up to six 4 inch wafers. In its design, the grounded electrode is the bottom one, that also serves as substrate holder. The samples are thus placed right side up.

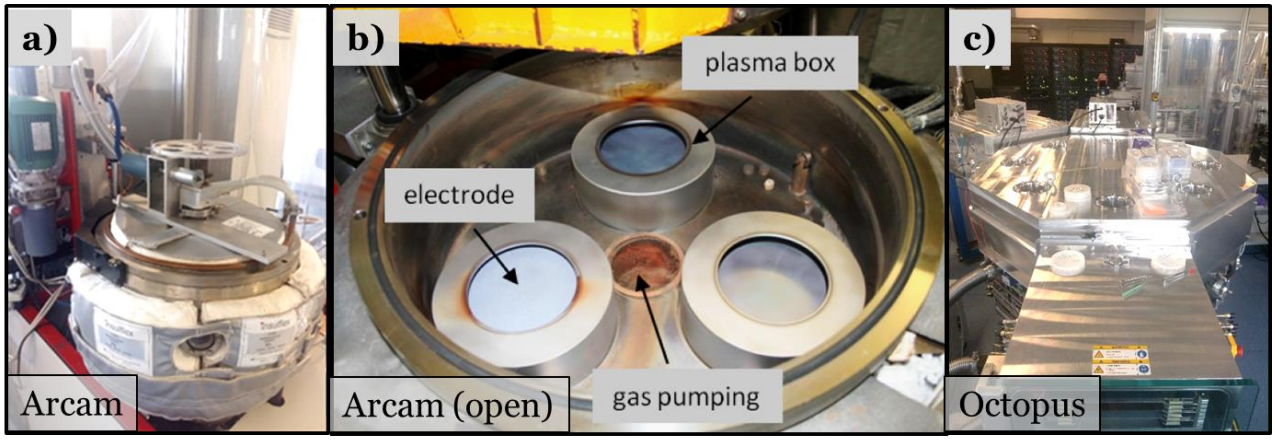



**Figure 2.2 - a) Picture of Arcam reactor, b) picture of the inside of Arcam reactor with the three separated plasma boxes. c) picture of the Octopus reactor from IndeoTec.**

The ARCAM reactor has been mostly used in the early stages of this PhD to perform some optimizations of Si and SiGe growth on Si and GaAs (used in Chapter III), along with the growth of doped c-Si on GaAs as it will be presented in Chapter IV. This chapter presents the results obtained on Si substrates in the new reactor Octopus, thanks to the strong work of process transfer and optimization performed by Nicolas Vaissière.

### II.1.1.3. Low temperature epitaxy by PECVD: overview

Growth of crystalline silicon by epitaxy has been studied since the early 1950s, by means of several deposition methods such as vapor-phase, liquid-phase, solid-phase and molecular beam epitaxy (MBE)[58]. Those epitaxial growth techniques operate at high temperature process (above 500 °C) so as to guarantee good epitaxial quality. However, high temperature has shown to induce diffusion of species such as dopants and impurities into the layer, affecting the bulk electronic properties. In this work, we are also interested in reducing as much as possible the thermal expansion mismatch between Si and GaAs. Low temperature PECVD of Si below 400 °C has first been observed in 1987 by Nagamine *et al.*[59], with a growth rate around 1 Å/s at 250 °C, using fluorine chemistries. They reported the importance of the balance between competitive effects of H and F. In 1988 [60] was reported some n-type Si, but achieved only 200 nm with a low deposition rate of 0.4 Å/s. Then, Xerox Company published results of PECVD epi-Si without fluorine in the plasma, using standard $SiH_4/H_2$ chemistry[61]. They pointed out the importance of the balance between deposition and etching by hydrogen to achieve whether amorphous, microcrystalline or epitaxial silicon. Doped layers and selective epitaxy of Si on (100) Si substrates was then achieved at IMEC by Baert *et al.* in the early 90's [62,63]. More recently, low-temperature epitaxy has then regained interest in the photovoltaic field. Indeed, LT-PECVD is a well-established growth technique in PV industry to grow microcrystalline and amorphous silicon for realization of heterojunction solar cells at large scale. For these applications, having atomically sharp interface between c-Si and a-Si:H is highly critical. However, researchers frequently observed unwanted epitaxial growth that was happening in the first stages of a-Si:H growth [64,65]. It was thus important to understand the mechanisms and to know the growth conditions to avoid such epitaxial growth by PECVD. It is now investigated in various

laboratories, in order to integrate PECVD epi-Si in a silicon solar cell as an optical absorber[66] or as a doped emitter [67–71].

### II.1.1.4. Epitaxy: standard growth mechanisms

While the growth mechanism of crystalline Si by LT-PECVD is still not fully understood (and will be discussed in Chapter 3), the growth mechanisms using common epitaxy techniques are divided in 3 main modes that we present in this section. Epitaxy, from the greek epi (placed or resting upon) and taxis (arrangement), is the extension of a single crystal on top of another crystal. We have already introduced in Chapter 1 the two types of epitaxial growth that can be distinguished: homoepitaxial growth, when the film is of the same material as the substrate, and heteroepitaxial growth, when the film is different, with different lattice parameter. In this chapter, we will deal with both: the homoepitaxy of Si on Si substrate and the heteroepitaxy of SiGe on Si, for different Ge contents. Up to now, three main growth modes have been identified. They depends not only on the lattice parameters, but also of the chemical potential of the surface.

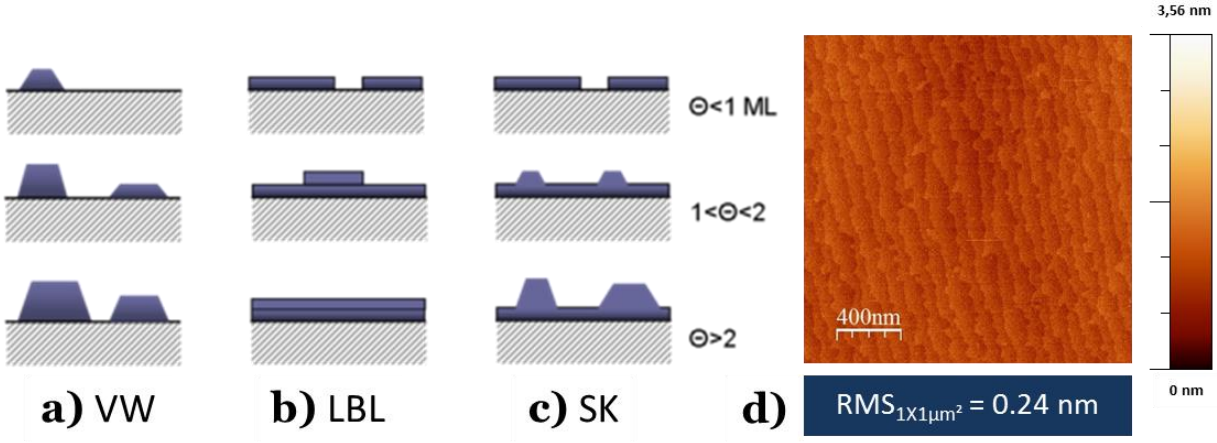



**Figure 2.3 - Illustration of the three main growth modes: a) Volmer-Weber mode (VW) b) Frank-van der Merwe mode (Layer-By-Layer) c) Stranski-Krastanov (SK) d) Atomic Force Microscopy mapping of the surface of an GaAs layer grown by MOVPE**

The Volmer-Weber **(VW)** mode consists of the formation of islands, as represented in Figure 2.3.a. The adatom-adatom interactions are stronger than the interactions between adatoms and the substrate surface. Thus, they coalesce together forming three dimensional adatom clusters or islands. This 3D growth mode is usually the dominant one at low temperature due to low surface diffusion of adatoms. It usually results in rough surfaces, and the films present some grain boundaries that appear when the clusters join each other.

The Frank-van der Merwe mode, represented in Figure 2.3.b, is the layer-by-layer **(LBL)** growth mode, in which the film grows, as its name suggests, layer by layer. Each adatom reaching the substrate diffuses on its surface until reaching an atomic step. This 2D mode occurs usually at high temperature, when surface diffusivity is rather high, and results in an atomically smooth surface. As an illustration, Figure 2.3.d shows an AFM image of the surface of one of our MOVPE grown GaAs samples. We can distinguish the terraces, corresponding to the atomic steps of the grown layer.

The Stranski-Krastanov **(SK)** mode, or layer-plus-island growth mode, consists of a combination of the two previous growth modes, as shown in Figure 2.3.c. In the SK mode, the growth happens first

in a layer-by-layer configuration. Over a certain thickness, islands start to appear and the growth continues in a 3D mode and follows its mechanism of nucleation and coalescence. The critical thickness depends on several parameters including surface energies or lattice parameters of the substrate and the film grown. This growth mode happens when the interface energy increases during the growth, for example when there is an increasing strain in the film due to lattice mismatch, thus mainly in heteroepitaxy.

## II.1.2 Material characterization

Assessing the structural and chemical properties of the material is essential to understand and optimize the effect of the growth parameters on the crystal quality. We present here most of the material characterization techniques that have been used during this PhD: ellipsometry, mainly used to assess the epi-Si quality, and X-Ray diffraction (XRD), to get an insight on the strains in the grown layers, along with the composition of $Si_{1-x}Ge_x$ alloys as well as III-V ternary alloys. Then, a list of different characterization techniques that have been less systematically used will be drawn up. Those techniques have been useful not only in this chapter dedicated to PECVD growth of Si and SiGe on Si substrates, but also in the following chapters.

### II.1.2.1. Ellipsometry

To evaluate the crystalline quality of the films grown by PECVD, the first characterization tool used is ellipsometry. While some of the reactors in the lab are equipped with in-situ ellipsometers, unfortunately the two reactors used in this work (Arcam and Octopus) do not have in-situ characterization. Thus, this technique was widely employed as ex-situ characterization. Ellipsometry is a non-destructive technique based on the polarization of light, and its interaction with the material when reflecting on the sample. It enables to analyze the film properties, provides

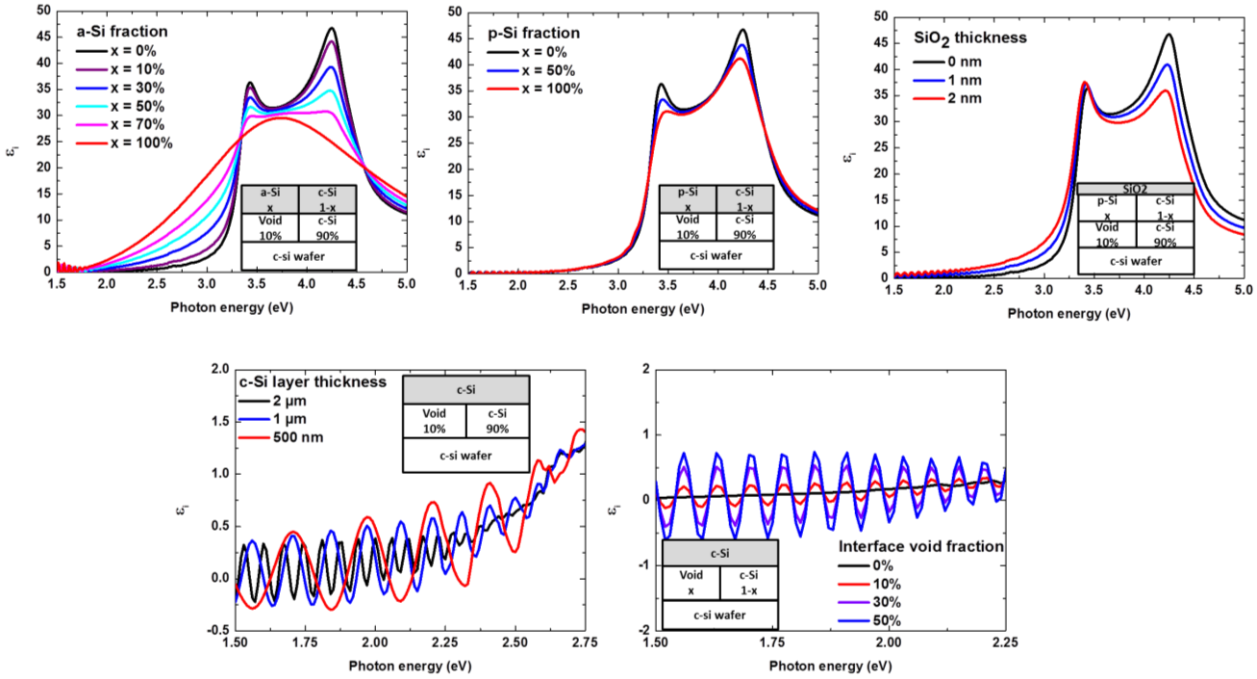



**Figure 2.4 - Ellipsometric spetra (imaginary part of the dielectric function) simulated with DeltaPsi2 by varying a) c-Si/a-Si fraction, b) c-Si/p-Si fraction, c) native SiO2 thickness d) c-Si thickness e) roughness or defectivity of interface between substrate and epi-layer**

information on surface and give its optical constants, its roughness and thickness. In this work, we used it mainly to have a quick estimation of the thickness of the Si film, and to assess its crystallinity, by performing fits with the software DeltaPsi², provided by Horiba. Figure 2.4.a. shows the simulated ellipsometric spectrum (imaginary part of the pseudo dielectric function) as a function of the photon energy. We see that epitaxial films show two characteristic peaks at $E_1$ = 3.4 eV and $E_2$ = 4.2 eV. On the contrary, an amorphous film will present a large peak centered around 3.5 eV. For decreasing crystalline quality, we see that both $E_1$ and $E_2$ peak intensities are decreasing. Figure 2.4.a shows the spectrum of a sample considered as a combination of crystalline silicon and amorphous silicon, and Figure 2.4.b. shows the simulated spectrum if we consider a mixture of polycrystalline silicon with large grains. The intensity of the peaks drops from a value of 38 to around 34 for $E_1$ and from 48 to 38 for $E_2$. However, $E_2$ is not only sensitive to the crystal fraction of the material. It is also widely sensitive to the surface state, especially when there is an oxide or some surface roughness. Figure 2.4.c. shows the influence of the surface oxide on the ellipsometric spectrum for various $SiO_2$ thicknesses. Oxide strongly lowers $E_2$ intensity. Thus, the measurements should be performed right after the deposition, so as to avoid the formation of native oxide that will modify the peak intensity, or must be taken into account when the measurement is performed too much time after deposition. The spectrum at low energies enables to have an insight on two parameters: the thickness of the layer, and the interface roughness. Figure 2.4d. is a zoom in the low energy range for various simulated samples with decreasing thicknesses of epi-layer. In this simulation, we considered an interface layer with 10% of void with a thickness of 1 nm. The thinner the layer, the larger is the period of oscillations. Also, the amplitude of the oscillations determines the quality of the interface. Indeed, as shown in Figure 2.4.e, adding in the simulation some "void", or anything that would lower the refractive index ($SiO_2$, H) increases the amplitude of oscillations. For a perfect interface, no oscillation can be distinguished[69]. Ellipsometry can also be used to determine the Ge content in $Si_{1-x}Ge_x$ alloys, and also to assess the GaAs oxide thickness.

### II.1.2.2. X-Ray diffraction

X-ray diffraction (XRD) is a highly powerful technique to get structural information on a crystalline material. It is a non-destructive characterization technique that enables to measure the lattice parameter of a crystal, its thickness, composition and strain. This technique has been used as a common routine to develop III-V ternary materials. In this manuscript, most XRD measurements presented will concern the development of Si and Si(Ge) materials by PECVD, and the assessment of the strain in the layer and its composition.

The XRD technique is based on elastic scattering of X-rays[72]. The interaction between incident X-rays and atoms must be considered. When an incident X-ray with a wavelength λ reaches a crystal, the rays are scattered by the atomic planes that are periodically arranged. Interferences between the scattered waves will happen for angles when the Bragg's law (Eq 2.1)) is verified. Figure 2.5. is the schematic representation of Bragg's law.

$$2d_{hkl}sin\theta = n\lambda \qquad \text{Eq 2.1}$$

$\boldsymbol{n}$ is the order of diffraction, $\boldsymbol{\lambda}$ the X-ray wavelength, $\boldsymbol{\theta}$ the angle between diffractive planes and the incident x-ray beam, and $\boldsymbol{d}$ the distance between those planes. Crystalline materials have a well-defined lattice constant, thus interplanar distance. When $\boldsymbol{\theta}$ satisfies the Bragg equation, the intensity diffracted is maximum. In general, for a tetragonal lattice, the distance $d_{hkl}$, is given by Eq 2.2)

$$d_{hkl} = \frac{h+k}{\mathrm{a}//} + \frac{l}{a\perp} \qquad \text{Eq 2.2}$$

where $\boldsymbol{h}$, $\boldsymbol{k}$ and $\boldsymbol{l}$ are the Miller indices, $\boldsymbol{a}_{//}$ is the in-plane parameter, identical in both x and y direction, and $\boldsymbol{a}_{\perp}$, is the out-of-plane parameter, corresponding to the parameter along growth direction, as schematized in Figure 2.7.a or b. Along {004} planes, $d_{004}$ gives us directly an information on $\boldsymbol{a}_{\perp}$, the out-of-plane parameter.

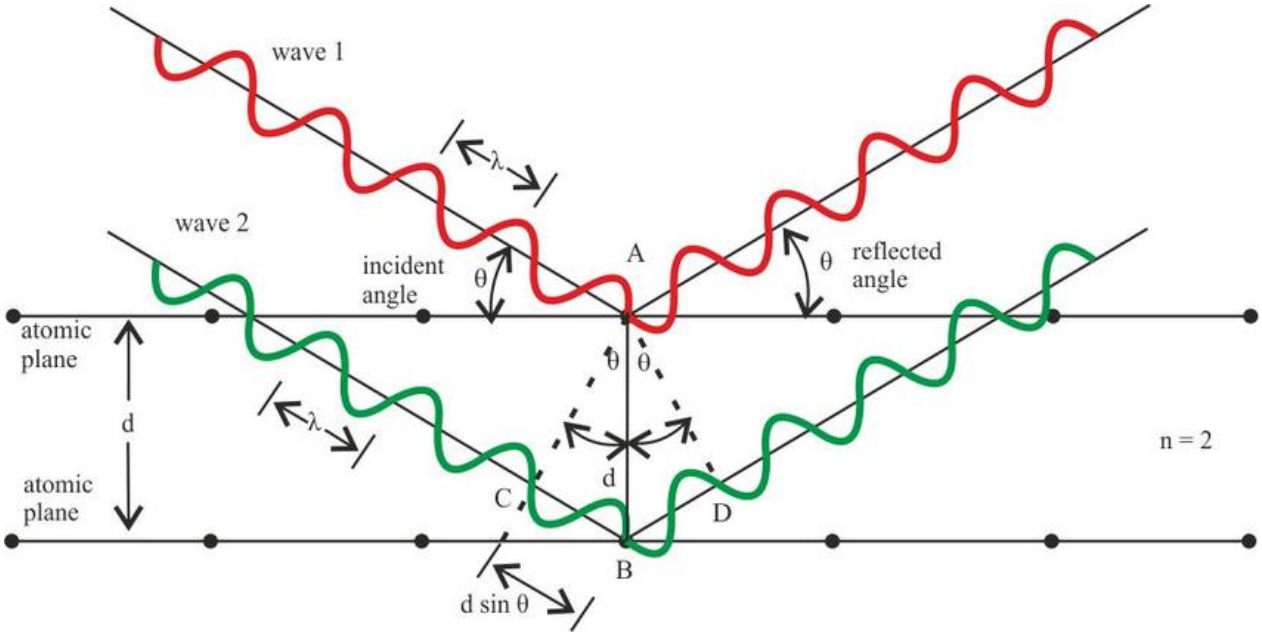



**Figure 2.5 - Schematic representation of Bragg's law**

In the case of an heteroepitaxial layer, two peaks will be distinguished, corresponding to the substrate and the layer. ω/2θ scan along {004} allows to find the thickness of the film, that induces oscillation, but also, the out-of-plane lattice parameter $\boldsymbol{a}_{\perp}$. As an example, Figure 2.6.a. shows simulated ω/2θ scans along {004} planes for $Si_{0.9}Ge_{0.1}$ crystal grown on top of a Si Substrate. The sharp peak around 69.15 ° corresponds to the Si substrate peak. The second peak corresponds to the layer peak. For different epi-layer thickness, two effects can be seen: first, for thinner layers, the intensity of the peak is lower, because the diffracting volume is low as compared with the substrate volume probed for a same measurement time integration. Second, the oscillations are linked to the thickness. The thicker is the layer, the higher is the oscillation period.

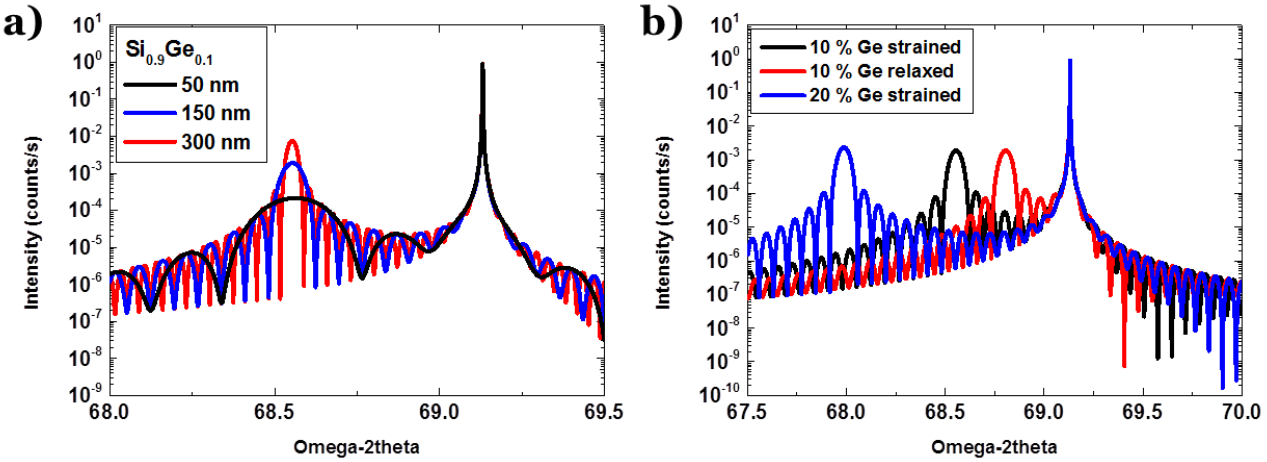



**Figure 2.6 - Simulation with Leptos software of a) $Si_{0.9}Ge_{0.1}$ layer with various thicknesses on a (100) Si substrate: the oscillation period and the peak intensity and FWHM are strongly dependent on the thickness b) Comparison of a strained $Si_{0.8}Ge_{0.2}$ layer with a strained $Si_{0.9}Ge_{0.1}$ and a relaxed one : the peak is shifted to the right when relaxed.**

In case of a strained film, the position of the layer peak is directly linked to the composition of the film. Figure 2.6.b shows the simulation of a strained SiGe film on Si with different Ge compositions (10 % and 20 % i.e. black and blue curves). The more Ge is incorporated, the higher is the lattice parameter of the crystal, thus the angle decreases (i.e. shifts to the left). However, this diffraction angle also depends on the strain of the layer. With only this scan, we do not have access to an information: the strain or relaxation of the film. In Figure 2.7 is represented the reciprocal space of an hetero-epitaxial stack. The purple dots correspond to the substrate and the pink ones to the layer, in case of a layer with higher lattice parameter than the substrate (which is the case of SiGe as compared with Si). {004} planes are framed in black. While performing an ω-2θ scan along these planes, we actually perform a scan along the vertical line. Figure 2.7.a. represents the case in which the layer is relaxed, thus has its own lattice parameter. Figure 2.7.b. corresponds to the strained case (compressive strain), when the in-plane parameter follows the substrate lattice parameter, leading to a deformation of the lattice with a higher out-of-plane parameter.

Thus, the strained case and the relaxed case will give different diffraction angles in ω-2θ configuration, as shown in Figure 2.7.a and b. Consequently, with only one ω-2θ scan along {004}, we will not be able to decorrelate the relaxation from the composition of the film. To do so, another scan, or more particularly a mapping of the reciprocal space (RSM) is needed. RSM are a gathering of ω/2θ scans offset starting with different ω angles. These mappings correspond to slices of the reciprocal space presented in Figure 2.7.a and b on the right. It typically requires much more time than a single ω/2θ scan. The asymmetric scan along {224} planes will be the most used because it gives information about the strain in the epitaxial film. The position of the substrate peak on a {224} asymmetric RSM will give us information on the state of the film: a fully strained film will present a diffraction peak vertically aligned with the substrate as seen in Figure 2.7.b, while a fully relaxed layer will have a diffraction peak following the line given by the origin of the reciprocal space and the substrate (Figure 2.7.a). Films that are partly relaxed will have peak position following the relaxation line drawn in Figure 2.7.c, with a relaxation rate R ranging from 0 (fully strained) to 1 (fully relaxed). An enlargement of the peak would be the proof of dispersion in film alignment, called “mosaicity”. The reciprocal space of such material together with a schematic of the atomic plane orientations is pictured in Figure 2.7.d. Mapping along {004} planes also contain information on the mosaicity of the sample. However, due to the long measurement time of both RSM (from 4 h

to 12 h depending on the precision required), only one RSM along {224} planes will usually be performed, coupled with one simple ω-2θ scan along {004} planes.

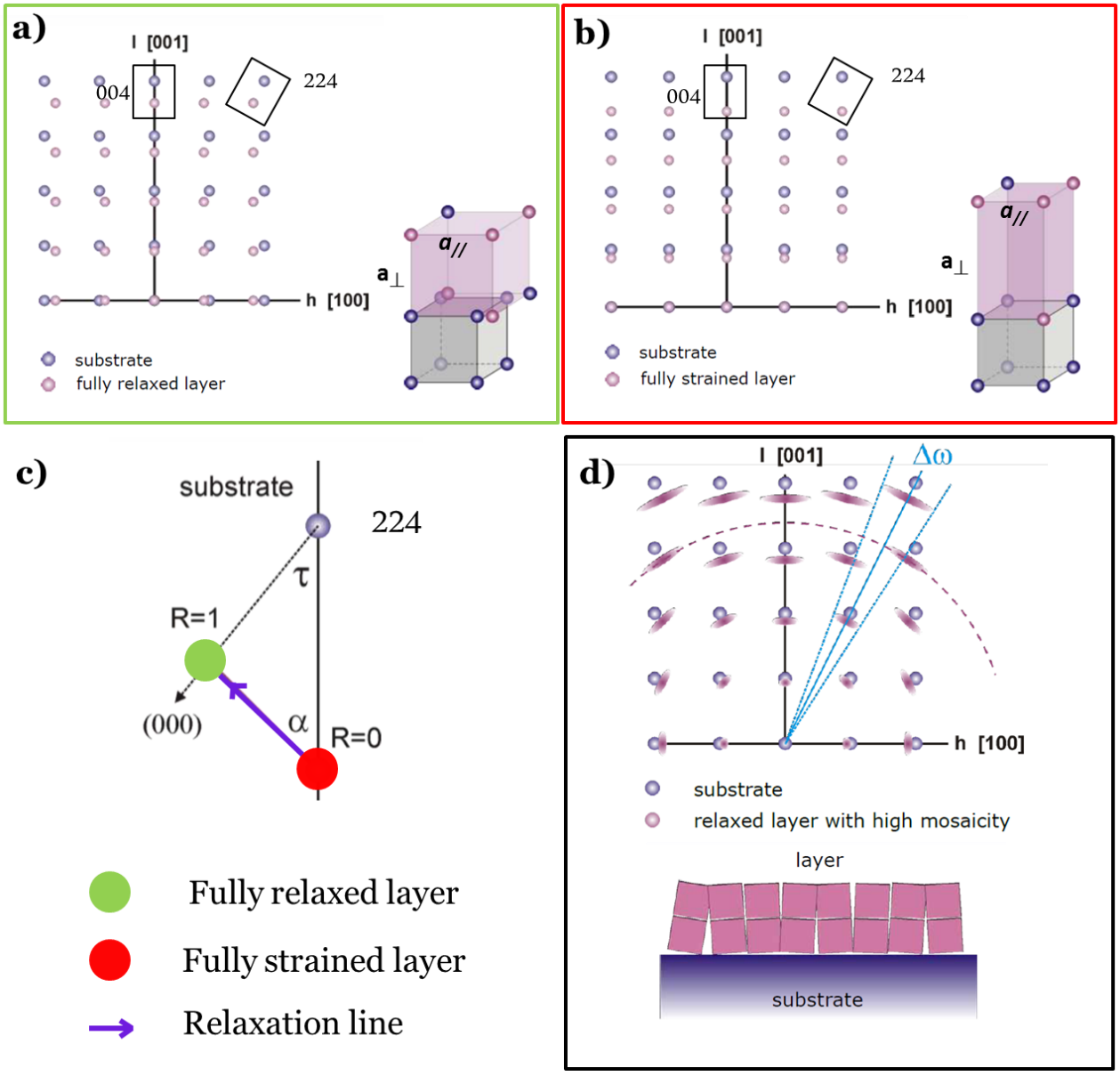



**Figure 2.7 - Schematic of the reciprocal space of an hetero-epitaxy considering a substrate with lower lattice parameter than the layer. Rectangles show the area that corresponds to reciprocal space mapping (RSM) along {004} planes and 224. a) In the relaxed configuration, b) in the fully strained configuration. c) The arrow represents the relaxation line for partly relaxed layer on along 224 planes. d) Reciprocal space schematics in case of relaxed layer with high mosaicity. (images: Bruker)**

The XRD setup used at LPICM is a Bruker D8, composed of a Cu tube for X-ray generation using the $K\alpha_1$ radiation ($\lambda$= 1.54056 Å). During this PhD, a rather new XRD equipment initially dedicated to powder analyses had to be understood, and set up to match our requirements at best. After optimization of the optics and finding compromises to suit for several applications in the lab, a fixed optical configuration has been chosen. Thus, for most of the experiments performed in this chapter, we used the following configuration for ω-2θ measurements as well as reciprocal space mapping: the primary beam optics (emission line) is composed of a Goebel mirror, a divergence slit set at 1.2 mm

large, and a double reflection Ge(220) monochromator to have a monochromatic incident beam. No back-monochromator was available in the lab. The detector is a linear detector of 14 mm, usually closed below 1 mm, and the detection arm includes a 1 mm large analysis slit.

Theoretically, epitaxially grown Si on a Si substrate should have the same lattice parameter as the substrate. We will see in this chapter that it is not always the case, and that in the case of Si grown with $SiH_4/H_2$ mixtures by low temperature PECVD, the epi-layer can have a slight different lattice parameter than the substrate, depending on the deposition conditions. X-Ray Reflection has also been also used to assess the density of our materials and determine the Ge content of $Si_{1-x}Ge_x$, but will not be presented in this manuscript, thus we do not present the technique despite its high interest in thin film characterization.

Thus, in this manuscript, ω-2θ scans to assess the out-of-plane parameter of the material and alloys grown are presented. The realization of 224 reciprocal space mapping will give us an insight on the relaxation of the layers. In Chapter 5, another configuration of XRD will be presented, that will allow having a precise measurement of the in-plane parameter: Grazing Incidence X-Ray Diffraction (GI-XRD). This configuration has been used on DiffAbs line of Synchrotron SOLEIL.

#### II.1.2.4. Other characterizations mentioned in this manuscript

**Atomic force microscopy (AFM)**[73] is a high-resolution scanning probe microscopy that enables to measure surface topography, and thus surface roughness with a precision below 1 nm. This non-destructive characterization will be used to assess the surface roughness of the materials after in-situ etching and after growth.

**Scanning electron microscopy (SEM)**[74] scans a sample surface with a focused beam of electrons. The interaction between the electrons and the atoms of the surface provides information about the sample surface topography and composition, with a resolution better than 1 nm. It is a destructive characterization technique that needs a cleavage of the sample when we want to investigate a cross-section.

**Transmission electron microscopy (TEM)**[75] is a microscopy technique in which a focused beam of electrons is transmitted through a thin sample (< 100 nm thick) than have been previously prepared. It allows to have a precision at the atomic scale and to distinguish atom arrangements, and the contrast can differentiate the different atom species.

**Secondary-ion mass spectrometry (SIMS)**[76] allows analyzing the composition of a sample along its depth by sputtering its surface with a focused ion beam. The ejected secondary ions are collected and measured thanks to a mass spectrometer. This technique is essential when it comes to analyze scarce atoms that do not constitute the crystal, such as O, H or C impurities, or dopant atoms. The measurements presented in this PhD were performed at Prob*Ion* Analysis.

**Electrochemical Capacitance-Voltage (ECV)** is a profiling technique used to measure the active carrier concentration profiles, thus the doping level. This technique will be presented more in details in Chapter 4.

**Raman Spectroscopy** [77] is a non-destructive characterization technique to get an insight on the chemical and structural composition of a layer. A laser is sent to a sample, and its light will interact with molecular vibrations, and phonons, resulting on a shift of the photon energies that are scattered by the material compared to the incoming photon energy. This shift gives us information about the vibrational modes in the system. For example it can assess easily the crystallinity of a Si sample

**Hall Effect** measurements[78] have been performed on some samples to assess the doping level of a film. It requires growing the doped film on an intrinsic substrate or a silicon-on-insulator (SOI) substrate.

**Profilometer** measures a surface's profile, in order to quantify its roughness. We used contact profilometers, in which a probe is physically moving in contact with the surface to acquire its height. This is done mechanically with a feedback loop that monitors the force from the sample pushing up against the probe as it scans along the surface

Part II.1. has been dedicated to the presentation of the PECVD growth technique used in this chapter as well as in Chapter III of this manuscript. We also presented the principle of the main characterization tools used to characterize PECVD grown Si and SiGe materials. Some of these tools are also used to characterize III-V materials as it will be seen in Chapters 4 and 5. We propose now to get to the heart of the subject: the epitaxial growth of thick crystalline Si and SiGe materials by LT-PECVD. We will study their structural properties (Chapter II.2. Low-Temperature Epitaxy of Si and SiGe by PECVD). Later, the electrical properties of such layers will be assessed by fabricating heterojunction solar cells (Chapter II.3. Solar cell ).

# II.2. Low-Temperature Epitaxy of Si and SiGe by PECVD

## II.2.1. Growth parameters

### II.2.1.1. Silane/hydrogen dilution

The optimum growth conditions for crystalline silicon on (100) Si have already been carried out in our laboratory in several reactors[79] (Philix, Arcam, Cluster tool). At high pressure and fixed temperature (below 200 °C), the importance of silane dilution in $H_2$ has been shown to be the main crucial parameter for epitaxial growth. For a fixed $H_2$ flow rate, with a low silane flux, the deposited material was microcrystalline, and a high silane flux resulted in an amorphous material. Figure 2.8.a. shows the calibrations made on Arcam reactor reported in the following paper[79]: for a fixed $H_2$ flow rate and other parameters (RF power, pressure, deposition temperature), $SiH_4$ flow rate was varied from 0 to 50 sccm. The graph shows the crystalline fraction as deduced from the modelling of ellipsometric spectra. The right axis represents the deposition rate calculated for each $SiH_4$ flow rate. Figure 2.8.b. represents the results obtained in the new Octopus reactor by fixing the $H_2$ flow rate at 500 sccm, for a growth temperature fixed at 200 °C, a RF power of 50 W and a pressure of 2 mbar. The same behavior can be observed in both reactors: the more $SiH_4$ is introduced in the plasma, the higher is the deposition rate, which is of course consistent with the fact that more Si atoms are available to be incorporated on the layer. However, the layer is fully crystalline for a silane

flow rate between 20 sccm and ~42 sccm. The optimum conditions are slightly different from one reactor to another, but the trend remains similar. For most of the deposition presented in this chapter, the silane flow rate will be fixed at 35 sccm. This value is far enough from the border of the process window for which the growth is amorphous, but high enough to ensure a sufficient deposition rate above 1.5 Å/s.

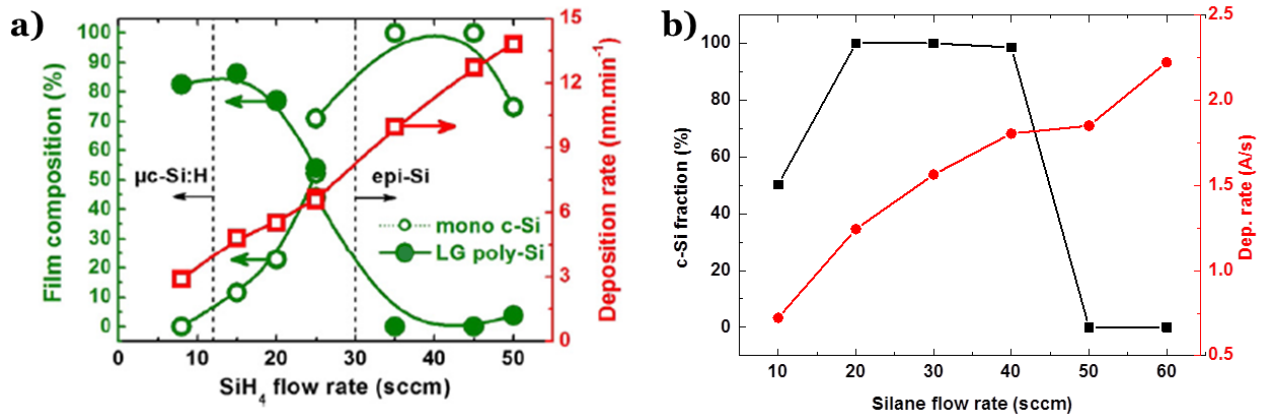



**Figure 2.8 - Deposition rate and percentages of monocrystalline silicon, as deduced from spectroscopic ellipsometry measurements, plotted as a function of the silane flow rate. a) from Roca I Cabarrocas et al.[22] in Arcam reactor, b) in Octopus reactor**

### II.2.1. 2. Surface cleaning of Si substrates

During this PhD, all the depositions have been performed on (100) oriented crystals (Si or GaAs). Low temperature epitaxial growth is known to be more difficult on (111) oriented surface even if it has recently been suggested that it was possible at very high power at 250 °C [Leal's thesis, to be published]. The preferential growth on (100) can be explained by the surface state of the wafer: in a (100) orientation, each Si atom has to form two covalent bonds with the underneath planes in order to be incorporated in the lattice. On (111) surfaces, the impinging Si needs to form only one bond with the underlying plane (and three with the upper planes), which gives more degrees of freedom for an amorphous growth.

#### Wet cleaning

Surface preparation is crucial in order to have epitaxial growth. First, there is a native oxide that is formed naturally on the c-Si substrate exposed to air, that is usually about 1.5 nm thick. This native oxide also contains all sorts of impurities such as organic compounds, traces of metals, etc. This $SiO_2$ layer is not only an electrical barrier for carriers, but also prevents from low temperature epitaxial growth as it is an amorphous layer. A review of the surface cleaning solutions can be found in a paper from Kern[80].For these deposition, surface treatment of Si wafers was performed by dipping them into a 5% solution of HF right before loading the wafer into the PECVD reactor. The oxide indeed quickly regrows after air exposure. Exposition to air for more than one hour will induce a too high $SiO_2$ thickness. Consequently, the samples are loaded into the reactor in the few minutes or tens of minutes that follow the HF dipping.

## Dry cleaning

HF is extremely corrosive and risky to handle, thus requiring many precautions. For safety reasons, but also for practical reasons (PhD students are not allowed to handle it by themselves), in-situ dry cleaning has been proposed and developed in the lab. It was proposed to use $SiF_4$ dry plasma to clean the surface. $SiF_4$ is commonly used in combination with Ar and $H_2$ in our reactors to grow microcrystalline silicon[81,82], and more recently, crystalline Si[69]. This plasma has also been shown to be efficient in cleaning Si surfaces for PECVD epitaxial growth [83]. In that work, the authors exposed a wafer containing a native oxide to several $SiF_4$ plasma conditions while monitoring by in-situ ellipsometry the second peak of crystalline silicon, which is linked with $SiO_2$ thickness, as introduced in Figure 2.4.c. They showed a maximum amplitude of $e_2$ after a certain time (300 s, which depends on the reactor used). An additional $H_2$ plasma of a few seconds (~30 s) is performed after the cleaning in order to remove F atoms that may remain at the surface, to produce a H-terminated surface. It was then shown that an epitaxial growth can occur on top of such a cleaned wafer[84].

a)

| Step | $SiF_4$ (sccm) | $H_2$ (sccm) | $SiH_4$ (sccm) | Pressure (mbar) | RF power (W) | Temperature (°C) | Time (min) |
|---|---|---|---|---|---|---|---|
| Oxyde etching | 30 | - | - | 0.8 | 75-125 | 175 | 5' |
| $H_2$ Plasma | - | 500 | - | 2.5 | 50 | 175 | 30'' |
| Epi-Si growth | - | 500 | 35 | 2 | 50 | 175 | 5' |

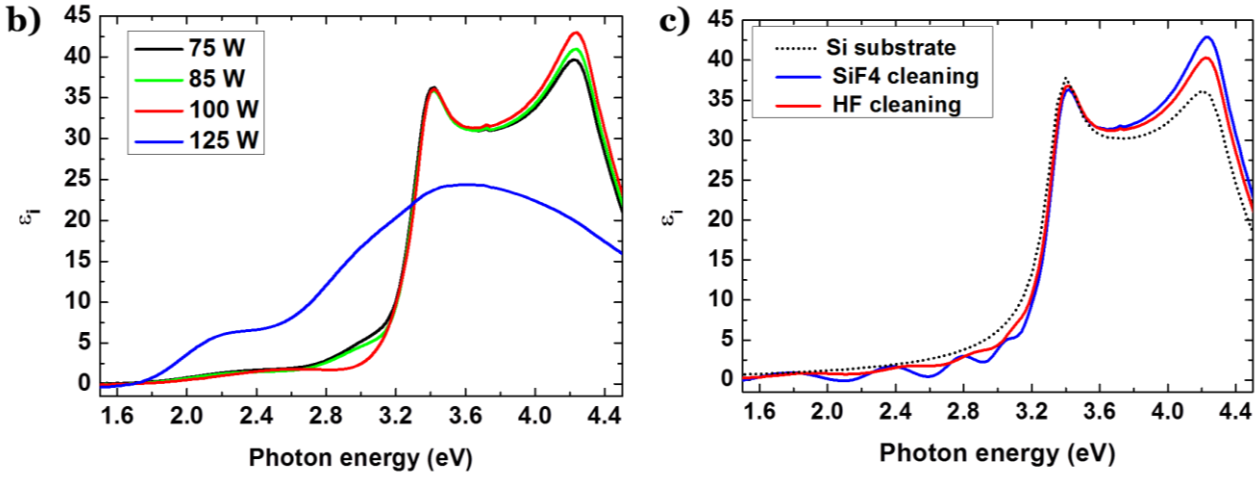



**Figure 2.9 - a) Optimized cleaning and deposition conditions in Octopus reactor, b) ellipsometric spectra of 5 minutes growth Si after cleaning at various values of the RF power c) comparison of the best SiF4 cleaning with HF cleaning, along with the substrate reference**

Figure 2.9.a. shows the plasma condition used in Octopus reactor for in-situ $SiF_4$ cleaning and Si deposition. On several (100) Si substrates (with native oxide), a 5 mn plasma etching has been performed on the Si substrate with various RF power values ranging from 75 W to 125 W, followed by a 30 seconds $H_2$ plasma, and a 5 mn growth of silicon in epitaxial conditions. The resulting ellipsometric spectra are presented in Figure 2.9.b. We see that epitaxial growth is happening for RF power values ranging from 75 W to 100 W. $E_1$ intensity are similar for each of these RF powers, and the best value for $E_2$ is reported for a plasma power of 100 W. For 125 W, the film grown is fully amorphous. Thus, the best cleaning conditions have been found to be: 5 mn of $SiF_4$ plasma at 175 °C

with a pressure of 0.8 mbar, 30 sccm of $SiF_4$ and a RF power of 100 W. Figure 2.9.c compares for similar growth time (~ 16 minutes), the ellipsometric spectra of epi-Si films grown on a HF cleaned wafers and a wafer cleaned with $SiF_4$ plasma. The spectrum of the "out-of-box" Si substrate (that has a native oxide) is plotted in dashed line. We notice that the crystalline quality, as judged by $E_2$ intensity, is a bit higher for $SiF_4$ cleaning. However, looking at the oscillations at low energies, the $SiF_4$ cleaning shows a wider amplitude. As introduced in Figure 2.9.e, it suggests that the interface between the substrate and the epitaxial layer is less smooth than that of HF cleaned sample.

Two main ways of cleaning the surface of Si substrates prior to epitaxial growth have been presented: 1) by dipping the wafer into 5% diluted HF, or 2) by using $SiF_4$ in-situ plasma cleaning followed by a short $H_2$ exposure. In this chapter, all the samples grown in Octopus will be prepared with HF (when the contrary is not specified). Also, in the next chapters, (especially Chapter III), in-situ cleaning will turn out to be essential for GaAs surface preparation prior to the heteroepitaxial growth of Si on GaAs. More details will be given in due time.

## II.2.2. Effect of annealing on a 1.5 µm thick epi-Si layer: structural analysis

We just presented experimental background on the growth of epitaxial silicon on (100) Si wafers, and especially its transfer from the old Arcam reactor to the new industrial Octopus reactor: the importance of $SiH_4$ flux for the film crystallinity. As the tandem solar cell targeted in this PhD requires a thick Si layer, we aim at growing thick epi-Si on Si. This section is dedicated to the material study of a layer of 1.5 µm on (100) Si substrates, and the effect of annealing at different temperatures on the structure of the epi-Si, in order to assess its stability over annealing. Then, thicker layers up to 10 µm will be grown and their quality will be assessed. The best conditions for growing epitaxial Si on (100) c-Si substrates in an industrial PECVD reactor Octopus have been used (HF cleaning + epi-Si conditions of Figure 2.9.a). Prior to each growth, the chamber is cleaned with in-situ $NF_3$ plasma, and a precoating of the chamber walls is performed with a-Si:H for 5 minutes.

Thick intrinsic (non-intentionally doped) epi-Si films are grown on top of 525 um thick p-doped c-Si substrates at 200°C. Prior to epitaxial growth, the wafer native oxide was removed by dipping the substrate into 5% diluted HF for 30 seconds. A 1.5 µm thick Si layer has been deposited on several

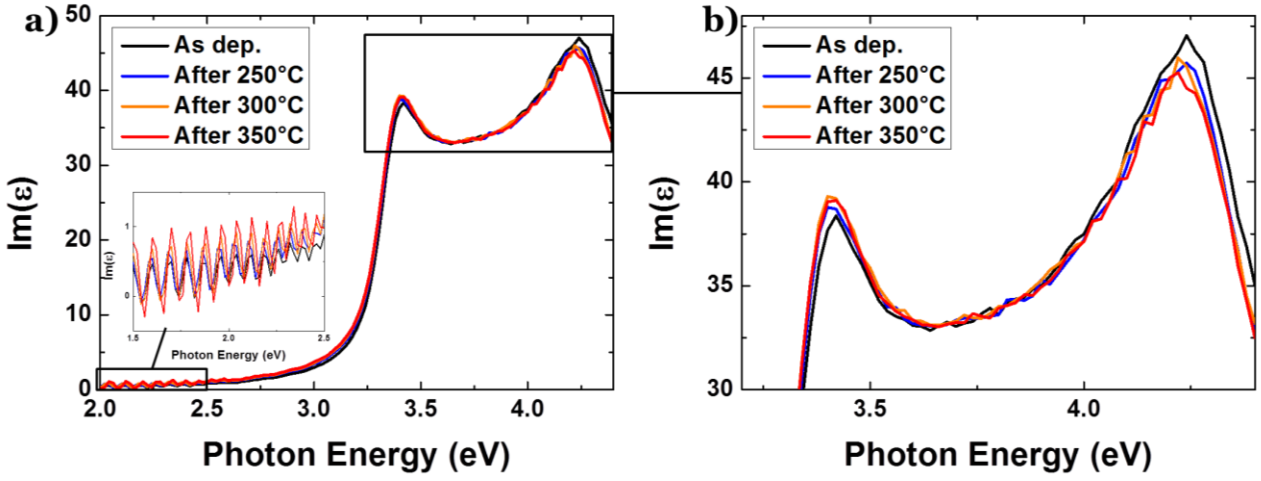
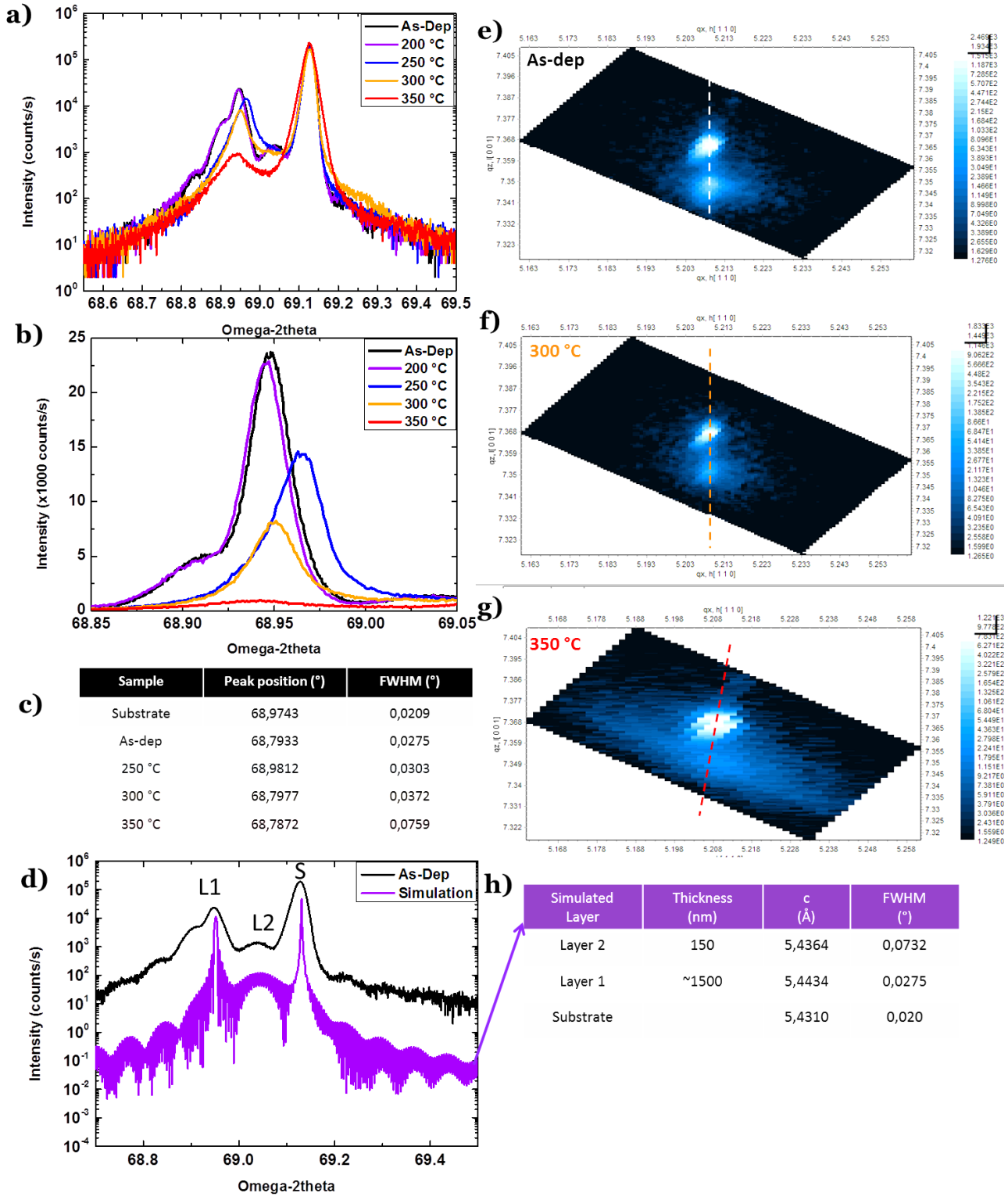



**Figure 2.10 - a) Ellipsometric spectra of of the samples as-deposited, and annealed at 250°C, 300 °C and 350 °C, along with a zoom on the low energy oscillations b) zoom on the characteristic peaks at $E_1$ and $E_2$**

identical 4 inch wafers, from the dissociation of an $SiH_4/H_2$ mixture, with a pressure of 2 mbar and a RF power of 50 W, using 500 sccm of $H_2$ and 30 sccm of $SiH_4$. The growth was performed at 200 °C. Then, the substrates were cut, and 5 different samples have been studied. One is kept in the as-deposited state, and 4 others have undergone an annealing step, using a rapid thermal annealing of 3 minutes under forming gas, with temperatures ranging from 200 °C to 350 °C. We present here first the material studies in order to assess the structural impact of these annealing. The imaginary part of the pseudo-dielectric function of the samples is shown in Figure 2.10.a. It exhibits the two characteristic peaks of crystalline silicon, with an $E_2$ peak intensity above 45, and an $E_1$ peak around 38. By looking closely to this peak Figure 2.10.b, we see that increasing the annealing temperature seems to slightly increase the $E_1$ value, thus the crystalline quality.

XRD analyses of the same samples were then performed to confirm these behaviors, and are reported in Figure 2.11.a. The first observation that can be made is that, even if we are having an homoepitaxial growth of Si on Si, two different peaks can be distinguished. On the right at 69.15 degrees, is the diffraction peak due to the Si substrate, and on the left, a second peak corresponding to the epitaxial layer can be distinguished. This difference in diffraction angle has already been observed on PECVD epi-Si materials: its intrinsic lattice parameter is slightly different from a bulk substrate Si, and this difference is widely dependent on the growth conditions, mainly hydrogen content [85–87]. Epi-Si has a bigger out-of-plane lattice parameter than bulk-Si. The intensity of the peak of the as-deposited sample and its FWHM (below 0.03 °) demonstrate very good quality of the grown film.

For the as-deposited and annealed at 200°C samples, the diffractograms are similar. This result is understandable, as annealing temperature is the same as growth temperature. No significant change in the crystalline structure has occurred. On both curves, we can distinguish some fringes that correspond to a certain thickness. But the oscillations due to a 1.5 µm thick layer would have a periodicity so low that we could not distinguish it with our measurement set up (see Figure 2.11.b). Thus, we performed simulations with Leptos software, in order to understand the origin of these oscillations. Figure 2.11.d. shows on the same curve the diffractograms of the as-deposited sample along with a simulation that fits with the peaks position and the oscillation periodicity. As expected, the oscillations due to the 1.5 µm sample are very narrow. The wider oscillations have been fitted by adding a second layer and changing its thickness. Actually, to really match the experimental results, it revealed that the small peak in-between the substrate and the layer peak is not an oscillation but an actual peak corresponding to a layer that has another lattice parameter. Figure 2.11.h. gathers the main parameters of the fitted layers: their peak position, the corresponding lattice parameters, the FWHM and the layer thickness. While the epitaxial layer is found to have a lattice parameter of 5.443 Å, the second layer that we can distinguish has a lattice parameter closer to that of the substrate, 5.436 Å, and a thickness of 150 nm. XRD does not provide the possibility to know where this layer is located. It can be located on top of the layer, or at the interface between the substrate and the epitaxial layer corresponding to the first stages of growth.




| Sample | Peak position (°) | FWHM (°) |
|---|---|---|
| Substrate | 68,9743 | 0,0209 |
| As-dep | 68,7933 | 0,0275 |
| 250 °C | 68,9812 | 0,0303 |
| 300 °C | 68,7977 | 0,0372 |
| 350 °C | 68,7872 | 0,0759 |

h)

| Simulated Layer | Thickness (nm) | c (Å) | FWHM (°) |
|---|---|---|---|
| Layer 2 | 150 | 5,4364 | 0,0732 |
| Layer 1 | ~1500 | 5,4434 | 0,0275 |
| Substrate | | 5,4310 | 0,020 |

**Figure 2.11 - ω-2θ XRD scans of the samples before and after annealing at different temperatures a) in logarithmic scale, b) zoom on the film peak in a linear scale. c) Peak position and FWHM for each sample, d) Leptos simulation of the as-deposited sample. Reciprocal space mappings of {224} planes on e) as-dep sample, f) 300°C annealed sample, g) 350 °C annealed sample. h) fit parameters obtained from simulation of as-deposited sample.**

After annealing, the film peak is widely impacted. To have a better insight on the effect on the film peak shapes, Figure 2.11.b. shows those peaks in a linear scale. The peak positions and peak FWHM are gathered in Figure 2.11.c. First, we do not see the oscillations previously studied, nor the peak in between. We may believe that this layer has been accommodated either the substrate lattice parameter, or to the layer. It is also possible that the distribution in lattice parameter of this peak is smoother, leading to a high FWHM that does not allow us to distinguish the peak nor the thickness fringes. Contrary to what we could have deduced from ellipsometry, the XRD measurements show a reduction in intensity of the layer peak, thus in film quality. At 250 °C, the intensity drops, and the substrate peak is shifted. Thus, the quality has been affected, and the lattice parameter of the layer has been slightly lowered. Then, for higher annealing temperature, the peak intensity keeps on decreasing. The diffraction angle is back to its as-deposited value. We do not really explain why the 250 °C has shifted in lattice parameter whereas higher temperature does not change it. At 350 °C, the XRD film peak is drastically decreased (red curve), with a large FWHM above 0.07 °. The peak substrate also seems to be wider, this shape often corresponds to a relaxed layer.

Reciprocal space mapping (RSM) on {224} planes has been performed in order to have an insight on the relaxation of the layers. We show in Figure 2.11 the {224} RSM of three samples: e) as-deposited, f) annealed at 300 °C, g) annealed at 350°C. On each mapping, the intense substrate peak can be seen on top, above a second peak. For as-dep and 300 °C annealed samples, the film peak is vertically aligned below the substrate peak, which means that the film is fully strained by the substrate: the in-plane parameter $\boldsymbol{a}_{//}$ is equal to that of the substrate. The same behavior is found for the 200 °C and 250 °C annealed samples, as well as the 300°C annealed sample, as seen in f). However, as far as the 350 °C annealed sample is concerned, we see that the layer peak is shifted to the left, resulting in a partly relaxed film. Furthermore, the widening of the peak is characteristics to the mosaicity of the layer following {224} planes, as introduced in the description part, Figure 2.7.d. Thus, the atomic planes of this layer are not fully aligned together nor with the substrate planes. There is a slight dispersion in horizontal atomic planes orientations.

Microscope images of the surface of the samples are presented in Figure 2.12. While the surface seems to be smooth for low temperature annealing and up to 300 °C, we notice that the 350 °C annealed sample presents some “bubbles”. This is attributed to the presence of hydrogen in the layer. Heating above 350 °C causes the formation of $H_2$ molecules that accumulate at hydrogen traps, mainly the interface between the epi-layer and the Si layer. This phenomenon is called blistering[88]. This result is actually consistent with the behavior seen at low energies in the ellipsometric spectrum. As seen in the inset of Figure 2.11.a, the 350 °C annealed sample has much

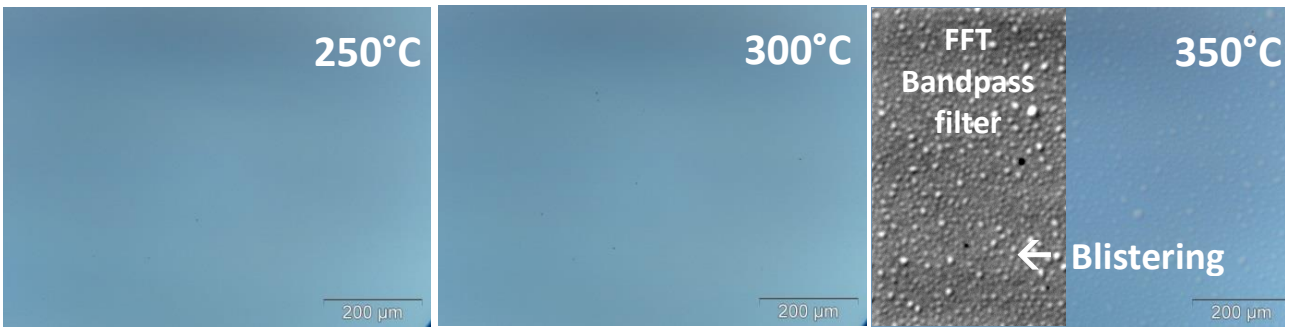



**Figure 2.12 - Optical microscope images of the sample surface for different annealing temperatures**

wider amplitude than the other samples. It is the proof that the interface between the substrate and the epitaxial layer contains a low optical index material, such as $SiO_2$, a high roughness modelled by a "void" material, or, most probably in our case, hydrogen. The presence of these $H_2$ bubbles also explains the mosaicity observed in RSM {224} measurements, because they would be responsible for local bending of the layer. Also, the formation of bubbles at the interface between the substrate and the film lowers the strain induced by the substrate crystal lattice, hence the relaxation of the grown film for the blistered sample.

Actually, the blistering of epi-Si also depends on the film thickness. We have observed on other samples that thin epitaxial Si layer (below 500 nm) does not lead to such blistering after 350 °C annealing. This may be due to the fact that hydrogen can more easily reach the surface and exodiffuse out of the sample, while thicker layers contain more hydrogen, that have more probability to meet another hydrogen in the layer before being exodiffused.

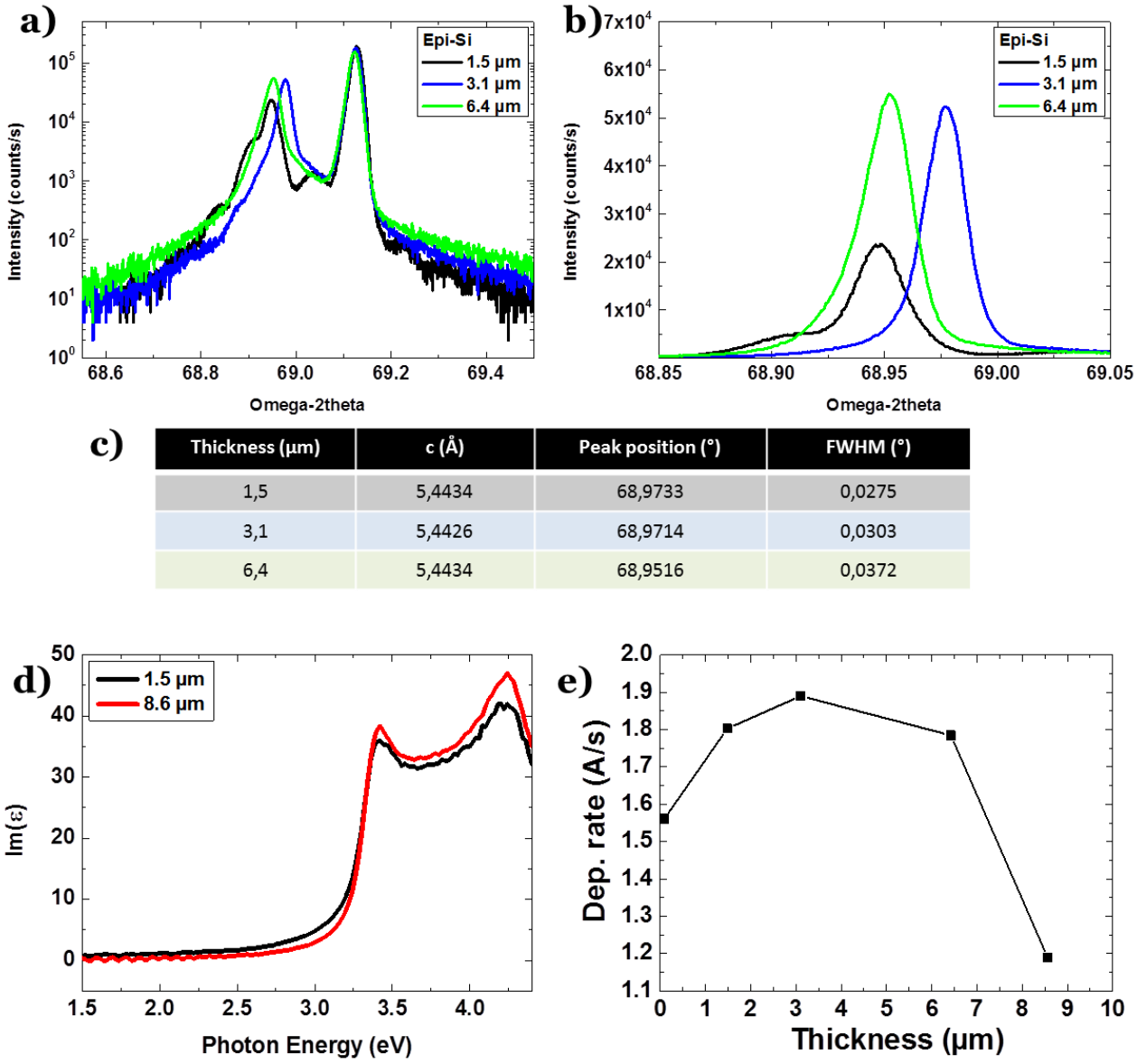
The material studies of the 1.5 µm-thick epitaxial Si film grown by PECVD before and after annealing showed that the crystalline quality of the film is very good for as-dep and 200°c annealed samples, as proven by XRD measurements. For higher annealing temperatures, the ellipsometric spectra show a higher amplitude of the peak at $E_1$, while X-ray diffraction shows a reduction in the diffracting volume as temperature increases. These different trends may come from the fact that at $E_1$ = 3.4 eV, the photons are probing only the top part of the film, (the penetration depth is in the range of 10 nm), while XRD probes the whole volume. After a 350 °C annealing, two phenomena are observed: the film is relaxed, and some $H_2$ blisters start to appear, leading a strong mosaicity of the film, and its relaxation.

We will thus have to keep in mind that the thermal budget is crucial in keeping a high Si quality and to prevent blistering of the layer. We will avoid as much as possible to anneal epitaxial Si films deposited at 200 °C to temperatures above 300 °C.

## II.2.3. Towards thick epi-Si layers

For the targeted tandem device, we are willing to grow thick layers of Si. We try here to assess the quality and electrical properties of epi-Si. It has already been reported that a critical thickness is often observed, above which epitaxy breaks down into amorphous or polycrystalline material[89]. While the optimization of the growth conditions, mainly the $SiH_4/H_2$ ratio, has shown a strong dependency of the crystal quality for low thicknesses. If the deposition parameters are slightly different from the optimum value, an epi-breakdown can occur. Epitaxy breakdown has been studied by Eaglesham *et al*[89]. using MBE below 500 °C, who reported an abrupt transition between epitaxy and amorphous deposition and proposed several origins of such breakdown: 1) the defect accumulation in epi-layer that continuously buildup lattice disorder in the epitaxial layer, 2) the segregation of H or impurities that modifies surface coverage, 3) the roughening of the surface. Indeed, low temperature epitaxy of Si often leads to a surface roughening that increases over deposition time[90,91]. It appears that the lower the growth temperature is, the lower the critical thickness for epi-breakdown. Thus, we may worry about the growth of thick epi-Si layers (> 10 µm).

Previous studies have already performed at LPICM using in-situ ellipsometry during growth, and showed no epitaxy breakdown for the used conditions[92]. Actually, it even showed an increase in the quality during the growth by probing the intensity of $E_2$ during the growth.




| Thickness (µm) | c (Å) | Peak position (°) | FWHM (°) |
|---|---|---|---|
| 1,5 | 5,4434 | 68,9733 | 0,0275 |
| 3,1 | 5,4426 | 68,9714 | 0,0303 |
| 6,4 | 5,4434 | 68,9516 | 0,0372 |

**Figure 2.13 - a) ω-2θ XRD scans of samples with various thicknesses: 1.5 µm, 3.1 µm and 6.4 µm, b) zoom on the epi layer peak in linear scale, c) lattice parameter, peak position and FWHM deduced from XRD data d) ellipsometric spectra of 1.5 µm and 8.6 µm samples, e) evolution of deposition rate as a function of the thickness of the film.**

With the same experimental conditions than in previous part, thicker absorbers were grown on top of p++ Si wafers. The ellipsometric spectra of the thicker layer (8.5 µm) is plotted in Figure 2.13.d., together with the previous 1.5 µm layer spectrum. We see that there is no epitaxy breakdown, and that moreover the crystallinity seems to have improved, as judged by the higher intensity of both $E_1$ and $E_2$ peaks. The low energy part does not provide enough information to determine the actual thickness of the layers. Thus, the thickness has been assessed by performing SEM images. The deposition rate (thickness/time) is actually not linear along deposition time. We plot on Figure 2.13.e the deposition rate calculated as a function of the layer thickness. We see that the deposition rate for a small thickness (below 100 nm) is around 1.55 Å/s. For thicker layers, it increases up to 1.8 - 1.9 Å/s. The possible explanation for such an increase in deposition rate could be the thermalization of the substrate holder. The substrate may not had time to be at the stable

temperature of 200 °C for the thin calibration sample (only 10 mn deposition), resulting in a lower growth rate. However, for the thicker layer that we grew (8.5 µm), the deposition rate has dropped to 1.2 Å/s. No in-situ characterization is available in the reactor, thus we cannot assess the evolution of the deposition rate over time, and thus, we do not have more information on the possible different stages in the growth.

XRD analyses of the different samples are gathered in Figure 2.13.a. with a zoom on the peak in Figure 2.13.b. We had troubles in measuring the 8.5 µm thick sample because of alignment issues. Figure 2.13.c. gathers the corresponding lattice parameter and FWHM. As expected, the intensity of the layer peak increases with the thickness. The FWHM remains good (below 0.04°) but slightly increases with thickness, showing a slight decrease in crystal quality or a bigger mosaicity. {224} RSM (not presented here) have shown that the layers remain strained for each measured layer, but that the layer peak is widened.

The SEM cross section images of each sample are gathered in Figure 2.14.(a to d). The epitaxial layer is easy to distinguish from the substrate, as it appears darker due to the presence of hydrogen. The thickness measurements of the layer were done based on these images. While up to 6.5 µm the layer seems homogeneous, the 8.8 µm one show a very inhomogeneous layer. Several contrasted layers can be observed, probably due to several hydrogen contents in the layers. This is not consistent with the fact that the 6.5 µm growth happened homogeneously. We actually believe that there were issues during the process, probably due to plasma instability or shut down.

Another interesting feature can be detected: the surface of the sample contains lots of defects as big as the deposited layer, as seen in Figure 2.14.e and f. Acetone cleaning under ultra-sounds did not remove those defects that are not volatile powders. The size of the defects, comparable to that of the deposited layer thickness, as well as the fact that is seems to have some craters formed around the defects lead us to one hypothesis: a deposition of thick particles has occurred during the growth, probably a peeling from the walls of the reactor. A more specific investigation of the surface has been performed in order to know the nature of these defects. Raman spectroscopy has been performed on several areas of the surface. Figure 2.14.g shows the microscope view of where the Raman measurements have been performed. We investigated two spots: the defect (red spot) and the surrounding material (blue spot). As seen in the Raman spectrum Figure 2.14.h, the defect has a signature of an amorphous layer, with a Raman shift around 490 $cm^{-1}$, which may come from the amorphous layer that is deposited in the meantime in the chamber walls. After a certain growth time, the walls of the chamber accumulate some deposition of amorphous silicon, and start peeling under its strain. In this reactor, the samples are not place upside down, but at the bottom. Thus, when the reactor walls start peeling, parts of amorphous layers fall down on the wafer surface. Meanwhile the PECVD growth keeps on happening around these amorphous defects, and the material deposited stays crystalline, as it is revealed by its Raman signature of the blue spot, with high intensity at 520 $cm^{-1}$.

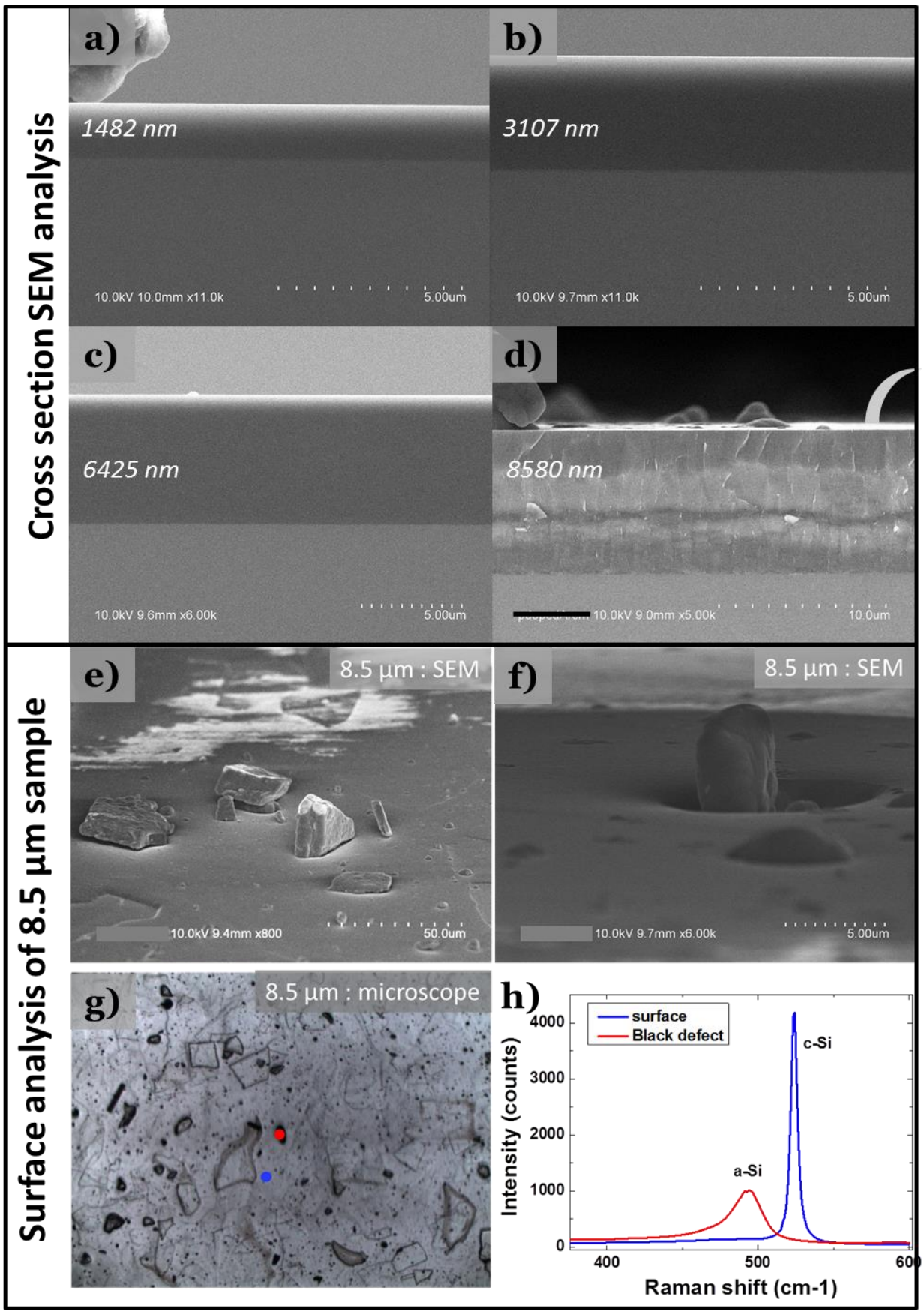



**Figure 2.14 - a)b)c)d) cross-section SEM analysis of samples with thicknesses of 1.5 µm, 3.1 µm, 6.4 µm, 8.5 µm, along with the thickness measured thanks to this image. e)f) SEM images of the surface of the 8.5 µm sample, g)h) Raman spectroscopy spectra of the material on different surface spots : a defect, and the smooth surface of the film**

## Conclusions and perspectives to grow thicker epi-Si

The growth of thick Si layers with good crystalline quality up to 6. 5 μm has been achieved, with a deposition rate around 1.8 Å/s. For higher thicknesses, it resulted in a material that is still crystalline as judged by the ellipsometry and the Raman shift, but that seems inhomogeneous, and especially that suffered from the peeling of the PECVD reactor walls. A possible solution for further enhancement of the epi-Si thickness is to unload the sample from the chamber after a certain thickness (about 6 μm), clean the chamber with in-situ $NF_3$ plasma, and perform a small precoating of the chamber with another grounded electrode (the previous one is a sample holder). If the sample is kept under vacuum in the load-lock, it can be reinserted in the clean deposition chamber so as so pursue the growth. This solution has not been tested yet, but is one of the main perspectives to grow Si layers thicker than 10 μm. Also, an issue that remains is the low deposition rate, which is around 1.8 Å/s under the present conditions. To grow this 8.5 μm layer, the deposition lasted 20 hours, which is way too much to be implemented in industry. Routes to improve this deposition rate are under study, and a deposition rate of 8.3 Å/s has already been achieved in our lab [85], leading to a highly hydrogenated crystalline silicon that contains amorphous cones. The use of Octopus with its high purity vacuum and the possibility to grow at temperatures up to 400 °C opens the path to growing good epi-Si at high growth rates.

## II.2.4. SiGe: material calibration

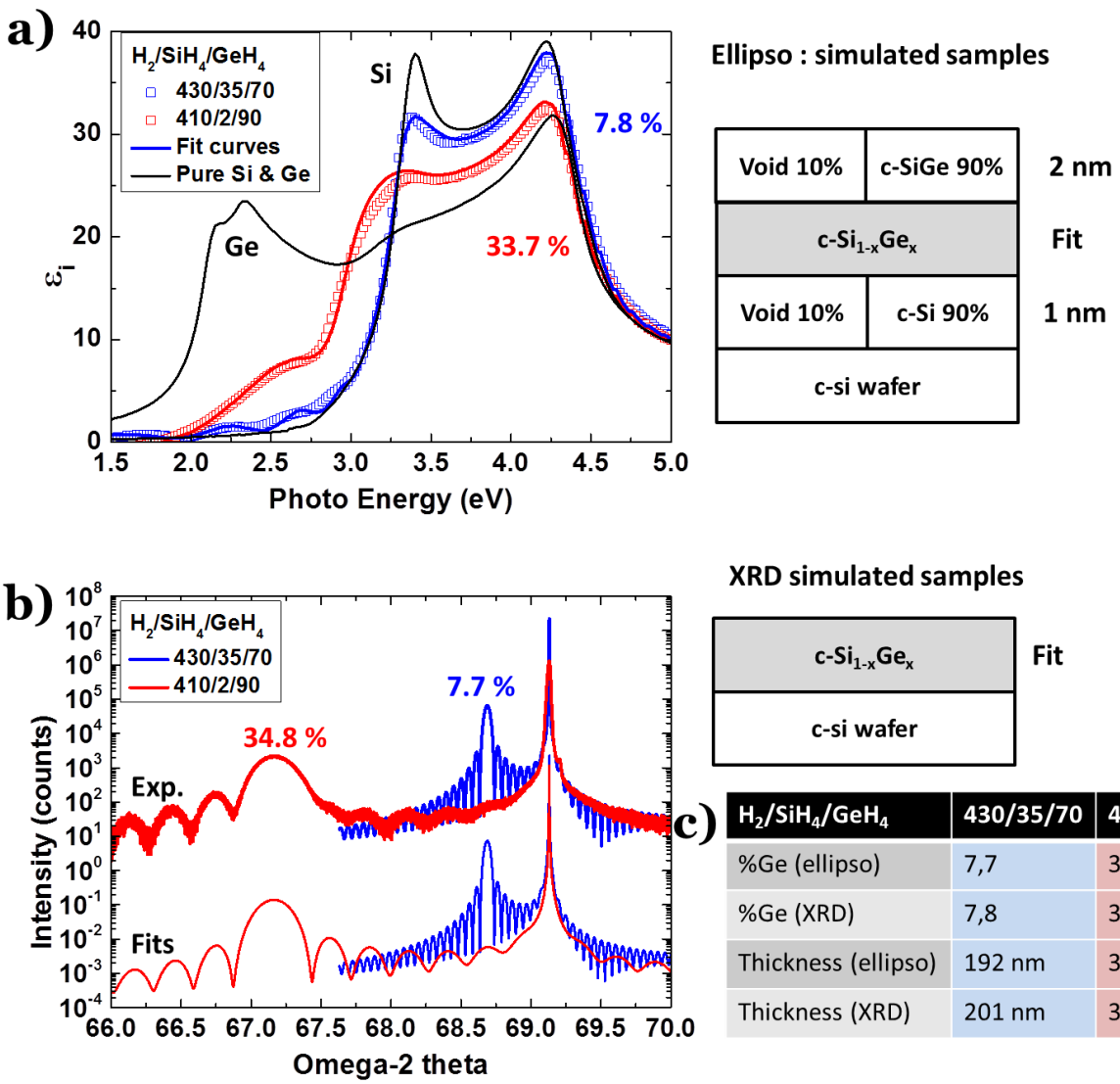
To reduce the required thickness of the bottom cell, it has been shown in the introduction chapter that we can alloy Si with Ge. Indeed, the absorption coefficient of SiGe increases with the addition of Ge[93]. Thus, to obtain the same tandem efficiency, a much thinner SiGe would be required. We propose in this part to study the growth of $Si_{1-x}Ge_x$ alloys by LT-PECVD on top of Si wafer. $Si_{1-x}Ge_x$ has a tunable bandgap whose value can change from 1.12 eV (Si) to 0.67 eV (Ge), depending on Ge content and strain[94]. A complete presentation of SiGe growth can be found in the book from John D. Cressler[95]. As already introduced in the first chapter, such SiGe material is already used in photovoltaics as a graded buffer layer to grow III-V on silicon. Ge and GaAs have the same lattice parameter, thus using SiGe graded buffers helps reducing dislocation density when growing GaAs on Si substrate. Moreover, SiGe, with its tunable bandgap, is also a good candidate as a bottom cell for SiGe/III-V tandem solar cells. For example, tandem solar cells of lattice-matched GaInP on $Si_{1-x}Ge_x$ have recently reached 18.9 % of efficiency, with x=82%, corresponding to a bandgap of 0.86 eV that is current matched with their top cell[96,97]. Low temperature PECVD of Ge has already been demonstrated in the lab on top of GaAs[98] substrate, and as Si/Ge multi layers on GaAs [99]. Also, c-Ge growth on Si has been demonstrated [100] on top of Ge substrate and Si substrate. Furthermore, some first results have been demonstrated on the Arcam reactor[54], studying the growth of $Si_{1-x}Ge_x$ on Si substrate with various Ge content up to x=35 %. We propose here to investigate in the new reactor Octopus the growth of $Si_{1-x}Ge_x$ with various Ge content, and various thicknesses.

We aim at growing thick SiGe layers up to 5 µm, and we aim at reaching Ge contents as high as possible. The modelling work presented in Chapter 1 was focused on $Si_{0.73}Ge_{0.27}$[52]. In the new Octopus reactor, we propose to develop the process conditions to grow crystalline $Si_{1-x}Ge_x$ for various x values, and to reach high thicknesses. The corresponding heterojunction solar cells will be presented in section II.3. But before depositing thick layers, we first developed the recipe for small thicknesses to be sure to have epitaxial growth, and to calibrate the amount of Ge incorporated in the layer for a certain conditions. The depositions were made in Octopus reactor at 175 °C on (100) Si wafers after an HF cleaning. The pressure was fixed at 2 mbar and a RF power at 50 W. The precursors used were $SiH_4$, $H_2$, and $GeH_4$ diluted at 1% into $H_2$.The $GeH_4/(SiH_4+GeH_4)$ ratio has been varied in order to incorporate different amounts of Ge. Most of the calibration samples have been done with a short deposition time of 16 minutes.

To determine the percentage of germanium incorporated into the epi-$Si_{1-x}Ge_x$, the lab has commonly used ellipsometry up to now. We propose to compare it to XRD measurements. We show here the calibration of a few samples in order to compare the obtained values. As the $GeH_4$ is diluted at 1% in $H_2$, we always keep the sum $H_2$+$GeH_4$ constant, in order to keep roughly the same amount of $H_2$ in the plasma. The ellipsometric spectra of the two samples grown with different gas flow rates are displayed in Figure 2.15.a, along with the references of c-Si and c-Ge. We see a clear evolution of the pseudo-dielectric function. The more Ge there is the gas mixture, the more the $E_1$ peak (around 3.4 eV) shifts towards lower energies and its amplitude decreases. It corresponds to a higher incorporation of Ge in the crystal. By fitting the ellipsometric spectra with the simulated structure represented on the right, the layer thickness and stoichiometry are deduced. The XRD measurements on the same two samples are shown in Figure 2.15.b. When the ratio $GeH_4/(GeH_4+SiH_4)$ increases, the diffraction peak shifts to the left, toward lower angles. $Si_{1-x}Ge_x$ lattice parameter follows the following equation[101]:

$$a_{SiGe}(x) = (1-x)a_{Si} + xa_{Ge} \qquad \text{Eq 2.3}$$

It means that he more Ge is incorporated, the higher its lattice parameter, and thus the lower its diffraction angles, which is consistent with the observations. The thicknesses and Ge contents deduced by both XRD and ellipsometer fits are gathered in Figure 2.15.c. If we compare both fits, the results for thickness and Ge content are very similar from one technique to another. Thus, in the rest of this part, we will characterize the germanium content in our $Si_{1-x}Ge_x$ grown layers only by means of XRD. Reciprocal space mapping (RSM) along {224} planes will also give us information on the strain or relaxation of the layers.




| $H_2/SiH_4/GeH_4$ | 430/35/70 | 410/2/90 |
|---|---|---|
| %Ge (ellipso) | 7,7 | 34,8 |
| %Ge (XRD) | 7,8 | 33,7 |
| Thickness (ellipso) | 192 nm | 35,4 nm |
| Thickness (XRD) | 201 nm | 37 nm |

**Figure 2.15 - a) and b): ω-2θ XRD scans and ellipsometric spectra of three $Si_{1-x}Ge_x$ samples with various GeH4/(SiH4=GeH4) grown in Octopus reactor. c) Comparison of Ge content deduced from ellipsometry and XRD fits for several $H_2/SiH_4/GeH_4$ conditions.**

It is worth noticing the big change in thickness from one sample to the other. For all the depositions that have been done with various gas flow rates, we plotted the deposition rate as a function of the Ge content in Figure 2.16. The growth rate of $Si_{1-x}Ge_x$ strongly decreases with the increase in Ge content. A few samples grown in Arcam reactor are also plotted in this graph, and show the same

trend. We also tried to deposit $Si_{1-x}Ge_x$ with x=70 %. The deposition was actually amorphous, but it revealed a really low deposition rate, below 0.1 A/s. Actually, this behavior does not follow the usual observation found in literature. For example, for SiGe grown by UHVCVD it has been reported that the growth rate increases with Ge content. By low pressure CVD it has also been observed that the more Ge is incorporated, the higher the growth rate [102], especially at low temperatures. Same trend was observed with atmospheric CVD experiments[103]. In our case, we suspect that this diminution in growth rate is due to the fact that we are limited by the mass flows. As already mentioned, the $GeH_4$ is diluted at 1% in $H_2$ and the flow rate is limited to 100 sccm. Thus, to incorporate enough Ge, we have to drastically decrease the $SiH_4$ flow rate in order to increase the $GeH_4/(SiH_4+GeH_4)$ ratio. Consequently, there are fewer precursors in the chamber that are available for the deposition, which strongly decreases the deposition rate. In order to keep a constant deposition rate, it would require a $GeH_4$ bottle that is less diluted into $H_2$.

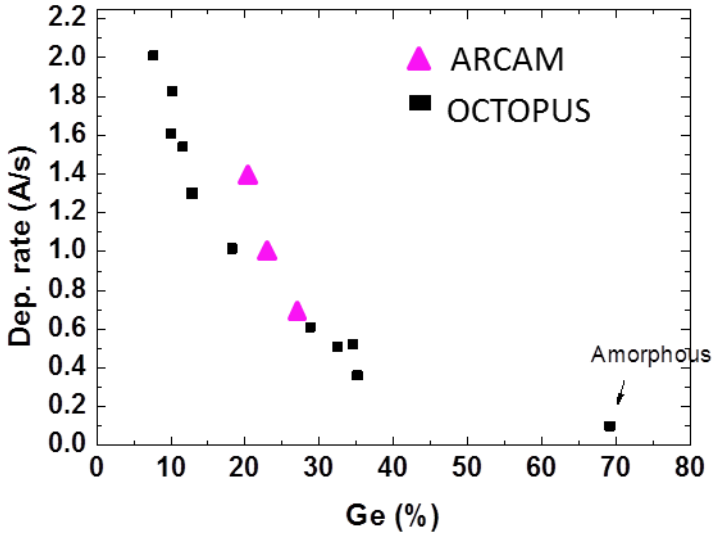



**Figure 2.16 - Deposition rate as a function of Ge content for various calibration samples in Octopus reactor (squares) and Arcam reactor (triangle): Deposition rate strongly decreases with %Ge. Too high %Ge leads to amorphous growth.**

## II.2.5. Thick $Si_{1-x}Ge_x$

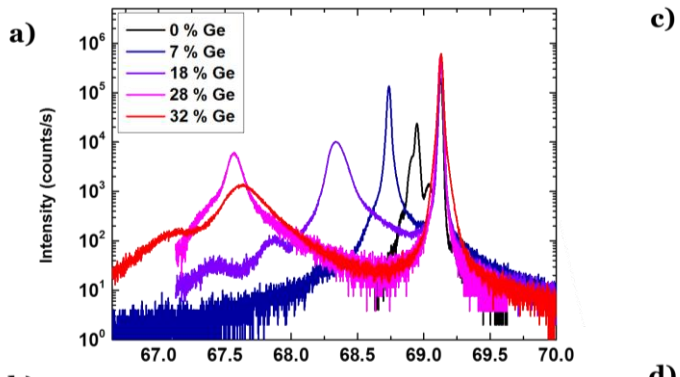
We propose now to grow thick layers of SiGe with increasing Ge content. We aim at achieving the highest %Ge with the highest thickness, in order to integrate it in a tandem solar cell configuration. Taking into account the growth rate determined for small thicknesses, we targeted to grow 1 µm thick $Si_{1-x}Ge_x$ layer with x = 7, 18, 28 and 32 %. The growths were performed with the following fixed parameters: the chamber temperature is set at 175 °C, the pressure is of 2 mbar, and we used a RF power of 50 W.

The resulting XRD measurements of each sample are shown in Figure 2.17.a. The targeted %Ge shown in Figure 2.17.b were deduced the thin calibration layers deposited with the same process parameters. We notice that the Ge content extracted from the XRD measurements slightly varies from its nominal value for the sample with 28% of Ge which is now of 25.8%. We also notice on the diffractograms for x≥ 13.5 % show some secondary peaks on the left (double peak for 13.5 % and a shouldering for 25.8 %) corresponding to thin layers with higher contents. For the 13.8% layer, two

low peaks are visible around 67.9° and 67.4 °, corresponding to $Si_{1-x}Ge_x$ layers with x≈26 % and x≈34 %. The low intensity and the high FWHM of these layers reveal their low thickness, or some relaxation. To have a better insight in the relaxation of these layers, {224} RSM of the sample with 13.8 %Ge is displayed in Figure 2.17.c. The double peak close to the substrate corresponds to some optical artifacts and must not be taken into account. In this mapping, we see that all the peaks are vertically aligned with the substrate peak, showing that the layers are not relaxed. The three different peaks are visible (indicated by white arrows). Thus, those 3 peaks correspond to three actual SiGe layers with various Ge content. Thus, during the growth, the incorporation of Ge in the film is not perfectly constant. It would be of interest to understand better why this incorporation is not constant, and when the change is occurring. Is it a graded layer? Is there more and more Ge incorporated during the growth? It could be due to the conditioning of the reactor walls that contain more Ge that also participates to the incorporation by memory effect?

Looking now at the 32% Ge layer, (red curve), the diffraction angle is higher than that of the 25.8 % (pink curve), whereas it should be lower in a strained configuration, because the lattice parameter follows Eq.2. We notice that the FWHM of the 32% peak is way higher than that of other samples (0.27 °). Performing an RSM mapping along {224} planes (Figure 2.17.d.) actually revealed that the grown layer is partially relaxed. The relaxation rate deduced from the {224} RSM is of 0.45. Thus, it is natural that the ω-2θ scan shows a peak shifted to the right. By taking into account this relaxation value into the Leptos simulation, the calculated Ge content is found to be 32.5 %, which is very close to the expected content of 32 %.

In the table of Figure 2.17.b, we also give information on the thicknesses that were deduced from cross-section SEM images, along with the new calculated deposition rate. The thickness targeted was 1 µm. We notice that the measured thickness is actually different from the expected one. For x ≤ 13.8%, the deposition rate is higher than expected, and for x ≥ 25.8%, the deposition rate was over-




b)

| Sample name | Targeted %Ge | Diffraction angle (°) | Relax. | %Ge (%) | FWHM (°) | Thickness (nm) | Dep. Rate (A/s) |
|---|---|---|---|---|---|---|---|
| O-170227-1 | 0 | 68,7933 | 0 | 0 | 0,0275 | 1400 | 2.00 |
| O-170209-2 | 7 | 68,7370 | 0 | 7 | 0,0240 | 1110 | 2.23 |
| O-170425-1 | 13,5 | 68,3381 | 0 | 13,8 | 0,1227 | 1230 | 1.24 |
| O-170216-1 | 28 | 67,657 | 0 | 25,8 | 0,1052 | 894 | 0.53 |
| O-170208-1 | 32 | 67,6339 | 0,45 | 32,5 | 0,2747 | 880 | 0.45 |

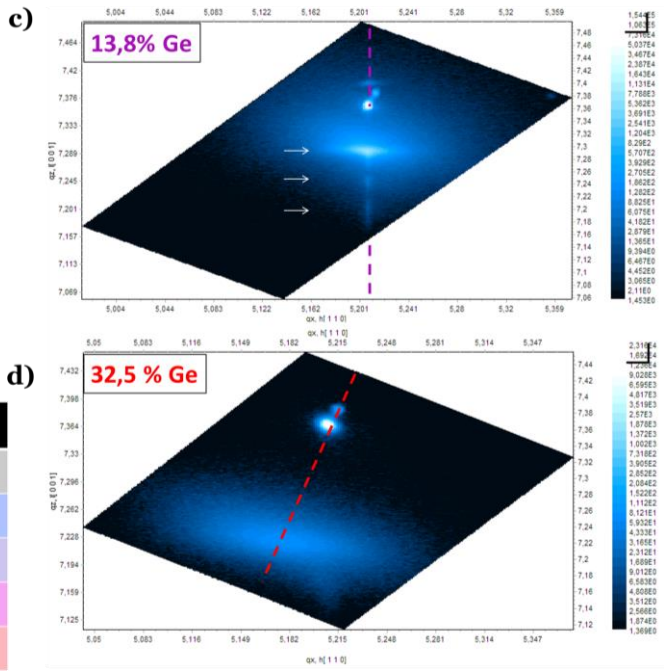



**Figure 2.17 - ω-2θ XRD scans of $Si_{1-x}Ge_x$ for various x values, aiming at a thickness of 1 µm b) fitted parameters deduced from XRD (diffraction angle, Ge content, FWHM) and SEM (thickness) d), RSM of the samples with x=13.8% and x=32.5% samples: the latest is partly relaxed.**

estimated. It raises several questions about the growth: is there any incubation time at the beginning of the growth? Is there an impact of the thermal stabilization? Is the presence of additional layers with higher content responsible for a non-uniformity of the deposition rate? Anyway, if we plot the deposition rate as a function of the %Ge for the thick layers, we see that the deposition rate for "1 μm" layers roughly follows the trend already observed with the thinner calibration samples. The difference in deposition rate over thickness rate may not be that significant, as seen in Figure 2.16.b.

To conclude this section, we studied the effect of adding $GeH_4$ into the $SiH_4/H_2$ plasma, and made the following observations. First, the deposition rate strongly decreases with the Ge content, due to a decrease of $SiH_4$ flow rate. While pure Si is grown at a deposition rate of 1.8 Å/s, that of a $Si_{0.72}Ge_{0.28}$ layer is only 0.6 Å/s. The deposition rate (which is calculated as the ratio of the film thickness over deposition time) is not constant during growth, as judged by the thickness obtained after long growth. The lack of in-situ characterization prevents us to have a better insight of the reasons of this change. We also find that thick $Si_{1-x}Ge_x$ layers contain some additional layers with other lattice parameters, thus Ge content. We also observed that for 32.7% of Ge, the epitaxial layer is partially relaxed.

We propose to focus on one sample, with the growth conditions leading to 25.8% of Ge, and to vary its thickness and growth temperature so as to have a better insight on the effect of these parameters on the layer quality and its strain.

### II.2.6. Strain relaxation in $Si_{0.75}Ge_{0.25}$

In SiGe epitaxial growth, SiGe layers of a certain composition are fully strained to Si substrate only under a certain critical thickness (pseudomorphic growth). Indeed, the SiGe layer, whose lattice parameter is mismatched with that of the Si substrate, is elasticly strained. However, it takes energy to accommodate this strain, depending on the lattice mismatch (thus the Ge amount) and on the thickness. It also requires energy to create a dislocation that will relieve the lattice mismatch strain. Thus, if the layer thickness is kept small enough to maintain the elastic strain energy below the energy of dislocation formation, the strained layer will be thermodynamically stable against dislocation formation. Above a certain thickness, the energy necessary to accommodate the strain becomes higher than that of dislocation formation. The strained layer will thus relieve the strain and become relaxed. Once the epitaxial layer reaches this critical thickness, the strain is relaxed, creating threading dislocations in the SiGe layer, and mostly misfit dislocations at the interface. This critical thickness is also dependent on the growth temperature. Figure 2.19.b. adapted from Hull *et al.*[104], shows the reported critical thicknesses as a function of Ge fraction for three growth temperatures: 550 °C, 750 °C and 900 °C. The more Ge is incorporated, the smaller is the critical thickness. At 550 °C, the critical thickness is one order of magnitude higher than that of a SiGe grown at 900 °C. At lower growth temperatures, the critical thickness is higher due to kinetic restriction of the relaxation.

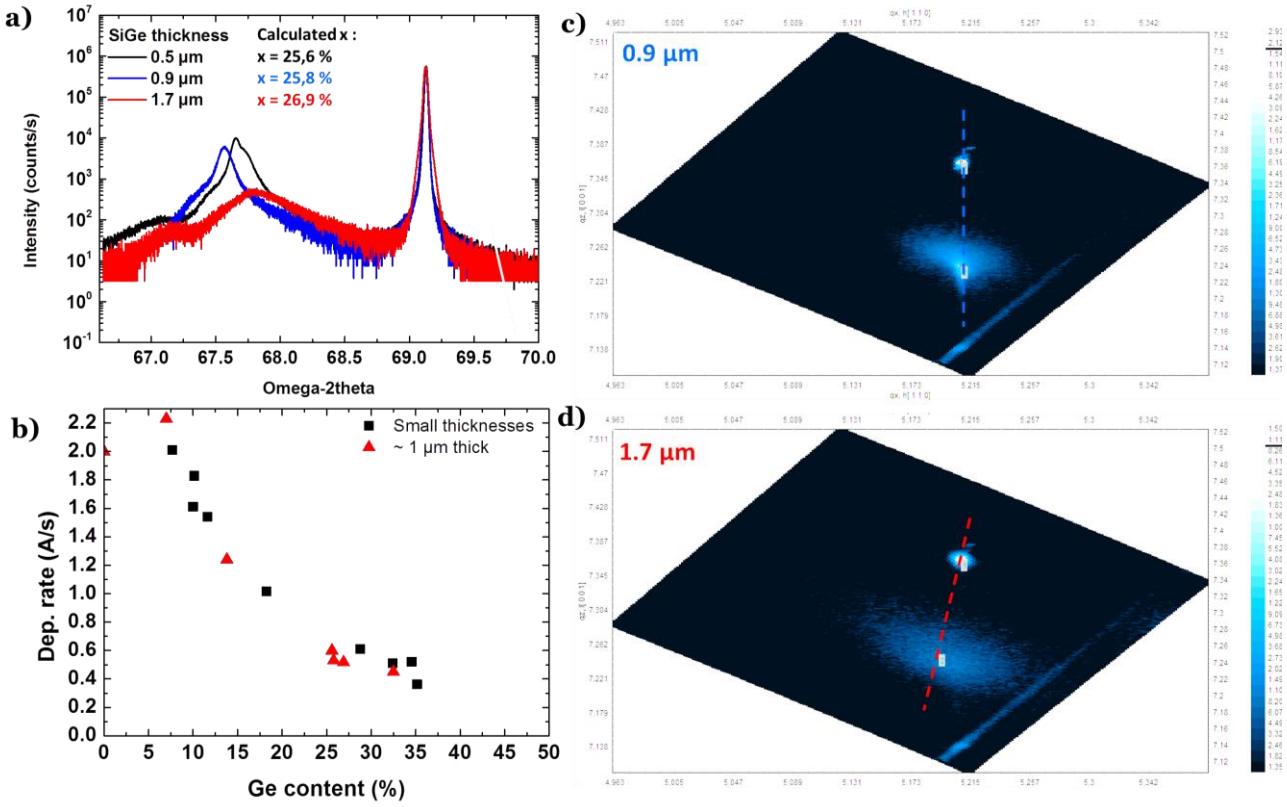



**Figure 2.18 - ω-2θ XRD scans of SiGe25.8 with increasing thicknesses: 0.5 µm, 0.9 µm and 1.7 µm, b) Deposition rate as a function of Ge content for the thin calibration layers (<200 nm) and the thick layers. c)d), RSM of 0.9 and 1.7 µm samples: the latest is partly relaxed.**

In case of our low-temperature PECVD layers, we already observed on SiGe with 32.5 % of Ge that a 880 nm layer is relaxed, thus above the critical thickness of the layer. We propose here to grow with the process conditions of $SiGe_{25.8}$ different thicknesses: 500 nm, 900 nm and 1.7 µm. The different samples were grown with the same PECVD parameters (P= 50W, p=2 mbar, $H_2/SiH_4/GeH_4$ = 400/100/5), only the deposition time has been varied. The thicknesses have been measured on SEM images. The XRD analyses of the three samples are gathered in Figure 2.18.a. For 500 nm and 900 nm, both peaks have similar shapes, however, it is slightly shifted. Simulations give us a Ge content of 25.6 % for 500 nm. We consider that this shift is negligible. For the thinner layer (500 nm, black curve), we notice that there is a visible large peak on the left of the film peak (centered around 67 °) that could be the proof of the presence of a thin layer of SiGe with x ≈ 37 %. The 900 nm layer is fully strained as deduced from the vertical alignment of the two diffraction peaks of the {224} RSM shown on Figure 2.18.c. In contrast, the 1.7 µm layer shows a partially relaxed layer, with a relaxation rate of R=0.27. By implementing this value in the model to determine the Ge content in the layer, we calculate x = 26.9 %.

We also proposed to study the effect of the substrate temperature on the properties of $Si_{1-x}Ge_x$ layers. To do so, we kept the process conditions (P= 50W, p=2 mbar, $H_2/SiH_4/GeH_4$ = 400/100/5) and grew several layers at 150 °C, 175 °C and 200 °C. The XRD and {224} RSM are not displayed here but revealed an unexpected trend: the layer grown at 150 °C is relaxed with R=32 %, while the two others are strained. Their Ge content and thicknesses deduced from XRD are gathered in Table 2.1.

The Ge incorporation has actually changed with growth temperature. The higher the growth temperature, the lower the Ge incorporation, which is actually consistent with the results found in literature[105,106]. While theoretically, at higher temperatures the critical thickness is higher, as seen in Figure 2.19.a, here, only the material grown at lower temperature (150 °C) is relaxed. This may not be a direct effect of the temperature, but rather due to the fact that the Ge incorporation is different. The layer grown at 150 °C exhibits the highest Ge content (27.7 %).

**Table 2.1 - Relaxation, %Ge and thickness for $Si_{1-x}Ge_x$ materials grown at various temperatures for ($H_2/SiH_4/GeH_4$) = (400/5/100)**

| Growth Temperature | Relaxation | %Ge | Thickness (nm) |
|---|---|---|---|
| 150 °C | 0.32 | 27.7 | 890 |
| 175 °C | 0 | 25.8 | 895 |
| 200 °C | 0 | 23.7 | 805 |

We report on Figure 2.19.a. some data points corresponding to our samples grown by LT-PECVD at 175°C, as compared with the critical thickness of $Si_{1-x}Ge_x$ from literature. The open symbols show the layers that are fully strained, thus below the critical thickness. The full symbols correspond to the three samples that are partly relaxed. We see that the low temperature of our process enables to increase drastically the critical thickness of the $Si_{1-x}Ge_x$ layer as compared to more standard growth techniques occurring above 500 °C. We will propose in the next section to fabricate heterojunction solar cells and compare the performances and material quality of each of those $Si_{1-x}Ge_x$ layers.

As a conclusion on $Si_{1-x}Ge_x$ materials grown by low-temperature PECVD, we gathered most of the samples presented in this study in Figure 2.19.b. Each color means that they were grown with the same $H_2/SiH_4/GeH_4$ flow rates. Dashed lines are displayed as guide to the eyes. We see that the Ge content is rather stable for fixed parameters, even if the XRD measurements have shown the presence of some additional layers with higher Ge content. Some SiGe layers are partly relaxed: for a Ge content above 27.7%, the layers are already relaxed for a 1 µm thick layer, and a layer with 26.9 % of Ge is relaxed for 1.7 µm while it is not for 900 nm. We observed the impact of the growth temperature on the Ge incorporation. At 200 °C, the Ge content is much lower than at lower temperatures (150 °C). We also showed that the deposition rate is not really constant over growth time, even if it is negligible as compared to the change in growth rate caused by the increase in Ge content. It has been attributed to the diminution of $SiH_4$ flow rate, which strongly reduces the available Si atoms in the plasma to be incorporated into the grown layer. While 7% of Ge grows at 2.2 Å /s, SiGe samples with 32 % Ge have a deposition rate below 0.5 Å/s. The high dilution of $GeH_4$ in $H_2$ (1%) gave us less room for Ge content adaptation, as it is diluted at 1% in $H_2$. It would require a lower diminution of $SiH_4$ flow rate for the same Ge incorporation thus leading to a less low deposition rate.. Also, a much more precise control of the Ge content, as well as the incorporate of more than 35 % in the layer would be possible.

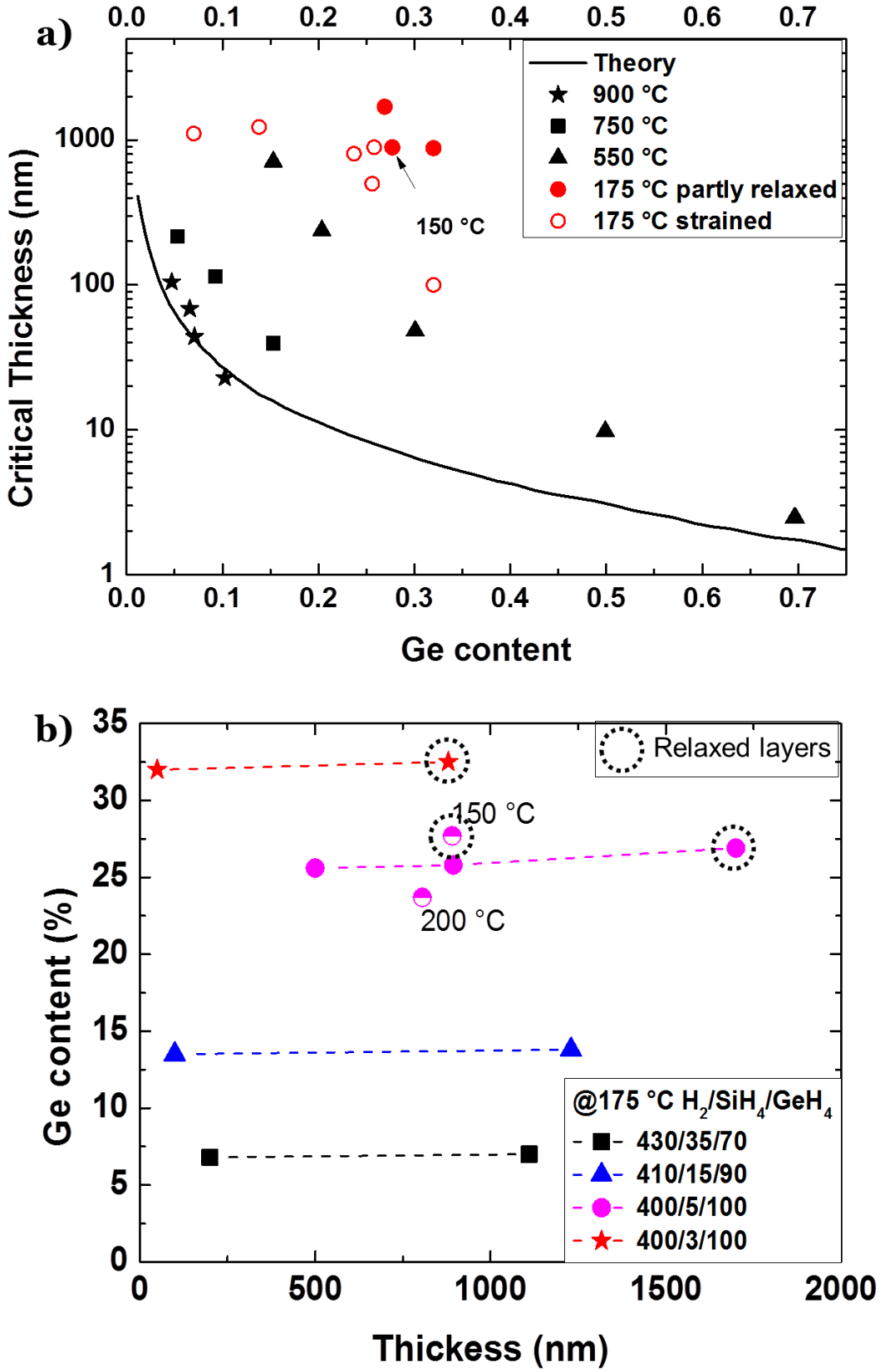



**Figure 2.19 - a) Critical thickness of SiGe reported from Hull *et al.* [107] as a function of the growth temperature, compared to our samples. Low-temperature PECVD has a higher critical thickness than other techniques b) Ge content as a function of thickness for various growth conditions.**

In section II.2, we presented the growth of Si on Si substrates and the influence of annealing at various temperatures on its structural properties. We also assessed the growth of Si with thicknesses up to 6.5 µm, and proposed pathways to growth thicker layers while keeping good structural properties. We also presented the growth of $Si_{1-x}Ge_x$ alloys, pointing out the influence of the Ge content on the deposition rate, analyzed the strains in the grown layers and studied the influence of growth temperature on the strain and composition. From all these layers grown, we propose now to assess their electrical properties by integrating them into heterojunction solar cells. In the following section, solar cells will be fabricated from the Si and SiGe epitaxial layers, and their electrical performances will be characterized.

# II.3. Solar cell fabrication

This section focuses on the heterojunction solar cells fabricated with the epitaxial layers presented previously. We will first introduce the fabrication process and the characterization techniques used to measure their efficiency. Then, the Si and $Si_{1-x}Ge_x$ heterojunction solar cells will be characterized and the results will be discussed.

## II.3.1. Fabrication process and electrical characterization tools

### II.3.1.1. Process

After epitaxy, several process steps are required in order to have a full solar cell device that can be measured. We present here the details of the structure of the heterojunction solar cells that will be fabricated. Note that the process flow for III-V solar cells is different, and requires more advanced clean room processing that will be the subject of Chapter 4.

The structure of a typical solar cell is pictured in Figure 2.20.a. On top of the epitaxial layer, a thin (5 nm) a-Si:H is deposited to form the heterojunction, followed by a n-type a-Si:H contact layer. On top of it, Indium Tin Oxide (ITO) is deposited through a physical shadow mask. It acts as an anti-reflective layer and ensures lateral conduction of the carriers. Then, a front contact is deposited through another shadow mask, with a central busbar and perpendicular metallic fingers.

To deposit the metallic contacts, two main techniques are available: evaporation and sputtering. Evaporation deposition is directional; however, it does not ensure a very good adhesion of the metal on the wafer. The second deposition technique is the sputtering. Under vacuum, an Ar plasma is created and directed towards a target. This target can be the metal (Al, Ag), or an alloy (ITO). This technique leads to a metal that has a better adhesion, however, the deposition is less directional. For the realization of the front grid, sputtering is not adapted, because we use a physical shadow mask that is not perfectly in contact with to the wafer. When using sputtering, the metal would be deposited below the borders of this mask, and will thus have wider patterns than expected, introducing more shadowing. Thus, for the front contact, evaporation will be preferred. The same process flow has been applied to all the materials studied earlier : 1.5 µm of epi-Si annealed at

different temperatures, thick epi-Si up to 10 µm, and Si(Ge). This work received great help from master's student Clément Lausecker.

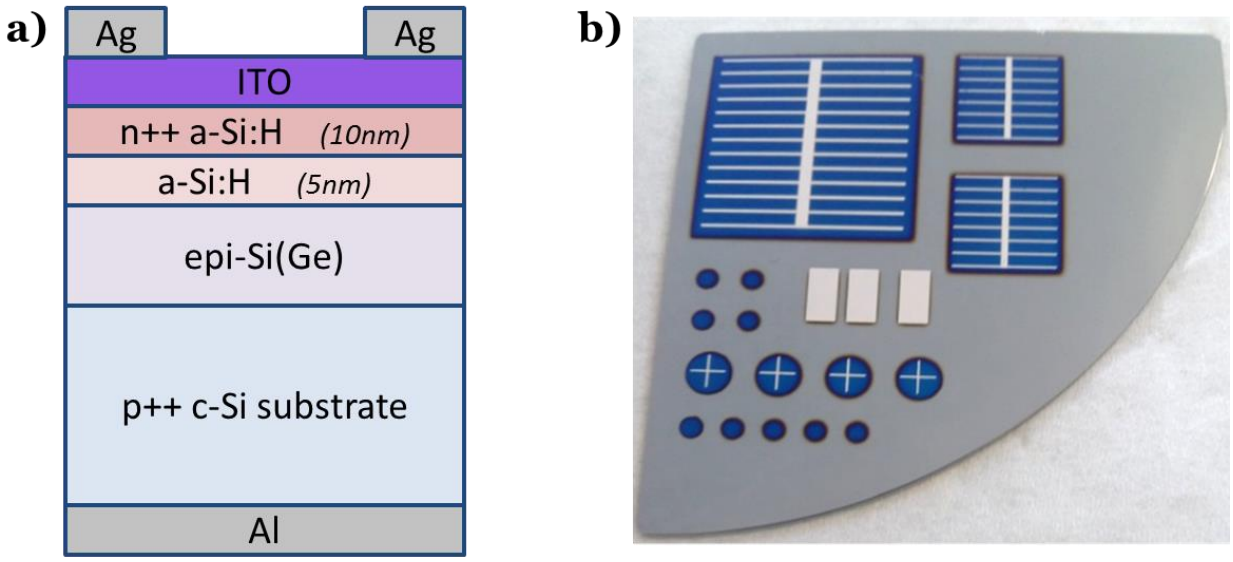



**Figure 2.20 - a) Structure of the heterojunction solar cell grown and processed, b) top-view picture of the device after ITO deposition and metallization : one 2x2 cm$^2$ and two 1x1 cm$^2$ cells can be distinguished.**

### II.3.1.2. Electrical characterizations

Two main characterization techniques are used to assess the electrical properties of our solar cells: the J-V characteristics under solar simulator give us the efficiency of the solar cell, and External Quantum Efficiency (EQE) helps us to have a better insight on the carrier collection depending on the wavelength. The principle of those two characterization techniques is presented here, along with the information we can deduct from them.

When a photon reaches the semi-conductor (SC), it is absorbed if its energy is above its bandgap, and an electron-hole pair is created into the SC. The photogenerated carriers will recombine after a certain time (carrier lifetime). In order to collect these photogenerated carriers, the use of a p-n junction is required to spatially separate electrons and holes and prevent them from recombining. In a p-n junction, electrons that are in high concentration in the n-type part diffuse towards the p-type side, while hole flow from p-side to n-side. By diffusing, they leave behind some fixed charges on dopant atom sites. Close to the junction, positive ions are left in the n side and negative ions in the p side. This fixed-charged region is called the space-charge region, in which an electric field is formed. This electric field will be the one separating the photogenerated carriers, leading electrons to the n-side and holes to the p-side. If both sides are connected by a metal, the light-generated carriers will flow through an external circuit, thus delivering a current.

In the dark, the current density *J* generated by a solar cell is described by the following equation :

$$J = J_0\left[\exp\left(q\frac{V - JR_S}{nkT}\right) - 1\right] \qquad \text{Eq 2.4}$$

Where $V$ is the applied voltage, $k$ the Boltzmann constant, $T$ the temperature, $J_o$ the saturation current density and $n$ the ideality factor of the diode. Measuring a solar cell in the dark already gives important information, because $J_0$ is linked with the carriers recombination in the device. A low $J_0$ indicates a high quality p-n junction. Under illumination, a current density $J_{ph}$ is photogenerated by the solar cell, flowing in the opposite direction. Also, some resistance must be considered in the equation to take into account the series resistance ($R_s$) that can be induced by the metal-semi-conductor contact at the top or at the rear, and the shunt resistance that can arise from leakages of current through the cell. The electrical model of a solar cell under illumination is described in the following equation:

$$J = J_0\left[\exp\left(q\frac{V - JR_S}{nkT}\right) - 1\right] + \frac{V - JR_S}{R_{Sh}} - J_{ph} \qquad \text{Eq 2.5}$$

J-V characteristics consist of measuring the current response of a solar cell to an applied voltage and give much information on the device quality. The measurement can be performed under illumination or in the dark. In the dark, we can determine $J_0$ and the ideality factor n. Under illumination, the solar cell parameters ($V_{OC}$, $J_{SC}$ and FF) can be determined. The set up used to have J-V characteristics is a solar simulator. During this PhD we used an Oriel Sol3A solar simulator, that reproduces AM1.5G spectrum and illuminates the solar cell with a calibrated power of 100 mW/cm², with a spectral distribution that matches the solar spectrum. Before each solar cell characterization, the spectrum is calibrated using a Si calibration solar cell furnished by the constructor. The measurements are performed at fixed temperature of 25 °C. Note that the same solar simulator was used to characterize the III-V solar cells.

The shape of a typical J-V curve of a solar cell under illumination is shown in Figure 2.21.a. Four important parameters have to be considered: 1) the $J_{SC}$, or short-circuit current, which corresponds to the current measured with no applied voltage, 2) the open-circuit voltage $V_{OC}$, measured when no

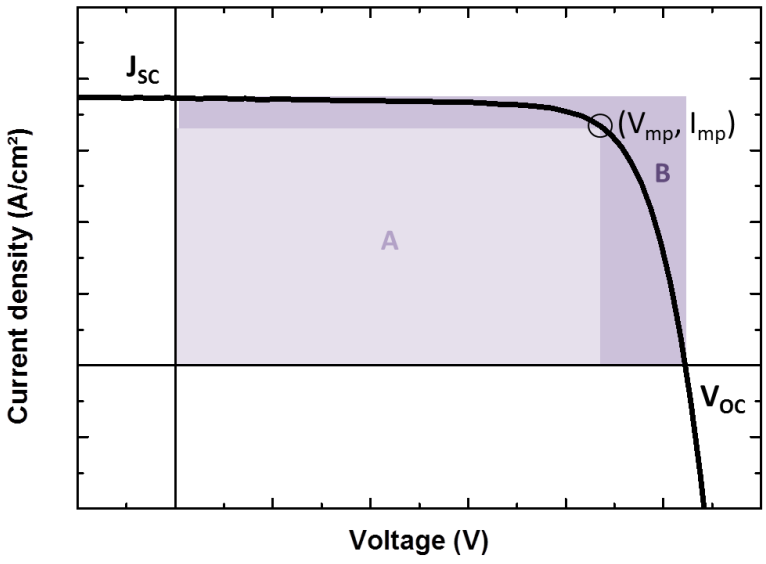



**Figure 2.21 - J-V characteristics of a solar cell under illumination.**

current flows, 3) the maximum power point (MPP) where the product current times voltage reaches its maximum. From the values of $V_{mpp}$ and $J_{mpp}$, we define the fill factor (FF) by Eq 2.6:

$$FF = \frac{J_{mp}V_{mp}}{J_{SC}V_{OC}} \qquad \text{Eq 2.6}$$

This parameter is the ratio between the areas of two rectangles: the one formed by the origin axis and the maximum power point (rectangle "A"), and the ideal rectangle formed by the origin and the point with coordinated ($V_{OC}$, $J_{SC}$) (rectangle "B"). The typical FF values for good Si solar cells are between 80 and 85 %. For GaAs solar cells FF can reach up to 89 %.

Fill factor can be lowered mainly by the series resistances and the shunt resistances. $R_S$ is due to all the resistive losses in the solar cell (such as contact resistance, resistivity of the layers) and should be kept as low as possible. Shunt resistance ($R_{Sh}$) is the shunt losses, often due to due to manufacturing defects. It causes power losses in solar cells by providing an alternate current path for the light-generated current, consequently reducing the amount of current flowing through the solar cell junction. It also reduces the voltage from the solar cell. $R_{Sh}$ must be maximized. The series resistance affects the slope at $V_{OC}$ and the shunt resistance affects the slope around $J_{SC}$.

Finally, the efficiency ($\eta$) of a solar cell is defined by the ratio of photogenerated electrical power over the incident light power.

$$\eta = \frac{J_{SC}.V_{OC}.FF}{P_{incident}} \qquad \text{Eq 2.7}$$

External quantum efficiency measurements (EQE) can provide further information on the solar cell. It is the probability that a photon with an energy E that reaches the solar cell results in an electron collected by the external circuit. The value of the quantum efficiency is 1 at one particular wavelength when all the photons of this wavelength are absorbed and the delivered electrons are all collected. We must distinguish external quantum efficiency from internal quantum efficiency (IQE). IQE only takes into account the photons that reach the semi-conductor without being neither reflected nor transmitted, and thus can be absorbed by the solar cell. It is used to characterize the ability to collect charge carriers generated by different wavelengths of the sun spectrum. As the 'blue" light is absorbed at the rear side and the "red" light is more absorbed in the bulk, EQE provides a depth resolution of the recombination processes. In Figure 2.22 is represented a typical EQE of a solar cell, along with the main causes of EQE reduction. The cut at high wavelength gives the value of the bandgap of the absorbing material.

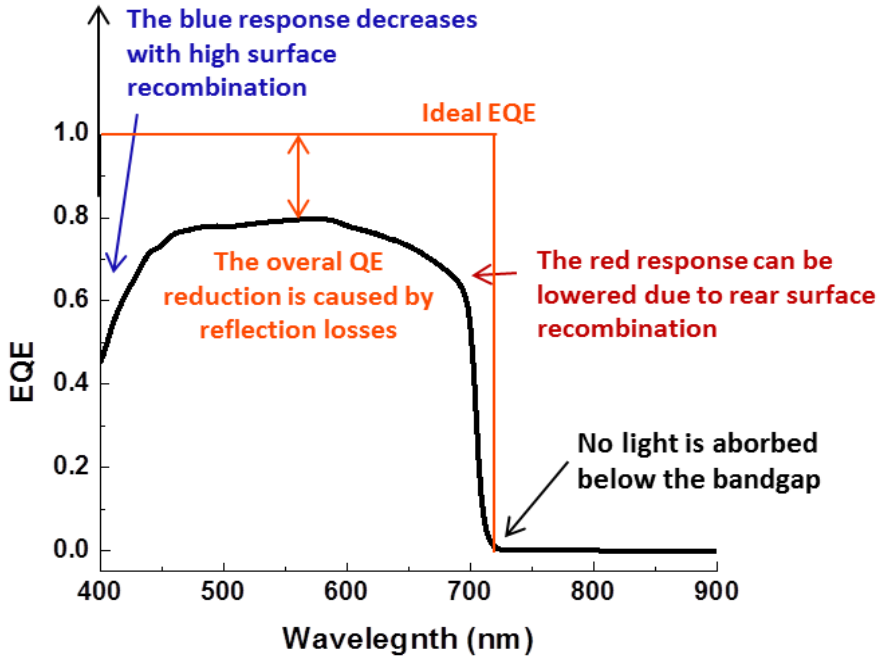



**Figure 2.22 - Measured quantum efficiency of a AlGaAs solar cell, along with the main contributions responsible for possible EQE reductions.**

## II.3.2. Si and SiGe heterojunction solar cells

### II.3.2.1. Effect of annealing on a 1.5 µm thick epi-Si layer

The solar cells were fabricated with the process steps presented in II.3.1.1.: The epi-layers previously presented were dipped into HF to remove the native oxide, and the solar cell presented in Figure 2.20 was fabricated.

Actually, in these solar cells, we needed to add a layer of micro-oxide on top of the (n+)-a-Si:H layer. Indeed, after the first J-V measurements performed on these solar cells, the measured J-V curves had systematically a "S-shape", as illustrated in Figure 2.27 (black curve). After several attempts on finding the origin of such a shape, we realized it was due to the front ohmic contact that was not good enough. The $PH_3$ gas cylinder, diluted at 0.1% into $H_2$, is not sufficient to dope enough the a-Si:H layer and perform a good ohmic contact with the ITO. As microcrystalline conductivity is higher than that of a-Si:H, we added this new layer in-between the a-Si layer and the ITO. This time, the red curve was obtained, that exhibits a typical shape of a solar cell J-V curve. The $V_{OC}$ is increased as compared with the previous "S-shape" curve, and also the FF, that reached 76.4%. The $J_{SC}$ has slightly decreased from 15.7 to 15.4 A/cm². This may be due to an additional absorption of the 20 nm thick µc-$SiO_x$:H that has been added. Once this issue of ohmic contact was solved, we added this µ-$SiO_2$ layer on top of each solar cell.

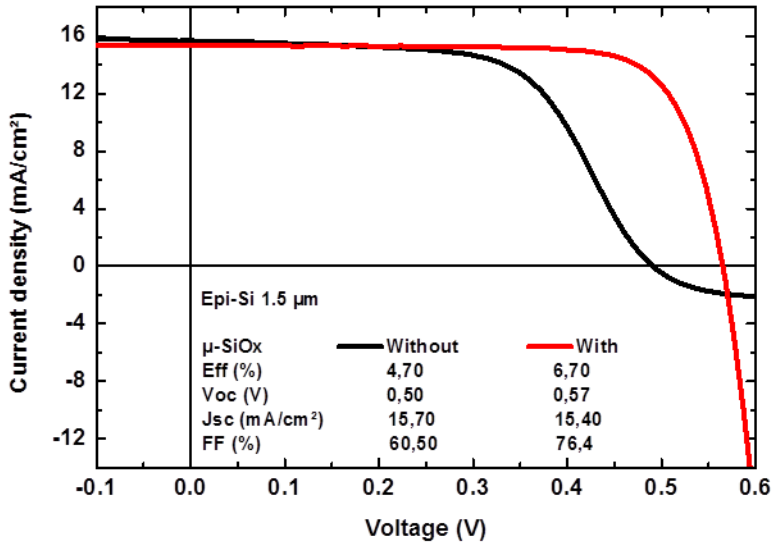
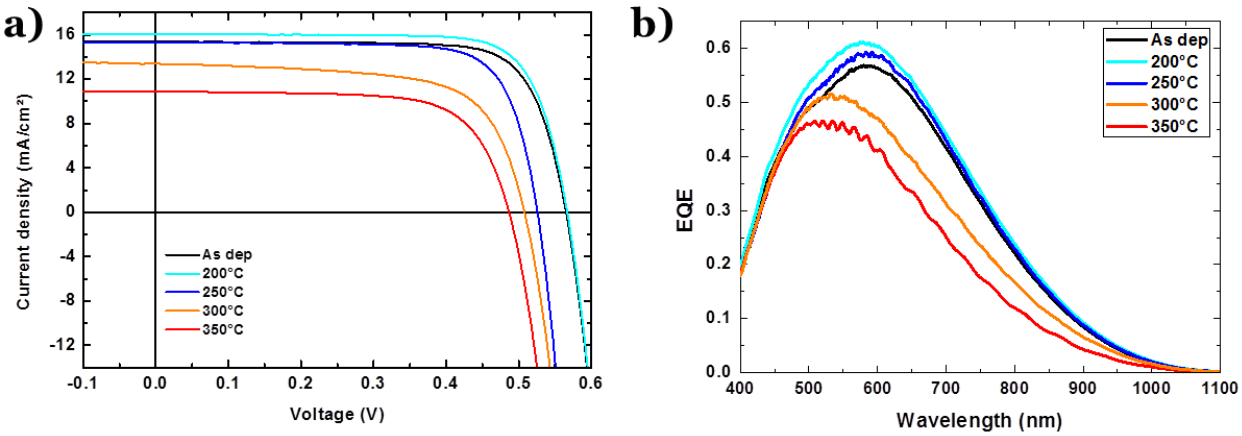



**Figure 2.23 - J-V characteristics of as-deposited 1.5 µm thick epi-Si without the addition of µ-SiO$_x$ (black curve), and with (red curve)**

We now study and compare the heterojunction solar cells that had been annealed at different temperatures prior to the deposition of a-Si:H. *J-V* measurements and external quantum efficiency measurements (EQE) are presented in Figure 2.27.a.b.c, along with the values of $V_{oc}$, FF, efficiency and the $J_{SC}$ measured by I-V and by EQE.

The following general observations can be made on the EQE measurements: 1) the high wavelength region is rather low for each sample because of the solar cell design. First, the low thickness of the absorber is responsible for this reduction, and second, the collection of the carriers at the rear is made at the back of a thick wafer. Thus, the photogenerated carriers need to travel through the whole 550 µm thick substrate, in which recombination may occur. 2) the rather low value of EQE at 400 nm is explained by a high absorption of our ITO at this wavelength. Simulations of the EQE of similar heterojunction structures can be found in Cariou *et al.*[107], showing that these two observations are inherent to our structure design, and not to the epitaxial absorber quality.

Interestingly, the *J-V* curves show a better efficiency for the 200 °C annealed sample than the as-deposited one, due to an increase in $J_{SC}$. EQE also confirms the increase in $J_{SC}$ from the as-deposited sample to the annealed at 200 °C one. They exhibit similar $V_{oc}$ and FF, only the $J_{sc}$ is enhanced. The increase in EQE occurs at low wavelength. The short wavelength EQE is particularly sensitive to surface passivation and emitter thickness. This may be due to a better epi-Si/a-Si:H interface, or a better passivation of the defects on the epi-layer by hydrogen. An annealing at 200 °C could have enabled hydrogen to move into the layer and to reach the defects so as to better passivate it.




c)

| Annealing T° | $V_{OC}$ (V) | $J_{SC,\ I\text{-}V}$ (mA/cm²) | $J_{SC,\ EQE}$ (mA/cm²) | FF (%) | Eff (%) |
|---|---|---|---|---|---|
| As dep | 0,57 | 15,4 | 12,6 | 76,4 | 6,7 |
| 200 °C | 0,57 | 16,0 | 13,6 | 76,9 | 7,0 |
| 250 °C | 0,53 | 15,3 | 13,0 | 76,0 | 6,1 |
| 300 °C | 0,50 | 13,4 | 10,7 | 68,4 | 4,5 |
| 350 °C | 0,48 | 10,9 | 9,2 | 71,7 | 3,7 |

**Figure 2.24 - a) J-V characteristics at low-temperature and b) external quantum efficiency of all the solar cells processed after various annealing temperatures, c) Solar cells characteristics calculated from I-V measurements and EQE**

The sample annealed at 250 °C has a slightly better EQE than the as-deposited one; however, it suffers from a strong $V_{oc}$ reduction that decreases from 0.57 V to 0.53 V, and a slight FF reduction. The similar EQE shows there is no significant degradation in the front surface or back surface. The lower $V_{OC}$ suggests a higher recombination rate in the epitaxial layer or at the epi-Si/Si substrate interface, which may come from the movement of hydrogen in the layer. While hydrogen were passivating the defects of the bulk in the as-dep and 200 °C layers, at 250 °C the hydrogen starts to migrate and exodiffuse, thus being less efficient in passivating bulk defects.

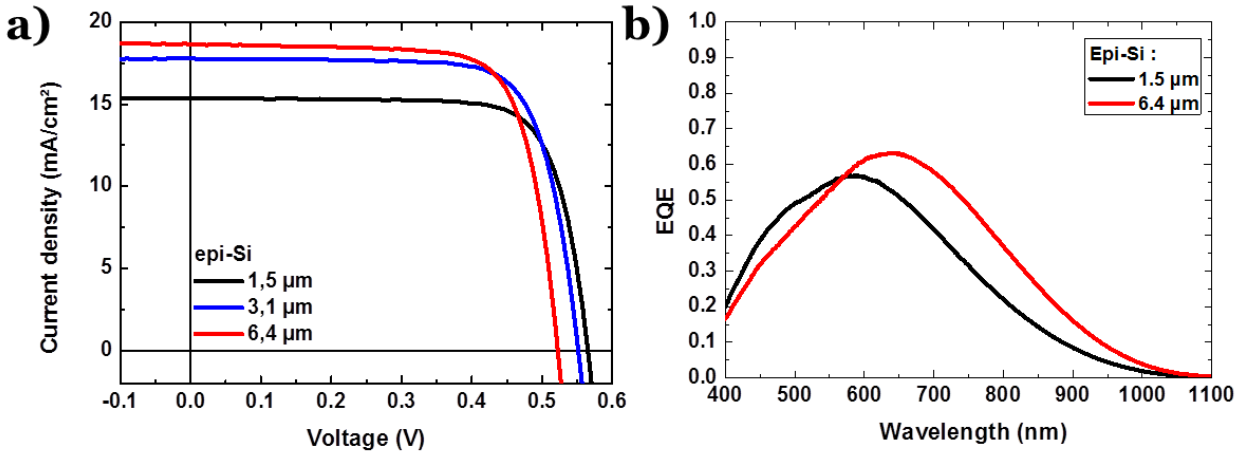
For even higher annealing temperatures, EQE is strongly reduced in the whole range above 500 nm. As the high wavelength is sensitive to the rear surface recombination, we attribute this to the defective interface between epi-Si and the c-Si substrate. This is consistent with the ellipsometric spectra presented in the previous section (Figure 2.4), which showed increasing oscillation amplitude upon temperature, thus a degradation in the interface quality for $T_{annealing} \geq 300$ °C. As expected, the 350 °C annealed solar cell has the worst electrical characteristic, with a low current, and a lower $V_{oc}$. The low EQE is mainly attributed to the very defective interface (containing $H_2$ blisters). Furthermore, the epi-Si relaxation has induced defects and mosaicity that induce dislocations in the epi-layer and thus lower the $V_{OC}$. Also, blisters provoke the detachment of the epi-layer from the substrate, leading to interface recombinations.

From these measurements, we can conclude on the importance of keeping the thermal budget as low as possible. Indeed, for a growth temperature of 200 °C, we reached an efficiency of 6.7 %, with $V_{OC}$

as high as 0.57 V, which proves the high potential of such an epitaxial layer for being used as an absorber. A post-growth annealing of the sample at 200°C seems to be beneficial for the solar cell operation that reaches 7.0 %. Annealing above 300 °C leads to the formation of $H_2$ blisters that are responsible for a strain in the epitaxial layer that relax from the substrate, and triggers high interface recombination. This strongly reduces the collections of the carriers. Furthermore, the hydrogen that was passivating the defects in the as-deposited state may have migrated or exodiffused, thus leading to more recombination centers in the film.

### II.3.4. Towards thicker absorbers

Solar cells have been fabricated with increasing epi-Si absorber layer thicknesses: 1.5 µm, 3.1 µm, and 6.4 µm, whose material characterizations have been presented in part II.2.3. The resulting ***J-V*** curves and characteristics are shown in Figure 2.25.a. and c., and their EQE of three of these samples are plot in Figure 2.25.b. The first observation we can make is that, the thicker the absorber is, the higher is its $J_{SC}$, which reaches 18.7 mA/cm² for the 6.4 µm thick layer. The FF stays rather constant. EQE show that the main gain in $J_{SC}$ is due to an increase in the red response, which is consistent with the fact that the epi-Si absorber is thicker. The slight decrease in EQE at short wavelength suggest a higher surface recombination, probably due to a slightly higher roughness of the epi-Si surface, leading to a less sharp interface between epi-Si and a-Si:H that forms the heterojunction. Thus, increasing epi-Si thickness helps to have a higher $J_{SC}$, however, higher surface or bulk recombination reduced the $V_{OC}$.




c)

| Thickness (µm) | $V_{OC}$ (V) | $J_{SC,\ I\text{-}V}$ (mA/cm²) | FF (%) | Eff (%) |
|---|---|---|---|---|
| 1,5 | 0,57 | 15,4 | 76,4 | 6,7 |
| 3,1 | 0,53 | 17,8 | 77,7 | 7,4 |
| 6,4 | 0,50 | 18,7 | 77,7 | 7,3 |

**Figure 2.25 - J-V characteristics at low-temperature and b) external quantum efficiency of all the solar cells with various epitaxial thicknesses, c) solar cells characteristics calculated from J-V measurements**

### II.3.5. c-SiGe heterojunction solar cells

We now study the impact of Ge content on the characteristics of a $Si_{1-x}Ge_x$ solar cells. Heterojunction $Si_{1-x}Ge_x$ solar cells have been already studied in literature using conventional epitaxial growths. A non-exhaustive list of $Si_{1-x}Ge_x$ heterojunctions is presented in Figure 2.27. The solar cell performances, as well as their Ge content and their thicknesses are specified. The record solar cell is held for a thick SiGe absorber of 15 µm, with 10% of Ge by Said *et al.*[108] It was grown by RP-CVD at 750 °C and revealed an efficiency of 10.3 % with a $V_{OC}$ of 559 mV, and a $J_{SC}$ of 24.2 A/cm². For thinner crystalline absorbers, Oshima *et al.*[109] reported a 1.8 % efficient $Si_{0.51}Ge_{0.49}$ solar cell of 3 µm grown by MBE. 2.9% was achieved by Li *et al.*[110] for a 2 µm heterojunction solar cell with 82 % of Ge, and 4.3 % was achieved by Hadi *et al.*[111,112] Microcrystalline results are taken from the following references : Matsui *et al.*[113], Cao *et al.*[114], and Huang *et al.*[115] Works in LPICM have already shown a 6.1 % efficiency $Si_{0.73}Ge_{0.27}$ heterojunction solar cell[54], grown by RF-PECVD at 175 °C, for a 1.9 µm thick absorber in the Arcam reactor. The $V_{OC}$ obtained was 413 mV, for a $J_{SC}$ of 18.8 mA/cm² and a high FF of 77.5 %.

For a fixed layer thickness, the main effects of additioning Ge into Si are expected to be: 1) an enhanced $J_{SC}$, due to a higher absorption coefficient of $Si_{1-x}Ge_x$ when x increases, and 2) a lower $V_{OC}$, due to the diminution of the bandgap with increasing Ge content. The results from Oshima *et al.*[109] reported in the table are consistent with this. However, their solar cells exhibit a strong reduction in FF that they attribute to an un-optimized processing temperature, adding point defects during the growth of their layers. PC1D simulations of SiGe heterojunctions with our device structure[92] are presented in Figure 2.26. For different Ge content, the $J_{SC}$ as a function of thickness is presented. It shows that for x> 10% there is a gain in $J_{SC}$ as compared with a pure Si heterojunction. The EQE shows that most of the gain in $J_{SC}$ is due to a better absorption in the high wavelength range. Thus, for our solar cells with increasing Ge content and a fixed thickness around 1 µm, we would expect an increase in $J_{SC}$ with %Ge, and a higher absorption at high wavelengths. The $V_{OC}$ should decrease, following the decrease in bandgap.

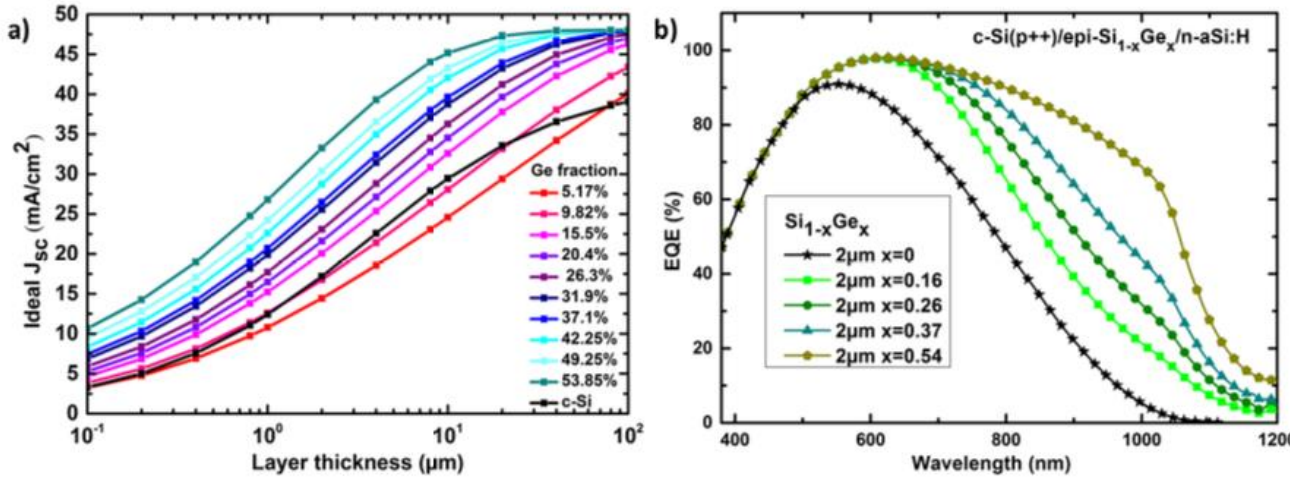
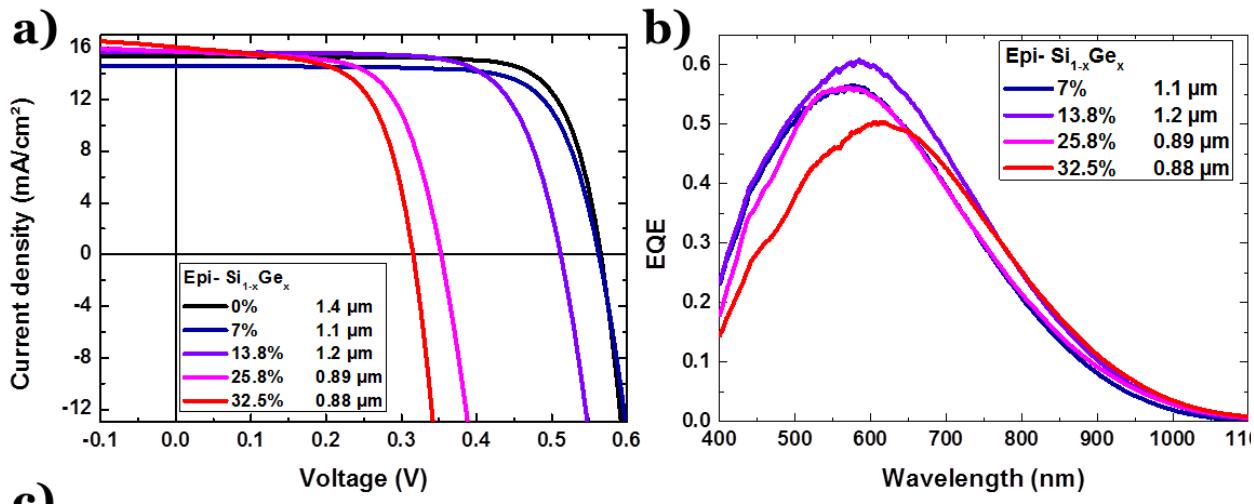



**Figure 2.26 - Ideal $J_{SC}$ as a function of SiGe thickness for various Ge content. b) PC1D model of EQE variation with Ge content for a (p++)c-Si/epi-SiGe/n-a-Si:H solar cell. From Cariou thesis p155.**

| Reference | Material | Technique | Deposit° Temp | %Ge (%) | Thickness (µm) | Voc (V) | Jsc (mA/cm$^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|---|---|---|---|
| Matsui 2009 | µ-Si | VHF-PECVD | 200 °C | 0 | 1 | 0,524 | 20,4 | 0,673 | 7,19 |
| Matsui 2009 | µ-SiGe | VHF-PECVD | 200 °C | 10 | 1,1 | 0,466 | 23,6 | 0,660 | 7,26 |
| Matsui 2009 | µSiGe | VHF-PECVD | 200 °C | 13 | 1,0 | 0,410 | 24,6 | 0,587 | 5,93 |
| Cao 2013 | µSiGe | RF-PECVD | 200 °C | 50 | 0,6 | 0,32 | 22,5 | 0,46 | 3,31 |
| Huang 2015 | µSiGe | RF-PECVD | 200 °C | 16,4 | 0,9 | 0,47 | 20 | 65 | 6,18 |
| Oshima 2015 | c-Si | MBE | 550 °C | 0 | 3 | 0,43 | 15,2 | 65,2 | 4,3 |
| Oshima 2015 | c-SiGe | MBE | 550 °C | 49 | 3 | 0,224 | 16,7 | 48,7 | 1,8 |
| Oshima 2015 | c-SiGe | MBE | 550 °C | 70 | 3 | 0,192 | 21,4 | 49,5 | 2,0 |
| Oshima 2015 | c-SiGe | MBE | 550 °C | 84 | 3 | 0,167 | 24 | 49,1 | 2,0 |
| Said 1999 | c-SiGe | RP-CVD | 750 °C | 10 | 15 | 0,559 | 24,2 | 73 | 10,3 |
| Li 2016 | c-SiGe | RP-CVD | 750 °C | 82 | 2 | 0,349 | 11,6 | 0,71 | 2,9 |
| Hadi 2014 | c-SiGe | LP-CVD | 900 °C | 25 | 2 | ~0,43 | 16,5 | ~ 60 | ~4,3 |
| Hadi 2014 | c-SiGe | LP-CVD | 900 °C | 25 | 4 | ~0,45 | 17,5 | ~ 58 | ~4,6 |
| Cariou 2014 | c-SiGe | RF-PECVD | 175 °C | 27 | 1,9 | 0,413 | 18,8 | 77,5 | 6,1 |
| Cariou 2014 | c-Si | RF-PECVD | 175 °C | 0 | 1,7 | 0,501 | 16,1 | 78,6 | 6,4 |
| This work | c-Si | RF-PECVD | 200 °C | 0 | 1,4 | 0,57 | 15,4 | 76,4 | 6,7 |
| This work | c-SiGe | RF-PECVD | 175 °C | 7 | 1,1 | 0,56 | 14,6 | 74,3 | 6,1 |
| This work | c-SiGe | RF-PECVD | 175 °C | 25,8 | 0,89 | 0,35 | 15,7 | 65,4 | 3,6 |
| This work | c-SiGe | RF-PECVD | 200 °C | 23,7 | 0,89 | 0,4 | 16,6 | 69,4 | 4,6 |

**Figure 2.27 - Review of single $Si_{1-x}Ge_x$ heterojunction solar cells from literature. Pure Si cells are in red, and the most comparable cells in terms of absorber thickness and Ge content are in green.**

The same heterojunction structures as presented before are fabricated from our SiGe epitaxial layers: (p++)c-Si wafer/epi-$Si_{0.73}Ge_{0.27}$/a-Si:H/(n)a-Si:H/µ-$SiO_x$. We will compare their characteristics to these of pure silicon equivalent devices. The epitaxial layers that had been presented in II.2.5 and 6 ($Si_{1-x}Ge_x$ absorbers with x=7, 13.8, 25.8 and 32.5) have then been dipped into HF before depositing the amorphous stack. The J-V characteristics of SiGe solar cells as compared with the previous Si solar cell are gathered in Figure 2.28, along with their measured characteristics. The thickness of each absorber is reported. We also calculated the difference between the theoretical bandgap of the layer and the measured $V_{OC}$, as an indication of recombination losses.




c)

| %Ge | Thickness (µm) | Gap (eV) | $V_{OC}$ (V) | Gap-Voc | $J_{SC, I-V}$ (mA/cm²) | FF (%) | Eff (%) |
|---|---|---|---|---|---|---|---|
| 0 | 1,4 | 1,12 | 0,57 | 0,55 | 15,4 | 76,4 | 6,7 |
| 7 | 1,11 | 1,09 | 0,56 | 0,53 | 14,6 | 74,3 | 6,1 |
| 13,8 | 1,23 | 1,06 | 0,50 | 0,56 | 15,7 | 73,7 | 5,7 |
| 25,8 | 0,89 | 1,02 | 0,35 | 0,67 | 15,7 | 65,4 | 3,6 |
| 32,5 | 0,88 | 0,99 | 0,32 | 0,67 | 16,1 | 62,9 | 3,2 |

**Figure 2.28 - a) J-V characteristics at low-temperature and b) external quantum efficiency of all the solar cells processed after various annealing temperatures, c) summary of the material and cell parameters obtained**

Looking at the $J_{SC}$, we see that that of $Si_{0.93}Ge_{0.07}$ cell is slightly lower than that of pure Si. This is consistent with the simulations, in addition to the fact that the Si is slightly thicker than the others (1.5 µm), consequently enhancing the $J_{SC}$. Then, the $J_{SC}$ increases with the Ge content, until x = 25.8 %. The sample with 32% of Ge was relaxed, leading to a lower crystallinity of the SiGe layer. Thus, its absorption may be lower than that of a strained layer, explaining its rather low $J_{SC}$.

As expected, we find a slight decrease in $V_{OC}$ with increasing %Ge. However the decrease in $V_{OC}$ is more significant than that of the bandgap, as deduced from the difference Bandgap-$V_{OC}$. Especially for the 25.6 and 32 % layers, the $V_{OC}$ has strongly dropped. The layer containing 32.5% of Ge is partly relaxed, thus inducing defects that increase the recombination in the layer.

The more Ge we add, the lower the short wavelength EQE, suggesting that the collection at the surface is lower. By looking at the SEM images of the SiGe layer displayed in Figure 2.29, we actually notice another phenomenon: while $SiGe_{0.07}$ and $SiGe_{0.13}$ exhibit a flat surface and an homogeneous layer, the surface of $SiGe_{25.8}$ is covered by islands. By looking at the cross-section, we realize that these islands result from the growth of a material with different density in the shape of a cone. This behavior has already been observed in the case of a pure crystalline Si grown by PECVD[85] with non-optimized growth parameters. Those cones were amorphous silicon cones, responsible for the epitaxy breakdown of a layer. An amorphous layer is initiated in the layer, and keeps on propagating during the growth. Thus, our $SiGe_{25.8}$ layer contains lots of cones that are made of amorphous SiGe.

The presence of these cones can be responsible for 1) the increase in shunt resistance observed on the ***J-V*** curves (thus a lower FF), as the cones can be alternative pathways for current to flow, 2) the lower $V_{OC}$ because the islands prevent from a sharp interface with a-Si:H emitter and from a good front contact passivation.

By comparing our result with these from literature gathered in Figure 2.27, we can observe that our $V_{OC}$ for Si heterojunction without Ge (0.57 eV) is higher than that of other heterojunctions reported (Cariou, Oshima, highlighted in red). The $J_{SC}$ of our pure Si solar cell is higher than that of an MBE grown Si absorber of 3 µm while ours is only 1.5 µm thick, leading to a record efficiency of 1.5 µm Si of 6.7 %, which is also better than previously achieved in the lab (Cariou et. al[54]). For our SiGe solar cells, we cannot compare directly the one with 7% and 13.6 % of Ge. But we notice that the $SiGe_{25.8}$ has performances below these reported in literatures (highlighted in green), mainly due to our lower $V_{OC}$.

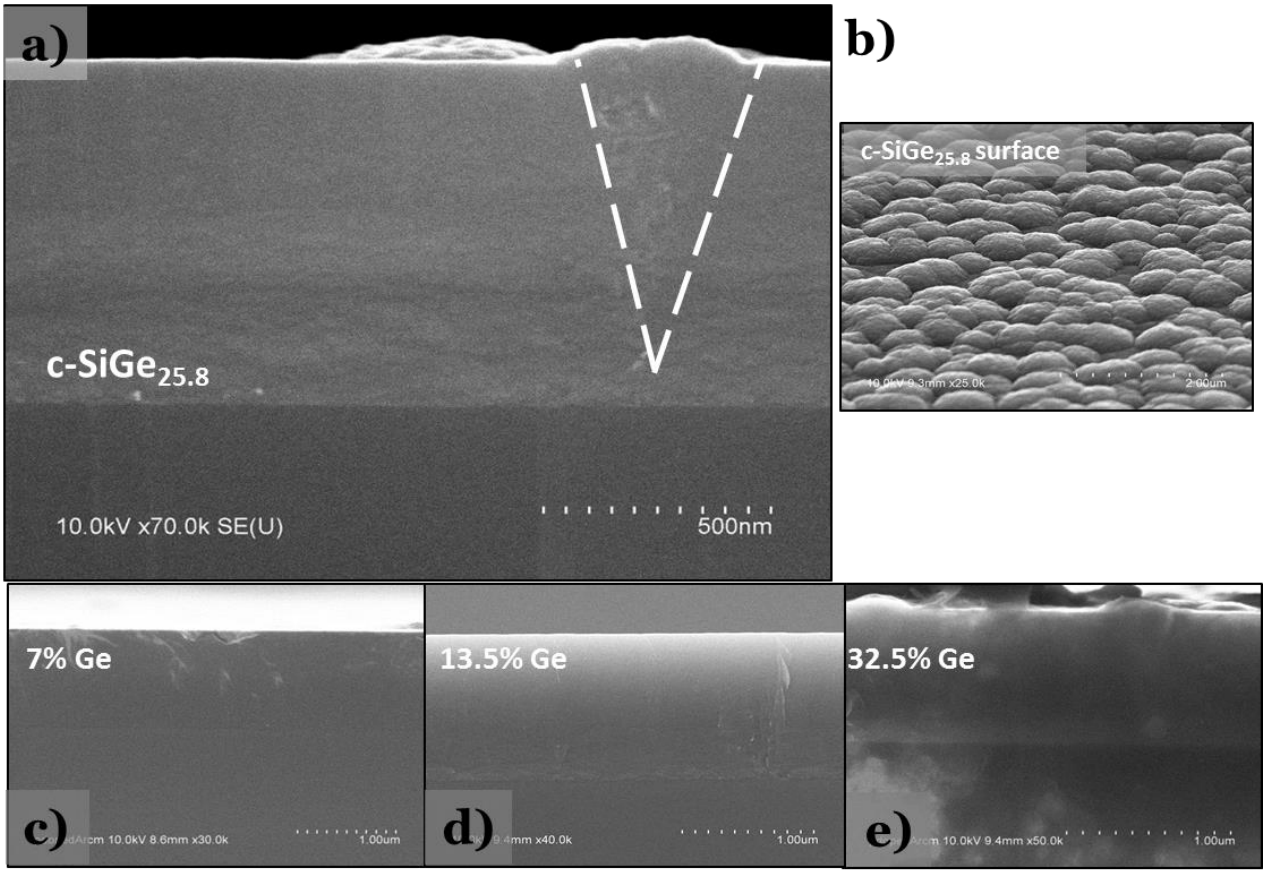


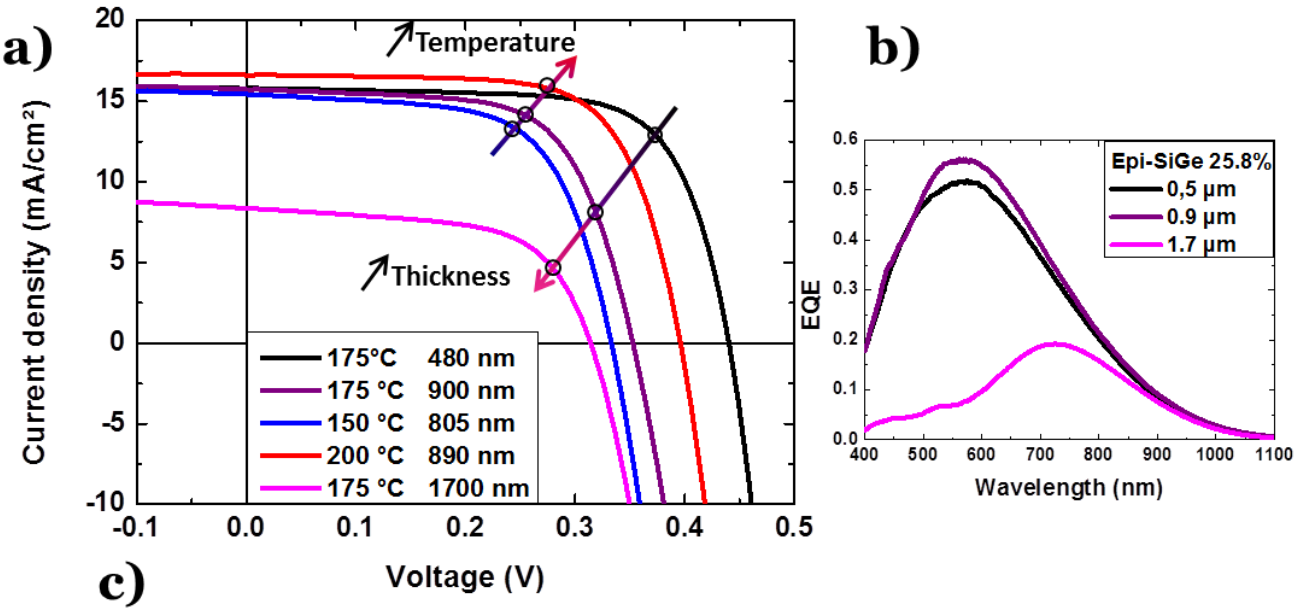

**Figure 2.29 -SEM images of a)b) the cross-section and surface of $SiGe_{25.8}$ c)d)e) the cross-section for x = 7%, 13.5% and 32.5%.**

In order to have a better insight in this strong $V_{OC}$ reduction, we varied the thickness of $SiGe_{25.8}$ absorber from 500 nm to 1.7 µm. We already observed from XRD that the best material quality was observed for 500 nm. Also, at 900 nm, amorphous cones were visible in the layer by SEM. The thicker layer appears to be relaxed. The ***J-V*** curves and characteristics of the different cells with various absorber thicknesses are displayed in Figure 2.30.a and c (Black, purple and pink curves). It appears that the best solar cell is the thinner one, which has an efficiency of 4.7 %. The $V_{OC}$ of 0.43 V is actually way more satisfying, and is comparable to that of literature (green lines in Figure 2.27). It

may be explained by the fact that there are no defective cones in the thinner layers that would higher the shunt resistance, and lower the quality of the epi-SiGe/a-Si:H interface. The cell with higher thickness (1.7 µm) has very bad solar cell characteristics. Not only the $V_{OC}$ and FF are low, but also the $J_{SC}$ is almost divided by 2 (only 8.35 A/cm²). This is not only explained by the relaxation of the layer. The EQE in Figure 2.30.b. confirms this huge drop in $J_{SC}$. There is almost no collection anymore at short wavelengths. It actually shows that the conditions that are used to grow $SiGe_{25}$ are not optimized in order to grow thick SiGe layers.

We thus propose to change the growth temperature, aiming at finding better growth conditions for the realization of SiGe layers, with a thickness around 900 nm: while all the SiGe absorbers studied up to now were performed at 175 °C, we studied the effect of a growth at 150 °C and 200 °C. Material characterizations from Part II.2.4. showed that the growth at 150 °C leads to a relaxed layer with higher Ge content. The 200 °C grown layer has a shrink on Ge content (only 23.7 %) but exhibits a higher XRD peak intensity. The resulting ***J-V*** curves (blue, purples and red in Figure 2.30.a) show that the layer grown at 200 °C exhibits the best electrical properties. The $V_{OC}$ reaches 0.4 V, and 4.6 % of conversion efficiency is measured, exceeding the efficiency of the comparable cell from Hadi *et al.*[116] The $J_{SC}$ of this layer is 1 mA/cm² above those grown at lower temperatures. This is not negligible, considering that the Ge content is lower (thus its $J_{SC}$ should be lower). It shows that the quality of the epitaxial layer is highly increased when grown at 200 °C. However, both $V_{OC}$ and FF are still slightly lower than those of the thinner (500 nm) layer grown at 175 °C, suggesting that there is still needs for improvement in the growth conditions for thick $Si_{1-x}Ge_x$ layers.

To conclude, we showed here that we still do not have the optimal growth conditions for growing thick $Si_{1-x}Ge_x$ at high Ge content. While $SiGe_{07}$ and $SiGe_{13.5}$ cells show acceptable structural and electrical properties, $SiGe_{25.8}$ is good for 500 nm thick absorber, but has strongly degraded performances for higher thicknesses, due to the apparition of amorphous cones and the relaxation of the layer. We showed that performing the growth at 200 °C can improve the crystalline quality, and also its solar cell performances. From now on, in order to optimize the growth conditions of $Si_{1-x}Ge_x$, we must play on the growth temperature, whose optimum seems to be higher than 175 °C. Once this optimum temperature found, we could gain in quality by playing on the two other tunable parameters that had been kept constant: RF power and pressure. Those parameters had been optimized for the growth of pure c-Si, but the optimum may be different for the growth of SiGe. Further experiments need thus to be performed on SiGe growth in order to be able to grow layers with thicknesses above 5 µm.




c)

| Thickness (nm) | Growth Temp. (°C) | %Ge | Relax. | $V_{OC}$ (V) | $J_{SC,\ I\text{-}V}$ (mA/cm²) | FF (%) | Eff (%) |
|---|---|---|---|---|---|---|---|
| 480 | 175 | 25,6 | 0 | 0,43 | 14,9 | 74,2 | 4,7 |
| 900 | 175 | 25,8 | 0 | 0,35 | 15,7 | 65,4 | 3,6 |
| 805 | 150 | 27,7 | 0,32 | 0,33 | 15,4 | 63,9 | 3,3 |
| 890 | 200 | 23,7 | 0 | 0,4 | 16,6 | 69,4 | 4,6 |
| 1700 | 175 | 26,9 | 0,27 | 0,31 | 8,35 | 60,6 | 1,6 |

**Figure 2.30 - a) *J-V* characteristics at low-temperature and b) external quantum efficiency of all the solar cells processed after various annealing temperatures, c) summary of the parameters obtained**

# II.4. Conclusion and perspectives

To conclude on the results on epi-Si layers, we actually have a very good heterojunction solar cell with 1.5 µm of epi-Si that has been annealed at 200 °C. We reached 7% of conversion efficiency, which is better than the previous results obtained in the lab for similar device structure and epi-thickness[54] mainly thanks to a higher $V_{OC}$ value (0.57 V). It shows the high potential of such material for the integration into a more complex device. The increase in epitaxial layer thickness led to an improvement of the efficiency, but we face a higher recombination that lowers the $V_{OC}$. The study of the effect of an annealing on the solar cell properties led to the conclusion that the epitaxial layer should not undergo an annealing at a temperature above its deposition temperature, otherwise the hydrogen may stop passivating the defects, and create blistering at the interface with the substrate.

Introducing Ge into the layer has shown an increase in $J_{SC}$ and a decrease in $V_{OC}$ as compared with a pure Si absorber. We showed that the more Ge is incorporated in our layer, the lower the growth rate, which could be limiting as we aim at growing layers thicker than 5 µm. The use of a less diluted Ge gas cylinder could help tackling this issue. We also found that the growth at 175 °C in Octopus with fixed pressure (2 mbar) and RF power (50 W) may not be the optimum growth conditions for $Si_{1-x}Ge_x$ layers. Indeed, if thin layers have good structural properties and lead to conversion efficiencies up to 6.1 %, our solar cells with $Si_{1-x}Ge_x$ layers still have a lower efficiency than with c-Si absorber. We faced issues by trying to grow thicker layers, due to the relaxation of the strain in SiGe, but also to the apparition of epitaxy breakdown. A path worth exploring would be to grow SiGe at higher temperature; we indeed showed that an absorber grown at 200 °C led to an increase in mostly $V_{OC}$, but also in $J_{SC}$ and FF, as compared with the same grown at 175 °C.

This chapter was dedicated to the growth of Si and SiGe on top of a (100) Si substrate by low temperature PECVD. We proved the good properties of these materials by fabricating Si(Ge) heterojunction solar cells, and proposed some paths towards the growth of better Si(Ge) layers with higher thicknesses. However, these results are satisfying enough to move to the next step: trying to grow crystalline c-Si and c-SiGe on top of a GaAs substrate and on top of a full epitaxially grown $Al_xGa_{1-x}As$ solar cell. The next chapter will be dedicated to the heteroepitaxy by PECVD of Si on GaAs substrates.

Chapter 3

# PECVD heteroepitaxy of Si on GaAs

## Content

In the previous chapter, we have presented the epitaxial growth of Si and SiGe on Si substrates, and assessed their crystalline and electrical quality. This chapter is dedicated to the integration of Si material with GaAs and their mutual effect on each other. We will introduce the heteroepitaxial growth of Si on GaAs, and use XRD and GIXRD to assess the structural properties of the Si layer grown on GaAs, aiming at understanding the first stages of PECVD growth. Then, in order to anticipate the integration of our process in the fabrication of a tandem solar cell, we will study the effect of PECVD on the doping properties of the GaAs material.

# III.1. Growth of Si on GaAs

The literature about the growth of Si on GaAs is quite scarce. In the late 80's, several papers mentioned the growth of crystalline Si on top of GaAs by Molecular Beam Epitaxy (MBE)[117,118]. However, they all report the growth of only a few Si monolayers. Actually, they found that the critical thickness of Si on GaAs is of the order of 1.5 nm, and grew Si below this critical thickness, mainly to form a contact layer on GaAs. Also, some Si/GaAs supperlattices have been successfully grown[119,120]. In 1985, Zalm *et al.*[121] tried to grow thicker Si (up to 500 nm) and showed that for MBE with a growth temperature below 400 °C, the deposited films are amorphous, even after further annealing at 600°C. They report the existence of a surface exchange between Ga and As atoms with the arriving Si adatoms. Moreover, when the growth occurs at 600 °C, there is an important doping of the Si layer by Ga and As atoms. The lattice-mismatch induced strain is accommodated by disorder at the very interface, where the dislocations are located. However, since then, no study on bulk Si can be found. Recently at LPICM, the first proof of monocrystalline silicon growth on top of GaAs has been shown. It is extensively described in the paper from Cariou *et al.*[122] We present here some of the key parameters needed to obtain epitaxial growth of Si on GaAs by PECVD, that will be taken into account in the realization of the layers presented in this chapter.

## III.1.1. Substrate cleaning

The first critical step to grow crystalline Si on GaAs is the GaAs substrate cleaning. In MOCVD, the GaAs oxide is thermally removed during the process taking place around 680 °C. Our low process temperature does not allow for such oxide removal. Literature reports some possible surface preparation by annealing at 600 °C in hydrogen[123]. Also, native oxide can be chemically etched, but it requires various steps into several chemical solutions [124,125]. Moreover the exposure to air between the chemical cleaning and the loading into the reactor would not give a stable passivated surface. Thus, etching the native oxide by an in-situ SiF4 plasma has been investigated. By modifying the power, and especially the etching time, it was possible to successfully remove the GaAs oxide. As for Si substrate cleaning (Chapter II.2.1.(p. 34)), GaAs cleaning is made in 3 steps: at 175 °C, 30 sccm of $SiF_4$ are introduced in the reactor with a pressure of 90 mTorr with two steps: about 4 minutes with 35 W, and then to smooth the surface, a 2 minutes at lower RF power (10 W). Finally, a 30 s step of $H_2$ plasma is added in order to remove the possible fluorine present at the growth surface and produce a better H-terminated surface. Not surprisingly, this step of $SiF_4$ plasma cleaning induces a certain roughness on the substrate.

For example, AFM measurements on the surface of an epitaxial GaAs layer grown by MOVPE are shown in Figure 3.1 before and after etching under the conditions given above. While the RMS (root mean square) was of 0.24 nm before etching, and we could distinguish the typical steps of MOVPE growth, after etching, the RMS increased to 0.4 nm and some spots with a height up to 5.8 nm can be distinguished. Note that this cleaning process leaves a surface under a state far from the ideal one used in a standard epitaxy.

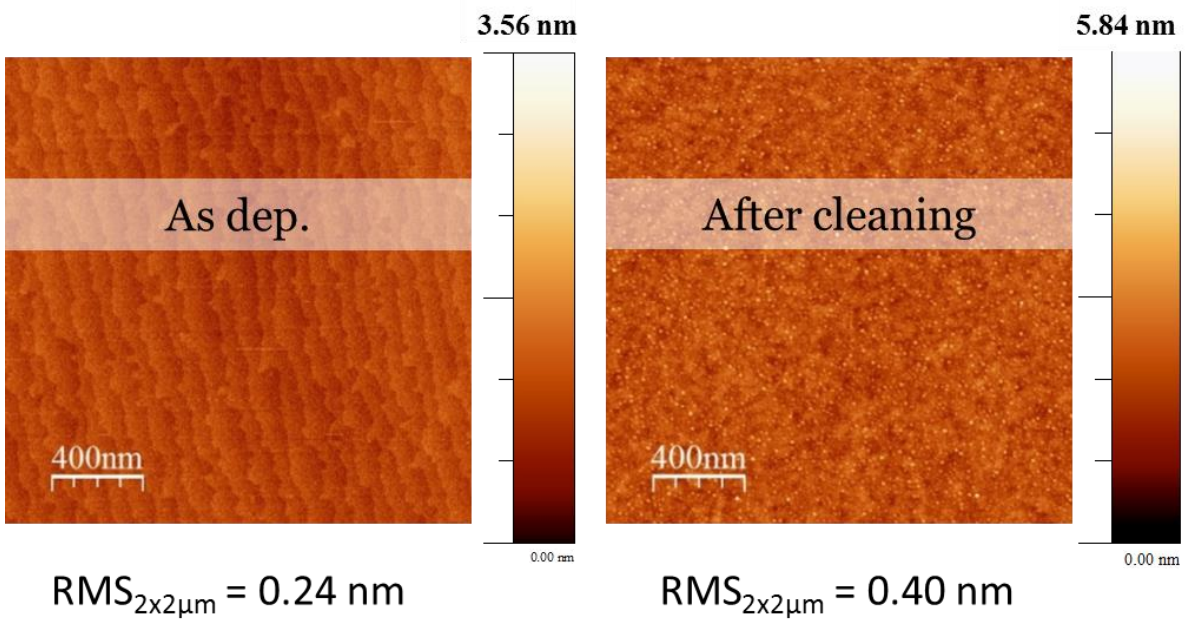



**Figure 3.1 - AFM images of the surface of the epitaxial GaAs layer before and after plasma cleaning under optimized process conditions for Si heteroepitaxy**

## III.1.2. Si heteroepitaxy on GaAs

As for the growth of Si on Si substrates, the silane/hydrogen dilution is a key parameter to obtain crystalline Si on GaAs. By varying the $SiH_4$ flow rate with fixed $H_2$ flow rate (similarly to Figure 2.8 of chapter II), we found that the epitaxy window is smaller than on Si substrates. In the Octopus reactor, it was found that the $SiH_4$ flow rate can be varied from 15 to 40 sccm on Si substrate. The same experiments on GaAs substrates showed that the Si grown is crystalline only for $SiH_4$ flow rate ranging from 20 to 30 sccm, and 35 sccm leads to a fully amorphous layer.

Figure 3.2. shows the TEM analysis of a Si film grown on GaAs by PECVD. Detailed analysis of the crystal quality can be found in Cariou *et al.*[122] The sample consists of a 650 nm thick Si layer on top of a GaAs wafer. The whole layer is visible in Figure 3.2.b. No threading dislocation is observable on the image, despite the 4% lattice mismatch between the two materials. The defects must thus be mainly misfits dislocations located at the interface. Moreover, a HRTEM analysis of the interface shows an excellent atomic order in the epi-Si, and a very sharp interface. The well-defined spots in the electron diffraction pattern in Figure 3.2.c. indicate a fully mono-crystalline layer. Zooms on the {004} and {440} planes (in Figure 3.2.d. and e.) reveal two distinct spots, corresponding to both GaAs and Si contributions, and indicating that the Si grown on GaAs is relaxed. Thus, it has been shown that it is possible to grow thick Si layers on GaAs substrates, which is fully relaxed, and

present no threading dislocations despite the 4 % lattice-mismatch. We will try in the next section to understand how this growth can happen with so few dislocations, by studying the early stages of the growth with X-ray diffraction.

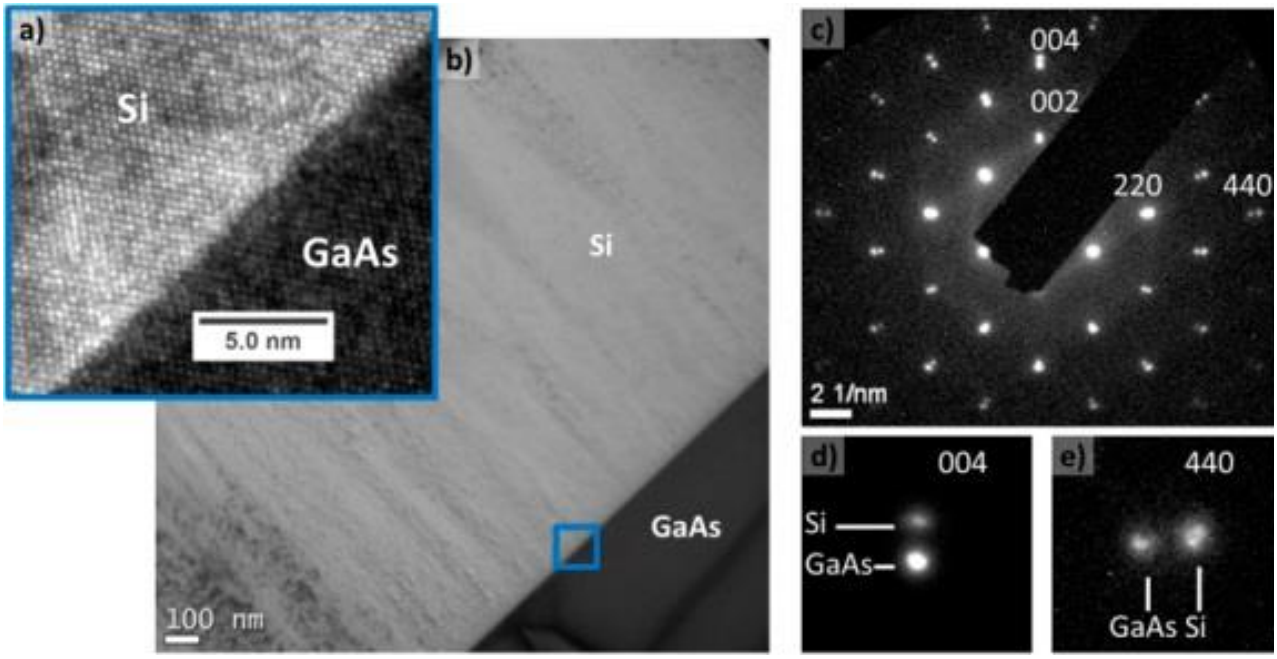



**Figure 3.2 - a) Cross-section HRTEM image of epi-Si/GaAs interface. b) Low magnification cross section picture of a 650 nm thick epi-Si layer on GaAs. c) Diffraction pattern of PECVD epi-Si/GaAs interface: the double points visible for each reflection (see zooms (d,e)) are the signature of both Si and GaAs lattices. From Cariou *et al.*[6]**

## III.2. Growth of Si on GaAs: study of the early stages

In this study, we focus on the very first stages of the growth of Si on GaAs, in order to assess its structural properties, relaxation, and stress in the lattice. In this way, we hope to better understand how PECVD epitaxial growth can happen at such low temperature, and what are the growth mechanisms involved. To do so, we studied Si layers grown on GaAs substrates with thicknesses ranging from 7 nm to 1 µm, and systematically measured the in-plane and out-of-plane lattice parameters of the grown Si. The very thin layers cannot be easily characterized in our laboratory diffractometer. Indeed, the diffracted volume is too small as compared to the substrate contribution, and also our incident X-Ray flux is too low. Thus, we applied for a synchrotron beam shift at Soleil, to have a flux high enough to determine the Bragg angles of the {004} diffraction planes. Also, with their diffractometer (DiffAbs), we will be able to probe the {220} planes that give accurate measurement of the in-plane parameter.

## III.2.1. Grazing Incidence X-ray Diffraction

For the following experiments, the beamline DiffAbs from SOLEIL synchrotron was used[126]. It is dedicated to the study of the structural properties of a wide variety of materials. It offers the possibility of doing X-ray diffraction combined with an oven that enables in-situ annealing. This line uses radiation from a bending magnet, and a monochromatic beam of X-Rays can be chosen in the spectral range from 3 to 23 keV. In our case we used 9.5 eV. The experimental station consists of a six-circle diffractometer. Four circles are used to orient the sample, and two circles are used for XRD measurements in the vertical and horizontal plane.

The geometry of this diffractometer enables not only to probe the {004} planes in high angle ω-2θ configuration, as already presented in Chapter 2, but also in $2\theta_\chi$-ϕ in-plane configuration Figure 3.3.a.&c show the planes probed in a ω-2θ scan, and one of the scans performed with synchrotron beam. The measured intensity is considerably higher ($10^{11}$ counts) than in our laboratory diffractometer (<$10^6$ counts). Thus, there is enough flux to be able to detect the signal due to the diffraction of the epitaxial layer, whose intensity is low as compared to that of the substrate. A

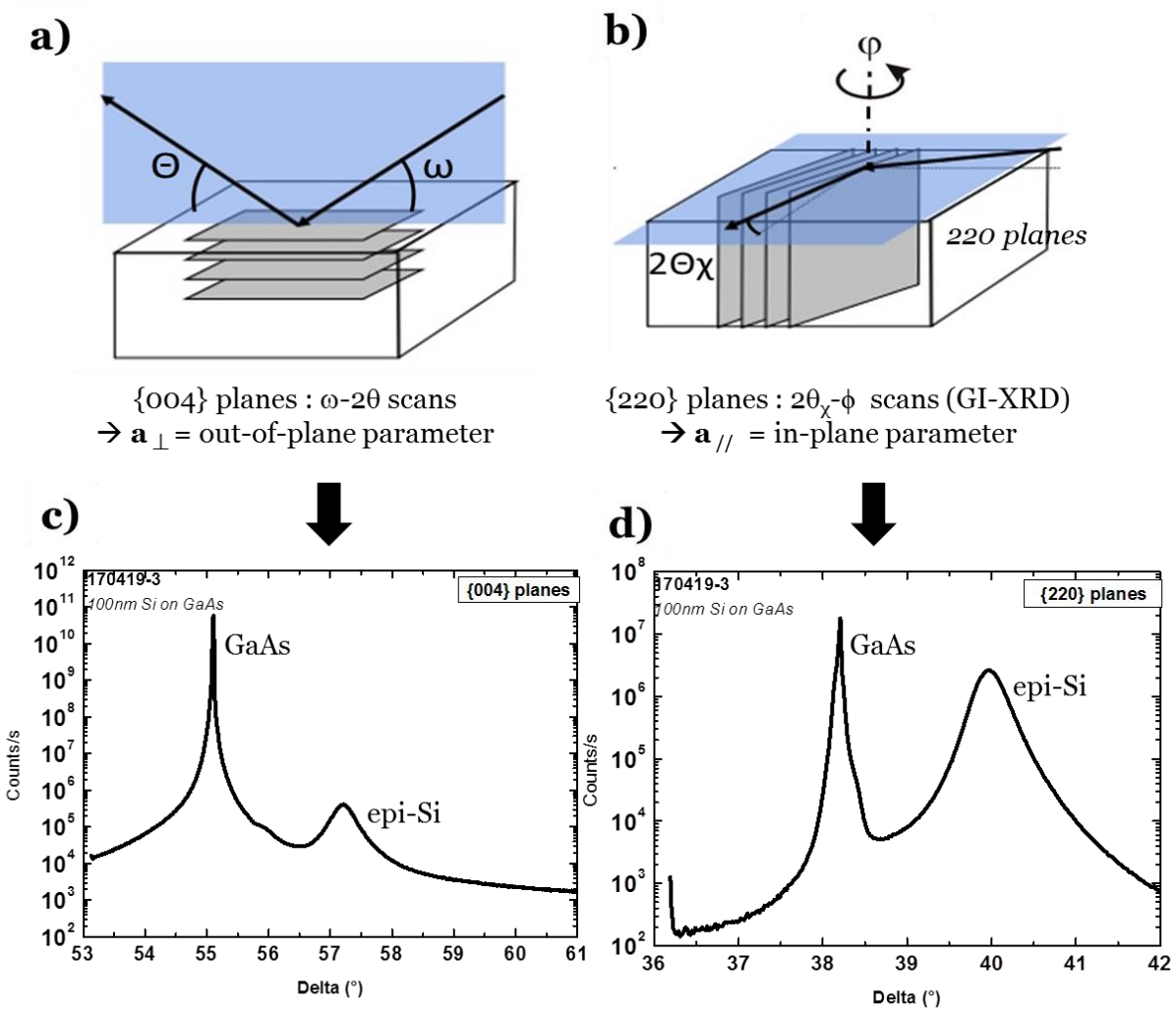



**Figure 3.3 - Schematics of a sample and the planes probed in a) a ω-2θ configuration b) GIXRD configuration. c) and d) corresponding scans on a 100 nm thick epi-Si sample on GaAs.**

second geometry could be used: Grazing Incidence X-Ray Diffraction (GIXRD). In this configuration, performing $2\theta_\chi$-$\varphi$ scans enables to probe the {220} planes, which are perpendicular to the (100) surface, giving information on the in-plane lattice parameters $a_{//}$, as schematized in Figure 3.3.b. We consider that the parameter along both x and y directions are identical. Figure 3.3.d. shows a {220} scan. We observe that the layer peak intensity is now almost comparable to that of the substrate. Actually, in this configuration, as it is at grazing incidence (0.2°), the beam probes a high volume of diffracting planes, and does not penetrate that much in the substrate.

To perform this study, a batch of samples has been grown in ARCAM reactor on GaAs layers previously grown by MOVPE. In order to have a better insight on what happens at the interface, in the early stages of the growth, we started with a 7 nm layer. Then, layers with increasing thicknesses were grown: 12 nm, 20 nm, 43 nm, 53 nm, 100 nm and 1 µm.

The {004} and {220} scans (i.e. out-of-plane and in-plane respectively) presented in Figure 3.3.c and d. correspond to a 100 nm epi layer on GaAs. We can distinguish two peaks: the sharper on the left is that of the GaAs substrate, and on the right, the wider peak with lower intensity corresponds to the epi-layer. The fact that in the {220} scan, two distinct peaks can be seen means that the layer is not strained by the substrate. Each material has its own in-plane parameter $a_{//}$. In a strained configuration, the epitaxial layer takes the $a_{//}$ value of the underlying substrate as shown in Figure 3.4.b. When the substrate lattice constant is higher than that of the epitaxial layer (which is the case for GaAs substrate compared to epi-Si), the strain should be tensile, and $a_\perp$ should decrease. As GIXRD scan shows that we are not in the strained case, the epi-Si should be in the relaxed state shown Figure 3.4.a, meaning that the Si is cubic with its own bulk lattice parameter $a_{o,Si}$.

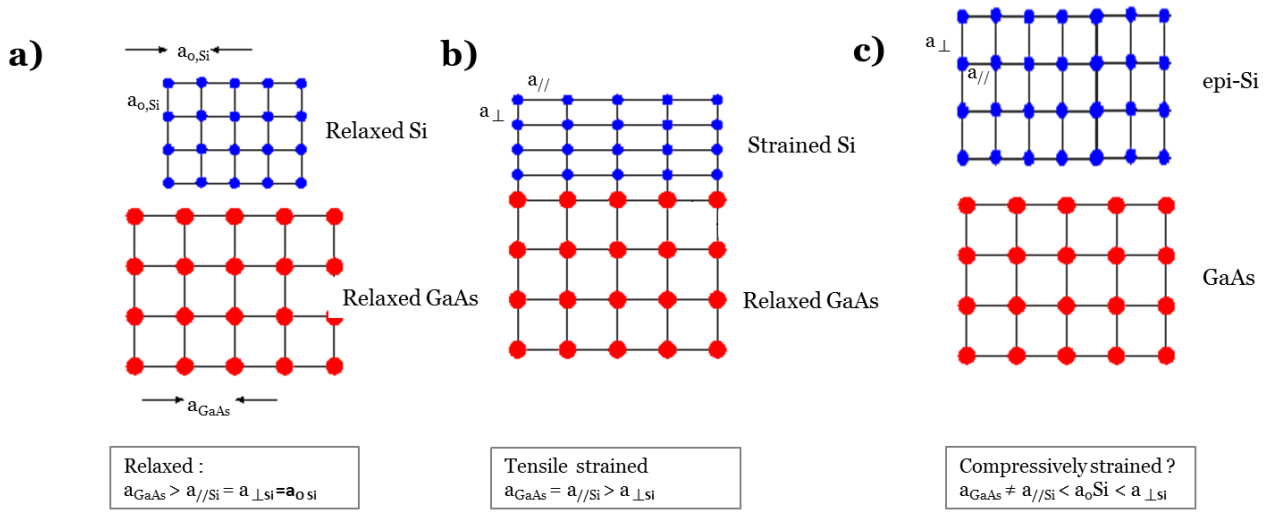



**Figure 3.4 - Schematics of an heteroepitaxy in case of a larger substrate lattice constant than that of theepi-layer in the a) relaxed configuration, b) strained configuration (tensile strain) c) shematics ofour epi-Si/GaAs according to the lattice parameters deduced from XRD measurements**

From both ω-2θ and 2θχ-φ scans, we use the following equations to determine the in-plane parameter $a_{//}$ and the out-of-plane parameter $a_\perp$:

$$\frac{\Delta a_{\parallel,epi}}{a_{\parallel,epi}} = \frac{\sin(\theta_{\chi,sub}^{(220)}) - \sin(\theta_{\chi,epi}^{(220)})}{\sin(\theta_{\chi,epi}^{(220)})} \quad \textbf{Eq 3.1,} \qquad \frac{\Delta a_{\perp,epi}}{a_{\perp,epi}} = \frac{\sin(\theta_{sub}^{(004)}) - \sin(\theta_{epi}^{(004)})}{\sin(\theta_{epi}^{(004)})} \quad \textbf{Eq 3.2}$$

Where $\theta_{\chi}^{(220)}$ is the diffraction angle of the {220} planes (in the grazing incidence configuration) and $\theta^{(004)}$ the diffraction angle of {004} planes. Considering that the substrate lattice parameter $a_{0,GaAs}$ is unchanged, $a_{//}$ and $a_{\perp}$ can be deduced from the following equations:

$$a_{\parallel,epi} = a_{0,GaAs}\left(1 + \frac{\Delta a_{\parallel,epi}}{a_{\parallel,epi}}\right) \quad \textbf{Eq 3.3,} \qquad a_{\perp,epi} = a_{0,GaAs}(1 + \frac{\Delta a_{\perp,epi}}{a_{\perp,epi}}) \quad \textbf{Eq 3.4}$$

We do not show all the scans here, but for each sample, the scans were similar to the one Figure 3.3.c and d. The thinner is the layer, the broader is the epitaxial peak. Even for our 7 nm layer, a peak on the right of the substrate peak could be distinguished in the in-plane configuration, meaning that the layer is relaxed even for this ultra-thin layer. For each sample, we calculated the $a_{//}$ and $a_{\perp}$ using Eq 3.3, and Eq 3.4. The values as a function of the layer thickness are gathered in Figure 3.5.a.

The calculations of in-plane and out-of-plane lattice parameters revealed the following behavior: first, we can notice that for each sample, $a_{\perp}$ is higher than $a_{//}$. As an indication, the theoretical lattice parameter of bulk Si is drawn in gray. The precision on $a_{//}$ is around ±0.004 Å, while the precision on $a_{\perp}$ varies with the film thickness. The values obtained for the 7 nm thick layer present such high error bars that we preferred not to include it in Figure 3.5.a. The FWHM of its peak is very high due to its very low thickness, however, the center of its large peak leads to the same trend than the presented result: not only $a_{\perp}$ is really higher than the theoretical value, but also $a_{//}$ happens to be lower than the theoretical one. Thus the Si has a tetragonal lattice. A schematic of the atom dispositions as deduced from the HRXRD measurements is shown in Figure 3.4.c: the Si lattice is not tensile strained by the GaAs lattice. On the contrary, it is compressively strained.

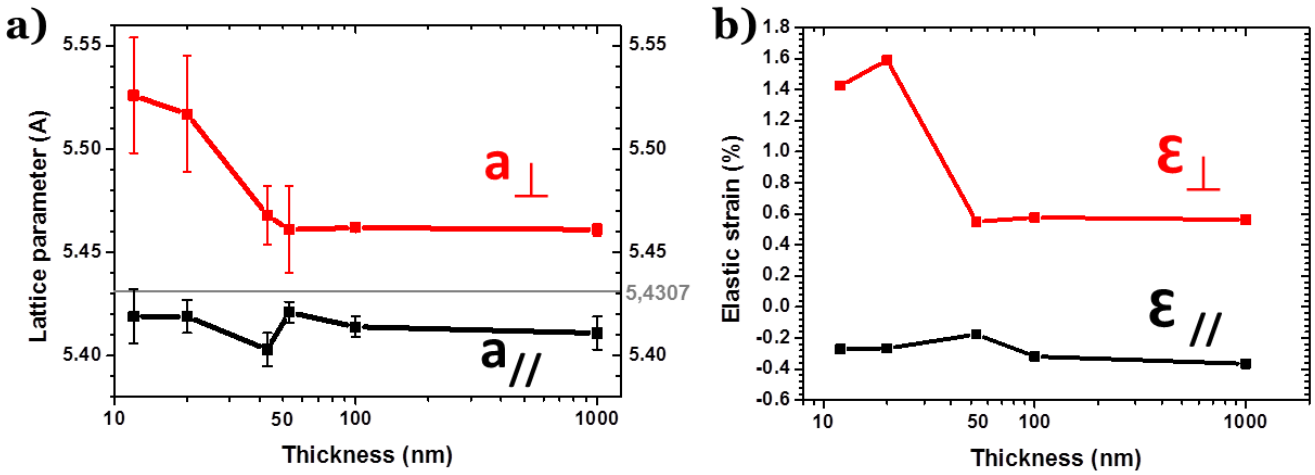



**Figure 3.5 - a) evolution of the in-plane ($a_{//}$) and out-of-plane ($a_{\perp}$) lattice parameters as a function of the layer thickness, b) elastic deformation as a function of the layer thickness.**

The deformations of the lattice are also calculated from the following equations:

$$\varepsilon_{\parallel,epi} = \frac{a_0 - a_{\parallel,epi}}{a_0} \quad \textbf{Eq 3.5,} \qquad \varepsilon_{\perp,epi} = \frac{a_0 - a_{\perp,epi}}{a_0} \quad \textbf{Eq 3.6}$$

By using the theoretical $a_o$ of Si ($a_o$ = 5.4307 Å), the in-plane and out-of-plane elastic strain ε has been calculated for each sample and is plotted in Figure 3.5.b. The in-plane deformation is rather independent of the epitaxial layer thickness, with a value around -0.3 %. Let us note that the 42 nm layer was grown on a GaAs layer highly doped with carbon, which was compressively strained, while all other samples are gown on intrinsic epi-GaAs. It could explain the slight discrepancy in the $a_{//}$ value for this sample. On the other hand, the out-of-plane deformation is very high for the thinner epi-layers, (higher than +1.4 % when the layer thickness is below 20 nm), and stabilizes for thicker layers around a (still high) value of +0.6 %.

Thus, two main phenomena are observed: 1) the out-of-plane parameter $a_\perp$ is really higher than the theoretical one (0.6 %), and even higher for layers below 50 nm (~1.5%). 2) The in-plane parameter $a_{//}$ is smaller than that of bulk Si, with a deformation of -0.3%. These behaviors cannot be explained by the standard strain considerations in heteroepitaxy. We will try to explain both of these phenomena in the following discussion.

## III.2.2. The role of hydrogen

The higher $a_\perp$ is a phenomenon that we have already observed in Chapter II.2.2.(p.37) when we grew epi-Si on a Si substrate. The XRD peak was slightly shifted to the left as compared with that of the substrate. The corresponding lattice parameter of the 1 µm thick layer was calculated to be 5.4434 Å (Figure 2.11.h.). Actually, it seems to be inherent to the growth technique. Literature on PECVD epitaxy on Si substrates using $SiH_4/H_2$ mixtures has already reported the importance of hydrogen in the strain on $a_\perp$, that leads to a slightly higher $a_\perp$ than that of the Si substrate[127]. For example, Shahrjerdi *et al.*[87] studied by ω-2θ scan the influence of the hydrogen content on the peak position of their epi-Si grown by low temperature PECVD. They realized that the higher the H content, the more the peak shifts towards low angles, meaning a higher $a_\perp$ than that of the substrate. Abe *et al*[128]. also reported a similar behavior in the $a_\perp$, and calculated the lattice distortion expected as a function of the H amount in the lattice. However, in all of these papers, the {224} RSM revealed a strained layer, meaning an $a_{//}$ identical to that of the substrate.

To confirm the role of hydrogen on the out-of-plane distortion, SIMS analyses have been performed on one epi-Si layer grown on GaAs. The quantity of hydrogen measured in our layers is presented in Figure 3.6. It confirms that the amount of hydrogen is high throughout the full layer, (around $2\times10^{21}$ at/cm$^3$). Also, interestingly, we notice that this amount is even higher over the first tens of nanometers after the interface with the substrate (it reaches $4\times10^{21}$ at/cm$^3$). This could explain why our layers with thicknesses below 50 nm exhibit a more important strain than that of thicker ones. As XRD analysis probes the full volume, what happens in the first 50 nanometers of a thick layer is hidden in the FWHM of the peak.

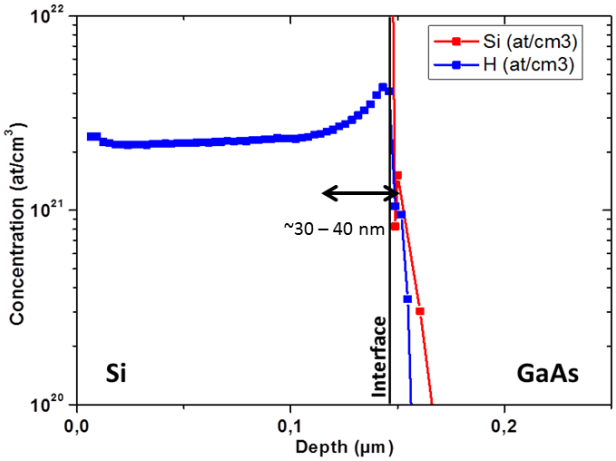



**Figure 3.6 - SIMS analysis of a 150 nm-thick epi-Si layer on GaAs.**

Thus, we found a strong correlation between the strain that increases the out-of-plane parameter and the high quantity of hydrogen in our layers, in accordance with what has already been reported in literature on PECVD epitaxy on Si substrates. The first nanometers close to the interface exhibit a higher concentration of hydrogen, which is consistent with the fact that the measured deformation is even higher for thin layers.

## III.2.3. Effect of thermal expansion mismatch

Let us now focus on the in-plane parameter $a_{//}$, which appears smaller than expected. In order to verify that our $a_{//}$ is indeed lower than that of the bulk Si, and not due to any measurement error or artifact, we performed a {224} RSM on a 1 µm thick layer in our Bruker diffractometer. The mapping is shown Figure 3.7a. As an indication, we drew the lines along which our epitaxial layer is expected to stand in case of a strained Si (yellow arrow) and a relaxed Si (orange arrow). Surprisingly, the position of the epitaxial film corresponds to none of these configurations. This RSM confirms what have been observed by GI-XRD measurements: the $a_{//}$ is smaller than that of the substrate and the Si is in compressive strain (as already illustrated in Figure 3.4.c.).

Contrary to the out-of-plane deformation case, we do not think that hydrogen is responsible for such in-plane deformation of the lattice. First, no obvious correlation was found between the hydrogen content and the $a_{//}$ deformation. Indeed, as seen in Figure 3.5, the deformation of $a_{//}$ is always roughly the same, even for the thinner epi-layers that contains more hydrogen (except for the 42 nm layer that was deposited on top of carbon doped GaAs instead of intrinsic GaAs). Second, if H had a role in this lattice deformation, we would have observed the same type of behavior in the RSM of Chapter 2 when growing epi-Si under similar plasma conditions, on top of Si substrates.

Thus, we must consider another source of strain, which was not present in Chapter 2: the GaAs substrate. Two main substrate-induced strains that can affect the $a_{//}$ of an epitaxial layer: the lattice parameter mismatch, and the thermal expansion mismatch. The lattice-mismatch induced strain should be tensile. {224} RSM and in-plane scans have both shown that the layer is not strained by the GaAs substrate.

We should thus consider the thermal expansion mismatch of our materials. When a material is alone, the lattice parameter evolution with temperature is defined by **Eq 3.7**:

$$a_{\parallel}(T) = a_{\parallel}(T_0) * (1 + \alpha * \Delta T) \qquad \textbf{Eq 3.7}$$

where $a_{//}(T)$ is the in-plane parameter at a considered temperature, $a_{//}(T_o)$ at a reference temperature, and $\boldsymbol{\alpha}$ is the thermal expansion coefficient (CTE) of the material. This coefficient is also dependent on temperature, but in the considered range, we will assume that it is constant. GaAs and Si have a different CTE: $\alpha_{GaAs} = 5.76\times10^{-6}$ $K^{-1}$, and $\alpha_{Si} = 2.6\times10^{-6}$ $K^{-1}$. The thermal expansion coefficients and bulk lattice parameters of Si and GaAs are gathered in **Table 3.1**.

**Table 3.1 : Theoretical bulk lattice parameter and thermal expansion coefficient of GaAs and Si**

| @300 K | | GaAs | Si |
|---|---|---|---|
| $a_{bulk}$ | (Å) | 5.6532 | 5.4307 |
| $\alpha$ | ($K^{-1}$) | $5.76\times10^{-6}$ | $2.7\times10^{-6}$ |

In the case of an heteroepitaxy, the grown layer follows the substrate thermal expansion coefficient, even if the layer is relaxed[129,130], thus thermal expansion strain is compressive. To verify if the epi-layer indeed follows the substrate expansion, we performed in-situ grazing incidence XRD

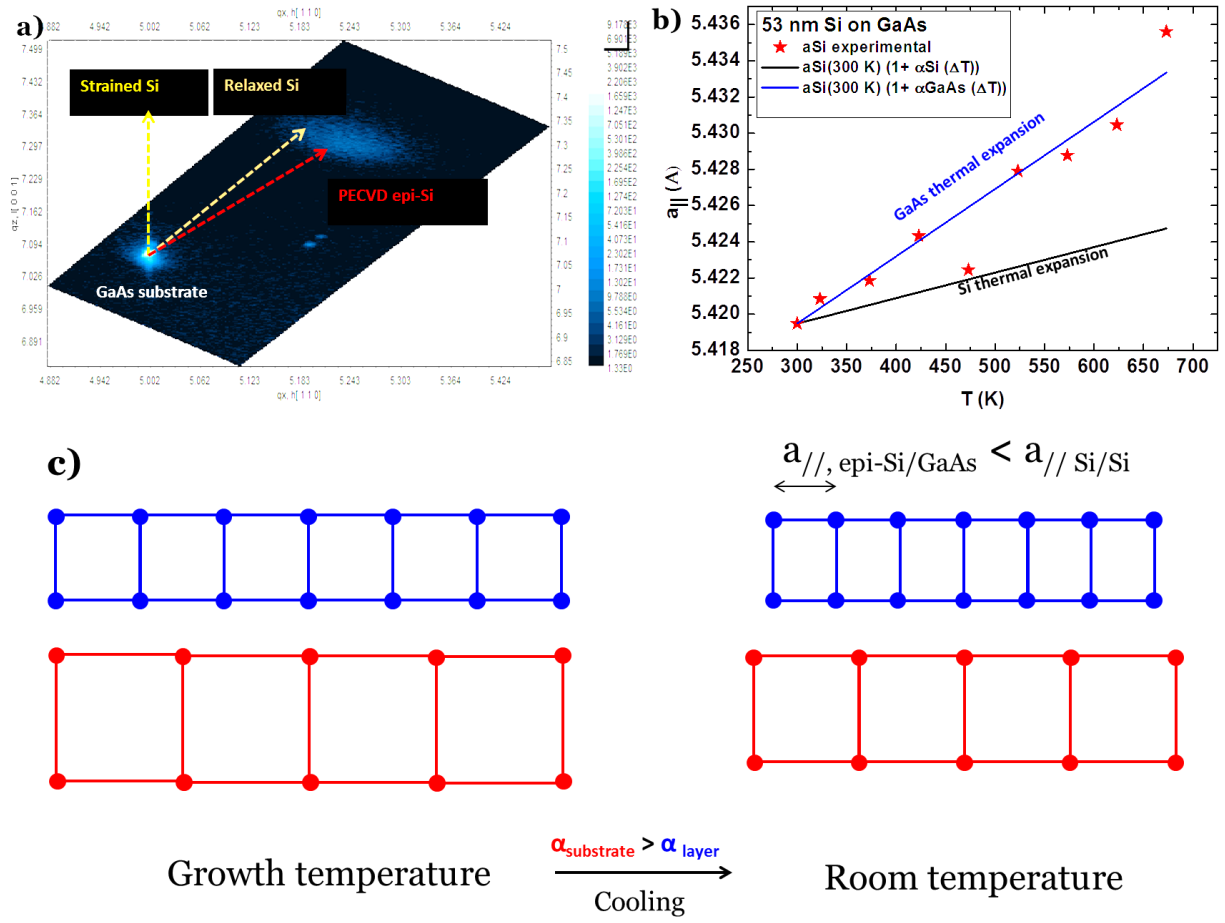



**Figure 3.7 - a) {224} reciprocal space mapping of a epi-Si/GaAs sample, b) evolution of the lattice-parameter of an epi-Si while performing an annealing up to 400 °C, c) Schematics of the lattice of a relaxed Si layer on top of a GaAs during growth, and after cooling down to room temperature, considering that Si follows GaAs thermal expansion coefficient.**

measurements during heating from room temperature to 400 °C. The $a_{//}$ deduced from GI-XRD are reported in Figure 3.7.b (red stars). As an indication, we drew the lattice constant evolution as a function of temperature in the case if epi-Si was following Si thermal expansion (black slope) and if epi-Si follows GaAs thermal expansion (blue slope). As expected, the $a_{//}$ of the epi-Si follows the thermal expansion of the GaAs substrate. Thus, during the cooling from growth temperature, the epi-Si has also followed the GaAs TCE. To illustrate this, a schematics of the deformations induced by the cooling of a relaxed layer is represented Figure 3.7.c, in the case of $a_{substrate} > a_{layer}$ and $\alpha_{substrate} > \alpha_{layer}$. The $a_{//}$ of the epi-Si shrinks due to the high thermal expansion of GaAs. The thermal deformation induced by the difference in thermal expansion between Si and GaAs is defined by **Eq 3.8** :

$$\varepsilon_{\parallel,th}(\Delta T) = \frac{(\alpha_s - \alpha_{epi}).\Delta T}{1 + \alpha_s.\Delta T} \qquad \textbf{Eq 3.8}$$

Where $\alpha_s$ is the GaAs substrate thermal expansion coefficient, and $\alpha_{epi}$ the thermal expansion coefficient of the epitaxial layer, that we assume identical to that of bulk silicon. Here, we calculate the deformation induced by the cooling down from growth temperature (175°C) to room temperature. This calculation leads to a thermoelastic deformation $\varepsilon_{\parallel,th}$=0.05 %. Thus, the thermal strain should slightly lower the in-plane lattice constant of the epi-Si layer. However, at such low growth temperature (175°C), the expected deformation is of 0.05%, i.e. much smaller than the 0.3% reported in Figure 3.5.b.

Let us calculate the $a_{//}$ that should have our heteroepitaxial layer grown at 175 °C on a GaAs substrate after being cooled down to 25 °C. As schematized in Figure 3.8 the lattice parameter at 175 °C of the Si deposited is 5.4328 Å (blue circle), calculated from **Eq 3.9**.

$$a_{\parallel,Si\ bulk}(175\ °C) = a_{\parallel,Si\ bulk}\ (25\ °C) * (1 + \alpha_{Si} * \Delta T) = 5.4307 * (1 + 2.6.10^{-6} * 150) = 5.4328\ Å \qquad \textbf{Eq 3.9}$$

Then, when cooling down from 175 °C to room temperature by following the GaAs thermal expansion coefficient, the Si epitaxial layer parameter should follow the slope given by the red dashed line, i.e. $\alpha_{GaAs}$. At room temperature, $a_{//,Si}$ should have slightly shrunk to the following value:

$$a_{\parallel,Si}(25\ °C) = a_{\parallel,Si}\ (175\ °C) * (1 + \alpha_{GaAs}\ \Delta T) = 5.4328 * (1 - 5.76.10^{-6} * 150) = 5.4281\ Å \qquad \textbf{Eq 3.10}$$

However, this value is still higher than the experimental one ($a_{//,\text{ epi-Si}}$ = 5.4195 Å for the 20 nm-thick layer, blue star in Figure 3.8). To explain this discrepancy, we can assume the following hypothesis: locally, the crystallization temperature of Si on GaAs is not that of the chamber (175°C), but a higher temperature. By resolving the following system of equations, we can deduce the supposed temperature at which our epi-Si was actually crystallized on GaAs, and then cooled down:

$$\begin{cases} a_{\parallel,Si\ bulk}(T_{growth}) = a_{\parallel,Si\ bulk}\ (25\ °C) * (1 + \alpha_{Si} * |\Delta T|) & \textbf{Eq 3.11} \\ a_{\parallel,epi-Si\ experimental}(25\ °C) = a_{\parallel,Si\ bulk}\ (T_{growth}) * (1 - \alpha_{GaAs} * |\Delta T|) & \textbf{Eq 3.12} \end{cases}$$

We calculate $\Delta T$ = 672 °C, thus $T_{growth} \approx$ 700 °C. This temperature can easily be distinguished on Figure 3.8: it corresponds to the intersection of the curve of theoretical $a_{o,Si}$ at a temperature T, and the curve of experimental $a_{Si}$ following $\alpha_{GaAs}$ slope. Note that this calculation contains many approximations: 1) we assume that the GaAs lattice itself is not affected by the epitaxial layer, 2) we have an uncertainty on the experimental measurements of the lattice parameters (±0.004 Å), 3) we considered that the thermal expansion coefficients were constant with temperature, and 4) we used the theoretical bulk Si CTE for our epi-Si. Literature gives no insight on the thermal expansion coefficient of hydrogenated c-Si. However, it has been shown in a-Si:H and µ-Si:H that the thermal expansion coefficient also slightly depends on the hydrogen content [131,132]. The higher the hydrogen content, the lower is the α, thus our c-Si:H may not rigorously follow the black line.

Thus, we believe that the reduction of $a_{//}$ is due to thermal strain induced by the substrate. This reduction is so important that it may have been induced by a cooling down from a higher temperature than the nominal one (175 °C).

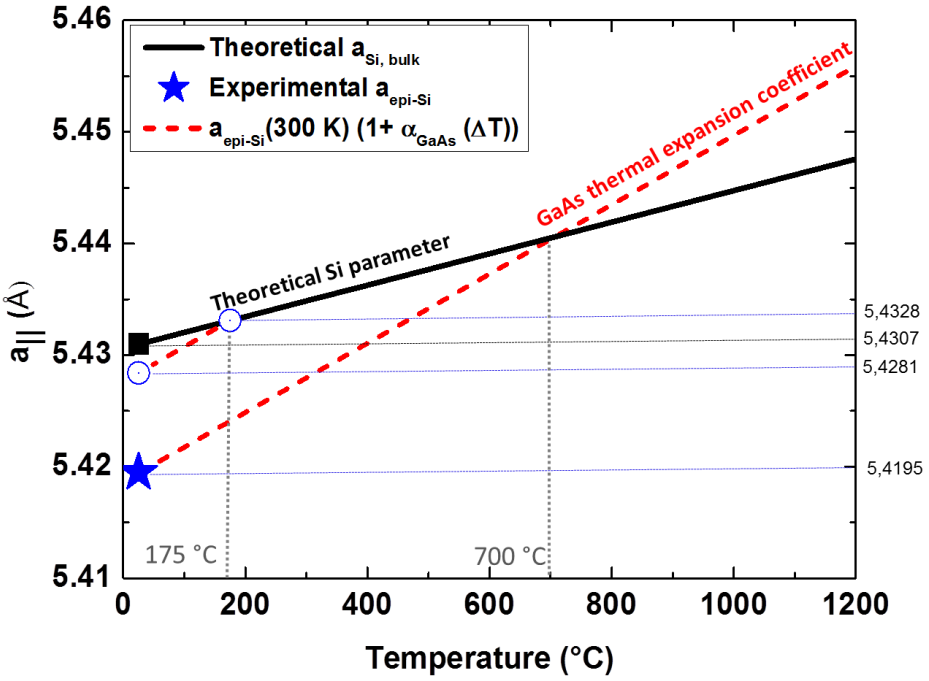



**Figure 3.8 - Evolution of a// of a bulk Si as a function of temperature (black) and expected evolution of a// of epi-Si layer that follows the GaAs substrate expansion.**

## III.2.4. Discussion on growth mechanisms

The mechanism of epitaxial growth of silicon by PECVD is not really understood yet. If TEM studies of the first stages show an island-growth in the first nanometers[133], the question of how epitaxy can happen at temperatures as low as 200 °C has to be raised. The observations and interpretations that we just showed may be the experimental proofs that there are local annealing happening during the PECVD growth, at temperatures high enough to ensure the crystallization of silicon, despite the process conditions that are commonly used to grow amorphous or polycrystalline silicon.

As hydrogen dilution plays an important role in the epitaxial quality, it is likely that hydrogen plays also a role in the crystalline growth, including the fact that it can etch the weak Si-Si bonds that would be responsible for an amorphous growth[134]. Also, hydrogen can provide a local annealing in the grown layer that could help the silicon atom arrangement[135]. This phenomenon is called "chemical annealing" considers the chemical reactions happening between H and the surface (Si dangling bonds or Si-H) is exothermic, and allows reorganization of the Si lattice[136]. Thus hydrogen may participate to the crystallization of Si in PECVD growth.

Also, in epitaxial conditions, the pressure regime used corresponds to a regime where there silicon clusters and nanoparticles are produced in the plasma, as it has been proved by several experimental studies[98,133]. One growth model has been proposed by Roca *et al.*[137] It suggests that the deposition leads to a crystalline material thanks to the contribution of these crystallized nanoparticles in the plasma. *Ab initio* molecular dynamics simulations made by Le. *et al.*[138] showed that depending on the size of these nanoparticles and the impinging power, there can be a local temperature elevation between 1000 and 3000 K, when they reach the substrate. This local heat happens for a short time in the range of the picosecond, followed by a rapid cooling down to the deposition temperature (175 °C in our case). This high temperature elevation can lead to a phase transition of the clusters. Dinda *et al.*[139] showed by simulations that hydrogenated silicon clusters can melt at temperatures around 1000 K, and then recrystallize in the same direction as the substrate. The presence of these crystalline nanoparticles has been experimentally proven in several ways[98,140], however their role in the epitaxial deposition is not easy to determine experimentally. If we consider that this growth mode is the one taking place during the growth of our epi-Si on GaAs, then the lattice deformation schematized in Figure 3.7.c. is happening very locally (the size of the nanoparticles is around 1 - 3 nanometers).

The ion bombardment of the plasma can also induce substrate heating[141]. However, if a temperature elevation was applied to the whole substrate during the deposition, and the substrate was cooled down after plasma shut down, we would have observed the formation of threading dislocations in the thick bulk layers due to the thermal mismatch. Thus, the suppositions of local heating at the growth surface due to hydrogen chemical annealing and/or nanoparticles impact are consistent with our bulks free of threading dislocations.

## III.2.5. Conclusions and perspectives

As a conclusion of this XRD and GI-XRD study of the out-of-plane and in-plane parameters of epi-Si grown by PECVD on GaAs, we can make the following observations and interpretations: first, we found that the out-of-plane lattice parameter ($a_{\perp}$) is more than 1% higher than that of the bulk Si lattice parameter. It has been attributed to the presence of hydrogen. The more hydrogen is present in the layer, the more strained is the epitaxial layer along the growth direction.

Second, we found that the epitaxial layer has a small $a_{//}$, even smaller than that of the Si bulk. Our epi-Si is compressively strained. This behavior is apparently not due to the lattice mismatch between GaAs and Si, neither to the presence of hydrogen. We can attribute this lattice deformation to thermal-strain. However, this strain is higher than expected at the nominal growth temperature (175°C). With no other satisfactory hypothesis, it is reasonable to assume that the shrink in $a_{//}$ is due to thermal mismatch considering a local elevation of crystallization temperature.

Further investigations are required in order to confirm this hypothesis. For example, trying to grow epi-Si on other substrates with different thermal expansion coefficients and probing the resulting $a_{//}$ would help understanding if the key to the PECVD growth of Si is indeed a local temperature elevation. Actually, previous work in the lab[99] showed the growth of Si on Ge. Ge has a thermal expansion coefficient similar to that of GaAs (5.9 $10^{-6}$ $K^{-1}$). GIXRD measurements showed that the epi-Si grown on top of the Ge epitaxial film also exhibits, as in our case, a small $a_{//}$ (5.4257 Å) and a high $a_{\perp}$ (5.444 Å). This behavior was not discussed at that time, but can be explained by the same lattice-mismatch deformation due to a high temperature local annealing. Performing the same kind of experiments with similar process conditions on a Ge substrate (and thus a fixed hydrogen content) would help us have a better insight on the effect of the substrate. For example, InP has a high (8%) lattice-mismatch with Si, and a CTE lower than that of GaAs and Ge (the values[25] are gathered in Table 3.2). We could thus decorrelate the effects of lattice mismatch and thermal mismatch. More accurate calculations, along with more systematic studies on several substrates would help confirm that the $a_{//}$ deformation is linked to the thermal expansion coefficients, and thus, that the epitaxial growth by PECVD happens thanks to a local annealing.

**Table 3.2: Theoretical values of lattice parameter and thermal expansion coefficient for several bulk semi-conductors**

| @300 K | GaAs | Si | Ge | InP |
|---|---|---|---|---|
| a (Å) | 5.6532 | 5.4307 | 5.658 | 5.8687 |
| α ($10^{-6}$ $K^{-1}$) | 5.76 | 2.7 | 5.9 | 4.6 |

Understanding the growth mechanisms of such an unusual epitaxy method is really important and could help us understanding better how to achieve the best material for the desired applications. Moreover, the fact that the grown Si is compressively strained could open the path towards strain engineering, in order to modify the properties of our Si. While the bandgap is not notably impacted by the strain in Si[142], literature reports an elevation in carrier mobility in case of tensile strained Si[143,144]. Also, the hole mobility has been found to be increased in compressive strained Si[145], which could be beneficial for a solar cell absorber.

# III.3. Effect of PECVD on doped GaAs

## III.3.1. Motivations

In the final tandem device, as introduced in Chapter I, the silicon will be grown on top of the tunnel junction (Figure 1.15). In our device, this tunnel junction will end up with a highly doped GaAs layer. This high doping level (>$2\times10^{19}$ $cm^{-3}$) is required for the good functioning of the tunnel junctions, as it will be developped in Chapter IV. The process steps to deposit Si on top of GaAs include a step of hydrogen plasma exposure (after in-situ cleaning). Also, the deposition happens in an environment that is mainly composed of hydrogen. Thus, we may wonder if this hydrogen has an impact on the GaAs layer. Indeed, literature from the eighties reports that a $H_2$ plasma can neutralize the dopants in doped GaAs[146,147]. For example, Rahbi *et al.*[148] studied the acceptor passivation in p-type GaAs doped with different atoms: Zn, C, Si and Ge. They exposed their samples to a hydrogen plasma at temperatures ranging from 150 °C to 300 °C for long durations (up to 8 hours) and found a strong decrease in the doping level determined by Hall Effect measurements. Their GaAs:C layers became

highly resistive after plasma exposure, and hydrogen had diffused into the p-type GaAs layers until a depth of 1 µm to 3 µm. In our device, the last layer will be a ~30 nm highly p-doped layer. Thus, even if our doped GaAs layer is exposed to a $H_2$ plasma in the PECVD chamber for much shorter time and lower temperature than reported in literature, we need to verify if our plasma process does not affect this important layer. To assess the impact of hydrogen on the doping level of GaAs, we exposed some GaAs layers doped with several dopants (Si, Te, C) to a $H_2$ plasma for 30 seconds, and studied their doping level by Electro-chemical Capacitance Voltage measurements, before focusing on carbon-doped GaAs (p-type) which will be the underlying layer in the tandem configuration.

## III.3.2. Doping level profiling: ECV measurements

We will first present this characterization technique which will be extensively used in the last part of this chapter, but also in the next one, dealing with the development of GaAs doped layers for tunnel junctions. Electrochemical Capacitance-Voltage measurements (ECV) allow performing an in-depth profiling of the doping level. We present here its principle, and also its limitations. Contrary to SIMS analysis (Secondary Ion Mass Spectroscopy) that gives the atomic content of a specie in a layer, ECV is employed to measure the active carrier concentration profiles. Those techniques are often coupled in order to have an idea of the doping efficiency (ratio between carrier concentration and dopant atom concentration). ECV uses an electrolyte-semiconductor Schottky contact, so as to create a depletion region where there are no free carriers, but contains ionized donors and electrically active defects or traps. This depletion region behaves like a capacitor. Thus, the measurement of the capacitance provides information of the doping and electrically active defect densities. From this capacitance measurement, the instrument deduces the doping level based on the following equation[149]:

$$N = \frac{C^3}{q\varepsilon 0\varepsilon r A^2} * \frac{1}{dC/dV} \qquad \textbf{Eq 3.13}$$

Between each capacitance measurement, an electrolytic etching of the III-V semiconductor is performed with a solution of Ammonium tartrate and an applied voltage. By controlling this voltage, we can tune the etching rate, and thus the spatial resolution of the measurement. We were thus able to have a very good resolution, enabling to distinguish the doping levels with a depth resolution below 5 nm. The electrochemical cell is pictured in Figure 3.9.a: the wafer is inserted in contact with a seal from which the Ammonium tartrate is inserted.

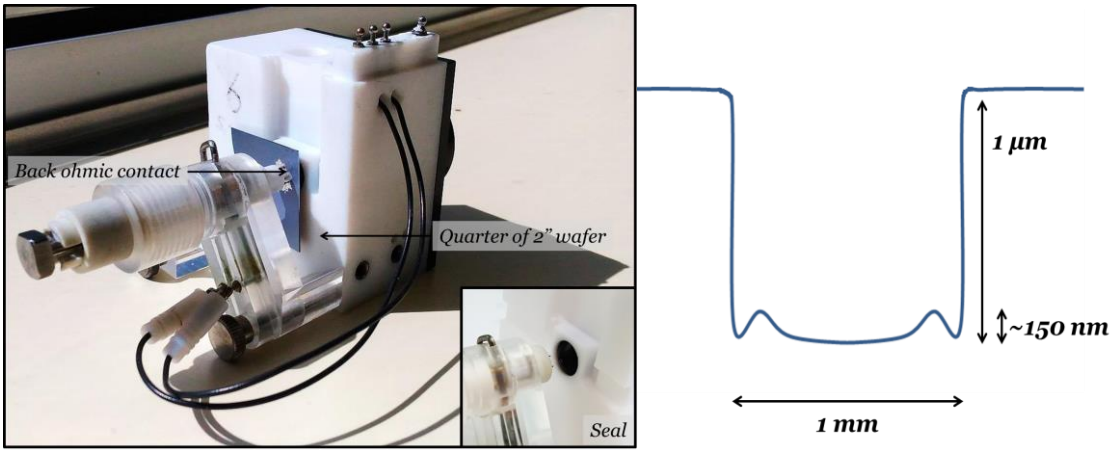



**Figure 3.9 - a) Picture of the electrochemical cell used in ECV. Inset down right: picture of the seal that contacts the wafer surface b) Depth profile of a typical crater after etching.**

However, it is worth mentioning that the deeper we etch and measure, the less reliable becomes the measurement, especially if we want to probe an interface between two layers. Indeed, the etching does not occur in a perfectly uniform way. Typically, after an etching of 1 μm, we find an uncertainty of about 150 nm in the depth of the crater, as shown in Figure 3.9.b. This uncertainty is reduced if the etch rate is drastically decreased, but the measurement would thus require hours. It is thus important, first to control manually all the etching parameters, and second, to be very critical when it comes to interpreting the data from deep layers, especially deep interfaces.

Thus, ECV is a powerful technique to determine the doping levels in a semi-conductor. We use it not only to calibrate a single layer, but also to probe the doping levels in full p-n devices (tunnel junctions). Note that, in this work, we could use this technique only for III-V materials. It is also theoretically possible to perform some ECV measurements on silicon, but it would have required another type of electrolytic cell with another etching solution (based on HF chemicals) that was not available in the III-V Lab.

### III.3.3. Doped GaAs exposed to $H_2$ plasma:

To examine the impact of the hydrogen plasma on doped GaAs, several samples were fabricated on (100) GaAs substrates using Metallorganic Vapor Phase Epitaxy (MOVPE). This technique will be presented in the next chapter. For each sample, first a 500 nm thick intrinsic buffer layer was grown, followed by a 500 nm thick doped layer. We grew GaAs layers doped with Si, Te (n-type), and C (p-type) with various p-doping levels ranging from $1.3\times10^{17}$ to $1\times10^{20}$ $cm^{-3}$. The 5 samples are gathered in Table 3.3.

**Table 3.3 - List of samples grown with their dopants and doping levels**

| **Sample** | **A** | **B** | **C** | **D** | **E** |
|---|---|---|---|---|---|
| **Type** | p | p | p | n | n |
| **Dopant** | Carbon | Carbon | Carbon | Silicon | Tellurium |
| **Doping level ($cm^{-3}$)** | $1\times10^{20}$ | $2\times10^{18}$ | $1.3\times10^{17}$ | $1.2\times10^{19}$ | $2\times10^{19}$ |

Those samples were exposed to very short (30 seconds for samples A, B and C, and 15 s for samples D and E) hydrogen plasmas in our PECVD reactor under the standard conditions of Si epitaxy. To characterize the doping level, ECV measurements were performed before and after hydrogenation. Figure 3.10.a. shows the resulting carrier concentration profiles after $H_2$ plasma exposure for GaAs:C samples. The dashed lines show the nominal doping profile in each sample. Figure 3.10.b) and c) are the ECV profiling before and after plasma exposure for GaAs:Si and GaAs:Te.

On each sample, we notice a strong effect on the doping level at the surface: The doping level has drastically decreased. The doping level in Samples A and B decreases by one order of magnitude at the surface, despite the two orders of magnitude difference in their nominal doping level. For sample A, initially doped at $1\times10^{20}$ $cm^{-3}$, the 30 seconds hydrogen plasma exposure affected about 20 nm of the layer, while for sample B, initially doped at $2\times10^{18}$ $cm^{-3}$, the doping level was reduced over a thicker layer (about 100 nm). The thickness over which dopants are neutralized seems to be inversely dependent on the initial dopant concentration. The neutralization of the dopants is attributed to the fact that atomic hydrogen diffuses extremely fast in the GaAs layer and forms complexes with the dopants (here, carbon, thus forming dopant-H complexes) and thus deactivates it. Actually, the shape of the doping profile and the depth of dopant neutralization are quite similar

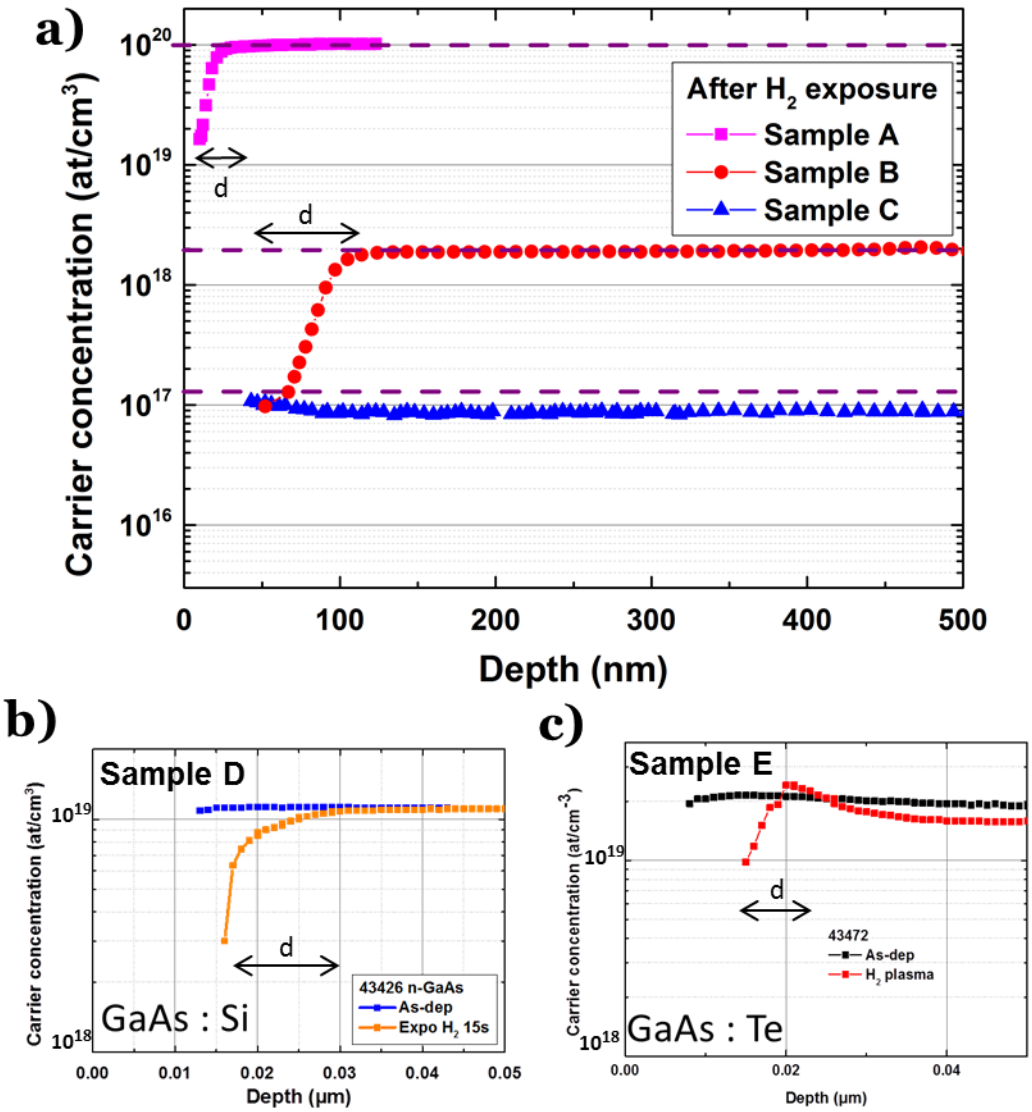



**Figure 3.10 - a) Carrier concentration profiles measured by ECVof three p-GaAs:C samples with different initial doping levels, after hydrogen plasma exposure. Dashed lines show the nominal carrier concentrations of each sample. b)c) Carrier concentration profiles before and after plasma exposure for b) GaAs:Si, c) GaAs:Te**

to what Chevallier *et al.*[147] observed in a n-type GaAs doped with silicon. If we look at Sample B, the passivated depth is higher than that of Sample A that is more doped.

Table 3.4 summarizes the obtained nominal carrier concentration of the layer and the values measured at the surface of the GaAs after plasma exposure, where **N°** is the nominal carrier concentration, $\mathbf{N^{H2}}$ is the carrier concentration at the surface after plasma exposure and **d** is the depth to which the carrier concentration is modified. In the case of sample C, which has the lowest carbon concentration, the decrease in doping level is smaller but happens over the whole 500 nm thick layer.

**Table 3.4 - Doping levels and penetration depth after $H_2$ plasma exposure.**

| | Sample A | Sample B | Sample C | Sample D | Sample E |
|---|---|---|---|---|---|
| ***Dopant*** | C | C | C | Si | Te |
| ***$H_2$ exposure*** | 30 s | 30 s | 15 s | 15 s | 15 s |
| ***N°* (cm$^{-3}$)** | $1\times10^{20}$ | $2\times10^{18}$ | $1.3\times10^{17}$ | $1.2\times10^{19}$ | $2\times10^{19}$ |
| ***$N^{H2}$*(cm$^{-3}$)** | $1.5\times10^{19}$ | $1\times10^{17}$ | $8.5\times10^{16}$ | $3\times10^{18}$ | $9.5\times10^{18}$ |
| ***d* (nm)** | 20 | 100 | 500 | 15 | 10 |

These measurements indicate that the hydrogen plasma that we perform prior to the growth of Si on GaAs affects the doping level of the underlying doped GaAs. This will have to be taken into account in the realization of the final tandem device.

Further experiments were designed to find out whether the electrical activity of acceptors can be restored by heat treatment. We focused on the layers doped with carbon at $1\times10^{20}$ cm$^{-3}$, which correspond to the layers that will be at the top during the process of the Si subcell. Thus, sample A has been annealed for 3 minutes at different temperatures from 250 °C to 400 °C after plasma exposure and ECV measurements were performed after each annealing step. The results of this study are presented in Figure 3.11.a.

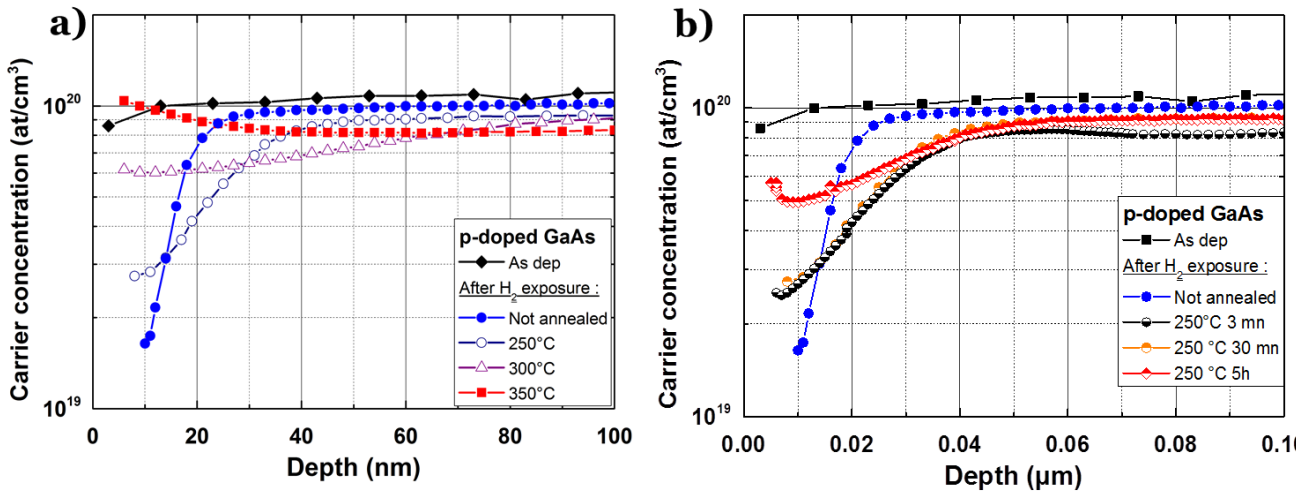



**Figure 3.11 -ECV profiling of GaAs :C before $H_2$ exposure, after $H_2$ exposure and after a) 3-minutes annealing at various temperatures, b) annealing at 250 °C for various durations**

Full symbols represent the active carrier concentration of the sample before (black squares) and after (blue circles) hydrogen plasma treatment. The samples have been annealed at various temperatures for 3 minutes. We notice that the higher the annealing temperature is, the better the doping level can be recovered. After a 250 °C annealing, a slight recovery of the carrier concentration is observed in the first ten nanometers, but the dopant passivation extends over a deeper region. This suggests that hydrogen has migrated from carbon atoms located close to the surface to deeper carbon atoms into the bulk. Annealing at 300 °C shows a better recovery of the doping level at the surface, which reaches $6\times10^{19}$ cm$^{-3}$. After a 350 °C annealing, the doping level at the surface is almost fully restored. The same study have been performed on sample B (not shown here), and a complete recovery of carrier concentration was also obtained after heating at 350 °C.

Thus, we have shown that exposing doped GaAs to a $H_2$ plasma in our process conditions deactivates the dopants of this layer, and we showed that an annealing at 350 °C helps recovering from this effect.

However, in our tandem integration, we have shown in Chapter 2 that annealing our epi-Si at temperatures higher than 300 °C for 3 minutes degrades the quality of the epitaxial layer, and can even create blistering at the interface between the epitaxial Si layer and the underlying one, which induces recombination Thus, we must avoid at best annealing our tandem device at temperatures higher than 250 °C. Figure 3.11.b. shows the same sample that have been annealed at 250 °C for longer annealing time. 30 minutes of annealing does not change the doping profile as compared to a 3 mn RTA at 250°C. However, by annealing for a much longer time (5 hours), the doped GaAs pass from a doping level at the surface increase from of $1.5\times10^{19}$ to $5\times10^{19}$ $cm^{-3}$. Actually, as this long annealing time roughly corresponds to the annealing that will be necessary for the bonding of the tandem solar cell, as it will be presented in Chapter V.2.2. (p.134).

# III. 4. Conclusion

In this chapter dedicated to the PECVD / GaAs integration, we first studied the heteroepitaxial growth by PECVD of Si on GaAs. By following the structural properties of thin Si layers, we managed to show that the grown Si is tetragonal. Its out-of-plane lattice parameter ($a_\perp$) is higher than that of bulk Si, and this increase is linked with the hydrogen content in the layer. Also, its in-plane lattice parameter ($a_{//}$) is smaller than that of bulk Si. We attribute this to the strain induced by the thermal mismatch between the GaAs substrate and the grown Si. But this behavior can be explained only if the surface temperature of the substrate is locally much higher than the nominal temperature of 175 °C. This observation could actually help understanding the growth mechanisms of low-temperature PECVD, by suggesting that there is a local heating at the growth surface. This route is worth exploring, by performing systematic experiments on various substrates (Ge, InP) to get on better insight on the behavior of the $a_{//}$ of our epitaxial layers.

We found that hydrogen also plays a role in the underlying GaAs layer. We found that an short exposure to a $H_2$ plasma decreases by almost one order of magnitude the active doping level of GaAs, whatever is the dopant atom (C, Te, Si). This behavior can be recovered after short annealing at 350°C. It will have to be taken into account in the realization of the final tandem device.

Chapter 4

# Tunnel Junctions

## Content

The realization of the IMPETUS tandem solar cell in a 2-terminal monolithic approach requires the development of the electrical connection between the two subcells: the tunnel junction (TJ). Before incorporating it into the final device, it must be characterized as a separated device, in order to assess its performances and its impact on the tandem device. An important part of this PhD was dedicated to the study of these structures. In this chapter, we will first introduce the principle of these highly doped p-n- junctions which allow the carrier flows to from one subcell to the other by tunnel effect, and discuss our requirements. Then, we present the facilities used for fabricating III-V compounds: MOVPE, and the clean room facilities. We afterwards realize III-V tunnel junctions grown by MOVPE, p and n doped with C and Si respectively, and show that the TJ performances are limited by the low n-doping of GaAs. We will then present the use and development of another dopant element: tellurium, in order to reach higher n-doping levels into GaAs and GaInP, and thus to enhance the TJ performances. The growth conditions, using the tellurium precursor Diisopropyl Telluride (DIPTe) will be studied, and the electrical measurements of the resulting TJ will be presented. Finally, the path towards hybrid tunnel junctions will be explored.

# IV.1. Introduction

## IV.1.1. Tunnel junctions: principle

In a 2-terminal monolithic approach of tandem solar cells, the two sub-cells are connected by means of tunnel junctions (TJ). Connecting directly two solar cells together would form a reverse pn junction in between and thus create a huge voltage drop. Therefore, to let the carriers flow from one cell to the other, a highly doped pn junction is added, enabling carriers to flow by tunneling effect. First tunnel diodes have been reported in 1957 by Leo Esaki[150]. He received in 1973 the Nobel Prize in Physics for discovering the electron tunneling effect used in these diodes. For such degenerated semi-conductors, the conduction band electron states on the n-side are aligned with valence band hole states on the p-side. Figure 4.1.*h*. shows the typical I-V characteristics of a tunnel junction**.** Figure 4.1.*a-g* details the evolution of the band diagram as a function of the applied voltage. Under reverse bias (b), filled states on the p-side are aligned with empty states on the n-side and electrons tunnel from n side to p side. At 0 V (a), the states are under thermodynamic equilibrium. In low bias region (c), the ***J-V*** curve presents a resistor like shape due to band-to-band tunneling: electrons tunnel through the very narrow p–n junction barrier. Electron states in the conduction band on the n-side are aligned with empty valence band hole states on the p-side of the p-n junction. This behavior is limited by a maximum current density $J_{peak}$ (d) reached for a given voltage $V_{peak}$**.** The low bias region is the most important one in multi-junction solar cells, since the TJ operates in this part of the ***J-V*** characteristics.

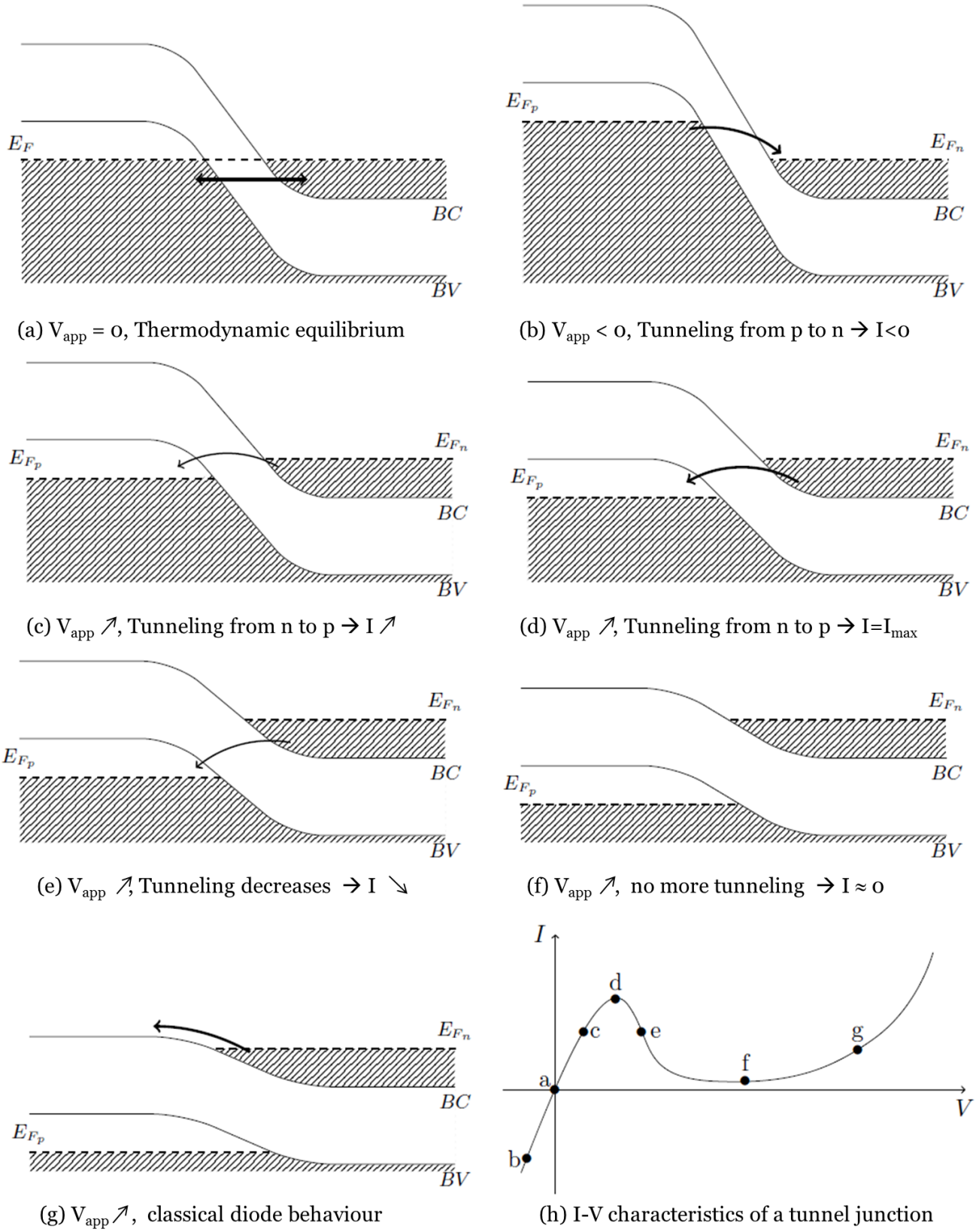



**Figure 4.1 - Evolution of the band diagram of a tunnel junctions as a function of the applied Voltage (a to g), and corresponding I-V characteristics (h)**

The value of the voltage at J = $J_{sc}$ will determine the voltage drop during solar cell operation. Consequently, the is lower resistivity, the better is the TJ for MJSC. As voltage increases further, these states become increasingly misaligned (e) leading to a current drop. In this region, the resistance is negative because less carriers can tunnel with increasing voltage. At higher voltage we reach the valley (f), and the diode begins to operate as a normal diode (g), where electrons travel by conduction across the p–n junction, and no longer by tunneling through the p–n junction barrier.

Tunnel junctions are usually characterized by two figures of merit pictured in Figure 4.2: the $J_{peak}$, and the resistivity at low bias R. $J_{peak}$ should be as high as possible, at least higher than the $J_{sc}$ of the considered operating solar cell. For example, the $J_{sc}$ of a tandem solar cell is expected to be around 21 mA/cm². Thus, the $J_{peak}$ of the tunnel junction needs to be above 21 mA/cm² if it operates under 1 sun illumination. For solar cells working under concentration, this $J_{peak}$ must be higher: if we consider a tandem solar cell working under 1000 suns, the $J_{peak}$ minimum value would be 21 A/cm². The resistance at low bias has to be as low as possible, so as to lower $V_{(Jpeak)}$, that will be the voltage drop in the solar cell.

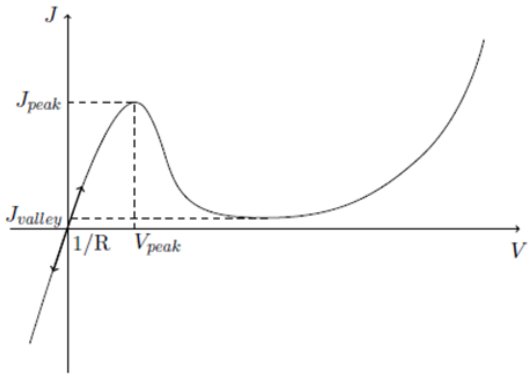



**Figure 4.2- Typical J-V curve of a tunnel junction, and main parameters**

In standard band-to-band tunneling, $J_{peak}$ follows the subsequent behavior:

$$J_{peak} \propto \exp\left(-\frac{Eg^{\frac{3}{2}}}{\sqrt{Neff}}\right) \text{ with } N_{eff} = \frac{N_{n++} \cdot N_{p++}}{N_{n++} + N_{p++}} \qquad \text{Eq 4.1}$$

$E_g$ is the bandgap of the semi-conductor that constitutes the TJ. We see that the higher the doping level in both sides of the tunnel junction, the higher the $N_{eff}$ and consequently the higher the $J_{peak}$. However, both sides must be more or less doped the same way. There is no need to highly increase one side if the other one remains with a low value. It will be thus important to dope both n and p sides as high as possible. Literature[151,152] also mentions another mechanism that could be responsible for $J_{peak}$ enhancement in TJ: trap-assisted tunneling (TAT). While growing semiconductor devices, crystalline defects can be involuntarily added, thus creating deep levels inside the bandgap. These trap levels can strongly modify the characteristics of the device.

From an optical point of view, the TJ should be as transparent as possible, not to absorb too much photons that are aimed to be absorbed by the underlying sub-cell. Thus, increasing the bandgap is necessary. However, as seen in Eq 2.1, $J_{peak}$ exponentially decreases with $E_g$. Consequently, a trade-off between the optical properties and the $J_{peak}$ will have to be found.

## IV.1.2. Literature overview

Best tunnel junctions in III-V materials for photovoltaic applications[153] show a $J_{peak}$ record of 10 kA/cm², as reported in Table 4.1. This result has been obtained for an AlGaAs/GaAs TJ where AlGaAs was p-doped with carbon and GaAs n-doped with tellurium. The voltage drop for a current density equivalent to the operation of the multi-junction solar cell up to 10 000 suns is below 5 mV. This so high $J_{peak}$ cannot be explained only by band-to-band tunneling. The authors suspect the effect of trap-assisted tunneling. This paper also reveals GaAs/GaAs TJ with $J_{peak}$ up to 8600 A/cm². Wheeldon *et al.*[154] published an interesting comparison study of different III-V TJs: GaAs/GaAs, AlGaAs/GaAs, AlGaAs/GaInP. Figure 4.3. shows simulation results along with their experimental data of the peak tunneling current as a function of the effective doping level for 4 different TJ configurations. It shows that AlGaAs/GaAs requires the least effective doping level to reach a $J_{peak}$ suitable for 2000 suns, being thus the easiest tunnel junction to fabricate. AlGaAs/GaInP TJ is the most transparent but requires an effective doping level above $2\times10^{19}$ cm$^{-3}$. Table 4.1 summarizes a few tunnel junctions reported in literature[152–158]. The material of each side of the tunnel junction is reported, as well as its doping level (when mentioned in the article) and the dopant used. We can notice that the dopant used in best TJ are carbon and Te.

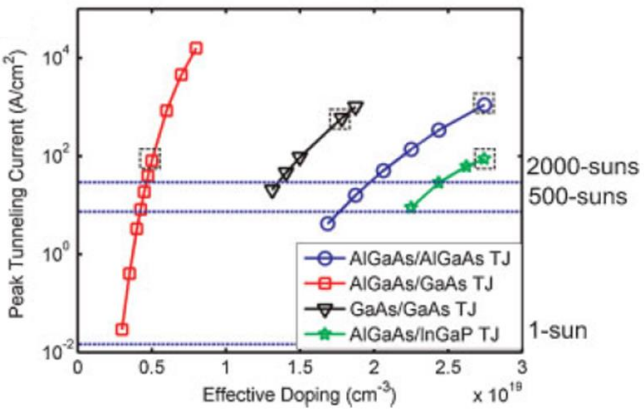



**Figure 4.3- Peak tunnelling current as a function of the effective doping level for various TJ material combinations. (Simulation and experimental, from Wheeldon *et al.* [158])**

**Table 4.1 - Performances of III-V tunnel junctions from literature, its doping level and its $J_{peak}$.( [152–158] )**

| Reference | Year | p material | n material | p- dopant | p -doping level (cm$^{-3}$) | n- dopant | n-doping level (cm$^{-3}$) | $J_{peak}$ (A/cm²) |
|---|---|---|---|---|---|---|---|---|
| Garcia | 2012 | AlGaAs | GaAs | C | 1x10$^{20}$ | Te | 3x10$^{19}$ | 10100 |
| Garcia | 2012 | GaAs | GaAs | C | 7x10$^{19}$ | Te | 3x10$^{19}$ | 8630 |
| Barrigon | 2014 | AlGaAs | GaInP | C | 6 x10$^{19}$ | Te | 1.1 x10$^{19}$ | 996 |
| Wheeldon | 2014 | AlGaAs | GaInP | C | 2,7x10$^{19}$ (eff) | Te | effective | 907 |
| Wheeldon | 2014 | AlGaAs | AlGaAs | C | 2,7x10$^{19}$ (eff) | Te | effective | 80 |
| Hermle | 2008 | GaAs | GaAs | C | 3,6.10$^{19}$ | Te | 1x10$^{19}$ | 25 |
| Zheng | 2015 | GaAs | GaAs | Mg | 1x10$^{19}$ | Te | 1,5x10$^{19}$ | 21 |
| Louarn | 2016 | GaAs | GaAs | C | 3x10$^{19}$ | Si | 9x10$^{18}$ | 10 |
| Zahraman | 1993 | GaAs | GaAs | C | 4 x10$^{19}$ | Te | 1x10$^{19}$ | 6 |

Meanwhile, Si/Si tunnel junctions have been widely studied for microelectronic devices. There are possible applications in high frequency and fast digital devices. In logic circuits, this structure with a negative differential resistance helps reducing the circuit complexity and/or increasing the speed and reduce the power consumption. MBE grown Si exhibits very high doping levels[159,160], together with high $J_{peak}$ up to 46kA/cm². SiGe tunnel junctions grown by MBE[161] showed $J_{peak}$ up to 8kA/cm². The literature about tunnel junctions applied to the photovoltaic industry is scarcer, but has recently found some interests. TJ formed by diffusion showed $J_{peak}$ of 100/cm² in 2003[162]. Recently, Fave *et al.*[163] realized some Si/Si tunnel junctions for photovoltaics applications. The n part reached 1.5 $10^{20}$ $cm^{-3}$ and the concentration of phosphorus is about $2\times10^{20}$ $cm^{-3}$. Those doping levels are much higher than the achievable doping levels in III-V materials. Their tunnel diodes exhibited very good $J_{sc}$ of 270 A/cm², opening the path to realizing tunnel junctions for III-V/Si tandem solar cells as well as any other type of tandem solar cell with Si (perovskite, CIGS etc…)

In this chapter, we focus on the realization of III-V tunnel junctions, aiming at catching up the state-of-the-art in our laboratory. However, we keep in mind the option of growing Si/Si TJ by low temperature PECVD. Moreover, the possibility of growing hybrid Si/III-V tunnel junction will also be discussed.

# IV.2. MOVPE and clean room facilities

While epitaxy has already been introduced and strongly discussed in the previous chapters using an uncommon growth technique, this part deals with a more standard technique, used to grow high quality monocrystalline materials: MOVPE (metalorganic vapor phase epitaxy). This is one of the dominant techniques for production of semiconductor. We used it during this PhD to grow III-V materials lattice-matched on GaAs substrates: mainly GaAs; AlGaAs; GaInP and AlInP. We present here an overview of this growth technique, that is not only used to grow the tunnel junctions presented in this chapter, but also the III-V solar cells presented in next chapter. We also present the main available clean room facilities that will be used in both chapters.

## IV.2.1. Metalorganic vapor phase epitaxy

MOVPE, or metalorganic vapor phase epitaxy is sometime called MOCVD (metalorganic chemical vapor deposition). MOCVD is the general term describing the growth process, that does not imply whether the resultant layer is single crystalline, polycrystalline or amorphous. In this work, we will only present the growth of crystalline material, thus referring to MOVPE. This technique has been developed in the 60's by Manasevit and Simpson[164], and is now widely used in semiconductor industry to grow III-V materials with abrupt interfaces and high purity materials, to produce GaAs and InP with purity equaling or exceeding all other techniques[165]. This technique uses precursor gazes that are diluted in a carrier gas: $H_2$. Unlike MBE (molecular beam epitaxy), the pressure in the MOVPE reactor is relatively high (a few hundreds of milibars), which allows vapor phase diffusion. During this PhD thesis, all III-V layers were grown using an horizontal AIXTRON AIX200/4; as shown in Figure 4.4. In this system, the group III atoms (Ga, Al, and In) are provided by metalorganic precursors: trimethylgallium ($Ga(CH3)_3$, TMGa), and trimethylaluminium ($Al(CH_3)_3$, TMAl), and trimethylindium ($In(CH_3)_3$, TMIn), respectively. Group V atoms (As and P) come from hydride precursors: arsine ($AsH_3$) and phosphine ($PH_3$) respectively.

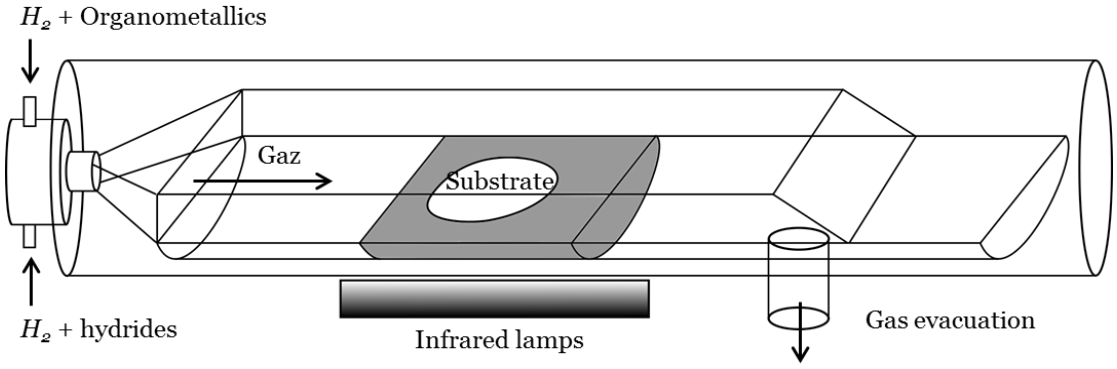



**Figure 4.4 - Principle of the AIX200 reactor**

The metalorganic precursors are carried in $H_2$ and sent to the reactor together with the hydride precursors. In the reactor, a rotating substrate is heated at temperatures around 600-700 °C by infra-red lamps, as seen in Figure 4.5. The rotation ensures a good uniformity up to 4 inches wafers. The heat breaks the precursors, and the desired atoms are deposited on the wafer. The exhaust gas and particles are then pumped and purified outside the reactor. By carefully varying the precursor flow rates, the properties and composition of the crystal can be accurately chosen, in a reproducible manner.

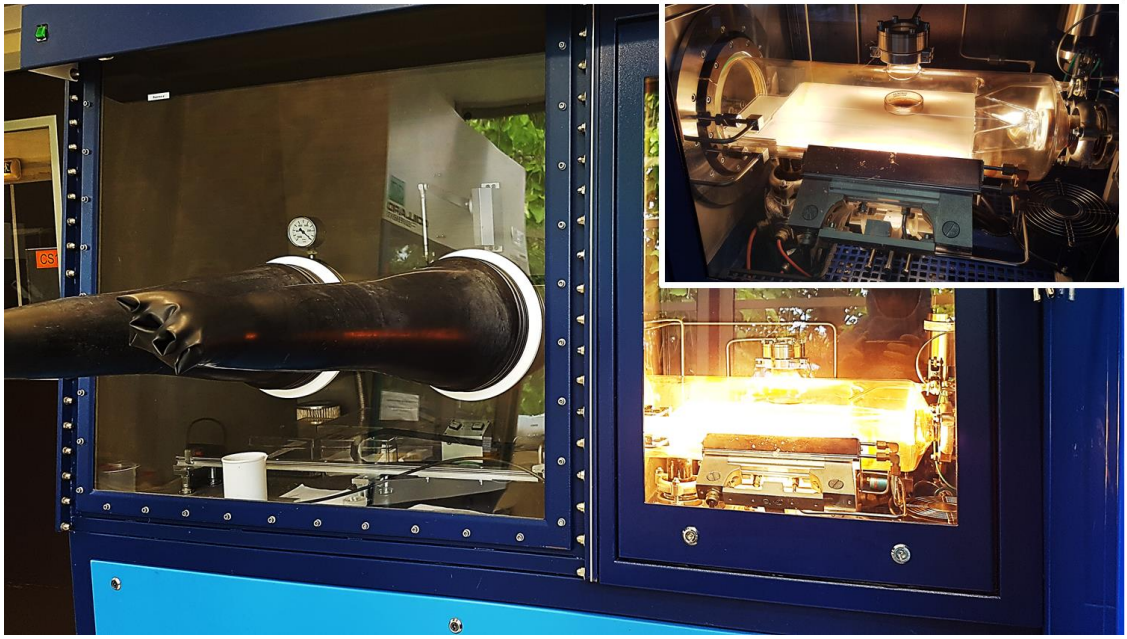


**Figure 4.5 - MOVPE reactor with its glovebox while heating. Inset up right: reactor during a process**

Other precursors are used to dope the III-V materials. In this work, for p-doping we use Zn (from DEZn) for moderated doping level (up to a few $10^{18}$ $cm^{-3}$), and C (from $CBr_4$) to dope above $1\times10^{19}cm^{-3}$. To n-doped our materials, we use S (from $H_2S$) for moderated doping level, Si (from $Si_2H_6$) to reach higher doping levels. To achieve n doping levels higher than $1.2\times10^{19}$ $cm^{-3}$, we installed a new precursor in our reactor: DiIsopropyl Telluride (DIPTe). A picture of the reactor used during this PhD at the III-V lab is presented in Figure 4.5. On the left, we see the glovebox

under $N_2$, in which the samples are prepared. On the right, we see the horizontal reactor heated by the infra-red lamps. The up-right inset shows a top view of the reactor.

## IV.2.2. Clean room microfabrication

III-V lab has a strong know-how in processing III-V materials for diverse applications. We do here a quick introduction of the main available techniques used in microfabrication. Those techniques will be adapted to our requirements, not only for the fabrication of tunnel junction test devices, but also in the fabrication of single AlGaAs solar cells and the final tandem device presented in chapter 5.

Photolithography

Photolithography is a process used in microfabrication to pattern parts of a film or a substrate, and to choose some areas that should be selectively etched, metallized, or implanted. It has a resolution of about 200 nm and an alignment precision of 500 nm. The principle is to coat a wafer by spin-coating with a light-sensitive chemical photoresist, commonly called "resist". Spin-coating consists of dispensing onto the wafer a viscous solution of resist, and to spin rapidly the wafer (typically 5000 rpm) for a certain time (30 to 50 seconds in our case). The spin-coated layer is uniform, with a controlled thickness (around 3 µm usually). The wafer with the resist is then exposed to a light through a photolithographic mask, on which the desired patterns have been previously printed. The exposure to light causes a chemical change in the resist, which allows some of the photoresist to be removed by a solution called "developer". There are two types of resists: Positive photoresist becomes soluble in the developer when exposed; while in negative photoresist, only unexposed regions are soluble in the developer. Once a photoresist is no longer needed on the wafer it can be removed either by dipping the wafer into acetone, or by using a plasma containing oxygen. Acetone is also used to perform a lift-off, a process that will be presented below.

Lift-off

The lift-off process is a method to create patterning on top of a wafer using a sacrificial material. In our case, we mainly need it to create metal patterning. Figure 4.6 details the lift-off of a metal: first, we deposit a photo resist and open it by photolithography as described above. Then, the targeted material (metal) is deposited on the whole surface of the wafer. Thus, the layer covers the remaining

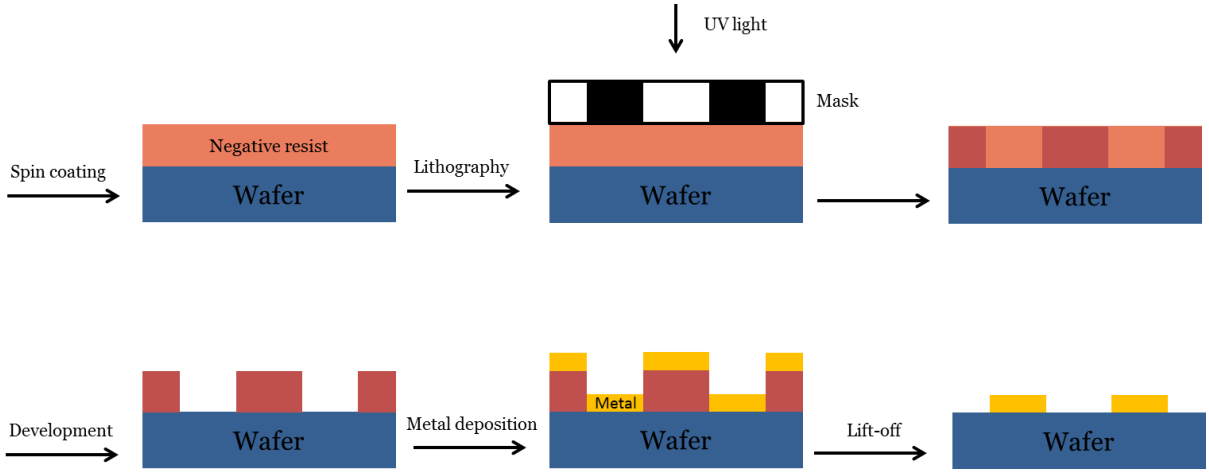



**Figure 4.6 - Detailed process of a metal pattern by lift-off technique**

resist as well as the semi-conductor where the resist was removed. By dipping the wafer into acetone, the resist is removed, eliminating the above metal simultaneously. Only the metal that was not above the resist stays on the wafer.

Metal deposition

During the microfabrication of a III-V device, metal deposition is required to form ohmic contacts. There are two deposition techniques for metals: evaporation and sputtering. To form ohmic contact on GaAs compounds, it is important to have a highly doped III-V layer, (so-called "cap layer"). For the p-type GaAs, we deposit a Pt/Au (150 nm of Pt, 250 nm of Au) after a short etch of the III-V surface by an Ar plasma. It removes the oxide, and roughens the surface, helping to get a better adhesion between the metal and the semi-conductor. The n-type GaAs ohmic contact is less easy to achieve, and requires a rapid thermal annealing at 400 °C to allow chemical intermixing and interdiffusion between the metal and the GaAs. The best ohmic contact for n-type is AuGe/Ni/Au[166], that we deposit by evaporation. However, for practical reasons due to the availability of the evaporator during my thesis, another contact is often used for the n-type part when it is the back ohmic contact: Ti/Pt/Au, deposited by sputtering. The good resistivity of AuGe/Ni/Au is essential when it comes to front contacts with small grid patterns, but is less crucial when it comes to a full wafer back contact.

Etching

Process flows can require different steps of etching: we can need to etch material in some specific zones: the III-V material, a dielectric, or even a metal. There are several ways of etching such materials: the chemical way (wet etch) and the plasma way (dry etch). Dry etching uses plasmas, leading to physical and/or chemical phenomena. It is only physical when some ions of the plasma directly bombard the surface of the wafer and removes material in an unprotected zone. This is the case of the Ar bombardment used before metallization to etch the oxide. This technique can etch any type of material: semiconductors, dielectrics, and metals. With high ion energies it is possible to etch thick layers of III-V or metals by ion beam etching (IBE)[167]. However this technique let damaged surfaces and sidewalls, and is not selective. The chemical dry etch can be done by RIE (reactive ion etching). It uses precursors that are chemically reactive to the material we want to etch. For example, to remove $SiO_2$ materials, plasma of $CHF_4$ is used. To etch deep III-V materials, a specific type of RIE will be used inductively coupled plasma (ICP) RIE. With ICP, very high plasma densities can be achieved, leading to etch profile that tends to be more isotropic. The wet etch is a technique in which we dip the wafer into a chemical mixture containing reactants that will etch the targeted layer. Wet etchants are usually isotropic, which leads to large bias when etching thick films. Depending on the chemistry chosen, the wet etching can be either selective, either non selective.

We just presented the standard techniques available in the III-V Labs clean room. Those techniques will be used in the realization of the III-V tunnel junctions as well as the III-V solar cells in next chapters.

## IV.3.1. Tunnel junctions: first studies

This part presents the first studies performed in the III-V lab to grow and fabricate operating tunnel junctions. We first calibrated the doping levels of the materials by using the dopants available in our

MOVPE reactor: carbon for the p-doping and silicon for the n-doping. Then, we will present the first III-V TJ grown and processed, along with its electrical characteristics.

### IV.3.1. GaAs/GaAs first tunnel junctions

We first calibrated the doping levels of GaAs by MOVPE with the available precursors. We used $CBr_4$ to p-dope with C, and $Si_2H_6$ to n-dope with Si. Both dopants are amphoteric, which means they can a priori occupy group III or group V sites. With carbon we could reach p-type doping levels up to $1\times10^{20}$ cm$^{-3}$, but with Si, we only reached a maximum n-type doping of 1.2 $10^{19}$ cm$^{-3}$.

Tunnel junctions were grown on (100) GaAs wafers. The typical structure of the TJs is presented in fig 6.b. It consists of a n doped GaAs buffer layer, followed by a heavily doped n++GaAs layer of 30 nm, with a nominal doping level of $1.2\times10^{19}$ cm$^{-3}$, followed by 30 nm of p++ GaAs. The two samples presented here differ in the p doping level: 43227 is doped at $3\times10^{19}$ cm$^{-3}$, and 43449 is doped at $1\times10^{20}$ cm$^{-3}$. Such low thicknesses have been chosen to ensure a low absorption in the tandem device. A spacer was then grown on top of the TJ, followed by a 50 nm cap layer to unsure good

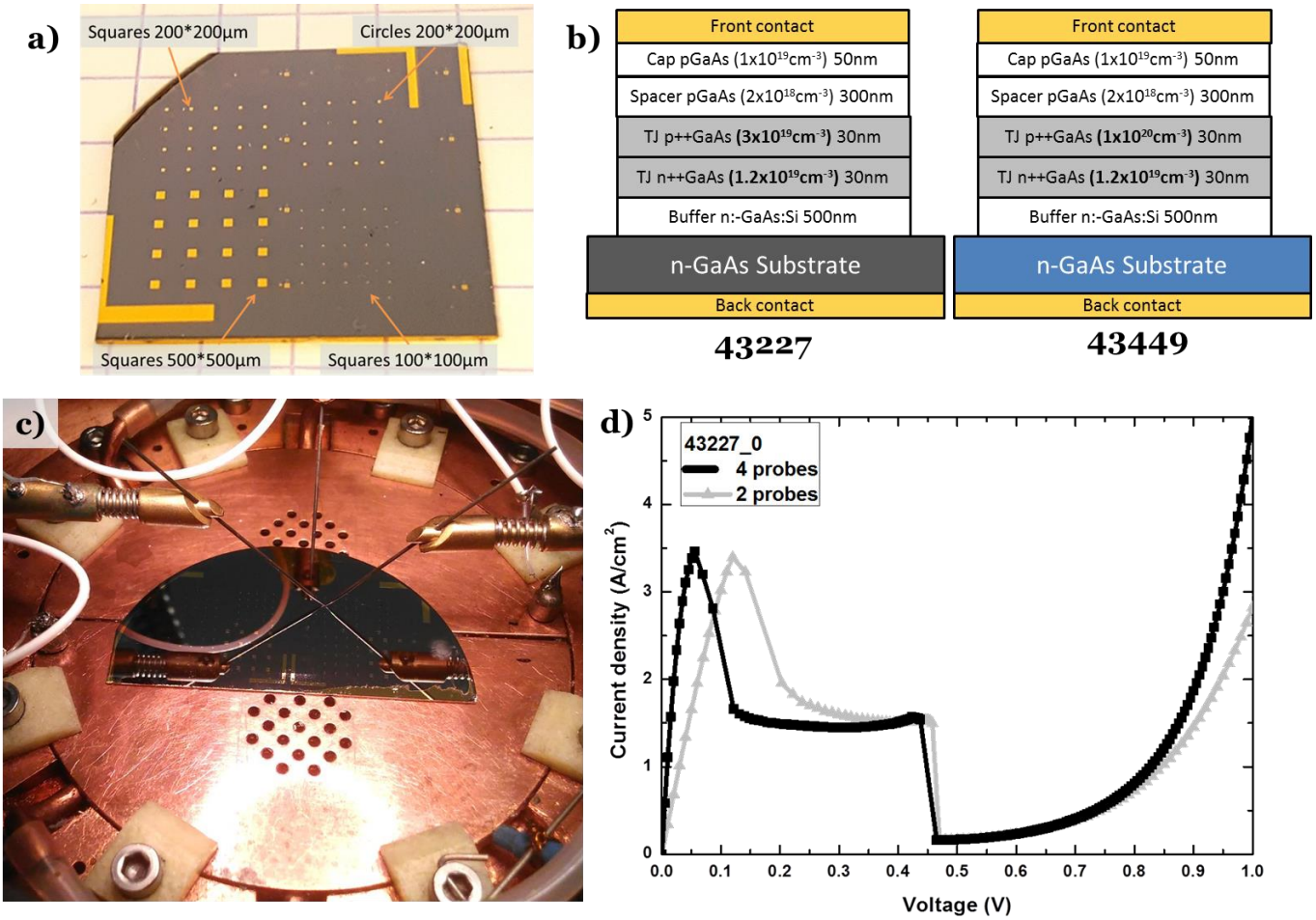



**Figure 4.7- a) Picture of a tunnel junction after processing b) material and device of the two considered tunnel junctions, c) picture of the 4 probe characterization tool, d) comparison between 2-probe and 4-probe measurement**

ohmic contact.

The process flow is then performed as followed: with a lithographic mask we define several diodes with different sizes, with Pt/Au on the p-doped front side. Figure 4.7.a. shows a picture of a quarter of 2 inch. wafer after processing. We pattern some diodes with various sizes and etch chemically the mesas between the diodes. As shown in Figure 4.7.a., it presents diodes ranging from 500*500 µm² to 100*100 µm². Finally, the back contact in AuGe/Ni/Au is deposited, and a rapid thermal annealing at 400°C is performed to ensure a ohmic back contact. Those structures were measured at room temperature in a four probes I-V bench, with a Keithley 2450 sourcemeter limited to 1A. A picture of the measurement set up is shown in Figure 4.7.c. This setup was used at the GeePs laboratory. Two front probes are placed on top of the diode, and the back contact is taken with two conductive plates that are electrically separated. A 2-probes measurement would have induced higher resistances, thus distorting the R measurement. Figure 4.7.d. shows the measurements of the same TJ with 2 probes and 4 probes. The peak position is shifted to higher voltage, and the resistance is higher in case of a 2-probe measurement. It is thus important to get rid of the probe specific resistance.

Figure 4.8 displays the room temperature current density versus applied voltage characteristics (J–V) of the 2 above mentioned tunnel junctions. Both curves exhibit the expected ***J-V*** curve shape with a peak current at low bias, followed by a negative region, and a classical diode characteristic. The peak tunneling current measured is around 3 A/cm². The resistance at low bias is slightly lower for the sample 43227 (Blue triangles) than 43449 (Black squares) whereas its p-doping level is higher. We would have expected a better $J_{peak}$ because its effective doping level $n_{eff}$ is equal to $1.07\times10^{19}$ cm$^{-3}$ while the other sample has $n_{eff}$ =$8.57\times10^{18}$ cm$^{-3}$. Anyway, the difference in resistivity and $J_{peak}$ remains very small and not that relevant concerning the impact of the increasing doping level in the p part of the tunnel junction. 4 A/cm² is lower than literature, but still good enough to work under 1 sun illumination and up to 190 suns. The resistivity measured is of $1.04\times10^{-2}$ Ω/cm². At 1 sun, the voltage drop would be of 0.2 mV.

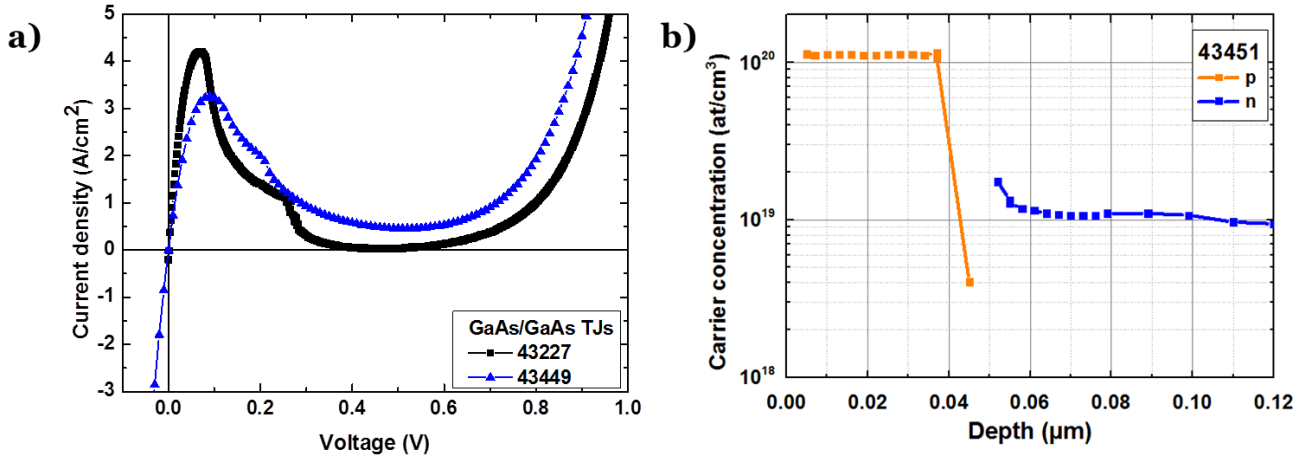



**Figure 4.8 - a) J-V curves of GaAs/GaAs tunnel junctions, b) ECV measurement of a p-GaAs/n-GaAs structure**

An ECV measurement of a structure identical to sample 43449 is shown on Figure 4.8.b. The spacer and cap layer have not been grown on this sample so as to limit the problems caused by a non-uniform etching. In this way, we have a better accuracy in the doping measurement. This measurement confirms the high p-doping level above $1\times10^{20}$ $cm^{-3}$ and a n-doping level slightly above $1\times10^{19}$ $cm^{-3}$.

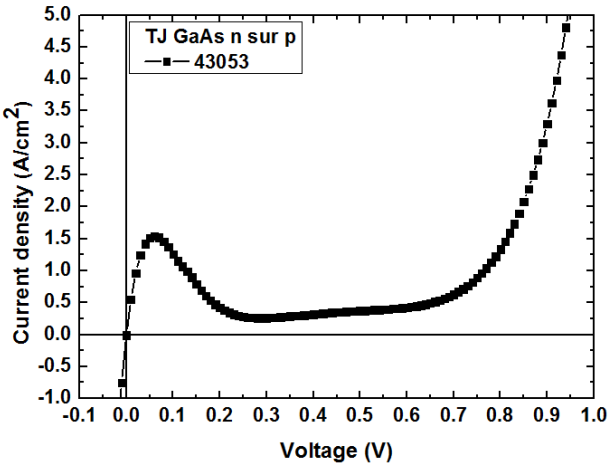



**Figure 4.9 - J-V characteristics of n on p GaAs tunnel junction**

In the meantime, we grew the reverse tunnel junction: an n on p tunnel diode. As presented in Chapter I, our device is designed with a n-doped base, thus leading to the growth of p on n growth of tunnel junction, which exhibits the tunneling properties presented above. However, we want to give the path to select the other polarity, and thus verify if the reverse polarity (n on p) also works. The reverse tunnel junction should, theoretically, exhibit the same characteristics, but the order of deposition in the MOVPE could lead to some variations, such as a possible diffusion of dopants. We thus grew and processed an n on p tunnel junction. The process flow was carried out the same way, outside from the metals that were interchanged: we deposited AuGe/Ni/Au on the n-part of the junction, which is the front side this time, and Pt/Au for the p-contact, at the back of the p-doped wafer. The resulting ***J-V*** curve is plot on Figure 4.9. The $J_{peak}$ is a bit lower than the p on n tunnel diode, but still in the same order of magnitude.

## IV.3.2. Transparent tunnel junctions

Growing tunnel junctions with wider bandgap materials would ensure a better tansparency, thus enabling more photons to reach the bottom cell. Therefore, we tried to perform AlGaAs/GaAs as well as AlGaAs/GaInP tunnel junctions, with the same process flow. AlGaAs can easily be grown with a p-type doping of $1x10^{20}cm^{-3}$ with carbon. However, lattice-matched GaInP is actually hard to dope with the conventional dopants such as S or Si [168,169]. This TJ was grown with GaInP doped with S, whose highest doping level was of $9\times10^{18}$ $cm^{-3}$. The structures and ***J-V*** curves of these tunnel junctions are shown in Figure 4.10. AlGaAs/GaAs exhibits a slightly higher $J_{peak}$ than the previous GaAs/GaAs one. This confirms the predictions of Figure 4.3[154], but the $J_{peak}$ only reaches 7 $mA/cm^2$, which is still very low compared to the values reported in literature (see Table 4.1). For the AlGaAs/GaInP tunnel junction, we actually see a standard diode characteristic. No tunneling is achieved. Integrating this "tunnel" junction into a tandem device under 1 sun would induce a loss in $V_{oc}$ above 50 mV. The reason for this behavior could come from the fact that GaInP is not doped enough. SIMS analysis was performed on this sample in order to have a better insight on the dopants. Figure 4.11 shows the atom concentration of S (green) and C (red). The matricial elements Ga (black), Al (blue) and In (red) are plotted to identify the AlGaAs and GaInP layers, and have an idea of their thickness. By comparing the peak in indium that corresponds to the GaInP layer and the peak in sulfur, we can easily notice, first that there is a very high incorporation of S in the layer (almost $10^{22}$ atoms), and second, that it seems to have diffused, not only in the bulk, but also in the upper AlGaAs layer. In addition to the fact that the active n doping level in GaInP is low, S diffusion

may have induced a compensation of active p dopant in the AlGaAs layer. Consequently, we think that the n-dopants available in our lab (S, Si) are not adapted for GaInP growth for tunnel junction applications. To tackle this problem, the use of another dopant element must be investigated in order to achieve high n-doping levels.

We have shown that we are able to grow GaAs/GaAs and AlGaAs/GaAs tunnel junctions with $J_{peak}$s up to 7 A/cm², in both p on n and n on p polarities. However, we could not produce good AlGaAs/GaInP junctions that exhibit standard diode behavior. Even if the performances of the working TJ are suitable for 1 sun application, we might want to improve these devices, for possible use under concentration, and to have transparent AlGaAs/GaInP TJs. Another motivation for improving these devices is the possible effect of the subsequent PECVD growth of Si on this tunnel junction. Also, as it was observed in Chapter III.3.3. Doped GaAs exposed to $H_2$ plasma:, the TJ performances may be lowered by the hydrogen plasma that passivates the dopant atoms. Literature results show that there is room for improvement, as best reported TJ up to now exhibits a $J_{peak}$ above 10.000 A/cm². To catch-up state-of-the-art TJ, we propose to explore the use of Te doping. This dopant was not available in the lab at the beginning of my PhD. We installed a new source on the MOVPE system for that purpose. The two next parts of this chapter deal with the calibration of the new precursor, the interpretations of the results to understand growth mechanisms, and the electrical results on newly grown tunnel junctions using Te.

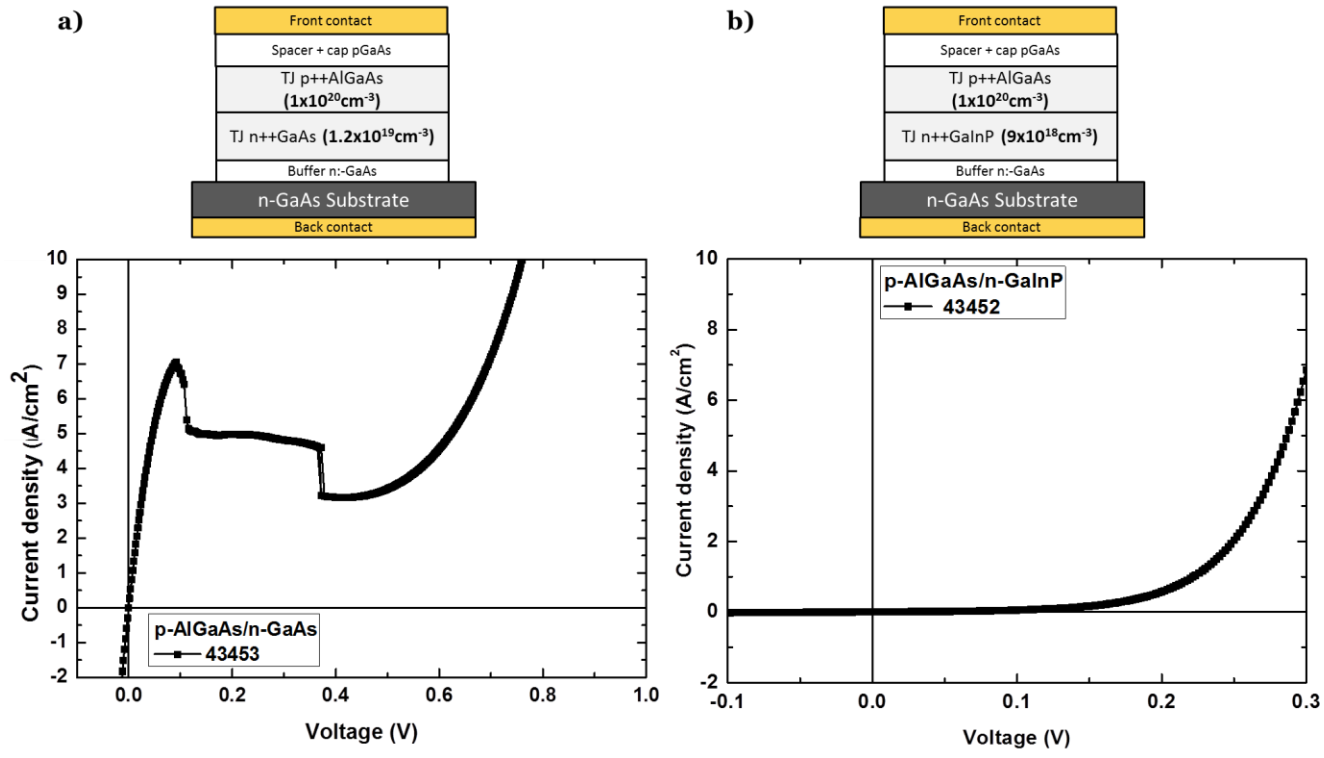



**Figure 4.10 - Structure and J-V characteristics of a) AlGaAs/GaAs tunnel junction and b) AlGaAs/GaInP**

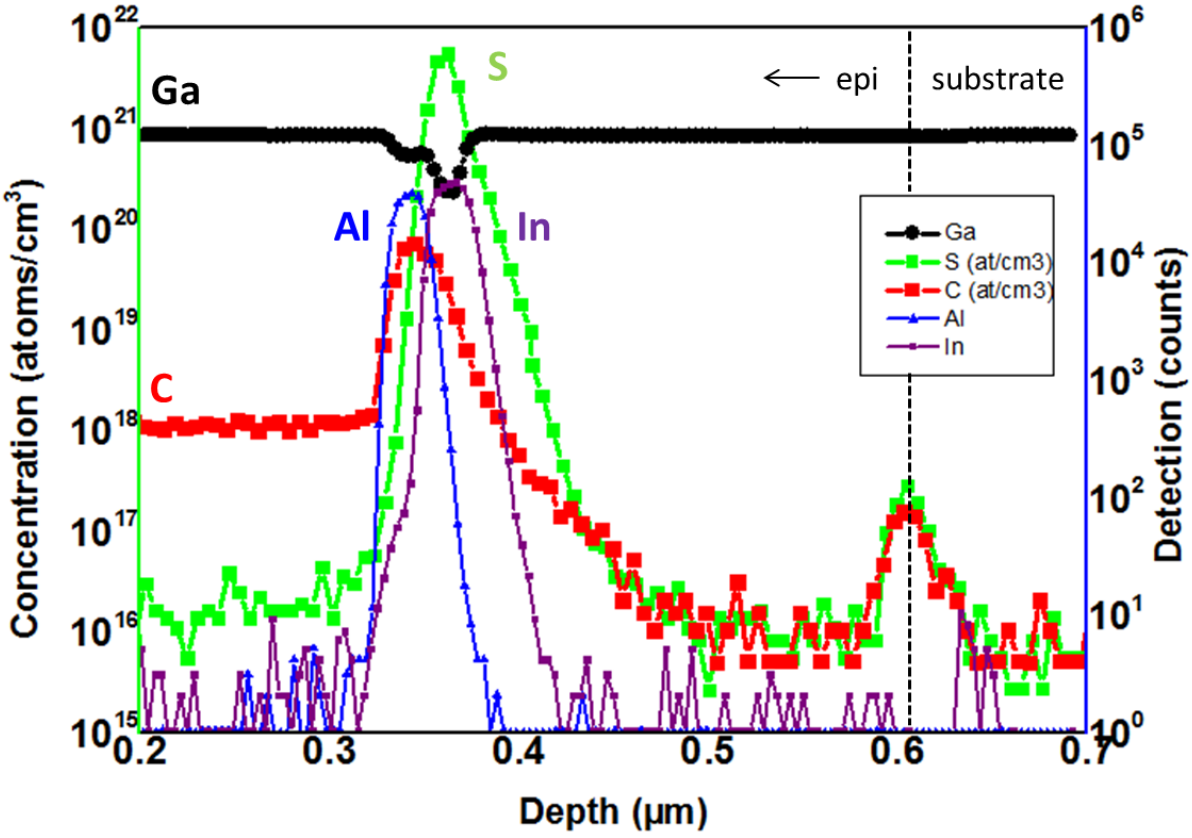



**Figure 4.11 - SIMS analysis of AlGaAs/GaInP tunnel junction.**

## IV.4. Calibration of n-doping with Te

Usual n-type dopants of GaAs material family by MOVPE are Si and S. Si is an amphoteric material and thus self-compensates the doping level for free-carrier concentrations above $5\times10^{19}$ $cm^{-3}$ [170]. The highest doping level achieved in our lab with Si was $1.2\times10^{19}$ $cm^{-3}$, as mentioned in the previous part. The best TJ from literature report the use of another n-type dopant: Tellurium. It has strong capacities to dope better the GaAs. Indeed, Te has a significantly lower diffusivity than Si and can provide donors with lower activation energy. It also allows more abrupt doping profiles. Previous papers report GaAs doping of $2\times10^{19}$ $cm^{-3}$ by molecular beam epitaxy (MBE)[171] or liquid phase epitaxy (LPE)[172]. Other studies showed doping levels up to 4. $10^{19}$ $cm^{-3}$ by MOVPE using DETe precursor[154,173]. Thanks to the strong motivation of Jean Decobert in installing a new precursor and the help of Nicolas Paillet, we show here a new type of precursor, the diisopropyl telluride (DIPTe), and to optimize the doping level of the layers grown, aiming at integrating into a tunnel junction. We will first present some parametric studies of the precursor, before pointing out the importance of the nature of the underlying buffer layers. Discussions based on the surfactant effect of Te will be proposed to explain this behavior.

## IV.4.1. A new precursor in the lab: DIPTe

Aiming at doping GaAs with Te, a new precursor has been installed in the MOVPE reactor: DiIsopropyl Telluride (DIPTe). This precursor is an organometallic that is widely used in the growth of II-VI materials such as HgCdTe. However, literature report the use of DETe (DiEthyl-Telluride) rather than DIPTe in MOVPE for III-V materials. DIPTe's saturation vapour pressure is slightly lower than DITe's one. DIPTe precursor is liquid at room temperature and is delivered into a stainless steel bubbler with a fixed temperature of 17 °C. Its line has a fixed pressure of 1950 mbar, leading to a molar fraction of DIPTe into $H_2$ of 0.12 %.

## IV.4.2. Parametric studies

A detailed analysis of the doping level as a function of several growth parameters is presented here. Our calibration samples usually consist of a thick intrinsic GaAs buffer layer of 300 nm grown on (100) GaAs substrates, followed by a 100 nm doped layer of GaAs:Te, which is the layer of interest. The stack is described on Table 4.1. The doping level of the GaAs:Te layers is systematically characterized using Electrochemical Capacitance-Voltage (ECV), whose principle has been introduced in Chapter III.3.2. (p.83). When necessary, secondary ion mass spectroscopy (SIMS) is used to determine the concentration of Te atoms. We study here the influence of the DIPTe/III ratio, the V/III ratio, and the growth temperature, aiming at reaching the highest possible n-doping level into GaAs to integrate into a tunnel junction.

**Table 4.1 - Typical stack of calibration samples**

| *Layer* | *Thickness* |
|---|---|
| GaAs:Te | 100 nm |
| GaAs Buffer | 300 nm |
| GaAs Substrate | - |

### Influence of V/III ratio

Te atoms are n dopants, thus they substitute As atoms. We first study the influence of the V/III ratio, by changing the $AsH_3$ flow rate at fixed DIPTe flow rate. To do so, we fixed the growth temperature at T = 580°C and the TMGa flow rate at 15 sccm, and DIPTe flow rate at 3 sccm, and varied $AsH_3$ flow rate. The resulting doping levels measured by ECV are shown in Figure 4.12.a. As expected, the higher is the $AsH_3$ flow rate (i.e. the lower V/III ratio), the less Te is incorporated into the layer. For the lowest V/III ratio used, we reached a doping level up to $3\times10^{19}$ $cm^{-3}$, which is already as desired: above the maximum $1.2\times10^{19}$ $cm^{-3}$ achievable with Si dopant.

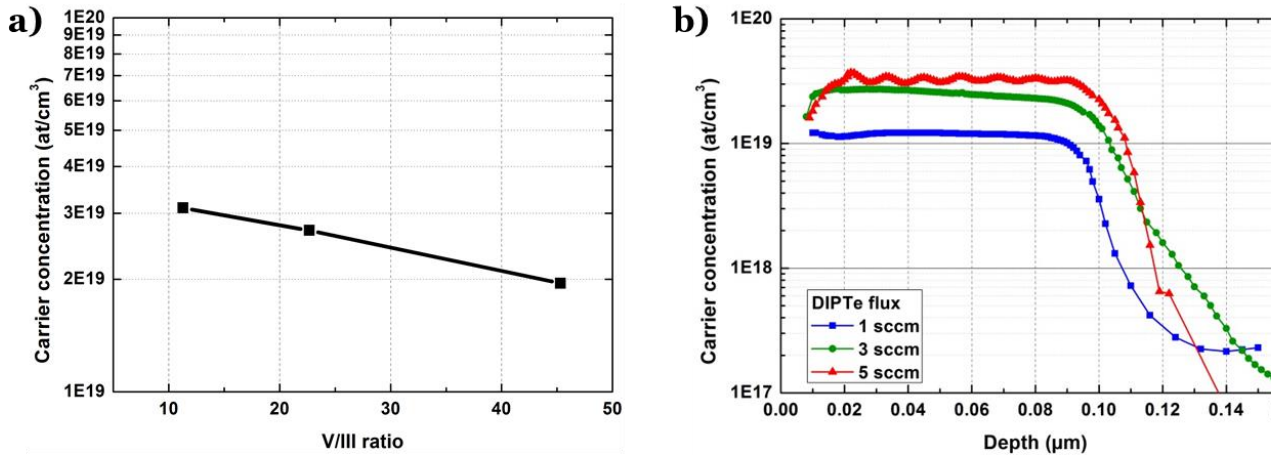



**Figure 4.12 - a) Carrier concentration as a function of III/V ratio with fixed growth conditions of T = 580 °C, on an undoped GaAs buffer. b) ECV measurements for three different DIPTe flow rates**

### Influence of the DIPTe flow rate

As we want to reach a doping level as high as possible in GaAs, we now vary the DIPTe flow rate. The 100 nm layer of doped GaAs was grown at a fixed temperature of 580 °C, with a constant growth rate of 22.9 nm/mn and a constant V/III ratio of 22.6. Here, only the DIPTe flow rate was modified: 1 sccm, 3 sccm and 5 sccm. Figure 4.12.b. shows the carrier concentration profile measured by ECV for each dopant flow rate. The carrier concentration increases while increasing the dopant flow rate. As seen in Figure 4.12.b, for 1 sccm of DIPTe, about $1.2\times10^{19}$ $cm^{-3}$ is reached, and $2.7\times10^{19}$ $cm^{-3}$ for 3 sccm. However at the highest flow rate, 5 sccm, the dopant reaches a maximum value for which the ECV measurement is unstable. This result is consistent with the results found in literature[174], where Te first increases with [DETe] mole fraction, then saturates. Nevertheless with a DIPTe flow rate of 3 sccm, we managed to have a stable measurement of a layer doped at $2.7\times10^{19}$ $cm^{-3}$. Thus, for the following studies, the DIPTe flow rate was held constant at 3 sccm and we studied the influence of other parameters.

### Influence of the deposition temperature

Temperature is a key element for incorporation of dopants. It must be high enough to dissociate the DIPTe precursor; however the lower temperature, the better Te can incorporate into the GaAs lattice. In this section, we study the effect of growth temperature upon dopant incorporation. The growth temperature was varied from 530 °C to 680 °C.

Figure 4.13 shows the Arrhenius plot of the carrier concentration. In the range of temperature that has been studied, the doping level increases while the temperature decreases. At 530 °C, a doping level up to $3.3\times10^{19}$ $cm^{-3}$ is reached. Same behavior has been observed with DETe precursor in GaAs[174–176]. At lower temperatures we expect the incorporation of dopants to be limited by the precursor decomposition[170]. In the range of temperature considered, the decrease in carrier concentration with increasing temperature can be explained by two different mechanisms. First, at high temperatures, the number of arsenic vacancies reduces, thus dropping the concentration of substitutional vacancies for Te atoms. Indeed, increasing the growth temperature increases the degree of thermal cracking of $AsH_3$, leading to an As overpressure. The second possible mechanism could be the re-evaporation of the Te atoms from the growing surface. It is worth noticing that the doping level drops from 3.3 $10^{19}$ to 2.5 $10^{19}$ $cm^{-3}$ for temperatures dropping from 530 °C to 680 °C, whereas in literature, GaAs layers doped with DETe drop by about one order of magnitude in the same range of temperatures[174,175]. Thus, the incorporation of Te in GaAs layers from DIPTe seems to be less sensitive to temperature modification than DETe.

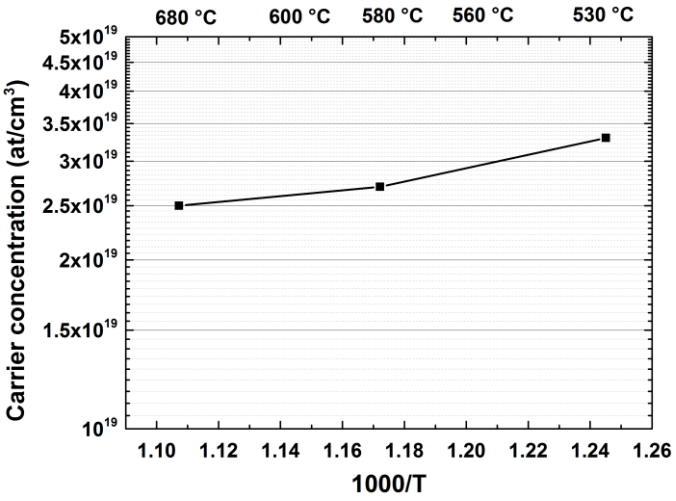



**Figure 4.13 - Carrier concentration as a function of temperature**

## IV.4.3. Effect of the buffer deposition temperature

In this part, we propose to study the impact of the underlying layer. Up to now, an intrinsic GaAs buffer layer was used. We now grow the highly doped GaAs:Te on top of a lowly Te-doped GaAs, because that is the buffer layer that will be integrated in the tunnel junction device. We also propose to analyze the impact of the growth temperature of this buffer layer. Five different samples have been grown with the structure shown in Figure 4.14.b. The varied parameters are: the buffer nature (intrinsic or Te doped) and the buffer growth temperature. The parameters of the upper layers were maintained constant: fixed temperature of 580 °C, 3 sccm of DIPTe, growth time.

**Observations**

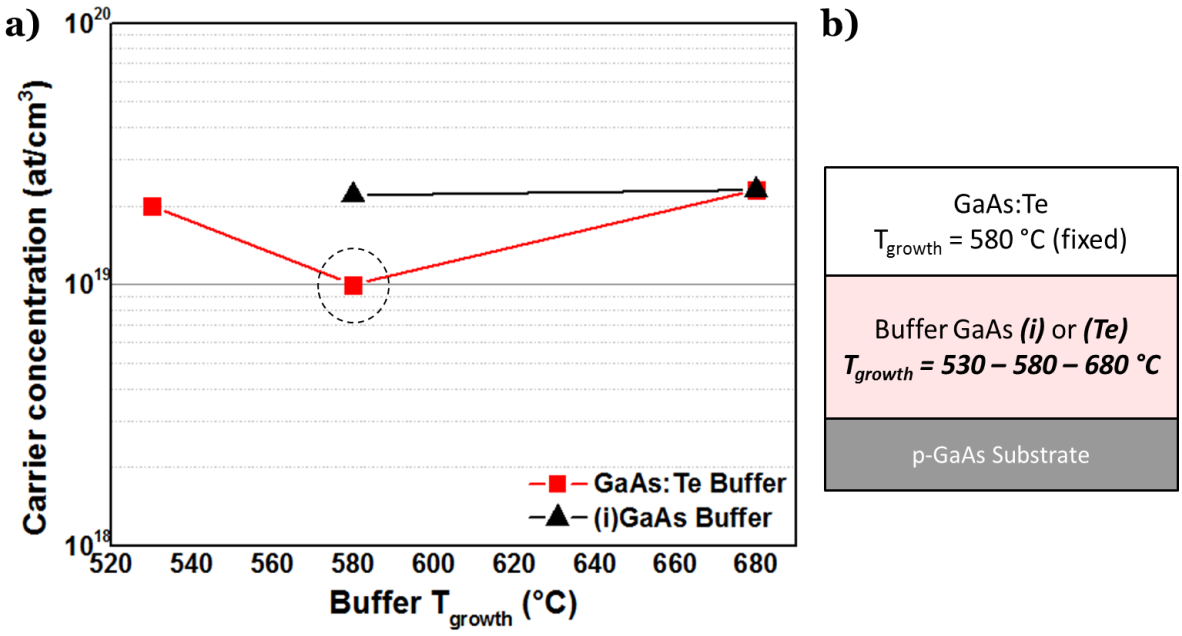



**Figure 4.14 - Carrier concentration of the heavily doped GaAs:Te layer as a function of growth temperature of the previous buffer layer for three different buffers : Te-doped and intrinsic GaAs.**

The Te-doped buffer was grown with a lower Te doping level of $2\times10^{18}$ $cm^{-3}$ at three different temperatures: 530 °C, 580 °C and 680 °C, and the intrinsic buffer was grown at 580 °C and 680 °C. The doping levels of the upper GaAs:Te layer are summarized in Figure 4.14.a. for different buffer layers nature and growth temperatures. Note that the abscise temperature corresponds the buffer layer growth temperature (and not the doped layer growth temperature), while the ordinate corresponds to the carrier concentration of the 100 nm upper GaAs:Te doped layer. We notice that the temperature of the buffer seems to have a strong impact on the Te-doped upper layer when the buffer is already Te-doped. While, at 530 °C and 690 °C, the doping level remains around the same order of magnitude than for an undoped buffer layer ($2\times10^{19}$ $cm^{-3}$), the doping level is surprisingly much lower when the buffer has been grown at the same temperature than the upper layer (580 °C). When the doped buffer is grown at a different temperature than the upper layer, the incorporation of Te seems to be better, and the ECV measurements are consistent with SIMS analysis that have also been performed on the same samples (not shown here). The most probable assumption is that this behavior is due to the time break that happens between the growths of the two layers, which is equivalent to an in-situ annealing. Indeed, as it is illustrated in Figure 4.15.a, when the temperature between the buffer layer and the GaAs:Te layer does not change, the upper layer growth happens directly after the buffer growth, with higher DIPTe flux, but no switch off. On the contrary, when the growth temperature changes, the reactor heating (or cooling) happens without TMGa nor DIPTe. The temperature stabilization usually takes around 15 minutes, and during this time, only $AsH_3$ enters the reactor. This stabilization phase is similar to an in-situ annealing.

In order to verify that the doping level of the upper layer is increased thanks to an in-situ annealing, the sample circled in Figure 4.14 was grown with the same GaAs:Te buffer grown at 580 °C, but this time with a 15 minutes break at 580 °C before growing the upper doped layer. Figure 4.15.b. shows the doping profile of the sample grown with a break between the GaAs:Te buffer layer

and the highly doped layers as compared with the directly grown after the Te-doped buffer layer. We see that the incorporation of Te in the upper layer is way more efficient with a break than without. Here we reach a doping level above $3\times10^{19}$ $cm^{-3}$. SIMS analysis have been performed on the same samples and confirm the same behavior: there is indeed less Te atoms in the sample that has been grown with a lightly doped GaAs:Te buffer layer without break before the upper doped layer. Consequently, our hypothesis seems to be confirmed: an annealing of the Te-doped buffer layer before the growth of the highly doped GaAs:Te seems to be necessary to reach high doping levels.

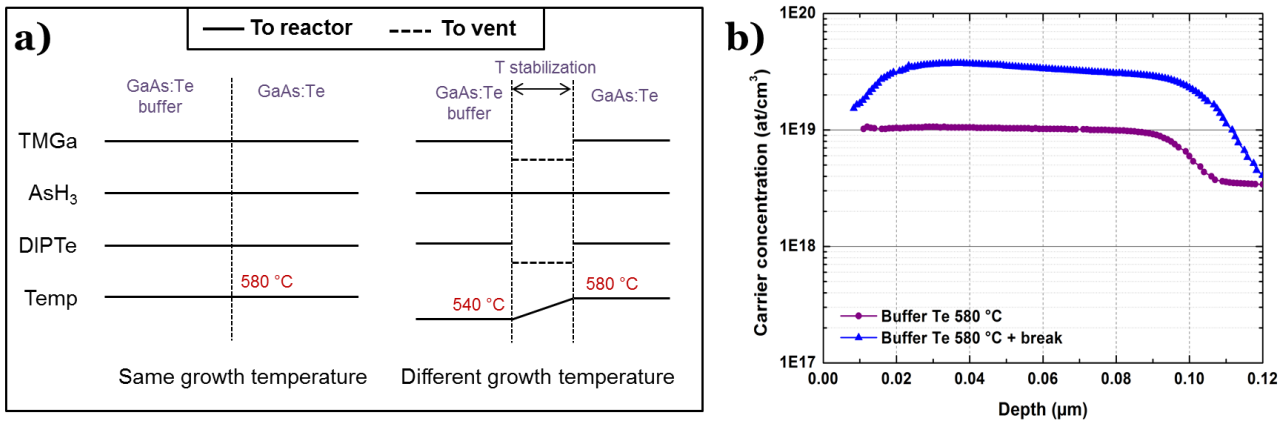



**Figure 4.15 - a) Switching sequences of precursors in case of no temperature change (left) andwith a temperature change (rigth) b) Doping profile of the upper doped layer grown directly after the buffer layer (purple circles), and grown after an annealing (blue triangles)**

This new experiment confirms that the difference in GaAs:Te doping level is due to a break during the growth that leads to an in-situ annealing, rather than a temperature effect. However, as seen in Figure 4.14, in the case of the undoped buffer layer, there is no significant change in the doping level. We thus may think that the effect comes from the presence of Te in the buffer layer. Te is known to have a memory effect [175,177] and to keep on being incorporated in layers grown after a Te-doped layer. Thus, we would have naturally expected a higher doping level in the growth without in-situ annealing, than in the growth where Te could have been desorbed. The following discussion tries to interpret the behavior that has been brought out.

### Discussion: Effect of surfactant on dopant incorporation

From the previous results, we have made the following observation: performing an annealing after the buffer layer growth and prior to the highly doped growth enables to have a better Te incorporation in the layer. In this discussion, we try to understand the mechanism that could be behind this observation. To do so, we must consider one particularity of Te atoms: they act as a surfactant (surface activating agent). In vapor phase growth, surfactants typically refer to substances that accumulate at the surface during growth and alter the surface properties. It has been widely seen in literature that Te affects the GaAs surface structure during MOVPE growth[178–180], but its effect on GaAs doping level has not been reported so far. Nevertheless, there are a few papers dealing with the effect of other surfactants on the doping level of III-V compounds. They show that a surfactant atom can modify the incorporation of dopants. Shurtleff *et al.*[181] studied Zn-doped GaAs grown by MOVPE using Sb as a surfactant specie. It revealed that Sb slightly enhances the Zn incorporation from $6\times10^{18}$ atoms/$cm^3$ to $9\times10^{18}$ atoms/$cm^3$. However, in the same paper they show

that the same Sb surfactant does not affect the Te incorporation. In a second paper[19], they reveal the same behavior on other p-type dopants: Zn, Be, Mg and Cd proposing the use of Sb surfactant as a way to enhance the p-doping level. The same team also showed that Sb and Bi surfactants decrease the incorporation of C, Si and S[182]. They attribute this behavior to a higher amount of hydrogen present at the growth surface, which helps the formation of volatile $SiH_4$ and $H_2S$, that would both desorb. A study on the incorporation of N into GaAs has been done by Dimroth et. al [183], using Te as surfactant. They report that the presence of Te reduces the incorporation of N, similarly to our case where Te surfactant seems to decrease the incorporation of Te dopant. They suggest that the surfactant atoms might block the N adsorption and thus, the incorporation of N into the solid. Garcia *et al.*[184] studied the surfactant effect of Te, but on GaInP: it reveals that Te and In react in the gas phase and on the growing surface. When there is more Te is in the gas phase, there is more In incorporated. They also show that the surfactant behavior of Te leads to a memory effect: an undoped layer grown on a Te-terminated surface would be Te-doped. However, there is no discussion about the effect of the presence of Te on the surface on the Te incorporation in the upper layers. Anyway, even if literature do not deal with the incorporation of Te dopant with a Te surfactant, it showed that a surfactant can be responsible for a decrease in the incorporation of an atom. To understand the observations made in our sample, we suggest to study the growth mechanisms of epitaxy using surfactant atoms, also called surfactant-mediated, so as to appreciate how Te atoms from the buffer layer can have an effect on the upper layer doping level.

**Surfactant mechanisms:**

A surfactant is an atom that tends to segregate and steadily cover the surface. It has first been demonstrated by Copel *et al.*[185] in 1989 on Si an Ge. Later, Grandjean and Massies [186] distinguished two types of surfactants: on the one hand, non-reactive surfactants, which are located on an interstitial sites. Their bonds with the semiconductor are rather weak, and have the effect to enhance the surface diffusion length. On the other hand, reactive surfactants - including Te - which are located in substitutional sites. They exchange with the growing adatoms. Figure 4.16 shows the segregating process they proposed. When a growing atom reaches the surface covered by surfactants (i), it creates bonds with the surfactant atoms (ii). Then, the segregation process imposes an exchange reaction between the adatoms of the growing layer and the surfactant atom, creating thus bonds with the underlying layers (iii). Reactive surfactants are known to reduce the surface diffusion length. The exchange between the growing adatom and the surfactant leads to a subsurface incorporation. The surfactant atom is consequently back to the surface, ready to exchange with the next growing adatom. At that stage, it is harder for the new grown atom to migrate because it would require to break their existing bonds, explaining the reduction in

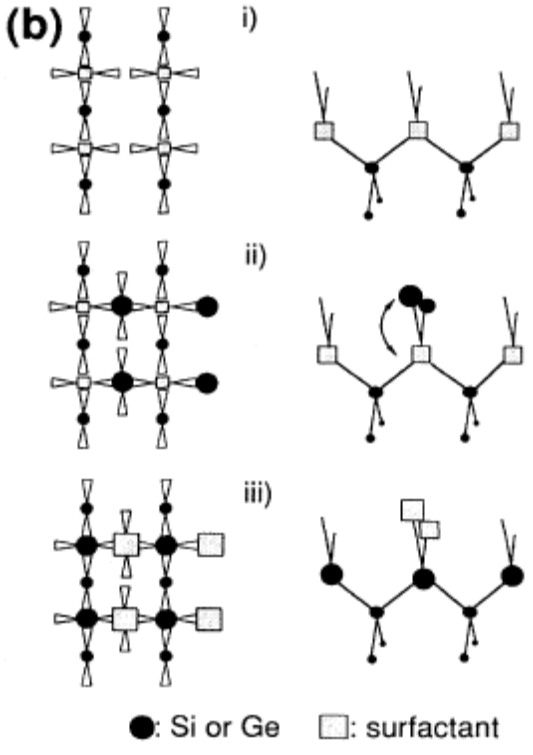



**Figure 4.16 - Schematic representation of atomic mechanisms with reactive surfactant (from Grandjean *et. al.* [186])**

surface diffusion length.

These mechanisms are consistent if we consider group IV materials. However, when it comes to III-V materials, a more complex mechanism has to be considered. The same authors [180] studied the surfactant effect on GaAs and deduced that, "the exchange process occurs only when As and Ga atoms are both present on top of a Te occupied site". Later, combining experimental evidences and simulation, Consorte *et al.*[187] determined a plausible exchange process for GaAs with Te surfactant. They proposed a cluster model to explain the growth process: the 3D view as well as the top view of their model is depicted in Figure 4.17. Both As and Ga adatoms should be present near the Te surfactant. Te atoms and As atoms move towards together, forming an As-Te bond (steps 1 to 5). In the meantime, a Ga adatom can form a bond with the underlying As atom (step 4). Then, the As-Te complex can rotate so that the As forms a bond with the new Ga. At this new position, the Te atom is in a similar configuration than prior to the layer growth, and is ready to repeat the exchange process and to help grow the next layer.

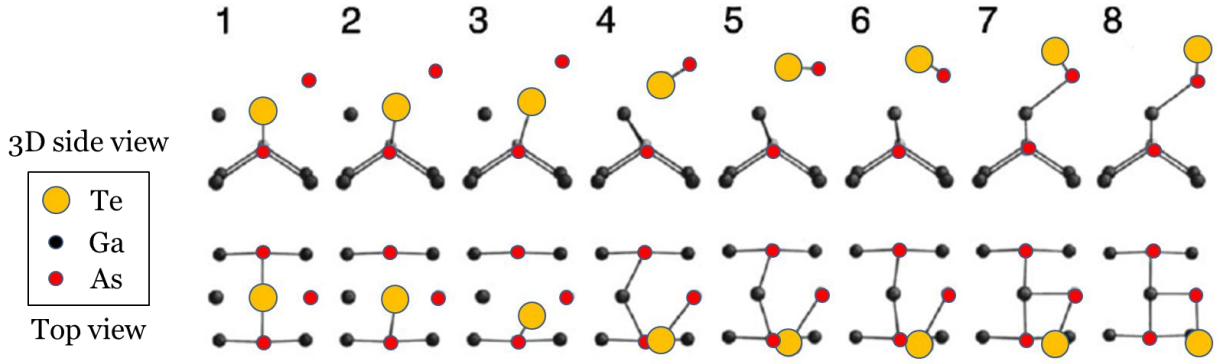



**Figure 4.17 - Exchange process between Te surfactant and GaAs (From Consorte *et al.* [187])**

By considering the growth mechanism that has been proposed by Consorte *et al.*[187], we can apply it to our observations with Te surfactant: if the surface of the Te-doped buffer layer is covered by Te adatoms. When increasing the DIPTe flow rate in order to highly dope the next layer, Te must replace As atoms to n-dope GaAs. It would mean that, to incorporate new Te atoms, at step 4 a Te-Te bond should be formed. However, it has also been reported that dimerization of Te atoms is not favorable [188,189]. Thus, this Te-Te bond is not likely to be formed and consequently than a As-Te one. Thus, an incorporation of Te instead of As is not favorable when a Te atom is already at the surface of the layer, because Te-As bond is more likely to be formed than a Te-Te bond. The in-situ annealing performed after the buffer layer growth may have helped the Te surfactants to desorb. More experiments would be necessary in order to confirm this exchange process, by for example performing the same experiment with buffer layers containing other type of surfactants (such as Sb or Bi[181]), or on buffer layers doped with other atoms (S, C, Si…) to give us a trend on the dependence of doping level with the nature of the underlying layer.

This parametric study allowed us to find the best growing conditions for having highly doped GaAs. We showed the importance of the nature of the buffer layer, and especially its growth temperature. We believe we understood that the presence of Te atoms at the surface of the buffer

layer reduces the Te incorporation of the upper layer (the doping level has dropped from 2 to $1\times10^{19}$ $cm^{-3}$). Nevertheless, we showed that an in-situ annealing of the buffer layer helps having the expected doping level of $3\times10^{19}$ $cm^{-3}$, probably because of the desorption of the Te atoms from the surface. Thus, in the further realization of tunnel junctions, we will perform an annealing after the growth of the lowly doped GaAs:Te buffer layer.

### IV.4.4. Growth of ternary compounds

After mastering the growth conditions for GaAs, growth of transparent ternary compounds (GaInP and AlGaAs) doped with Te has been studied in order to integrate into an AlGaAs/GaInP transparent tunnel junction. Literature shows that it is rather easy to reach high doping level in GaInP[170,190,191], even if the addition of Te affects the amount of In incorporated. By using the same conditions than in GaAs (DIPTe flow rate, V/III ratio, temperature), the conditions for our usual lattice-matched intrinsic GaInP had to be adapted, because we are used to grow GaInP at 680°C instead of 580°C. At lower temperatures, more In was incorporated into the crystal. After a few iterations of depositions and XRD characterizations changing the TMIn flow rate, we could grow lattice-matched GaInP doped at a satisfactory doping level 2.5 $10^{19}$ $cm^{-3}$. The ECV measurement of the calibration sample is shown inFigure 4.18.a. However, the doping of AlGaAs was more difficult to achieve. There are few papers[174,192,193] reporting the study of Te doping in AlGaAs, but they do not report high doping levels. After a few trials that led to the doping profile presented in Figure 4.18.b., with a maximum doping level of $5\times10^{18}$ $cm^{-3}$., we decided not to further explore the n-doping of AlGaAs.

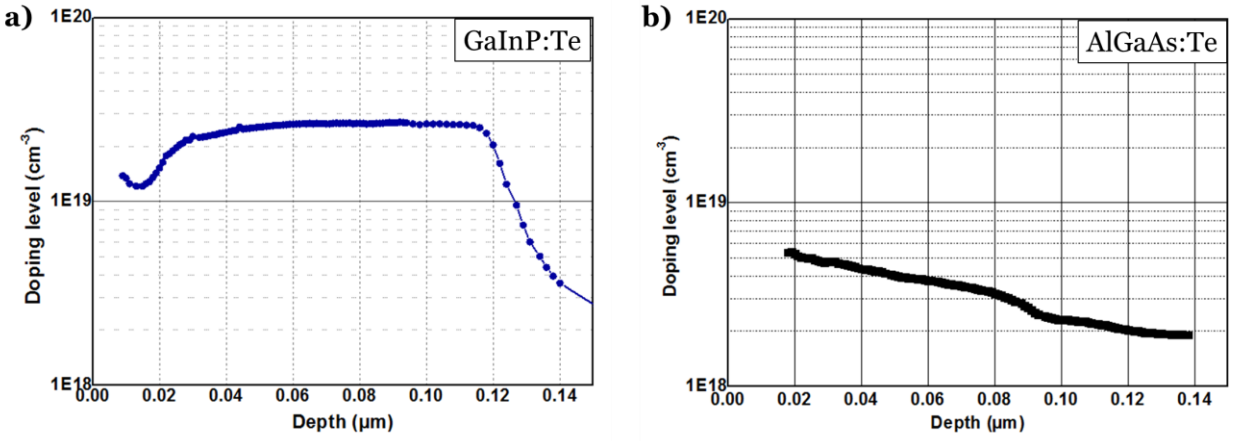



**Figure 4.18 - ECV measurements : best doping profiles obtained for a. GaInP doped with Te, b. AlGaAs doped with Te.**

# IV.5. Characterization of tunnel junctions doped with Te

## IV.5.1. n on p tunnel junctions

With the growth parameters determined in the previous part, tunnel junctions were grown on (100) p-GaAs wafers, and processed using the same process flow than presented in Figure 4.19. shows the ECV measurement of a GaAs/GaAs tunnel junction grown with the best conditions, as compared with the SIMS measurement of the two dopants: Te and C. We achieved $2\times10^{19}$ $cm^{-3}$ in the n-doped part. If we compare with the SIMS measurement, we see that not all the Te incorporated in the layer is activated. There is close to $1\times10^{20}$ $cm^{-3}$ atoms of Te in GaAs. Nevertheless, an active concentration of $2\times10^{19}$ $cm^{-3}$ is high enough to ensure good tunneling properties. At the junction, the ECV measurement is not reliable, and we trust the SIMS profile, which shows a very sharp interface between n- and p-layers. The p-doped layer seems to be less doped than expected (the nominal doping level was $1\times10^{20}$ $cm^{-3}$, but only $2.5\times10^{19}$ $cm^{-3}$ was measured by ECV). This behavior is not fully explained, but the sample has nevertheless been processed and measured, its doping levels being sufficient to allow tunneling at the junction.

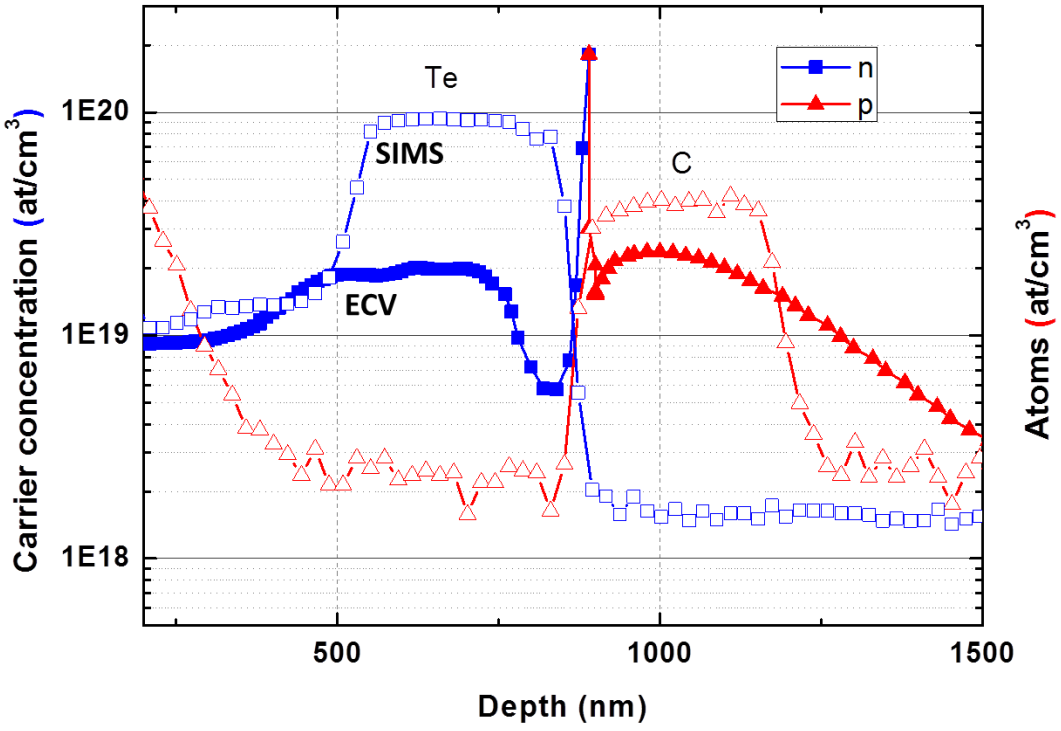



**Figure 4.19 - ECV measurements (full symbols) as compared with SIMS analyses (open symbols) of a n on p GaAs/GaAs tunnel junction doped with Te and C.**

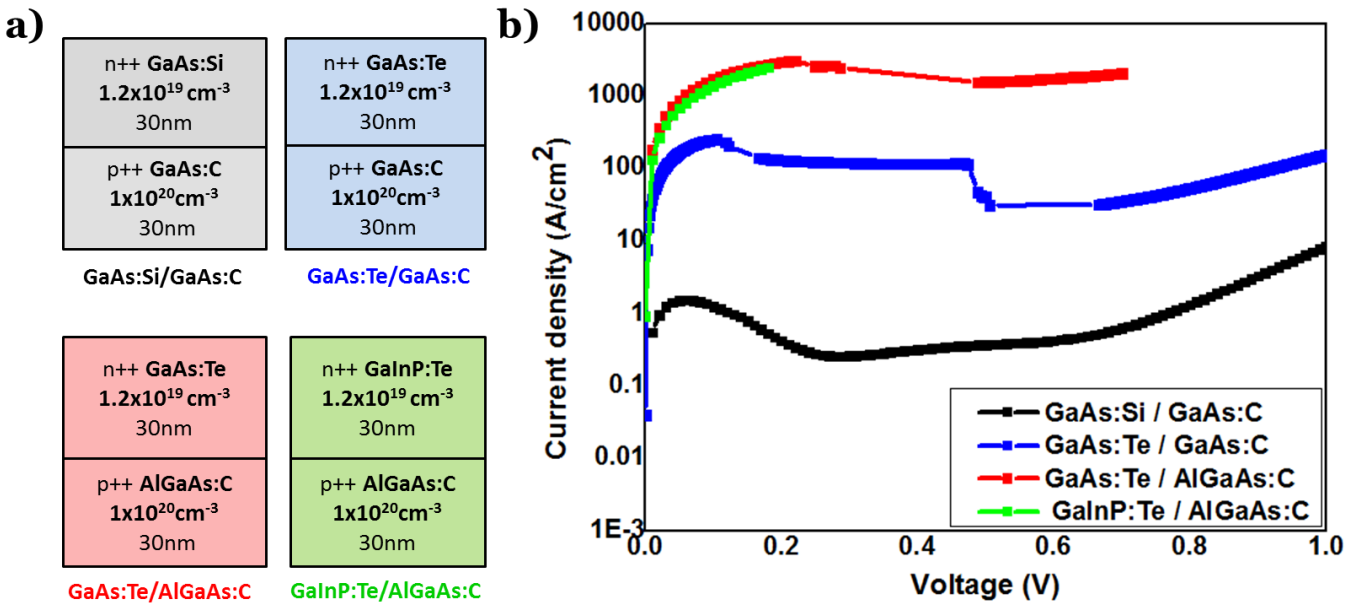



**Figure 4.20 - a) Tunnel junction structures b) and J-V characteristics**

Figure 4.20.a. shows the various TJ processed, in comparison with the previous Si-doped one. The three new samples are doped with Te: GaAs/GaAs, GaAs/AlGaAs and GaInP/AlGaAs. Samples were processed the same way that the previous TJs. We thus measured several diodes with different sizes. For all Te-doped samples, measurements on big diodes (500 µm* 500 µm and 200 µm * 200 µm) were hard to perform, because our I-V bench was limited to 1 A, thus the current was saturating. Though, on the smallest diodes (100 µm * 100 µm), we managed to have the ***J-V*** curves. For the GaInP/AlGaAs tunnel junction (green curve), we faced troubles measuring the ***J-V*** curves: the 100*100 diodes were "burning" during the measurement. We attribute this to a high resistance between the probes and the metal, leading to a local overheat. Thus, we only plot the measurements on 200 µm squares diodes. The ***J-V*** characteristics of the considered tunnel junctions are presented in Figure 4.20.b. The black curve corresponds to the previous sample n-doped with Si as a comparison. It has been plot in logarithmic scale, because the difference in $J_{peak}$ is of several orders of magnitude.

**Table 4.2 - Performances of n on p tunnel junctions**

| p material | n material | p- dopant | n- dopant | $J_{peak}$ (A/cm²) | $R_{peak}$ (Ω.cm²) |
|---|---|---|---|---|---|
| GaAs | GaAs | C | Si | 1.5 | $2.10x10^{-2}$ |
| GaAs | GaAs | C | Te | 250 | $3.14x10^{-4}$ |
| AlGaAs | GaInP | C | Te | >2500 | $7.23x10^{-5}$ |
| AlGaAs | GaAs | C | Te | 3080 | $6.29x10^{-5}$ |

Table 4.2 summarizes the $J_{peak}$ and $R_{peak}$ of the four structures. First, for the GaAs/GaAs tunnel junction, we reach a $J_{peak}$ of 250 A/cm² (blue curve), which is more than 100 times higher than the Si-doped one. By using GaAs/AlGaAs TJ (red curve), we still gain more than one order of magnitude: we reach above 3000 A/cm². This is consistent with the numerical simulations presented in Wheeldon *et al.*[154] for a given effective doping level (Figure 4.3). We find a resistivity as low as $6.29\times10^{-5}$ Ω.cm². Regarding the GaInP/AlGaAs TJ, despite the measurement issues already mentioned, we managed to measure the beginning of the curve, until the bench saturation at 2500 A/cm². However, theoretically, AlGaAs/GaInP tunnel junctions should not have as good performances as our AlGaAs/GaAs tunnel junction, thus we can also wonder if this TJ is shunted. In order to be able to measure this TJ, our perspectives are, first, try other contacting probes. We are using probes made of Tungsten (W), however we may hope to avoid burning the diodes by using other type of probes such as Au or Be. Also, designing a new lithographic mask with intermediate sizes (150*150 µm for example) could help understanding the behavior of this TJ, and would be more adapted to high $J_{peak}$ tunnel junctions. Actually this mask has already been designed, on which we also add of transmission line measurements (TLM) patterns in order to measure the contact resistance. However it has been received at the end of this PhD and has not been used in this study. Anyway, if this TJ is not shunted, its resistivity is in the same order of magnitude as the GaAs/AlGaAs one (~$3.\times10^{-5}$ Ω.cm²), exceeding the required performances of our application.

Thus, these results prove that Te is a good candidate to achieve n-doping levels for tunnel junctions suitable not only for 1 sun application, but also for solar cells working under high concentration.

## IV.5.2. p on n tunnel junctions: importance of ohmic contact

While most of the literature studies report n on p tunnel junctions, in our project the required polarity is p on n. Thus we grew the similar structures on n substrate. Learning from our observations of Chapter IV.4.3 (p.105) after the growth of the n buffer layer, we performed an in-situ annealing so as to maximize the n-doping level in the TJ. The diodes were then processed by depositing Ti/Pt/Au on the full back wafer and Pt/Au in front. At first, no contact annealing had been performed. The resulting ***J-V*** characteristics of a GaAs:C/GaAs:Te tunnel junction is shown in Figure 4.21.b. Interestingly, we measured an unusual shape. We first suspected a possible memory effect of the Te, which would have lowered the p doping level, even if we tried to avoid this memory effect by also performing an in-situ annealing prior to the p++ growth. Anyway, it may have still reduced the p++ doping level. To verify the doping levels, we performed the ECV measurement on this sample, shown in Figure 4.21.c. We notice that the doping levels in both parts of the tunnel junctions are similar to that of the previous working n on p diodes (see ECV in Figure 4.19). The interface is, as already explained, a measurement artefact, but Te diffusion into the p-part should not be the reason for the lack of tunneling at low bias. Thus, this TJ should show a usual TJ J-V curve. Looking at literature, we found one paper where the same behavior has been observed [194]. They attribute this to a too low doping level of the cap layer that subsequently prevents from forming a good ohmic front contact. Actually, we realized on the same ECV measurement, that no highly doped cap layer was grown on this sample. The doping level of the top layer is close to $1\times10^{18}$ cm$^{-3}$, which is probably too low to ensure good ohmic contact. Thus, we grew the same sample, but this time with a doped cap layer. In the meantime, AlGaAs/GaAs and AlGaAs/GaInP tunnel junctions were grown, also with the right cap layer. The details of the layers are presented in Figure 4.21a.. The full device is similar to that of the previous studies (n-buffer layer on a n substrate below

the TJ, and a spacer followed by a cap layer on top). The ***J-V*** characteristics of all the new samples are depicted in Figure 4.21.d. All the characteristics display diode-like behavior. As a comparison, the one n-doped with sulfur has also been plot (blue curve). We notice that the newly doped layers have a pretty good resistivity at low bias (about $2\times10^{-3}\ \Omega.cm^2$), even if they do not exhibit the typical shape of a TJ with the negative region. This resistivity is even better than the first TJ grown in the first part of this chapter. We thus think that there is actually tunneling occurring in this layer, but we do not manage to measure the negative resistance. The fact that we do not see this negative region could come from two reasons: either, the dislocation density in the layer is too high[195], or the contact resistance is too important[196]. We thus decided to perform an annealing of several processed samples, hoping to obtain a better ohmic contact. After 1 mn of Rapid Thermal Annealing at 400 °C, the samples we re-measured. The resulting ***J-V*** curves are plot in Figure 4.22, cas compared with the same TJs before annealing.

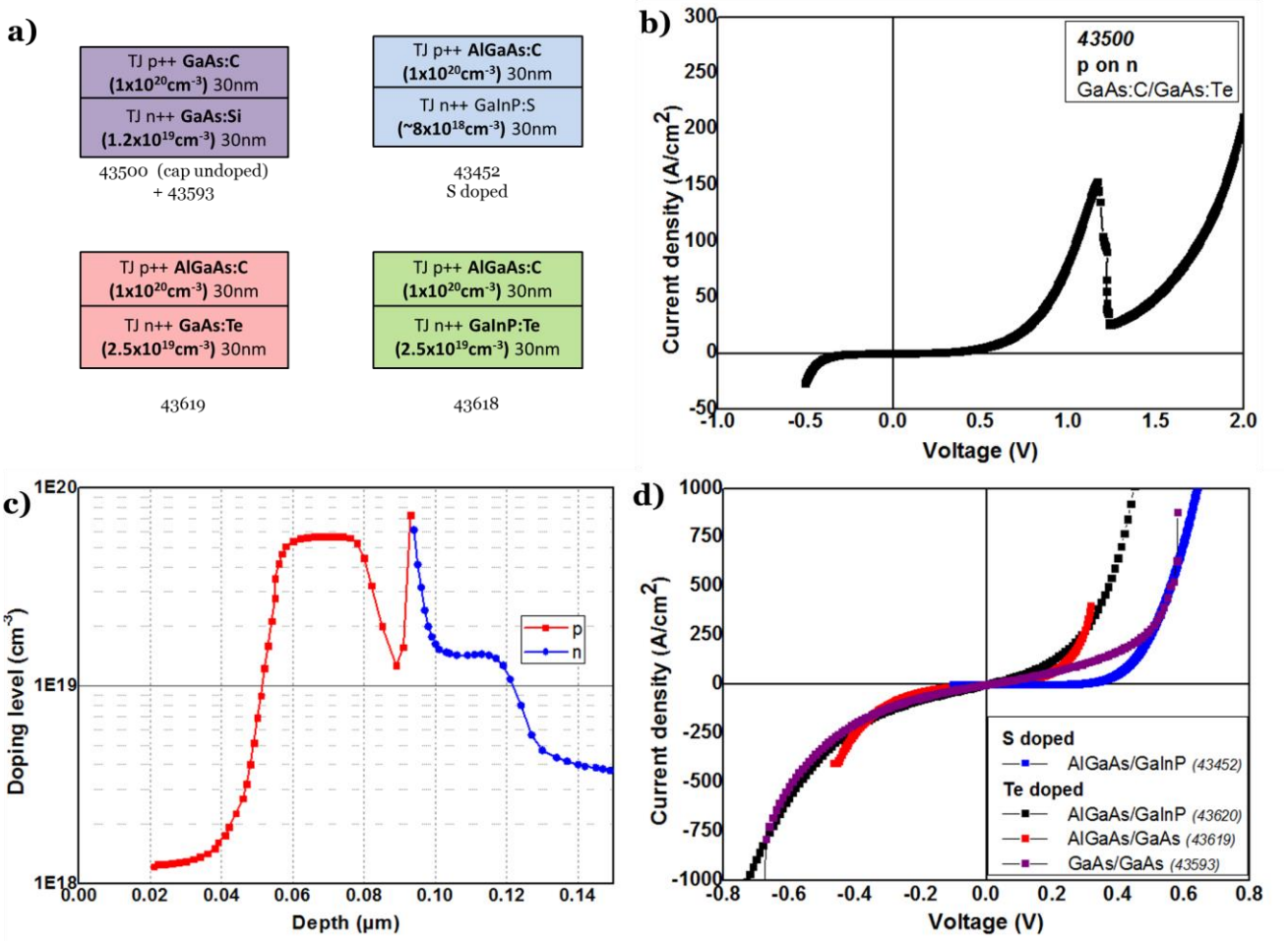



**Figure 4.21 - a) structure of 4 tunnel junctions b) J-V characteristics of a p on n GaAs/GaAs tunnel junction with lowly doped cap layer. c) ECV measurement on the same GaAs/GaAs TJ, d) J-V characteristics of 4 different p on n tunnel junctions with highly doped cap layer**

The result show, this time, the expected shape of a tunnel junction. Both AlGaAs/GaAs and AlGaAs/GaInP TJ have similar properties with $J_{peaks}$ around 1500 A/cm². This shows that the quality of the ohmic contacts is essential in order to properly characterize a tunnel junction. The fact that

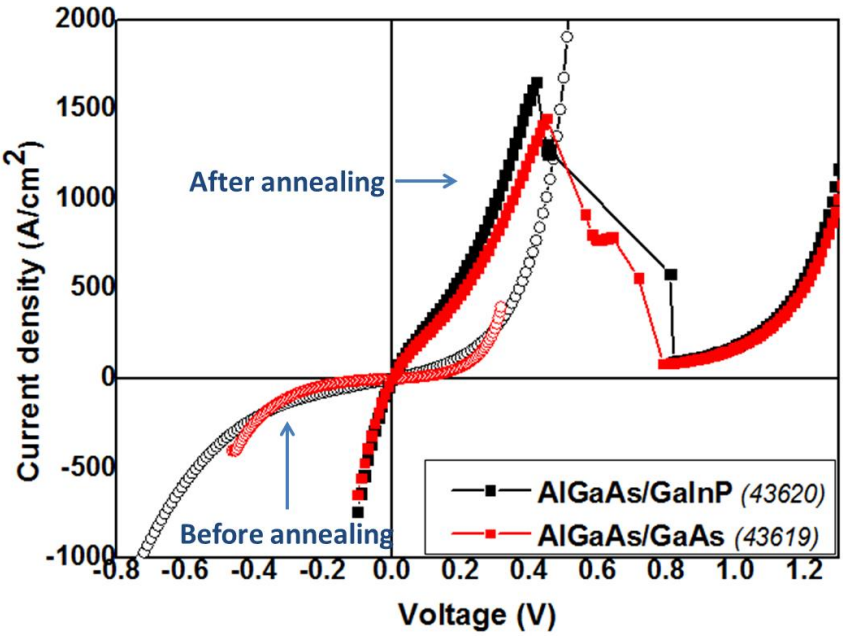



**Figure 4.22 - J-V characteristics of AlGaAs/GaInP (black) and AlGaAs/GaAs (red) tunnel junctions before (open symbols) and after annealing (full symbols)**

the two p on n TJ are similar comfort us on the fact that beginning of the curve of n on p AlGaAs/GaInP that we could not properly measure in Figure 4.20 is probably real, and not due to a shunt. Thus, we showed that we were able to also fabricate very good p/n tunnel junctions that are fully suitable with the final IMPETUS tandem device. We also pointed out, despite the necessity of enough doped layers for the TJ, the importance of the device grown, and especially its ohmic contact. A TJ can be a good TJ, but with bad contacts, it is possible that we cannot detect it in the ***J-V*** measurements. However, we proved with both n on p and p on n tunnel junctions that Tellurium was the good candidate for high n-type doping of TJ structures.

## IV. 6. Towards hybrid tunnel junctions

In the tandem device, the tunnel junction can be made as presented in the previous part, with III-V materials. On top of this III-V TJ, the Si epitaxial layer will be grown, which may induce interface defects between the GaAs and the Si, mainly with misfits dislocations. We do not have insight on the electrical activities of theses defects, but there are likely to induce recombination at the interface between Si and GaAs. In this part, we explore the possibility of taking advantage from these interface defects, by placing them at the middle of the tunnel junction. These defects would possibly enhance the tunneling via trap-assisted-tunneling[151]. In a recent paper, we presented numerical simulations of such hybrid GaAs/Si tunnel junctions[196], showing that even without defects at the interface, both n-Si/p-GaAs and p-Si/n-GaAs heterostructures can tunnel if the layers have a sufficient doping level (> $2x10^{19}$ $cm^{-3}$). Here, we present the development of the growth of doped Si by PECVD on GaAs, aiming at having highly doped Si for hybrid tunnel junctions. Previous works at the LPICM have shown the possibility of growing doped silicon on silicon (100) wafers [67]. The main challenge was to adapt the conditions to deposit these layers on doped GaAs grown by MOVPE. The details of these PECVD growths are presented here.

## IV.6.1. n-type c-Si with $PH_3$

For each sample, the cleaning and the deposition were performed in two different chambers of the Arcam reactor. One chamber was dedicated to the in-situ $SiF_4$ cleaning, and the other one to the short $H_2$ plasma, followed by the deposition of doped Si, in order to avoid any contamination during the crucial step of substrate cleaning. Before each new deposition, a precoating of the chamber walls with intrinsic silicon was performed, in order to limit the contribution of the dopants present on the walls of the reactor due to the previous deposition.

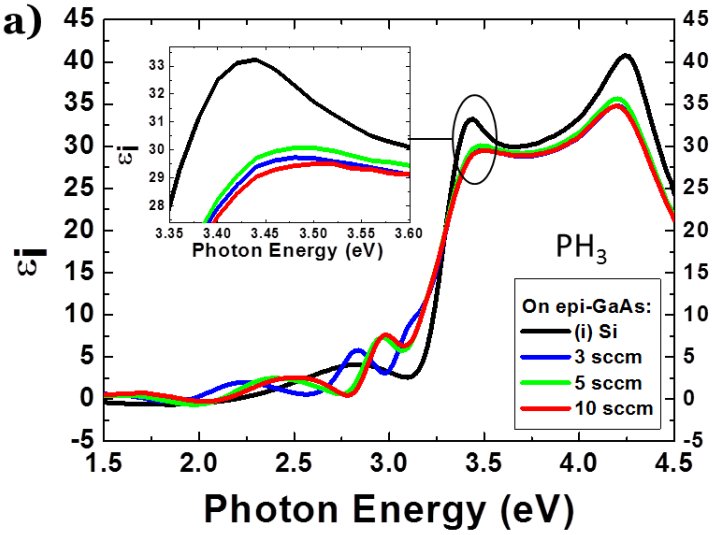
In this series of experiment, we present the growth of doped Si on top of GaAs. We first present the deposition of phosphorus doped layers, in ARCAM reactor. The depositions were made at 175 °C using the best epitaxy condition that was determined earlier. In this part, we propose to deposit the layers not on GaAs wafers but on GaAs layers that have already been epitaxially grown by MOVPE. The $PH_3$ bottle used was diluted at 0.01% into hydrogen. The depositions were made at 175 °C on p-doped GaAs:C samples grown by MOVPE. The cleaning of the GaAs substrate was done in-situ with the conditions gathered in Table 4.3.

**Table 4.3 - Cleaning and growth conditions of doped Si layers on GaAs (Arcam)**

| Step | Time | Pressure | RF Power | $SiF_4$ | $H_2$ | $SiH_4$ | PH3 |
|---|---|---|---|---|---|---|---|
| Cleaning | 4 mn 15<br>2 mn<br>30 s | 90 mTorr<br>90 mTorr<br>2,1 Torr | 11 W<br>5 W<br>30 W | 30 sccm<br>30 sccm<br>- | -<br>-<br>200 sccm | -<br>-<br>- | -<br>-<br>- |
| Deposition | 10 mn | 2,1 Torr | 30 W | - | 200 sccm | 34 sccm | 0-3–5–10 sccm |

Four different samples were grown with $PH_3$ flow rates ranging from 0 to 10 sccm, which is the maximum value of the mass flow controller. The ellipsometric spectra of the epitaxial layers are presented in Figure 4.23.a. We can see that the introduction of $PH_3$ decreases the crystalline fraction of the c-Si layer, as compared with the intrinsic c-Si layer grown on the same epi-GaAs wafer. However, increasing the $PH_3$ flow rate from 3 to 10 sccm does not significantly modifies the value of $E_1$ or $E_2$. The samples were co-deposited on an intrinsic GaAs wafer in order to perform Hall Effect measurements. The resulting values obtained are gathered in Figure 4.23.b. As expected, the higher is the $PH_3$ flow rate, the higher is the n-doping level. For 10 sccm, we could reach $1\times10^{20}$ $cm^{-3}$. SIMS analysis on the sample grown with 10 sccm also revealed $1x10^{20}$ $cm^{-3}$ of $PH_3$, thus a full activation of the dopants. Those values are consistent with the results that have been obtained on Si substrates using LT-PECVD[68]. Note that the phosphorus doping efficiency in c-Si is much higher than in a-Si:H. Experimentally, we used a bottle of $PH_3$ diluted to at 0.01% in $H_2$, while to have similar doping levels in an amorphous layer, we used phosphine diluted at 1% into $H_2$. In the Octopus reactor, as mentioned in Chapter II, the dilution of the phosphine was 0.1%. It is too diluted to ensure a good doping of the amorphous layer (hence the need of adding a micro-oxide to ensure a good ohmic contact in our heterojunction solar cells), but it is adapted to ensure a good control of the doping level in crystalline Si.

a)




b)

| $PH_3$ flow rate (sccm) | Doping level Hall effect ($cm^{-3}$) |
|---|---|
| 3 | $1.10^{19}$ |
| 5 | $6.10^{19}$ |
| 10 | $1.10^{20}$ |

**Figure 4.23 - Ellipsometric spectra of silicon thin films grown on epi-GaAs with various $PH_3$ flow rates**

## IV.6.2. p-type c-Si with TMB

The growth of boron-doped epitaxial film has also been studied. We use trimethylborane (TMB), 2%-diluted in $H_2$. As for $PH_3$, we used the optimum cleaning and deposition parameters to grow crystalline Si on GaAs i.e. the same parameters than reported in Table 4.3. and added 0.5 sccm and 0.8 sccm of TMB. The growth was performed at 175 °C, and the films were codeposited a c-Si substrate and an epitaxial film of n-type GaAs doped with Si. The ellipsometric spectra of the deposition with the two flow rates of TMB are shown in Figure 4.24.a, as compared with intrinsic epi-Si. The squares correspond to the depositions made on Si substrates, while the simple lines are deposited on epi-GaAs layers. We notice that the depositions of boron-doped layers are crystalline on Si substrates. For 0.5 sccm of TMB (blue curve), the crystallinity is already lower than that of (i)-epi-Si as deduced from the intensity of the peaks at 3.4 eV and 4.2 eV. For 0.8 sccm, the crystalline quality keeps on dropping, with an intensity at $E_1$ and $E_2$ around 28. On GaAs wafers, both boron-doped layers are found to be 100 % amorphous. We tried to increase the etching time in order to have a better surface preparation (4mn15, 6mn, 8 mn and 10 mn), but all the results on GaAs were amorphous. Then, we performed the growth at lower temperature: 150 °C. The ellipsometric spectra of this new deposition with 0.5 sccm of TMB on Si and GaAs are shown Figure 4.24.b, in blue, and compared with the intrinsic growth at 175 °C (black) and the growth with 0.5 sccm of TMB at 175 °C (red). This time, the film grown on GaAs wafer was epitaxial. We can even notice that the growth of doped Si on GaAs at 150 °C has a better crystalline quality than that of the intrinsic layer grown at 175 °C on GaAs, as judged by the higher value at $E_1$=3.4 eV. Also, on Si substrate, for the same TMB flux of 0.5 sccm, we see that the quality of the film grown at 150 °C (blue squares) is better than the one grown at 175 °C (red squares).

Previous studies in the lab have shown that the TMB is not really sensitive to the change in substrate temperatures (Labrune's thesis, [197] p172). By growing epi-Si with 0.8 sccm of TMB with temperature ranging from 175 °C to 225 °C, no significant change in the ellipsometric spectrum was observed.

However, we cannot compare our results on Si substrates with theirs, considering that they cleaned their Si substrates with ex-situ with HF dipping, while the in-situ cleaning that we used in these experiment is not optimized for Si growth. Thus, it is possible that the quality of the epitaxial growth of p-doped Si on Si is better at 150 °C than 175 °C due to the fact the in-situ cleaning has been performed at 150 °C instead of 175 °C. Actually, no study of the effect of the chamber temperature during $SiF_4$ plasma has been performed yet, thus, we do not know exactly how the surface preparation is affected by the in-situ cleaning. Nevertheless, we found that performing the in-situ cleaning and the boron-doped Si deposition on a GaAs substrate led to an amorphous layer when performed at 175 °C and to a crystalline one at 150 °C.

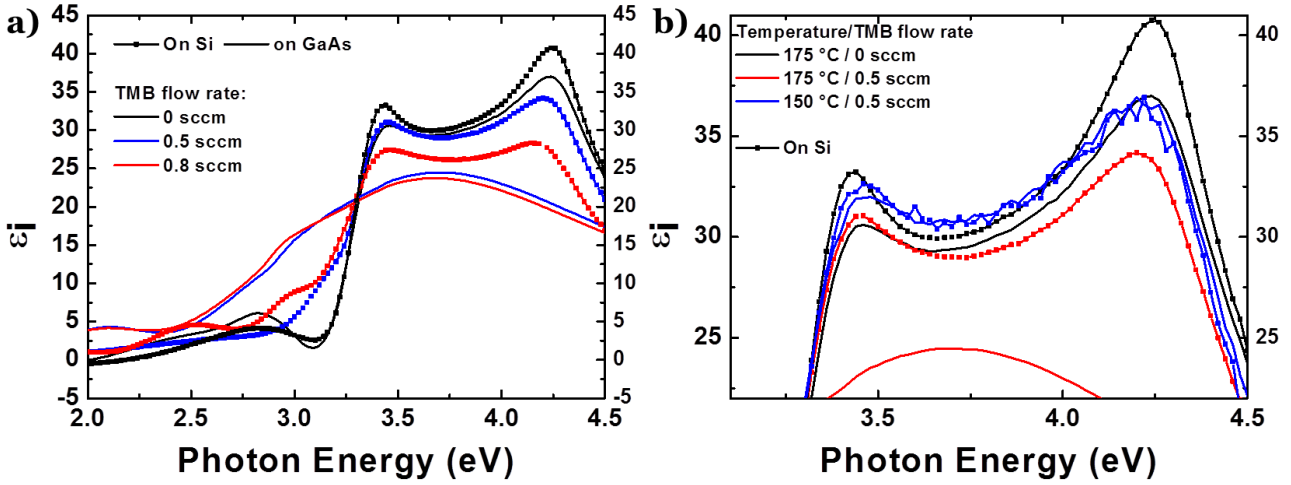



**Figure 4.24 - a) Ellpisometric spectra of Si grown with TMB on Si substrate (squared) and on epi-GaAs (lines) with various TMB flow rates, b) Ellipsometric spectra on Si and epi-GaAs at various TMB flow rate and temperatures**

Hall Effect measurements were also performed on the boron-doped Si layer grown, that was co-deposited on a semi-insulating GaAs substrate. For 0.5 sccm of TMB, we measured an active doping level of $3\times10^{19}$ $cm^{-3}$. SIMS analyses showed around $8\times10^{19}$ $cm^{-3}$ boron atoms in this epitaxial layer of 180 nm grown with 0.5 sccm of TMB. It means that boron is not fully activated. However, this doping level should be high enough for hybrid tunnel junction integration.

## IV.6.3. Characteristics of hybrid tunnel junctions

Thus, we managed to grow both n-type and p-type silicon, with respective doping levels of $1\times10^{20}$ $cm^{-3}$ and $3\times10^{19}$ $cm^{-3}$ on GaAs epitaxial layers. A n-Si on p-GaAs tunnel junction has thus been fabricated using the previous deposition conditions. p-GaAs with $1x10^{20}$ $cm^{-3}$ was grown by MOVPE and n-Si with $1x10^{20}$ $cm^{-3}$ by PECVD. The back contact was made with Pt/Au, and the front contact in Ti/Au was deposited directly on the doped Si layer (~120 nm thick), without adding spacer nor cap layers. The resulting ***J-V*** curve measured is presented in Figure 4.25., as compared with the synthesis of all our III-V tunnel junctions presented in Figure 4.20.b. The hybrid junction

characteristics before annealing show a diode-like behavior, without tunneling effect. The voltage drop at a typical $J_{SC}$ around 21 mA/cm² would be of 0.06 V if this junction was integrated in a tandem solar cell. The main hypothesis for such a behavior comes from the observation made in Chapter III.3 (p.82), the PECVD process has reduced the p-doping level in the GaAs at it surface; because of the formation of C-H complexes that deactivates the dopants. In an hybrid device, the doping level at the surface of GaAs is even more crucial, as it corresponds to the tunneling interface. It is also possible that the contact performed on the Si side (Ti/Au) is not good enough, and thus prevents from measuring the real ***J-V*** curve, as we have also observed in Figure 4.20. We performed an annealing at 350 °C as suggested by the results from Chapter III.3.3 (p.84), in order to recover from this doping level reduction. The ***J-V*** curve after annealing show a resistance of $9\times10^{-4}$ Ω.cm², which is even better than our previous GaAs/GaAs TJ doped with Si (black line), and slightly lower than that of the one doped with Te (in blue).

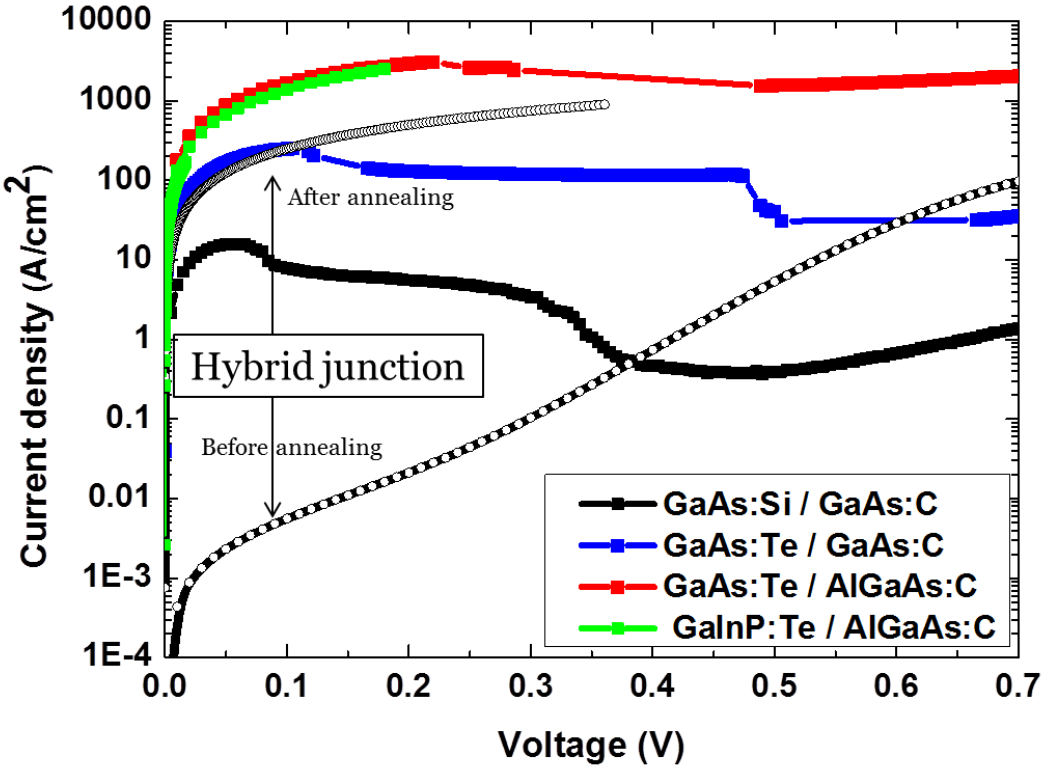



**Figure 4.25 - Hybrid Si/GaAs junction as compared with III-V tunnel junctions before and after annealing**

This is a very promising even though the measurements did not permit is to see the negative region of the ***J-V*** curve, thus it is hard to conclude on the performances of this tunnel junction. Literature has shown with modelling that in case of a material containing a too high defect density in the tunnel junction doped layers, the negative region cannot be visible[195]. Considering that the doped Si is more defective due to the high concentration of phosphorus, this may explain our results. But other hypotheses can be raised, linked to the front contact: 1) either this contact exhibits a resistivity close to the one measured ($9\times10^{-4}$ Ω.cm²), and the tunnel resistivity is so low that it cannot be distinguished, or, 2) the p-n junction is simply shunted, due to the metal diffusion during annealing.

Once again, we show that the tunnel junction performance does not only rely on the doping level of the p- and n- layers, but also on the design and the process of the structure. The need to use

appropriate ohmic contacts that do not risk diffusing in the layer over annealing is primordial. A 'bad' ***J-V*** characteristic of a separated TJ device does no necessary means that the TJ itself is not functioning. It could work once integrated in a tandem solar cell, away from any poor ohmic contact issue or metal diffusion. This study requires further experiments in order to assess whether or not a hybrid tunnel junction is feasible. A new lithographic mask for tunnel junctions that includes TLM (transmission line measurements[198]) patterns has been fabricated. TLM measurements allow assessing the specific resistance of a contact on a semi-conductor. We will thus be able to verify the resistance value after each metal deposition, and if it has diffused after a 3-minutes annealing at 350°C.

# IV.7. Conclusion

This chapter introduced one of the building blocks of the IMPETUS tandem solar cell: the tunnel junction (TJ). This essential part of the device allows carriers to flow from one subcell to the other, by tunneling effect. We developed III-V/III-V TJ using standard dopants C and Si. They exhibit good peak tunneling current of 7 A/cm², with a resistivity of ~$1\times10^{-2}$ Ω/cm². These values are sufficient for a tandem solar cell working under 1 sun. However, we could not grow efficient transparent AlGaAs/GaInP tunnel junctions with those dopants. The development and understanding of the growth of n-type GaAs with DIPTe precursor was undertaken. We first show that Te incorporation with DIPTe is less sensitive to the growth temperature than with DETe, the usual precursor used in literature. We found that the presence of Te in underlying layers reduces the incorporation of Te in the upper highly doped layer. We suggest that it is due to the surfactant effect of Te, and propose a mechanism to explain the lower incorporation of Te. We show that annealing the underlying layer avoids this reduction in dopant incorporation. Using this dopant allowed to reach n-type doping levels above $2.7\times10^{19}$ $cm^{-3}$.

The fabrication of both n on p and p on n tunnel junctions doped with Te led to state-of-the-art performances: peak tunneling currents up 3000 A/cm² along with resistivity of $6\times10^{-5}$ Ω/cm² have been measured, which is way higher than required for our tandem solar cell. We also pointed out the importance of the design of the test structure, and especially of the ohmic contacts. We explored the possibility of doing hybrid Si/GaAs tunnel junctions, but could not conclude on their performances due to too many uncertainties concerning the contacts. This path still remains to be further explored for the integration in the tandem solar cell. Further development of the tandem cell in this thesis, we will use III-V tunnel junctions doped with Te, whose good performances have been proven.

Chapter 5

# III-V solar cells processing and bonding: towards inverted metamorphic tandem devices

## Content

This chapter deals with the process development of two main building blocks of the tandem device that we aim to fabricate: the III-V sub-cell, and its bonding to a foreign substrate. We first present the design of the structure and the realization of the device in clean room environments. The III-V lab has a strong expertise in III-V materials for optoelectronic and photonic devices, but its expertise had to be adapted to our application: photovoltaics. Combining the strong know-how in PV of LPICM together with the techniques available in the III-V Lab clean rooms was one of the milestones of my PhD. While the classical techniques used in III-V industry (MOVPE and clean room technologies) have been introduced in the previous chapter, we present here their application to the growth and processing of an $Al_{0.22}Ga_{0.78}As$ solar cell structure. Then, we assess the final step of the realization of the tandem solar cell: the bonding, followed by the substrate etching and cell processing. First on single inverted III-V solar cells, then on an inverted Si/AlGaAs tandem solar cell, we detail the numerous technological challenges that we have to overcome in order to successfully complete the tandem device.

# V.1. AlGaAs solar cells

## V.1.1. AlGaAs solar cell structure

GaAs single solar cells have been developed for many years. Back in 1990, MOCVD grown GaAs cells reached a 24.8 % under 1-sun AM1.5[199]. Indeed, the GaAs bandgap of 1.42 eV is closed to the optimum bandgap for AM1.5G solar spectrum, as presented in Chapter I (Figure 1.1). Moreover, unlike Si, it has a direct bandgap, thus requiring only a few microns of GaAs to absorb totally the photons with energies above 1.42 eV. More recent works have enabled to reach 28.8% conversion efficiency under 1 sun[200,4]. The detachment of the thin active layer from its substrate by a lift-off process enables to add a metallic back reflector, which lowers the required active region thickness. Furthermore, the substrate can be reuse, cutting down the costs.

However, for integration in a tandem device, a bandgap higher than 1.42 eV is needed. Simulations show that the required bandgap to be in current matching condition with Si should be around 1.74 eV. This bandgap corresponds to $Al_xGa_{1-x}As$ with x = 22 %. AlGaAs is chosen because it stays lattice-matched to GaAs while varying x, as introduced in Figure 1.5, thus the bandgap can be easily tuned. Extensive studies of AlGaAs with x>20% solar cells grown by MBE[201–203] [204]or MOVPE[205–207] have

**Table 5.1 - GaAs and AlGaAs performances reported from literature ([200, 216, 205, 204, 207])**

| Reference | Dep. Technique | Structure | %Al (%) | $V_{OC}$ (V) | Jsc (mA/cm$^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|---|---|
| Kayes 2011 | MOVPE | p / n | 0 | 1,107 | 29,6 | 84,1 | 27,6 |
| Van Geelen 1997 | MOVPE | p / n | 0 | 1,038 | 27,15 | 84,6 | 23,9 |
| Virshup 1985 | MOVPE | n / p | 20 | 1,18 | 14,5 | 83 | 14,2 |
| Yazawa 1994 | MBE | n / p | 22 | 1,2 | 12 | 80 | 13,7 |
| Heckelmann 2015 | MOVPE | n / p | 20 | 1,246 | 15,8 | 85,9 | 16,91 |
| This work | MOVPE | p / n | 22 | 1,24 | 17,33 | 81,75 | 17,62 |

been carried out, leading to conversion efficiencies around 14% for MBE grown $Al_{0.20}Ga_{0.80}As$ solar cell and up to ~17% for MOVPE grown $Al_{0.20}Ga_{0.80}As$. A summary of a few GaAs and AlGaAs record solar cells are presented in Table 5.1. Also, the typical structures of the solar cells in case of a p-type base and a n-type base are shown in Figure 5.1. We developed AlGaAs solar cells with an Al content of 0.22 %, by using a structure similar to that of Figure 5.1.b. The various layers of our final tandem solar cell is presented in Figure 5.2.a., and corresponds to the structure that has been used for simulation in Chapter 1[52]. The main reason why we chose a n-based subcell is that, as deduced from Chapter II.2.2. (p.37) we must avoid performing annealing at temperatures higher than 250°C. As a good ohmic contact on n-doped GaAs requires an annealing at 400 °C (Chapter IV.5.2 (p.113)), a p-type contact should be preferably used, hence our polarity choice. We consequently realized the structure detailed in Figure 5.2.b. An $Al_xGa_{1-x}As$ solar cell with x=0.22 so has to be current-matched with the Si subcell, that corresponds to a bandgap of ~1.74 eV.

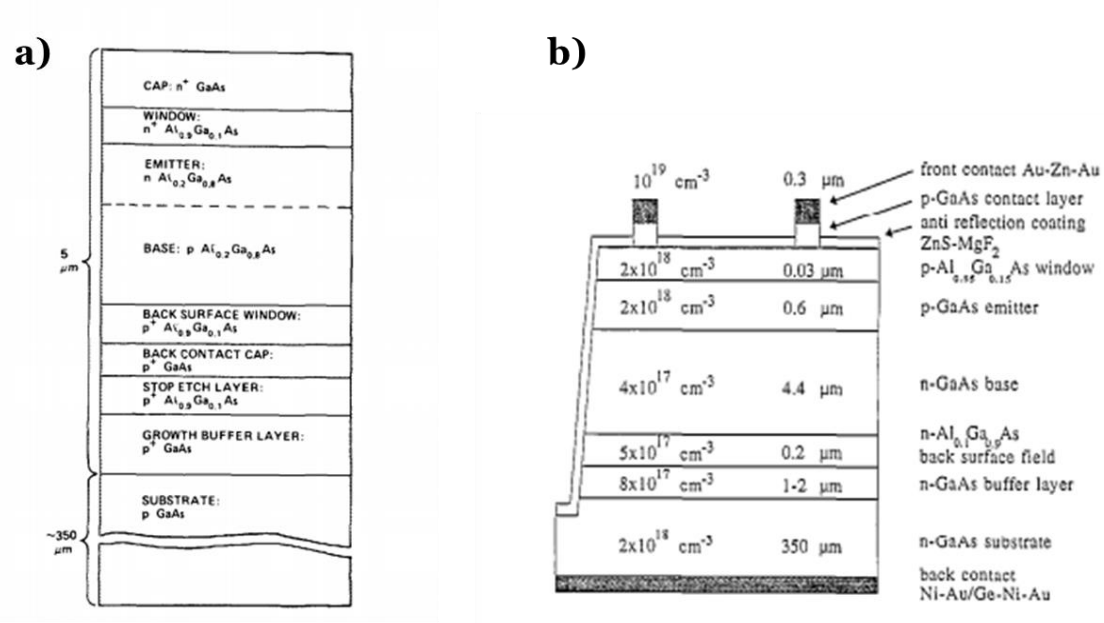
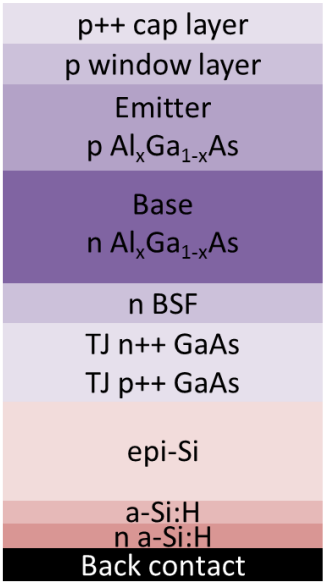



**Figure 5.1 - a) Typical n on p structure (from Virshup et al.[205]) b) Typical n on p structure (from van Geelen et al[216].)**

In addition to the thick base (2 µm) and thin absorber (around 100 nm), the structure of III-V solar cells contains several additional layers. On the top, a **window layer** is added in order to reduce recombination losses by reflecting the minority carriers. It consists of a high bandgap material, usually in $Al_xGa_{1-x}As$ with x> 0.6 % or GaInP. In n-type base structures, the use of AlInP window has also been studied[207]. As AlGaAs is known to be rapidly oxidized, a oxidation-barrier must be added when used as a window layer. Also, on top of the window layer, a so-called "**cap layer**" is added. It is the contact layer made of a highly doped GaAs layer that will help forming good ohmic contact with the metal. This contact layer often serves as an oxidation barrier. It is etched at the end of the process, before depositing the antireclective coating, as schematized in Figure 5.1.b. However, to avoid the oxidation of the underlying AlGaAs window, those two steps must be performed successively. In our case we added a thin (10 nm) transparent GaInP layer, in case the two steps cannot be done at the same time, as it has been previously experimented in the lab[92]. At the back of the solar cell is added a **back surface field** layer (BSF), which, as the window layer, is inserted in order to reflect the minority carriers at the back and thus avoid their recombination in the thick GaAs substrate.

**a)**




**b)**

| Layer # | Layer type | Material | Thickness (nm) | Dopant ($at.cm^{-3}$) | Type |
|---|---|---|---|---|---|
| 7 | Cap layer | GaAs | 50 | Zn $5.10^{18}$ | **p** |
| 6 | Window | InGaP | 10 | Zn $2.10^{18}$ | **p** |
| 5 | | $Al_{0.6}Ga_{0.4}As$ | 30 | | |
| 4 | Emitter | $Al_{0.22}Ga_{0.78}As$ | 100 | Zn $2.10^{18}$ | **p** |
| 3 | Base | $Al_{0.22}Ga_{0.78}As$ | 2000 | Si $1.10^{17}$ | **n** |
| 2 | BSF | $Al_{0.6}Ga_{0.4}As$ | 150 | Si $2.10^{18}$ | **n** |
| 1 | Buffer | GaAs | 500 | $2.10^{18}$ | **n** |
| 0 | Substrate | GaAs | | $2.10^{18}$ | **n** |

**Figure 5.2 - a) Complete structure of the tandem solar cell b) Al0.22Ga0.78As solar cell structure grown by MOVPE on GaAs substrate**

## V.1.2. Grid design

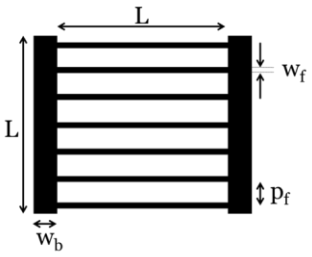
Designing a metallic grid for a III-V cell was another step of the process flow elaboration. Using the same mask as for Si cells was not conceivable, for two reasons : first because we are not working on quarters of 4 inches wafers anymore but on 2 inches, and second because the density and disposition of the fingers have to be changed. Indeed, carrier diffusion length in GaAs is much smaller than in Si. In order to collect these carriers, the fingers must be placed closer. We thus had to define a new design, and fabricate a dedicated lithographic mask. Grid designs found in literature of III-V solar cells[208,209] are composed of two thick busbars connected with thin fingers, as shown in Figure 5.3. Several parameters can be varied: the cell designated area ($L^2$), the finger pitch $p_f$, the finger width $w_f$, and the busbar width $w_b$. The most relevant parameter is the density of metallic fingers, linked to $p_f$ and $w_f$. On the one hand, we need a high contact density because it reduces the impact of the surface sheet resistance, and thus allows more current to flow. On the other hand, as the metal is not transparent, the shading will be more important and fewer photons will reach the semiconductor and be absorbed. Therefore, a trade-off had to be found between a low sheet resistance and a low shading.

According to Steiner et. al.[209], the choice and optimization of the grid for solar cells working at low concentration is not as crucial as in high concentration applications. As our project is focuses on low concentration applications, the need of optimization is not that critical, but we took care of choosing relevant parameters. We converged on 6 different designs. We chose to design square cells, with two different cell areas: 1x1$cm^2$ and 0.5x0.5 $cm^2$. For each size, the fingers were separated by a pitch of 100 µm, 200 µm and 300 µm, resulting on shading factors of 10%, 5% and 3.3%, respectively. Tables in Figure 5.3 sum up the parameters of each 3 pattern. The busbar width was fixed in order to be thick enough to ensure an easy manipulation of the probes while doing the

measurements. We picked $w_b$ = 600 µm. The finger width was fixed at 10 µm, and we varied the finger pitch, linked to the shading factor.

a)

| Fixed parameters | Value |
|---|---|
| Finger width ($w_f$) | 10 µm |
| Busbar width ($w_b$) | 600 µm |
| Cell length (L) | 1 cm & 0.5 cm |




| Pattern | Finger pitch ($p_f$) | Shading factor |
|---|---|---|
| A | 100 µm | 10 % |
| B | 200 µm | 5 % |
| C | 300 µm | 3.3 % |

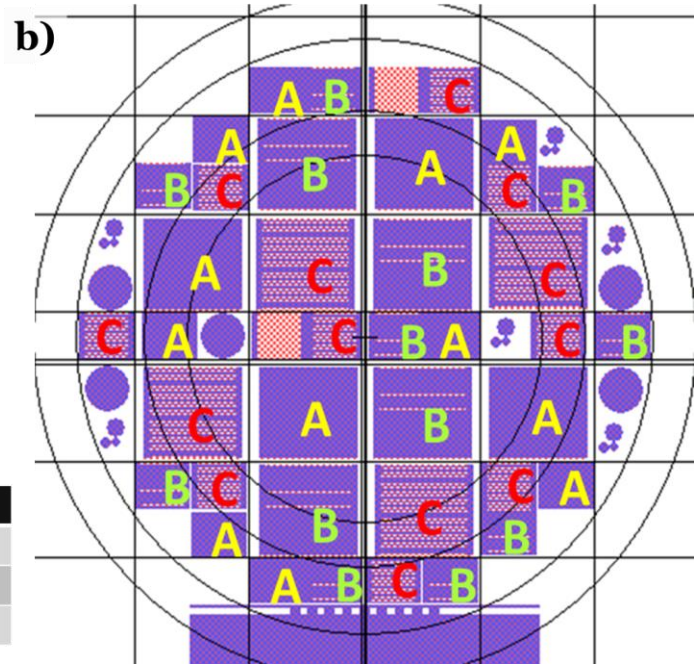



**Figure 5.3- a) 3 different patterns with various busbars and finger dimensions of the tested cells. b) L-edit screenshot of the grid disposition on a 3 inch. wafer. The 3 configurations are tested on 1x1 cm2 and 0.5x0.5cm$^2$ cells.**

Consequently, we chose 3 design patterns named A, B and C in Figure 5.3.*a.*, each one used on large cells (1x1 cm²) and small cells (0.5x0.5 cm²), resulting in 6 different designs. Using L-edit software to design the lithographic mask, we distributed these 6 designs on a 3 inch. wafer. We decided to define a zone of 5 mm around the wafer without any cell, so as to avoid uncertainties due to edge effects (spin-coating inhomogeneity, clamps holding the wafer during metallization etc...). We also tried to arrange it so as to have as many cells as possible on a 2 inch. wafer. Indeed, we anticipate the fact that this mask could be used by other users in the lab, working on other materials on 2 inch. wafers. Each design has been repeated and placed in different zones of the wafer (center, border...). This ensures significant statistics to check reproducibility and deduce some trends. We also took care of making the mask as symmetrical as possible, to anticipate eventual cleavage of the wafer during the process flow. The final distribution is shown in Figure 5.3.b.: the large cells (1x1 cm²) are repeated 4 times each, and the small ones (0.5x0.5 cm²) between 8 and 9 times each, resulting in 40 different cells to be tested on the wafer.

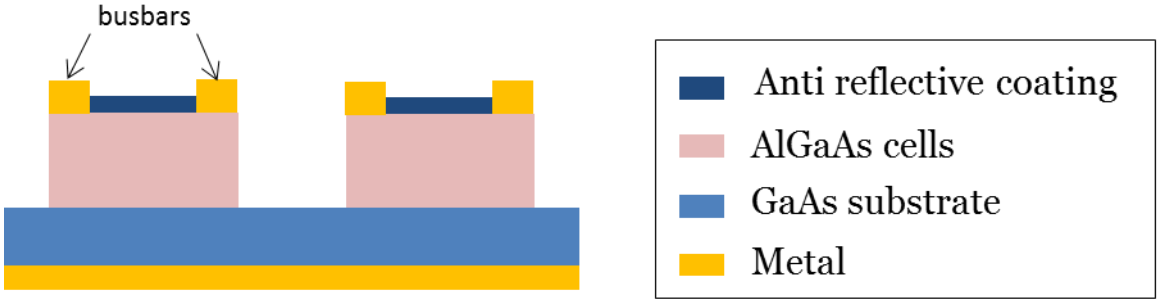



**Figure 5.4 - Cross-section schematic of the targeted device after process**

In this part, we chose to test 6 different designs: 2 cell sizes along with 3 different shading factors. We disposed it on a full 3 inches wafer so as to be able to measure all the cells separately on the same full wafer, facilitating the handling during ***J-V*** measurements. The next section will gives more details on the process flow and the 2 masks designed for the required lithographic steps.

### V.1.3. Photomask set design

The design of the masks requires not only the design of the grid patterns, but also a design of a full set of masks that could lead from the structure grown *(*Figure 5.2*)* to the targeted device. Figure 5.4 shows a cross-section schematic of the required final devices on a wafer, where two neighbor solar cells are represented. In order to avoid some heavy steps of cleavage and wire bonding of the 40 cells, we decide to maintain all the cells on the same wafer. We thus need to separate them electrically. To do so, a step of mesa etching will be needed, thus requiring a specific lithographic mask. This mask consists of squares of the same size than the cell, protecting the whole cell.

Also, an anti-reflective coating (ARC) needs to be deposited on top of the semi-conductor. However, we must protect the busbars from this deposition, to be able to contact the probes for the I-V measurements. Depositing the ARC at the end of the process would require a third lithographic step to protect the busbars. Here we think of another way to avoid this lithographic step, and use the grid definition mask for both patterning the metal and the ARC. To do so, instead of patterning the metal by lift-off technique, we propose to use ion beam etching (IBE) of the metal, and deposit the ARC on top of the protecting resist after the metal etching.
Thus, only two lithographic masks are designed. One, that we call “grid”, defines the busbars and fingers, and one, pictured in Figure 5.5 called “mesa”, defines the separated cells.

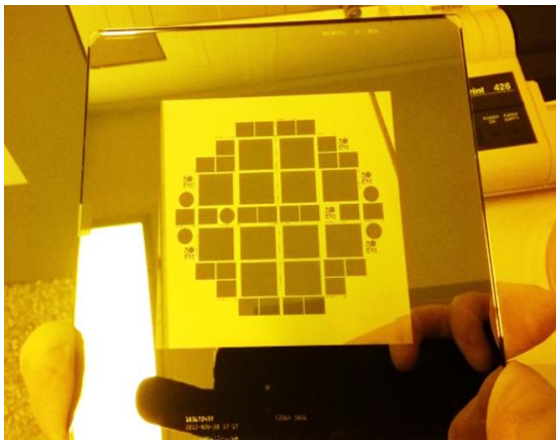


**Figure 5.5 - Picture of the lithographic mask used to define the mesa etching pattern**

### V.1.4. Fabrication

Here we describe the details of the process flow of our AlGaAs solar cell. Note that in the next section that deals with the processing after bonding (V.2.), this process flow will be simplified in order to avoid some critical steps. Two main lithographic steps are performed: we used a first mask to deposit the metal and etch by ICP the III-V between the separated cells. The second one deals with the definition of the busbars and fingers previously designed. The cross-section representations of the first 11 steps of the process flow are presented in Figure 5.6. Step (1) is the epitaxial growth of the AlGaAs solar cell. The detailed structure grown by MOVPE was presented earlier in Figure 5.2.b. To simplify the schematics, we only represent one block for the solar cell, and one layer corresponding to the cap layer. During step (2), the front contact metallization: Pt (150 nm) /Au

(250 nm) is deposited on the whole surface of the wafer by sputtering. A 2 minutes sputtering with Ar plasma was performed in-situ before the metal deposition to remove the oxide and help adhesion of the metal on the semi-conductor. Step (3) is the deposition of 700 nm of $SiO_2$ on the full wafer. This $SiO_2$ will act as a mask for further ICP etching of the mesa (i.e. about 3 µm of AlGaAs and GaAs-family compounds). Then, this $SiO_2$ mask needs to be patterned. To do so, a lithographic step is needed. Step (4) is the spin-coating of the positive resist, (5) the insolation of the resist through the mask level "mesa", and (6) the opening of the resist where it has been insolated. Then, the $SiO_2$ mask is etched by RIE during step (7), using fluorine compounds in the plasma. $SiO_2$ is etched where it is not protected by the resist. In-situ reflectometry is used to monitor the etching of the $SiO_2$ layer. Step (8) consists of removing the metal by Ion Beam Etching (IBE) with Ar plasma. This technique is not selective, we should thus control the etch rate.

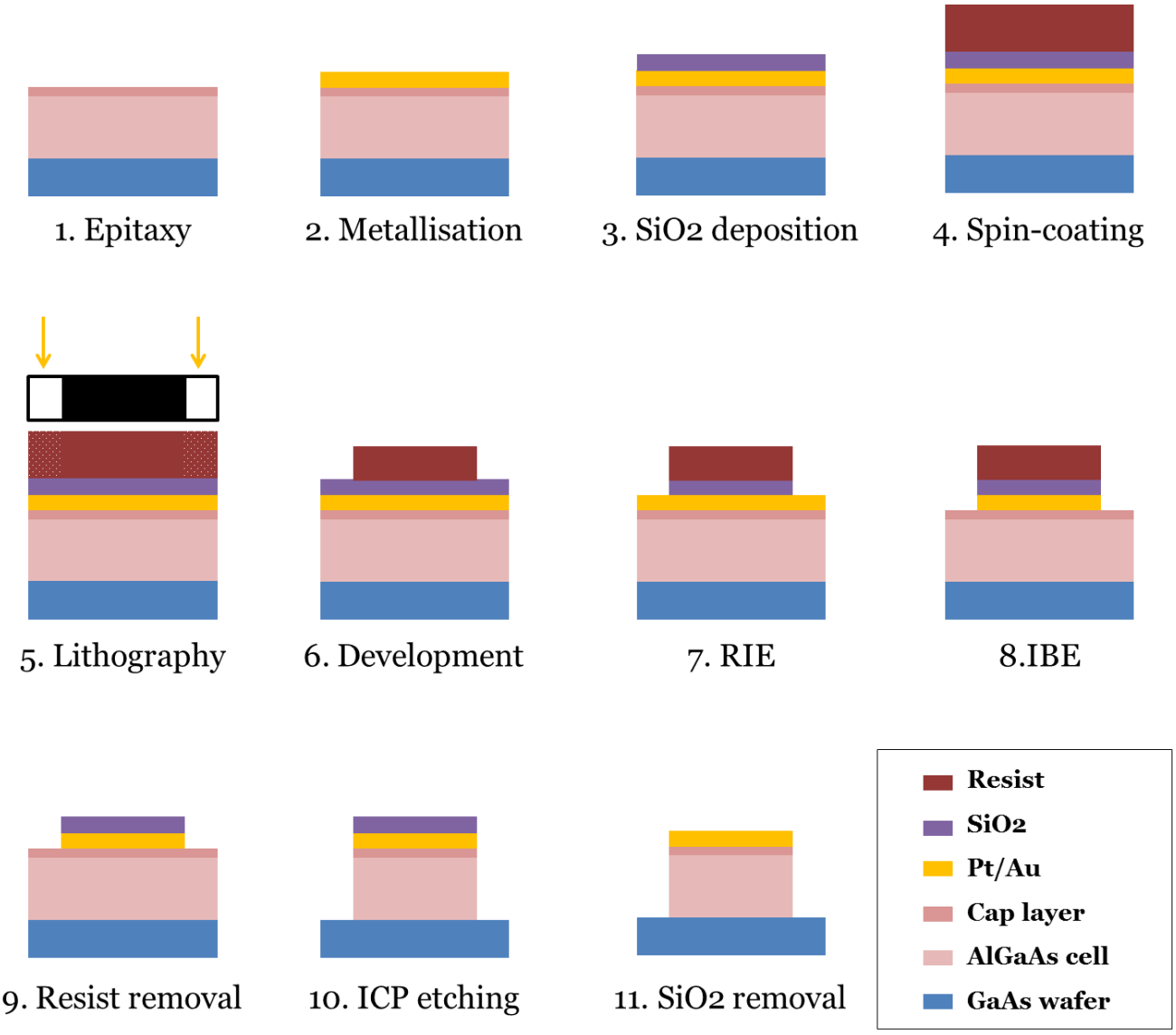



**Figure 5.6 - Cross section schematics of the solar cell process flow detailing the 11 first steps required for the mesa etching**

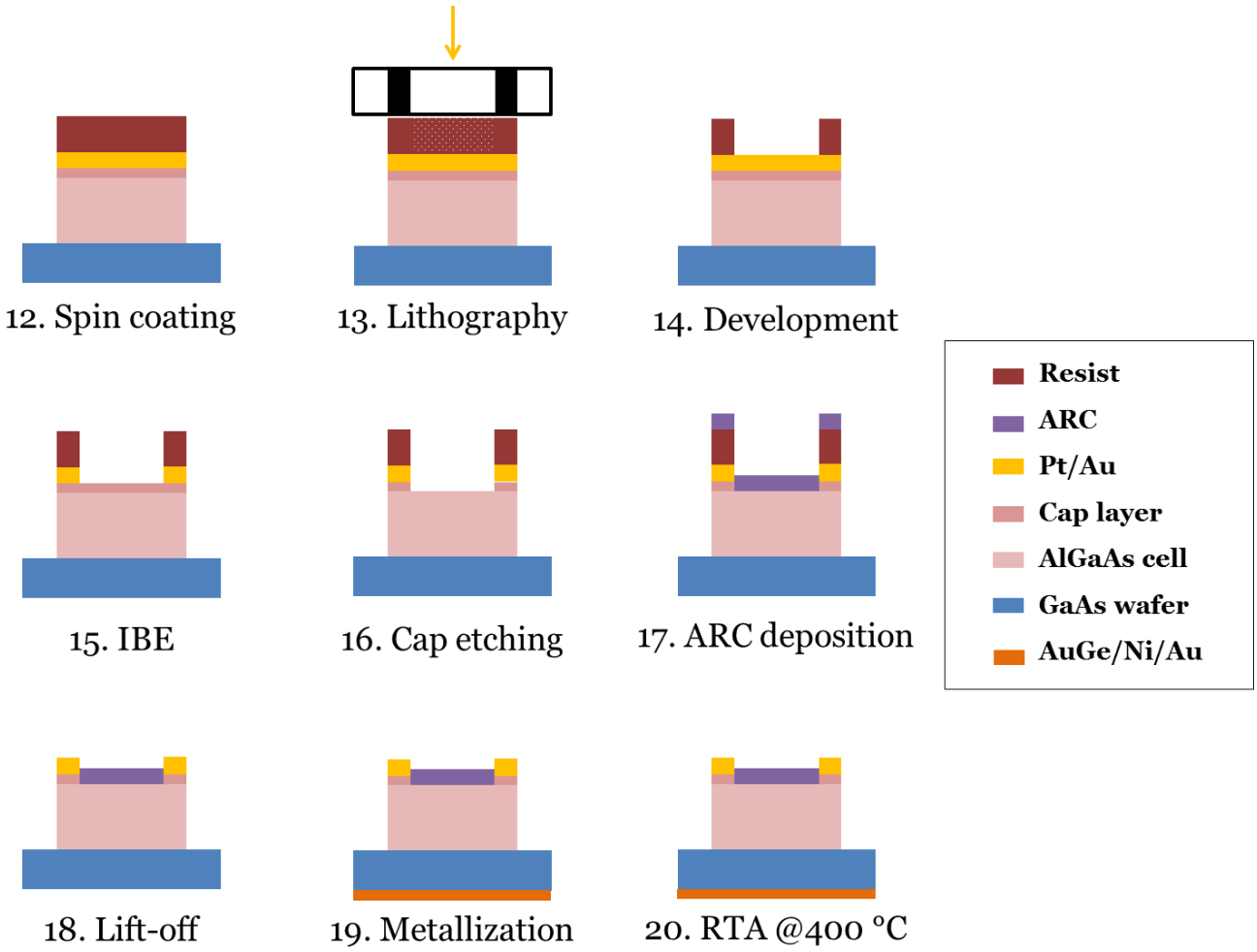



**Figure 5.7 - Cross section schematics of the solar cell process flow: grid definition and ARC deposition**

A slight under-etch at this stage is not that critical, because the underlying III-V layer is also aimed to be etched by ICP. During step (9) we remove the resist. The $SiO_2$ is now protecting the semi-conductor from ICP etching in the area that must not be etched. Step (10) is the ICP plasma etching. The plasma is composed of chlorine compounds and will etch all the III-V materials. In-situ reflectometry is used again to know when all the layers are etched and stop the plasma when we reach the substrate.

Now that the cells are electrically separated, we need to define the busbars and fingers into the metal, etch the cap layer and deposit the an anti-reflective coating. To do so, a new lithographic step is required (12, 13, 14) in order to protect the metal where the busbars and fingers must remain. To simplify the schematics, only the two busbars are represented on Figure 5.7. The metal is then etched by IBE (15). This time, the selectivity is more crucial. The cap layer is only 50 nm thick. We can etch a few nanometers of the cap layer, but must absolutely not reach the underlying GaInP layer that is only 10 nm thick.

The next step is the cap layer etching. This ~50 nm thick layer is etched chemically. As the underlying layer is the 10 nm GaInP oxidation barrier, we use a selective mixture that etches GaAs and not GaInP. Phosphoride compounds can only be etched by mixtures containing HCl[210]. Thus, we used in this case a mixture of $H_2O/H_3PO_4/H_2O$, that attacks the GaAs but does not affect the

underlying GaInP. The next step (17) is to deposit an anti-reflective coating. We deposit $SiO_2/TiO_2$ on top of the cell, and on top of the resist. Deeping the whole wafer into acetone enables the lift-off of the resist together with the ARC on top of the metal grids (18). Finally, the back contact metallization with AuGe/Ni/Au is performed (19) followed by a 400 °C Rapid Thermal Annealing for 1 mn.

## V.1.5. Solar cell characteristics

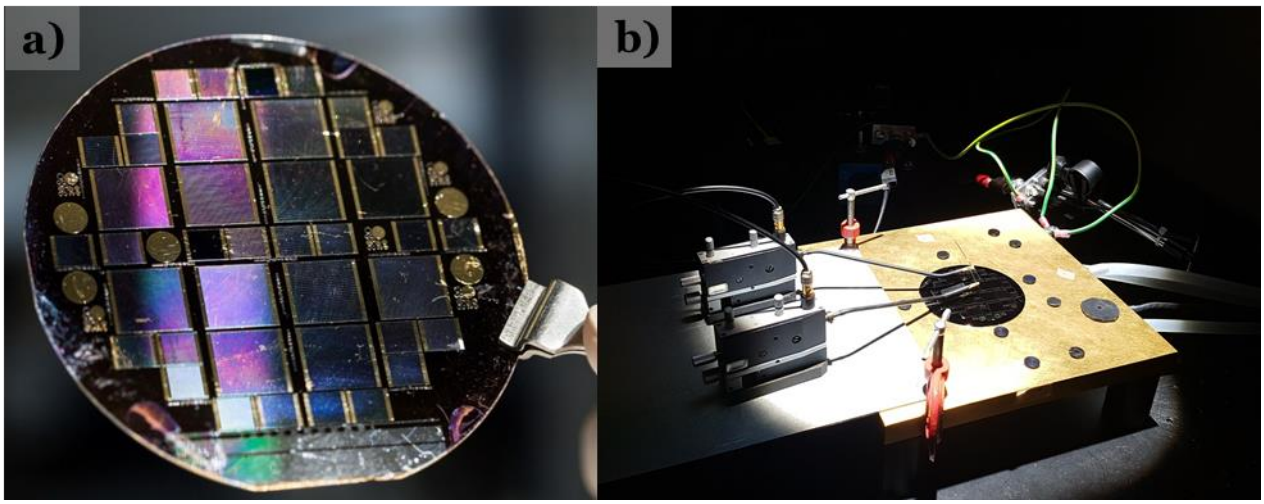
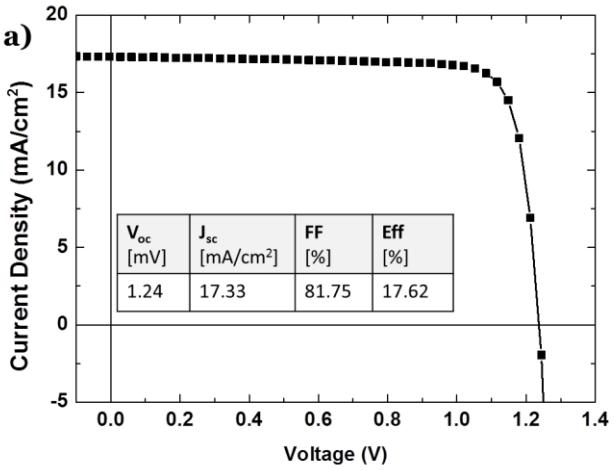



**Figure 5.9 - a) Picture of the wafer after processing, b) picture of the measurement under AM1.5G spectrum**

The $Al_{0.22}Ga_{0.78}As$ solar cells have been fabricated in clean rooms using the process flow described in the previous part. The resulting wafer containing the 40 different cells and a few test diodes is pictured in Figure 5.9.*a*. Keeping all the cells on the same wafer facilitated the handling and the measurement of each cell. A picture of the solar cell during the measurement under solar simulator is shown on Figure 5.9.b. The two front probes are placed on the two opposite busbars of each cell. The back contact is taken on the back conductive plate, and all the cells can be measured

a)




b)

| % Al | Voc [V] | Jsc [mA/cm²] | FF [%] | Eff [%] |
|---|---|---|---|---|
| 0 | 1,04 | 21,2 | 82,7 | 18,25 |
| 5 | 1,09 | 19,8 | 83,4 | 17,98 |
| 20 | 1,25 | 15,8 | 85,9 | 16,91 |
| 22 | 1,24 | 17,33 | 81,75 | 17,62 |
| 27 | 1,34 | 13,7 | 86,8 | 15,89 |
| 37 | 1,40 | 10,4 | 85,8 | 12,43 |

**Figure 5.8 - a) J-V characteristics of the Al0.22Ga0.78As solar cell, b) detailed characteristics of the same cell as compared with results from Heckelmann *et al.* [207]**

by just moving the front probes from one cell to another.

The ***J-V*** curve under 1 sun illumination of the best AlGaAs solar cell is shown on Figure 5.5.a. The device exhibits a good $V_{oc}$ of 1.24 V, consistent with the bandgap of the solar cell (~1.74eV). We measured a $J_{sc}$ of 17.33 mA/cm² and a fill factor of 81.75%, leading to conversion efficiency under AMG1.5 of 17.62 %. Heckelmann *et al.*[207] deeply studied the performances of AlGaAs solar cell grown by MOVPE, and showed the influence of Al content. They reported the best AlGaAs solar cells in literature (see Table 5.1). Their structure consists of a 2.5 µm p-type base in $Al_xGa_{1-x}As$ with x ranging from 0 to 37 %. They used an AlInP window layer. Even if our structures differ in their polarity, it is relevant to compare our results with theirs. Figure 5.5.b. summarizes the performances of their solar cells as a function of the Al content, as compared to the AlGaAs cell of this work with 22% of Al. Our solar cell exhibits a better overall efficiency according to the amount of Al that we have. This is mainly explained by a much better $J_{sc}$ than them: we find a $J_{sc}$ of 17.33 A/cm² instead of 15.8 A/cm² for their $Al_{0.20}Ga_{0.8}As$ solar cell. This is explained by the fact that their solar cells do not comprise an anti-reflective coating, whereas we added a $SiO_2/TiO_2$ ARC to enhance the current. However our solar cells have a fill factor of 81.75 % whereas theirs are above 85 %. Also, our $V_{OC}$ is slightly lower for the considering bandgap. It can be attributed to the non-optimized window, especially to the GaInP layer that could induce more recombination in this layer.

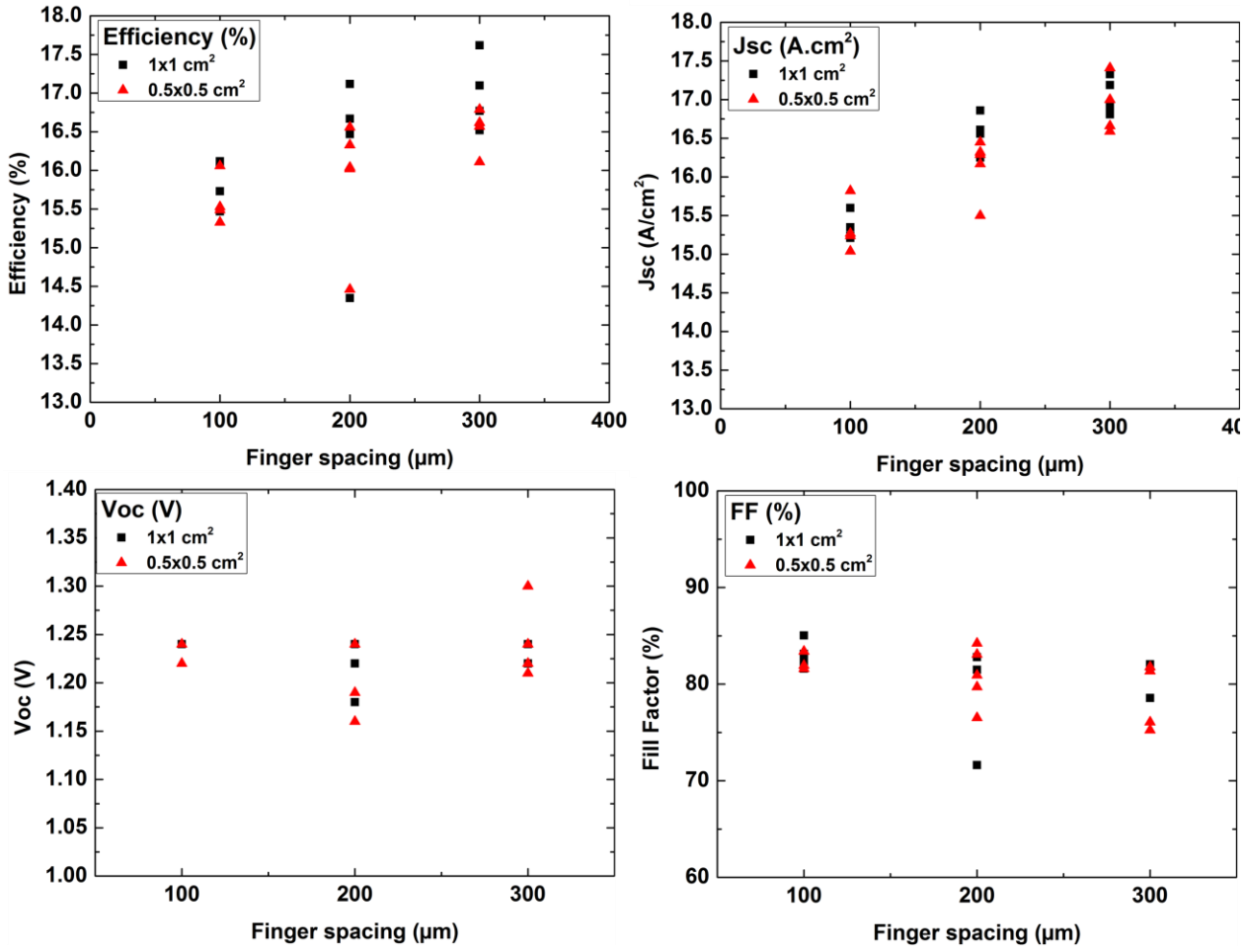



**Figure 5.10 - Solar cell parameters as a function of the finger spacing. Black squares correspond to the large cells (1x1 cm²) and red triangles to the small ones (0.5x0.5 cm²)**

We can nevertheless conclude that the AlGaAs solar cell grown by MOVPE and processed in our clean rooms exhibits very good performances. We reached a conversion efficiency of 17.62 % for the best solar cell, corresponding to a 1x1 $cm^2$ cell with a shading factor of 3.3 %. Now, if we consider all the different cells measured on the same wafer, the efficiencies range from 15 % to 17.6 %. The overall parameters of the cells are summarized in Figure 5.10. We plot the efficiency, $J_{sc}$, $V_{oc}$ and FF as a function of the finger spacing. Black squares correspond to the big cells (1x1 $cm^2$) and red triangles to the small ones (0.5x0.5 $cm^2$). We notice that the $J_{sc}$ is strongly impacted by the distribution of fingers. The smaller the shading factor (i.e. the more spaced are the fingers), the higher $J_{sc}$. This is obviously explained by the fact that more photons reach the semi-conductor and can consequently be absorbed. We notice that the FF is slightly impacted. It decreases while increasing the finger spacing. This is attributed to the increasing series resistances. The $V_{oc}$ remains not impacted by the variation of the shading factor. The overall performances show that the best efficiencies are achieved for finger spacing of 300 µm, corresponding to a shading factor of 3.3 %.

To conclude this part, the mask designed especially for solar cell application has been used to perform the process flow on the $Al_{0.22}Ga_{0.78}As$ structure that we grew by MOVPE. The solar cells exhibited excellent performances with record efficiency of 17.6 %. This result validates not only the good quality of the material grown, but also the numerous steps of the process flow that have been realized. Further optimization of the grid pattern and of the window layer could be done in order to enhance the efficiency. We could also further reduce the shading factor by increasing the finger spacing. However, we can settle for this result that already meets the requirements to have a working Si(Ge)/AlGaAs tandem solar cell. We thus acquired the basic expertise to process good III-V solar cells, and can now confidently move on to the last technological challenge: the bonding of the tandem solar cell.

# V.2. Bonding of a III-V solar cell

## V.2.1. Bonding requirements

There are numerous bonding techniques that are used in order to bond two materials[211]. In this part, we do not pretend to find the best bonding technique for the processing of our tandem solar cell, but we need to find a technique that could be available in our clean rooms, without a full development of a new field, in order to do a proof of concept of the tandem device. The bonding that is required is only a mechanical bonding in order to handle physically the tandem cell after GaAs substrate removal. As our active layer thickness will not exceed 15 µm, it requires a host carrier to handle the wafer during the further processing of the solar cells. However, it must meet some expectations specific to our tandem device, and be compatible with all the following technological steps required to complete the tandem solar cell (metallization, mesa definition etc…).

As it was introduced in Chapter I.4.2. (p 17) the addition of a light-trapping scheme on the bottom Si cell would highly enhance the absorption for a fixed Si thickness[52]. The feasibility of such light-trapping has already been studied on the PECVD epitaxial Si[212,213], and must be considered for further improvement of the tandem solar cell. Thus, the bonding technique should not require a flat surface with crucial surface preparation (it is the case for surface-activated direct wafer bonding[48]), so as to be compatible with the possibility of texturing the epitaxial silicon surface. Also, the

previous chapters helped us to anticipate a few technological issues: first, the tandem solar cell should not be heated at temperatures higher than 300 °C, to avoid the blistering of the Si that has been observed in Chapter II.2.2 (p. 37). It was also important that the bonding could be compatible with the process flow. Indeed, it should be resistant to the numerous process steps including the chemical etching, the aceton lift-off, and possibly the PECVD $SiO_2$ deposition at 250 °C, and the dry etch steps. Also, (and most importantly), it should not add any contamination to the process tools of the clean rooms, that are also used for production matters. Any unknown contamination could be very critical for the good functioning of the process clean rooms for other applications.

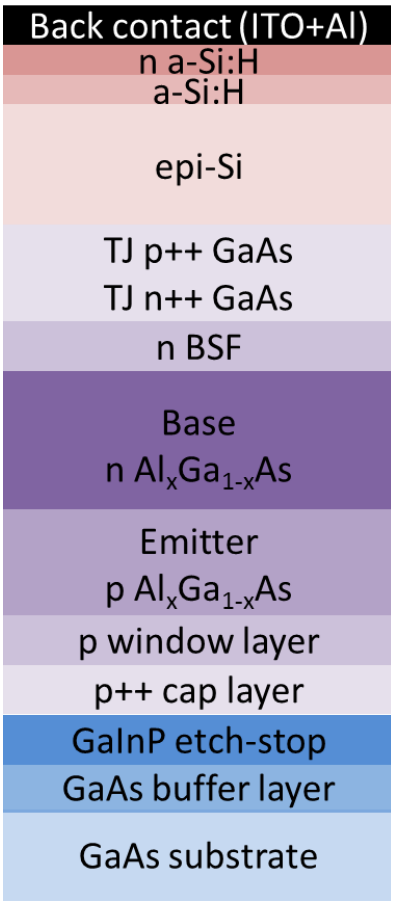



**Figure 5.11 - Structure of the tandem device before bonding**

To account for these requirements, we chose a silicon substrate as a host. Using a glass or cheap flexible substrate could be feasible; however, for our proof-of-concept it was easier to settle and to test in our process reactors with a Si substrate. After several discussions with the process experts from III-V Lab, and bonding experts from partner laboratories Thales Research & Technology, CNRS-$C_2N$ and CEA-Leti, we could gather several considered bonding techniques that are shown in Table 5.2 with their advantages and drawbacks.

Actually, most of the possible bonding techniques were not available, nor easy to settle in the clean rooms. Some techniques could have been outsourced by suppliers, however many questions were remaining, such as the possible diffusion of the metal used. The structure of the tandem device that we want to bond is presented in Figure 5.11. Literature report a technique to reuse GaAs substrate by epitaxial lift-off[214–216]. It uses a sacrificial layer in AlAs, which is selectively etched by HF. The development of such substrate reuse was not the purpose of this work. Thus, for a proof of concept, we chose to simplify the process, and to etch totally the GaAs substrate. Consequently, we inserted a etch-stop in GaInP in the structure, so as to enable a selective chemical etching of the GaAs substrate.

**Table 5.2 - Review of a few possible bonding techniques with its advantages and drawbacks**

| Bonding technique | Pros | Cons |
|---|---|---|
| **Surface activated bonding** | - Low temperature process | - Flat surface required<br>- No equipment available |
| **Eutectic bonding** | - Provides conductive interface with host substrate | - Temperatures > 300 °C<br>- Risks of metal diffusion in Si<br>- To be outsourced |
| **Ultraviolet adhesive** | - Low temperature process | - Only on glass host substrate |
| **Electroplating** | - No bonding (thick metal deposition)<br>- Conductive contact | - Not available |
| **BCB** | - Low temperature process<br>- Compatible with further process steps<br>- Available | - To be mastered on full 2 inch' wafers |

## V.2.2. Bonding with BCB

The bonding technique that has been chosen satisfies the temperature requirements of our device, and is also compatible with the use of all the clean room process tools needed for the following process flow. We used a bonding with a polymer: the cycloten 3022-46 (commercialized by DOW Chemicals), which is a part of the polymer family called BCB (Benzocyclobutene). The process had been developed internally in Thales teams, and the details can be found in the following theses[217,218]. I therefore would like to thank Gaëlle Lehoucq and Raphaël Aubry for giving me the opportunity to access to their know-how and equipment in this field. The process steps of the bonding are shown in Figure 5.12. (a) After cleaning the substrate surface with aceton and rinsing it with propanol to remove any possible remaining dust, the BCB is spin-coated on both GaAs and Si substrates after the use of an adhesion promoter. Then, the two substrates are placed in a vacuum chamber during 5 minutes in order to eliminate the bubbles that could have been created in the BCB during the spin-coating step. Afterwards (b), the two substrates are contacted together. This step is performed manually, thus needs a particular attention to align the two substrates. Finally, the two wafers are bonded under a mechanical press and placed on a heating plate in order to anneal the BCB so as to crystallize it. This is achieved in two stages: a first stage at 180°C during 5 hours, and a second one around 275 °C during 45 minutes, used to crystallize BCB. After this step, the remaining BCB must be removed by RIE (c). Indeed, it may have flown around and above the wafers due to the press.

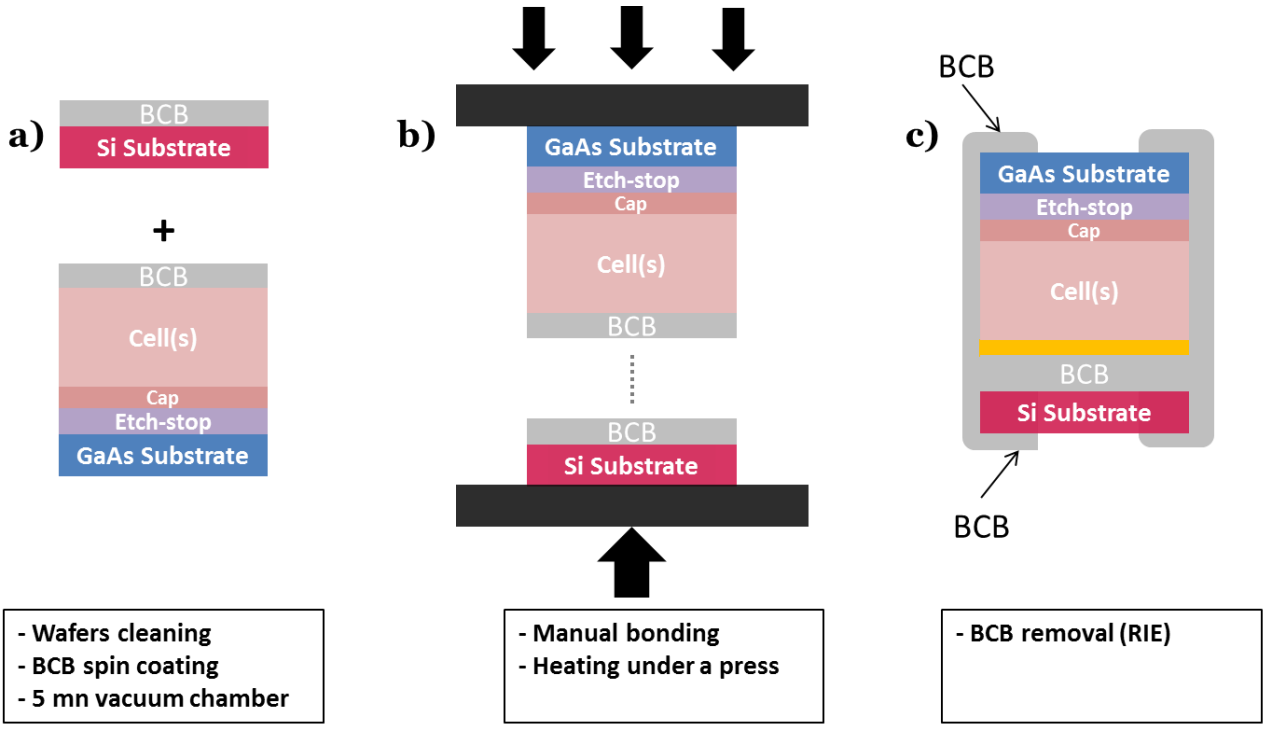



**Figure 5.12- Schematics of the main technological steps of bonding with BCB**

Then, the GaAs substrate is removed, in order to reveal the III-V sub-cell. To do so, we used chemical etching. A selective mixture over GaInP is used: $H_2O/H_2O_2/H_2SO_4$. The etch rate is about 5 µm/mn, and the substrate can be removed in about 1 hour of etching. One of the main issues of this step is to achieve an homogeneous etching on the whole wafer. Indeed, the selectivity with GaInP is

high[219] (about 150:1), but the etch-stop layer is found to be affected by the chemicals when exposed too long, as it will be shown in the next experimental part. The end of the substrate etching is determined visually. Indeed, the back surface of the wafer in non-polished. As soon at the etch-stop layer is reached, the surface become mirror-like. This will be illustrated later in Figure 5.15.a: at the center of the sample, the etch stop is reached (thus the substrate removed), and at the surrounding, it is still rough, which means that the substrate is not totally removed. Afterward, the GaInP etch-stop is etched with a good selectivity on GaAs[220] using $HCl:H_3PO_4$.

As the bonding press was only designed for 2 inch" wafers, we redesigned a lithographic mask adapted for 2 inches, using the same patterns as presented in part V.1.3. (p. 126), but we only kept the smaller cells (0.5x0.5 $cm^2$). Also, the very first bonding tries made us realize that the process flow should be simplified. Indeed, as it will be detailed, we faced issues at each plasma process, each lithographic step, and resist lift-off. Thus, we decided to use a less optimized process flow, which would induce less critical material issues. In particular, we did not deposit the anti-reflective coating, and performed a wet mesa etching instead of ICP.

## V.2.2. Bonding of an inverted GaAs solar cell

This part presents several experimental steps performed to prove the feasibility of bonding full 2 inches wafer. Many issues have been faced, and by several iterations we found ways of avoiding them. Before bonding a tandem solar cell with both Si and AlGaAs cells, we decided to test the bonding process with a single GaAs solar cell, inversely grown. The structure is presented in Figure 5.13.a. It is actually the same as in Figure 5.2.b, but grown invertly with an additional GaInP etch-stop. Because of some unexpected issues due to an empty TMAl bubbler, the base and emitter of these cells are made of GaAs instead of AlGaAs (the BSF and window layers remain in AlGaAs). The structure after processing is presented in Figure 5.13.b. We decided not to add any anti-reflective layer in order to simplify the process. Instead of defining the grid metal by ion beam etching, we defined it by using a lift-off process, and performed a chemical mesa etching instead of a dry one, which suppresses the steps that were dedicated to the deposition of the $SiO_2$ hard mask. Thus, the simplified solar cell process including the bonding is presented inFigure 5.13.c. and is designed for single but also tandem solar cells. After the epitaxy of the inverted solar cell(s) (1), we deposited the metal (2) (here, Ti/Pt/Au on top of the n-doped GaAs, and ITO+Al in case of the tandem cell). Note that no annealing has been performed. Then, the cell was bonded to a Si substrate using BCB, and the BCB that had overflowed on the wafers was removed by RIE (step 3, that was detailed in Figure 5.12). After, the GaAs substrate and the etch-stop are removed (4-5). At this stage, the solar cell is like a standard upright solar cell. A first lithography step is performed to open the grid design (6) followed by the front contact metallization of Pt/Au on p-GaAs cap layer (7) and the metal lift-off (8). Then, a second lithographic step defines the mesa (9) that is etched chemically (10). The remaining resist is then removed in acetone (11), and finally the cap layer is chemically etched.

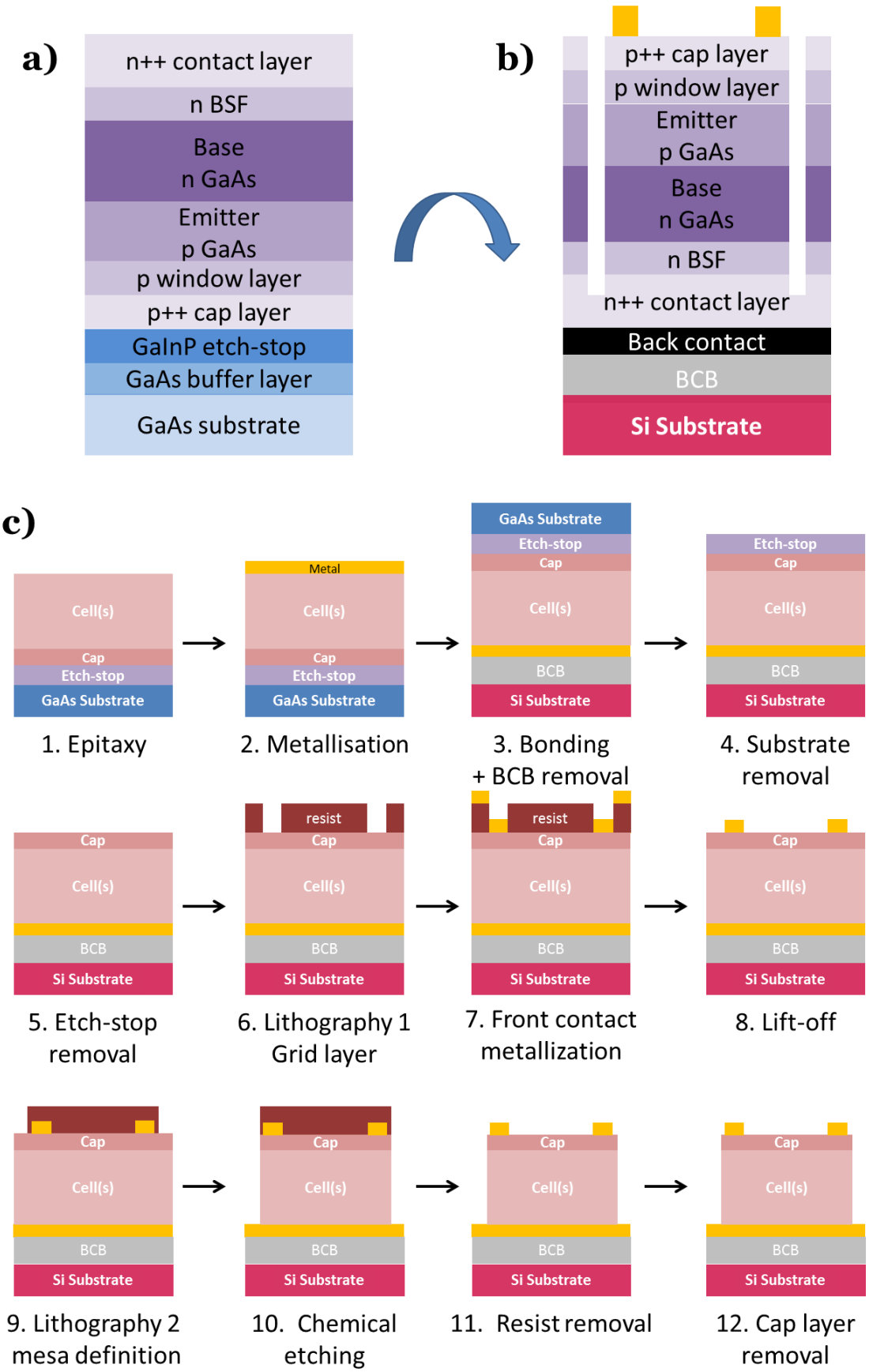



**Figure 5.13 - Structure of a single GaAs (a) before and (b) after bonding an processing. c) Cross-section schematics of the process flow of inverted single or tandem solar cells**

### V.2.2.1. Process flow: issues and suggested improvements

Several inverted 2 inch wafers have been bonded, and we could finish the process until obtaining functioning solar cels. In this part we will present separately some of the crucial steps, explaining the issues that have been faced during the several bonding attempts, and the pathways to avoid it.

***Steps 3 and 4: BCB removal and substrate removal***

During the first attempts of bonding GaAs on a Si wafer, we pointed out the importance of performing properly the removal of the BCB that have overflowed on the wafer during the bonding and annealing process. Figure 5.14.a. a ¼ GaAs wafer bonded on top of a ¼ 3 inch. Si wafer, right after the step of GaAs substrate removal. The material we can observe on the borders (on top and on the right) is BCB that is present in the wafer side walls. The surrounded part corresponds to somewhere where the BCB was remaining on top of the GaAs wafer. We see that it actually has acted as a hard mask for the substrate removal. This must be totally avoided because, not only we lose some part of the semiconductor, but also it could prevent us from performing the following process steps. Indeed, with this zone that contains a material that is more than 250 µm high than the rest of the sample, it is not possible anymore to perform a lithographic step, that needs to contact the wafer surface with the lithographic mask and create a vacuum. This would prevent the vacuum from being made, and will probably scratch our mask or break the wafer. Another unwanted feature that can be observed is the formation of long cracks on the GaAs stack.

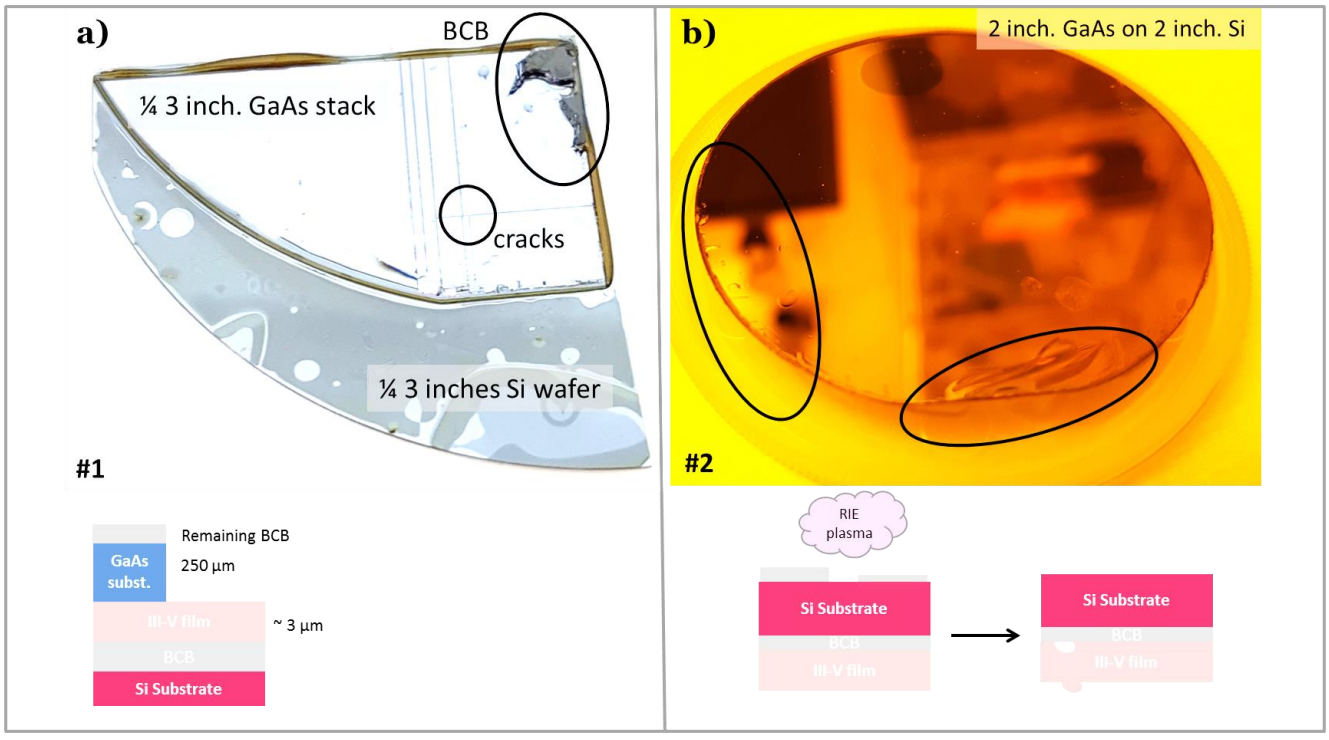



**Figure 5.14 - a) Picture a wafer #1 after substrate removal with some remaining BCB, b) picture of wafer #2 after substrate removal followed by a RIE**

Those are due to the presence of bubbles that have initiated strain in the layers. This strain has been relaxed during the thick GaAs substrate removal. As an indication, on the bottom left side of the images, we gave a number to the wafer that is processed and discussed. Thus, for the next attempt

(wafer #2), we performed the RIE cleaning step, but prior to it, we made an aceton cleaning that helped removing the bigger parts of BCB on top of the GaAs wafer. After this step, the substrate removal happened without cracks nor BCB masking. However, we did not remove the BCB on the Si part, and it revealed to be an issue in the next step: this back relief prevented to make the vacuum in the lithographic tool. Thus, we performed afterwards the RIE plasma with the Si substrate on top. After this step, the III-V film was found as seen in the picture on Figure 5.14.b, where one can see a detachment of the film in some part of the substrate. Thus, the step of BCB removal after the bonding is primordial, and is required on both GaAs and Si sides.

***Substrate removal + etch-stop removal***

During the substrate removal, the wafer was placed vertically into a beaker, under magnetic stirring, aiming at having homogeneous etching of the substrate. Figure 5.15.a and b show pictures of the wafers (2 inches bonded on 2 inches) after 40 and 50 minutes in the chemical solution. After 40 minutes, there is a mirror like area that is appearing in the center of the 2 inch. wafer. It corresponds to the area where the wafer has been fully etched, and the etching has stopped at the surface of the GaInP layer. After 10 more minutes, the mirror-like area has extended. However, there are still some areas at the surrounding where the substrate is not fully etched. For this sample (wafer #3), we waited until 1h10mn of etching to be sure that the whole substrate is etched. However, we could observe that for such long etching time, the GaInP layer had started to react. Some pink and green fringes appeared (hard to distinguish on Figure 5.15, inside the circle). After the etching of GaInP layer with $HCl/H_2SO_4$ chemical mixture the surface had become rough, especially in the area that was the first fully etched. Microscope images of two areas are presented in Figure 5.15.c and d, which correspond to the two yellow crosses in b. Those characterizations have been done further in the process (after metallization and mesa etching). It revealed that the surface contains big defects. The density and size of these defects (larger than 20 μm) are more important in the center (area c) than at the edge of the wafer (area d). Because these defects are bigger than the size of the metallic fingers, we expect to have strong series resistance on the resulting solar cells. Moreover, as these defects appear where the wafer has been over-etched, we would expect to have a hollow. However, profilometer analyses showed it was hills. To have a better insight on the origin of these defects, SEM analyses are presented in Figure 5.15.e. On the left, the mesa has been etched and we reached the back metallization. On the right, we see the III-V layers and the front metal. The defects appear to be hills. We also see that it has acted as a mask for mesa etching in the left part.

Thus, we suppose that, during the substrate etching, some material present in the chemical mixture (probably GaAs substrate flakes), have been redeposited on top of the GaInP. To minimize these effects, it was proposed to change the chemical solution as soon as the etching reaches the GaInP layer. We tested it on wafer #4, and dipped the wafer into a new and clean etching solution with a slightly lower etch rate. It revealed a clean surface without any defects after etch-stop removal. However, for other issues, this inverted solar cell could not be fully processed until a measurable device.

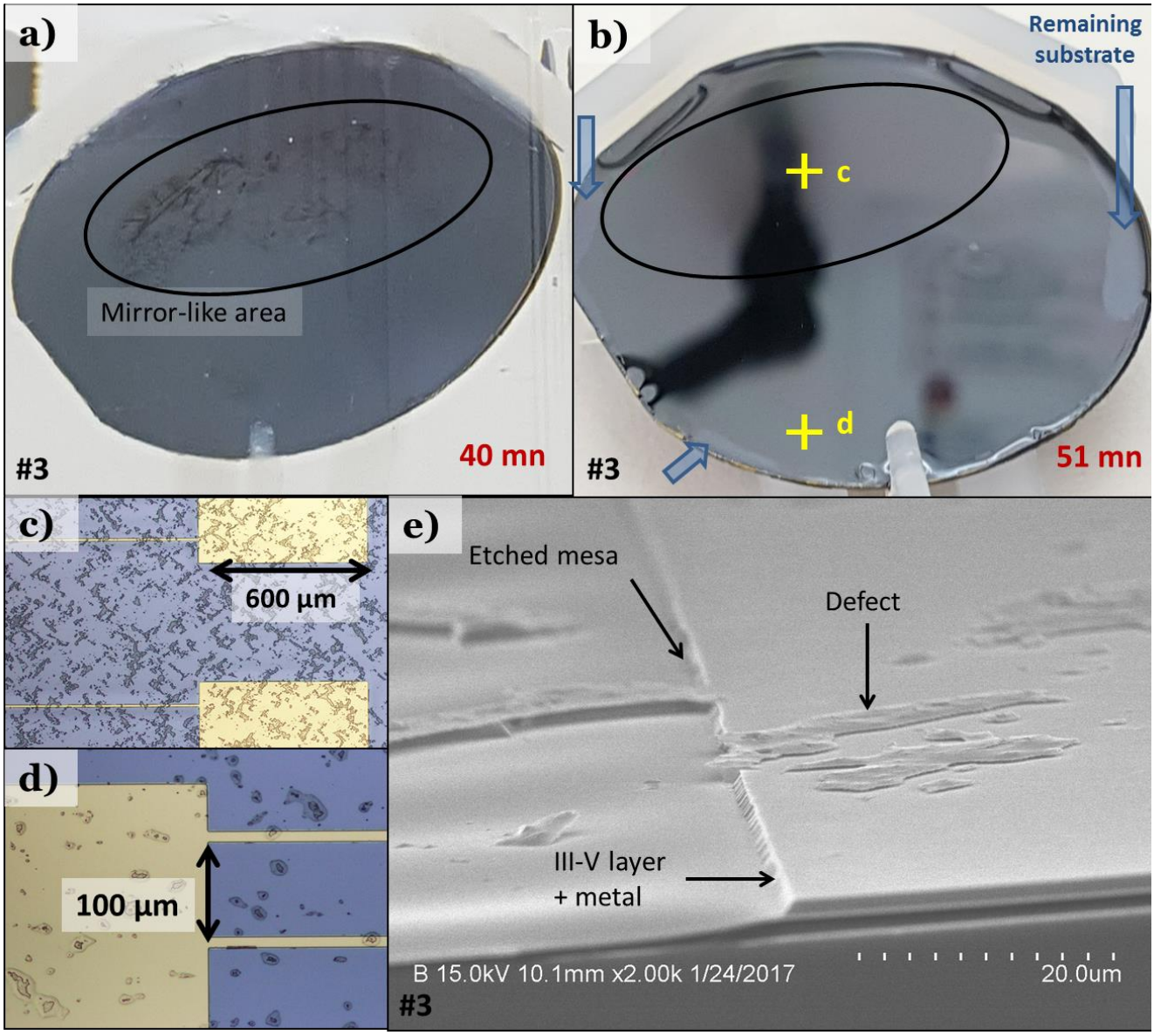



**Figure 5.15 - a) Picture of wafer #3 after 40 mn of wafer etching, b) after 51 mn. c) and d) microscope images of the surface in area c and d, e) SEM image in area c.**

***Lithography***

After lithographic steps, we observed the apparition of cracks on the layer (see Figure 5.16.a), in the middle of the wafer. We found out that the chuck used during spincoating was applying a too high vacuum, only in the middle of the wafer, which induced an excessive local strain. It was visible to the eye that the substrate was curved by the local vacuum. Thus, it is not surprising that this strong mechanical strain on the wafer had induced cracks in the thin III-V layer. Other chucks for 2 inches wafers were available, applying less strain, and not curving the wafer. This chuck will be preferred for the future processes, so as to reduce de risks of cracks at this stage. Also, during the sputtering metallization process, we noticed that the previous crack has extended, and a perpendicular crack appeared, as shown in Figure 5.16.b.

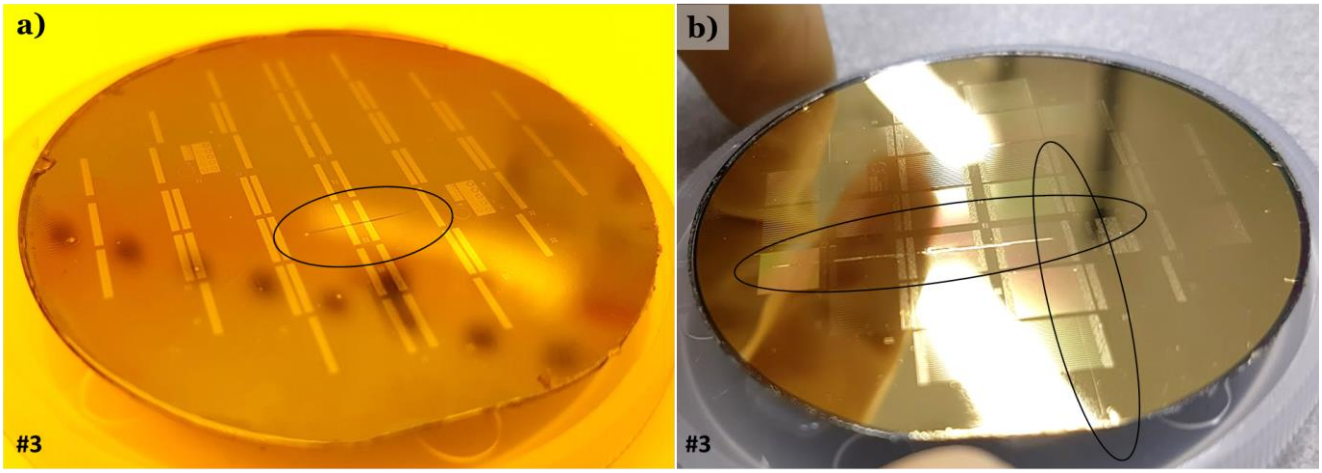



**Figure 5.16 - Wafer #3 a) after resist deposition, b) after front metal deposition**

***Lift-off***

The lift-off of a metal is a step during which we dip the wafer into acetone for a long time - at least 30 mn. During this step, we realized that the cracks already present in the previous steps were actually enlarging. The effect on the layer that had been partially detached (#2, in Figure 5.17.a.) revealed that the BCB actually reacts with the acetone. During the long dipping of the wafer into acetone, there is also a "lift-off" of the III-V layer. This emphasizes the fact that it is important to avoid those cracks in the last steps (spin-coating). Also, another suggestion would be to deposit the metal by using evaporation instead of sputtering. Indeed, the deposition being less conformal, we can expect the resist to be easily been lifted.

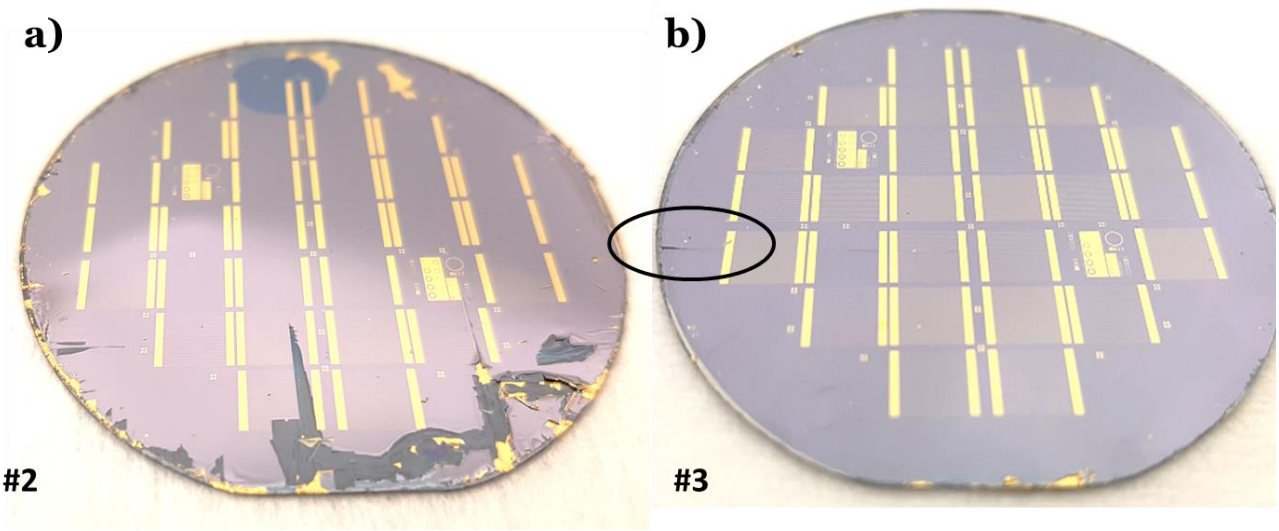
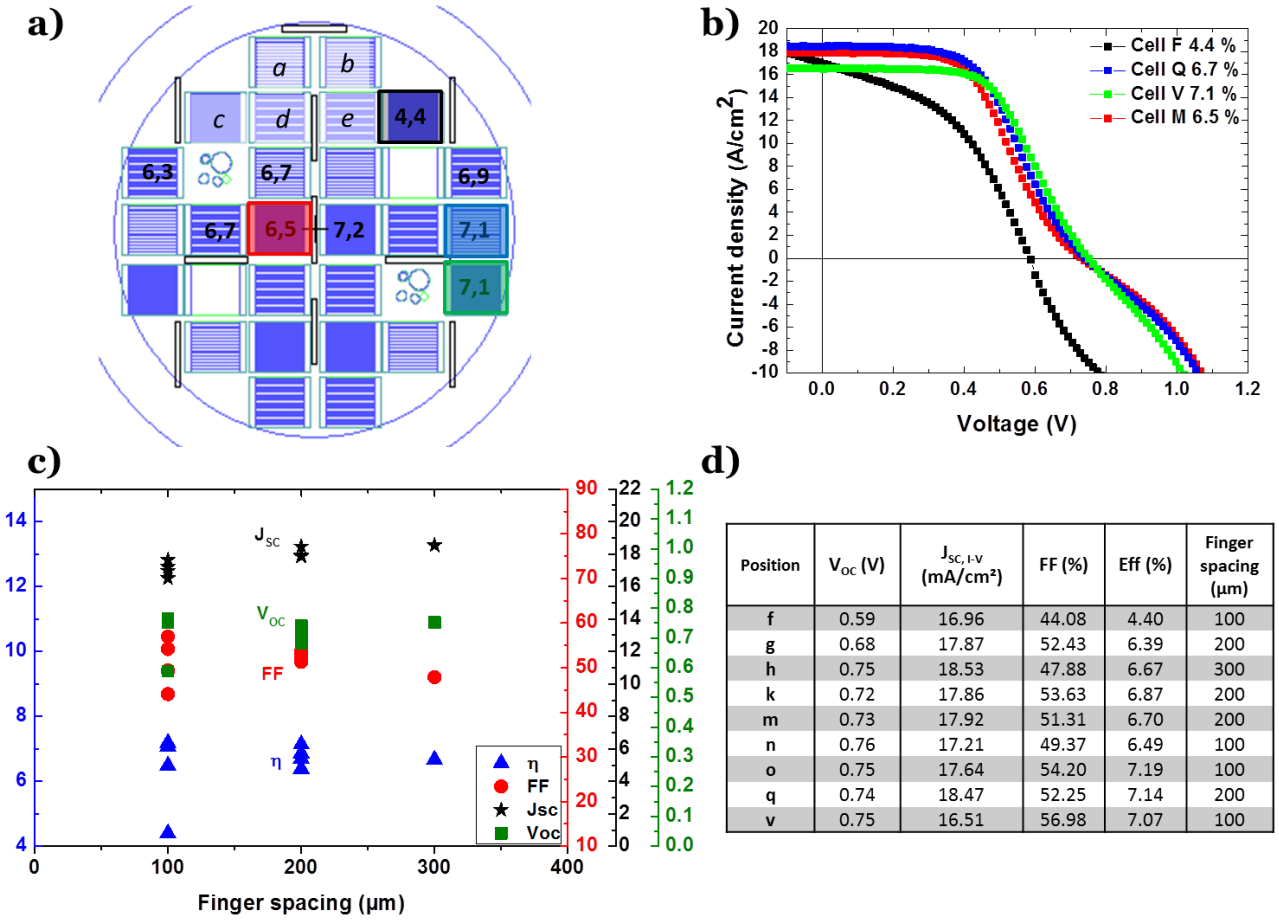



**Figure 5.17 - a) Wafer #2 after metal lift-off: the active layer has been removed where the previous bubles were present. b) Wafer #3 after metal lift-off: the previous cracks have been enlarged.**

### V.2.2.2. Electrical characteristics

We present here the electrical characteristics of the solar cells obtained on the full 2 inch. wafer #3, that has been processed according to the process flow presented in Figure 5.13.c. Due to the cracks issues, only a few of the 0.5x0.5 cm² solar cell over the full wafer were working. Figure 5.18.a. shows the spatial repartition of the solar cells of wafer #3. On the few solar cells that were not shunted are reported the corresponding conversion efficiencies. The *J-V* curves of some of them are represented on Figure 5.18.b. Several observations can be made. First, the measured $V_{OC}$ (below 0.8 V) is lower than expected. Indeed, for a GaAs solar cell, we expected to reach around 1.0 V (see Table 5.1). Series resistances are really high, as we could have expected from the previous observations of defects on the metallic fingers. The black curve shows a partly shunted solar cell. Interestingly, we do not see any effect of $R_{shunt}$ on the other cells, meaning that they are not shunted at all and do not present any pinholes. Figure 5.18.c and d gather the solar cells parameters of all the functioning cells. We plot all these characteristics as a function of the finger spacing of the designed cell. Once again, $J_{SC}$ increases (from 16.5 to 18.5 A/cm²) when the finger spacing is wider, which is consistent with the fact that there is less shadowing, enabling more photons to reach the solar cell. The other parameters have a dispersion that is too high to conclude on any trend.

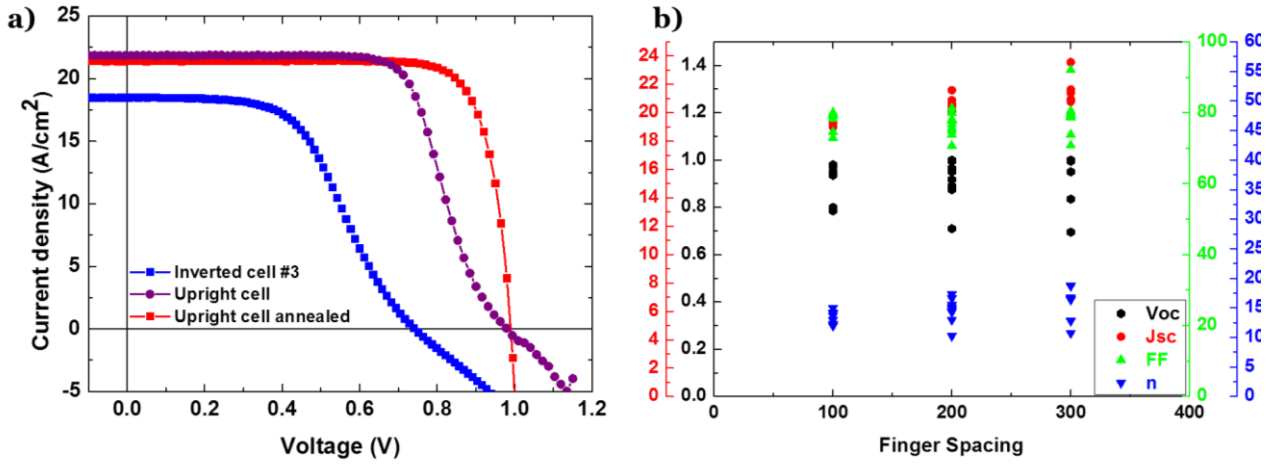



| Position | $V_{OC}$ (V) | $J_{SC,\ I\text{-}V}$ (mA/cm²) | FF (%) | Eff (%) | Finger spacing (µm) |
|---|---|---|---|---|---|
| f | 0.59 | 16.96 | 44.08 | 4.40 | 100 |
| g | 0.68 | 17.87 | 52.43 | 6.39 | 200 |
| h | 0.75 | 18.53 | 47.88 | 6.67 | 300 |
| k | 0.72 | 17.86 | 53.63 | 6.87 | 200 |
| m | 0.73 | 17.92 | 51.31 | 6.70 | 200 |
| n | 0.76 | 17.21 | 49.37 | 6.49 | 100 |
| o | 0.75 | 17.64 | 54.20 | 7.19 | 100 |
| q | 0.74 | 18.47 | 52.25 | 7.14 | 200 |
| v | 0.75 | 16.51 | 56.98 | 7.07 | 100 |

**Figure 5.18 - a) Spatial repartition of the different cells that are not shunted with their efficiency. b) J-V curve of 4 of these functioning cells c) $V_{OC}$, $J_{SC}$, FF and efficiency as a function of the finger spacing, d) Results on each functioning cell**

The overall shape of the *J-V* curves remind us of what has already been observed in our epi-Si heterojunction solar cells in Chapter 2 (Figure 2.23): it exhibits a S-shape. In that previous part, we found that this was due to a poor ohmic contact, due to an insufficient doping of the contacting cap layer. Here, we have a cap layer that is doped enough on the front side, and we also carefully added a back cap layer. Thus, the problem should not come from insufficient doping of the cap layer.

To have a better insight on the origin of this problem, we grew an identical GaAs solar cell right side up, and performed the exact same process flow (i.e. steps 6 to 12 from Figure 5.13). After step 12, the back contact was performed in Ti/Pt/Au at the back of the GaAs substrate. The resulting *J-V* curve is displayed in Figure 5.19 (purple circles), as compared with the reported cell #3. The $J_{SC}$, as well as the $V_{OC}$ are higher than that of the bonded one. We also deduce from the slope below $V_{OC}$ that the series resistances are lowered. This is certainly due to the fact that this new upright cell does not have the defects induced by the substrate etching presented in Figure 5.15. However, the FF remains rather low (below 70 %), while GaAs solar cells usually exhibit FF between 80 and 85 %. More importantly, we notice that the "S-shape" is still visible. Thus, it confirms there is a contact issue coming from our process. Pt/Au, deposited on p-GaAs, should form a ohmic contact without performing annealing (~ $2x10^{-5}$ Ω.cm²). However, the Ti/Pt/Au contact on n-doped GaAs is more difficult to achieve, and results in a shottky contact when not annealed [221]. We already faced the same contact issue in Chapter IV.5.2. (p.113), and showed that performing a rapid thermal annealing helps getting the expected low resistivity. Thus, a RTA at 400 °C for 1 minute has been performed on the upright solar cell. The resulting *J-V* curve (red squares) shows that the issue was indeed resolved by performing an annealing on the device. Note that the purple and red curves correspond to the exact same cell before and after annealing, whose parameters are gathered in Figure 5.19.c. We see that the annealing only affected the FF. The $V_{OC}$ is not changed, and the $J_{SC}$ is slightly lowered. We also reported the mean $V_{OC}$ $J_{SC}$ and FF values of all cells after annealing.




c)

| | $V_{OC}$ (V) | $J_{SC, I-V}$ (mA/cm²) | FF (%) | Eff (%) |
|---|---|---|---|---|
| Before annealing | 0,98 | 21,8 | 67,7 | 14,5 |
| After annealing | 0,99 | 21,4 | 79,7 | 16,9 |
| Mean value after annealing | 0,93 | 20,7 | 78,3 | 15,1 |
| Reported cell | 0,74 | 18,47 | 52,25 | 7,14 |

**Figure 5.19 - a) JV curves of a bonded inverted solar cell (blue), and an uprigth solar cell before (purple) and after annealing (red) b) characteristics of the uptight solar cells after annealing as a function of the finger spacing, c) Details of the solar cell characteristics**

This behavior is the same on all the 40 different cells of the wafer: the $J_{SC}$ slightly reduces after annealing, the $V_{OC}$ stays rather the same, and the big improvement lies in the FF. More than +10% absolute fill factor increase is obtained, and the resulting FF is close to 80 %. This fill factor could be further enhanced by using a better ohmic contact such as AuGe/Ni/Au alloy.

The characteristics of the 40 different cells over the wafer are gathered in Figure 5.19.b, sorted by finger spacing. There is a large dispersion in the results. The final conversion efficiencies range from 12 % to 18.7 %. $J_{SC}$ increases with the finger spacing while there is no noticeable trend upon the other parameters. $J_{SC}$ remains below the values from literature (record $J_{SC}$ values are above 27 mA/cm²). Note that this could be enhanced by optimizing the grid design (a higher finger spacing may further increase the $J_{SC}$). Also, we did not add any anti-reflective coating, thus the $J_{SC}$ is reduced due to reflection losses. The $V_{OC}$ obtained is consistent with the bandgap of GaAs, and really close to state-of-the art presented in Table 5.1.

Thus, studying the upright solar cell helped us to find the origin of the S-shape, and the low FF, and gave us insight on how to improve the performance of the bonded solar cell. The main and easy improvement can be done by performing an annealing of the n-type contact. However, this annealing must be performed before the bonding (right after step 2 from Figure 5.13.c). Indeed, we tried to anneal at 400 °C the bonded cell #3, but we observed a detachment of the layer, and every cell was then shunted. To improve the n-side contact, we could also use another cap layer. Up to now, the cap layer was made with Si-doped GaAs. Now that we master heavier doping level with Te thanks to the studies presented in Chapter 4, we can use such layer as the contact layer. With a better ohmic contact, we expect a fill factor approaching 80 % instead of 52 %, to reach a 11% efficiency inverted solar cell. Also, the $V_{OC}$ and $J_{SC}$ are both lower than that of the upright cell, probably due to more recombination especially at the surface that is very defective due to the issues during substrate and etch-stop layer removal. This issue can also be solved, by changing the chemical bath when reaching the etch-stop.

# V.3. Bonding of Si/GaAs stacks

## V3.1. Observations

This part deals with the bonding of full tandem solar cells. We faced again new technological challenge. We consider the 5 first steps of the process flow presented in Figure 5.13.c. The structure that we bond is the one presented in Figure 5.11: an AlGaAs solar cell grown by MOVPE on a GaAs wafer with a GaInP etch-stop, followed by a III-V tunnel junction. On top of it is grown the epitaxial Si layer, followed by the amorphous stack to ensure passivation and contact, as presented in Chapter II.3.1. (p. 54). On top of the c-Si/a-Si:H stack is deposited ITO, followed by Ag or Al. In these experiments, the thickness of the Si epitaxial layer is maintained in the range of 1 µm.

During the first trial, after substrate removal, the metal was Ag, and it was deposited by evaporation. After substrate removal, we observed a detachment of the film at the interface between ITO and Ag that was deposited by evaporation, as seen in Figure 5.20.a. Evaporation does not provide good enough adhesion. Also, Ag is usually less adhesive with ITO than Al. Thus, we decided to deposit Al by sputtering instead of Ag by evaporation.

After a few other trials, we were facing the same issue: as soon as the etch-stop is reached, some cracks appear at the surface. They keep on propagating on the wafer after several hours. Also, our first trials were performed on samples grown on 750 µm thick GaAs substrates (#1 and #2 in Figure 5.20.a and b.)

Interestingly, same bonding using a tandem solar cell grown on a 350 µm thick substrate led to fewer cracks, as seen in Figure 5.20.c. (the half wafer on the right it completely free of cracks). On the left part, the cracks seem to be initiated from the cleavage edge, where the wafer has been weaken (this wafer had unfortunately been broken in two pieces before the bonding). This result was really encouraging, and we could thus pursue the process to the next step: the GaInP etch-stop

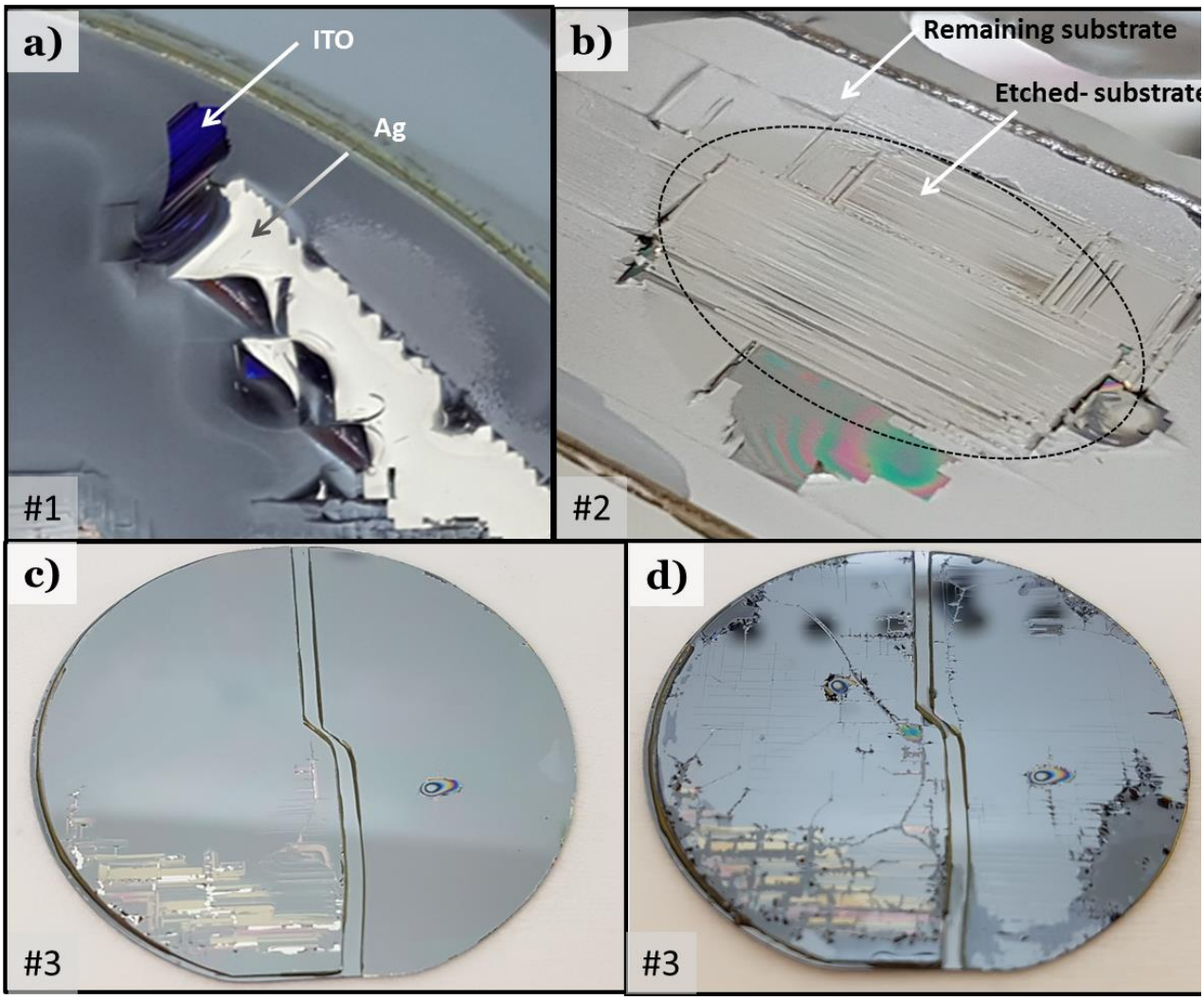



**Figure 5.20 - a) Picture of layer detachment between Ag and ITO, b) picture of a tandem solar cell (#2) after 750 µm-thick GaAs substrate removal, c) picture of a tandem solar cell (#3) after 350 µm - thick substrate removal d) #3 after GaInP etch-stop etching**

etching. Regrettably, we did not anticipate by changing the metal from Ag to Al, the reaction of Al with the chemicals involved in the process flow. Indeed, GaInP can be etched selectively only with chemicals containing HCl, which also strongly reacts with Al. By dipping the wafer into HCl, the semiconducting layer was removed, and at some point even lifted-off. Even if the Al is buried under the semiconductor layers, the HCl could have access to Al via the trenches due to the cracks, but also

from the borders of the wafer (see Figure 5.20.d, right part). As a pathway to overcome this issue, we could change the metal and try to use Ag instead of Al, but deposited by sputtering this time, and not by evaporation so as to ensure a better adhesion. However, we must consider a feature in this tandem solar cell, which is that the Si epitaxial layer is strained. In the next part, we try to understand the origin of the cracks observed during substrate removal, which seems to be a recurrent issue during the bonding of the tandem solar cells.

## V.3.2. Strain induced by Si

### V.3.2.1. Reciprocal Space Mapping

Let us take a closer look at the cracks induced during GaAs substrate removal. Those cracks are certainly due to the release of mechanical stress induced in the layer. To have a better insight on this stress, we compared the {224} reciprocal space mapping (RSM) of one sample right after Si deposition, and after bonding and GaAs substrate etching (the X-ray beam was placed on an area of about 5mm*5mm that did not contain any crack). Before bonding, we could see a well-defined peak for the GaAs substrate and the lattice-matched AlGaAs solar cell, and a wide peak corresponding to the relaxed crystalline silicon. After substrate etching, only the Si layer and the AlGaAs stack remains. We notice that the peaks of the AlGaAs and epi-Si layers remain at the same coordinates in the reciprocal space. However, we see a large widening of the peak corresponding to the AlGaAs stack, revealing a huge mosaicity in the layer (Figure 2.7). While the GaAs substrate was in contact with the AlGaAs stack, the stress induced by the Si was supported by the thick GaAs substrate. However, when the substrate is removed, the AlGaAs film needed to relieve the strain. The AlGaAs stack probably reached its elastic-plastic transition, leading to the numerous cracks observed experimentally. It is worth noticing that the width of the epi-Si signature has not changed, thus the mosaicity concerns only the III-V layer. In other words, Si structure has not changed, only the AlGaAs stack is affected.

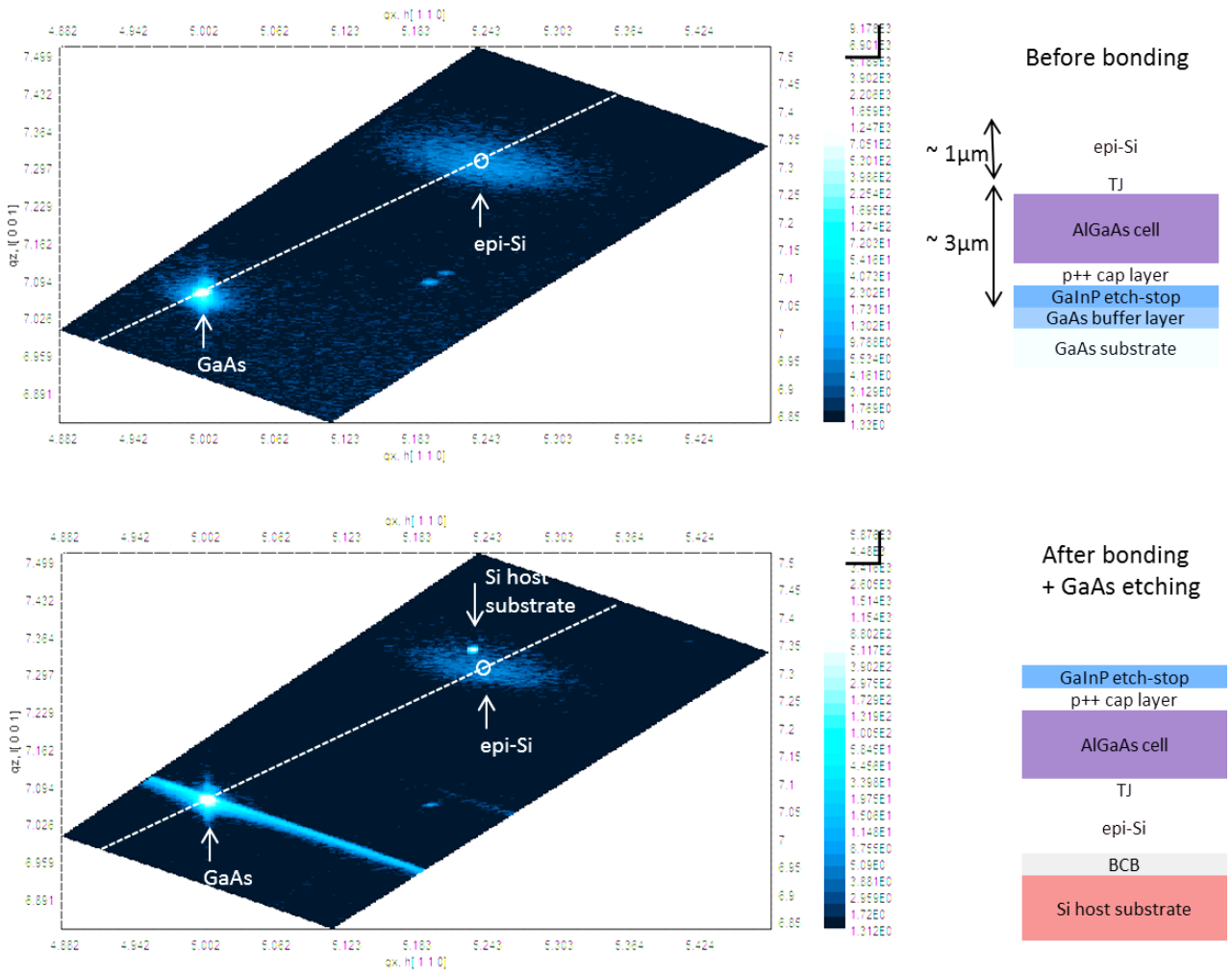



**Figure 5.21 - {224} reciprocal space mapping of a tandem stack before and after bonding and substrate removal.**

### V.3.22. Curvature measurements:

To have an insight on the strain in the wafer, we did some curvature measurements with a mechanical profilometer. Indeed, curvature measurement are often used to assess the strain in heteroepitaxial layers [222]. We thus measured the bowing of the substrate before and after epitaxy of Si on GaAs. From the bowing, we can deduce the radius of curvature of the substrate with Eq. 5.1. An illustration of this equation is shown in Figure 5.22.a.

$$R = \frac{a^2 + b^2}{2 * \mathrm{b}} \qquad \textbf{Eq 5.1}$$

With a 800 nm thick epi-Si, the radius of curvature was found to be ~4.5 m, while before it was in the range of 20m. Thus, the Si induced a bending of the substrate, as illustrated in Figure 5.22.b.

Then, from this value, it is possible to deduce the stress in the epitaxial layer by using Stoney equation[223]:

$$\sigma_{epi-Si} = \frac{{h_{sub,GaAs}}^2 * E_{sub,GaAs} * (\frac{1}{R} - \frac{1}{R0})}{6 * h_{epi-Si} * (1 - \nu_{sub,GaAs})}$$ **Eq 5.2**

$h_{sub,GaAs}$ and $h_{epi-Si}$ are the respective thicknesses of the GaAs substrate and the epitaxial Si layer. $E_{sub,GaAs}$ is the Young modulus of GaAs substrate and $\nu_{sub,GaAs}$ its Poisson coefficient.
All the theoretical values[224] for GaAs and bulk Si are reported in Table 5.3. We also reported the measured radius of curvatures and the thicknesses of the wafer and the epitaxial layer.

**Table 5.3: Theoretical Young moduli and Poisson coefficients of GaAs and Si, and experimental values of R, $R_0$ and h**

| | Young Modulus **E** (GPa) | Poisson coefficient **ν** | R (m) | R with epi-Si (m) | h (µm) |
|---|---|---|---|---|---|
| GaAs | 85.5 | 0.31 | 20 ±3 | | 350 |
| Si | 179 | 0.22 | | 4.5 ±1 | 0.8 |

The calculation using Eq 5.2 and the values in Table 1 lead to a stress in Si layer of

$$\sigma_{epi,Si} = -0.57\ GPa$$

The stress is negative, thus the strain is compressive. The relation between the stress and the strain in a linear regime is given by the following equation:

$$\varepsilon_{epi-Si} = \frac{\sigma_{epi-Si} * (1 - \nu_{epi-Si})}{E_{epi-Si}}$$ **Eq 5.3**

By approximating the values of $E_{epi\text{-}Si}$ and $\nu_{epi,Si}$ with the values found in literature for bulk Si reported in table 1 we calculate a strain in the epitaxial Si of :

$$\varepsilon_{epi-Si} = -0.30\% \pm 0.04$$

If we now look back in Chapter III, figure 3.5.b, at the values of the in-plain strain in the epitaxial layer, we are glad to see that these results are consistent with the values obtained by the GIXRD measurements, confirming once again that the epitaxial layer is compressively strained in the plane.

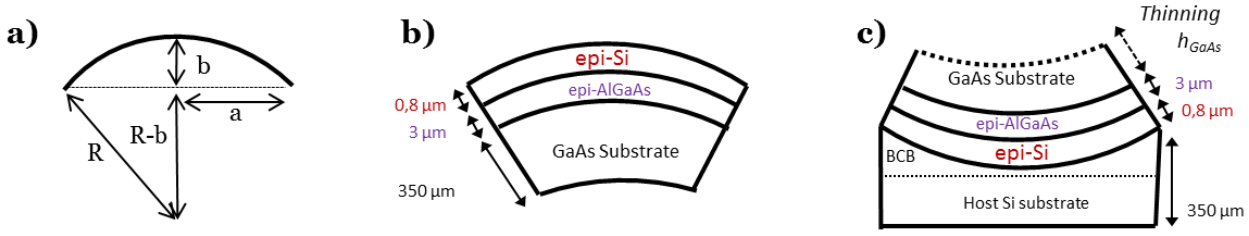



**Figure 5.22 - a) schematics of the radius of curvature as a function of the bowing, b) schematics of the tandem solar cell before bonding, c) schematics of the tandem solar cell after bonding during substrate removal**

Now, let us try to estimate what happens when we bond this strained system and remove the substrate, in order to understand the cracks observed experimentally. After the bonding, the system consists of a thick "substrate" which consists of the epi-Si bonded to the BCB and the host substrate, the "AlGaAs stack" which corresponds to the stack of the III-V subcell and the GaInP etch-stop layer as it was presented in Figure 5.2.

While accurate calculations have to be performed, we will try here to explain roughly the tendencies by doing some assumptions. We suppose that the new system is as presented in Figure 5.22.c.
The following assumptions were made:

1) We suppose that the radius of curvature after bonding is the opposite of that of before bonding
2) We took the same value of $R_0$ than for the GaAs substrate
3) We used the mechanical constants of bulk Si from literature
4) We considered only one "GaAs" material, not a stack of 350 µm GaAs substrate+ ~3 µm of III-V stack.
5) We also considered that the system of host Si+BCB+epi-Si was equivalent one thick 350 µm Si substrate with Si mechanical properties

In this new configuration, we consider the stress in the GaAs layer during the thinning of the substrate. The stoney equation in this new configuration becomes:

$$\sigma_{GaAs} = \frac{h_{host\ Si,}^{\ 2} * E_{host\ Si} * (\frac{1}{R_0} - \frac{1}{R})}{6 * h_{GaAs} * (1 - \nu_{host,Si})} \qquad \text{Eq 5.4}$$

Intuitively, we deduce that the thinner will become the III-V layer (low $h_{GaAs}$), the higher will be the strain. We plot in Figure 5.23the stress as a function of the GaAs thickness. The right axis corresponds to the strain calculated by adapting Eq 5.3 to GaAs.

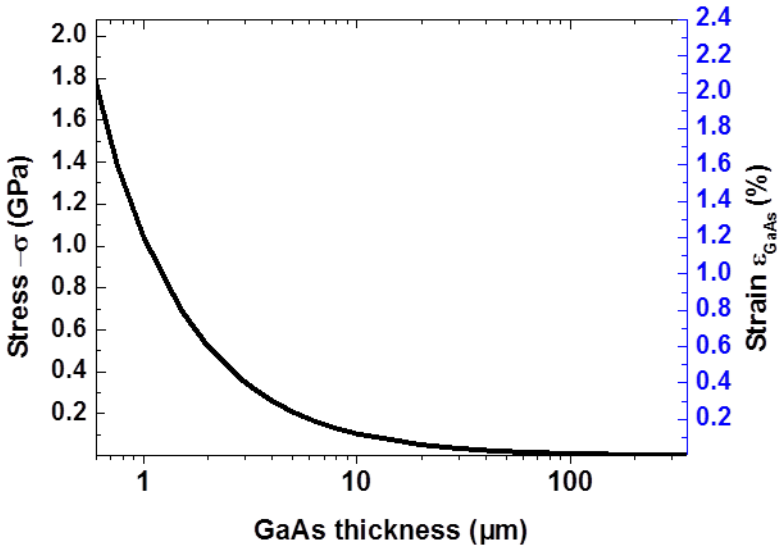



**Figure 5.23 : Stress and strain in the III-V stack during GaAs substrate removal**

More literature research remains to be done in order to know the critical stress in GaAs that leads to a plastic relaxation. We found that this value depends, not only on the temperature[225], as well as

other parameters, such as the doping level in the layer[226]. For a rought estimation, we found in this paper[225] that the critical stress is in the order of magnitude of 120 MPa for an elastic plastic transition in undoped GaAs (at 280 °C, which is their lowest temperature reported). In our black curve, 120 MPa corresponda in our curve to a GaAs thickness around 8 µm.

Thus, these estimations show that, considering the strain in the epitaxial silicon layer, it was predictible, that the reduction of the GaAs thickness would lead to the plastic relaxation of the III-V subcell with thicknesses lower than 8 µm, and thus to the cracks in the semi-conductor.

However, there are some routes to limit those issues. Indeed, it is possible to do some strain compensation by adding on top of the Si a material which is tensile strained. For example, SiN is often used for such strain compensations[227]. In this way, the radius of curvature can be compensated, and the GaAs substrate removal would not induce too high stress in the III-V subcell.

### Thicker epi-Si layers

To have an efficient tandem solar cell, thick epitaxial Si layers are required in order to ensure enough light absorption. We propose now to calculate the stress that would be induced on the III-V subcell during GaAs substrate removal.

Let us suppose that we grow thicker Si layers (5 µm and 10 µm). The radius of curvature obtained by using Eq 5.3, with σ Si = 0.57 GPa are: R(5 µm) = 1.6 m and R(10µm)= 0.87 m. By plotting Eq 5.4 as a function of the GaAs stack thickness, the red and blue curves are obtained for 5 µm and 10 µm of Si respectively.

Following the same reasonning as earlier, we calculated the stress induced in the GaAs stack during substrate removal and reported it in Figure 5.24.We see that for thicker layers, the stress induced is even higher in the GaAs stack.

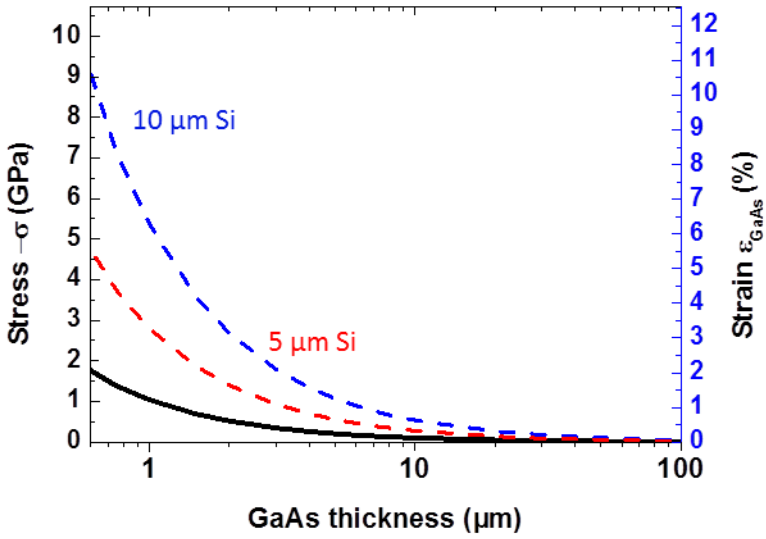



**Figure 5.24 - Stress and strain in the III-V stack during GaAs substrate removal for various epi-Si thicknesses**

Qualitatively, for a 10 µm-thick strained epitaxial Si layer, if we consider that the critical stress is of 120 MPa, the substrate would crack for a thickness around 50 µm.

If we try to grow even thicker Si layers, we can even expect to see the cracking of the substrate during the epitaxial step. The crack of a substrate during heteroepitaxy has already been observed in case of compressive strained GaN heteroepitaxy on sapphire[228].

Thus, this part tried to assess qualitatively the effect of the strain in the epitaxial Si layer on the III-V layer during substrate removal after bonding. We could link the stress measured by curvature analysis with the strain measured in Chapter III by GIXRD analysis. Even though these calculations include some assumptions that need more accurate determinations, we can anyway conclude that the crack in the III-V layer is somehow unavoidable, especially if we grow thick Si layers (above 10 µm). To prevent this effect, we can consider the addition of a strain compensation layer on top of Si. However, the most promising solution to avoid such a stress in the group IV layer would be to use SiGe on GaAs instead of Si. With a lattice parameter closer to that of the GaAs, SiGe is expected to have a lower in-plane strain. This assumption needs of course to be verified, given the fact that our PECVD grown epitaxial materials do not seem to behave as expected in terms of strain.

## V.4. Conclusion & perspectives

In this chapter, we successfully grew and fully processed state-of-the-art AlGaAs solar cells adapted for integration in a tandem solar cell. With our design, we achieved conversion efficiencies up to 17.6 %, with fill factors between 80 and 85 %. If further improvements of the design can be considered, such as the reduction in the shading due to the metal fingers, this result meets the requirements for integration in a tandem solar cell. Then, we simplified the process in order to bond some inverted GaAs solar cells. To do so, we used BCB, and faced several technological issues that have mostly been solved, but the fill factor was rather poor (FF≈50 %). For the next trials, we expect a significant enhancement of the FF with a better ohmic contact. Finally, we bonded an inverted tandem solar cell on a host substrate and removed the substrate. We observed the apparition of cracks during the GaAs substrate removal, which are most certainly due to the strain in the epitaxial silicon layer. We will anyway try to process tandem solar cells with thin epi-Si layers (below 800 nm) in order to be able to measure electrically the device and have an insight on the quality of the interface between Si and GaAs, but the future perspectives for this work are to grow SiGe on GaAs and assess the strain in the SiGe layer. This way, SiGe will not only help to solve the strain issues emphasized in this chapter, but also enhance the absorption in the bottom cell, thus requiring a much thinner SiGe layer for similar tandem solar cell efficiency.

# General conclusions and perspectives

Combining III-V and silicon represents a promising pathway to fabricate tandem solar cells that would overcome the ~29% efficiency limit of a single c-Si solar cell. In this manuscript, we presented an innovative approach to grow such tandem solar cell: by performing an inverted metamorphic growth of crystalline silicon and SiGe on GaAs thanks to a low temperature (below 200 °C) PECVD process.

## Conclusions

We first studied the epitaxy of Si and SiGe compounds on Si substrates, and fabricated heterojunction solar cells. We reached a conversion efficiency of 6.7 % for a 1.5 µm c-Si absorber with a $V_{OC}$ of 0.57 V, showing that our epitaxial films are electrically suitable for integration in a solar cell. A 3 minutes annealing at 200 °C showed an increase in the device performance up to 7%. However, in our epitaxial conditions, annealing above 300 °C leads to the degradation of the interface between the substrate and the epi-layer. This is probably due to the accumulation of hydrogen at the interface leading to blistering, thus its detachment from the substrate. The addition of Ge to Si (from 7 to 32 %) induced an increase in $J_{SC}$ for comparable epitaxial thicknesses due the stronger absorption in SiGe, along with a reduction in $V_{OC}$ due to a lower bandgap. We observed that the performances of SiGe heterojunction solar cells are highly deteriorated when the SiGe layer is relaxed. The relaxation happens above a critical thickness (> 1µm) of the heteroepitaxial layer, that depends on Ge content: the higher the Ge content, the lower the critical thickness. In our case, 32% of Ge was relaxed for a thickness of 1 µm. We found that the critical thickness values for our PECVD growth at 175 °C are higher than that of other epitaxial techniques happening at higher temperatures (for which $SiGe_{32}$ layers relax below 100 nm). Thus with PECVD we can grow thicker SiGe layers on Si while keeping the layer strained. We also found that SiGe solar cells exhibit better efficiencies when grown at 200 °C instead of 175 °C.

Then, the heteroepitaxy of silicon on gallium arsenide has been studied. We successfully grew monocrystalline silicon with thicknesses of 1 µm. The strain has been fully relaxed at the interface, leading to thick epitaxial layers of monocrystalline silicon with no threading dislocations. Using XRD analysis of both out-of-plane and in-plane lattice parameters, we observed two interesting phenomena on the epi-Si layers. On the one hand, we found that the out-of-plane parameter ($a_{\perp}$) is 1% higher than that of the theoretical bulk Si. We correlate this behavior to the presence of hydrogen that induces strain in the growth direction. On the other hand, the in-plane parameter ($a_{//}$) is lower than that of the bulk. As the lattice parameter of the bulk GaAs is 4% higher than that of Si, we would have expected a tensile strain, but we found here a compressive strain. In order to explain this unexpected result, we must consider the role of the thermal strain of the GaAs substrate that has a higher thermal expansion coefficient than Si. But this behavior can be explained only if the surface temperature of the substrate is locally much higher than the 175 °C set point of the reactor. This observation could actually help understanding the growth mechanisms of low-temperature PECVD, and be an experimental proof that the growth surface during the growth is locally at really higher temperatures. This would explain how a full monocrystal can be obtained at such low reactor temperature.

The development of the tandem solar cell does not only lie on the growth of Si on GaAs. To manufacture a working tandem device, a large number of steps and building blocks had also to be achieved. While the III-V lab has a strong expertise in MOVPE growth and processing for various other applications (photonics, optoelectronics…), photovoltaic was a new topic, and we had to adapt the know-how to our application. Thus, we developed the materials necessary to grow the III-V subcell with $Al_{0.22}Ga_{0.78}As$, designed to be current-matched with Si. The full process in clean rooms, along with the design of the grid geometry had to be developed, in order to realize measurable III-V solar cells. With our design, we achieved conversion efficiencies up to 17.6 % with fill factors between 80 and 85 %, reaching state-of-the-art for $Al_xGa_{1-x}As$ solar cells with a bandgap adapted for integration into a tandem solar cell with Si.

Also, heavily doped n-type and p-type III-V layers (GaAs, AlGaAs and GaInP) have been developed in order to fabricate tunnel junctions (TJ), which is another essential part of our targeted device. Indeed, in a two terminal configuration, a TJ is essential to allow the carrier to flow from the top-cell to the bottom by tunnel effect. We could reach good peak tunneling current ($J_{peak}$ ~10 mA/cm²) with standard dopants used in MOVPE (C for p-type and Si for n-type). However, as n-doping level is limited to $1.2\times10^{19}$ $cm^{-3}$ due to Si amphoteric behavior, optimization of p-type doping level did not enhance the $J_{peak}$. Thus, to further increase the performances of our TJs, we developed the doping of GaAs with tellurium, using DIPTe precursor. We finally could reach doping levels higher than $2.7\times10^{19}$ $cm^{-3}$, and found that our precursor is less sensitive to the growth temperature than the other common precursor (DETe). We also found that the nature of the underlying layer can decrease Te incorporation, but it can be solved by performing an in-situ annealing between the growths of the two layers. With such a n-doped layer, we reached state-of-the-art tunnel junctions with peak tunneling currents as high as 3000 A/cm². These TJs are not only suitable for our application, but can also be integrated in multi-junction solar cells working under high concentration. We also explored the possibility of doing Si/GaAs hybrid tunnel junctions aiming at taking advantage from the defects located at the interface of the heteroepitaxy to enhance the TJ performances. This would also avoid having this interface elsewhere, where the recombination due to these defects could be critical for tandem solar cell performances. We successfully grew heavily doped crystalline Si layers on top of GaAs, but issues in the device measurements did not allow us to conclude on its performances.

We must however keep in mind that the dopants of the tunnel junction can be partly passivated due to the further exposition to a $H_2$ plasma during PECVD heteroepitaxy. Indeed, we showed that hydrogen plasma can deactivate the dopants in GaAs (Te, C, Si), in a non-negligible way: at the surface of the III-V material, the doping level can be reduced by up to one order of magnitude. This passivation is due to the diffusion of hydrogen in the layer that forms complexes with the dopant atoms. Luckily, this behavior can be recovered by performing a thermal annealing.

Once all of these steps were mastered, we could thus grow the inverted metamorphic solar cell, which is composed of the inverted III-V solar cell followed by the III-V tunnel junction and finally the epitaxial growth of Si layer. For a working tandem solar cell, one last crucial step was missing: the bonding of the stack on a mechanical holder so as to etch the GaAs substrate and handle the 5 to 10 µm-thick remaining active layer for the following solar cell process flow. With the available techniques in our clean room environment, we chose to bond our stack with a polymer (BCB). The process was simplified as compared to the upright solar cell, because, each additional process step (substrate etching, spin coating, lift-off…) can induce critical deterioration of the active layer. With several iterations, we learnt how to avoid these process issues and succeeded in bonding full 2

inches wafers with functioning solar cells designed with a 5×5 mm² area. Once relatively confident on these steps, we finally bonded a full stack of III-V/TJ/epi-Si with 1 µm of epi-Si. The substrate removal was found to be even more critical than for the III-V inverted cell. Indeed, as we have observed earlier by studying the structure of the epi-layer, our Si is in tensile strain. When removing a 750 µm substrate, we actually observed that the AlGaAs layer was relaxing the strain and inducing cracks all over the wafer. We could reduce these issues by using a thinner GaAs substrate (350 µm thick), and we are thus close to finally fabricate and measure our first tandem solar cell made by inverted metamorphic growth of c-Si on GaAs by low temperature PECVD.

## Perspectives

During this work, various aspects of the fabrication of a tandem solar cell have been explored. This has led to the achievements presented above and had also raised numerous questions. These are worth exploring in order, not only to further improve the building blocks of the tandem solar cell, and obviously, of the final tandem solar cell itself, but also to understand more fundamental physical phenomena.

The development of SiGe on GaAs is the next step towards the fabrication of tandem solar cells with our approach. Indeed, the bandgap combination between AlGaAs and SiGe with the right compositions can also lead to high efficiency tandem solar cells, and it would reduce the required thickness of epitaxial SiGe due to the higher absorption coefficient of SiGe. Also, as Ge lattice constant is close to that of GaAs, high Ge content could be achievable without relaxation of the SiGe layer. It would also be interesting to explore the growth of c-Si by PECVD at higher temperature (from 300 to 400 °C) to reduce the amount of hydrogen incorporated in the epitaxial layer, and thus increase the thermal stability of the layers upon annealing.

In this manuscript, the interpretation of the small in-plane lattice parameter of our epi-Si on GaAs leads to the following possible conclusion: the growth of epitaxial Si may happen thanks to a local high temperature at the growing surface. Our hypothesis is that this smaller in-plane lattice parameter is due to the thermal strain induced by the GaAs substrate. It seems that the growth surface is at higher temperature than the reactor temperature. If this assumption remains qualitative and with lots of approximations, the trend seems to be confirmed by the values already obtained in the lab on Si/GaAs heteroepitaxy as well as Si on Ge. It is definitely a route to explore, by performing systematic studies on the in-plane parameter of heteroepitaxial Si layers grown on various (100) substrates (GaAs, Ge, InP) with fixed deposition conditions. This way, we would get a better insight on the origin of the observed compressive strain, by decorrelating the thermal strain from the lattice strain and the hydrogen content.

For fabricating tandem solar cells, the main challenge is now to remove the substrate without inducing cracks in the layers. Also, if we may succeed with 1 µm thick epi-layer, detailed investigation must be done on the strain induced by the epi-Si layer on the epi-III-V stack once the GaAs substrate is removed. Indeed, to obtain reasonable conversion efficiencies we need to grow thick epi-Si(Ge) layers. With thicker Si layer, is expected a higher higher strain in the III-V subcell. While we can consider the addition of a strain compensation layer on top of Si, the most efficient solution would be to use SiGe on GaAs instead of Si. Indeed, with a lattice parameter closer to that of the GaAs, SiGe is expected to induce a lower strain on the GaAs layer after substrate removal. This

assumption needs of course to be verified, given the fact that our PECVD grown epitaxial material does not seem to behave as expected in terms of strain.

Even if we are not at this stage of the development of our tandem solar cell, further improvements of the tandem solar cell can be anticipated. First, concerning the AlGaAs solar cell, further optimization of the absorber thickness and the Al content will be needed in order to have a current-match with the SiGe layer that we would be able to grow on GaAs. Also, the addition of a back light-trapping scheme would have to be considered, in order to further reduce the required epitaxial thickness of Si(Ge).

Finally, this PhD enabled to build-up expertise on several domains, nourishing each lab from their different knowledge. Being at the crossroads between the worlds of crystalline III-V materials (III-V Lab), and of silicon-based photovoltaics (PECVD materials at LPICM-Total, modelling and electrical characterization at GeePs), enabled to build-up new expertise in those different worlds, and to open the path to new research topics and applications. Photovoltaic can now be counted as a new field of expertise at the III-V Lab, providing opportunities for other projects dealing with multi-junction solar cells. Moreover, the tunnel junctions fabricated can be used not only in multijunction solar cells but also in various other III-V devices. Furthermore, the building of a new know-how on characterization of crystalline materials by means of X-Ray diffraction gives to LPICM a new tool to understand the crystalline growth by PECVD. Finally, by performing heteroepitaxy on III-V compounds, we may have found a key to understand the physics behind low-temperature PECVD epitaxy.

# List of publications

## Publications

1. W. Chen, G. Hamon, R. Léal, J.-L. Maurice, L. Largeau, and P. Roca i Cabarrocas, Growth of Tetragonal Si via Plasma-Enhanced Epitaxy. *Cryst. Growth Des.* 17, 4265–4269 (2017).

2. G. Hamon, N. Vaissiere, R. Cariou, R. Lachaume, J. Alvarez, W.Chen, J.-P. Kleider, J. Decobert, P. Roca i Cabarrocas, Plasma-enhanced chemical vapor deposition epitaxy of Si on GaAs for tunnel junction applications in tandem solar cells. *J. Photonics Energy* 7, 022504 (2017).

3. W. Chen, R. Cariou, G. Hamon, R. Léal, J.-L. Maurice & P.Roca i Cabarrocas, "Influence of deposition rate on the structural properties of plasma-enhanced CVD epitaxial silicon*", Sci. Rep.* 7, 43968, 2017

4. R. Lachaume, M. Foldyna, G. Hamon, J. Decobert, R. Cariou, P. Roca i Cabarrocas, J. Alvarez, J.P. Kleider, "Detailed analysis of III-V/epi-SiGe tandem solar cell performance including light trapping schemes", *Sol. Energ. Mater. Sol. Cells*, December, 2016

5. G. Hamon, J. Decobert, N. Vaissiere, R. Lachaume, R. Cariou, W. Chen, J. Alvarez, N. Habka, J. P. Kleider, P. Roca i Cabarrocas."Direct growth of crystalline silicon on GaAs by low temperature PECVD: Towards hybrid tunnel junctions for III-V/Si tandem cells", 2016 *IEEE 43rd Photovoltaic Specialists Conference* (PVSC), 2016

6. G. Hamon, R. Cariou, R. Lachaume, J. Decobert, K. Louarn, W. Chen, J. Alvarez, J.P. Kleider, P. Roca i Cabarrocas 'Investigation of Hybrid Tunnel Junction Architectures for III-V/Si Tandem Solar Cells'*, 31st European Photovoltaic Solar Energy Conf. and Exhibition*, pp. 75–79, 2015

7. R. Lachaume, R. Cariou, J. Decobert, M. Foldyna, G. Hamon, P.Roca. i Cabarrocas, J. Alvarez, J.-P. Kleider, "Performance Analysis of AlxGa1-xAs/epi-Si(Ge) Tandem Solar Cells: A Simulation Study", *Energy Procedia*. 84, 41–46., 2015

## Communications:

1. G. Hamon, Concentrating Photovoltaic Conference (CPV-13), Ottawa, Canada, May 2017 ***(Oral presentation)***

2. G. Hamon, Journées Nationales du PhotoVoltaïque (JNPV), Dourdan, France, December 2016 ***(Invited Oral presentation)***

3. G. Hamon, IEEE 43rd Photovoltaic Specialists Conf. (PVSC), Portland, USA, June 2016 ***(Poster)***

4. G. Hamon, Photovoltaic Technical Conference (PVTC), Marseille, France, May 2016 ***(Oral presentation)***

5. G. Hamon, 31st European Photovoltaic Solar Energy Conf. and Exhibition (EU PVSEC), Hambourg, Germany, September 2015 ***(Oral presentation)***

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ÉCOLE DOCTORALE
INTERFACES
Approches Interdisciplinaires : Fondements, Applications et Innovation

**Titre :**.Cellules solaires tandem III-V/Si : une approche inverse métamorphique par PECVD basse température de c-Si(Ge)

**Mots clés :** Epitaxie, PECVD, MOVPE, Hétéro-épitaxie, Cellules Solaires Tandem, III-V/Si, Jonctions Tunnel

**Résumé :**
Ce travail présente une approche innovante pour fabriquer ces cellules solaires tandem III-V/Si en utilisant une approche inverse métamorphique par PECVD à basse température (<200 °C). Pour réaliser la structure finale de la cellule solaire tandem en SiGe/AlGaAs, le développement et l'optimisation de plusieurs briques technologiques. Tout d'abord, nous développons l'épitaxie à 175 °C de Si(Ge) sur des substrats de Si (100), et montrons leurs bonnes performances électriques en réalisant des cellules solaires à hétérojonctions avec un absorbeur épitaxié de 1.5 µm ayant un $V_{OC}$ jusqu'à 0.57 V. Ensuite, les premiers stades de l'hétéroépitaxie de Si sur GaAs par PECVD sont étudions par diffraction des rayons X par rayonnement synchrotron. Nous trouvons un comportement inattendu : le Si est relâché dès les premiers nanomètres, mais sa maille est tétragonale. Il présente un $a_{\perp}$ élevé, que l'on attribue à la présence d'hydrogène dans la couche. Le faible $a_{//}$ est attribué à une contrainte thermique induite par le substrat GaAs. L'hydrogène joue aussi un rôle dans le GaAs : nous trouvons que le niveau de dopage dans le GaAs est diminué d'un ordre de grandeur lorsqu'il est exposé à un plasma d'hydrogène. En parallèle, nous développons par MOVPE des jonctions tunnel en matériaux III-V. En particulier, le dopage n du GaAs au tellurium avec le précurseur DIPTe permets de réaliser des jonctions tunnel avec des courants pic atteignant jusqu'à 3000 A/cm$^2$, rejoignant ainsi les résultats de l'état de l'art.
De plus, nous développons la croissance des matériaux pour réaliser une cellule solaire en AlGaAs, ainsi que le design et les étapes technologiques en salle blanche. Nous réalisons ainsi des cellules $Al_{0.22}Ga_{0.78}As$ à l'état de l'art atteignant une efficacité de 17.6 %.
Enfin, une dernière étape de la fabrication du dispositif est étudiée : le report sur un substrat hôte. Nous montrons que l'on peut reporter une cellule simple inversée en AlGaAs sur du Si, retirer le substrat GaAs et effectuer les étapes de microfabrication sur 2 pouces. Après avoir fait croître la structure d'une cellule tandem complète avec 1 µm de Si, nous étudions le collage ainsi que le retrait du substrat de cette cellule solare tandem en Si/AlGaAs.

**Title :** III-V/Si tandem solar cells: an inverted metamorphic approach using low temperature PECVD of c-Si(Ge) on GaAs

**Keywords :** Epitaxy, PECVD, MOVPE, Heteroepitaxy, Tandem Solar Cells, III-V/Si, Tunnel Junctions

**Abstract:** This thesis focuses on an innovative way of fabricating III-V/Si tandem solar cells with an inverted metamorphic approach using low temperature (<200°C) PECVD. The realization of the final tandem solar cell made of SiGe/AlGaAs requires the development and optimization of various building blocks.
First, we develop the epitaxy at 175°C of Si(Ge) on (100) Si substrates and show promising electrical performances of such grown Si(Ge) by realizing heterojunction solar cells with 1.5 µm epitaxial absorber leading to a $V_{oc}$ up to 0.57V. Then, the hetero-epitaxy of Si on GaAs by PECVD is studied, and the first stages of the growth are investigated by X-ray diffraction with synchrotron beam. We find an unexpected behavior: the grown Si is fully relaxed, but tetragonal. The high $a_{\perp}$ is attributed to the high hydrogen content, and the low a// to the thermal strain induced by the GaAs substrate. Also, we found that hydrogen plays a strong role in GaAs: its doping level is decreased by one order of magnitude when exposed to a $H_2$ plasma
Meanwhile, tunnel junctions are developed, and in particular the n-doping of GaAs with tellurium by MOVPE. The high doping levels achieved lead to state-of-the-art tunnel junction with peak tunneling currents up to 3000 A/cm$^2$.
Furthermore, we develop materials for AlGaAs solar cells by MOVPE, as well as their full grid design and process flow in clean rooms. We reach state-of-the art efficiency of 17.6 % for a $Al_{0.22}Ga_{0.78}As$ solar cell, being thus suitable for its integration in the tandem solar cell.
Finally, the last step of device fabrication is studied: the bonding on a host substrate. We successfully bond an inverted AlGaAs cell, remove it from its substrate, and process a full 2" wafer. We succeed in growing our first tandem solar cells by growing thick layers (> 1 µm) of Si on inverted AlGaAs solar cells followed by a TJ, and we study the bonding and substrate removal of this final Si/AlGaAs device.

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